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CHIPLETS SOLUTIONS FOR CUSTOM IC

Design Workshop

April 22nd and 23rd, 2026 – Seattle, WA – USA

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Keynote Speakers

Dr. Amit Khanna

GlobalFoundries

Silicon Photonics, Complexity Scaling

Roadmapping Advanced Packaging Technologies for Heterogeneous Integration

Dr. Ravi Mahajan

intel

CHISIC 2026 Full Program

CICC - CHISIC Joint Paper Session			Wed, Apr 22nd, 2026	Author	Affiliation
10:05	10:55	Paper	***Toward Open-Source Chiplets for HPC and AI: Occamy and Beyond***	**Paul Scheffler**	**ETH Zurich**
10:55	11:20	Paper	***A 5nm 91.43 TOPS/W 4-Chiplet Generalizable-Rendering-Processor with UCIe-Enabled Cross-Die-Cache and Balance-Aware Progressive Multi-Level Sparsity***	**Mr. Yonghao Tan**	**Hong Kong University of Science and Technology**
11:20	11:45	Paper	***A 51.19 mm2, 4 TB/s bandwidth 3D Logic-on-SRAM Stacking CGRA Chip***	**Dr. Zizheng Dong**	**Shanghai Jiao Tong University**
11:45	13:30		*Lunch Break*		
CHISIC			***Wed, Apr 22nd, 2026***		
13:30	14:30	Tutorial	***Seamless 3DIC Design Flow: From Netlist Creation to Verification with Innovator 3DIC Integrator and Calibre 3DSTACK***	**Mr. Justin Locke**	**Siemens**
14:30	15:30	Tutorial	***Thermal and power integrity for 3D/2.5D chiplets***	**Dr. Lang Lin**	**Synopsys - Ansys**
15:30	15:45		*Coffee Break*		
15:45	16:45	Tutorial	***A Ring Resonator-Based Dense Wavelength Division Multiplexed Clock-Forwarded Optical Link***	**Dr. Angad Rekhi**	**Nvidia**
16:45	17:25	Tutorial	***UCIe™ Overview and Recent Advancements***	**Dr. Zuoguo (Joe) Wu**	**Intel**
17:25	17:35		*Break*		
17:35	18:35	CHISIC Keynote	***Silicon Photonics, Complexity Scaling***	**Dr. Amit Khanna**	**GlobalFoundries**
18:35	20:35		*Networking & Exhibits*		
CHISIC			***Thu, Apr 23rd, 2026***		
7:00	8:00		*Breakfast*		
8:00	9:00	CHISIC Keynote	***Roadmapping Advanced Packaging Technologies for Heterogeneous Integration***	**Dr. Ravi Mahajan**	**Intel**
9:00	9:50	Invited Talk	***Energy-Efficient Die-to-Die Transceiver Architectures***	**Dr. Sam Palermo**	**Texas A&M**
9:50	10:20		*Extended Coffee Break*		
10:20	11:10	Invited Talk	***Heterogeneous FPGA and Chiplet Multi-Chip Packaged Devices***	**Mr. Carmine Pagano**	**Altera**
11:10	12:00	Invited Talk	***Integrated Vertical Power Delivery Technologies for Heterogeneous Integrated High-Performance Computing Systems***	**Dr. Hanh-Phuc Le**	**UCSD**
12:00	12:05		*Group Pictures*		
12:05	13:05		***Lunch Break & Panel: Breaking Down Chiplet Barriers: 100x Reach Optical Integration for AI-Scale Disaggregation***	**Dr. Emily Naviasky**	**IBM**
13:05	13:55	Invited Talk	***Enforcing Transparency in the Supply Chain of Chiplets***	**Dr. Sylvain Guilley**	**Cadence / Secure-IC**
13:55	14:45	Invited Talk	***Packaging Technology for Next Generation mmWave Systems - Scalable Heterogeneous AiP Modules and the Future Role of Chiplets***	**Dr. Alberto Valdes-Garcia**	**IBM**
14:45	15:00		*Coffee Break*		
15:00	15:50	Invited Talk	***Deploying Chiplet Interfaces at Scale for AI***	**Mr. Anwar Kashem**	**AMD**
15:50	16:00		***Closing ceremony***		

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Roadmapping Advanced Packaging Technologies for Heterogeneous Integration

Dr. Ravi Mahajan

intel

ABSTRACT: Heterogeneous Integration (HI) is a powerful and crucial enabler for the continued growth of computing and communication performance. Advanced packaging technologies are critical enablers of HI because of their importance as compact, power efficient platforms. This talk will focus on the tremendous opportunities in different application environments and the projected evolution of advanced packaging architectures. Interest in HI research and development has picked up in recent years and this opens up greater collaboration opportunities between academia and industry. A broad scope roadmap of the future generated as part of an industry-academic collaboration will be discussed in this context to highlight the directions, challenges and opportunities generated by HI with a focus on interconnect scaling, thermal management and manufacturability.

BIO: Ravi Mahajan is an Intel Fellow and Director of Assembly and Packaging Technology Pathfinding. Ravi holds the original patents for silicon bridges that became the foundation for Intel's EMIB technologyHis contributions during his Intel career have earned him numerous industry honors, including the SRC's 2015 Mahboob Khan Outstanding Industry Liaison Award, the 2016 THERMI Award from SEMITHERM, the 2016 Allan Kraus Thermal Management Medal & the 2018 InterPACK Achievement award from ASME, the 2019 "Outstanding Service and Leadership to the IEEE" Awards from IEEE Phoenix Section & Region 6, the 2020 Richard Chu ITherm Award and the 2020 ASME EPPD Excellence in Mechanics Award. He is one of the founding editors for the Intel Assembly and Test Technology Journal (IATTJ) and currently VP of Publications & Managing Editor-in-Chief of the IEEE Transactions of the CPMT. He is a Distinguished Lecturer for the IEEE Electronics Packaging Society. Ravi is a Fellow of two leading societies, ASME and IEEE. He was elected to the National Academy of Engineering in 2022 for contributions to advanced microelectronics packaging architectures and their thermal management.

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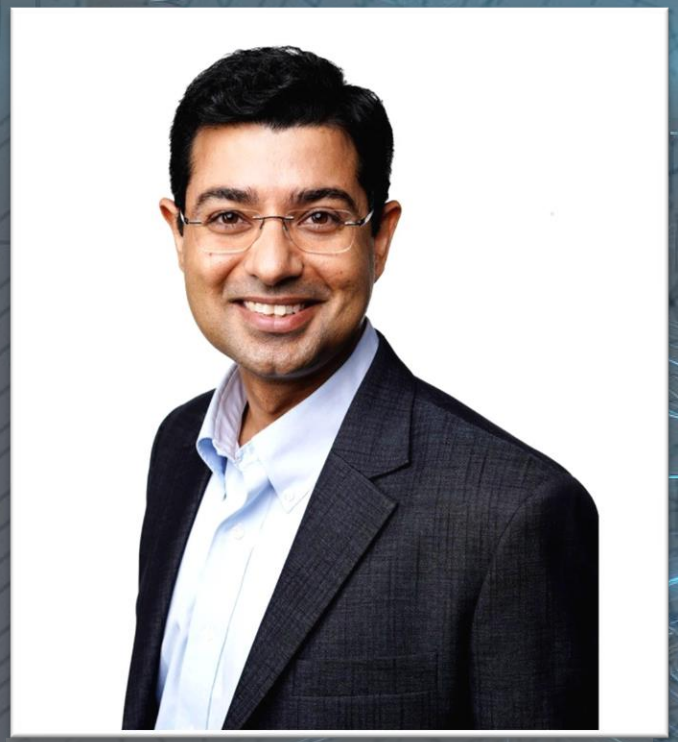
Silicon Photonics, Complexity Scaling



Dr. Amit Khanna

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ABSTRACT: The silicon photonics industry is undergoing standardization and maturity resulting in an emergence of an ecosystem. The driving forces are the increasing market demand, and economics of scale offered by the Silicon platform. This keynote explores increasing complexity in silicon photonics systems related to – design, data rate evolution curves, and advanced packaging architectures.

BIO Amit Khanna is a silicon photonics technology and business leader with deep experience spanning academic research, semiconductor manufacturing, photonic platform development, and related business management. His work focuses on CMOS integrated photonics, and scalable foundry processes for high performance optical interconnects. He has contributed to leading research groups at Aalto University and Ghent University–imec, and has supported commercial photonics deployment through roles in global semiconductor and optics organizations such as Broadcom, Elenion Technologies (now Nokia), and now at Global Foundries. Khanna's work continues to advance next generation photonic integrated circuits and the broader ecosystem enabling high bandwidth, energy efficient optical communication.

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Seamless 3DIC Design Flow: From Netlist Creation to Verification with Innovator 3DIC Integrator and Calibre 3DSTACK

Justin Locke

SIEMENS

ABSTRACT: Navigating the complexities of 3DIC integration requires efficient tools for design and verification. This presentation offers a practical demonstration of how Siemens EDA tools streamline the entire 3DIC system-level design process. We will showcase Innovator 3DIC Integrator for importing device data, defining and optimizing a system-level netlist, and managing design changes as source definitions evolve. The session will conclude with a demonstration of 3DIC Layout Versus Schematic (LVS) verification using Calibre 3DSTACK, ensuring design accuracy and reliability. Attendees will gain valuable insights into building a more efficient, error-resistant, and agile 3DIC design and verification workflow.

BIO: Justin Locke is an Application Engineering Manager with 7 years of dedicated experience within the 3DIC team at Siemens EDA. Throughout his career, Justin has focused on empowering engineers to tackle the intricate challenges of 3DIC integration, specializing in advanced design and verification methodologies. His expertise lies in optimizing complex multi-die systems and ensuring design integrity through the effective application of cutting-edge tools like Innovator 3DIC Integrator and Calibre 3DSTACK.

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Towards Multiphysics Integrity simulation of mega-scale 3DIC

Dr. Lang Lin

SYNOPSYS®

ABSTRACT: The relentless drive for higher performance, energy efficiency, and functional density has accelerated the adoption of 3DICs into the next-generation datacenter system and edge AI devices. As device dimensions scale and integration complexity reaches the mega-scale beyond hundreds of chiplets, ensuring system reliability requires a holistic approach that accounts for the interplay of multiple physical domains. This presentation introduces a framework for multiphysics integrity simulation that integrates electrical, thermal, mechanical, and reliability analyses into a unified methodology. A tutorial of Synopsys EDA tools using such a framework will demonstrate a practical EMIR, thermal and structural integrity flow of a complicated 2.5D/3D heterogeneous integration system.

BIO: Dr. Lang Lin is a principal product manager of Synopsys Inc. based in California. He is dedicated into deploying power integrity, thermal integrity and IC security verification methodologies to the worldwide semiconductor customers to achieve IC product success. He holds a doctorate degree in electrical and computer engineering from University of Massachusetts with research expertise in low-power design, side-channel analysis, and hardware security. He has co-authored 30+ technical papers and patents, including the best paper award of IEEE HOST, DAC and the CEO innovation award of Ansys TechCon.

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Dr. Angad Rekhi

NVIDIA

A Ring Resonator-Based Dense Wavelength Division Multiplexed Clock-Forwarded Optical Link

ABSTRACT: The growth of data centers to meet the ever-increasing demand from AI training and inference has highlighted the limitations of traditional electrical links in terms of density, reach, and energy efficiency. Optical links hold the potential to alleviate these bottlenecks. In this talk, we review how integrating the optical engine onto the same interposer as the host ASIC presents a compelling solution for the required interconnect scaling. We then motivate the use of dense wavelength-division multiplexing (DWDM) as an architecture choice that can meet required density and energy efficiency targets. Finally, we cover the design and measurement of a 32Gb/s/λ DWDM bandpass-filtered clock-forwarding optical link featuring 9 200GHz-spaced wavelengths (8 for data and 1 for clk), achieving a throughput of 256Gb/s/fiber, an energy efficiency of ~2.78pJ/b, and an area efficiency of 1.33Tbps/mm2, with 0.46UI-wide eye openings at <1E-11 BER.

BIO: Angad Rekhi (Member, IEEE) received the B.S. degree in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2014 and the M.S and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, USA, in 2016 and 2020, respectively. He is currently a Senior Research Scientist with the Circuits Research Group, NVIDIA, Inc., Santa Clara, CA, USA. His research interests include electrical and optical high-speed links, mixed-signal approaches for machine learning acceleration, and thermal-aware chip design. Angad was a recipient of the NSF GRFP in 2014, the NDSEG Fellowship in 2016, the ADI Outstanding Student Designer Award in 2014 and 2018, and the IEEE SSCS Predoctoral Achievement Award in 2019.

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UCIe Overview and Recent Advancements

Dr. Zuoguo Wu

intel

ABSTRACT: This tutorial presents a comprehensive analysis of Universal Chiplet Interconnect Express (UCIe) electrical links, covering the evolution from initial implementations up to 32 GT/s through recent advancements at 48 and 64 GT/s data rates. Drawing from the authors' direct involvement in UCIe standard development, we examine the circuit progression enabling these high-speed interconnects, signal integrity optimization, and power efficiency improvements across generations. Reliability analysis through failure probability distributions, and error management strategies for fault-tolerant operation are also covered. Additionally, we explore UCIe-3D as an orthogonal advancement, discussing its unique design considerations in 3D chiplet architectures.

BIO: Zuoguo (Joe) Wu is a Senior Principal Engineer at Intel, where he manages an I/O circuits and architecture team working on the latest interfaces. He currently serves as Co-Chair of the UCIe Consortium Electrical Working Group. He has led the development of UCIe electrical PHY and authored the electrical specification since its inception. He is also a key contributor to every generation of the PCIe specification since 3.0. He holds 171 patents worldwide and has published over 50 external and Intel-internal papers. He received a PhD in EE from Texas A&M University and a BS in Physics from University of Science and Technology of China.

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Energy-Efficient Die-to-Die Transceiver Architectures

Dr. Samuel Palermo

TEXAS A&M UNIVERSITY

ABSTRACT: Chip-to-chip I/O bandwidth demand has increased dramatically due to data-intensive applications and AI workloads. The rise of chiplet-based system-in-package architectures with 2.5D and 3D integration necessitates energy-efficient die-to-die transceivers that achieve very high bandwidth density for communication between XPUs and memory. This talk gives an overview of energy-efficient die-to-die transceivers that achieve very high bandwidth density (>1Tbps/mm and >10Tbps/mm2). Advanced transceiver architectures, signaling approaches, and circuit design techniques will be covered.

BIO: Samuel Palermo (S'98–M'07–SM'17) received his B.S. and M.S. degrees in electrical engineering from Texas A&M University in 1997 and 1999, and his Ph.D. in electrical engineering from Stanford University in 2007. He began his career at Texas Instruments, designing mixed-signal ICs for high-speed serial communication, and later worked at Intel on high-speed optical and electrical I/O architectures. In 2009, he joined the Electrical and Computer Engineering Department at Texas A&M University, where he is now the J. W. Runyon Jr. Professor. His research focuses on high-speed electrical and optical interconnects, RF photonics, advanced clocking circuits, and radiation-hardened design. Dr. Palermo received the 2013 NSF CAREER Award and is a member of Eta Kappa Nu and IEEE. He has served as an associate editor for multiple IEEE journals and as a distinguished lecturer. His work has earned several best-paper awards, and he has received multiple faculty honors from Texas A&M University.

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Heterogeneous FPGA & Chiplet Multichip Packaged Devices

Carmine Pagano

altera

ABSTRACT: This talk describes six Heterogeneous Multichip Packaged (MCP) devices integrating state of the art RF Data Converter chiplets in the same package with a leading-edge Field Programmable Gate Array (FPGA) device and High Speed Serdes chiplets. Three different highly complex chiplets are utilized across three FPGA families using three different semiconductor process nodes. The concept of producing a complicated chiplet function and being able to reuse this chiplet in different package configurations and carrying these chiplets forward by combining them with newer FPGA device nodes is very compelling. This paper will discuss the MCP different topologies built and the benefits of reusing complicated chiplets in regards to validation, package layout, software/IP support and time to market.

BIO: Carmine is a Systems Architect and the Engineering Technical Director in the Aerospace Defense & Government Division of Altera. Carmine supports the definition and execution of Heterogeneous Multichip Packages (MCPs) as well as the Heterogeneous MCP device roadmap. Carmine has worked for Altera (formerly Intel's FPGA division) for 10 years, initially as a DSP & Mixed Signal Specialist before assuming his current Technical Director role in March 2022.

Carmine has held individual contributor and managerial roles at AT&T Bell Laboratories, Lucent Technologies, Broadcom, Andrew/Commscope, ALU/Nokia, Intel & Altera. Carmine's background is in the areas of Digital Signal Processing, Mixed Signal devices, FPGA design and ASIC design with experience in RF systems and Optical Communications. Carmine has a BSEE degree from the University of Pittsburgh and a MSEE from Columbia University and holds 11 US patents.

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Integrated Vertical Power Delivery Technologies for Heterogenous Integrated High-Performance Computing Systems

Dr. Hanh-Phuc Le

UC San Diego

ABSTRACT: The semiconductor industry is increasingly leveraging Heterogeneous Integration (HI) to maximize performance density in next-generation microelectronics—specifically for AI/ML, data centers, and autonomous systems. To sustain this trajectory, vertical power delivery must evolve to meet stringent demands for efficiency, footprint, and reliability. These challenges are compounded by the need to support multiple supply rails and high current densities across significant voltage gaps. In this talk, the speaker explores high-potential power management strategies, including innovative converter topologies, new integrated passive devices (IPDs), emerging active processes, and advanced packaging. The presentation will feature recent design examples from the speaker's research group, alongside key advancements from both academia and industry.

BIO: Dr. Hanh-Phuc Le is an Associate Professor of ECE at UC San Diego and co-Director of the NSF Power Management Integration Center. In 2012, he co-founded Lion Semiconductor to commercialize his doctoral research on switched-capacitor DC-DC converters. The company's technology powered over 200 million fast-charging ICs for leading mobile manufacturers before its acquisition by Cirrus Logic in 2021. Dr. Le's career includes roles at Intel, Oracle, Rambus, and CU Boulder. He has authored over 70 publications and holds 24 U.S. patents. A recipient of the 2021 NSF CAREER Award, he is an IEEE Senior Member and has held leadership roles in the IEEE Power Electronics Society (PELS) in addition to serving as a member of the Steering Committee of the International Workshop on Power Supply On Chip (PwrSoC) since 2021. His current research focuses on miniaturized power conversion and smart delivery for high-performance computing, automotive, wearable, healthcare, and IoT applications.

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Panel: Breaking Down Chiplet Barriers: 100x Reach Optical Integration for AI-Scale Disaggregation

ABSTRACT: Chiplet integration is widely discussed as a practical path to higher yield, faster product cadence, and heterogeneous composition; in AI, its value is increasingly determined by the AI memory wall, the imbalance where peak computation (FLOP/s) has far outpaced data movement through the memory and interconnect stack (token latency and energy/token). The imbalance widens further as advances such as Mixture-of-Experts routing and reasoning-style inference further increase memory communication demand. Mainstream I/O approaches such as Co-Packaged Optics and copper have improved package-to-package bandwidth density by relying on higher-speed SerDes, but incur compounding latency and power penalties when inference quality of service is most sensitive. To go beyond package-to-package, a wafer-scale optical interposer using many parallel low loss waveguides fed by directly modulated micro-VCSELs and terminated by waveguide-integrated photodetection can support direct chip-to-chip optical links at 100X the reach of UCIE (2 mm vs 200 mm) and, subsequently, 50X larger disaggregated memory pools with uniform low access latency at UCIE-class bandwidth density and energy/bit. Massively parallel VCSEL-waveguide links eliminate the overhead (power, complexity, packaging) of external lasers, leverage smartphone-class VCSEL foundries, and support wide and efficient optical links that satisfy performance, bandwidth density and energy/bit requirements more stringent than co-packaged approaches. Reframing the optics discussion from a faster lane to the interconnect/memory boundary facilitates the co-optimization of architecture, reliability, packaging, and link design for concurrent reduced latency and high memory capacity and bandwidth.

Moderator

Dr. Emily Naviasky

IBM

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Enforcing transparency in the supply chain of chiplets

Dr. Sylvain Guilley

ABSTRACT: In an open market, a massive amount of chiplets will arise from various provenances. How to ascertain that they are genuine? How to ensure that they won't be counterfeited? In this presentation, I will advocate that ecosystem coordination is required. Trust in the chiplets model requires that IP can be traced. Hence the need for an industry-level transparency in the sourcing. For such a vision to become concrete, chiplets shall be considered as roots of trust. Concrete solutions will be put forward, building on open standards.

BIO: Sylvain Guilley is Fellow at Cadence, within the Silicon Solution Group. Prior to this position, he was co-founder & CTO at Secure-IC, a company acquired by Cadence in 2025. Sylvain is also adjunct professor at Telecom Paris, and research associate at Ecole Normale Superieure (ENS). He is lead editor of international standards, such as ISO/IEC 20897 (Physically Unclonable Functions), ISO/IEC 20085 (Calibration of non-invasive testing tools), and ISO/IEC TR 24485 (White Box Cryptography). As administrator of Embedded France professional association, he leads the cybersecurity working group. Sylvain has co-authored 350+ research papers and filed 40+ invention patents.

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Packaging Technology for Next Generation mmWave Systems - Scalable Heterogeneous AiP Modules and the Future Role of Chiplets

Dr. Alberto Valdes-Garcia

IBM

ABSTRACT: This talk presents an overview of emerging packaging technology trends for mmWave communications with a focus on design and integration methodologies for scalable phased array antenna modules. The presentation will first describe a heterogeneous integration strategy used to facilitate the effective integration of various active ICs, passive components, and decoupling capacitors into a substrate to form a 5G scalable phased array antenna module. The design is based on a 64-element antenna-in-package tile designed using an organic substrate. Each tile uses chips in different substrate technologies to perform beamforming, frequency conversion, filtering, combining/splitting, and supply decoupling functions. Design, assembly, and over-the-air characterization results will be provided. The talk will also discuss the anticipated advantages of adopting a chiplet-based approach for digital baseband processing enabling the implementation of full end-to-end antennas-to-AI systems mmWave systems for communications and sensing.

BIO: Alberto Valdes-Garcia received the Ph.D. degree in E.E. from Texas A&M University in 2026. He is currently Principal Research Scientist, and Manager at the IBM T. J. Watson Research Center. In this role, he leads a multi-disciplinary team in the development of vertically-integrated antennas-to-AI systems that enable new capabilities for millimeter-wave communications and sensing. He also contributes to the development Si-based RF electronics for scalable quantum computing. He holds >140 issued U.S. patents and has co-authored >150 peer-reviewed publications. He currently serves in the Editorial Board of the IEEE Journal of Microwaves and in the Technical Program Committee of the International Solid-State Circuits Conference. He is a Fellow of the IEEE.

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Deploying Chiplet Interfaces at Scale for AI

Anwar Kashem

AMD

ABSTRACT: AI accelerators demand modularity, bandwidth, and power efficiency that push chiplet and chip to chip interfaces to the available technological limits. This talk examines architectural integration challenges across Packaging, PHY, link, protocol, and system management layers. We'll cover requirements of advanced packaging; clocking and synchronization across heterogeneous dies; signal integrity and power delivery at extreme I/O; and security and reliability at die boundaries. We'll also examine partitioning trade-offs, verification and interoperability, and thermal and mechanical co-design, concluding with practical design patterns and test strategies for scalable multi-die systems.

BIO: Anwar Kashem holds the position of CVP I/O Architecture at AMD, responsible for I/O subsystems and chiplet interconnect. He has extensive design experience designing the PHY, Logical, and Controller layers for high-speed parallel interfaces including GDDR, HBM, LPDDR, DDR, UCIe, and proprietary chiplet interfaces. Anwar has received B.S. (2002) and M.S. (2004) degrees from Cornell University. Prior to AMD, he was responsible for several families of DPUs and RAN accelerators at Marvell and Memory interface IP at Synopsys.

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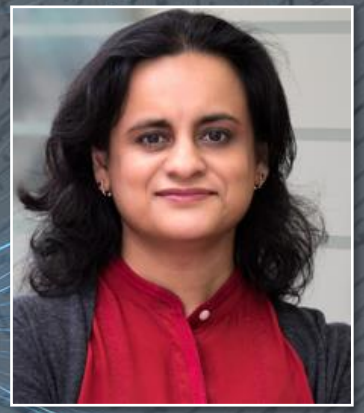

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Chip to Chip Communication for Next Generation AI Datacenters

Dr. Tom Gray

NVIDIA

ABSTRACT: AI applications on GPU systems have exploded with single-chip inference performance increasing 1000X over the last 10 years. Tens of thousands of datacenter connected GPUs are needed for training and inference of state-of-the-art generative AI models. Bandwidth density requirements increase on the order of 2x in each generation. At the core of these systems, processors and switches are implemented as multiple die in 2.5D and 3D configurations. Ultra efficient interconnect between these die in the system is required to support the overall system bandwidths. This talk will look at state-of-the-art current and future electrical and optical chip-to-chip communication from the standpoint of circuits, packaging, power delivery, and thermal management targeting energy efficiencies <100fJ/b and bandwidth density >10Tbps/mm.

BIO: C. Thomas Gray received the B.S. degree in computer science and mathematics from Mississippi College, Clinton, MS, USA, and the M.S. and Ph.D. degrees in computer engineering from North Carolina State University, Raleigh, NC, USA. He worked in a variety of different roles at IBM, Cadence Design Systems, Artisan/ARM, and Nethra Imaging in the Raleigh/Durham, NC, USA, area primarily as a SerDes System Architect. His work experience includes digital signal processing design and CMOS implementation of DSP blocks as well as high-speed serial link communication systems, architectures, and implementation. In 2011, he joined NVIDIA, Inc., Durham, NC, USA, where he is currently Senior Director of Circuit Research, leading activities related to high-speed electrical signaling, photonics, power delivery, security circuits, low-energy and resilient memories, circuits for machine learning, and variation-tolerant clocking and power delivery.

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Petascale photonic connectivity for energy efficient computing

Prof. Keren Bergman

Columbia University

ABSTRACT: High-performance systems are increasingly bottlenecked by the energy and communications costs of interconnecting numerous compute and memory resources. Current systems face a gap of nearly two orders of magnitude between on-chip, intra-socket, communication capacities, and the capacities of links transporting data over longer distances. The per bit energy cost of data movement dominates that of data processing, as does density, throughput, and latency. Integrated silicon photonics offer the opportunity of optical connectivity that delivers high off-chip communication bandwidth densities with low power consumption. To realize these benefits the co-integration of photonics with the compute and memory is critical. This talk will cover approaches for leveraging photonic IO that can scale to realize Petabit/s chip escape bandwidths with sub-picojoule/bit energy consumption, as well as new architectural approaches that enable flexible connectivity tailored to accelerate distributed AI/ML applications.

BIO: Keren Bergman is the Charles Batchelor Professor of Electrical Engineering at Columbia University where she also serves as the Faculty Director of the Columbia Nano Initiative. Bergman received the B.S. from Bucknell University in 1988, and the M.S. in 1991 and Ph.D. in 1994 from M.I.T. all in Electrical Engineering. At Columbia, Bergman leads the Lightwave Research Laboratory encompassing multiple cross-disciplinary programs at the intersection of computing and photonics. Since 2023 Bergman is the Director of the Center for Ubiquitous Connectivity (CUbiC), a 5-year multi-university center funded by DARPA and the Semiconductor Research Corporation (SRC) under the Joint University Microelectronics Program 2.0 (JUMP 2.0). Bergman serves on the Leadership Council of the American Institute of Manufacturing (AIM) Photonics leading projects that support the institute's silicon photonics manufacturing capabilities and Datacom applications. She is the recipient of the IEEE Photonics Engineering Award and is a Fellow of Optica and IEEE.

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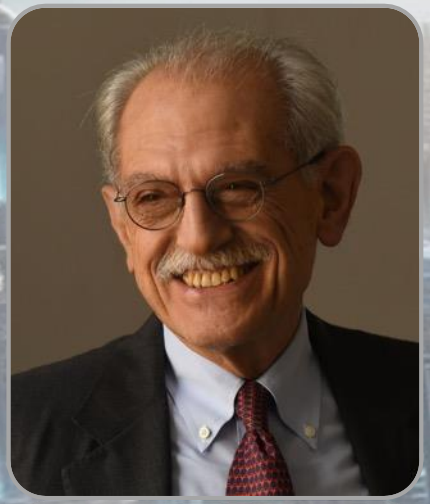

Prof. A. Sangiovanni-Vincentelli (UCB)
- Keynote Speaker -

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