



IEEE CICC 2026 Call for Papers

Regular Paper Submission Opens: 8 September 2025

Regular Paper Submission FIRM Deadline: 17 November 2025

2026 IEEE Custom Integrated Circuits Conference (CICC)

Sponsored by the IEEE Solid-State Circuits Society
and the IEEE Circuits and Systems Society

April 19 – 23, 2026 – Seattle, WA, USA

Submission of original unpublished work in following areas:

Analog Circuits and Techniques encompass circuits characterized by analog-dominated innovation, featuring building blocks such as amplifiers, comparators, frequency generation (oscillators and PLL) and clocking circuits, dividers, filters, references, nonlinear signal processing circuits, digitally-assisted analog circuits, sensor interface circuits.

Biomedical Technologies and Applications focus on biomedical circuits, systems, and applications including but not limited to neural interfaces, microarrays, lab-on-a-chip, bio-inspired circuits, implantable and/or wearable systems, neuromodulation, electroceuticals, closed-loop systems with sensing and actuation, medical imaging, biotelemetry systems, bio-energy harvesting/scavenging systems, body area sensor networks for wireless health monitoring, biomedical signal processing SoCs, AI/ML techniques for mixed-signal biomedical applications, brain computer interfaces, and other biosensors.

Data Converters include a range of innovative converters, such as Nyquist and oversampled A/D, D/A, time-to-digital, frequency-to-digital, and analog-to-information converters of all types driven by innovative techniques, architectures, technologies or applications.

Digital Circuits welcome papers with IC prototypes in technologies that enhance the efficiency, performance, reliability, or integrity of integrated systems. Areas of interest include but are not limited to processors, accelerators, interconnect fabrics, communication SoCs, memory, and in-memory computing. Foundational hardware design building blocks, and associated techniques to demonstrate novel circuits in relevant technology nodes are encouraged. Holistic innovations such as hardware-software codesign, advancement in cloud and edge computing, and autonomy are also of interest.

Emerging Technologies, Systems, and Applications solicit hardware-focused papers exploring the technologies of tomorrow spanning from new devices and circuits to advanced applications. Topics of interest include next-generation technology for MEMS, THz, flexible, printed, large-area, and organic electronics, as well as emerging computing paradigms such as photonic and quantum computing hardware.

Systems and Security seek papers on the latest advancements in system and platform design as well as hardware security. For the security category, contributions are invited on topics covering innovative security primitives, circuit-level attack/defense mechanisms, and approaches to secure system designs. Relevant topics on system platforms include large-scale SoCs and FPGA-based designs, large-scale RISC-V platforms and neuromorphic platforms. Papers related to novel work on chiplets like 2.5D/3D chiplets, system-in-package (SiP), system-on-interposer, novel methodologies and EDA for system and platform design, test, packaging, power and thermal and cross-disciplinary approaches bridging design, manufacturing, and system integration will be selected for a special session with the CHISIC Design Workshop.

Power Management solicit circuits and design techniques in areas including switched-mode integrated converters with inductive, capacitive, and hybrid architectures, 3D power delivery for high performance computing and chiplets, energy harvesting, wireless power transfer, isolated power, power management for automotive applications. Relevant topics also include linear regulators and digital LDOs, circuit with novel wide-bandgap devices and drivers,

battery chargers, supply modulators, and innovative methods to enhance overall system energy efficiency and performance.

Wireless Transceivers and RF/mm-Wave Circuits and Systems cover applications from IoT and cellular (5G, LTE-M, NB-IoT) to vehicle-to-vehicle (V2V), WLAN, THz systems, and integrated sensing-communication systems. Papers should focus on low-power, high-performance links, design-technology co-optimization, agile spectrum management, AI/ML-assisted designs, novel RF front-ends, frequency synthesis, and LO generation.

Wireline and Optical Communication Circuits and Systems welcome papers on serial/parallel data links for intra-chip/chip-to-chip/die-to-die interconnections, memory/graphics interfaces, backplanes, silicon-photonics optical communications, 2.5/3D interconnects, and chiplet-based packaging solutions. Additionally papers on novel I/O circuits, signaling methods, CDRs, equalizers, ADC/DAC/DSP-based transceivers, and electro-optical interface circuitry for pluggable and co-packaged optics are of interest.

Conference Technical Sessions and Events

Technical Sessions addressing a broad range of circuits, applications, design techniques, reliability, emerging technologies, and providing exposure to novel, state-of-the-art developments are the core of the CICC technical program.

Educational Sessions, led by distinguished invited speakers from both industry and academia, are included in the conference. These sessions provide valuable opportunities to refresh key skills in traditional circuit-design methods and acquire knowledge.

Panels, Forums and Keynote Sessions provide a platform for leaders from industry and academia to highlight new development directions and debate key issues and controversial topics.

Chiplets Solutions for Custom IC (CHISIC) Design Workshop is co-located with CICC as a platform for professionals and researchers to advance and grow the chiplet ecosystem.

Our **Welcome Reception** and **Keynote Luncheon** provide additional opportunities for discussion and peer networking.

Paper Submission

Regular Technical Session Papers are **4 pages** in length. Papers should be camera-ready and submitted electronically in PDF format using the CICC website instructions (www.ieee-cicc.org). **Please follow the instructions on the submission website to provide a blind version for review and a complete version for publication.** Appropriate company and government clearances **MUST** be obtained prior to submission. Papers must report **original unpublished work** and concisely explain how the state-of-the-art is advanced, and include measured experimental results that substantiate performance claims. **FIRM DEADLINE for paper submission is 11:59 pm PT on 17 November 2025.** Authors of accepted papers will be notified by email by **13 January 2026**. Top-rated papers will be invited to special issues in the **IEEE Journal of Solid-State Circuits, IEEE Solid-State Circuits Letters, and IEEE Transactions on Biomedical Circuits and Systems.**

For more information, please visit www.ieee-cicc.org.

General Chair: Nan Sun, *Tsinghua University*:

sunnansunny@gmail.com

Conference Chair: Carlos Tokunaga, *Intel*: c.tokunaga@ieee.org

Technical Program Chairs:

Ulkuhan Guler, *WPI*: uguler@wpi.edu

Shenggao Li, *TSMC*: shenggao.li@gmail.com