Sunday, 23 April

9am	**Educational Session 1** *Salon A*
9am	**Educational Session 2** *Salon B*
9am	**Educational Session 3** *Salon C*
9am	**Educational Session 4** *Salon F*
12:15pm	**Break**
12:15pm	**Break**
12:15pm	**Break**
12:15pm	**Break**
1:30pm	**Educational Session 1** *Salon A*
1:30pm	**Educational Session 2** *Salon B*
1:30pm	**Educational Session 3** *Salon C*
1:30pm	**Educational Session 4** *Salon F*

Monday, 24 April

8am	**Welcome and Opening Remarks** *Salon C*
8:20am	**Session 1: Keynote Session** *Salon C*
8:20am	**TBD** » Daniel Cooley (United States)[1] (1. Chief Technology Officer, Silicon Labs)
9:30am	**Digital Circuits, SoCs, and Systems I - Session 2: Low-power Digital Circuits** *Salon A* Chaired by: Alicia Klinefelter (United States) and Weiwei Shan (China)
9:30am	**Introduction: Low-power Digital Circuits** » Alicia Klinefelter (United States)[1], WeiWei Shan (China)[2] (1. nVidia, 2. Southeast University, Nanjing)
9:35am	**2-1: A 28nm All-Digital, 1.92-7.32mV/LSB, 0.5-2GS/s sample rate, 0-latency Voltage Sensor with Dynamic PVT Calibration for Wide-range Adaptive Voltage Scaling** » Yuxuan Du (China)[1], Haitao Ge (China)[1], Zhuo Chen (China)[1], Kaize Zhou (China)[1], Zhengguo Shen (China)[1], Weiwei Shan (China)[1] (1. Southeast University, Nanjing)
10am	**2-2: (Invited) Synchronous Die-to-Die Signaling Using Aeonic Connect** » Marcus van Ierssel (Canada)[1], Fred Buhler (United States)[1], David Moore (United States)[1], Jeff Fredenburg (United States)[1] (1. Movellus Inc)

Continued from **Monday, 24 April**

10:50am

2-3: A 65nm 2.02mW 50Mbps Direct Analog to MJPEG Converter for Video Sensor Nodes using low-noise Switched Capacitor MAC-Quantizer with automatic calibration and Sparsity-aware ADC

» Gaurav Kumar K (United States)[1], Gourab Barik (United States)[1], Baibhab Chatterjee (United States)[2], Sumon Bose (United States)[3], Shovan Maity (United States)[3], Shreyas Sen (United States)[1] (1. Purdue University, 2. University of Florida, 3. Quasistatics Inc)

11:15am

2-4: A 40nm 0.35V 25MHz Half-Select Disturb-Free Bit-interleaving 10T SRAM With Data-Aware Write-Path

» Yifei Li (China)[1], Jian Chen (China)[1], Yuqi Wang (China)[1], Zihan Yin (United States)[2], Hongyu Chen (China)[3], Yajun Ha (China)[1] (1. ShanghaiTech University, 2. USC, 3. Innovation Academy for Microsatellites)

9:30am

Session 3: Forum: Ultra High-Speed Data Converters

Salon B

9:30am

Power Management I -
Session 4: Gate Drivers and GaN ICs

Salon C

Chaired by: Alan Roth (United States) and Raveesh Magod Ramakrishna (United States)

9:30am

Introduction: Gate Drivers and GaN ICs

» Alan Roth (United States)[1], Raveesh Magod (United States)[2] (1. TSMC, 2. Texas Instruments)

9:35am

4-1: (Invited) Digital Gate ICs for Driving and Sensing Power Devices to Achieve Low-Loss, Low-Noise, and Highly Reliable Power Electronic Systems

» Dibo Zhang (Japan)[1], Kohei Horii (Japan)[1], Katsuhiro Hata (Japan)[1], Makoto Takamiya (Japan)[1] (1. The University of Tokyo)

10:25am

4-2: A Monolithic GaN Driver and GaN Power Switch with Power-rail Charging Saturation Bootstrap Technique Achieving Gate Rising and Falling Time Ratio of 1.28

» Yao Qin (China)[1], Xin Ming (China)[1], Zhi-yi Lin (China)[1], Zhijiu Wu (China)[1], Chunwang Zhuang (China)[1], Jian-Jun Kuang (China)[1], Peng Luo (China)[2], Bo Zhang (China)[1] (1. University of Electronic Science and Technology of China, 2. Chengdu Danxi Technology Co., Ltd)

10:50am

4-3: (Invited) A GaN-on-Si Gate Driver with 14.7X Reduction in Tailing Current Loss and 37.0% Reduction of Reverse Conduction Loss

» Hsing-Yen Tsai (Taiwan)[1], Kuo-Lin Zheng (Taiwan)[2], Ke-Horng Chen (Taiwan)[1], Ying-His Lin (Taiwan)[3], Shian-Ru Lin (Taiwan)[3], Tsung-Yen Tsai (Taiwan)[3] (1. National Yang Ming Chiao Tung University, 2. National Yang Ming Chiao Tung University & Chip-GaN Power Semiconductor Corp., 3. Realtek Semiconductor Corp.)

9:30am

Wireless Transceivers and RF/mm-Wave Circuits and Systems I -
Session 5: Low Power Quantum Computing & Wireless Transceivers

Salon E

Chaired by: Julian Tham (United States) and Mustafijur Rahman (India)

9:30am

Introduction: Low Power Quantum Computing & Wireless Transceivers

» Julian Tham (United States)[1], Mustafijur Rahman (India)[2] (1. Infineon Technologies, 2. IIT Delhi)

9:35am

5-1: (Invited) Low power cryogenic RF ASICs for quantum computing

» David Frank (United States)[1], Sudipto Chakraborty (United States)[1], Kevin Tien (United States)[1], Pat Rosno (United States)[2], Mark Yeck (United States)[1], Joseph Glick (United States)[1], Raphael Robertazzi (United States)[1], Ray Richetta (United States)[3], John Bulzacchelli (United States)[1], Daniel Ramirez (United States)[3], Dereje Yilma (United States)[3], Andy Davies (United States)[3], Rajiv Joshi (United States)[1], Scott Lekuch (United States)[1], Ken Inoue (United States)[1], Devin Underwood (United States)[1], Dorothy Wisnieff (United States)[1], Chris Baks (United States)[1], John Timmerwilke (United States)[1], Peilin Song (United States)[1], Blake Johnson (United States)[1], Brian Gaucher (United States)[1], Daniel Friedman (United States)[1] (1. IBM T.J. Watson Research Center, 2. IBM Systems, 3. IBM Systems)

Continued from **Monday, 24 April**

10:25am

5-2: A -102dBm Sensitivity, 2.2µA Packet-Level-Duty-cycled Wake-Up Receiver with ADPLL achieving -30dB SIR

» Linsheng Zhang (United States)[1], Divya Duvvuri (United States)[1], Suprio Bhattacharya (United States)[1], Anjana Dissanayake (United States)[1], Xinjian Liu (United States)[1], Henry Bishop (United States)[1], Yaobin Zhang (United States)[1], Travis Blalock (United States)[1], Benton Calhoun (United States)[1], Steven Bowers (United States)[1] (1. University of Virginia)

10:50am

5-3: A 12.2µW Interference Robust Wake-Up Receiver

» Hamid Jafari Sharemi (Iran, Islamic Republic of)[1], Mehrdad Sharif Bakhtiar (Iran, Islamic Republic of)[1] (1. Sharif University of Technology)

11:15am

5-4: A Digital-Intensive 6-to-11 GHz 1T2R IEEE 802.15.4/4z-Compliant Multi-Functional Joint-Radar-Communication Transceiver SoC for Wireless Indoor Sensing Data-fusion

» Bufan Zhu (China)[1], Wei Deng (China)[1], Ziying Huang (China)[1], Haikun Jia (China)[1], Haiyang Jia (China)[1], Angxiao Yan (China)[1], Yumeng Yang (China)[1], Junfeng Liu (China)[1], Yu Fu (China)[1], Shiyan Sun (China)[1], Chao Tang (China)[1], Taikun Ma (China)[1], Jiajie Tang (China)[1], Baoyong Chi (China)[1] (1. Tsinghua University)

9:30am

Emerging Technologies, Systems, and Applications I - Session 6: Architectures for Advancing Computing

Salon F

Chaired by: Shih-Chii Liu (Switzerland) and Kaiyuan Yang (United States)

9:30am

Introduction: Architectures for Advancing Computing

» Shih-Chii Liu (Switzerland)[1], KaiYuan Yang (United States)[2] (1. ETH, 2. Rice University)

9:35am

6-1: A 333TOPS/W Logic-Compatible Multi-Level Embedded Flash Compute-In-Memory Macro with Dual-Slope Computation

» Edward Choi (Korea, Republic of)[1], Injun Choi (Korea, Republic of)[1], Vincent Lukito (Korea, Republic of)[1], Dong-Hwi Choi (Korea, Republic of)[1], Donghyeon Yi (Korea, Republic of)[1], Ik-joon Chang (Korea, Republic of)[2], Sohmyung Ha (United Arab Emirates)[3], Minkyu Je (Korea, Republic of)[1] (1. Korea Advanced Institute of Science and Technology, 2. Kyung Hee University, 3. New York University Abu Dhabi)

10am

6-2: Sub-mW/qubit 5.2-7.2GHz 65nm Cryo-CMOS RX for Scalable Quantum Computing Applications

» Aravind Nagulu (United States)[1], Leonardo M Ranzani (United States)[2], Guilhem J Ribeill (United States)[2], Martin V Gustafsson (United States)[2], Thomas A Ohki (United States)[2], Harish Krishnaswamy (United States)[3] (1. Washington University in St. Louis, 2. Raytheon BBN Technologies, 3. Columbia University)

10:25am

6-3: A 138-TOPS/W Delta-Sigma Modulator-Based Variable-Resolution Activation In-Memory Computing Macro

» Vasundhara Damodaran (United States)[1], Ziyu Liu (United States)[1], Jae-sun Seo (United States)[1], Arindam Sanyal (United States)[1] (1. Arizona State University)

10:50am

6-4: DenseCIM: Binary Weighted-Capacitor SRAM Computation-In-Memory with Column-by-Column Dynamic Range Calibration SAR ADC

» Yong-Jun Jo (Singapore)[1], Boon Peng Yap (Singapore)[1], Dong-Hyun Yoon (Singapore)[1], Hyunjoon Kim (Singapore)[1], Yuanjin Zheng (Singapore)[1], Tony Tae-Hyoung Kim (Singapore)[1] (1. Nanyang Technological University)

Continued from **Monday, 24 April**

11:15am

6-5: dToF LIDAR System Using Addressable Multi-Channel VCSEL Transmitter, 128x80 SPAD Sensor, and ML-Based Object Detection for Adaptive Beam-Steering

» Yifan Wu (China)[1], Sifan Zhou (China)[2], Miao Sun (China)[3], Tao Xia (China)[3], Jian Qian (China)[3], Lei Wang (China)[4], Shi Shi (China)[4], Lebei Cui (China)[3], Jier Wang (China)[3], Yuan Li (China)[3], Hengwei Yu (China)[3], Zhihong Lin (China)[3], Lei Qiu (China)[1], Yajie Qin (China)[3], Min Sun (China)[5], Rui Bai (China)[4], Xuefeng Chen (China)[4], Patrick Chiang (China)[3], Shenglong Zhuo (China)[3] (1. The college of electronics and information engineering, Tongji University, Shanghai, China;, 2. Southeast University, Nanjing, 3. State Key Laboratory of ASIC and System, Fudan University, Shanghai, China, 4. PhotonIC Technologies, Shanghai, China, 5. Tencent Research)

1pm

Digital Circuits, SoCs, and Systems II -
Session 7: Compute in Memory and Ising Machines
Salon A
Chaired by: Bongjin Kim (United States) and Yongpan Liu (China)

1pm

Introduction: Compute in Memory and Ising Machines

» Bongjin Kim (United States)[1], Yongpan Liu (China)[2] (1. University of California, Santa Barbara, 2. Tsinghua University)

1:05pm

7-1: A Calibration-Free 15-level/Cell eDRAM Computing-in-Memory Macro with 3T1C Current-Programmed Dynamic-Cascoded MLC achieving 233-to-304-TOPS/W 4b MAC

» Jiahao Song (China)[1], Xiyuan Tang (China)[1], Haoyang Luo (China)[1], Haoyi Zhang (China)[1], Xin Qiao (China)[1], Zixuan Sun (China)[1], Xiangxing Yang (United States)[2], Yuan Wang (China)[1], Runsheng Wang (China)[1], Ru Huang (China)[1] (1. Peking University, 2. pSemi Corporation)

1:30pm

7-2: CIMC: A 603TOPS/W In-Memory-Computing C3T Macro with Boolean/Convolutional Operation for Cryogenic Computing

» Yuhao Shu (China)[1], Hongtu Zhang (China)[1], Qi Deng (China)[1], Hao Sun (China)[1], Yajun Ha (China)[1] (1. ShanghaiTech University)

1:55pm

7-3: A Double-Mode Sparse Compute-In-Memory Macro with Reconfigurable Single and Dual Layer Computation

» Yuanzhe ZHAO (Macao)[1], Minglei Zhang (Macao)[1], Pengyu He (Macao)[1], Yan Zhu (Macao)[1], Chi-Hang Chan (Macao)[1], R. P. Martins (Macao)[1] (1. University of Macau)

2:20pm

7-4: A Graph Neural Network Computing-in-Memory Macro and Accelerator with Analog-Digital Hybrid Transformation and CAM-enabled Search-reduce

» Yipeng Wang (United States)[1], Shanshan Xie (United States)[1], Jacob Rohan (United States)[1], Meizhi Wang (United States)[1], Mengtian Yang (United States)[1], Sirish Oruganti (United States)[1], Jaydeep P Kulkarni (United States)[1] (1. University of Texas at Austin)

1pm

Data Converters I -
Session 8: Data Converter Design Techniques
Salon B
Chaired by: Shaolan Li (United States) and Zhichao Tan (China)

1pm

Introduction: Data Converter Design Techniques

» Shaolan Li (United States)[1], Zhichao Tan (China)[2] (1. Georgia Institute of Technology, 2. Zhejiang University)

1:05pm

8-1: (Best Invited Paper Candidate) Calibration Techniques for Optimizing Performance of High-Speed ADCs

» Ewout Martens (Belgium)[1], Nereo Markulic (Belgium)[1], Jorge Lagos Benites (Belgium)[1], Jan Craninckx (Belgium)[1] (1. IMEC)

1:55pm

8-2: (Best Student Paper Candidate) A 4.6K to 400K Functional PVT-Robust Ringamp-Based 250MS/s 12b Pipelined ADC with Pole-Aware Bias Calibration

» Kaoru Yamashita (Japan)[1], Benjamin Hershberg (United States)[1], Kentaro Yoshioka (Japan)[1], Hiroki Ishikuro (Japan)[1] (1. Keio University)

2:20pm

8-3: A 1GS/s 6-Core Programmable A/D Converter Array Supporting Architecture Restructuring and Multitasking

» Zhishuai Zhang (China)[1], Zijie Gao (China)[1], Siyu Huang (China)[1], Nan Sun (China)[1], Lu Jie (China)[1] (1. Tsinghua University)

Continued from **Monday, 24 April**

1pm **Power Management II -**
Session 9: DC-DC Converters
Salon C
Chaired by: John Pigott (United States) and SriHarsh Pakala (United States)

1pm **Introduction: DC-DC Converters**
» John Pigott (United States)[1], SriHarsh Pakala (United States)[1] (1. NXP)

1:05pm **9-1: 4C 3-Level Hybrid Buck Converter for 12~48V-to-1V Point-of-Load Applications**
» Hon-Piu Lam (Hong Kong)[1], Wing-Hung Ki (Hong Kong)[1], Philip K. T. Mok (Hong Kong)[1] (1. Hong Kong University of Science and Technology)

1:30pm **9-2: A 4-to-42V Input, 95.5% Efficiency, 3.2μA-IQ, DC-DC Buck Converter Featuring a Leakage-Emulated Bootstrap Refresher and Anti-Deadlock Self-Bias Supply for Battery-Powered Automotive Uses**
» Heejun Lee (Korea, Republic of)[1], Hyunki Han (Korea, Republic of)[1], Hyun-Sik Kim (Korea, Republic of)[1] (1. KAIST)

1:55pm **9-3: An 87.2%-peak efficiency 4.1W-output power switched capacitor 3-level inverting buck-boost dc-dc converter**
» Samuele Fusetto (Italy)[1], Elisabetta Moisello (Italy)[1], Holger Petersen (Germany)[2], Siamak Abedinpour (United States)[2], Piero Malcovati (Italy)[1], Edoardo Bonizzoni (Italy)[1] (1. University of Pavia, 2. Renesas Electronics)

2:20pm **9-4: (Best Student Paper Candidate) A Li-ion Battery Input 96.8% Peak Efficiency Single-Inductor Off-Chip-Capacitor-Free 2-Switch LED Driver with Two-Color Mixing Capability**
» Caiyu Tong (China)[1], Zihao Fan (China)[1], Yuan Gao (China)[1] (1. Southern University of Science and Technology)

1pm **Wireless Transceivers and RF/mm-Wave Circuits and Systems II -**
Session 10: Recent Advances in Silicon Based Terahertz Solutions
Salon E
Chaired by: Sudipto Chakraborty (United States) and Wanghua Wu (United States)

1pm **Introduction: Recent Advances in Silicon Based Terahertz Solutions**
» Sudipto Chakraborty (United States)[1], Wanghua Wu (United States)[2] (1. IBM, 2. Samsung)

1:05pm **10-1: (Invited) High-Power, Efficient THz Generation in Silicon for Broadband Sensing and Wireless Communication**
» Aydin Babakhani (United States)[1], Sidharth Thomas (United States)[1], Sam Razavian (United States)[1] (1. University of California, Los Angeles)

1:55pm **10-2: A 194-238GHz Fully On-Chip Self-Referenced Frequency Stabilized Radiator for High Range Resolution Imaging**
» Bahareh Hadidian (United States)[1], Farzad Khoeini (United States)[1], S. M. Hossein Naghavi (United States)[1], Andreia Cathelin (France)[2], Kamal Sarabandi (United States)[1], Ehsan Afshari (United States)[1] (1. University of Michigan, Ann Arbor, 2. STMicroelectronics, Crolles)

2:20pm **10-3: A Compact CMOS 390 GHz Autodyne FMCW Radar with 57 GHz Bandwidth for Dental Imaging**
» Morteza Tavakoli Taba (United States)[1], S. M. Hossein Naghavi (United States)[1], Morteza Fayazi (United States)[1], Ali Sadeghi (United States)[2], Mohammed Aseeri (Saudi Arabia)[3], Andreia Cathelin (France)[4], Ehsan Afshari (United States)[1] (1. University of Michigan, Ann Arbor, 2. University of Washington, 3. King Abdulaziz City for Science and Technology, 4. STMicroelectronics, Crolles)

1pm **Analog Circuits and Techniques I -**
Session 11: Analog Sensor Interfaces
Salon F
Chaired by: Edoardo Bonizzoni (Italy) and DEVRIM AKSIN (United States)

1pm **Introduction: Analog Sensor Interfaces**
» Edoardo Bonizzoni (Italy)[1], Devrim Aksin (United States)[2] (1. University of Pavia, 2. ADI)

Continued from **Monday, 24 April**

1:05pm **11-1: A 72-Channel Resistive-and-Capacitive Sensor Interface Achieving 0.74μW/Channel and 0.038mm2/Channel by Noise-Orthogonalizing and Pad-Sharing Techniques**

» Xiangdong Feng (China)[1], Yuxuan Luo (China)[1], Tianyi Cai (China)[1], Yangfan Xuan (China)[1], Yunshan Zhang (China)[1], Yili Shen (China)[1], Changgui Yang (China)[1], Qijing Xiao (China)[1], Yong Chen (Macao)[2], Bo Zhao (China)[1] (1. Zhejiang University, 2. University of Macau)

1:30pm **11-2: A 15.5b-ENOB 335mVpp-Linear-Input-Range 4.7GΩ-Input-Impedance Direct-ADC Based Analog Front-End**

» Yijie Li (China)[1], Weiqi Zhi (China)[1], Yuying Li (China)[1], Zhiliang Hong (China)[1], Jiawei Xu (China)[1] (1. Fudan University)

1:55pm **11-3: A 0.06-mm² Current-Mode Noise-Shaping SAR based Temperature-to-Digital Converter with a 4.9-nJ Energy/Conversion**

» Antonio Aprile (Italy)[1], Daniele Gardino (Italy)[2], Michele Folz (Italy)[2], Piero Malcovati (Italy)[1], Edoardo Bonizzoni (Italy)[1] (1. University of Pavia, 2. TDK InvenSense)

2:20pm **11-4: A 9.7fJ/Conv.-Step Capacitive Sensor Readout Circuit with Incremental Zoomed Time Domain Quantization**

» Zilong Shen (China)[1], Xiyuan Tang (China)[1], Zhongyi Wu (China)[1], Haoyang Luo (China)[1], Zongnan Wang (China)[1], Mingjie Liu (United States)[2], Xing Zhang (China)[1], Yuan Wang (China)[1] (1. Peking University, 2. NVIDIA Corporation)

2:45pm **Break**

2:45pm **Break**

2:45pm **Break**

2:45pm **Break**

2:45pm **Break**

3pm **Digital Circuits, SoCs, and Systems II cont'd -**
Session 7: Compute in Memory and Ising Machines
Salon A
Chaired by: Bongjin Kim (United States) and Yongpan Liu (China)

3pm **7-5: A 65 nm 1.4-6.7 TOPS/W Adaptive-SNR Sparsity-Aware CIM Core with Load Balancing Support for DL workloads**

» Mustafa Ali (United States)[1], Indranil Chakraborty (United States)[1], Sakshi Choudhary (United States)[1], Dong Eun Kim (United States)[1], Muya Chang (United States)[2], Arijit Raychowdhury (United States)[2], Kaushik Roy (United States)[1] (1. Purdue University, 2. Georgia Institute of Technology)

3:25pm **7-6: iMCU: A 102-μJ, 61-ms Digital In-Memory Computing-based Microcontroller Unit for Edge TinyML**

» Chuan-Tung Lin (United States)[1], Paul Huang (United States)[1], Jonghyun Oh (United States)[1], Dewei Wang (United States)[1], Mingoo Seok (United States)[1] (1. Columbia University)

3:50pm **7-7: A Continuous-Time Ising Machine Using Coupled Inverter Chains Featuring Fully-Parallel One-Shot Spin Updates**

» Chengshuo Yu (Singapore)[1], JUNJIE MU (Singapore)[1], Kevin Chai (Singapore)[2], Tony Tae-Hyoung Kim (Singapore)[1], Bongjin Kim (United States)[3] (1. Nanyang Technological University, 2. Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), 3. University of California, Santa Barbara)

4:15pm **7-8: A Reconfigurable Ising Machine for Boolean Satisfiability Problems Featuring Many-Body Spin Interactions**

» Yuqi Su (Singapore)[1], Tony Tae-Hyoung Kim (Singapore)[1], Bongjin Kim (United States)[2] (1. Nanyang Technological University, 2. University of California, Santa Barbara)

3pm **Data Converters I cont'd -**
Session 8: Data Converter Design Techniques
Salon B
Chaired by: Shaolan Li (United States) and Zhichao Tan (China)

Continued from **Monday, 24 April**

3pm

8-4: An 80.2-to-89.1dB-SNDR 24k-to-200kHz-BW VCO-Based Synthesized ΔΣ ADC with 105dB SFDR in 28-nm CMOS

» Yi Zhong (China)[1], Mingtao Zhan (China)[1], Wei Wang (China)[1], Xiyuan Tang (China)[2], Lu Jie (China)[1], Nan Sun (China)[1] (1. Tsinghua University, 2. Peking University)

3:25pm

8-5: Sniff-SAR: A 9.8fJ/c.-s 12b secure ADC with detection-driven protection against power and EM side-channel attack

» Ruicong Chen (United States)[1], Anantha P. Chandrakasan (United States)[1], Hae-Seung Lee (United States)[1] (1. Massachusetts Institute of Technology)

3:50pm

8-6: A Fully-Dynamic kT/C-Noise-Canceled SAR ADC with Trimming-Free Dynamic Amplifier

» Haoyu Zhuang (China)[1], Nan Sun (China)[2], Linzhi Tao (China)[1], Yizhan Li (China)[1], Qiang Li (China)[1] (1. University of Electronic Science and Technology of China, 2. Tsinghua University)

3pm

Power Management II cont'd -

Session 9: DC-DC Converters

Salon C

Chaired by: John Pigott (United States) and SriHarsh Pakala (United States)

3pm

9-5: A 150nA IQ, 850mA ILOAD, <10mV Ripple Buck Converter with >90% Efficiency over 10µA to 450mA Loading Range

» Baochuang Wang (China)[1], Yiling Xie (China)[1], Jianping Guo (China)[1], Lin Cheng (China)[2] (1. Sun Yat-sen University, 2. University of Science and Technology of China)

3:25pm

9-6: A 5V-to-0.5V Inductor-First Inductor-on-Ground Switched Capacitor Multi-Path Hybrid DC-DC Converter

» Junwei Huang (China)[1], Zhiguo Tong (China)[1], Yan Lu (China)[1], Chi-Seng Lam (China)[1], R. P. Martins (China)[1] (1. University of Macau, Macau, China)

3:50pm

9-7: A 96.6%-Efficiency Inductively Assisted Switched-Capacitor DC-DC Converter with 0.5-to-1.5V Output Voltage Range

» Sandeep Reddy Kukunuru (United States)[1], Loai Salem (United States)[1] (1. University of California, Santa Barbara)

4:15pm

9-8: A 65nm Fully-integrated Fast-switching Buck Converter with Resonant Gate Drive and Automatic Tracking

» Xi Chen (United States)[1], Aly Shoukry (United States)[1], Tianyu Jia (United States)[1], Xin Zhang (United States)[2], Raveesh Magod (United States)[3], Nachiket Desai (United States)[4], Jie Gu (United States)[1] (1. Northwestern University, 2. IBM, 3. Texas Instruments, 4. Intel)

4:40pm

9-9: (Best Student Paper Candidate) A Fully-Integrated Direct-Conversion Resonant Switched Capacitor Converter with Modular Multi-Winding Current Ballasting

» Kishalay Datta (United States)[1], Prescott H Mclaughlin (United States)[2], Jason Stauth (United States)[1] (1. Dartmouth, 2. Intel)

3pm

Wireless Transceivers and RF/mm-Wave Circuits and Systems II cont'd -

Session 10: Recent Advances in Silicon Based Terahertz Solutions

Salon E

3pm

10-4: An Ultra-Wideband Amplifier with A Novel Non-Distributed Butterfly Topology Achieving 2-250 GHz Bandwidth and 4.67 THz GBW in 130nm SiGe BiCMOS

» Dawei Tang (China)[1], Zekun Li (China)[1], Jixin Chen (China)[1], Peigen Zhou (China)[1], Zhe Chen (China)[1], Debin Hou (China)[1], Wei Hong (China)[1] (1. Southeast University)

3:25pm

10-5: A Low-Power 20Gb/s 196GHz BPSK Wireless Transmitter with Energy Efficiency FoM of 0.15pJ/bit/cm

» Lili Chen (United States)[1], Morteza Tavakoli Taba (United States)[1], Andreia Cathelin (France)[2], Ehsan Afshari (United States)[1] (1. University of Michigan, Ann Arbor, 2. STMicroelectronics, Crolles)

Continued from **Monday, 24 April**

3:50pm **10-6: (Best Student Paper Candidate) A 1.54mm2 Wake-Up Receiver Based on THz Carrier Wave and Integrated Cryptographic Authentication**

» Eunseok Lee (United States)[1], Muhammad Ibrahim Wasiq Khan (United States)[1], Xibi Chen (United States)[1], Utsav Banerjee (India)[2], Nathan Monroe (United States)[1], Rabia Tugce Yazicigil (United States)[3], Ruonan Han (United States)[1], Anantha P. Chandrakasan (United States)[1] (1. Massachusetts Institute of Technology, 2. Indian Institute of Science, 3. Boston University)

3pm **Session 11: Analog Sensor Interfaces**

Salon F

Chaired by: Edoardo Bonizzoni (Italy) and DEVRIM AKSIN (United States)

3pm **11-5: (Best Invited Paper Candidate) Analog Front-End Circuits for MEMS Microphones**

» Piero Malcovati (Italy)[1] (1. University of Pavia)

3:50pm **11-6: A 3.9kHz bandwidth and 2μV offset current sensor analog front-end with a capacitively coupled amplifier using a dual frequency conversion technique**

» Shotaro Wada (Japan)[1], Yoshikazu Furuta (Japan)[1], Soya Taniguchi (Japan)[1], Masaya Kondo (Japan)[1], Shogo Kawahara (Japan)[1], Tomohiro Nezuka (Japan)[1] (1. MIRISE Technologies Corporation)

4:15pm **11-7: A 56fJ/Conversion-Step 178dB-FoMS Third-Order Hybrid CT-DT ΔΣ Capacitance-to-Digital Converter**

» Yoontae Jung (Korea, Republic of)[1], Jimin Koo (Korea, Republic of)[1], Sein Oh (Korea, Republic of)[1], Seunga Park (Korea, Republic of)[1], Ji-Hoon Suh (Korea, Republic of)[1], Donghee Cho (Korea, Republic of)[1], Minkyu Je (Korea, Republic of)[1] (1. KAIST)

4:40pm **11-8: A 7.4μJ·ppm2 Resistance Sensor with ±120ppm (3σ) 1-Point-Trimmed Inaccuracy and <4ppm/°C Temperature Drift from −55°C to 125°C**

» Sining Pan (China)[1], Ning Pu (China)[1], Haiyu Wang (China)[1], Hanjun Jiang (China)[1], Zhihua Wang (China)[1], Huaqiang Wu (China)[1] (1. Tsinghua University)

5:30pm **Welcome Reception**

River Terrace and Patio

Tuesday, 25 April

8am **Session 12: Forum: Recent Progress in LDOs and Voltage, Current, and Timing References**

Salon A

8am **Session 13: Forum: Emerging Electrical and Optical Devices for Biomedical Applications**

Salon B

8am **Foundation of System Design I -**
Session 14: Heterogenous SoCs for Next-Gen Compute Applications

Salon C

Chaired by: Farhana Sheikh (United States) and Zhengya Zhang (United States) and Jaydeep P Kulkarni (United States)

8am **Introduction: Heterogenous SoCs for Next-Gen Compute Applications**

» Farhana Sheikh (United States)[1], Zhengya Zhang (United States)[2], Jaydeep Kulkarni (United States)[3] (1. Intel, 2. University of Michigan, 3. The University of Texas at Austin)

8:05am **14-1: (Invited) System Aspects of Deploying FPGAs for Cloud Infrastructure**

» Derek Chiou (United States)[1] (1. The University of Texas at Austin and Microsoft)

Continued from **Tuesday, 25 April**

8:55am **14-2: (Best Student Paper Candidate) DECADES: A 67mm2, 1.46TOPS, 55 Giga Cache-Coherent 64-bit RISC-V Instructions per second, Heterogeneous Manycore SoC with 109 Tiles including Accelerators, Intelligent Storage, and eFPGA in 12nm FinFET**

» Fei Gao (United States)[1], Ting-Jung Chang (United States)[1], Ang Li (United States)[1], Marcelo Orenes-Vera (United States)[1], Davide Giri (United States)[2], Paul Jackson (United States)[1], August Ning (United States)[1], Georgios Tziantzioulis (United States)[1], Joseph Zuckerman (United States)[2], Jinzheng Tu (United States)[1], Kaifeng Xu (United States)[1], Grigory Chirkov (United States)[1], Gabriele Tombesi (United States)[2], Jonathan Balkind (United States)[3], Margaret Martonosi (United States)[1], Luca Carloni (United States)[2], David Wentzlaff (United States)[1] (1. Princeton University, 2. Columbia University, 3. University of California, Santa Barbara)

9:20am **14-3: CIFER: A 12nm, 16mm2, 22-Core SoC with a 1541 LUT6/mm2, 1.92 MOPS/LUT, Fully Synthesizable, Cache-Coherent, Embedded FPGA**

» Ting-Jung Chang (United States)[1], Ang Li (United States)[1], Fei Gao (United States)[1], Tuan Ta (United States)[2], Georgios Tziantzioulis (United States)[1], Yanghui Ou (United States)[2], Moyang Wang (United States)[2], Jinzheng Tu (United States)[1], Kaifeng Xu (United States)[1], Paul Jackson (United States)[1], August Ning (United States)[1], Grigory Chirkov (United States)[1], Marcelo Orenes-Vera (United States)[1], Shady Agwa (United States)[2], Xiaoyu Yan (United States)[1], Eric Tang (United States)[2], Jonathan Balkind (United States)[3], Christopher Batten (United States)[2], David Wentzlaff (United States)[1] (1. Princeton University, 2. Cornell University, 3. University of California, Santa Barbara)

8am **Wireless Transceivers and RF/mm-Wave Circuits and Systems III - Session 15: Frequency Generation, Clocking and Power Transfer**

Salon E

Chaired by: Debo Chowdhury (United States) and Renzhi Liu (United States)

8am **Introduction: Frequency Generation, Clocking and Power Transfer**

» Debopriyo Chowdhury (United States)[1], Renzhi Liu (United States)[2] (1. Broadcom, 2. Intel)

8:05am **15-1: (Invited) Wireless Power Transfer at Distance**

» Ali Hajimiri (United States)[1] (1. California Institute of Technology)

8:55am **15-2: A 25.0-to-35.9GHz Dual-Layer Quad-Core Dual-Mode VCO with 189.1dBc/Hz FoM and 200.2dBc/Hz FoMT at 1MHz Offset in 65nm CMOS**

» Pingda Guan (China)[1], Haikun Jia (China)[1], Wei Deng (China)[1], Ruichang Ma (China)[1], Huabing Liao (China)[1], Zhihua Wang (China)[1], Baoyong Chi (China)[1] (1. Tsinghua University)

9:20am **15-3: A 13.5-to-28.8GHz 72.3%-Locking Range Multi-Phase Injection-Locked Frequency Tripler with Improved Output Power and Wideband Subharmonic-Spur Rejection in 28nm CMOS**

» Chao Fan (China)[1], Ya Zhao (China)[1], Yanlong Zhang (China)[1], Jun Yin (China)[2], Pui-In Mak (China)[2], Guohe Zhang (China)[1], Li Geng (China)[1] (1. Xi'an Jiaotong university, 2. University of Macau)

8am **Data Converters II - Session 16: ADCs with Noise Shaping**

Salon F

Chaired by: Seung-Tak Ryu (Korea, Republic of) and Chia-Hung Chen (Taiwan)

8am **Introduction: ADCs with Noise Shaping**

» Seung-Tak Ryu (Korea, Republic of)[1], Chia-Hung Chen (Taiwan)[2] (1. KAIST, 2. National Chiao Tung University)

8:05am **16-1: (Invited) Weightings in Incremental ADCs: A Tutorial Review**

» Ruiqi Gao (Macao)[1], Mingqiang Guo (Macao)[1], Sai-Weng Sin (Macao)[1], Liang Qi (China)[2], Biao Wang (Macao)[1], Guoxing Wang (China)[2], R. P. Martins (Macao)[1] (1. University of Macau, 2. Shanghai Jiao Tong University)

8:55am **16-2: An ELDC-Free 2.78mW 20MHz-BW 75.5dB-SNDR 4th-Order CTSDM Facilitated by 2nd-Order CT NS-SAR and AC-Coupled Negative-R**

» ZiXuan Xu (Macao)[1], Kai Xing (Macao)[1], Yan Zhu (Macao)[1], Chi-Hang Chan (Macao)[1], R. P. Martins (Portugal)[2] (1. University of Macau, 2. Instituto Superior Tecnico/University of Lisboa)

Continued from **Tuesday, 25 April**

9:20am **16-3: An 84dB-SNDR 1-0 Quasi-MASH NS SAR with LSB Repeating and 12-bit Bridge-Crossing Segmented CDAC**
» Zihao Jiao (China)[1], Hongrui Luo (China)[1], Jie Zhang (China)[1], Xiaofei Wang (China)[2], Liang Chen (China)[3], Hong Zhang (China)[1] (1. Xi'an Jiaotong University, 2. Xi'an Jiaotong university, 3. Changzhou Power Supply Company, State Grid Jiangsu Electric Power Company)

9:45am **Break**

9:45am **Break**

9:45am **Break**

10am **Break**

10am **Break**

10am **Foundation of System Design I cont'd -**
Session 14: Heterogenous SoCs for Next-Gen Compute Applications
Salon C
Chaired by: Farhana Sheikh (United States) and Zhengya Zhang (United States) and Jaydeep P Kulkarni (United States)

10am **14-4: (Invited) Open-Source AXI4 Adapters for Chiplet Architectures**
» Nij Dorairaj (United States)[1], David Kehlet (United States)[1], Farhana Sheikh (United States)[2], Julie Zhang (United States)[1], YunHui Huang (United States)[1], Shawn Wang (United States)[1] (1. Intel Corporation, 2. Intel)

10am **Wireless Transceivers and RF/mm-Wave Circuits and Systems III cont'd -**
Session 15: Frequency Generation, Clocking and Power Transfer
Salon E
Chaired by: Debo Chowdhury (United States) and Renzhi Liu (United States)

10am **15-4: An 86.5-105.6GHz LO Generator with Cascaded Implicit Frequency Quintupling and Tripling Achieving -107.7dBc/Hz Phase Noise and 191.2dBc/Hz FoM at 1MHz Offset**
» Hao Guo (United States)[1], Taiyun Chi (United States)[1] (1. Rice University)

10:25am **15-5: A 26GHz Fractional-N Charge-Pump PLL Based on A Dual-DTC-Assisted Time-Amplifying-Phase-Frequency Detector Achieving 37.1fs and 45.6fs rms Jitter for Integer-N and Fractional-N Channel**
» Xinlin Geng (China)[1], Zonglin Ye (China)[1], Yao Xiao (China)[1], Qian Xie (China)[1], Zheng Wang (China)[1] (1. University of Electronic Science and Technology of China)

10:50am **15-6: A 21.8-41.6GHz Fractional-N Sub-Sampling PLL with Dividerless Unequal-REF-Delay Frequency-Locked Loop Achieving −246.9dB FoMj and −270.3dB FoMj,N**
» Wen Chen (China)[1], Yiyang Shu (China)[1], Xun Luo (China)[1] (1. University of Electronic Science and Technology of China)

11:15am **15-7: A 6.5-to-8GHz Cascaded Dual-Fractional-N Digital PLL Achieving -63.7dBc Fractional Spurs with 50MHz Reference**
» Dingxin Xu (Japan)[1], Yuncheng Zhang (Japan)[1], Hongye Huang (Japan)[1], Zheng Sun (Japan)[1], Bangan Liu (Japan)[1], Ashbir Aviat Fadila (Japan)[1], Junjun Qiu (Japan)[1], Zezheng Liu (Japan)[1], Wenqian Wang (Japan)[1], Yuang Xiong (Japan)[1], Waleed Madany (Japan)[1], Atsushi Shirane (Japan)[1], Kenichi Okada (Japan)[1] (1. Tokyo Institute of Technology)

10am **Data Converters II cont'd -**
Session 16: ADCs with Noise Shaping
Salon F
Chaired by: Seung-Tak Ryu (Korea, Republic of) and Chia-Hung Chen (Taiwan)

10am **16-4: A 243µW 97.4dB-DR 50kHz-BW Multi-Rate CT Zoom ADC with Inherent DAC Mismatch Tolerance**
» Junghyun Yoon (Korea, Republic of)[1], MoonHyung Jang (United States)[2], Changuk Lee (United States)[3], Youngcheol Chae (Korea, Republic of)[1], Yong Lim (Korea, Republic of)[4] (1. Yonsei University, 2. Stanford University, 3. University of California, Berkeley, 4. Samsung Electronics)

Continued from **Tuesday, 25 April**

10:25am **16-5: An 81.2dB-SNDR Dual-Residue Pipeline ADC with a 2nd-Order Noise-Shaping Interpolating SAR ADC**

» Jae-Hyun Chung (Korea, Republic of)[1], Ye-Dam Kim (Korea, Republic of)[1], Chang-Un Park (Korea, Republic of)[1], Kun-Woo Park (Korea, Republic of)[1], Min-Jae Seo (Korea, Republic of)[2], Seung-Tak Ryu (Korea, Republic of)[1] (1. KAIST, 2. Gachon University)

10:50am **16-6: Mixed-Order Correlated Dual-loop Sturdy MASH CT ΔΣ Modulator with Distributed Signal Feed-in and VCO quantizer**

» xiaodong xu (United States)[1], Beomsoo Park (United States)[1], Marino Guzman (United States)[1], Nima Maghari (United States)[2] (1. University of Florida, 2. Univeristy of Florida)

11:02am **16-7: A 1-MHz-Bandwidth Continuous-Time Delta-Sigma ADC Achieving >90dB SFDR and >80dB Antialiasing Using Reference-Switched Resistive Feedback DACs**

» Sharvil Patil (Canada)[1], Raviteja Theertham (India)[1], Hajime Shibata (Canada)[1], Victor Kozlov (Canada)[1], Asha Ganesan (Canada)[1], Efram Burlingame (Canada)[1], Zhao Li (Canada)[1], Rama Thakar (United States)[1], Qianqian Zhang (Canada)[1], Yue Yin (United States)[2], Aathreya Bhat (United States)[3] (1. Analog Devices, 2. Meta, 3. NVIDIA Corporation)

10:10am **Analog Circuits and Techniques II - Session 17: Analog Techniques**

Salon A

Chaired by: Mark Stefan Oude Alink (Netherlands) and Antonio Liscidini (Canada)

10:10am **Introduction: Analog Techniques**

» Mark Oude Alink (Netherlands)[1], Antonio Liscidini (Canada)[2] (1. University of Twente, 2. University of Toronto)

10:15am **17-1: A 0.69-Noise-Efficiency-Factor 4x-Current-Reuse Dynamic Comparator with A Stacking FIA**

» Haoyu Zhuang (China)[1], Nan Sun (China)[2], Yirui Cao (China)[1], Linzhi Tao (China)[1], Qiang Li (China)[1] (1. University of Electronic Science and Technology of China, 2. Tsinghua University)

10:40am **17-2: A 69MHz-Bandwidth 40V/µs-Slew-rate 3nV/√Hz-Noise 4.5µV-Offset Chopper Operational Amplifier**

» Yarallah Koolivand (Iran, Islamic Republic of)[1], Yasser Rezayean (Denmark)[2], Milad Zamani (Denmark)[2], Meysam Akbari (Iran, Islamic Republic of)[3], Omid Shoaei (Iran, Islamic Republic of)[4], Kea-Tiong Tang (Taiwan)[5], Farshad Moradi (Denmark)[2] (1. K. N. Toosi University of Technology, 2. Aarhus University, 3. University of Kurdistan, 4. University of Tehran, 5. National Tsing Hua University)

11:05am **17-3: A 92F2/bit Physically Unclonable Function Exploiting Channel Charge Injection and Mismatch Accumulation**

» Injune Yeo (Korea, Republic of)[1], Dong-Woo Jee (Korea, Republic of)[2], Jae-sun Seo (United States)[3] (1. Chosun University, 2. Ajou University, 3. Arizona State University)

10:10am **A-SSCC Best Student Papers**

Salon B

10:10am **A 110-120-GHz, 12.2% Efficiency, 16.2-dBm Output Power Multiplying Outphasing Transmitter in 22-nm FDSOI**

» Jeff Shih-Chieh Chien (United States)[1] (1. University of California, Santa Barbara)

10:30am **A 37-39GHz Phase and Amplitude Detection Circuit with 0.060 degree and 0.043dB RMS Errors for the Calibration of 5GNR Phased-Array Beamforming**

» Yudai Yamazaki (Japan)[1] (1. Tokyo Institute of Technology)

10:50am **A 20-MHz 2.3-mW Receiver and a 25-V Transmitter for Ultrasound Capsule Endoscopy**

» Kyeongwon Jeong (Korea, Republic of)[1] (1. KAIST)

11:10am **A 0.56V/0.8V Vision Sensor with Temporal Contrast Pixel and Column-Parallel Local Binary Pattern Extraction for Dynamic Depth Sensing Using Stereo Vision**

» Min-Yang Chiu (Taiwan)[1] (1. National Tsing Hua University)

11:30am **A 0.95pJ/b 5.12Gb/s/pin Charge-Recycling IOs with 47% Energy Reduction for Big Data Applications**

» Han Wu (Singapore)[1] (1. National University of Singapore)

Continued from **Tuesday, 25 April**

12pm **Session 18: Keynote Luncheon**
Salon D

12pm **Terahertz CMOS Going Anywhere?**
» Kenneth O (United States)[1] (1. Professor - Electrical Engineering, Texas Instruments Distinguished University Chair)

1:45pm **Analog Circuits and Techniques III - Session 19: Timing Circuits**
Salon A
Chaired by: Antonio Liscidini (Canada) and Hiroki Ishikuro (Japan)

1:45pm **Introduction: Timing Circuits**
» Antonio Liscidini (Canada)[1], Hiroki Ishikuro (Japan)[2] (1. University of Toronto, 2. Keio University)

1:50pm **19-1: A 0.012mm2 36.41kHz Temperature-Insensitive Current-Reuse Ring Oscillator Achieving 0.077%/V Line Sensitivity across a 1.3V-to-3.7V Unregulated Supply**
» Zhicheng Dong (China)[1], Shubin Liu (China)[1], Xiaoteng Zhao (China)[1], Baotian Hao (China)[2], Hongzhi Liang (China)[1], Haolin Han (China)[1], Menghao Wang (China)[1], Weijie Han (United States)[3], Zhangming Zhu (China)[1] (1. Xidian University, 2. legendsemi, 3. University of Texas at Dallas)

2:15pm **19-2: A 0.9V 2MHz 6.4x-Slope-Boosted Quadrature-Phase Relaxation Oscillator with 164.2dBc/Hz FoM and 62.5ppm Period Jitter in 0.18µm CMOS**
» Hoyong Seong (Korea, Republic of)[1], Donghyun Youn (Korea, Republic of)[1], Injun Choi (Korea, Republic of)[1], Junghyup Lee (Korea, Republic of)[2], Sohmyung Ha (United Arab Emirates)[3], Minkyu Je (Korea, Republic of)[1] (1. KAIST, 2. DGIST, 3. New York University Abu Dhabi)

2:40pm **19-3: A High-Order-Temperature-Compensated 328kHz On-Chip RC Timer Using Time-Interleaved Resistors Achieving 1.5pJ/Cycle and 5.86ppm/°C**
» Jiawei Liao (Switzerland)[1], Hesam Omdeh Ghiasi (Switzerland)[1], Giorgio Cristiano (Switzerland)[1], Taekwang Jang (Switzerland)[1] (1. ETH Zürich)

3:05pm **19-4: A 16GHz 33fs rms Integrated Jitter FLL-less Gear Shifting Reference Sampling PLL**
» Jusung Lee (Korea, Republic of)[1], Youngwoo Jo (Korea, Republic of)[1], Wonsik Yu (Korea, Republic of)[1], WooSeok Kim (Korea, Republic of)[1], Michael Choi (Korea, Republic of)[1], Sanghune Park (Korea, Republic of)[1], Jongshin Shin (Korea, Republic of)[1] (1. Samsung Electronics)

1:45pm **Digital Circuits, SoCs, and Systems III - Session 20: Machine Learning**
Salon B
Chaired by: Ningyuan Cao (United States) and Behnam Amelifard (United States)

1:45pm **Introduction: Machine Learning**
» Ningyuan Cao (United States)[1], Behnam Amelifard (United States)[2] (1. University of Notre Dame, 2. Qualcomm)

1:50pm **20-1: AI Processor with Sparsity-adaptive Real-time Dynamic Frequency Modulation for Convolutional Neural Networks and Transformers**
» Yugandhar Khodke (United States)[1], Sadhana Shanmugasundaram (United States)[1], Yidong Li (United States)[1], Mingu Kang (United States)[2] (1. University of California san diego, 2. University of california, san diego)

2:15pm **20-2: A 608nW Near-Microphone Keyword-Spotting Chip Using Real-Point Serial FFT-Based MFCC and Temporal Depthwise Separable CNN in 28nm CMOS**
» Cai Li (China)[1], Haochang Zhi (China)[1], Long Chen (China)[1], Kaiyue Yang (China)[1], Junyi Qian (China)[1], Zhihao Yan (China)[1], Lixuan Zhu (China)[1], Weiwei Shan (China)[1] (1. Southeast University)

Continued from **Tuesday, 25 April**

2:40pm **20-3: (Invited) AI SoC Design Challenges in the Foundation Model Era**

» Zhengyu Chen (United States)[1], Dawei Huang (United States)[1], Mingran Wang (United States)[1], Bowen Yang (United States)[1], Jinuk Luke Shin (United States)[1], Changran Hu (United States)[1], Bo Li (United States)[1], Raghu Prabhakar (United States)[1], Gao Deng (United States)[1], Yongning Sheng (United States)[1], Sihua Fu (United States)[1], Lu Yuan (United States)[1], Tian Zhao (United States)[1], Yun Du (United States)[1], Jun Yang (United States)[1], Chen Liu (United States)[1], Viren Shah (United States)[1], Venkat Srinivasan (United States)[1], Sumti Jairath (United States)[1] (1. SambaNova Systems)

1:45pm **Session 21: Mixed-Signal Foundational IPs for Emerging Systems**

Salon C

Chaired by: Siddharth Joshi (United States) and Xuan (Silvia) Zhang (United States) and Jing (Jane) Li (United States)

1:45pm **Introduction: Mixed-Signal Foundational IPs for Emerging Systems**

» Siddharth Joshi (United States)[1], Xuan (Silvia) Zhang (United States)[2], Jing (Jane) Li (United States)[3] (1. University of Notre Dame, 2. Washington University in St. Louis, 3. University of Pennsylvania)

1:50pm **21-1: (Best Invited Paper Candidate) Silicon Process Technology Constraints for Vertical Die-to-Die Interconnects**

» Harrison Liew (United States)[1], Farhana Sheikh (United States)[1], David Kehlet (United States)[1], Borivoje Nikolić (United States)[2] (1. Intel, 2. University of California, Berkeley)

2:40pm **21-2: A 12-ADC 25-Core Smart MPSoC Using ABB in 22FDX for 77GHz MIMO Radars at 52.6mW Average Power**

» Hector Andres Gonzalez Diaz (Germany)[1], Bernhard Vogginger (Germany)[1], Chen Liu (Germany)[1], Marco Stolba (Germany)[1], Florian Kelber (Germany)[1], Heiner Bauer (Germany)[1], Stefan Hänzsche (Germany)[1], Stefan Scholze (Germany)[1], Marc Berthel (Germany)[1], Tim Rosmeisl (Germany)[1], Liyuan Guo (Germany)[1], Dennis Walter (Germany)[1], Piash Das (Germany)[1], Khaleelulla Khan Nazeer (Germany)[1], Tilo Schubert (Germany)[1], Sebastian Höppner (Germany)[1], Christian Mayr (Germany)[1] (1. Technische Universität Dresden)

3:05pm **21-3: A Memristor-Based Analog Accelerator for Solving Quadratic Programming Problems**

» Hsiang-Chun Cheng (United States)[1], Shiyu Su (Canada)[2], Mayank Palaria (United States)[1], Qiaochu Zhang (United States)[1], Ce Yang (United States)[1], Sushmit Hossain (United States)[1], Ryan Bena (United States)[1], Buyun Chen (United States)[1], Zerui Liu (United States)[1], Juzheng Liu (United States)[1], Rezwan Rasul (United States)[1], Quan Nguyen (United States)[1], Wei Wu (United States)[1], Mike Chen (United States)[1] (1. University of Southern California, 2. University of Waterloo)

1:45pm **Session 22: Panel: It's 2023. Where are our self-driving cars?**

Salon E

Chaired by: Tolga Dinc (United States)

1:45pm **Emerging Technologies, Systems, and Applications II - Session 23: Advances in Low-power, High-performance Sensor Interfaces**

Salon F

Chaired by: Chul Kim (Korea, Republic of) and Constantine Sideris (United States)

1:45pm **Introduction: Advances in Low-power, High-performance Sensor Interfaces**

» Chul Kim (Korea, Republic of)[1], Constantine Sideris (United States)[2] (1. KAIST, 2. University of Southern California)

1:50pm **23-1: A CMOS BD-BCI Incorporating Stimulation with Dual-Mode Charge Balancing and Time-Domain Pipelined Recording**

» Haoran Pu (United States)[1], Ahmad Reza Danesh (United States)[1], Mahyar Safiallah (United States)[1], Jeffrey Lim (United States)[1], An H. Do (United States)[1], Zoran Nenadic (United States)[1], Payam Heydari (United States)[1] (1. University of California, Irvine)

2:15pm **23-2: A 1.8V 16µA 136.5dB DR PPG/NIRS Recording IC using Noise Shaping Triple Slope Light to Digital Converter**

» Mengyu Li (China)[1], Shuang Song (China)[1], Dehong Wang (China)[1], Feijun Zheng (China)[1], Tian Yang (China)[1], Yalong Wan (China)[1], Kai Huang (China)[1], Zhichao Tan (China)[1], Menglian Zhao (China)[1] (1. Zhejiang University)

Continued from **Tuesday, 25 April**

2:40pm **23-3: (Best Student Paper Candidate) A 9V-Tolerant 71.4%-Efficiency Stacked-Switched-Capacitor Stimulation System with Level-Adaptive Switching Control and Rapid Stimulus-Synchronized Charge Balancing**

» Minju Park (Korea, Republic of)[1], Kyeongho Eom (Korea, Republic of)[1], Han-Sol Lee (Korea, Republic of)[1], Seung-Beom Ku (Korea, Republic of)[1], Hyung-Min Lee (Korea, Republic of)[1] (1. Korea University)

3:05pm **23-4: (Best Regular Paper Candidate) A 4 kHz, 25 µg/√Hz, 3-Axis MEMS Accelerometer ASIC Using Beyond-Resonant-Frequency Sensing**

» James Lin (United States)[1], Long Pham (United States)[1], Ran Tao (United States)[1], A Gutmann (United States)[1], Shanglin Guo (United States)[1], Adam Cywar (United States)[1], Adam Spirer (United States)[1], Johan Mansson (United States)[1], Khiem Nguyen (United States)[1] (1. Analog Devices)

3:30pm **Break**

3:30pm **Break**

3:30pm **Break**

3:30pm **Break**

3:45pm **Analog Circuits and Techniques III cont'd - Session 19: Timing Circuits**

Salon A

Chaired by: Antonio Liscidini (Canada) and Hiroki Ishikuro (Japan)

3:45pm **19-5: A 100 MHz-Reference, 10.3-to-11.1 GHz Quadrature PLL with 33.7-fsrms Jitter and -83.9 dBc Reference Spur Level using a -130.8 dBc/Hz Phase Noise at 1MHz offset Folded Series-Resonance VCO in 65nm CMOS**

» Shiwei Zhang (China)[1], Wei Deng (China)[1], Haikun Jia (China)[1], Hongzhuo Liu (China)[1], Shiyan Sun (China)[1], Pingda Guan (China)[1], Baoyong Chi (China)[1] (1. Tsinghua University)

4:10pm **19-6: (Best Student Paper Candidate) A 2.6GHz ΔΣ Fractional-N Bang-Bang PLL with FIR-Embedded Injection-Locking Phase-Domain Low-Pass Filter**

» Liqun Feng (China)[1], Woogeun Rhee (China)[1], Zhihua Wang (China)[1] (1. Tsinghua University)

3:45pm **Digital Circuits, SoCs, and Systems III cont'd - Session 20: Machine Learning**

Salon B

Chaired by: Behnam Amelifard (United States) and Ningyuan Cao (United States)

3:45pm **20-4: A 28nm 1.07TFLOPS/mm² Dynamic-Precision Training Processor with Online Dynamic Execution and Multi-Level-Aligned Block-FP Processing**

» Yixiong Yang (China)[1], Ruoyang Liu (China)[1], Chenhan Wei (China)[1], Wenxun Wang (China)[1], Wenyu Sun (China)[1], Jinshan Yue (China)[2], Huazhong Yang (China)[1], Yongpan Liu (China)[1] (1. Tsinghua University, 2. Institute of Microelectronics, Chinese Acadamy of Sciences)

4:10pm **20-5: A 22nm 0.43pJ/SOP Sparsity-Aware In-Memory Neuromorphic Computing System with Hybrid Spiking and Artificial Neural Network and Configurable Topology**

» Ying Liu (China)[1], Zhiyuan Chen (China)[1], Zhixuan Wang (China)[1], Wentao Zhao (China)[1], Wei He (China)[1], Jianfen Zhu (China)[2], Tianyu Jia (China)[1], Qijun Wang (China)[2], Ning Zhang (China)[2], Yufei Ma (China)[1], Le Ye (China)[1], Ru Huang (China)[1] (1. Peking University, 2. Nano Core Chip Electronic Technology)

4:35pm **20-6: A 26.55TOPS/W Explainable AI Processor with Dynamic Workload Allocation and Heat Map Compression/Pruning**

» Junsoo Kim (Korea, Republic of)[1], Geonwoo Ko (Korea, Republic of)[1], Ji-Hoon Kim (Korea, Republic of)[1], Changha Lee (Korea, Republic of)[1], Taewoo Kim (Korea, Republic of)[1], Chan-Hyun Youn (Korea, Republic of)[1], Joo-Young Kim (Korea, Republic of)[1] (1. KAIST)

3:45pm **Session 21: Mixed-Signal Foundational IPs for Emerging Systems**

Salon C

Chaired by: Siddharth Joshi (United States) and Xuan (Silvia) Zhang (United States) and Jing (Jane) Li (United States)

Continued from **Tuesday, 25 April**

3:45pm **21-4: (Invited) Cryogenic CMOS: design considerations for future quantum computing systems**
» Rajiv Joshi (United States)[1], Sudipto Chakraborty (United States)[1] (1. IBM T. J. Watson Research Center)

3:45pm **Emerging Technologies, Systems, and Applications II cont'd - Session 23: Advances in Low-power, High-performance Sensor Interfaces**
Salon F
Chaired by: Constantine Sideris (United States) and Chul Kim (Korea, Republic of)

3:45pm **23-5: (Best Student Paper Candidate) A Monolithic 3D Magnetic Sensor in 65nm CMOS with <10μTrms Noise and 14.8μW Power**
» Saransh Sharma (United States)[1], Hayward Melton (United States)[1], Liliana Edmonds (United States)[2], Olivia Addington (United States)[1], Mikhail Shapiro (United States)[1], Azita Emami (United States)[1] (1. California Institute of Technology, 2. Massachusetts Institute of Technology)

4:10pm **23-6: A 44V Driver Array for Ultrasonic Haptic Feedback in Display Compatible Thin-Film Low Temperature Poly-Silicon**
» Jonas Pelgrims (Belgium)[1], Kris Myny (Belgium)[2], Wim Dehaene (Belgium)[1] (1. MICAS, ESAT, KU Leuven, 2. COSIC diepenbeek, ESAT, KU Leuven)

4:35pm **23-7: A 2.67GΩ 454nVrms 14.9μW Dry-Electrode Enabled ECG-on-Chip with Arrhythmia Detection**
» Xinzi Xu (China)[1], Yanxing Suo (China)[1], Peiyi Zhou (China)[1], Xiao Han (China)[1], Qiao Cai (China)[1], Guoxing Wang (China)[1], Yong Lian (China)[1], Yang Zhao (China)[1] (1. Shanghai Jiao Tong University)

5pm **23-8: A Wireless Implantable Opto-Electro Neural Interface ASIC for Simultaneous Neural Recording and Stimulation**
» Linran Zhao (United States)[1], Raymond Stephany (United States)[1], Yan Gong (United States)[2], Wei Shi (United States)[1], Wen Li (United States)[2], Yaoyao Jia (United States)[1] (1. University of Texas at Austin, 2. Michigan State University)

5:30pm **CICC Conference Reception**
River Terrace and Patio

Wednesday, 26 April

8am **Session 24: Keynote Session**
Salon C

8am **TBD**
» Billy Dally (United States)[1] (1. Chief Scientist, NVIDIA)

8:50am **Coffee Break**

9am **Session 25: Panel: Improving ASIC Productivity**
Salon A
Chaired by: Yingyan Lin (United States)

9am **Session 26: Forum: Standardizing Chiplet Design**
Salon B

9am **Wireless and Optical Communications Circuits and Systems I - Session 27: Advanced Techniques for Wireline Communications**
Salon C
Chaired by: Tzu-Chien Hsueh (United States) and Zhipeng Li (United States)

9am **Introduction: Advanced Techniques for Wireline Communications**
» Tzu-Chien Hsueh (United States)[1], Zhipeng Li (United States)[2] (1. University of California san diego, 2. Marvell)

Continued from **Wednesday, 26 April**

9:05am **27-1: (Invited) Short to Medium-Reach Wireline Transceivers Using Single-Ended Signaling, Clock Forwarding, and Spatial Encoding for Die-to-Die Applications**

» Scott Huss (United States)[1], Chris Moscone (United States)[1], Mark Summers (United States)[1], James Vandersand (United States)[1], Kelvin McCollough (United States)[1], Randall Smith (United States)[1] (1. Cadence Design Systems, Inc)

9:30am **27-2: A 1.6pJ/b 65Gb/s Si-Dielectric-Waveguide based Multi-Mode Multi-Drop sub-THz Interconnect in 65nm CMOS**

» Xuan Ding (United States)[1], Hai Yu (United States)[1], Sajjad Sabbaghi (United States)[1], Qun Jane Gu (United States)[1] (1. University of California Davis)

9:55am **27-3: A 0.99µs FFT-Based Fast-Locking, 0.82GHz-to-4.1GHz DPLL-Based Input-Jitter-Filtering Clock Driver with Wide-Range Mode-Switching 8-Shaped LC Oscillator for DRAM Interfaces**

» Woosong Jung (Korea, Republic of)[1], Hyojun Kim (Korea, Republic of)[1], Yeonggeun Song (Korea, Republic of)[1], Kwang-Hoon Lee (Korea, Republic of)[1], Deog-Kyoon Jeong (Korea, Republic of)[1] (1. Seoul National University)

10:20am **27-4: (Best Regular Paper Candidate) A 3D-integrated 8λ x 32 Gbps/λ Silicon Photonic Microring-based DWDM Transmitter**

» Cooper Levy (United States)[1], Zhe Xuan (United States)[1], Duanni Huang (United States)[1], Ranjeet Kumar (United States)[1], Jahnavi Sharma (United States)[1], Taehwan Kim (United States)[1], Chaoxuan Ma (United States)[1], Guan-Lin Su (United States)[1], Songtao Liu (United States)[1], Jinyong Kim (United States)[1], Xinru Wu (United States)[1], Ganesh Balamurugan (United States)[1], Haisheng Rong (United States)[1], James Jaussi (United States)[1] (1. Intel)

9am **Wireless Transceivers and RF/mm-Wave Circuits and Systems IV -**
Session 28: mm-Wave Transceiver and Front-end Building Blocks for Radar and Communication
Salon E
Chaired by: Yanjie Wang (China) and Ritesh Bhat (United States)

9am **Introduction: mm-Wave Transceiver and Front-end Building Blocks for Radar and Communication**

» Yanjie Wang (China)[1], Ritesh Bhat (United States)[2] (1. South China University of Technology, 2. Intel)

9:05am **28-1: A 52-to-73GHz Tri-Coupled Transformer Based Noise-Self-Canceling and Gm-Boosting LNA with 3.78dB NF and 22.4dB Gain in 40nm CMOS**

» Jiacong Ke (China)[1], Guangyin Feng (China)[1], Yanjie Wang (Canada)[1] (1. South China University of Technology)

9:30am **28-2: A 52-67GHz Ultra-Compact Bi-directional Gate-switching Cascode Amplifier with Tri-coil Broadband Matching in 40-nm CMOS**

» Haoyang Jia (Ireland)[1], Yanjie Wang (China)[2], Anding Zhu (Ireland)[1] (1. University College Dublin, 2. South China University of Technology)

9:55am **28-3: A 38GHz Power-Combined Doherty PA Based on an Extended Rat-Race Coupler Achieving 27.5dBm Saturated Power and 15.0% Efficiency at 6dB Back-Off**

» Xiaohan Zhang (United States)[1], Sensen Li (United States)[2], Taiyun Chi (United States)[1] (1. Rice University, 2. University of Texas at Austin)

10:20am **28-4: An 8-Element 23-40 GHz Continuously Auto Link-Tracking Phased-Array Transceiver with Time Division Modulator Achieving 7µs Tracking Time, 25.3% TX System Efficiency, 800MHz-64QAM Modulation for 5G NR**

» Zhixian Deng (China)[1], Bingzheng Yang (China)[1], Wen Chen (China)[1], Jie Zhou (China)[1], Changxuan Han (China)[1], Yifan Li (China)[1], Yiyang Shu (China)[1], Xun Luo (China)[1] (1. University of Electronic Science and Technology of China)

9am **Data Converters III -**
Session 29: Gigasample-Rate Data Converters
Salon F
Chaired by: Martin Kinyua (United States) and Filip Tavernier (Belgium)

9am **Introduction: Gigasample-Rate Data Converters**

» Martin Kinyua (United States)[1], Filip Tavernier (Belgium)[2] (1. TSMC, 2. Katholieke Universiteit Leuven)

Continued from **Wednesday, 26 April**

9:05am

29-1: A 12-bit 1GS/s Current-Steering DAC with Paired Current Source Switching Background Mismatch Calibration

» Chang-Un Park (Korea, Republic of)[1], Jae-Hyun Chung (Korea, Republic of)[1], Seung-Tak Ryu (Korea, Republic of)[1] (1. KAIST)

9:30am

29-2: A 12b 1GS/s ADC with Lightweight Input Buffer Distortion Background Calibration Achieving >75dB SFDR over PVT

» Xianghui Pan (China)[1], Buhui Rui* (China)[1], Yuefeng Cao (China)[1], Yan Zhu (China)[1], Chi-Hang Chan (China)[1], R. P. Martins (China)[1] (1. University of Macau)

9:55am

29-3: A 2GS/s 8.5-Bit Time-Based ADC Using a Segmented Stochastic Flash TDC

» Shiyu Su (Canada)[1], Qiaochu Zhang (United States)[2], Mike Chen (United States)[2] (1. University of Waterloo, 2. University of Southern California)

10:20am

29-4: A 0.009mm2, 6.5mW, 6.2b-ENOB 2.5GS/s Flash-and-VCO-Based Subranging ADC Using a Resistor-Ladder-Based Residue Shifter

» Jeonghyun Lee (Korea, Republic of)[1], Yoonseo Cho (Korea, Republic of)[1], Jintae Kim (Korea, Republic of)[2], Jaehyouk Choi (Korea, Republic of)[1] (1. Korea Advanced Institute of Science and Technology, 2. Konkuk University)

1pm

Digital Circuits, SoCs, and Systems IV -
Session 30: Hardware Security

Salon A

Chaired by: Shreyas Sen (United States) and Elkim Roa (United States)

1pm

Introduction: Hardware Security

» Shreyas Sen (United States)[1], Elkim Roa (United States)[2] (1. Purdue University, 2. Global Foundries)

1:05pm

30-1: Power and EM SCA Resilience in 65nm AES-256 Exploiting Clock-Slew Dependent Variability in CMOS Digital Circuits

» Archisman Ghosh (United States)[1], Md. Abdur Rahman (United States)[1], Debayan Das (United States)[2], Santosh Ghosh (United States)[2], Shreyas Sen (United States)[1] (1. Purdue University, 2. Intel)

1:30pm

30-2: A 166F2/bit 0.0136%-Native-BER Physically Unclonable Function Based on Gate-Overhang-Shortened Transistor

» Haibiao Zuo (China)[1], Jiacheng Hao (China)[1], Jianlin Zhong (China)[1], Xiaojin Zhao (China)[1] (1. Shenzhen University)

1:55pm

30-3: A 100-Bit-Output Modeling Attack-Resistant SPN Strong PUF with Uniform and High-Randomness Response

» Kunyang Liu (Japan)[1], Yichen Tang (Japan)[1], Shufan Xu (Japan)[1], Ruilin Zhang (Japan)[1], Hirofumi Shinohara (Japan)[1] (1. Waseda University)

1pm

Session 31: Panel: Where is the balance between circuit and system-level innovation in our solid-state circuit conference?

Salon B

Chaired by: Mark Stefan Oude Alink (Netherlands)

1pm

Session 32: Panel: CHIPS Act and Future of Semiconductor Innovation

Salon C

Chaired by: Tod Dickson (United States)

1pm

Power Management III -
Session 33: Energy Harvesting and Wireless/Isolated Power Converters

Salon E

Chaired by: Cheng Huang (United States) and Hyun-Sik Kim (Korea, Republic of)

1pm

Introduction: Energy Harvesting and Wireless/Isolated Power Converters

» Hyun-Sik Kim (Korea, Republic of)[1], Cheng Huang (United States)[2] (1. KAIST, 2. Iowa State University)

Continued from **Wednesday, 26 April**

1:05pm **33-1: A Self-Bias-flip Piezoelectric Energy Harvester Array without External Energy Reservoirs achieving 488% Improvement with 4-Ratio Switched-PEH DC-DC Converter**

» Zhen Li (China)[1], Zhiyuan Chen (China)[1], Man-Kay Law (Macao)[2], Sijun Du (Netherlands)[3], Xu Cheng (China)[1], Xiaoyang Zeng (China)[1], Jun Han (China)[1] (1. Fudan University, 2. University of Macau, 3. Delft University of Technology)

1:30pm **33-2: (Best Student Paper Candidate) SLiMO: A 61.8% Efficiency Single-Link Multiple-Output Isolated DC-DC Converter Using Low-Cost FPC Micro-Transformer with Local Voltage and Global Power Regulation**

» Jiangiang Jiang (United States)[1], Junyao Tang (United States)[1], Lei Zhao (United States)[1], Chenchang Zhan (China)[2], Cheng Huang (United States)[1] (1. Iowa State University, 2. Southern University of Science and Technology)

1:55pm **33-3: A 0.24mm2 Bridge-less Hybrid SSHI Interface Circuit for Piezoelectric Energy Harvesting with a Wide Load Range and Up to 1620% Power-Extraction Improvement**

» Chuhui Wang (China)[1], Dingxuan Zhang (China)[1], Jianping Guo (China)[1] (1. Sun Yat-sen University)

2:20pm **33-4: A 13.56MHz Fully Integrated 91.8% Efficiency Single-Stage Dual-Output Regulating Voltage Doubler for Biomedical Wireless Power Transfer**

» Tiangi Lu (Netherlands)[1], Zu-yao Chang (Netherlands)[1], Junmin Jiang (China)[2], Kofi A. A. Makinwa (Netherlands)[1], Sijun Du (Netherlands)[1] (1. Delft University of Technology, 2. Southern University of Science and Technology)

1pm **Data Converters IV -**
Session 34: SAR-based Gigasample-rate ADCs
Salon F
Chaired by: Martin Kinyua (United States) and Filip Tavernier (Belgium)

1pm **Introduction: SAR-based Gigasample-rate ADCs**

» Martin Kinyua (United States)[1], Filip Tavernier (Belgium)[2] (1. TSMC, 2. Katholieke Universiteit Leuven)

1:05pm **34-1: A 7GHz ERBW 1.1GS/s 6-bit PVT Tolerant Asynchronous CI-SAR with only 8.5fF Input Capacitance**

» Jongho Kim (Korea, Republic of)[1], Gyuchan Cho (Korea, Republic of)[1], Jintae Kim (Korea, Republic of)[1] (1. Konkuk University, Seoul)

1:30pm **34-2: A 6-Bit 10-GS/s 17.6-mW CMOS ADC with 0.8-V Supply**

» Matias Jara (United States)[1], Behzad Razavi (United States)[1] (1. University of California, Los Angeles)

1:42pm **34-3: A 12b 1.5GS/s Single-Channel Pipelined SAR ADC with a Pipelined Residue Amplification Stage**

» Yi Shen (China)[1], Shubin Liu (China)[1], Yue Cao (China)[1], Haolin Han (China)[1], Hongzhi Liang (China)[1], Zhicheng Dong (China)[1], Dengquan Li (China)[1], Ruixue Ding (China)[1], Zhangming Zhu (China)[1] (1. Xidian University)

2:07pm **34-4: A 7.9-ENOB 1.5GS/s Common-Mode and Temperature Insensitive Pipelined-SAR ADC with an On-Chip Temperature-Sensor-Based Stage-Gain Compensation**

» Hwankyu Song (Korea, Republic of)[1], Gyuchan Cho (Korea, Republic of)[1], Jintae Kim (Korea, Republic of)[1] (1. Konkuk University, Seoul)

3pm **Best Paper Poster Session & Closing and Awards Ceremony**
Salon C