Title of the Paper



Fig. 1. Pipeline SAR ADC with a dynamic residue amplifier.

Authors

Affiliation

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A+B=C (1)

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Fig. 2. Output level shifting settling technique and residue amplifier implementation.

# References:

[1] N. Maghari *et al*., “A Third-Order DT ΔΣ Modulator Using Noise-Shaped Bidirectional Single-Slope Quantizer,” ISSCC, Feb. 2011.

[2] C. Huang *et al*., "A CMOS 6-bit 16-GS/s time-interleaved ADC using digital background calibration techniques," JSSC, Apr. 2011.

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