Session 20 - High-Performance Low-Power Wireless Receivers

Wednesday, May 3, 9:00 - 12:00, Lady Bird 1 Room
Session Chair: Julian Tham, Cypress Semiconductor
Session Co-Chair: Hossein Lavasani, Georgia Institute of Technology

This session covers recent advances in wireless receiver design with a focus on low power high performance RF techniques.

9:00 am **Introduction**

9:05 am 20-1 **N-path Filters and Mixer-First Receivers: A Review (Invited)**, E.A.M. Klumperink, H.J. Westerveld, Bram Nauta, University of Twente

To realize a Software Defined Radio covering the mainstream 0.5-6 GHz wireless communication bands, new SAW-less radio receiver architectures are being explored which realize selectivity in a more flexible and programmable fashion. N-path filters and mixer-first receivers can offer high-linearity high-Q RF-filtering around a center frequency defined by a digital clock, which offers the desired flexible programmability. This paper reviews recent research on N-path filters and mixer-first receivers, identifies advances in performance analysis, circuit performance and applications.

9:55 am 20-2 **A Digital Sine-Weighted Switched-Gm mixer for Single-Clock Power-Scalable Parallel Receivers**, Reda Kasri[1,2,3], Eric Klumperink[2], Philippe Cathelin[1], Eric Tournier[3],Bram Nauta[2,] [1]STMicroelectronics, [2]University of Twente, [3]LAAS-CNRS, Université de Toulouse

10:20 am 20-3 **A Scalable Architecture for Fully Integrated Multi-TV Tuners**, M. H. Koroglu, A. L. Coban, V. M. Pereira, F. Barale, S. X. Wu , W. Yu, R. Sun, and K. Pentakota Silicon Labs Inc.

Silicon TV tuners surpassed CAN-tuners, providing manufacturers with lower-cost, smaller and reliable solutions. Multi-tuners are needed in TVs and Set-Top-Boxes. This paper presents the major blocks for a monolithic dual-tuner with active splitter, tracking filters, buffers, low-power VCO based ADC and local oscillator featuring a 17GHz VCO with fractional dividers.

10:45 am **Break**

11:05 am 20-4 **A LTE RX Front-end with Digitally Programmable Multi-Band Blocker Cancellation in 28nm CMOS**, Q. Wang, H. Shibata*, A. Chan Carusone, A. Liscidini, University of Toronto, *Analog Devices

This paper presents a LTE receiver front-end with a feedback digital filter in the baseband to perform multiband blocker cancellation. The programmable filter provides 34.9dB attenuation of TX leakage and variable attenuation of an additional blocker anywhere in the frequency range 17.5MHz–107.5MHz. The receiver front-end operates at 1.8GHz with a noise figure of 3.9dB, IIP3 of -5dBm, and consumes only 20.4–37.5mW, the lowest among state-of-the-art designs.

11:30 am 20-5 **A 980µW 5.2dB-NF Current-Reused Direct-Conversion Bluetooth-Low-Energy Receiver in 40nm CMOS**, A.Masnadi, H.Lavasani, M.Sharifzadeh, Y.Rajavi, S.Mirabbasi*, M.Taghivand, Qualcomm Inc., *University of British Columbia

Bluetooth Low Energy (BLE) is one of the most popular standards for ultra-low-power radios. Most BLE radios are based on power-hungry low-IF architectures. In this work, current-reuse and subthreshold techniques are employed to deliver a 980µW direct-conversion BLE receiver in 40nm CMOS with multiple µW-level feedbacks that make the design robust over PVT.

Session 21 - Analog Techniques II

Wednesday, May 3, 9:00 - 12:00, Lady Bird 2 Room
Session Chair: Farhan Adil, Massachusetts Institute of Technology
Session Co-Chair: Jiangfeng Wu, Tongji University

This session will present analog techniques ranging from building blocks to full systems including a current stimulator, machine learning processor, delay cells, ESD circuits, and imagers.

9:00 am **Introduction**

9:05 am 21-1 **A ±5V, ±10V, ±15V, 4-Channel Class-G Biphasic Constant-Current Stimulator**, E. Lee, Alfred Mann Foundation

A 4-channel class-G biphasic constant-current (CC) stimulator using ±5V, ±10V and ±15V supplies was proposed to improve average power efficiency (PE). Based on monitoring the output voltage (VSTO), output current would be drawn from different supplies. Bias currents for producing output were reused to monitor VSTO and to switch softly the current drawn from different supplies. Based on a 0.18µm process, the stimulator achieved an improvement of 35% on PE when compared to a conventional CC stimulator.

9:30 am 21-2 **From Algorithms to Devices: Enabling Machine Learning through Ultra-Low-Power VLSI Mixed-Signal Array Processing (Invited)**, Siddharth Joshi, Chul Kim, Sohmyung Ha*, Gert Cauwenberghs, University of California San Diego, * New York University Abu Dhabi

Machine learning and related statistical signal processing algorithms are expected to transform sensor networks and greatly facilitate the Internet of Things. As such, incorporating these algorithms leads to oft-ignored architectures and presents a new set of design trade-offs. This paper considers the implementation of mixed-signal matrix-vector multiplication as a central computational primitive enabling machine learning and statistical signal processing. We describe algorithms that can be implemented on such primitives in the presence of analog variation. We also briefly introduce emerging devices and technologies, providing examples of their use.

10:20 am 21-3 **Design of Tunable Digital Delay Cells**, Yu Chen, Rajit Manohar*, Yannis Tsividis, Columbia University, *Cornell University

This work discusses design considerations for tunable delay cells with good matching, low jitter, and robust communication interface. Effects resulting in signal-dependent delay are discussed and eliminated. A 1.2V 65nm prototype achieves a tunability range of 5n-10µs, with a matching standard deviation of 2.3% and jitter standard deviation of 0.065%.

10:45 am **Break**

11:05 am 21-4 **RC-Triggered ESD Clamp with Low Turn-on Voltage**, M. Stockinger, R. Mertens, NXP Semiconductors

We present circuit techniques for improving system-level ESD performance of RC-triggered boosted rail clamps. We lower the trigger voltage by switching a capacitor onto the RC detector stage. VDD stress is further reduced by adding a dedicated VDD detector stage. Test and simulation data of a CMOS microcontroller are included.

11:30 am 21-5 **A CMOS Pixel Design with Binary Space-time Exposure Encoding for Computational Imaging**, Y. Luo, S. Mirabbasi, University of British Columbia

A CMOS pixel design targeting to spatial-temporal exposure encoding based computational imaging is presented. By integration of selective charge storage units and exposure code memories, the prototyped pixel design performs both temporal and spatial-temporal encoded exposure.

Session 22 - Oversampling Data Converter

Wednesday, May 3, 9:00 - 12:00, Lady Bird 3 Room
Session Chair: Nima Maghari, University of Florida
Session Co-Chair: Ivan O'Connell, University College Cork

This session presents data converter techniques that include a ring amplifier based pipeline and successive approximation registers with pipelinging, residue boosting, time-interleaving and a time domain method.

9:00 am **Introduction**

9:05 am 22-1 **An 84 dB Dynamic Range 62.5-625 kHz Bandwidth Clock-Scalable Noise-Shaping SAR ADC with Open-Loop Integrator using Dynamic Amplifier**, M. Miyahara, A. Matsuzawa, Tokyo Institute of Technology

This paper proposes a noise shaping SAR ADC with open-loop integrator using dynamic amplifier. The proposed integrator requires low-gain open-loop amplifiers, therefore low power dynamic amplifier can be used. An SNDR of 83.5dB, a power consumption 273.4μW, and a FoM of 173dB with a bandwidth of 250kHz is achieved.

9:30 am 22-2 **A 2.4mW, 111 dB SNR Continuous-time ΣΔ ADC With A Three-level DEM Technique**, Khiem Nguyen, Michael Determan, Sejun Kim*, Analog Devices Inc., *Broadcom Corp.

A multi-bit continuous-time ΣΔ audio ADC employing 3-level unit-elements with 1st-order mismatch shaping which achieves 111dB A-weighted SNR, -98dB THD+N in the 22 kHz bandwidth, while consumes a total of 2.4mW from a 3.3V supply, and occupies ~0.5 mm^2 in a 0.18μm CMOS process

9:55 am 22-3 **A 50 MHz BW 73.5 dB SNDR Two-stage Continuous-time ΔΣ Modulator with VCO Quantizer Nonlinearity Cancellation**, S Dey, K Reddy*, K Mayaram, T Fiez**, Oregon State University, *Linear Technology Corporation, **University of Colorado Boulder

A 50MHz bandwidth two-stage continuous-time ΔΣ modulator with VCO-quantize r(VCOQ) is presented. The modulator suppresses the VCOQ Voltage-to-Frequency nonlinearity through dual path cancellation and achieves 73.5dB/88dB SNDR/SFDR. This architecture exhibit robustness against first stage quantization error leakage to the

output. The SNDR variation remains within 1.5dB for ±10% gain mismatch between the two stages and temperature variation of 0C-80C.

10:20 am 22-4 **Adaptive Digital Noise-Cancellation Filtering using Cross-Correlators for Continuous-Time MASH ADC in 28nm CMOS**, Yunzhi Dong , Jose B-Silva, Qingdong Meng, Jialin Zhao, Wenhua Yang, Trevor Caldwell, Hajime Shibata, Zhao Li, Donald Paterson, Jeffrey Gealow, Analog Devices

This paper presents an adaptive digital noise cancellation filter (DNCF) using cross-correlation (XCORR) developed for continuous-time (CT) multi-stage noise-shaping (MASH) ADCs. The XCORR engine continuously estimates the transfer functions of sub DS loops and updates the coefficients for the DNCF. An ADC prototype with this engine is built in 28nm CMOS and it achieves 72dB of dynamic range over 440MHz BW, with a total power of 1.25W from 1V and 1.8V supplies. Comparing to a power-up least-mean squares (LMS) engine, the XCORR-based adaptive DNCF achieves 2dB better noise cancellation across up to 10% supply variations.

10:45 am **Break**

11:05 am 22-5 **An 11.0 bit ENOB, 9.8 fJ/conv.-step Noise-Shaping SAR ADC Calibrated by Least Squares Estimation**, H. Garvik, C. Wulff, T. Ytterdal, Norwegian University of Science and Technology

A noise-shaping SAR ADC in 28 nm FDSOI, using an inverter-based loop filter is presented. A calibration technique that estimates CDAC calibration coefficients from a digitized test sequence is proposed. At Nyquist bandwidth 1.75 MHz, measured accuracy is 11.0 bit ENOB, and Walden FOM 9.8 fJ/conv.-step.

11:30 am 22-6 **A Two-Capacitor SAR-Assisted Multi-Step Incremental ADC with a Single Amplifier Achieving 96.6 dB SNDR over 1.2 kHz BW**, Y. Zhang, C.-H. Chen, T. He, Kazuki Sobue*, Koichi Hamashita*, and G. Temes, Oregon State University, *Asahi Kasei Microdevices

This paper presents a two-step incremental ADC (IADC) using SAR-assisted extended counting. In the first step, the IADC is configured as a first-order $\Delta\Sigma$ loop with an input feedforward architecture. In the second step, a two-capacitor SAR-assisted extended counting technique enhances the accuracy. A single active integrator is shared in both steps.

11:55 am 22-7 **A 1.2 V, 0.84 pJ/Conv.-Step Ultra-low Power Capacitance to Digital Converter for Microphone based Auscultation**, Neelakantan Narasimman[1,2], Dipankar Nag[2], Kevin Chai Tshun Chuan[2], and Tony T. Kim[1] , [1]VIRTUS, IC Design Centre of Excellence, Nanyang Technological University, [2]Institute of Microelectronics, A*STAR

We propose a novel architecture and circuit implementation for Capacitance to Digital Converter. Capacitance information is digitized using a continuous time second order delta-sigma modulator with multi-bit quantization. Proposed architecture embeds a Capacitance to Voltage Converter in the delta-sigma loop, which improves dynamic range and energy efficiency of the CDC.

Session 23 - Panel - Bio-inspired Learning and Inference Systems: What Works and What Didn't

Wednesday, May 3, 9:00 - 12:00, Lady Bird Studio Room
Moderators: Mingoo Seok, Columbia University and Jae-Sun Seo, Arizona State University

Panelists:
Rajit Manohar – Cornell University
Vijaykrishnan Narayanan – Penn State University
Gert Cauwenberghs – University of California San Diego
Ram Krishnamurthy - Intel
Andrew Cassidy - IBM

We are observing significant success in artificial intelligence, where machines achieve comparable performance or even outperform humans in complicated tasks such as playing Go, driving a car, and diagnosing cancers. Particularly interesting is that some of the techniques enabling those successes were developed with the inspiration from behaviors of biological brains. In this panel, we will invite the world experts in this field and discuss the successes and failures of bio-inspired learning and inference.

Session 24 - Millimeter-Wave Communication Circuits

Wednesday, May 3, 1:30 - 3:40, Lady Bird 1 Room
Session Chair: John Long, University of Waterloo
Session Co-Chair: Fa Foster Dai, Auburn University

The millimeter- and sub-millimeter-wave bands promise wireless systems at Gbit/s data rates. This session presents circuits and techniques for accessing these very high frequency bands.

1:30 pm **Introduction**

1:35 pm 24-1 **Millimeter-wave Full-Duplex Wireless: Applications, Antenna Interfaces and Systems (Invited)**, T. Dinc, H. Krishnaswamy, Columbia University

Millimeter-waves offer significantly wider channel bandwidths (BW) than RF and are drawing significant interest for short-range wireless personal area networks (WPANs), vehicular radar and next generation (5G) cellular communication. Full-duplex is another emergent technology which can theoretically double the spectral efficiency by transmitting and receiving simultaneously on the same frequency. This paper reviews recent developments at Columbia University on millimeter-wave full-duplex which merges these two emergent technologies. In this context, potential applications for millimeter-wave full-duplex links are described. A 60GHz full-duplex transceiver and 25GHz magnetic-free non-reciprocal passive circulator implemented in 45nm SOI CMOS process are discussed.

2:25 pm 24-2 **A Bidirectional Lens-Free Digital-Bits-In/-Out 0.57mm^2 Terahertz Nano-Radio in CMOS with 49.3mW Peak Power Consumption Supporting 50cm Internet-of-Things Communication**, Taiyun Chi, Hechen Wang*, Min-Yu Huang, Fa Foster Dai*, and Hua Wang, Georgia Institute of Technology, *Auburn University

A CMOS digital-bits-in/-out THz nano-radio with 0.57mm^2 chip area is presented. The THz operation and bidirectional architecture lead to radio ultra-miniaturization. The TX harmonic oscillator is OOK- modulated, while an on-chip TDC measures RX oscillation start-up time for THz-to-bits receiving. It supports maximum 4.4Mb/s OOK over 50cm without Si lens.

2:50 pm 24-3 **An Efficient 4-Way-Combined 291 GHz Signal Source with 1.75 mW Peak Output Power in 65 nm CMOS**, A. Apriyana, G. Feng, S. Yang, J. Wen*, L. Sun*, H. Yu*, Nanyang Technological University,, *Hangzhou Dianzi University

A 291 GHz injection-locked signal source using two power-combined of 4-cell zero-phase coupled oscillator networks (CON) is demonstrated. The source exhibits 7.5% tuning range centered at 291 GHz or equivalently operating frequency range of 280 – 302 GHz and a peak output power of 1.75mW.

3:15 pm
24-4 **An up to 36Gbps Analog Baseband Equalizer and Demodulator for mm-Wave Wireless Communication in 28nm CMOS**, Oscar Elisio Mattia[1,2], Davide Guermandi[2], Guy Torfsy[3], Piet Wambacq[1,2, 1]Vrije Universiteit Brussel, [2]imec, [3]imec - Ghent University

In this paper we present, to the authors' best knowledge, the first complex DFE capable of equalizing 5 complex taps of inter-symbol interference on QPSK/16QAM data, at a maximum data-rate of 18/36Gbps, respectively, aggregating all 4 channels of the 60GHz IEEE802.11ad standard. This is realized with I and Q signal paths that can each handle 4PAM signals, leading to 16 possible constellation points to demodulate.

Session 25 - Linear Regulator Techniques

Wednesday, May 3, 1:30 - 2:50, Lady Bird 2 Room
Session Chair: Jeff Morroni, Texas Instruments
Session Co-Chair: Mike Mulligan, Silicon Laboratories

This session features novel switched-capacitor and inductive converter design techniques. The focus ranges from integrated isolated converters, and multi-mode compensators, to ultra-low-power IoT applications.

1:30 pm **Introduction**

1:35 pm
25-1 **Digitally-Assisted Leakage Current Supply Circuit for Reducing the Analog LDO Minimum Dropout Voltage**, Samantak Gangopadhyay, Saad Bin Nasir, *Hoan Nguyen, *Jihoon Jeong,*Francois Atallah, *Keith Bowman, Arijit Raychowdhury,School of ECE, Georgia Institute of Technology, GA, USA,*Qualcomm Technologies, Inc., Raleigh, NC, USA

A digitally-assisted leakage current supply (LCS) circuit reduces the maximum current demand for analog low-dropout (LDO) voltage regulators to lower the minimum dropout voltage (VDO,MIN), and consequently, enable a wider range of LDO operation for power savings in system-on-chip processor cores. From silicon measurements in a 130nm test chip, the LCS assisted hybrid LDO decreases VDO,MIN by 30-38%, resulting in core power reduction of 21-28% at equal clock frequencies within the wider LDO operating range.

2:00 pm
25-2 **An External-Capacitor-less Low-Dropout Regulator with Less than –36dB PSRR at All Frequencies from 10kHz to 1GHz Using an Adaptive Supply-Ripple Cancellation Technique to the Body-Gate**, Younghyun Lim, Jeonghyun Lee, Suneui Park, Jaehyouk Choi, Ulsan National Institute of Science and Technology

This work presented an external-capacitor-less gate-dominant LDO that provides PSRR less than –36dB from 10kHz to 1GHz. Using an adaptive supply-ripple cancellation (ASRC) technique, the PSRR-hump of conventional gate-dominant LDOs was suppressed dramatically. Since the ASRC scaled ripples adaptively, the LDO maintained high PSRRs despite changes in load-current and dropout-voltage.

2:25 pm 25-3 **Digitally Controlled Voltage Regulator Using Oscillator-based ADC with fast-transient-response and wide dropout range in 14nm CMOS**, Tarun Mahajan, Ramnarayanan Muthukaruppan, Dheeraj M. Shetty, Sumedha Mangal, Harish K. Krishnamurthy, Intel Corporation

This work targets 1-1.15V input voltage with output voltage range of 0.5-1.12V with minimum 30mV dropout, and load current range of >22x with 0.1-2.2A at 50mV dropout with <0.006mV/mA load regulation using 10-bit power-stage binary control and characterized using programmable synthetic resistive load with 18nF load capacitance on-die over load.

Session 26 - Forum - Emerging Techniques for Data Converters

Wednesday, May 3, 1:30 - 4:30, Lady Bird 3 Room
Forum Chairs: Mike Chen, University of Southern California and Ayman Shabra, MediaTek

1:30 pm **Introduction**

1:35 pm 26-1 **Stranger Things: Problems, Solutions, and Possible Trends in High Speed Data Converters**, David Robertson, Analog Devices

While there continues to be a healthy level of publication of new data converter papers, we can argue that we are really entering the “Post-Figure-of-Merit” phase of converter technology. Rather than judge a data converter on the basis of abstract technical performance, we need to look at how well it solves the application problem. This presentation will take a look at some of the recent trends in architectures and circuit technologies, and reflect on how they are being used (or sometimes misused) to address today’s application challenges.

2:10 pm 26-2 **Time-Based Circuits for High-Performance ADC,** Matt Straayer, Maxim.

Time-based circuits have seen an increased use in advanced process nodes with fast transistors and low supply voltages. Specifically, high-performance ADC see benefits using time-based circuits due to the ease of quantizing binary time-based signals with simple digital circuits. This talk will discuss concepts such as phase-domain signals, noise-shaping, and metastability of time-based quantizers, highlighting a number of ADC architectures that directly utilize time. Finally, recent examples of state-of-the art time-based ADC will be reviewed.

2:45 pm 26-3 **Time-based encoders and digital signal processors in continuous time**, Sharvil Patil, Analog Devices, Inc. and Yannis Tsividis, Columbia University

3:20 pm 26-4 **Emerging Data Conversion Architectures**, Nan Sun, University of Texas at Austin

In this talk, I will present several unconventional data conversion architectures. First, I will talk about how we can make use of noise, which is usually deemed as an undesirable thing, to estimate the conversion residue and increase the SNR of a SAR ADC. It is an interesting example of stochastic resonance, in which the presence of noise can lead to not SNR degradation but SNR enhancement. Second, I will talk about how we can perform data conversion below the Nyquist rate by exploiting the sparsity of the input

signal. I will show two example compressive sensing ADCs and how the effective ADC conversion rate can be reduced by 4 times but without losing information. Third, I will discuss hybrid ADC architectures, especially the combination of SAR and delta-sigma ADC. This novel noise-shaping SAR ADC can achieve high power efficiency and high resolution but without the need for OTA based integrator. Last but not least, I will show our groups' research on time/phase-domain delta-sigma ADCs that use simple logic gates for integration and quantization. They can not only achieve high performance and are scaling friendly, but also are fully synthesizable using standard digital flow, greatly improving productivity.

3:55 pm 26-5 **Trend in High Speed Digital to Analog Converters**, Mike Chen, University of Southern California.

Session 27 - Technology Directions

Wednesday, May 3, 1:30 – 2:50, Lady Bird Studio Room
Session Chair: Christophe Antoine, Analog Devices
Session Co-Chair: Marco Tartagni, University of Bologna

This session gathers three emerging multidisciplinary applications of electronic circuits: flexible substrates, energy harvesting sensors on power lines and optically-assisted high-bandwidth electronics.

1:30 pm **Introduction**

1:35 pm 27-1 **Flexible Selfbiased 66.7nJ/c.s. 6bit 26S/s Successive-Approximation C-2C ADC with Offset Cancellation using Unipolar Metal-Oxide TFTs**, Nikolas Papadopoulos[1], Florian De Roosey[1], Yi-Cheng Lai[3], Jan-Laurens van der Steen[4], Marc Ameys[1], Wim Dehaene[1], Jan Genoe[1,2] and Kris Myny[1, 1]imec, [2]KU Leuven, [3]AU Optronics Corporation, [4]Holst Center

Dual-gate InGaZnO TFTs are demonstrated to achieve a 6-bit SAR ADC operated at a clock of 400Hz and a power dissipation of 52.2µW at a supply of 15V on flexible substrate. DNL of 0.7LSB and an INL of 0.58 LSB using only n-type TFTs and FoM of 66.7nJ/c.s. is achieved.

2:00 pm 27-2 **Smart-Wire: A 0.5V 44uW 0°C to 100°C Powerline Energy Harvesting Sensor Node**, A. Chua, R. Maestro, J. Jardin, K. Monisit, R. Nuestro, K. Fabay, B. Pelayo, W. Lofamia, J. Ortiz, J. Madamba, L. Alarcon, University of the Philippines-Diliman

A 44µW 0.5V self-powered powerline-monitoring sensor node is implemented in 65nm CMOS. A 450kHz 30kbps BPSK-modulated transceiver enables 1.5-meter node-to-node powerline communication at 10E-6 BER. The node has a 3.354 ENOB 50kSps SAR ADC for current measurements and a 440Sps time-to-digital converter for 0-100°C temperature measurements with 1.12°C granularity.

2:25 pm 27-3 **A Monolithically Integrated, Optically Clocked 10GS/s Sampler with a Bandwidth of > 30GHz and a Jitter of < 30fs in Photonic SiGe BiCMOS Technology**, B. Krueger[1,4], R. E. Makon[1], O. Landolt[1], O. Hidri[1], T. Schweiger[1], E. Krune[2], D. Knoll[3], S. Lischke[3] and J. Schulze[4, 1]Rohde & Schwarz GmbH & Co., [2]Technische Universitaet Berlin, [3]Innovations for High-Performance Microelectronics (IHP), [4]University of Stuttgart

An optically clocked 10GS/s sampler integrated in a photonic 0.25µm SiGe-BiCMOS technology uses an optical pulse train generated by a mode-locked laser to sample an

electrical signal. Experimental results demonstrate a bandwidth >30GHz, a jitter <30fs, a THD <−33dB over the entire bandwidth, and a SNR of 35.3dB.