A System Verilog Behavioral Model for PLLs for Pre-Silicon Validation and Top-Down Design Methodology

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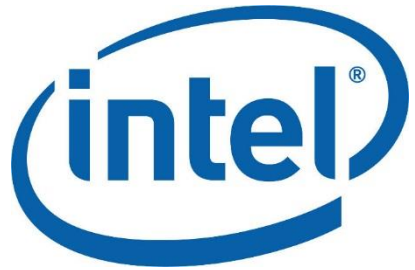

Agenda

- Problem formulation.
- PLL System-Verilog behavioral model.
- Model results and correlation with circuit behavior.
- Model applications in top-down design methodology.
- Model applications in pre-silicon validation.
- Conclusion.

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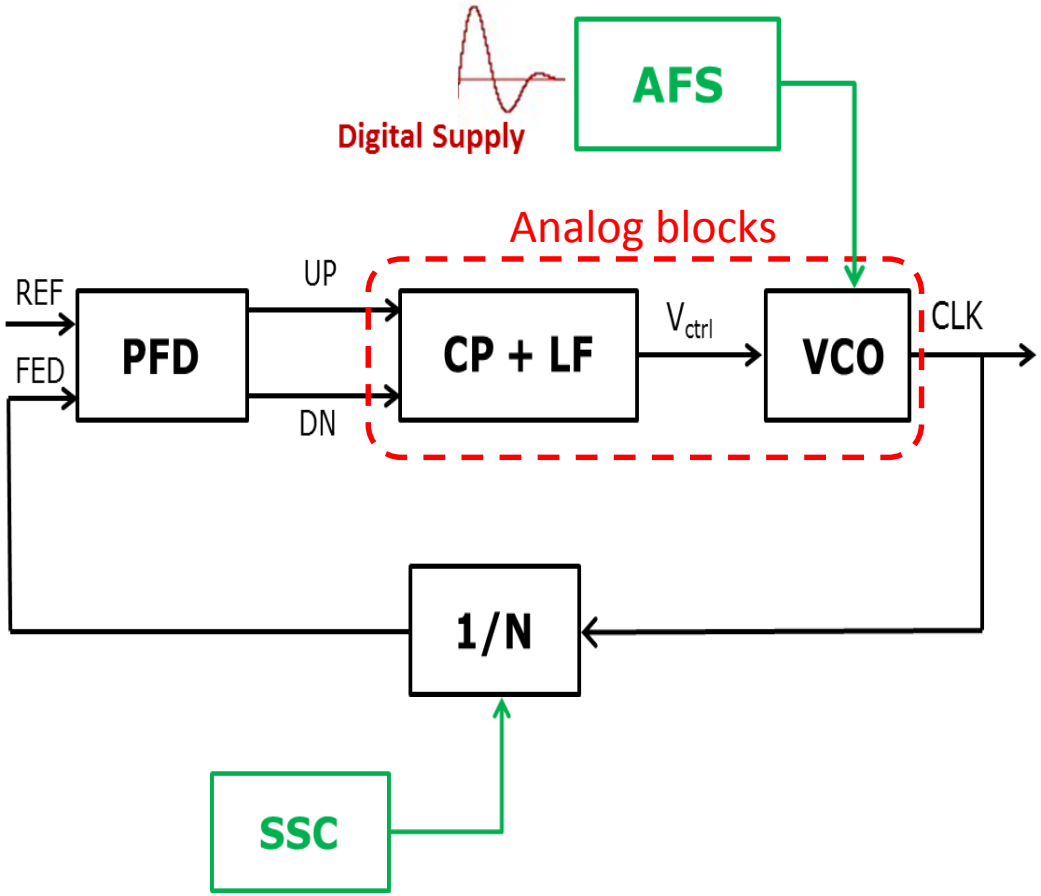
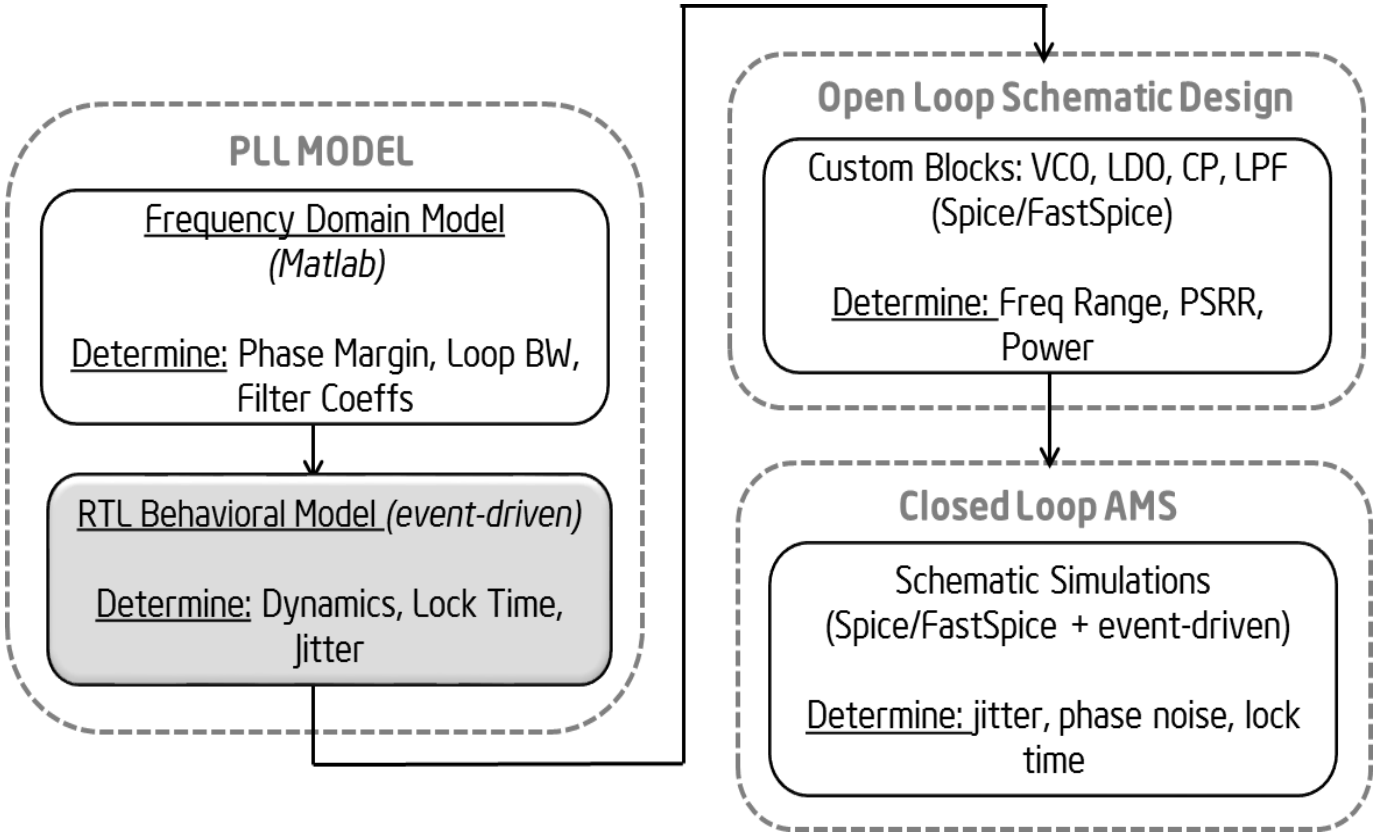
Problem Formulation





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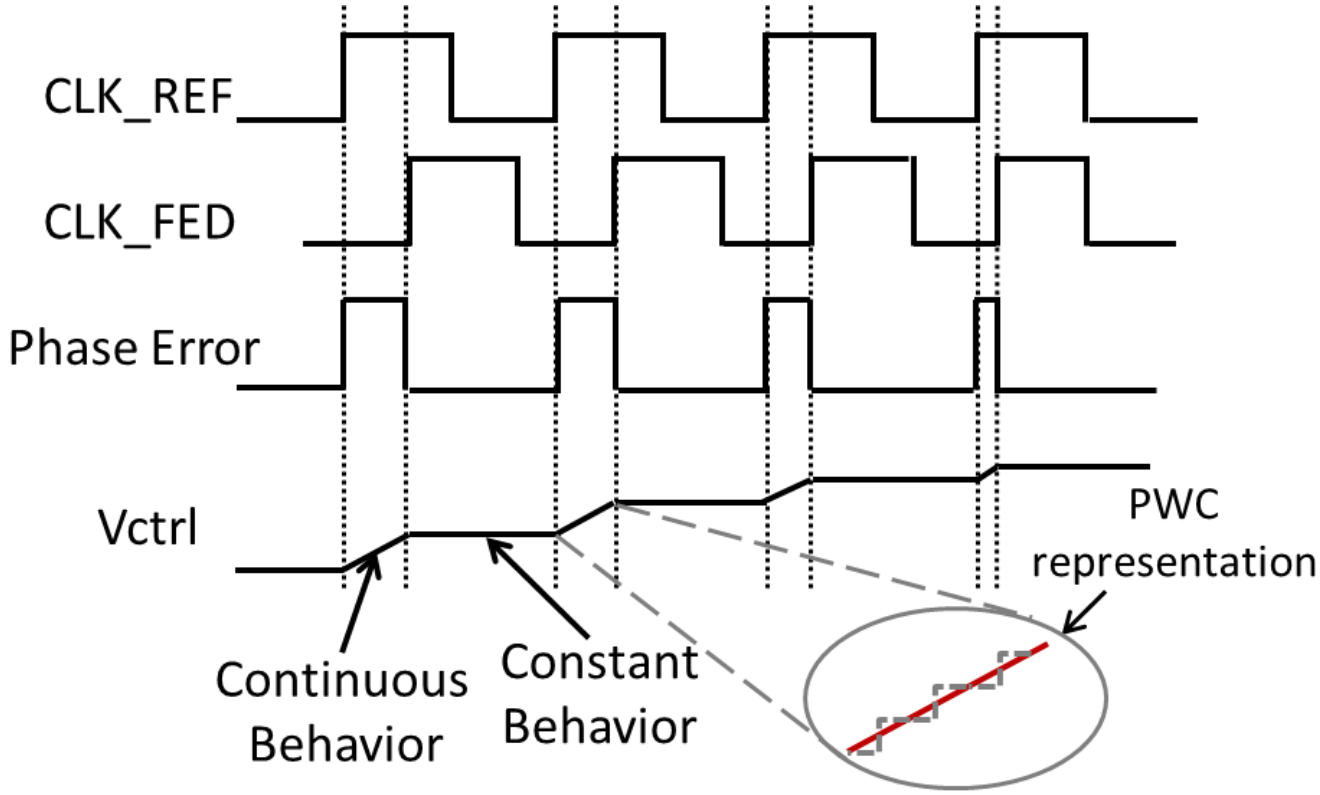
Modeling Approach

Event Driven (Digital Simulation) Approach

Real Number PWC representation for analog signals during phase error

Look-up tables for non-linear behavior

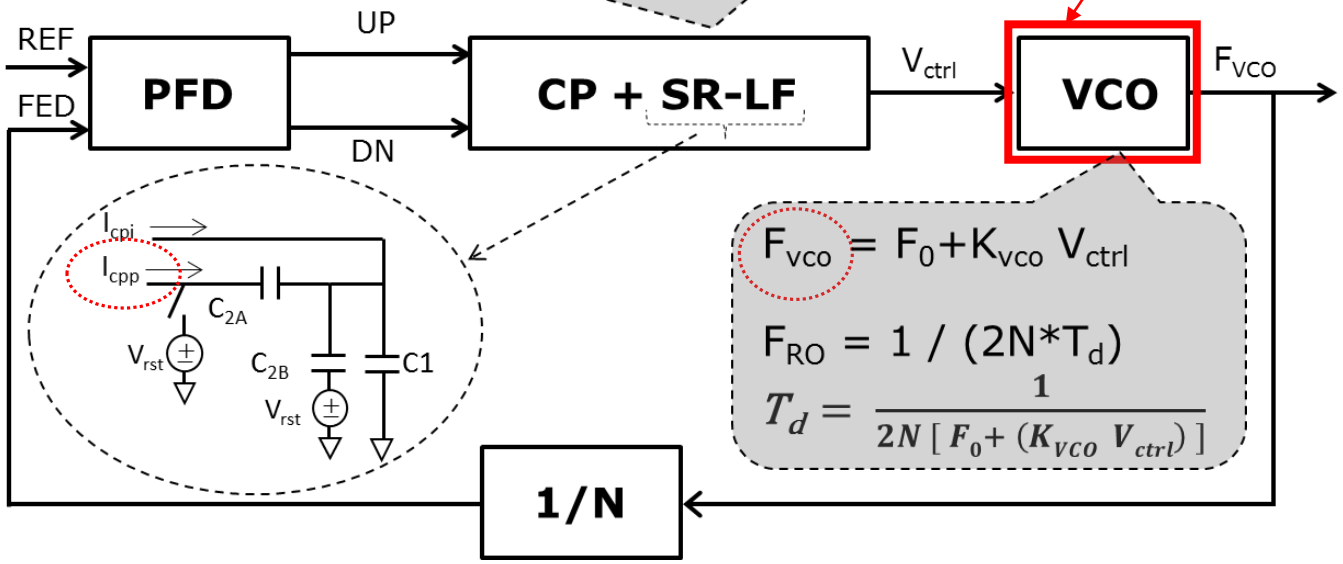
Noise modeling for main blocks



Example PLL using Switched Cap Loop Filter

$$\mathbf{V_{ctrl}} = \underbrace{\frac{I_{cpi}}{C_1 + C_{2B}} * \Delta t}_{\mathbf{V_{int}}} + \underbrace{\frac{I_{cpp}}{C_1 + C_{2B}} * \Delta t}_{\mathbf{V_{prop}}}$$

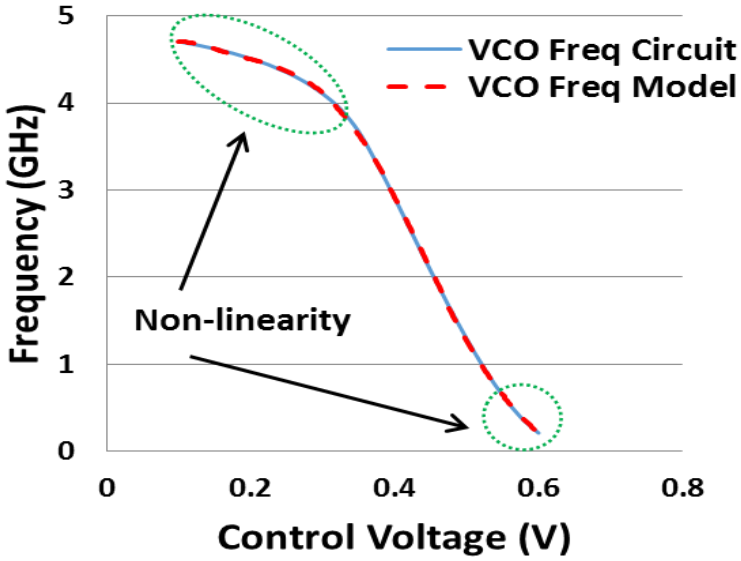
Thermal noise modeled as random jitter with normal dist.

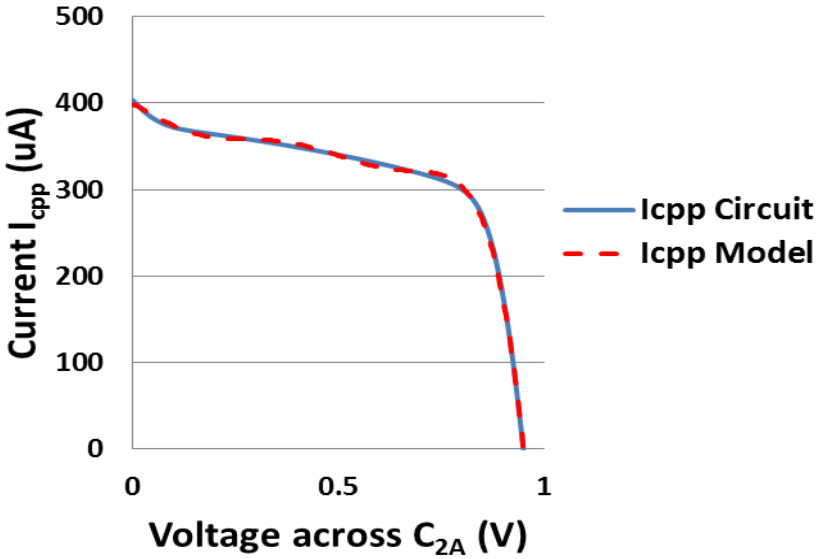


$F_{vco} = F_0 + K_{vco}\, V_{ctrl}$

$F_{RO} = 1 / (2N * T_d)$

$$T_d = \frac{1}{2N\,[\,F_0 + (K_{vco}\,V_{ctrl})\,]}$$





Ref: A. Maxim, ISSCC 2001

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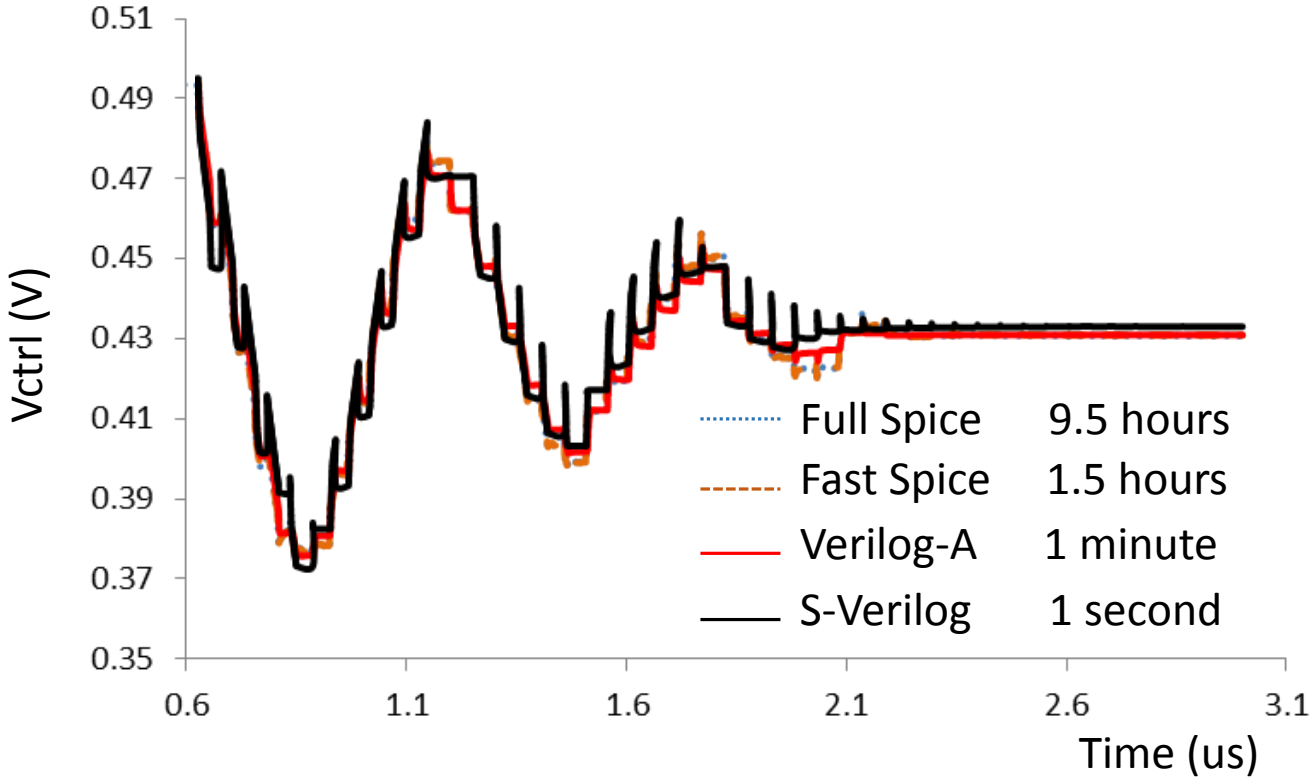
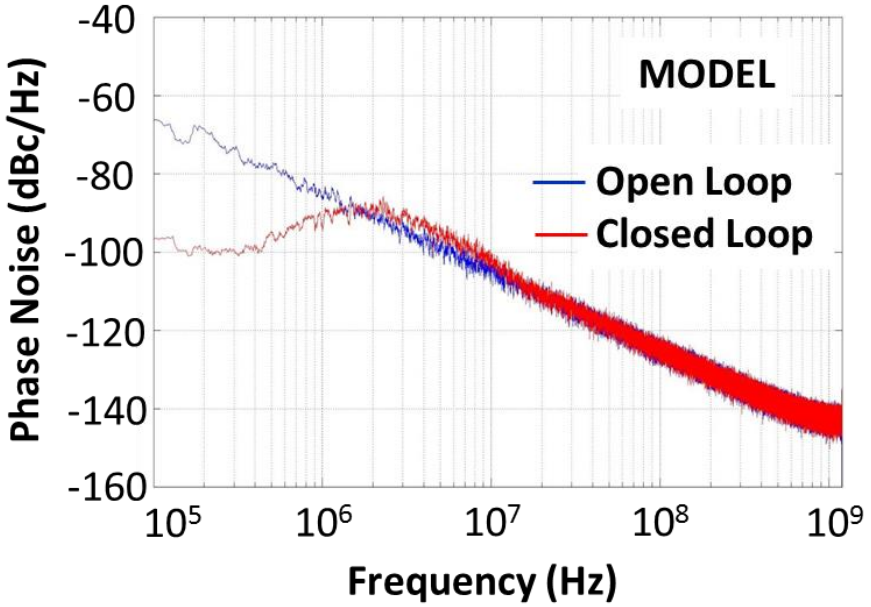
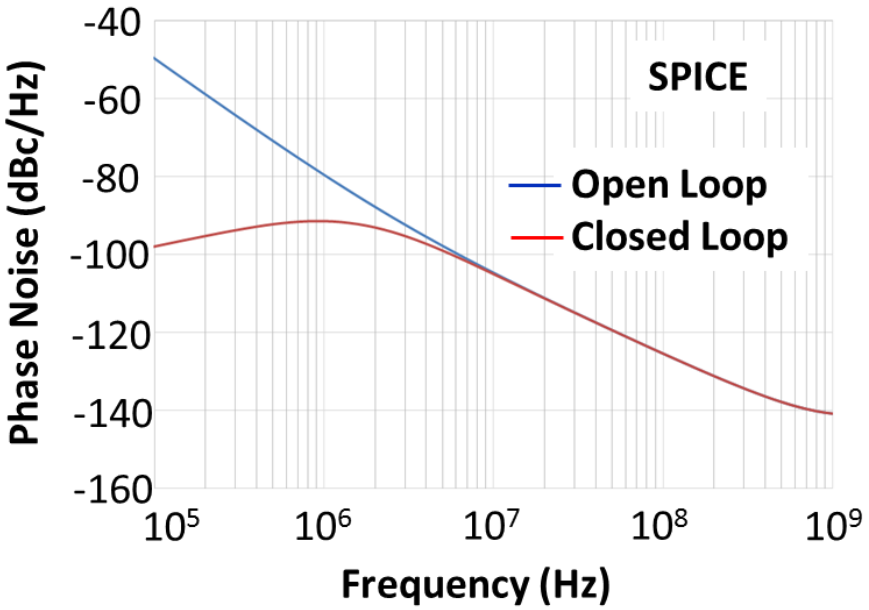
Model vs. Circuit



	Run Time	Correlation with Full Spice
Full Spice	9.5 hours	N/A
Fast Spice	1.5 hours	99.99%
Verilog-A	1 minute	98.8%
S-Verilog	1 second	97.6%





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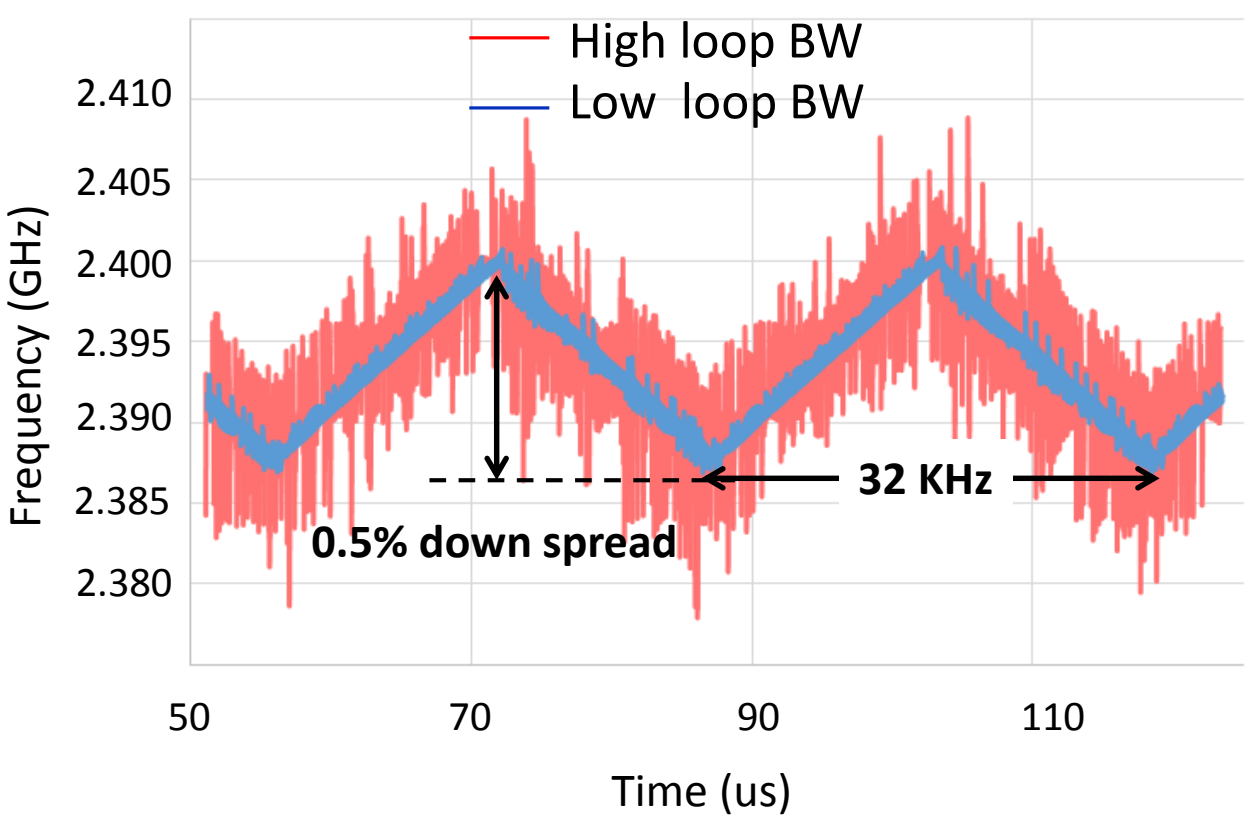
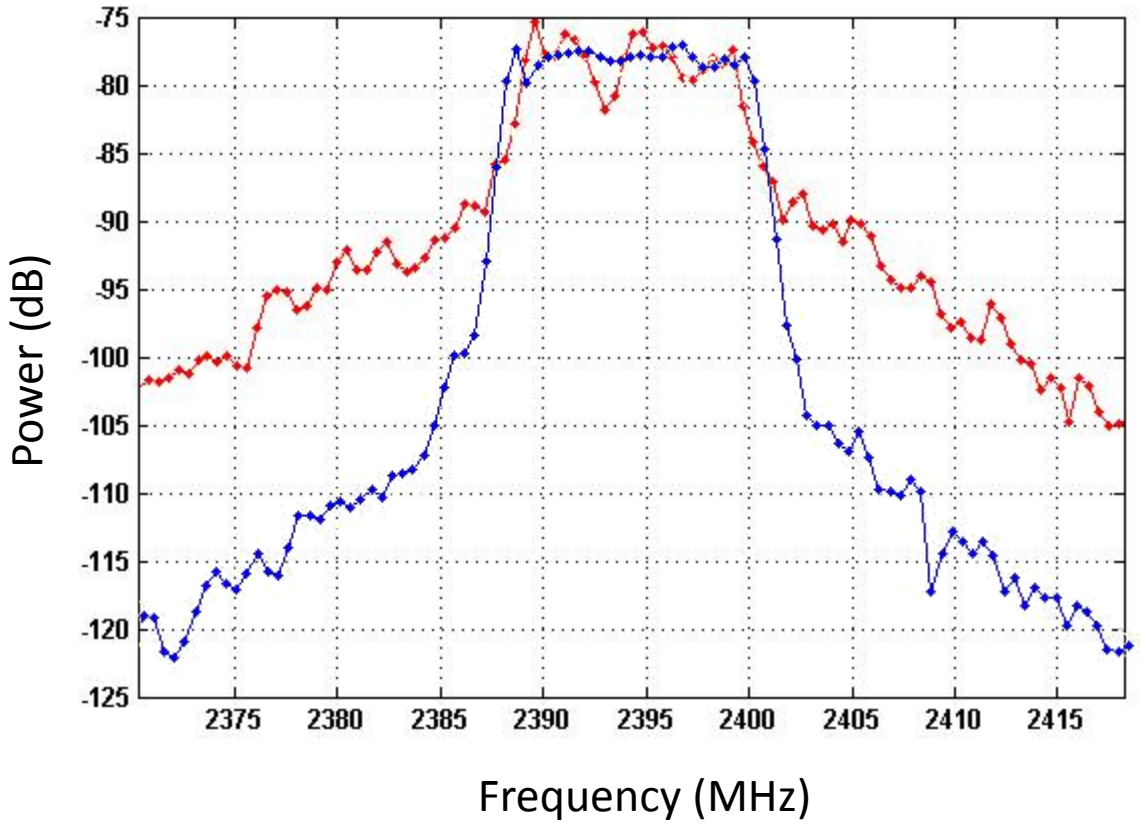
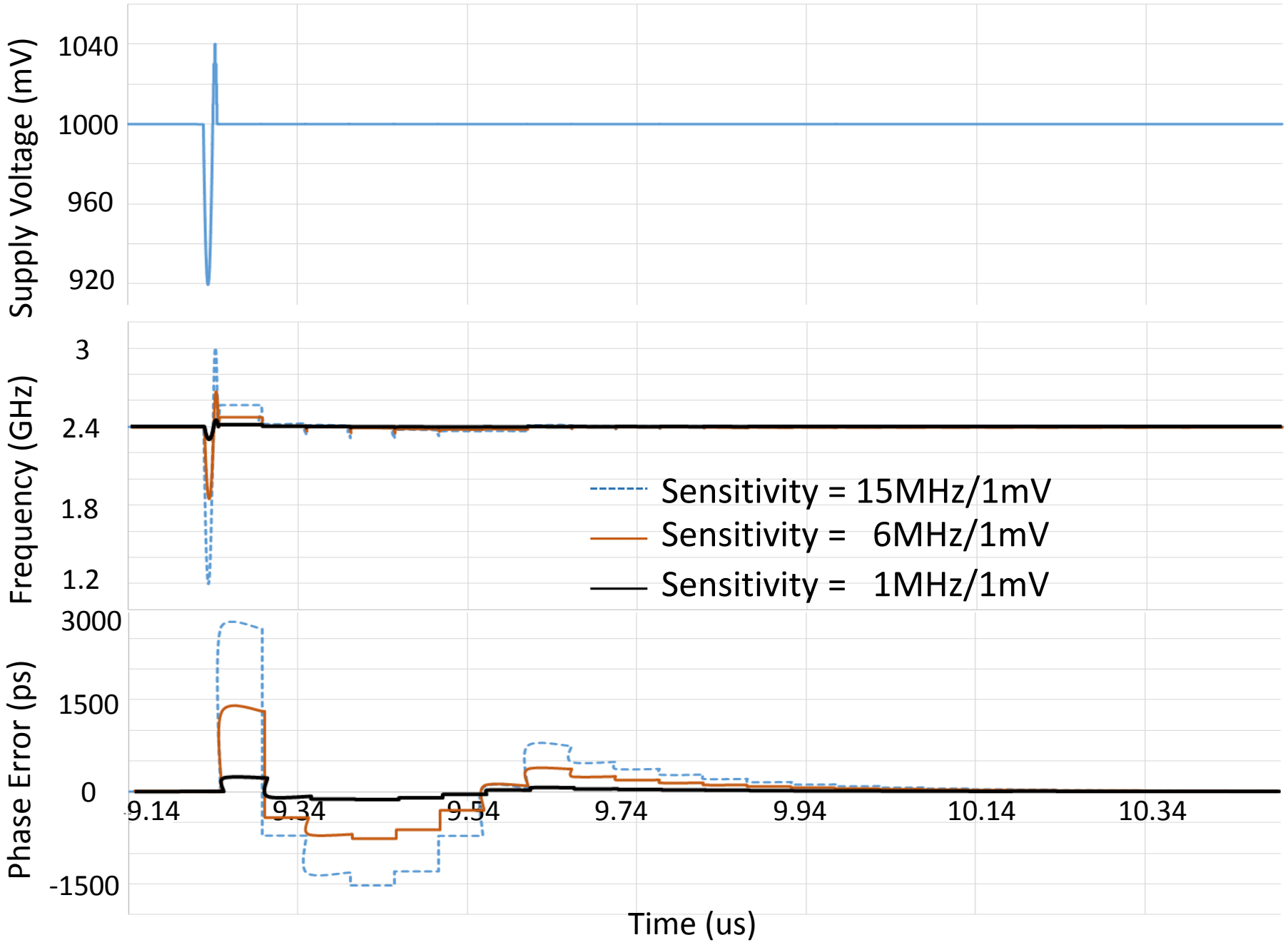
Exercising Spread Spectrum Clocking





Exercising Adaptive Frequency Scaling



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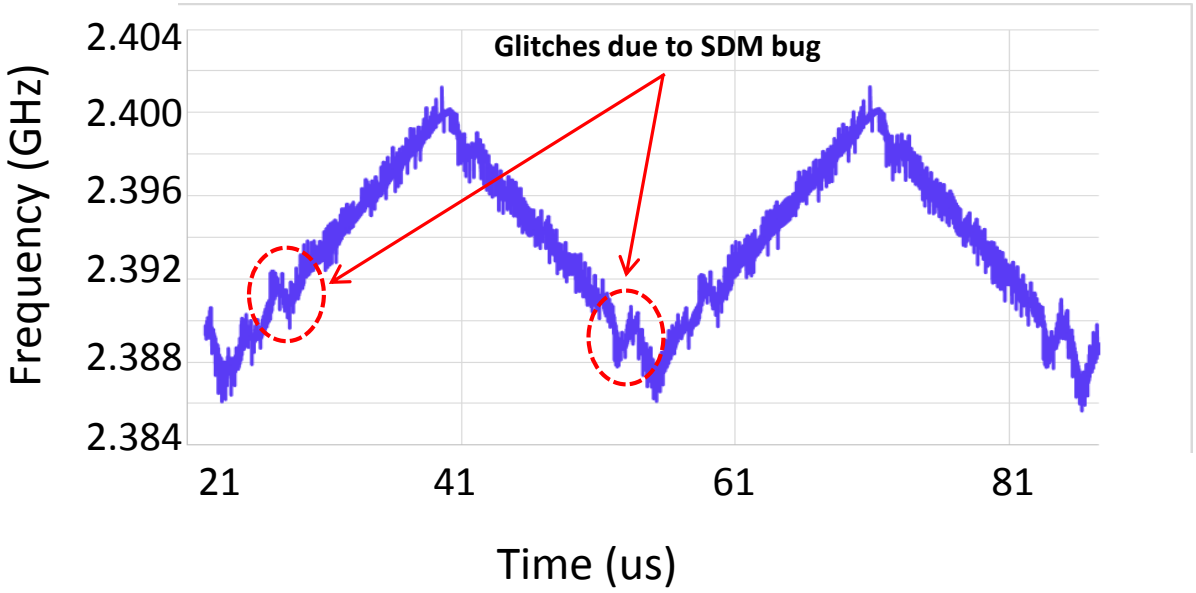
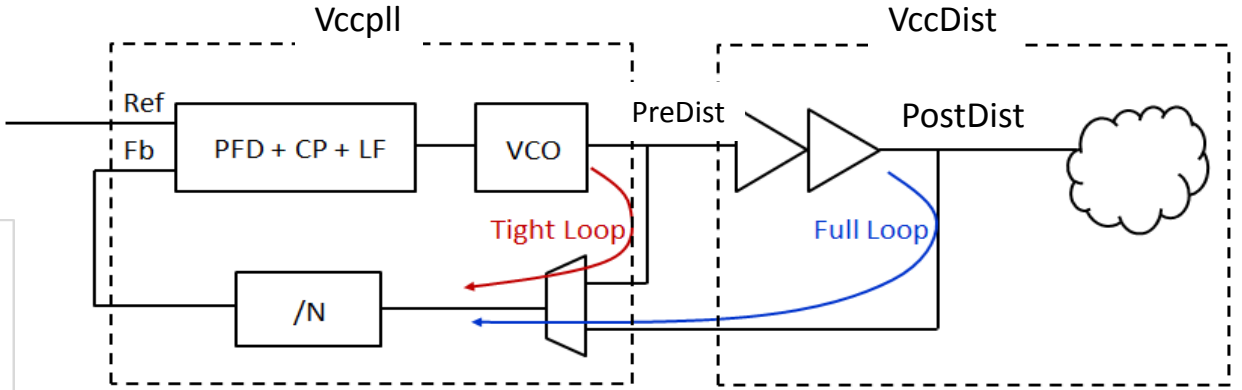
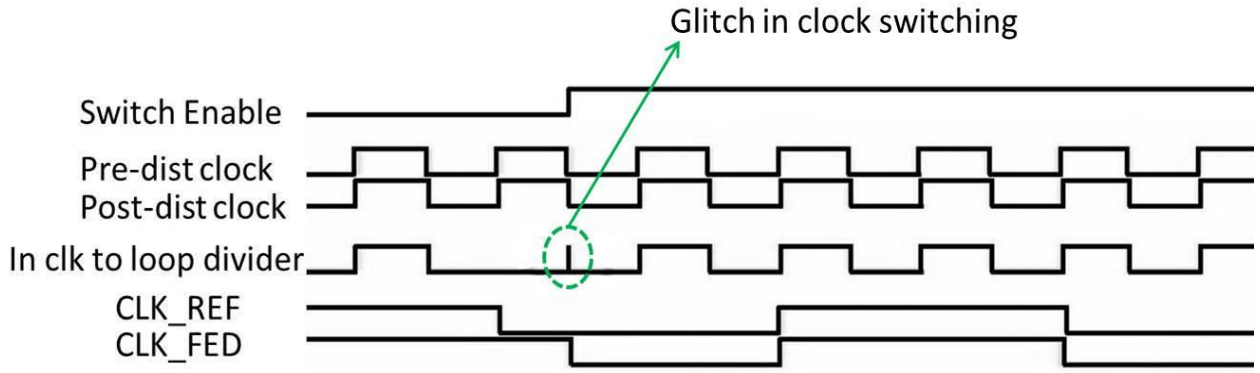
Validating SSC and TL to FL Features







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Conclusion and Future Work

- A System-Verilog Behavioral Model for PLLs runs in 1 second with more than 97% correlation with circuit behavior.
- Modeling Approach relies mainly on four key factors
  - Event Driven Simulation to fit for bot pre-silicon validation and top-down design.
  - Real number PWC representation for analog signals during phase error only.
  - Look-up tables for non-linear blocks.
  - Noise modeling for VCO thermal noise.
- New top down design methodology for PLLs that utilizes the new model to exercise design features with fast simulations.
- The model was integrated in pre-silicon validation environment, and caught design bugs without the need for long AMS.
- Modeling other noise sources, and extending the model to other types of PLLs including digital PLLs, are considered future work.

Thank You

Q&A