A Voltage Doubling Passive Rectifier/Regulator Circuit for Biomedical Implants

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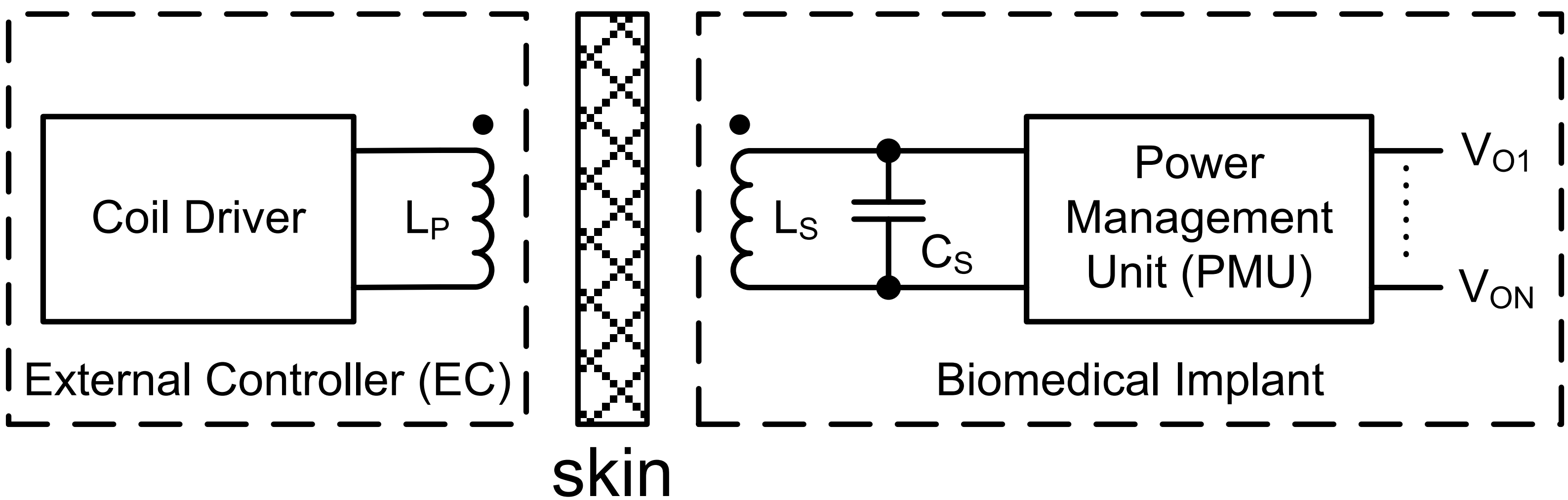
Outline

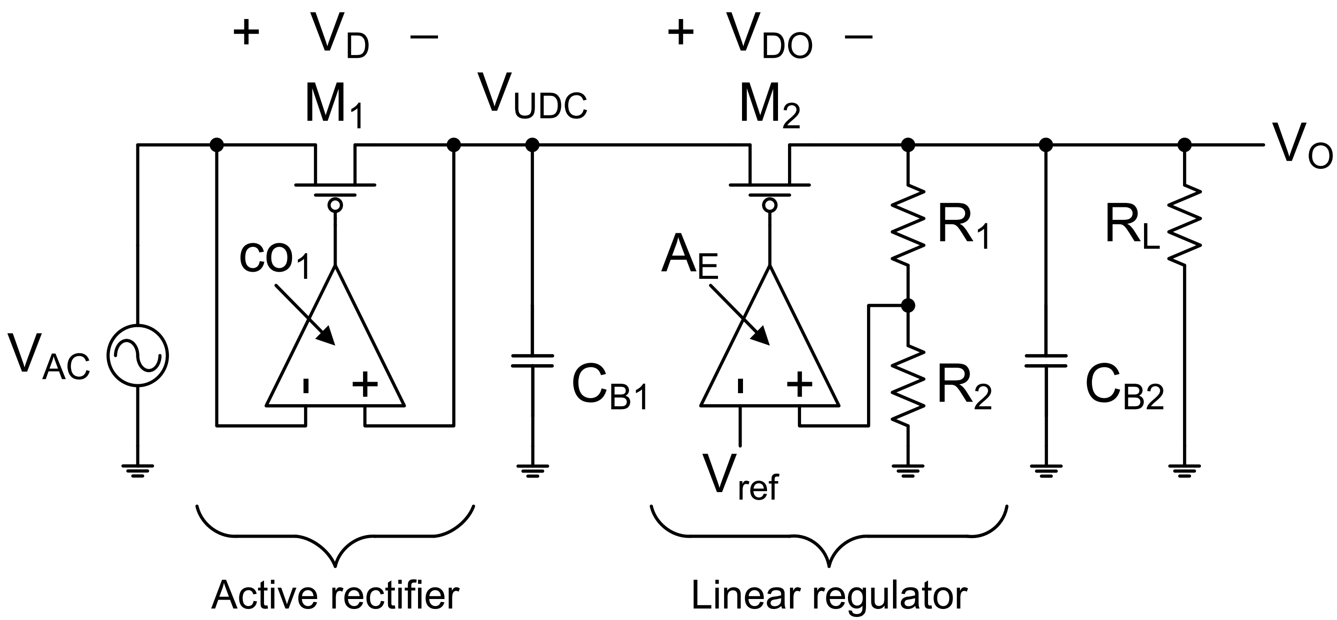
- Motivation
- Review of previous works
- Proposed passive rectifier/regulator technique
- Voltage doubling passive rectifier/regulator circuit
- Implementation and experimental results
- Summary and conclusion

Motivation

- Transcutaneous power transmission commonly used to power biomedical implants wirelessly
- Power transmitted from L_P to L_S inductively
- DC supplies provided by power efficient PMU

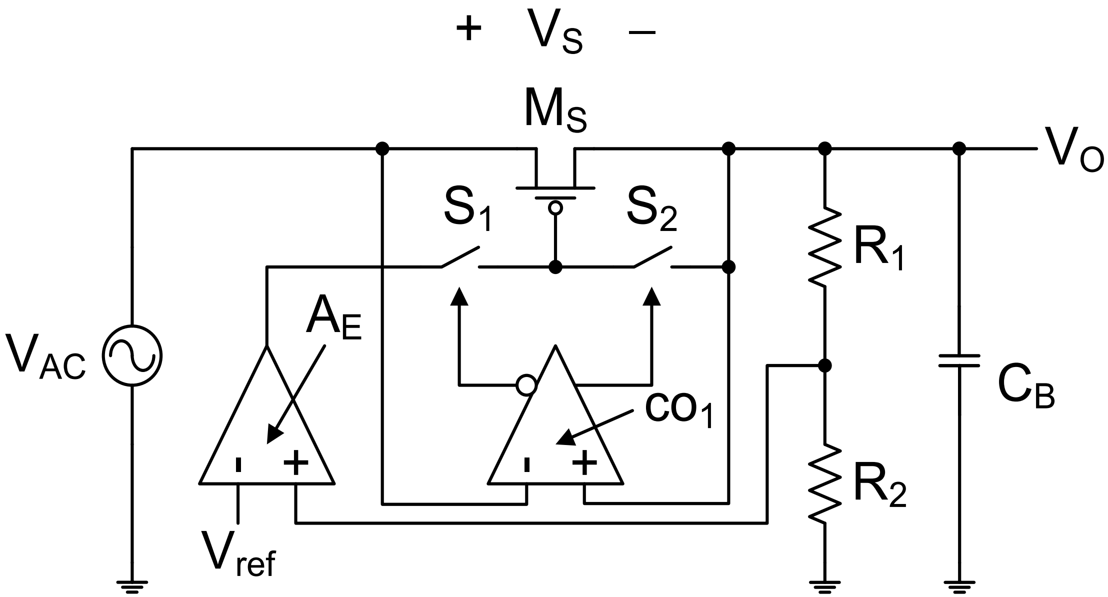


Conventional PMU Approach



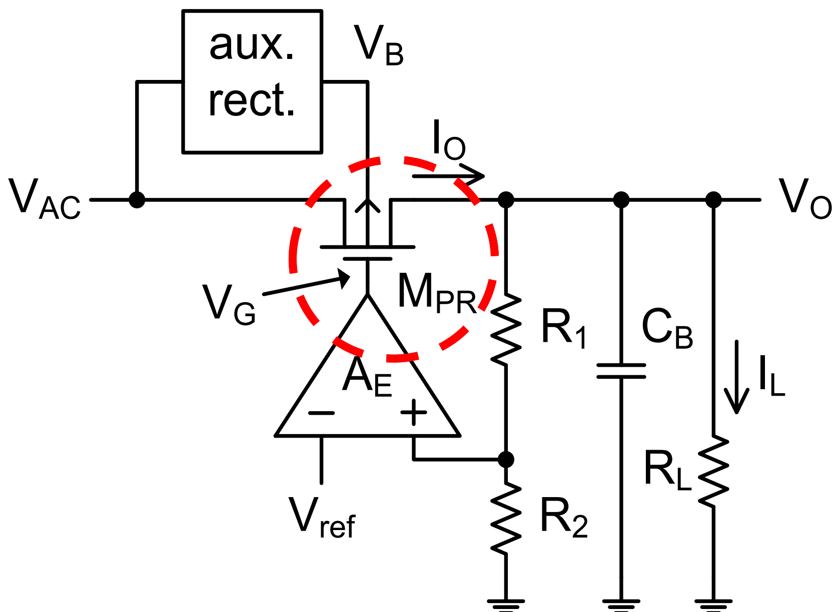
- Passive or active rectifier followed by linear regulator
- Min. peak V_{AC} → $\min[V_{ACP}] = V_O + V_{DO} + V_D$
- V_{DO}: Regulator dropout voltage
- V_D: Voltage drop on rectifier
- Limited power & voltage conversion eff. to 65 – 80%

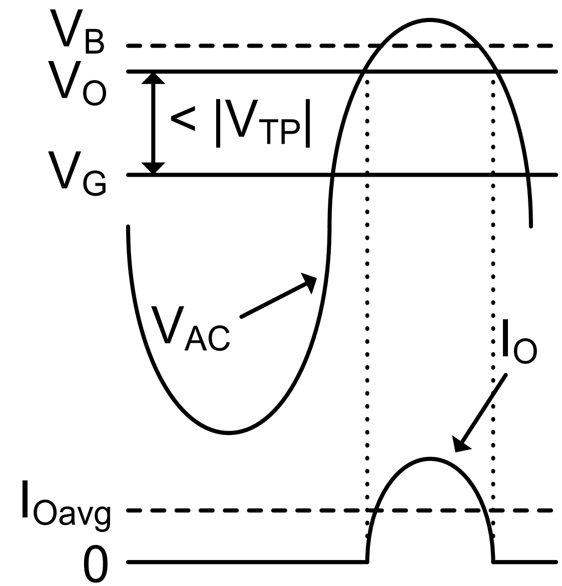
Active Rectifier/Regulator in [6]



- Combine PFETs in rectifier & regulator → ***rectulator***
- For $V_{AC} > V_O$, A_E drives M_S to have $V_O = (1 + R_1/R_2)\cdot V_{ref}$
- For $V_{AC} < V_O$, M_S is off → no current flow b/w V_{AC} & V_O
- Improve power & voltage conversion eff. (η_P & R_V)
- Input frequency (f_{AC}) limited by delay of CO_1

Proposed *Passive* Rectifier/Regulator (I)





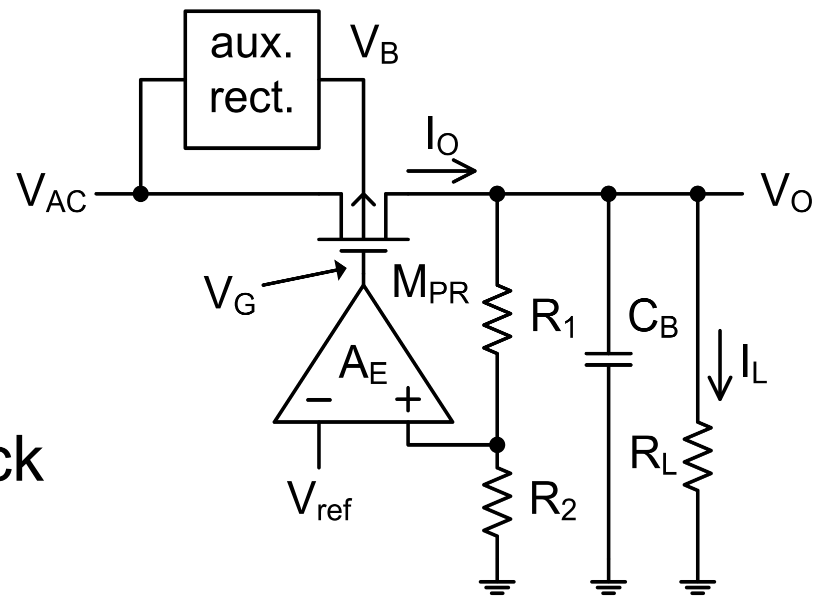
- Combine passive rectifier into regulator → ***prectulator***
- M_{PR} also used as passive rectifier **w/o using comparator**
- $V_B > V_O - V_{Di}$ & $V_{ACP} - V_{Di}$, (V_{Di} = parasitic diode drop)
- $I_O > 0$ for $V_{AC} > V_G + |V_{TP}|$
- V_O regulated to $(1+R_1/R_2) \cdot V_{ref}$ by A_E thru controlling I_O

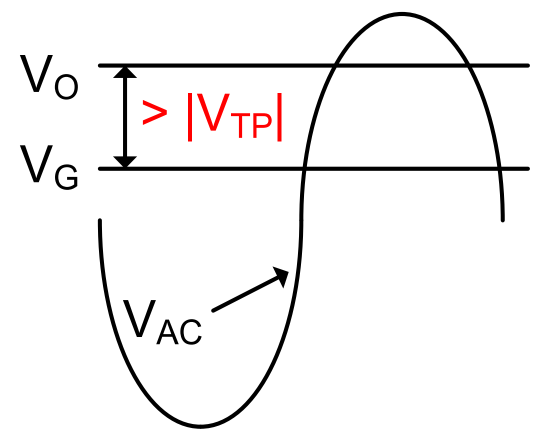
Proposed *Passive* Rectifier/Regulator (II)

- Startup situation
  - M_{PR} on for ↑ V_{AC} & $V_G \sim 0V$
  - But, $V_O < (1+R_1/R_2)\cdot V_{ref}$

    → A_E keeps $V_G \sim 0V$
  - $V_O > V_G + |V_{TP}|$ → I_O flow back
  - V_O stuck at low value
- Overload situation
  - Increase I_L → $V_G < V_O - |V_{TP}|$
  - I_O flow back to V_{AC}
  - Abrupt drop on V_O & η_P

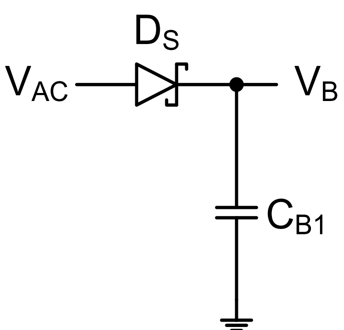
➢ A_E needs to keep $V_G > V_O - |V_{TP}|$



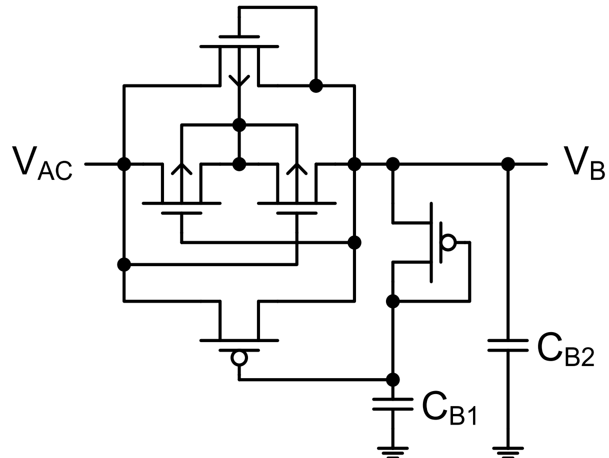


Proposed *Passive* Rectifier/Regulator (III)

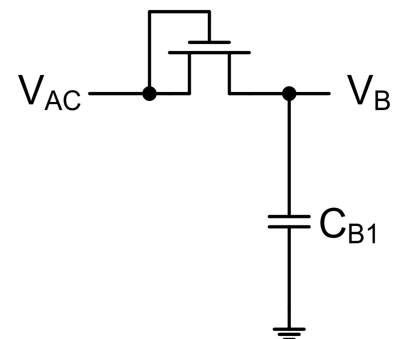
- Auxiliary rectifier designs with $V_D < 0.65V$



Schottky diode



Bootstrapping [3]

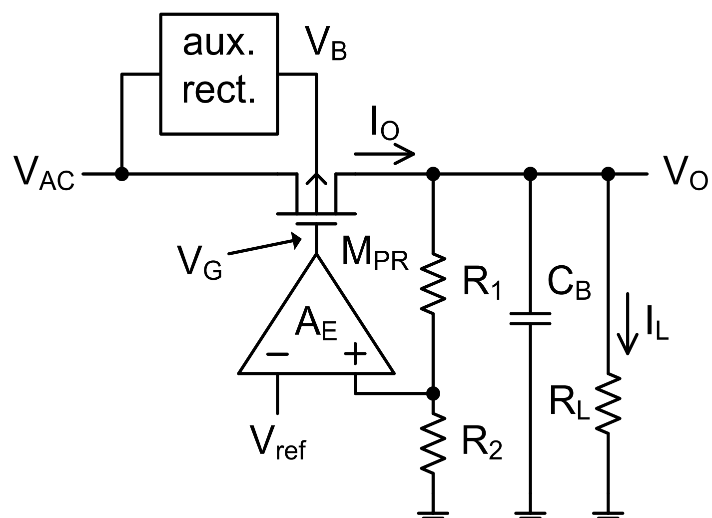


Low V_T MOS

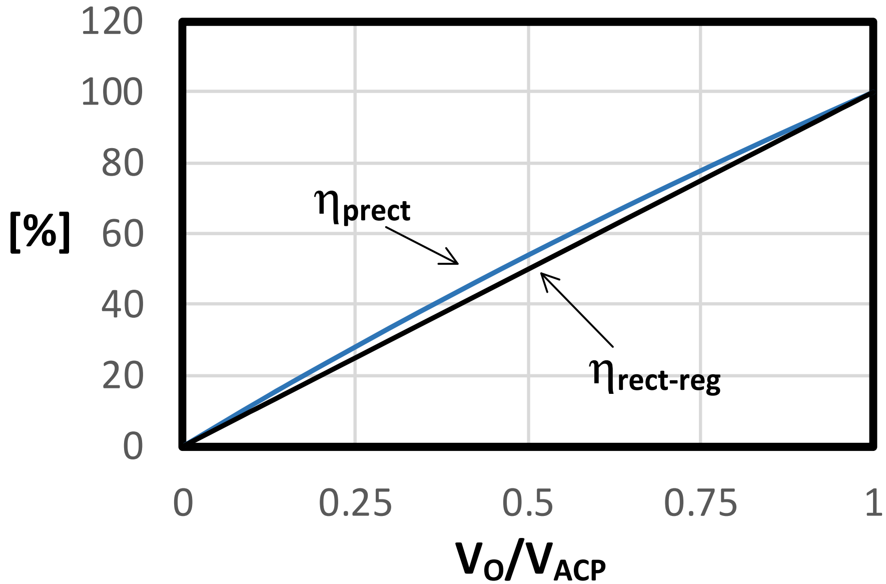
- Designed similar to regulator

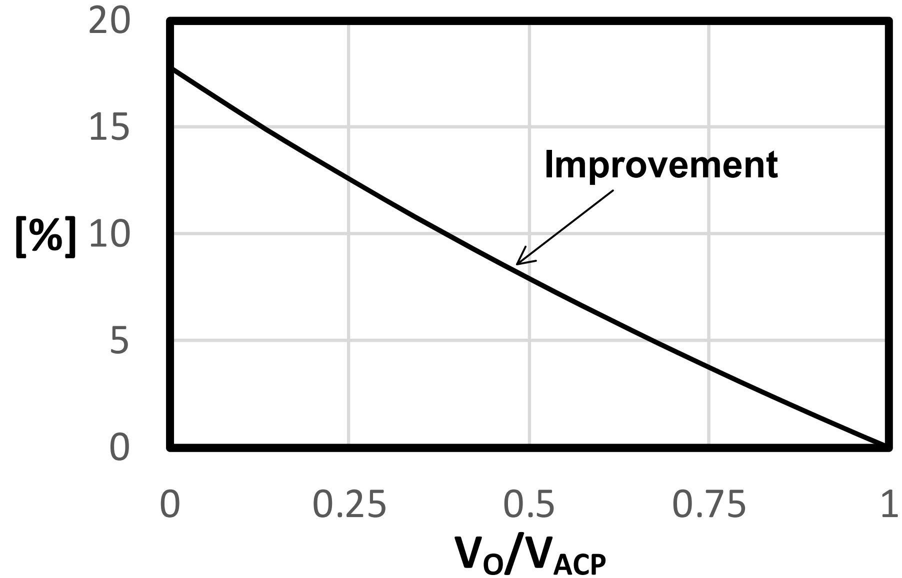
$$g_m \text{ of } M_{PR} \sim \sqrt{\frac{2}{\pi}\mu_P C_{OX}\frac{W}{L} I_L \cos^{-1}\frac{V_O}{V_{ACP}}}$$

for V_O approaching V_{ACP}



Comparison w/ Conventional Rect.-Reg.





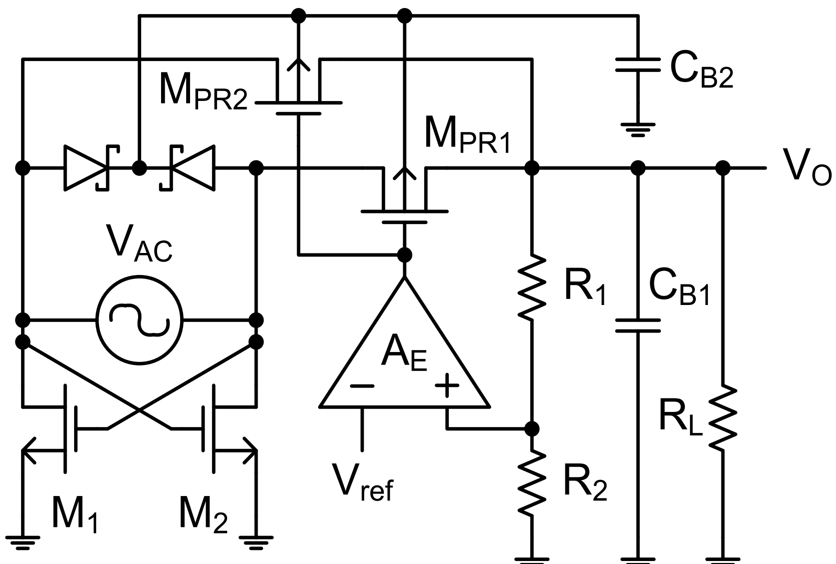
$$\eta_{rect-reg} = \frac{V_O}{V_{rect\_out}} = \frac{V_O}{V_{ACP}}$$

$$\eta_{prect} = \frac{V_O I_L}{\frac{1}{2\pi}\int_0^{2\pi} V_{ACP}\cos\theta \cdot I_O(\theta)\, d\theta}$$

$$\text{Improvement} = \frac{\eta_{prect} - \eta_{rect-reg}}{\eta_{rect-reg}}$$

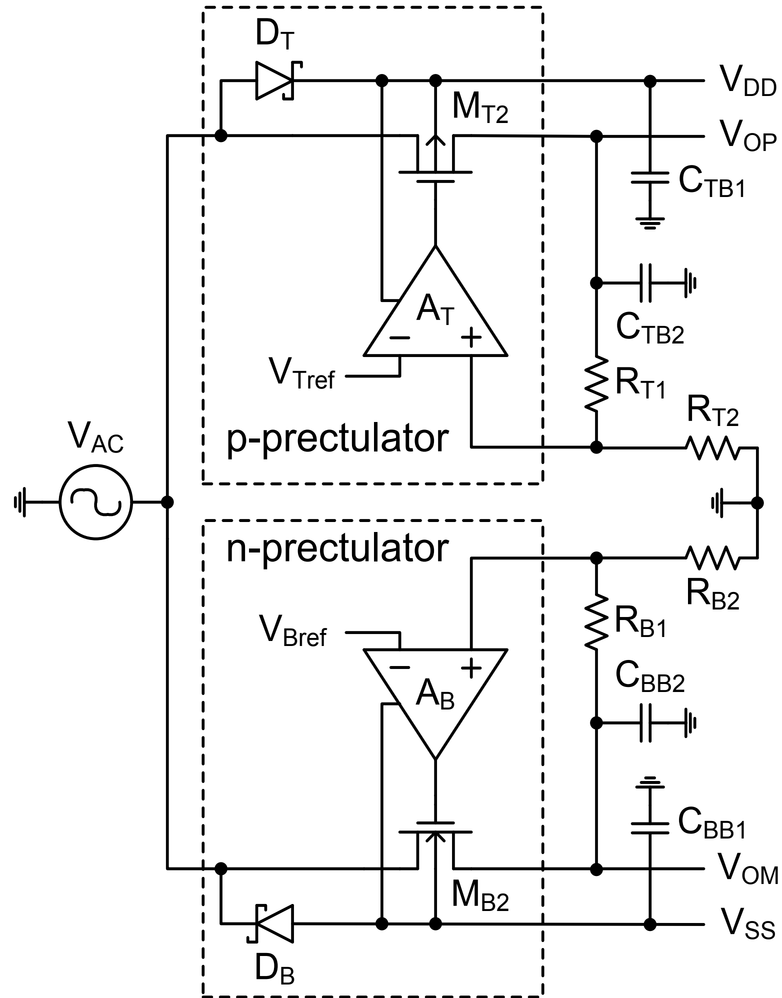
Different Prectulator Configurations

- Using both V_{AC} polarities

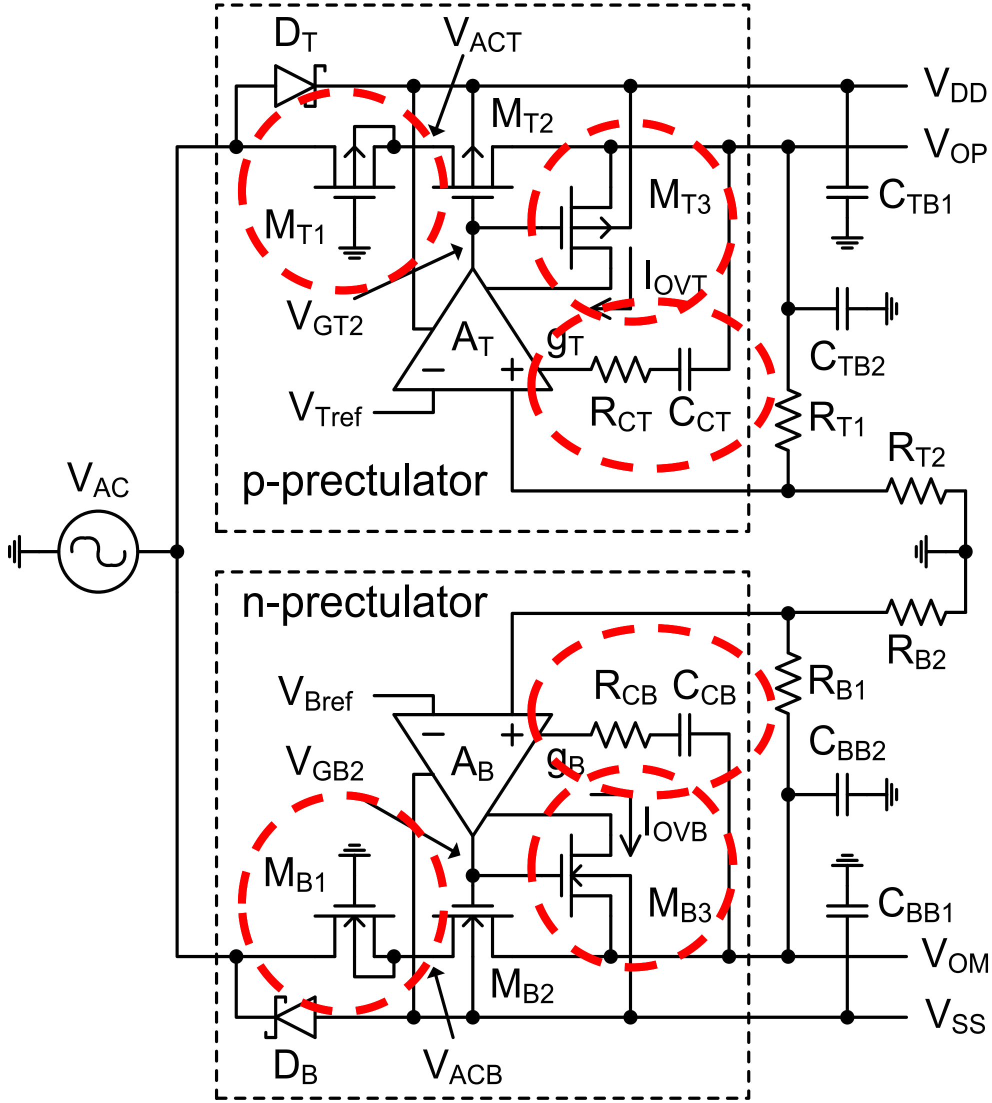


  - Multiple V_O's can also be obtained using multiple A_E's & M_{PR}'s

- Voltage doubling



Voltage doubling Prectulator Design

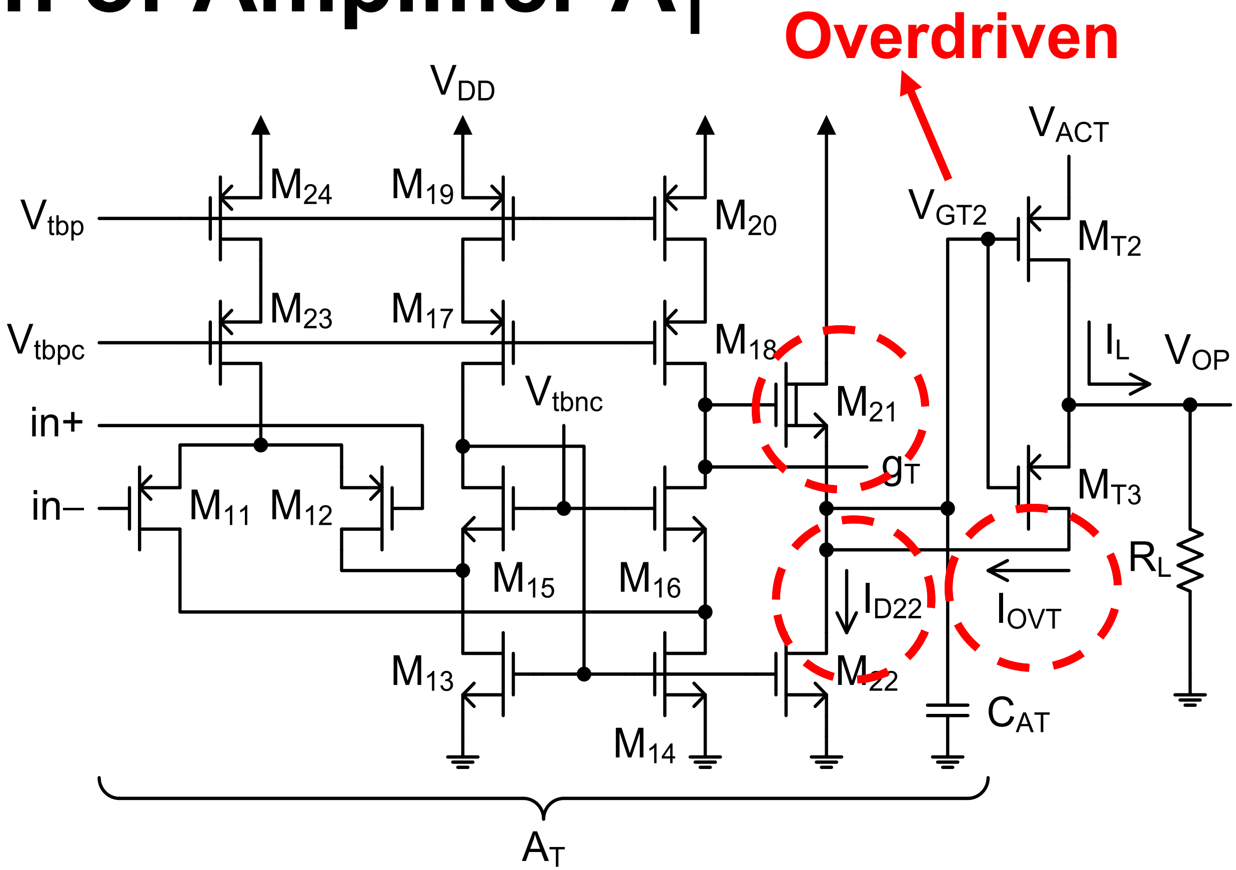


- M_{T1} used for limiting V_{ACT} b/w ~0V & $+V_{ACP}$
- M_{B1} used for limiting V_{ACB} b/w ~0V & $-V_{ACP}$

➢ Increase range of V_{AC}

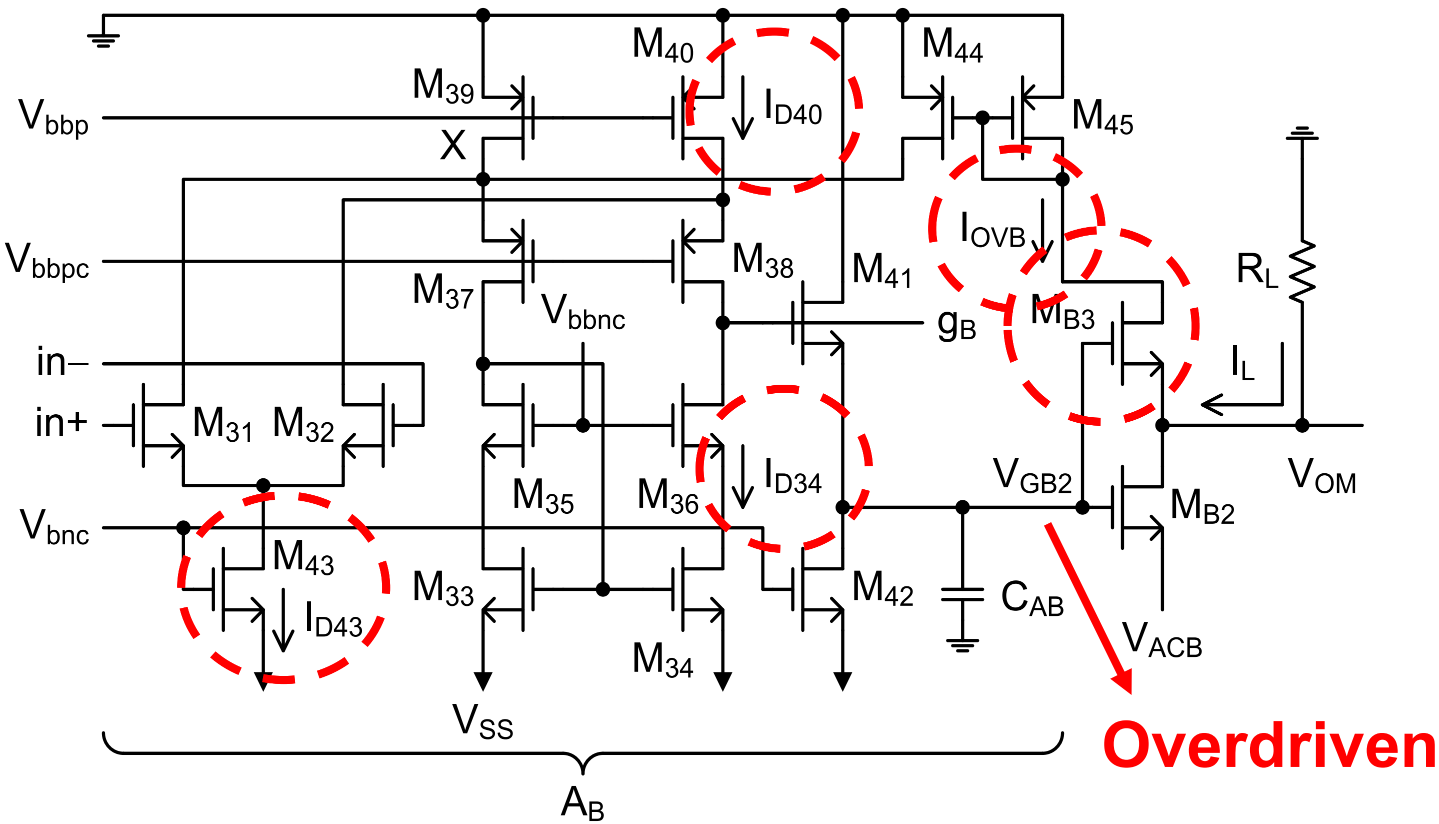
- M_{T3} added for detecting overdriven situations
  - $I_{OVT} > 0$ for $V_{GT2} < V_{OP} - |V_{TP}|$
- M_{B3} added similarly
- R_C's & C_C's added for freq. compensation

Design of Amplifier A_T



- For startup or high I_L situations with $V_{GT2} \sim V_{OP} - |V_{TP}|$ & $I_{OVT} \sim I_{D22}$, M_{21} is off → A_T not continue to drive V_{GT2} lower
- Prevent current flow back but V_O is no longer regulated

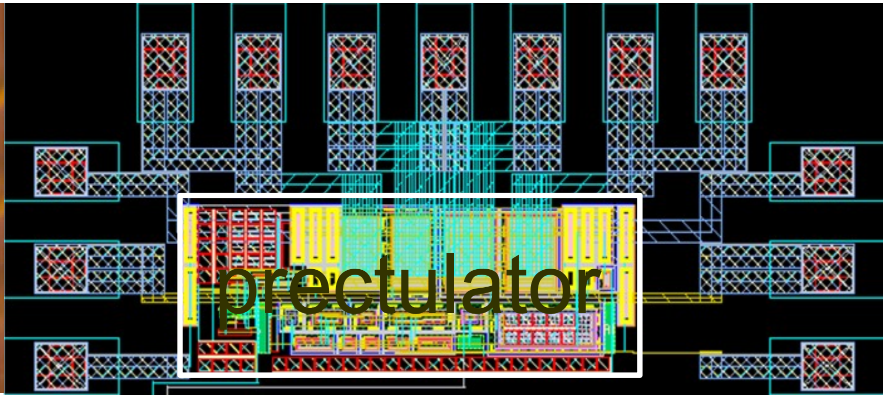
Design of Amplifier A_B



- $V_{GB2} \sim V_{OM} + V_{TN}$ & $I_{OVB} > 0$ for startup or high I_L situations
- I_{OVB} mirrored to node X → A_B no longer continues to drive V_{GB2} higher when $I_{OVB} \sim I_{D43}$ with $I_{D40} \sim I_{D34}$

Die Photo & Layout

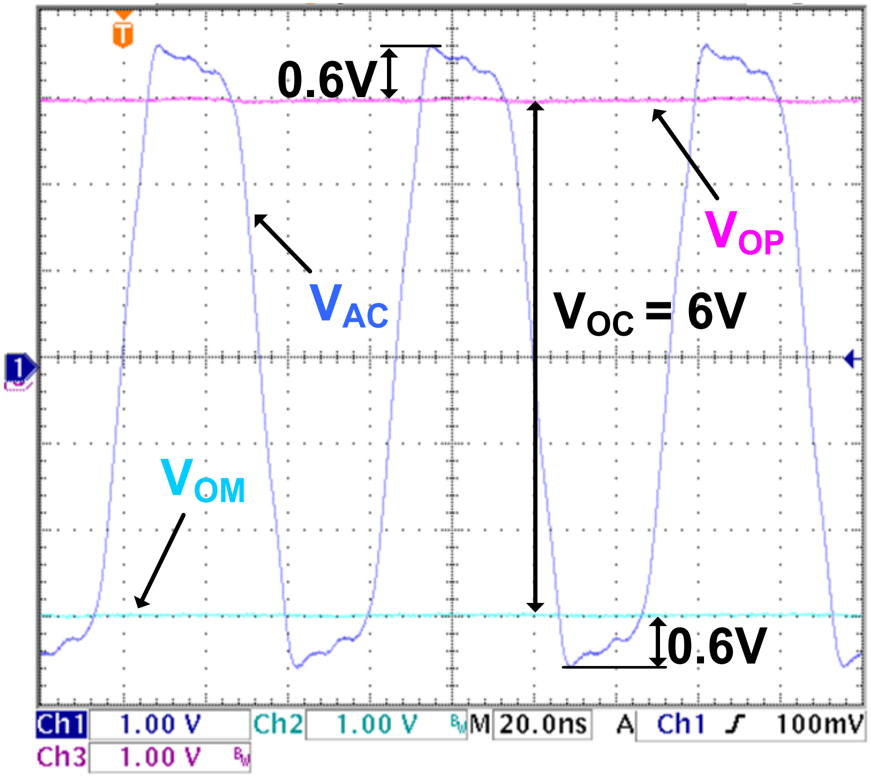
Die photo

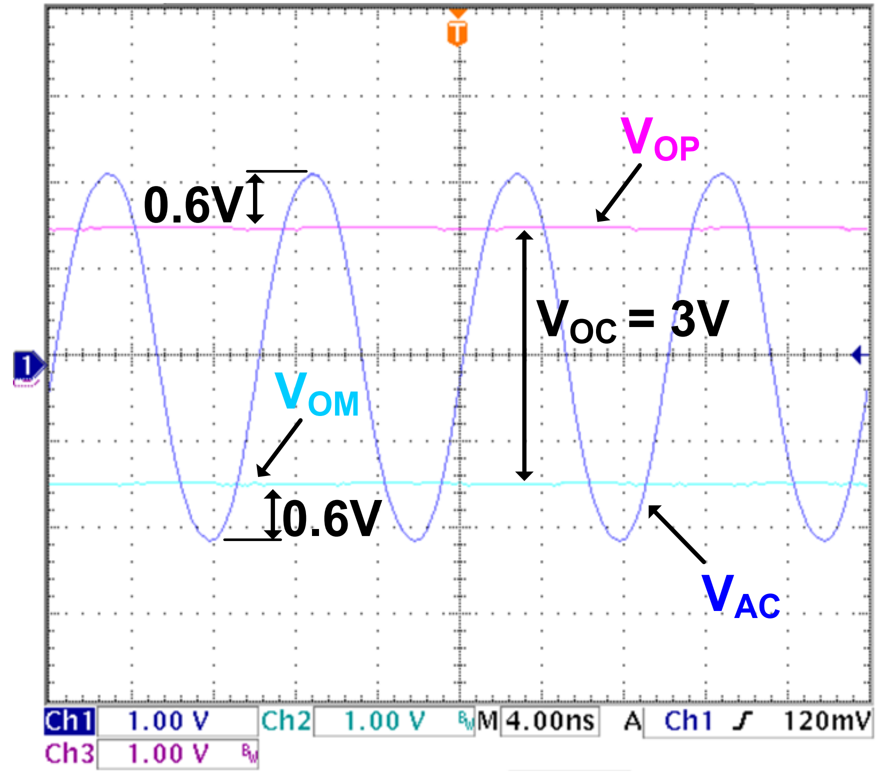


Layout

- Process: 0.18μm CMOS
- Active area: $560 \times 200 \mu m^2$
- Designed using 3.3V I/O devices
- Tested using 50Ω AC source w/ 10Ω resistor for input power (P_{in}) measurement
- Two 1μF caps connected to V_{OP} & V_{OM}

Experimental Output Waveforms

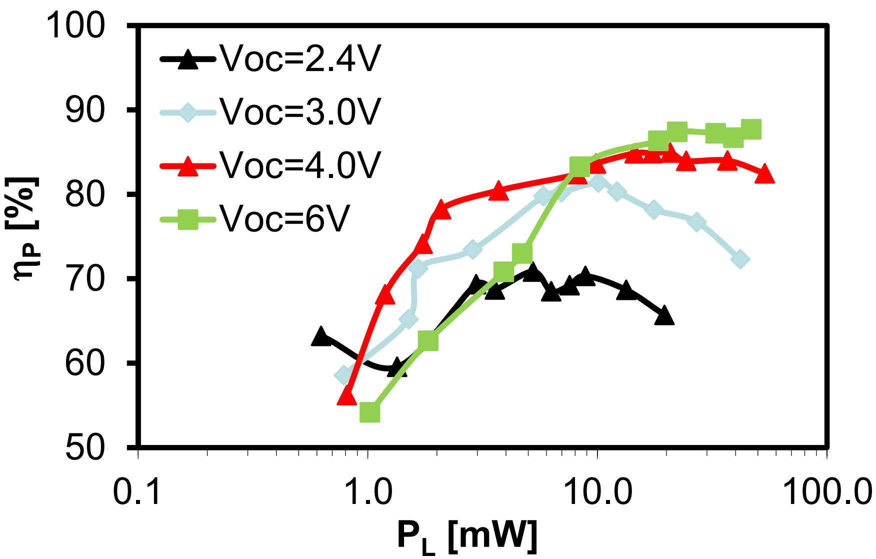


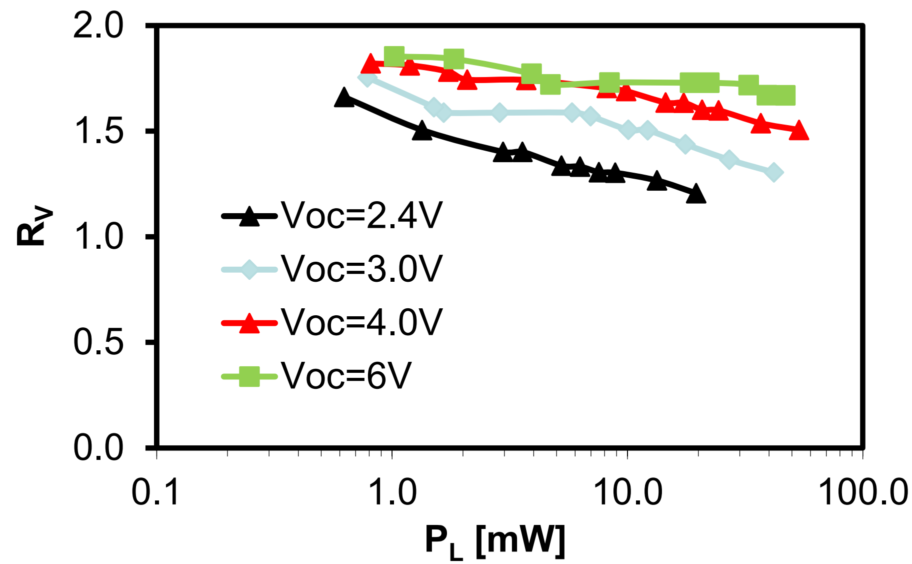


- f_{AC} = 15MHz, P_L = 46.8mW
- min[V_{ACP}] = 3.6V
- η_P @ min[V_{ACP}] = 87.7%
- $R_V = V_{OC}$/min[V_{ACP}] = 1.67

- f_{AC} = 100MHz, P_L = 8mW
- min[V_{ACP}] = 2.1V
- R_V = 1.42

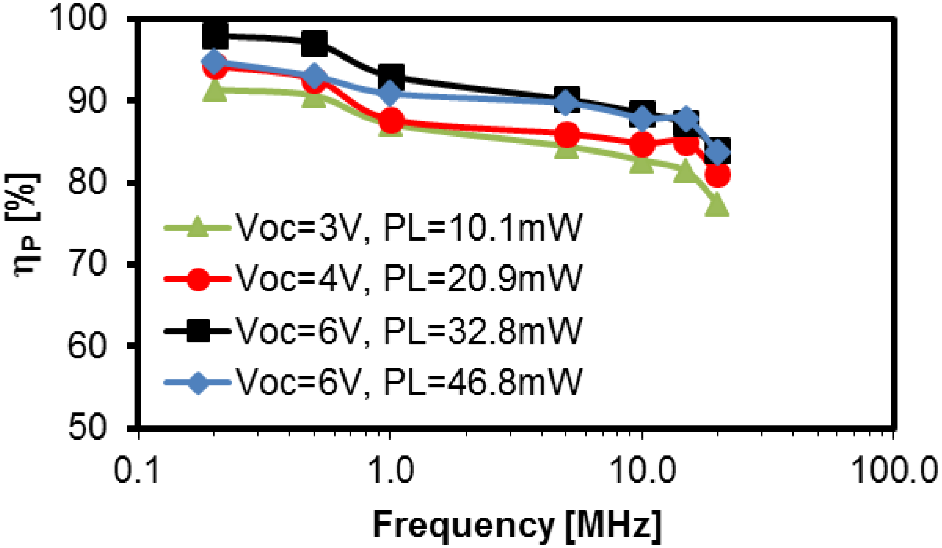
Measured η_P & R_V vs. P_L @ f_{AC} = 15MHz

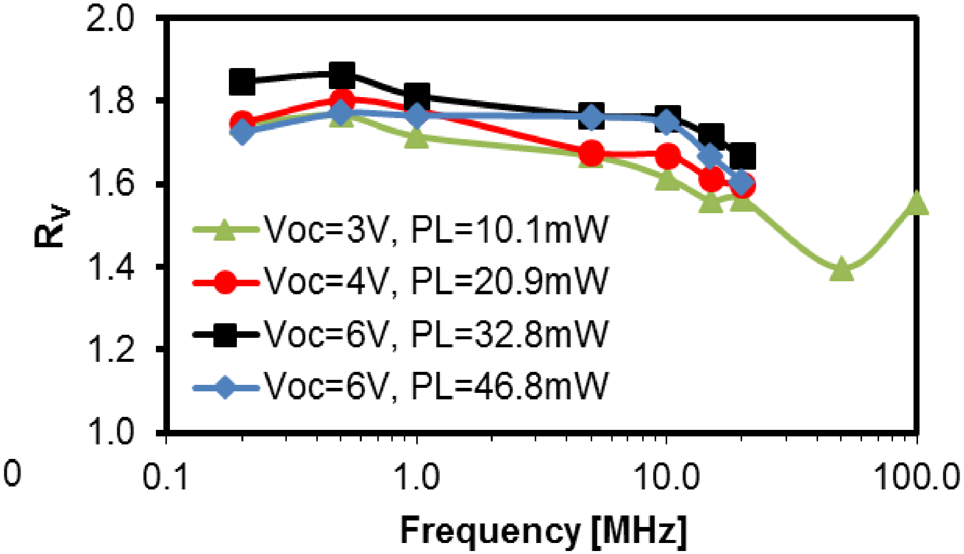




- max[η_P] ~ 87.7% & max[R_V] ~ 1.82 at V_{OC} = 6V
- η_P > 80% for P_L > 5mW & V_{OC} > 4V
- At overload situation (V_{OC} dropped 0.1V from 4V), η_P only dropped < 0.13% for P_L ~ 65mW
  - ➢ No significant current flow back

Measured η_P & R_V vs. f_{AC}

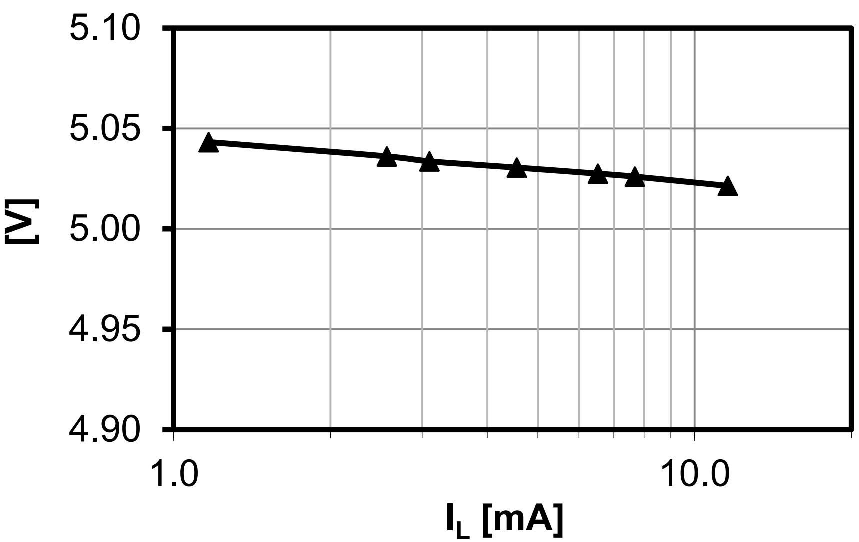




- η_P > 93% for $f_{AC} \leq$ 1MHz & V_{OC} > 4V
- max[η_P] @ 20MHz = 84.0%
- R_V > 1.7 for $f_{AC} \leq$ 1MHz; max[R_V] = 1.71 @ f_{AC} = 15MHz
- η_P & R_V degraded at high f_{AC}'s due to M_{T1} & M_{B1} added for reducing voltage stress & increasing ranges of V_{ACP} & V_{OC}

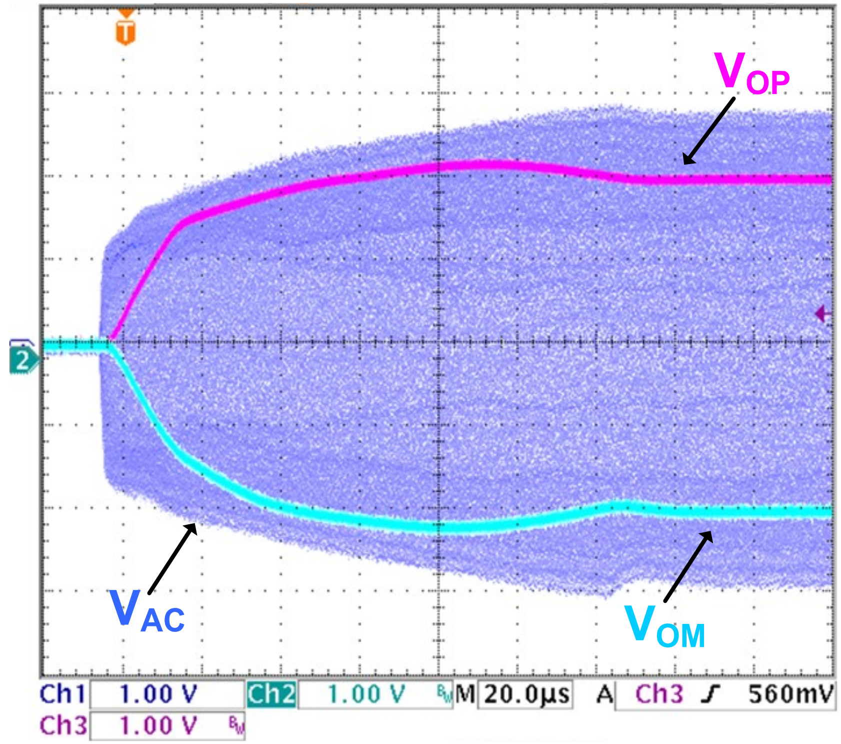
Load Regulation & Startup

- Load Regulation



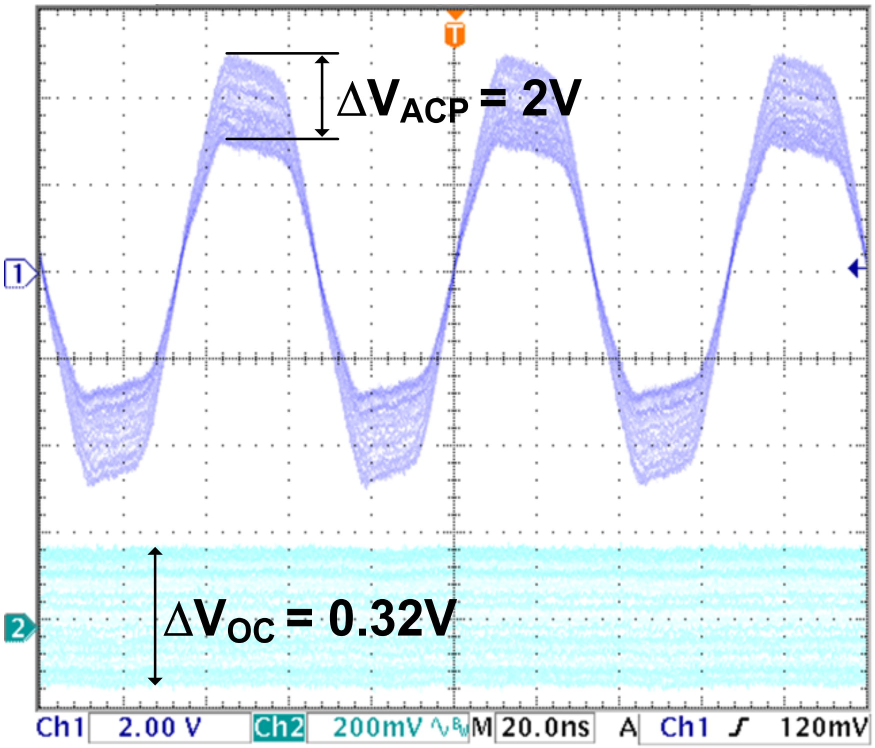
- f_{AC} = 15MHz
- V_{ACP} = 3.2V
- $\Delta V_{OC}/\Delta I_L = -1.9$mV/mA

- Startup

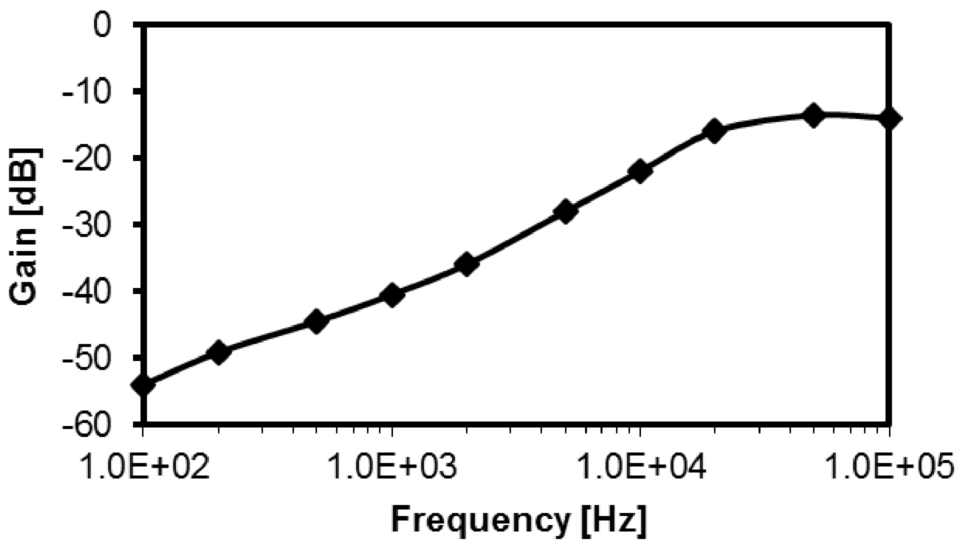


- f_{AC} = 15MHz
- R_L's @ V_{OP} & V_{OM} = 820Ω
- Startup time < 145µs

AM Rejection & Input Regulation



- $\Delta V_{OC}/\Delta V_{ACP}$ vs. f_{AM}



- f_{AM} = 20kHz & f_{AC} = 15MHz
- 2.8V < V_{ACP} < 4.8V with V_{OC} = 4V
- $\Delta V_{OC}/\Delta V_{ACP}$ = −15.9dB

- AM rejection limited by BWs of A_T & A_B @ high f_{AM}'s
- Input regulation = 1.1mV/V for f_{AM} = DC

Performance Comparison

	[4]	[5]	[6]	This work
Technology	0.18μm	0.35μm	0.18μm	0.18μm
Output range (V)	1.8	1.19 – 3.56	1.5 – 3.4	2.4 – 6.4
Active area	0.12mm^2	0.186mm^2	0.07mm^2	0.112mm^2
max[P_L]	40mW^A	24.8mW*	58.1mW	83.2mW
f_{AC} (MHz)	13.56	13.56	0.5 – 15	0.2 – >20
R_V	1.5^B	0.79 – 0.93*	0.57 – 0.96	1.4 – 1.86
max[η_P] (%) @ f_{AC} (Hz)	74.8 @ 13.56M	90.1* @ 13.56M	81.5 @ 15M	87.7 @ 15M 84.0 @ 20M
Load regulation	–	No	< 61μV/mA	< 1.9mV/mA

*rectifier only; ^{A}voltage doubler only; ^{B}including linear regulators

Summary and Conclusion

- ***Prectulator*** combined passive rectifier into linear regulator
- Regulator output transistor used both for output voltage regulation as well as rectification
- High speed comparators not required to achieve high f_{AC}
- Bulk voltage biased by low voltage drop auxiliary rectifier
- Gate voltage controlled by amp. for voltage regulation
- Startup & overload situations detected by other transistors that output currents to prevent amp. from overdriving
- Voltage doubling prectulator implemented in 0.18μm CMOS process
  - ➢ Achieved max[η_P] = 87.7% & max[R_V] = 1.71 @ 15MHz