Design of PVT Tolerant Inverter Based Circuits for Low Supply Voltages

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Talk Outline

- **Motivation**
  - Technology trends
  - Inverter amplifier vs differential pairs
- **Inverter based OTA design techniques**
  - Inverter biasing techniques (3)
  - Common mode rejection ratio
  - Cascoding in inverter circuits
  - Inverter based OTA design
- **Other inverter based designs**
  - ADC driver
  - Channel select filter
- **Conclusions**

Simulations & analysis

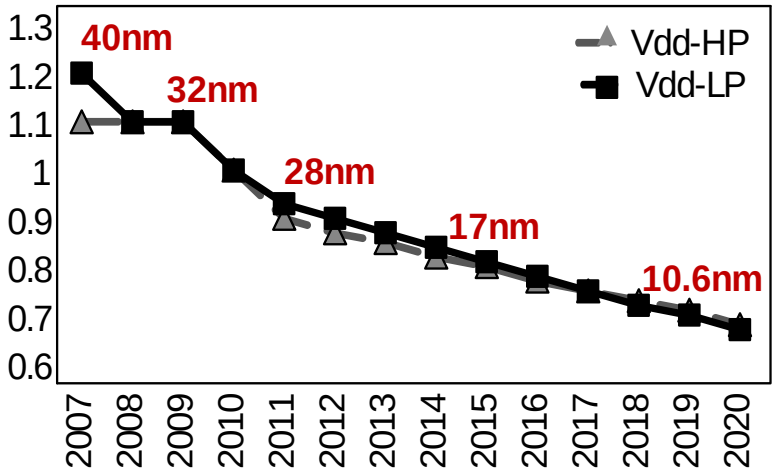
Three prototype designs

Technology Trends: Vdd

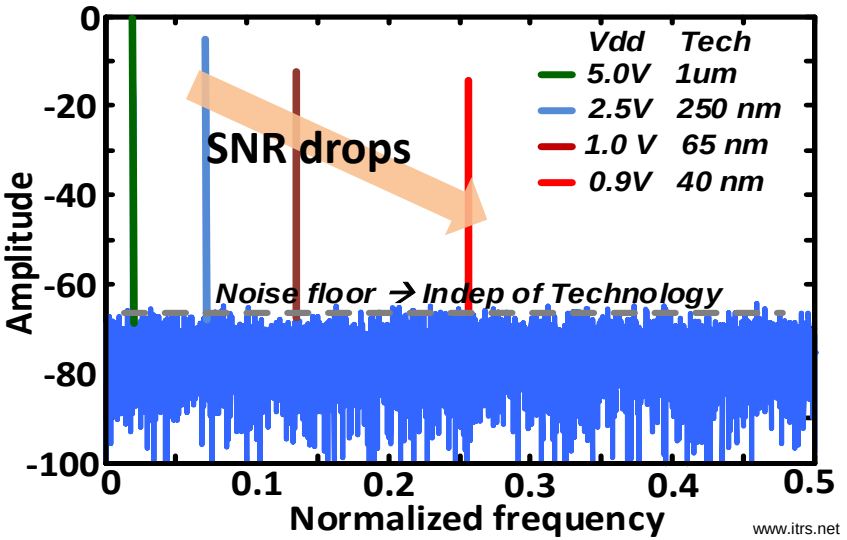
- **Smaller feature sizes (Moore)**
- **Digital**
  - Lower digital active power

$$P = CV^2 f + I_{leak} + I_{sc}$$

  - Low Vdd good for digital
- **Analog**
  - Reduces attainable SNR
  - Reduces output impedance
  - F_T increases but generally
  - Low Vdd bad for analog circuits
- **It is a Big "D" small "A" world**



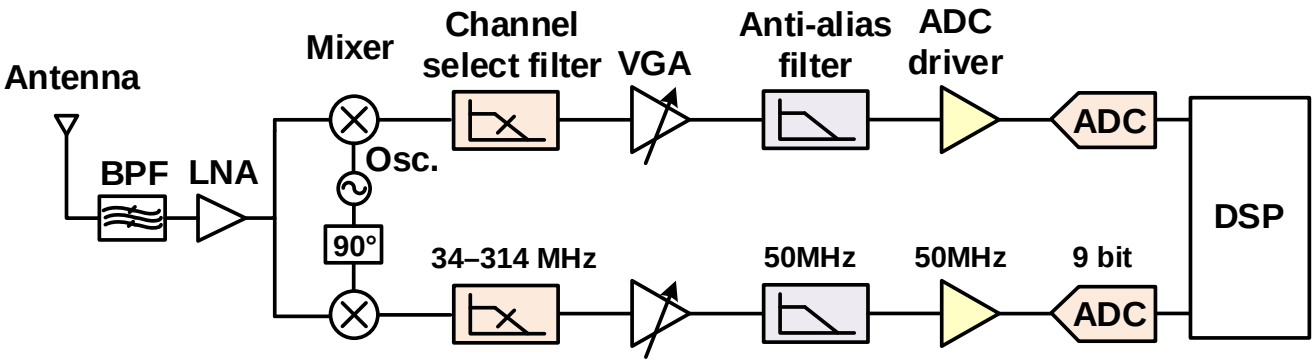
ITRS VDD Roadmap



Effect of Vdd scaling on SNR

Analog & Amplifiers

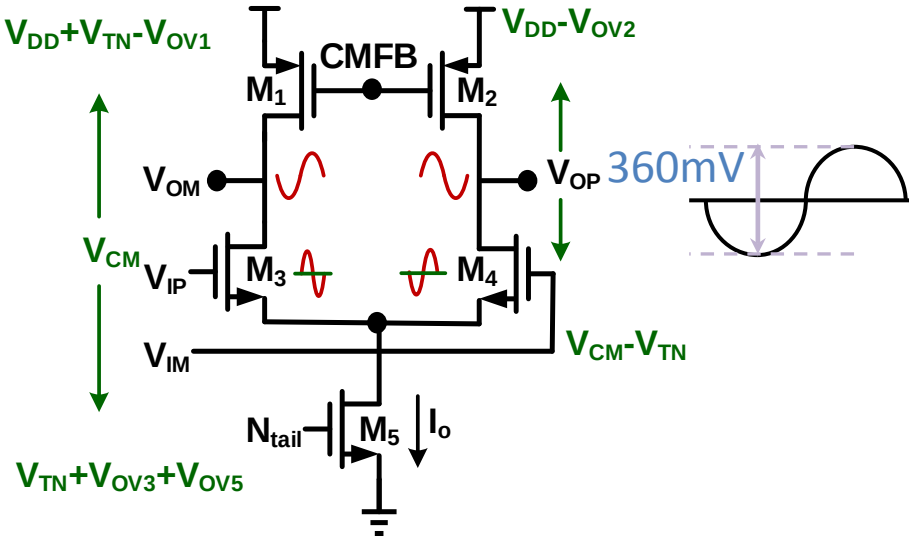
- **The world is analog**
  - Interface between world and digital is analog
  - Amplifiers, filters, drivers, sampler, ADC are inevitable
- **Amplifiers are everywhere**
  - E.g., low power wireless transceiver



Amplifiers are critical blocks in analog design

Traditional OTAs

- **Differential pair converts voltage to current**
- **Input /output DC voltage equal for cont. time systems**

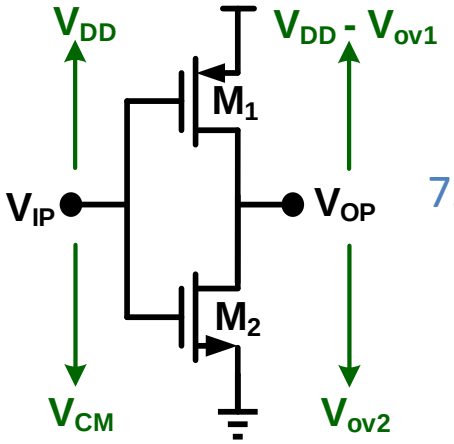


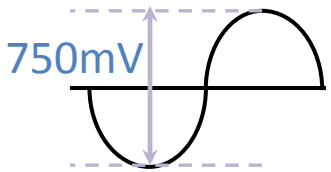
Example
Vdd=1V, Vtn=0.45V, Vtp= -0.45V
Common mode voltage = 0.69V
Max output amplitude = 360mV$_{pp}$

Traditional OTAs not suitable for lower Vdd

New Amplifiers: Inverters

- **Allow rail to rail input swings**





Example
Vdd=1V, Vtn=0.45V, Vtp= -0.45V
Common mode voltage = 0.5V
Max output amplitude = 750mV_{pp}

~2X higher swing

- **Maximum possible output swing in CMOS technology**

Inverters good for higher swings

Traditional OTA vs Inverter OTA: V_{PP}

- **Traditional OTA**
  - Vo_{max} limited by output
  - Vin_{min} limited by input

$$Vo_{\max} = Vdd - \Delta V$$

$$Vin_{\min} = 2\Delta V + V_{TN}^{'}$$

$$Vpp_{OTA} = Vdd - 3\Delta V - V_{TN}^{'}$$

- **Inverter**
  - Vo_{max} limited by output
  - Vo_{min} limited by output

$$Vo_{\max} = Vdd - \Delta V_{INV}$$

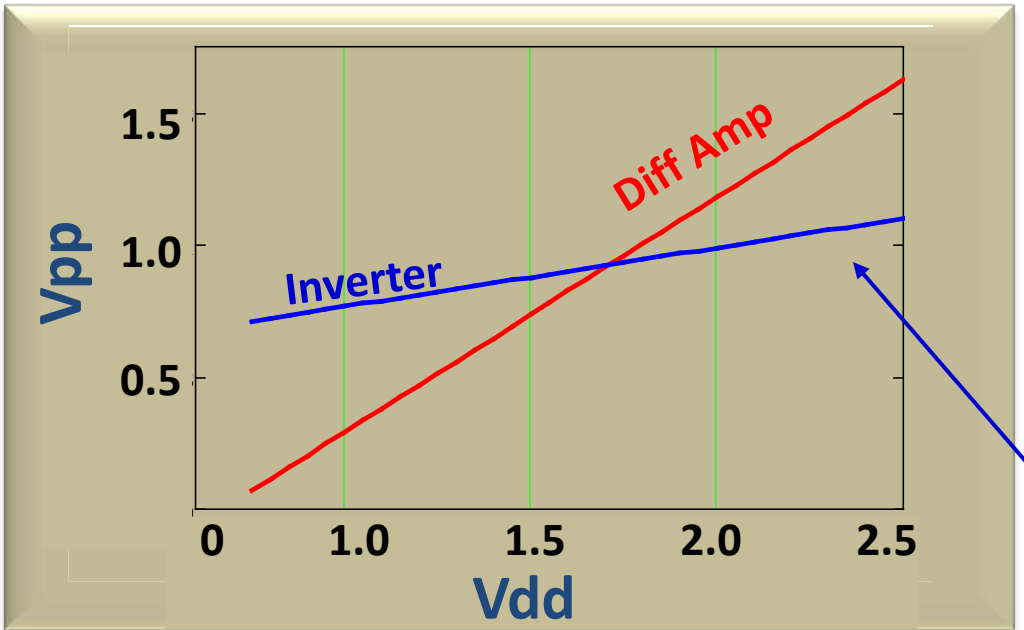
$$Vo_{\min} = \Delta V_{INV}$$

$$Vpp_{INV} = Vdd - 2\Delta V_{INV}$$

$$Vdd = V_{TN} + |V_{TP}| + 2\Delta V_{INV}$$

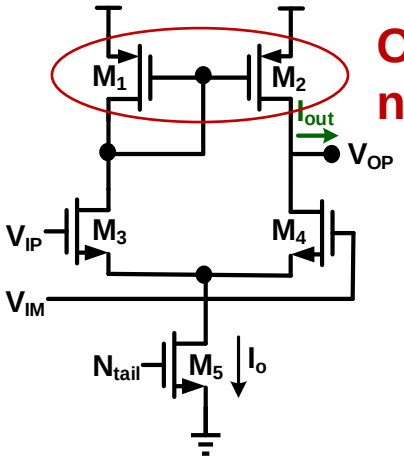
$$\Delta V_{INV} = \frac{Vdd - V_{TN} - |V_{TP}|}{2}$$

$$Vpp_{INV} = V_{TN} + |V_{TP}|$$

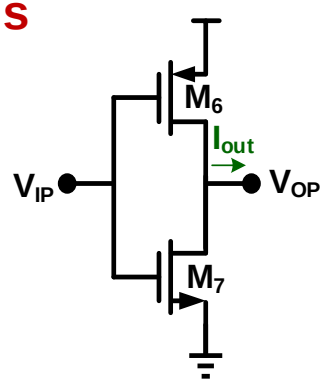


V_T scales slightly with VDD

Differential Pair vs Inverter: Noise



Only adds noise



Example

$gm_3 = gm_6 + gm_7 = 1mS$

$gm_1 = 0.5mS$

$\gamma = 2/3$

$$Vn_{diff}^2 = \frac{4kT\gamma}{g_{m3}}\left(1+\frac{g_{m1}}{g_{m3}}\right)$$

Excess noise factor

$$Vn_{inv}^2 = \frac{4kT\gamma}{g_{m6}+g_{m7}}$$

$Vn_{diff} = 4.9nV/\sqrt{Hz}$

$Vn_{inv} = 3.3nV/\sqrt{Hz}$

- **The load in differential pair contribute only noise**
- **The inverter transistors amplifies signals and adds noise**
- **Excess noise factor of inverter is 1 (< diff pair)**

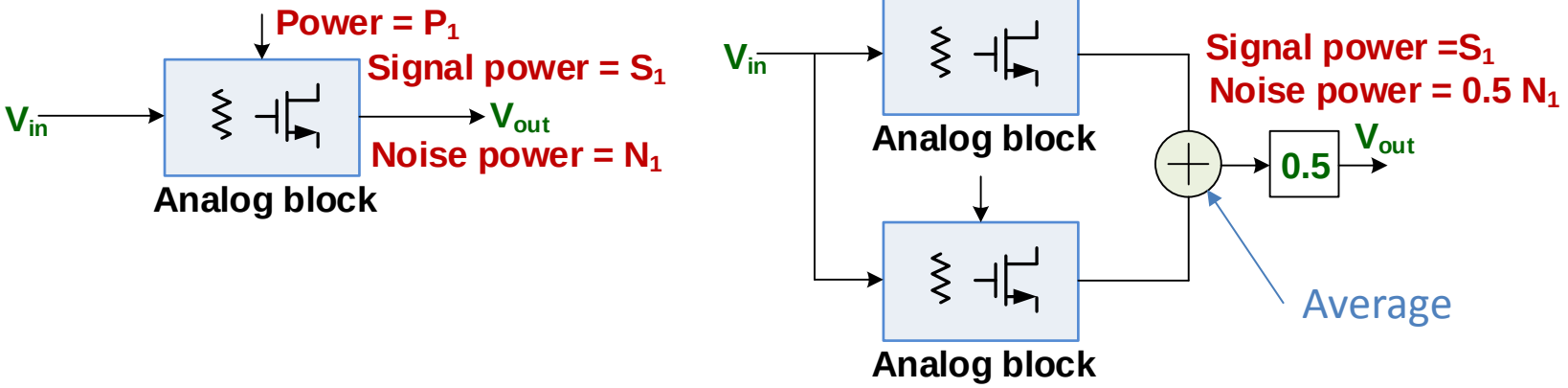
Inverters are less noisy than differential pairs

Differential Pair vs Inverter (II)

- **Multiple ways to compare performance**
  - Constant ΔV for all transistors for calculating gm
  - This comparison ignores signal swing (will look at SNR next)

	Diff Amplifier			Inverter		
Condition/Spec	**Io Total**	**Gm Total**	**Noise Input**	**Io Total**	**Gm Total**	**Noise Input**
		gm_3	$\frac{4kT\gamma}{gm_3}\left(1+\frac{gm_1}{gm_3}\right)$		gm_6+gm_7	$\frac{4kT\gamma}{gm_6+gm_7}$
Constant gm/Transistor	2	Gm	3	1	2Gm	1
Constant gm Total	4	Gm	1.5	1	Gm	1
Constant Power (Io)	Io	1	6	Io	4	1

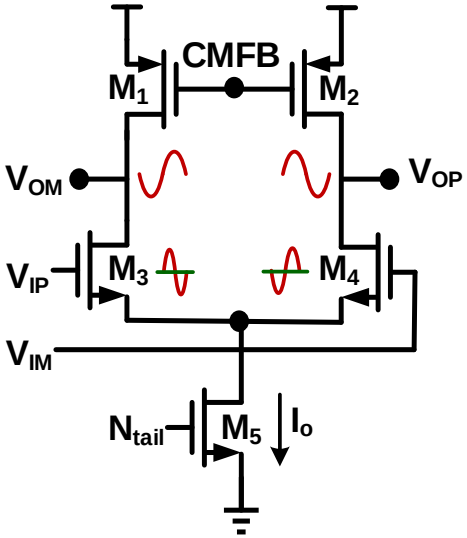
SNR vs Power Consumption

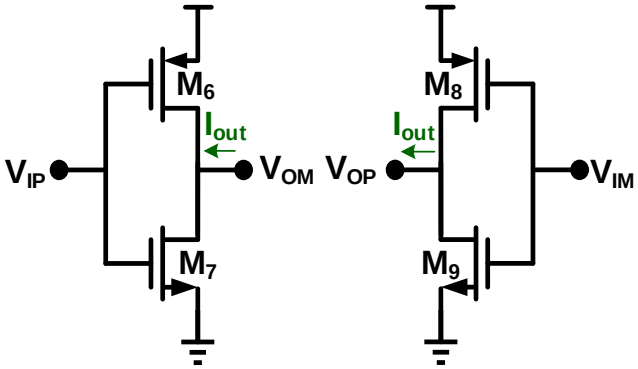


- **Analog block power is P_1, input referred noise N_1**
- **Averaging two analog blocks**
  - Increases power $2P_1$ and reduces noise power to 0.5 N1
  - SNR (10log(S1/0.5N1)) increases by 3dB

3dB higher SNR needs 2X power & 2X area

Swing vs Power Consumption



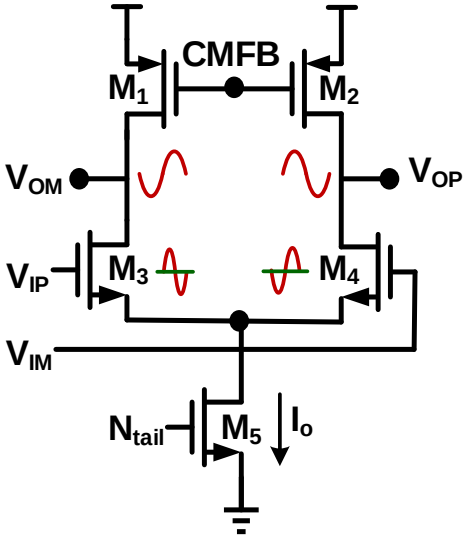


Vdd=1.0V

	Differential Pair	Inverter	Ratio
Swing (single-ended)	180mV	375mV	2.1X
Integrated noise (100MHz)	$50uV_{rms}$	$32uV_{rms}$	0.6X
SNR	68 dB	78 dB	10dB
Power	$V_{DD}I_o$	$0.5V_{DD}I_o$	1/2

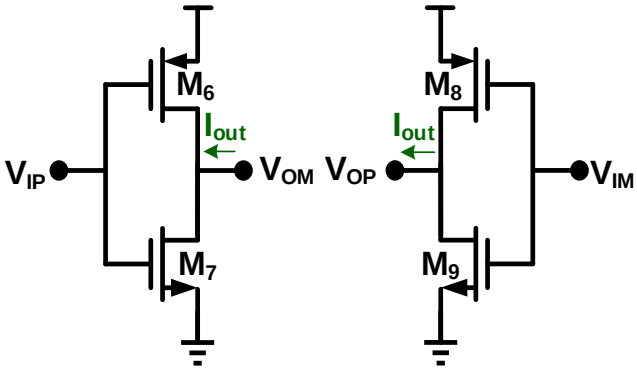
Constant gm / transistor $(gm_3 = gm_6 = gm_7)$

Swing vs Power Consumption (II)



	Diff Pair	Inverter
SNR	68 dB	78 dB
Power	$V_{DD}I_o$	$0.5V_{DD}I_o$

Vdd=1.0V



- **Every doubling of power increases SNR by 3dB**
- **In order to maintain same SNR of 78dB for diff pair**
  - Power of differential pair = 8VDDIo
- **Inverter provides the same SNR at 0.5VDDIo**

@1V Vdd inverters are 16X more power efficient

Linear Circuits From Quadratic Devices

- **How do we get linear gain from a differential pair when the devices themselves are quadratic?**

$$I_1 = \beta\left[\left(Vb + \Delta V\right)^2\right], \qquad I_2 = \beta\left[\left(Vb - \Delta V\right)^2\right]$$

$$I_1 - I_2 = \beta\left[\left(Vb + \Delta V\right)^2 - \left(Vb - \Delta V\right)^2\right]$$

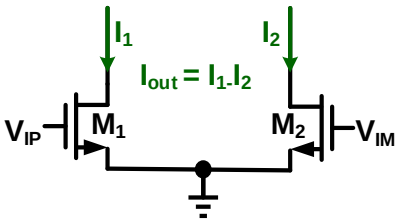
$$= \beta\left[\left(Vb^2 + 2Vb\cdot\Delta V + \Delta V^2\right) - \left(Vb^2 - 2Vb\cdot\Delta V + \Delta V^2\right)\right]$$

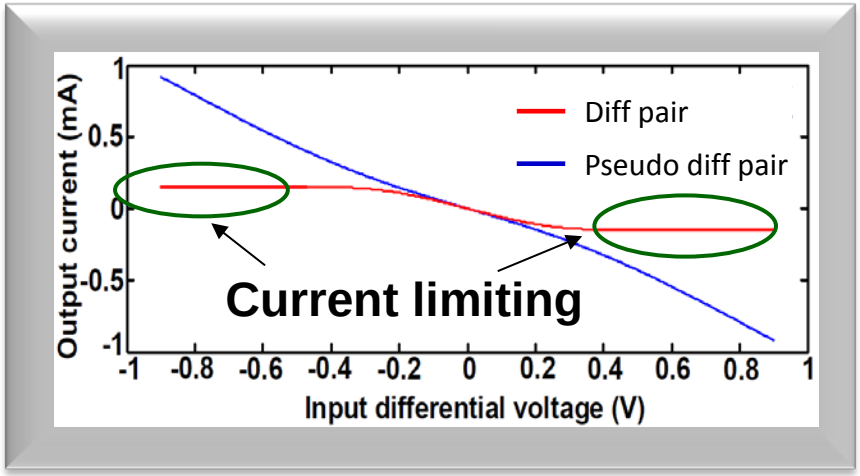
$$= 4\beta\cdot Vb\cdot\Delta V$$

- **The difference between two quadratics is linear provided we add some and subtract some**
- **One current increases while the other decreases**
- **For single ended -> quadratic cancellation for same β**

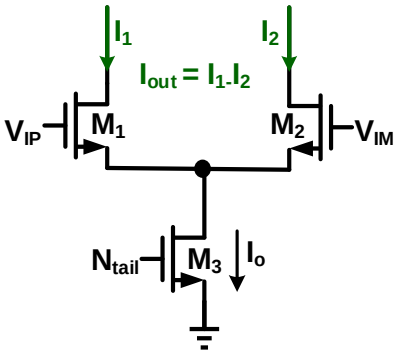
Effect Of Tail Current Source

(Pseudo differential pair)





(Differential pair)



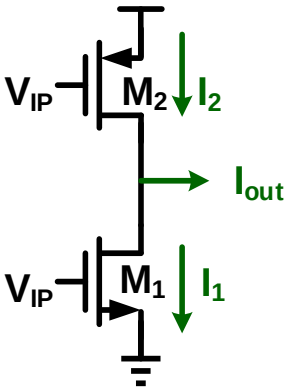
$$I_{out} = -(V_{IP} - V_{IM})2\beta_n V_{TN}$$

$$I_{out} = -(V_{IP} - V_{IM})\beta_n \sqrt{\frac{2I_0}{\beta_n} - (V_{IP} - V_{IM})^2}$$

- **Pseudo differential pair is highly linear**
  - Poor CMRR, poor PVT tolerance
- **Current limiting in differential pair creates non-linearity**
  - Good CMRR, high PVT tolerance

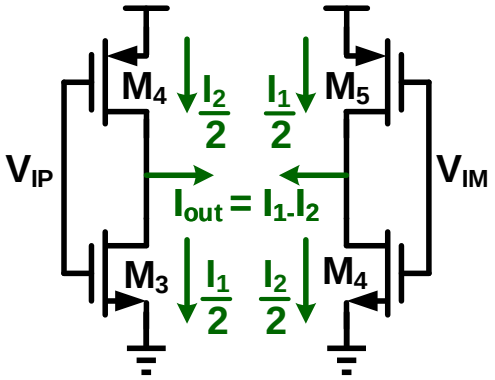
Current limiting results in nonlinearity

Inverter → Current Reuse Pseudo Diff Pair



$$I_{out} = I_2 - I_1$$

- **When V_{IP} increases**
  - I_1 increases
  - I_2 decreases



$$I_{out} = -(V_{IP} - V_{IM})\left[\beta_p (V_{DD} - V_{TP}) - \beta_n V_{TN}\right]$$

- **Inverters → current reuse pseudo differential pair**
- **Inverters are highly linear**
  - No current limiting, class-AB operation
  - Poor CMRR, poor PVT tolerance

Inverters are highly linear, Poor PVT, Poor CMRR

Differential Pair vs Inverter: Summary

- **Inverter based circuits**
  - High linearity, low noise, high slew rate & high swing
  - Poor CMRR, poor PSRR, poor PVT tolerance

	Differential pair	Inverter
Swing	Low	High
Linearity	Low	High
Noise	High	Low
Slew rate	Low	High
CMRR	High	Low
PSRR	High	Low
PVT Tolerance	High	Low

Tutorial Focus

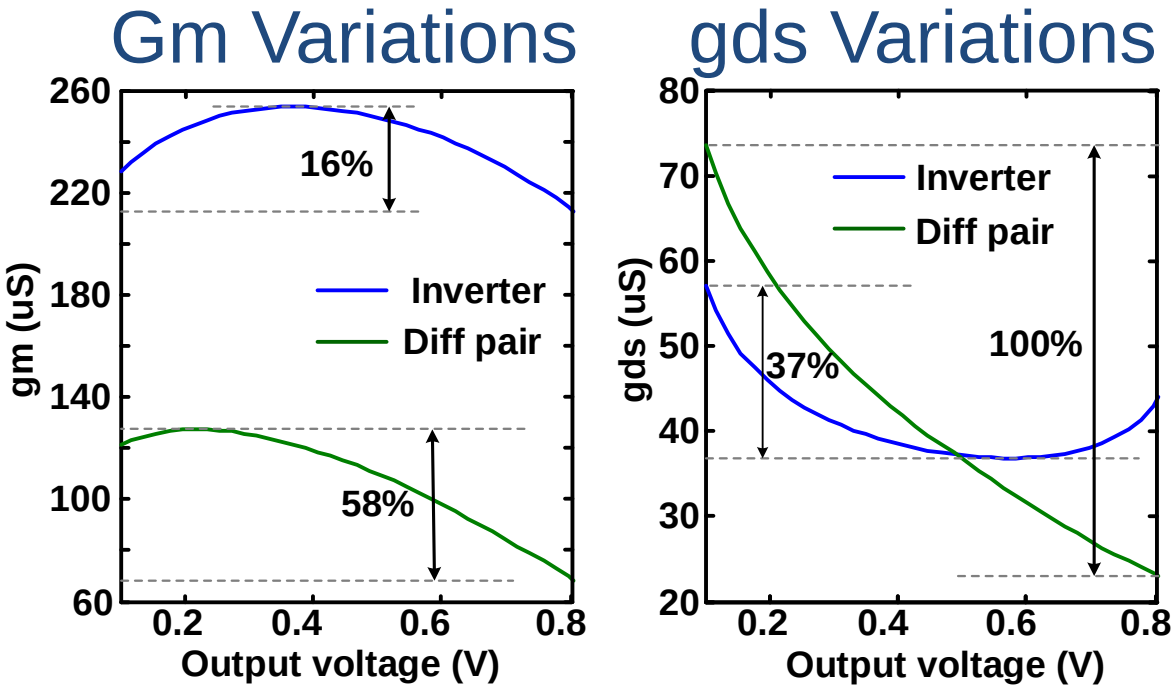
Talk Outline

- **Motivation**
  - Technology trends
  - Inverter amplifier vs differential pairs
- **Inverter based OTA design techniques**
  - Inverter biasing techniques (3)
  - Common mode rejection ratio
  - Cascoding in inverter circuits
  - Inverter based OTA design
- **Other inverter based designs**
  - ADC driver
  - Channel select filter
- **Conclusions**

Simulations & analysis

Three prototype designs

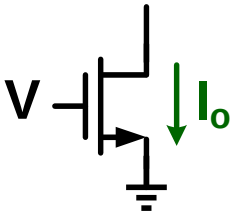
Gm/gds Variation with Signal Swing

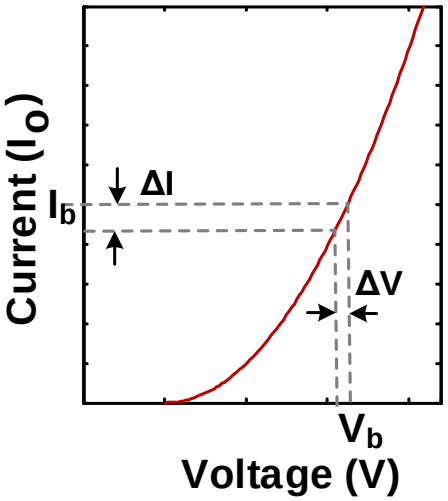


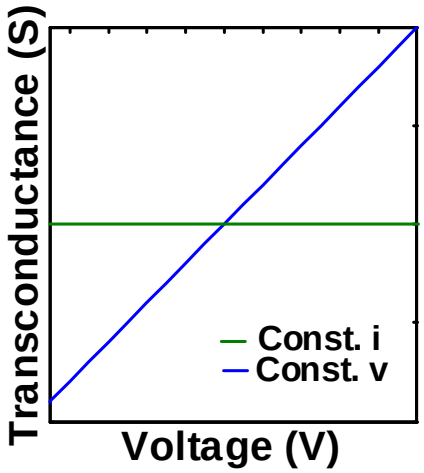
- **Signal swing changes the dc operating parameters**
- **Inverters are push pull amplifiers**
  - Gm variation is only 16% compared to 58% in diff pair
  - Gds variation is only 37% compared to 100% in diff pair

Inverters have less gain variation

Why Biasing Is Important ?







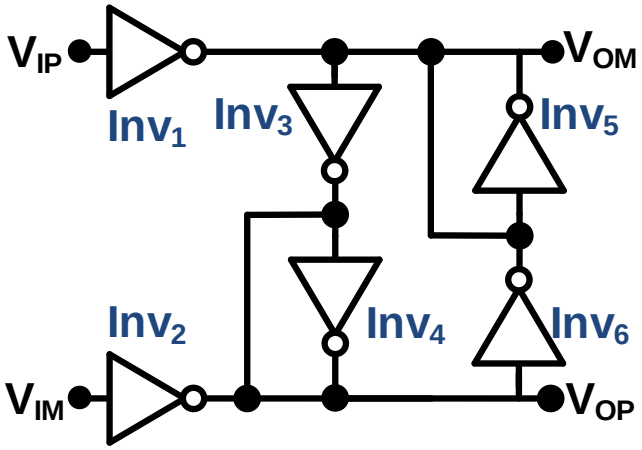
$$g_m = \sqrt{2 I_b \mu_n c_{ox} \frac{W}{L}}$$ (Const.i)

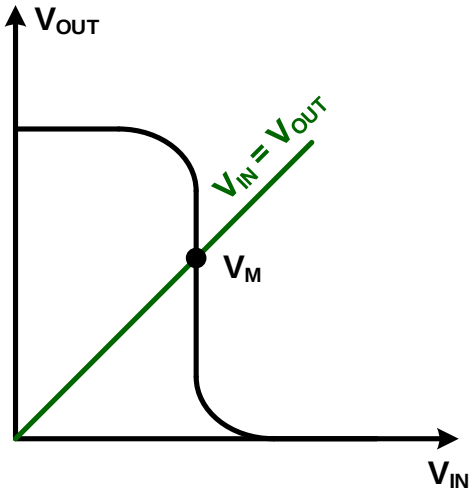
$$g_m = \mu_n c_{ox} \frac{W}{L}\left(V_b - V_{TN}\right)$$ (Const.V)

- **Biasing determines PVT tolerance**
  - Voltage biasing (Inverter): ΔV increase in V_b → larger increase in I_b
  - Current biasing (Diff pair): ΔI increase in I_b → smaller increase in V_b
- **It determines the optimal gain and linearity**

Current biasing better than voltage biasing

Traditional Inverter Biasing: Prior Work



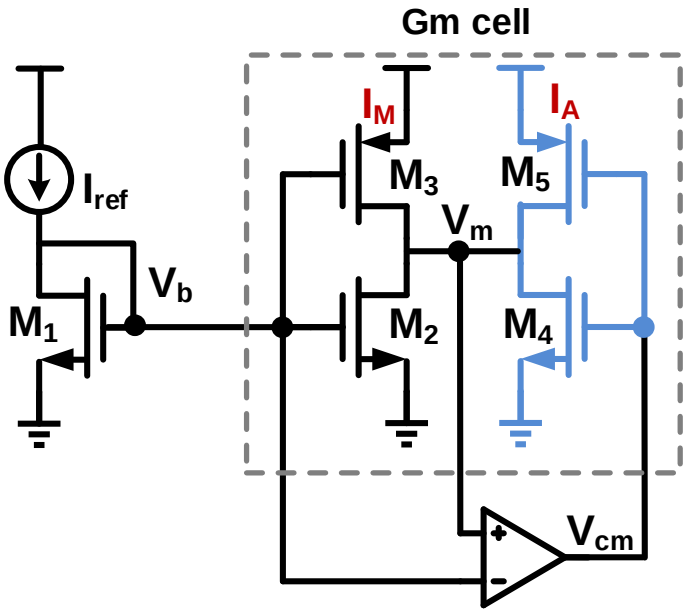


- $Inv_{4\text{-}5}$ sets the output bias point for inverters
- Metastable biasing (max trans conductance biasing)
- Current and transconductance varies across PVT
- Inverter parameter depends on input common mode

Ref: [9] Nauta, JSSC Feb 1992

Semi Constant Current Biasing (SCCB)

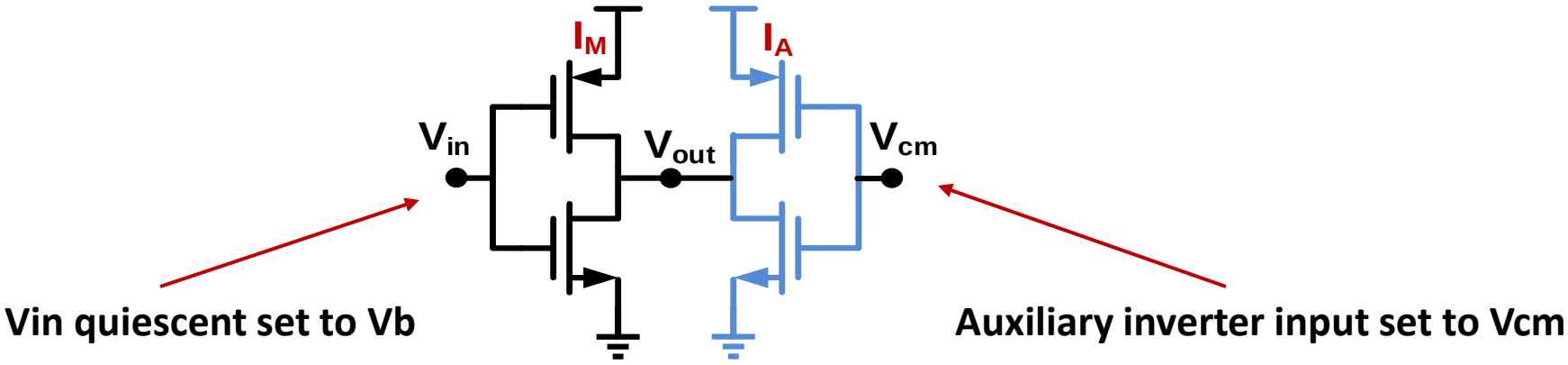
- **Bias voltage (V_b) is derived from NMOS current**
  - NMOS (M_2) current is constant
  - PMOS (M_3) current varies with Vdd
- **Input (V_b) and output voltages (V_m) are made equal**
  - Auxiliary inverter with negative feedback
  - Overall variation in gm is small



$$\left[\frac{W}{L}\right]_{M_3} = \left[\frac{W}{L}\right]_{M_2}$$

SCCB: Circuit Usage

- **Auxiliary inverter is used along with main inverter**
- **NMOS transconductance variation is reduced**
- **PMOS current is determined by negative feedback**
  - It varies with PVT, PMOS is weaker → less impact
- **NMOS gm > PMOS gm**
  - Overall variation is gm is small

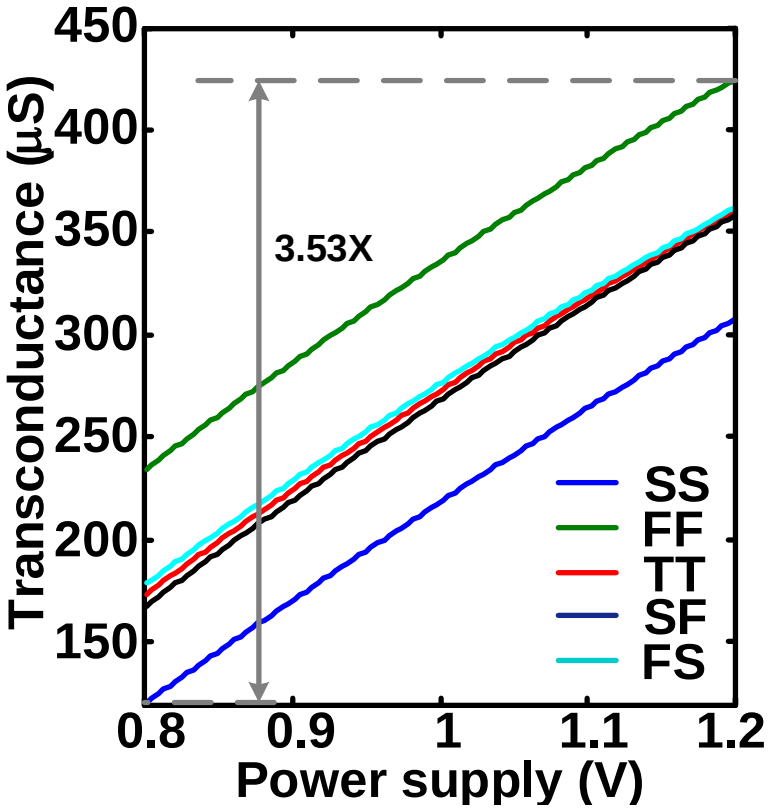


Use of SCCB biased inverters

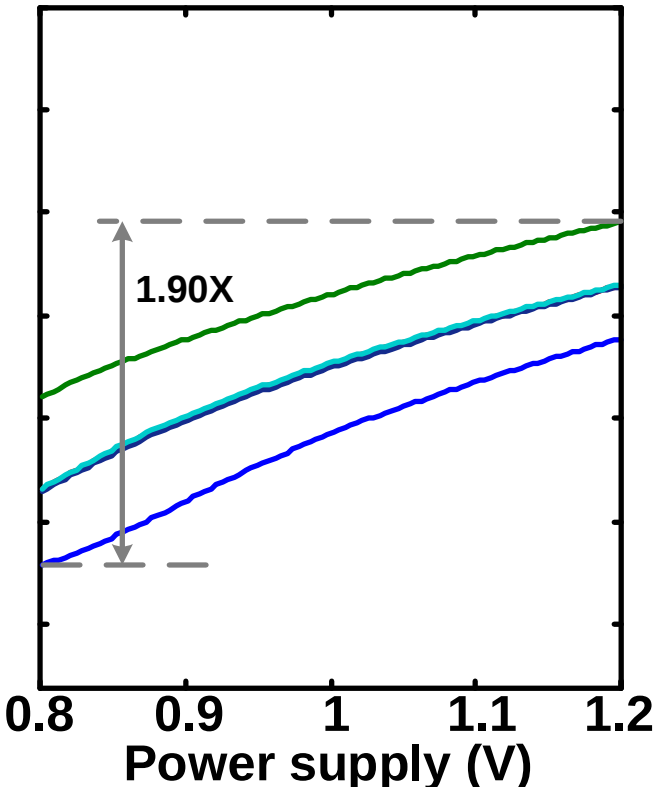
SCCB: Simulation Results

- **Variation in gm is reduced by 50%**

Traditional metastable biasing

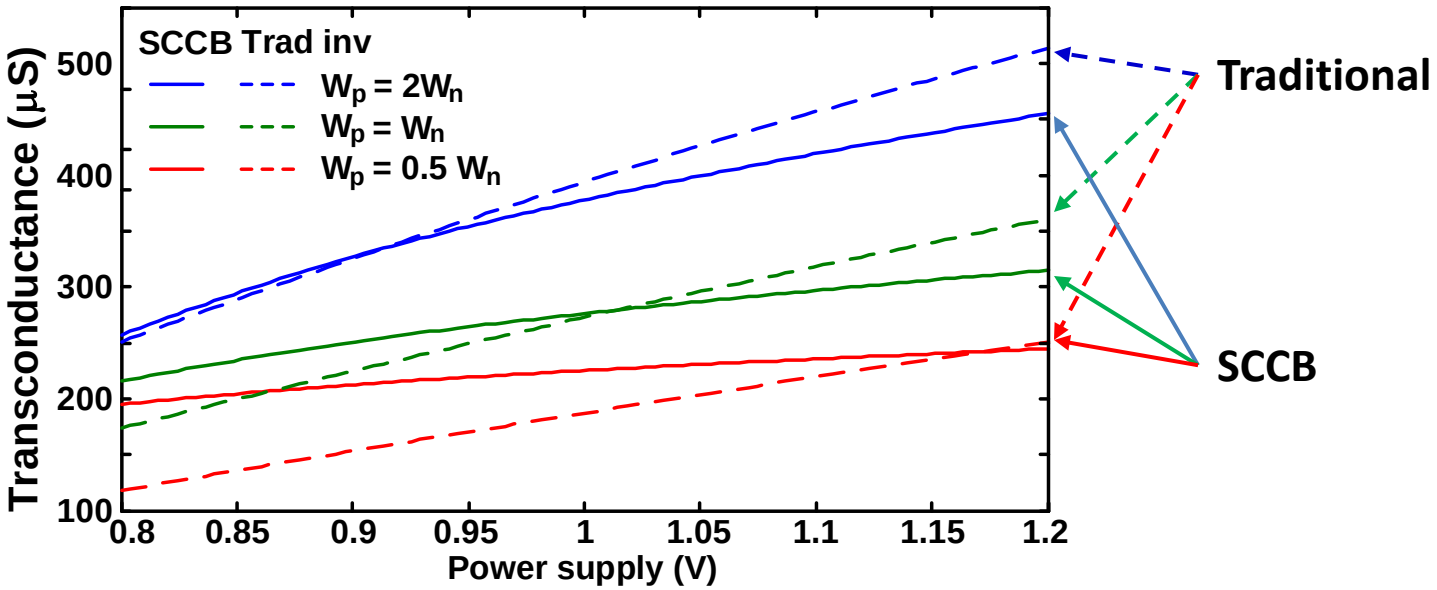


SCCB biasing



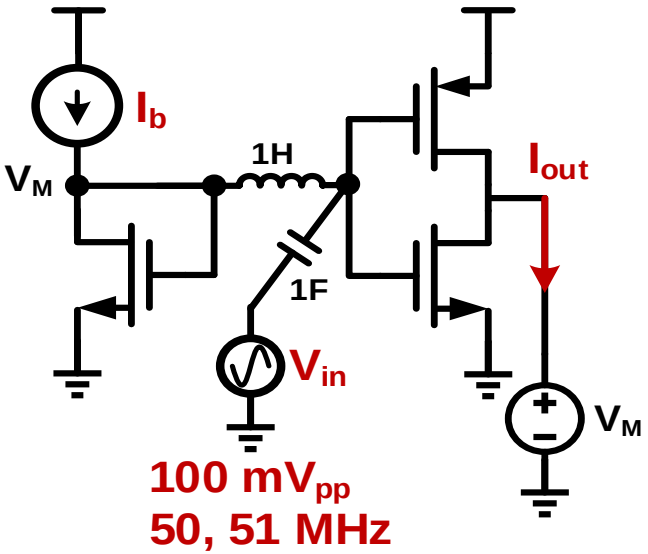
SCCB: Optimal Sizing

- **Higher PMOS size $W_p > W_n$**
  - Higher transconductance but larger variation
- **Lower PMOS size $W_p < W_n$**
  - Lower transconductance and lower variation

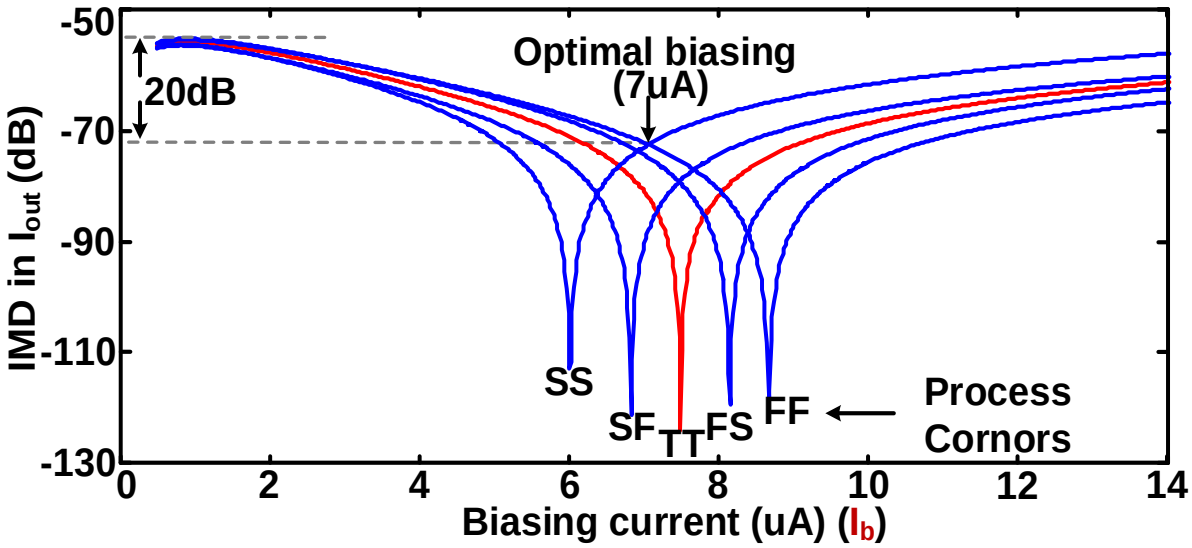


Sizing tradeoff between gm and its variation

SCCB: Linearity



Simulation setup

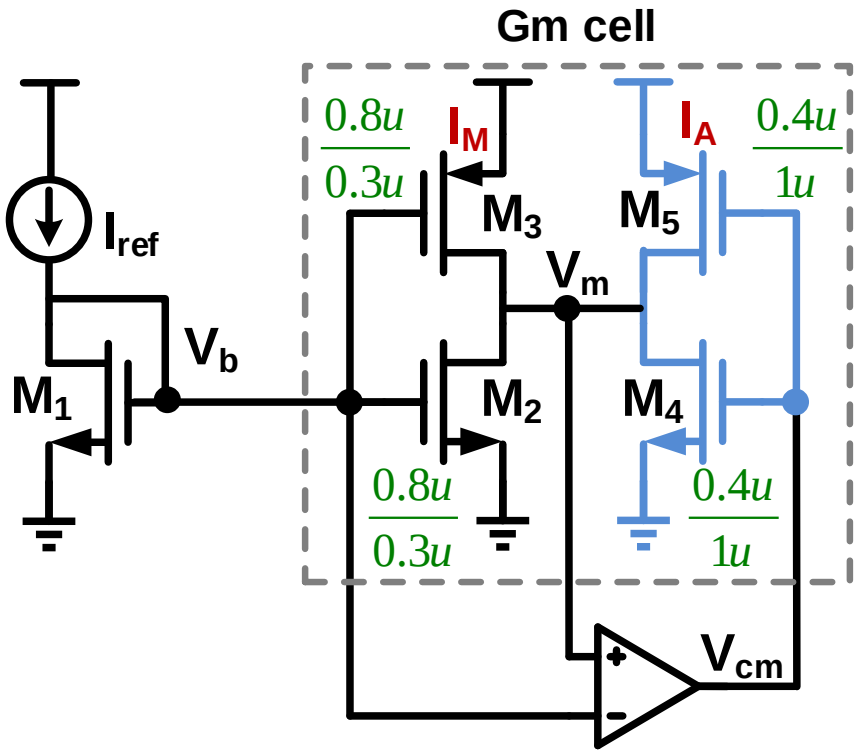


Simulation of IMD for I_{out}

- **NMOS/PMOS current can be selected**
  - To increase inherent linearity of inverter
  - Optimal biasing results in 20 dB improvement in IMD
  - NMOS and PMOS harmonic terms cancel out

SCCB: Summary

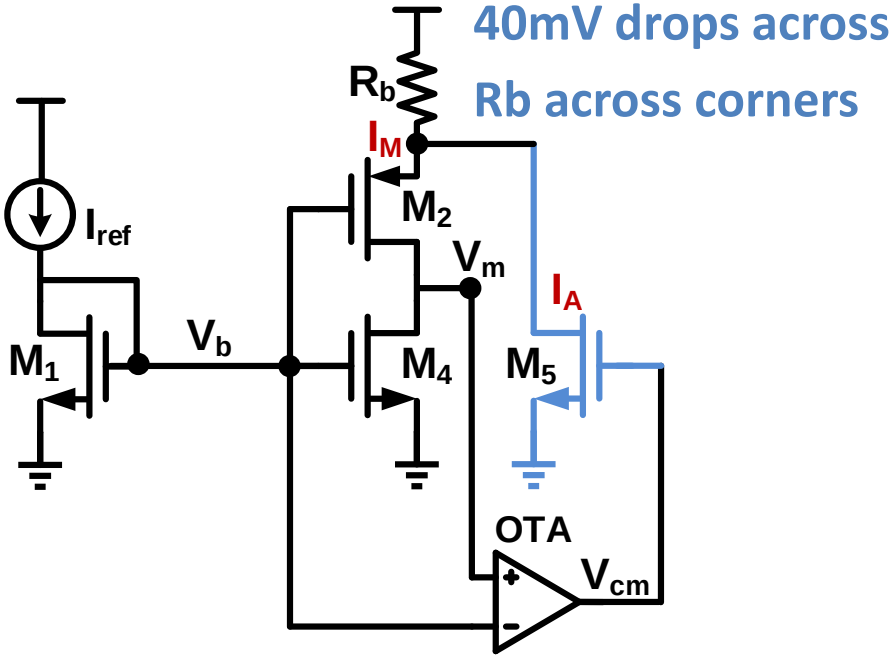
- **Variation in gm is reduced by 50%**
- **NMOS/PMOS current can be selected for best linearity**
- **Auxiliary inverter loads the main inverter**
  - Reduces the output impedance/ gain of amplifier



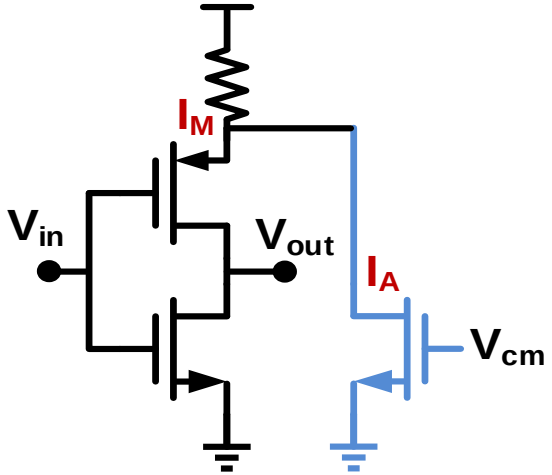
Auxiliary inverter skinnier and taller

Constant Current Biasing (CCB)

- **PMOS and NMOS current is kept constant**
- **Auxiliary transistor sets VDD for inverter**
- **Constant current → gm constant**
  - With V_T & V_{DD} variation
- **Auxiliary inverter is used with main inverter**



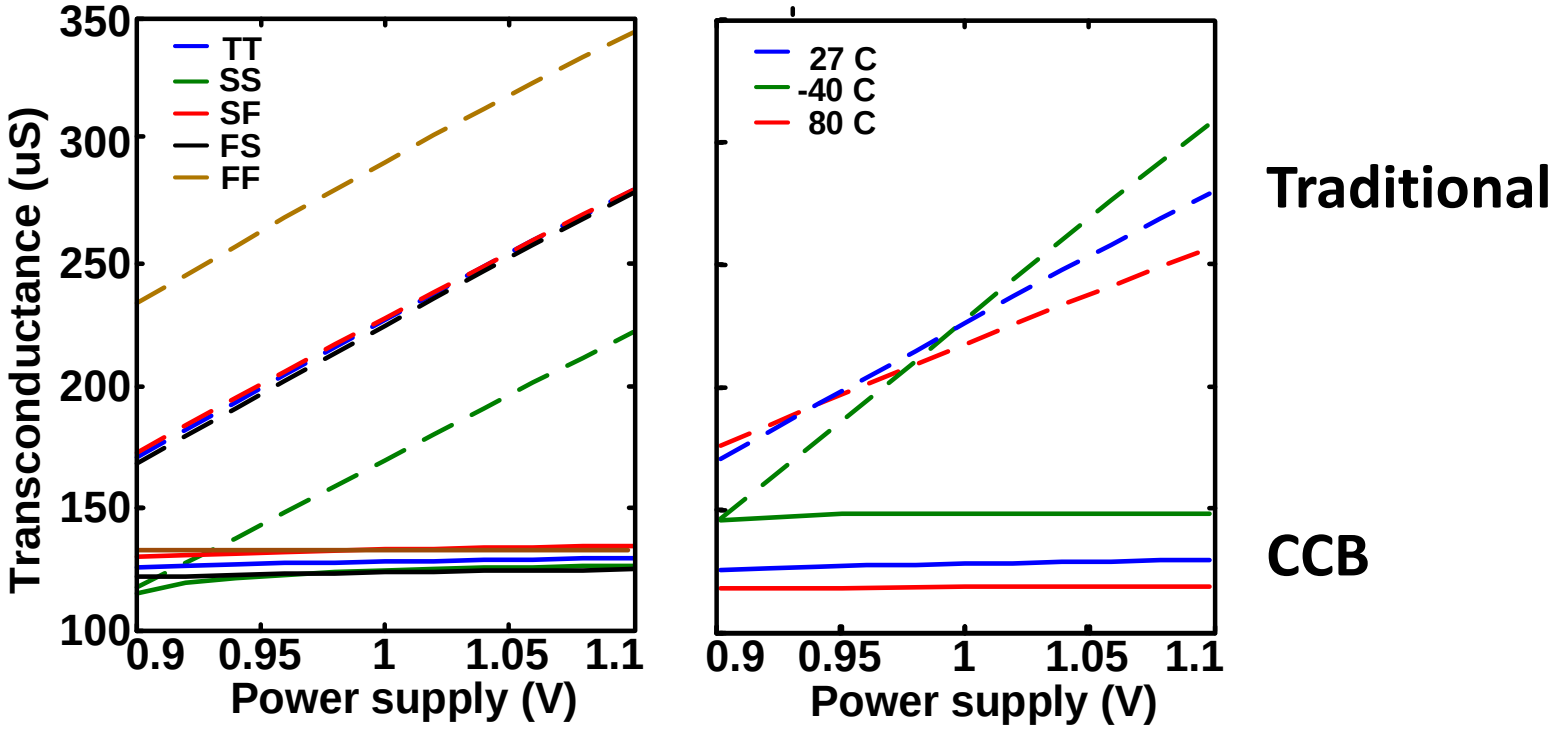
Effectively a shunt regulator



Use of CCB inverters

CCB: Simulation Results

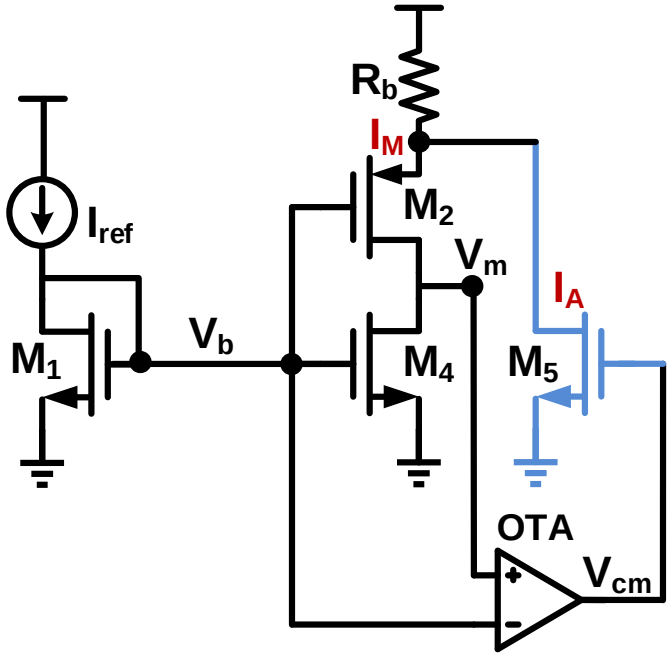
- **Variation in gm is reduced**
  - 10% across process and power supply
  - 22% across temperature



Variation of gm with traditional and constant current biasing

CCB: Summary

- **Variation in gm is further reduced**
  - 10% across process and power supply
  - 22% across temperature
- **Auxiliary inverter does not load main inverter**

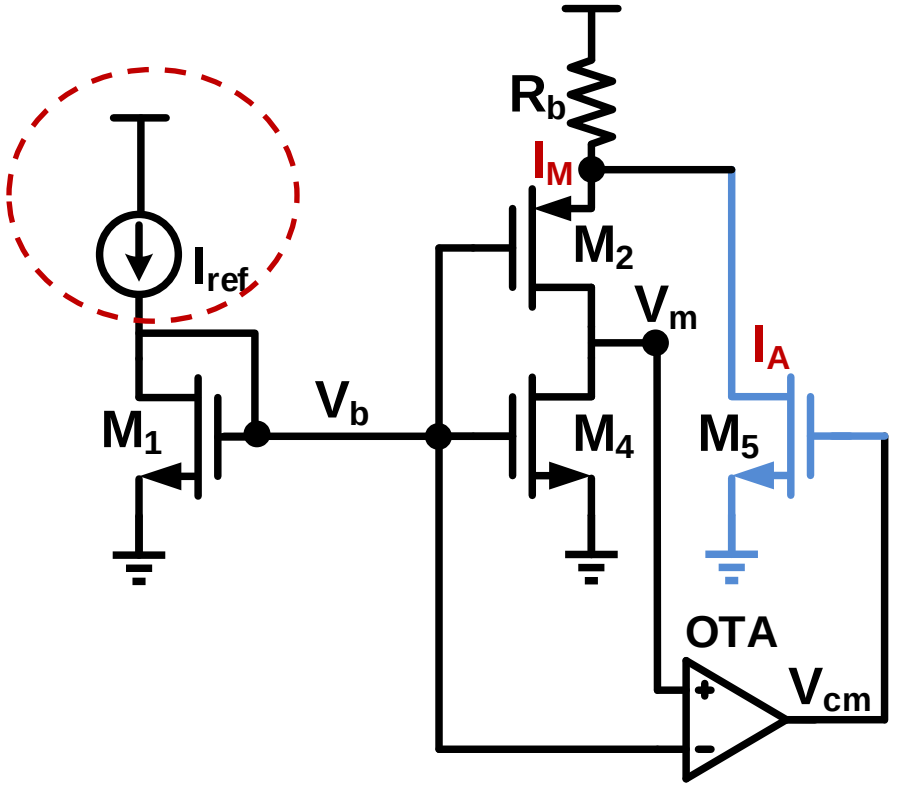


Constant gm Biasing

- **Derive I_{ref} in CCB using an external resistor**
  - To make overall gm constant

Derived to make

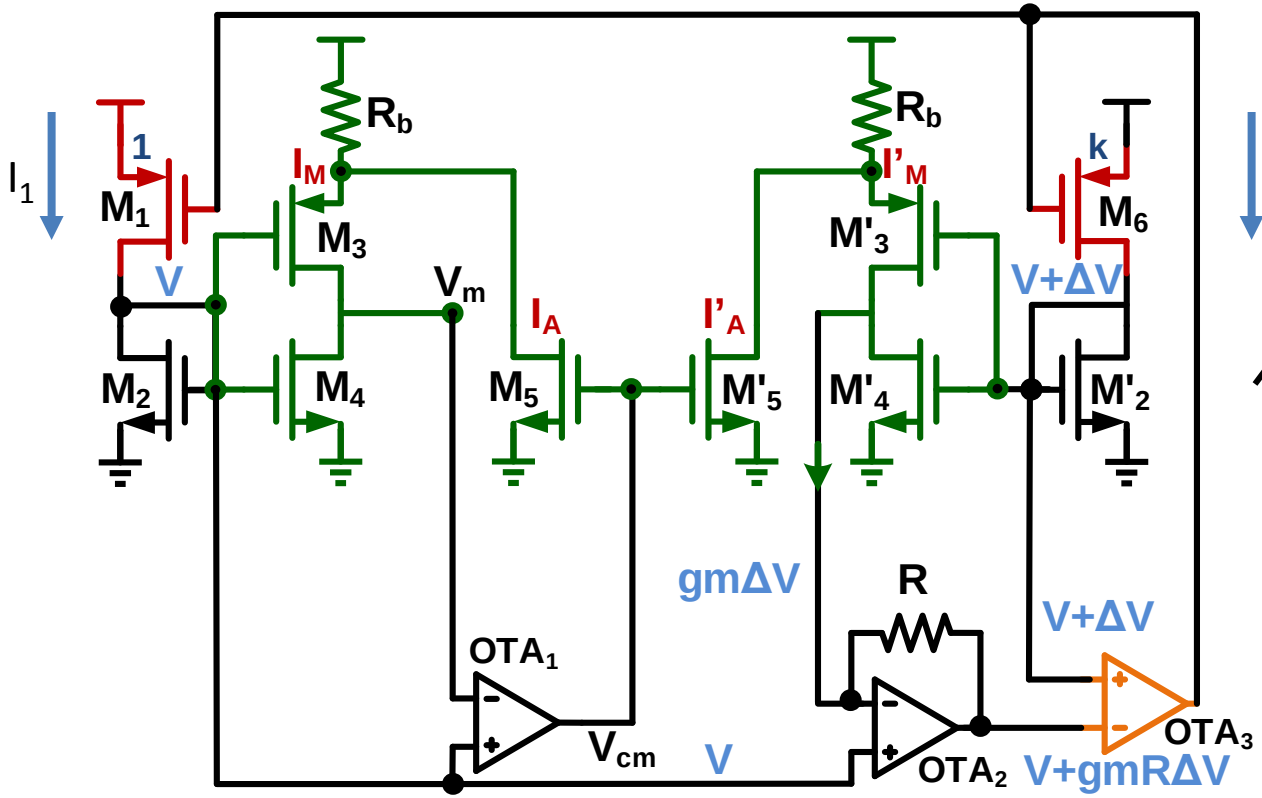
$g_{m2} + g_{m4} = 1/R$



Ref: [16] Pavan, ISCAS 2004 (OTA)

Constant gm Biasing

- Current I_1 sets Vgs_2=V, I_6 sets Vgs'_2=V+ΔV (note k)
- OTA_3 makes gmR=1

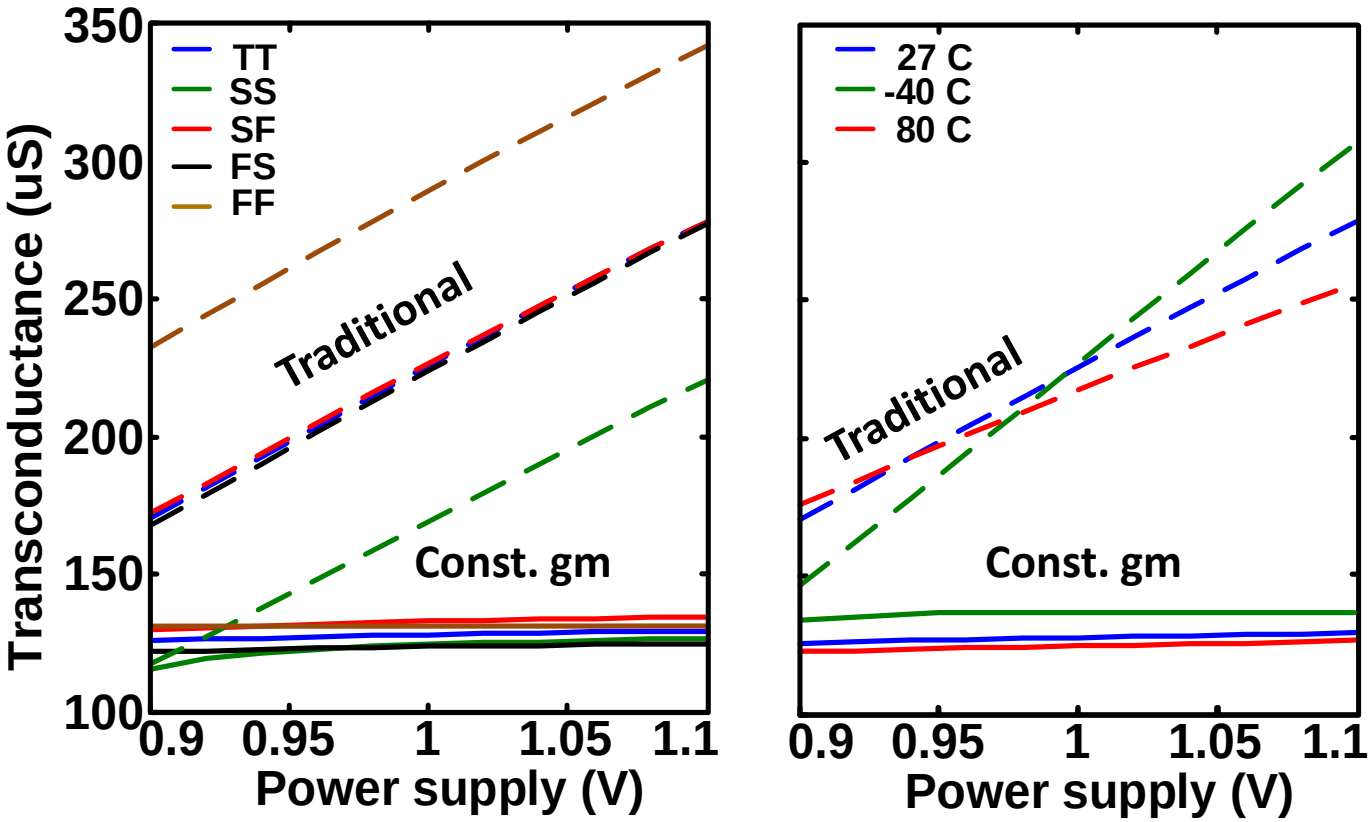


$$V + \Delta V = V + gm \cdot R \cdot \Delta V$$

$$\Delta V = gm \cdot R \cdot \Delta V$$

$$1 = gm \cdot R$$

Constant gm Biasing: Simulations



Variation of gm with traditional and constant gm biasing

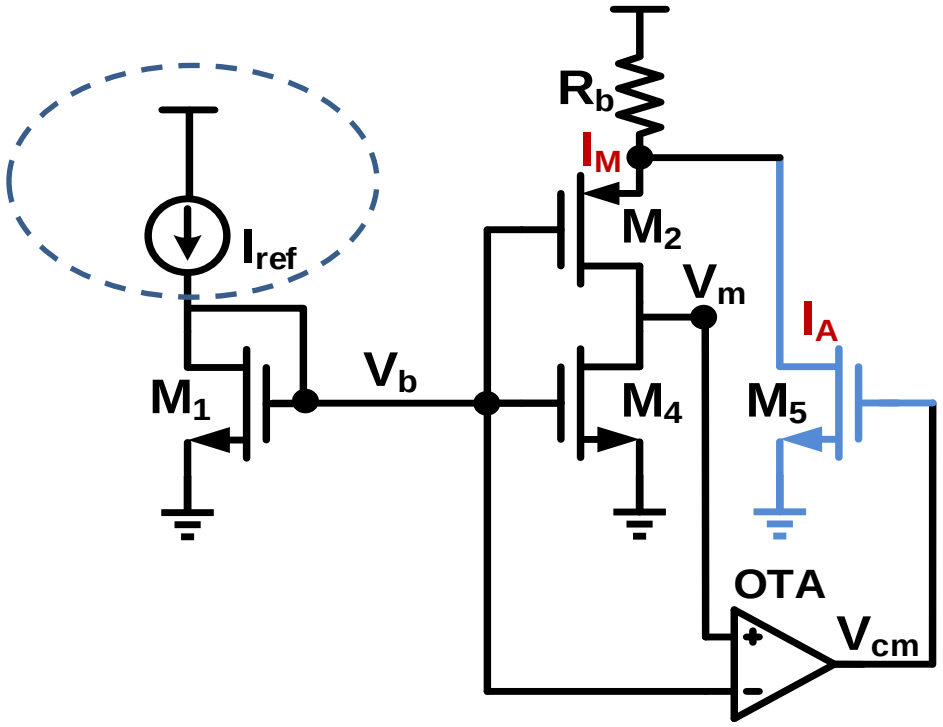
- **Overall trans conductance variation**
  - 10% across process, voltage and temperature
  - PVT problems solved for inverter based amplifiers

Constant gm Biasing: Summary

- **Reduced transconductance variation**
  - 10% across process, voltage and temperature
- **Auxiliary inverter does not load main transistor**
- **Requires a high precision external resistor**

Derived to make

$g_{m2} + g_{m4} = 1/R$



Talk Outline

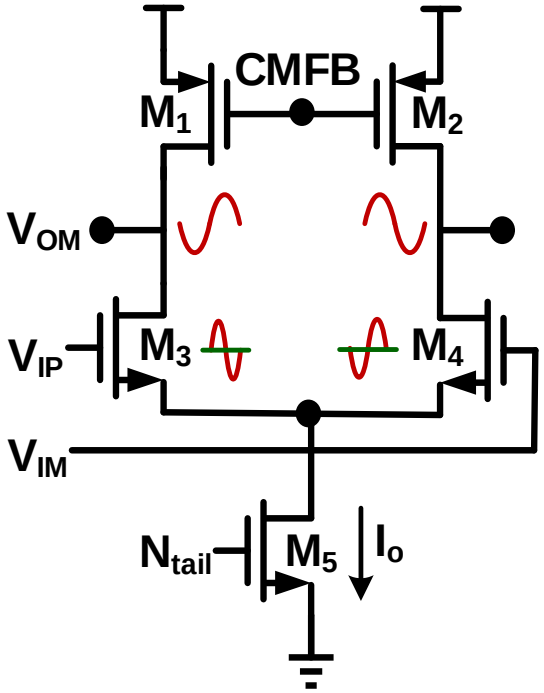
- **Motivation**
  - Technology trends
  - Inverter amplifier vs differential pairs
- **Inverter based OTA design techniques**
  - Inverter biasing techniques (3)
  - Common mode rejection ratio
  - Cascoding in inverter circuits
  - Inverter based OTA design
- **Other inverter based designs**
  - ADC driver
  - Channel select filter
- **Conclusions**

Simulations & analysis

Three prototype designs

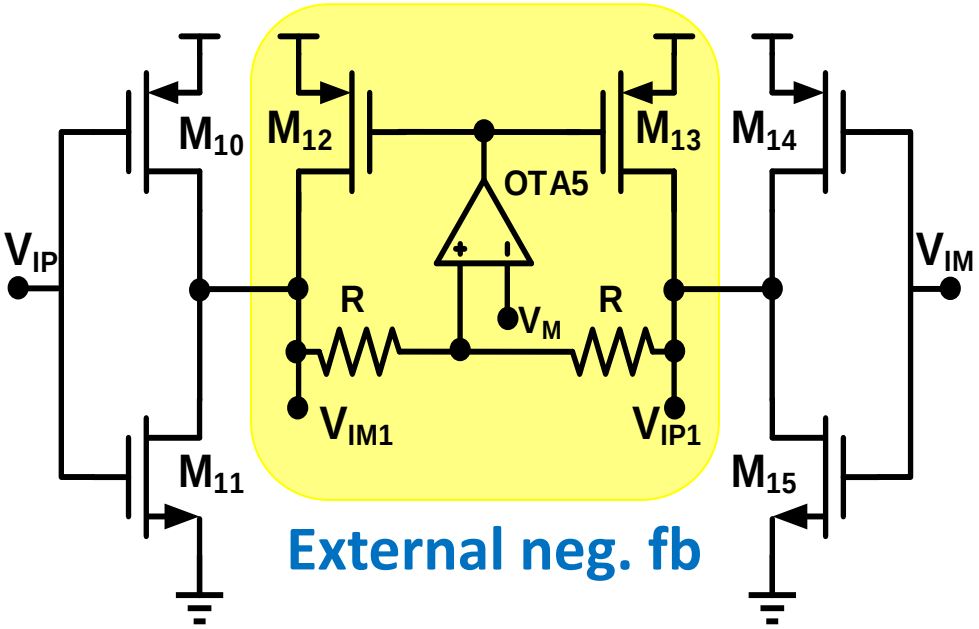
Common Mode Rejection: Diff Pair

- **Tail source M_5 provides**
  - Negative feedback for common mode signals
  - Reduces gm for common mode signals
- **CMRR depends on output impedance of M_5**



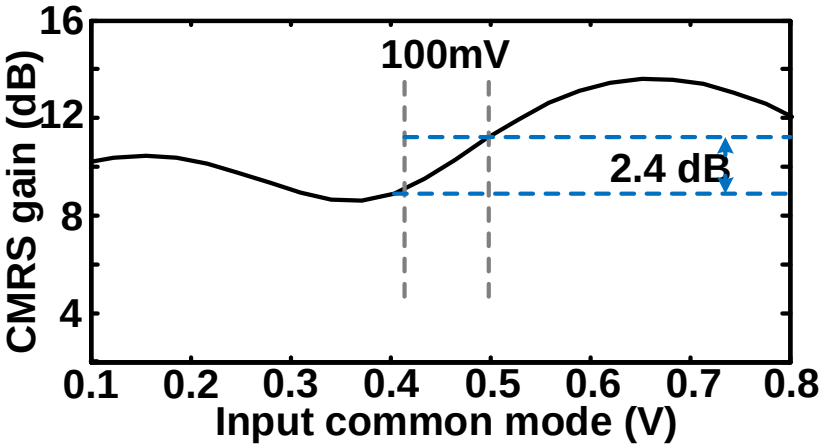
Common Mode Rejection Stage: Inverter

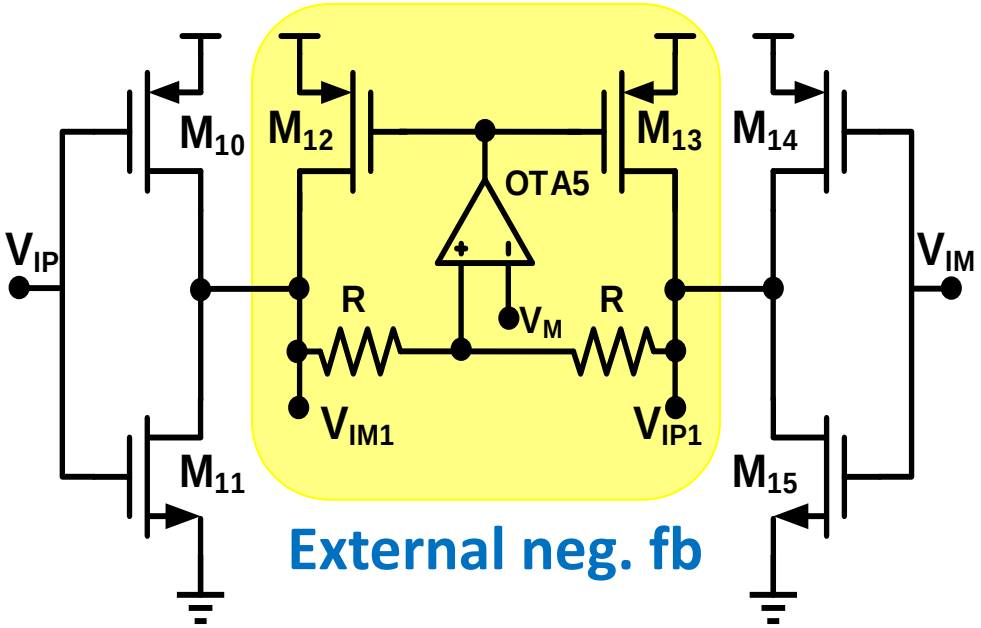
- **External negative feedback for common mode signals**
  - Reduces the output impedance for common mode signals
- **CMRR depends on external loop gain**
  - Higher than typical differential pair based designs
- **V_M is bias voltage derived from any biasing technique**



Common Mode Rejection: Inverter

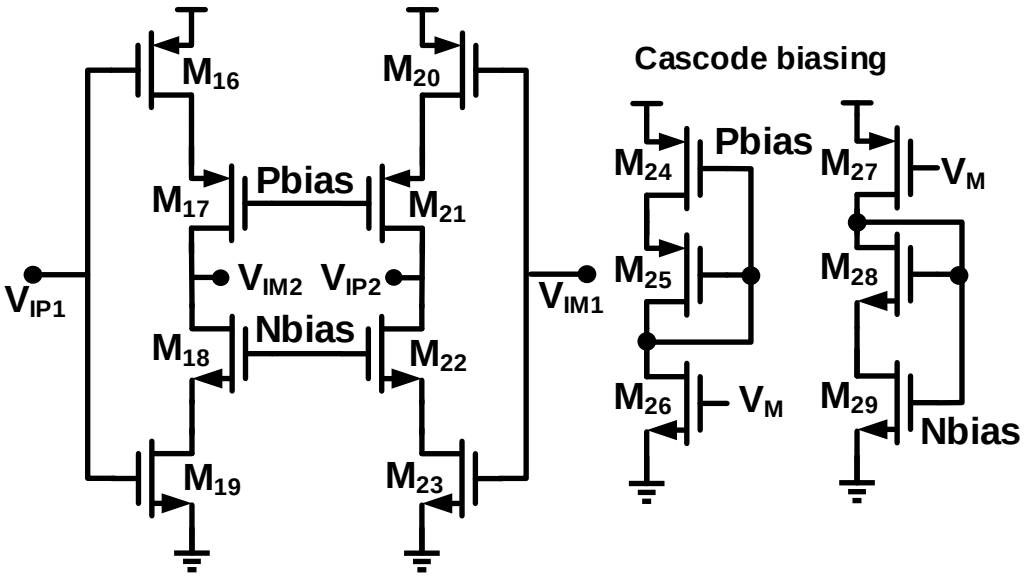
- **Resistor senses common mode voltage**
- **OTA_5 in negative feedback provides**
  - Low impedance for common mode signals ($1/(A_5 gm_{12})$)
- **$M_{10\text{-}11}$ converts both diff and common mode signals**
- **Stage gain is low**
  - High CMRR, Stability





10dB gain in this design as trade off between noise and stability

Cascoding Inverter Amplifiers: Gain stage



- **Cascode and main transistors carries same current**
- **Main transistor current depend on inp. common mode**
- **CMRS stage fixes main transistor common mode voltage**
  - This enables current reference free cascode biasing

Talk Outline

- **Motivation**
  - Technology trends
  - Inverter amplifier vs differential pairs
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  - Inverter biasing techniques (3)
  - Common mode rejection ratio
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  - Inverter based OTA design
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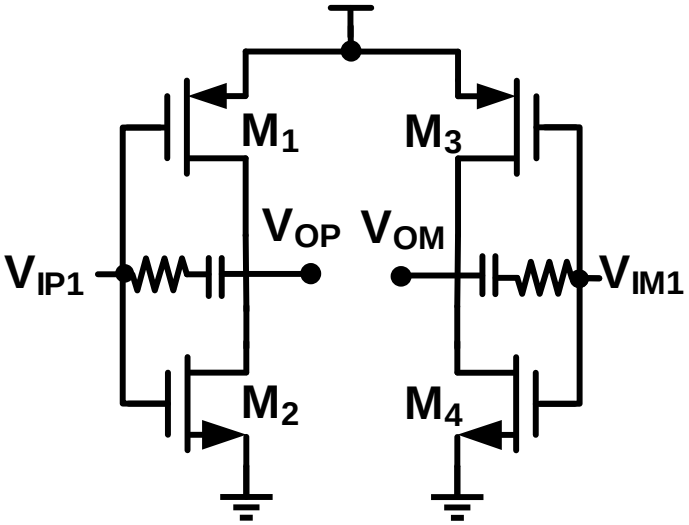
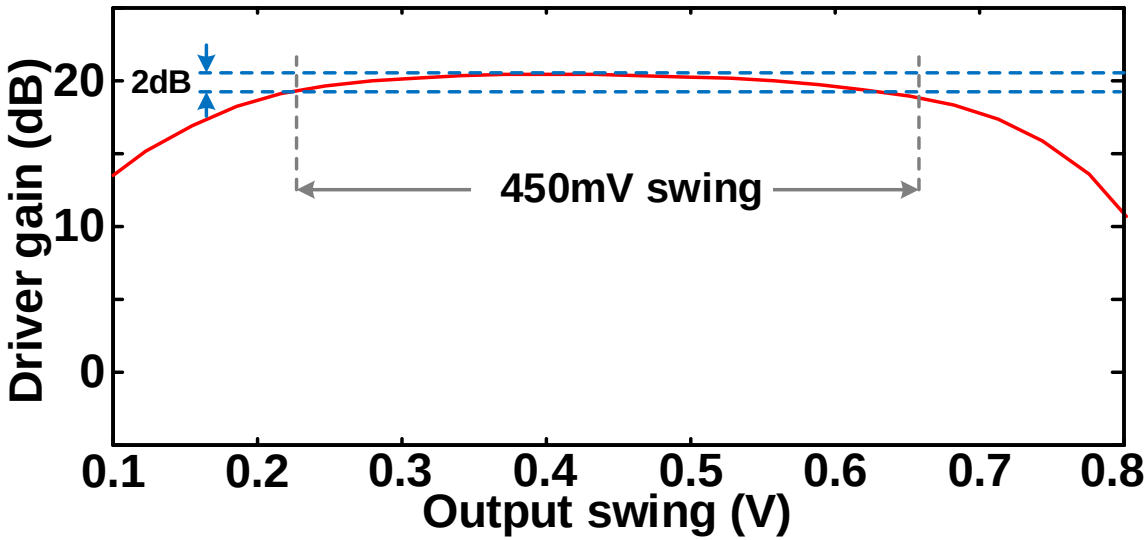
  - ADC driver
  - Channel select filter
- **Conclusions**

Simulations & analysis

Three prototype designs

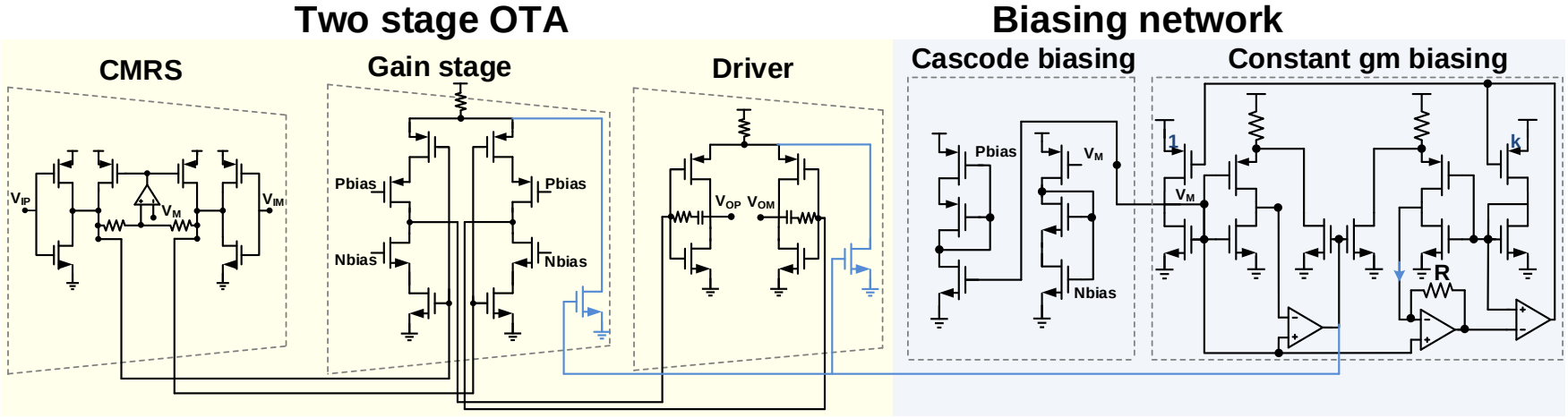
Driver Stage





- Responsible for driving load capacitance
- Minimize gain variation with swing
- All inverter based design
- Vdd=0.9V

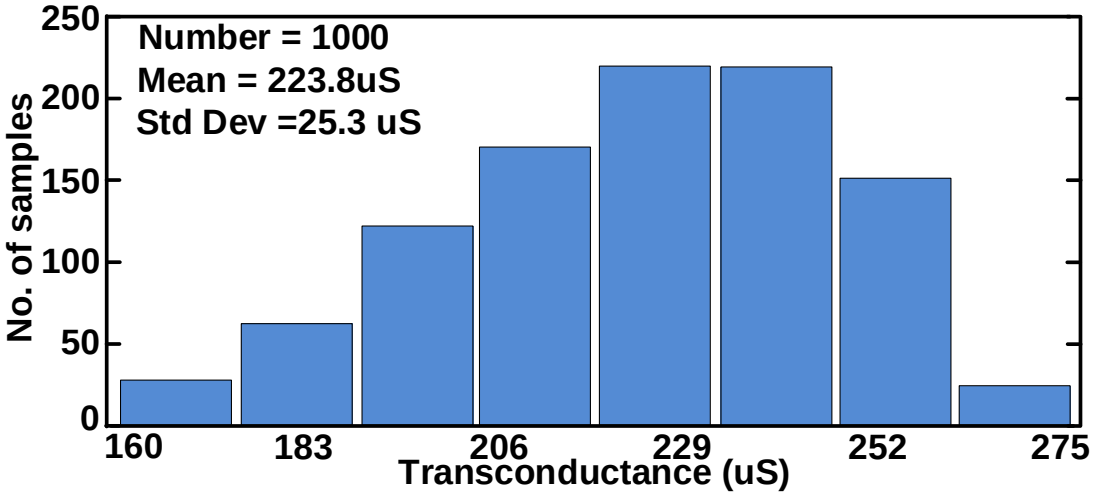
Constant Gm Biased Inverter OTA

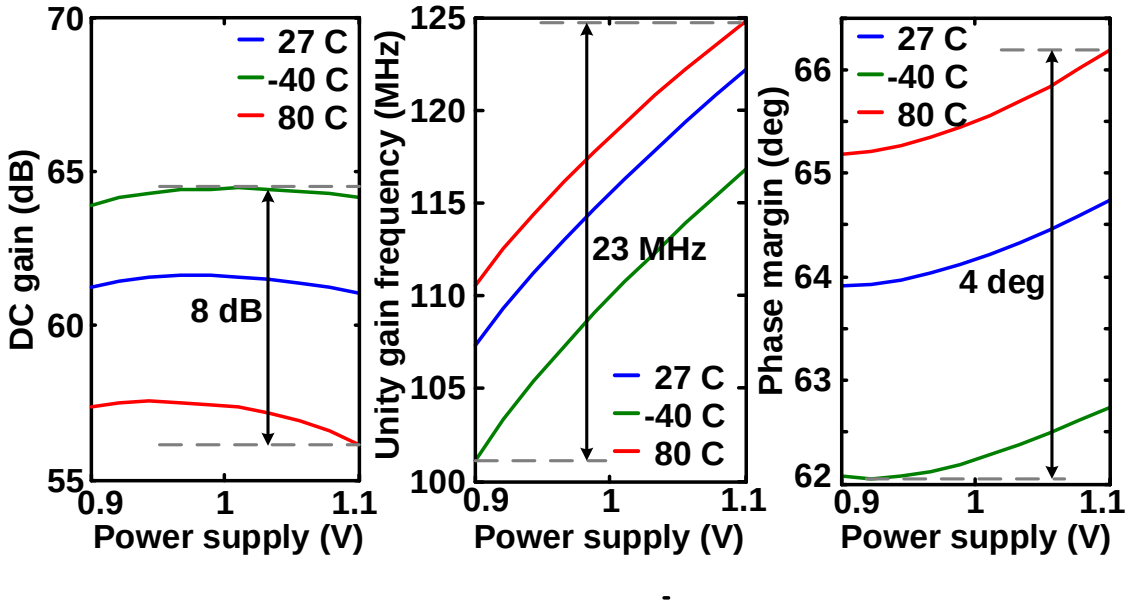


- **CMRS stage**
  - Rejects common mode variation
  - Fixes bias voltage for gain stage and cascade transistors
- **Gain stage**
  - Responsible for gain
- **Driver stage**
  - Responsible for driving the load
- **Constant gm biasing**
  - Biases all the inverters at constant transconductance

Constant Gm Biased Inverter OTA: Simulation

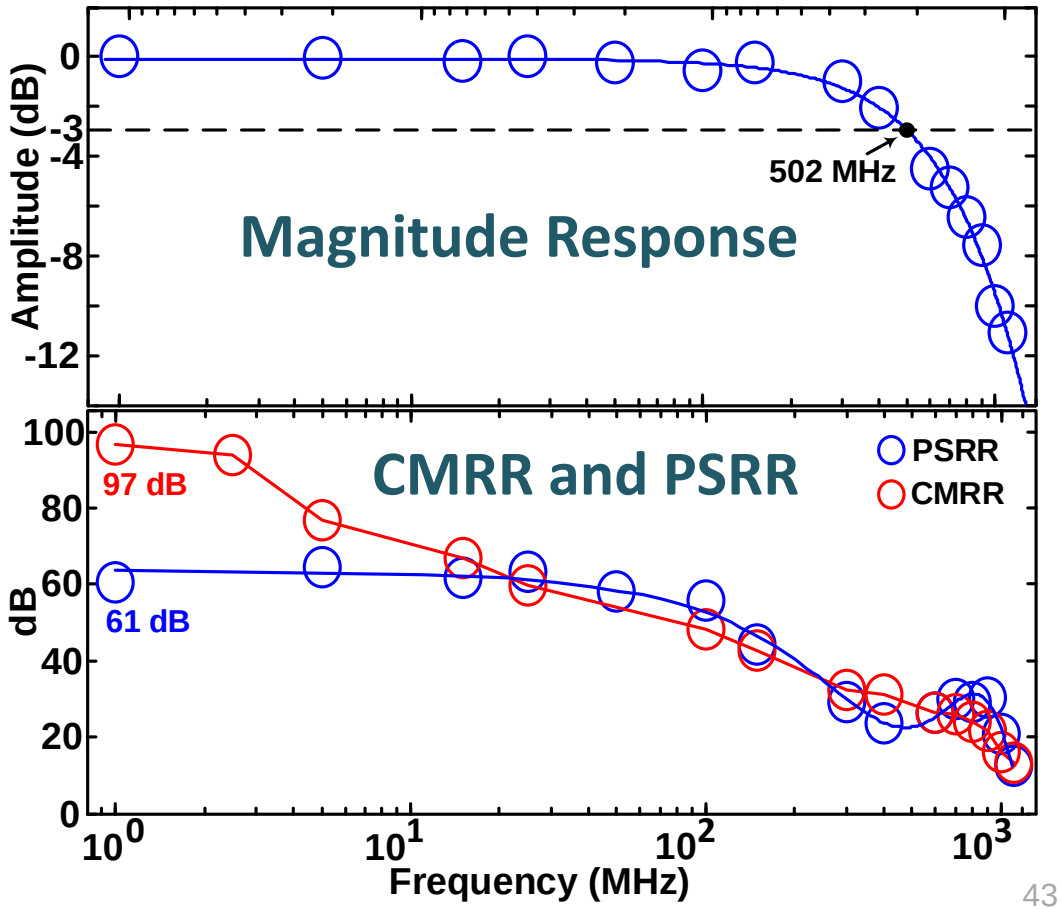
- **DC gain**
  - Varies by 8dB
- **UGB**
  - Varies by 23MHz
- **Phase margin**
  - Varies by 4 deg





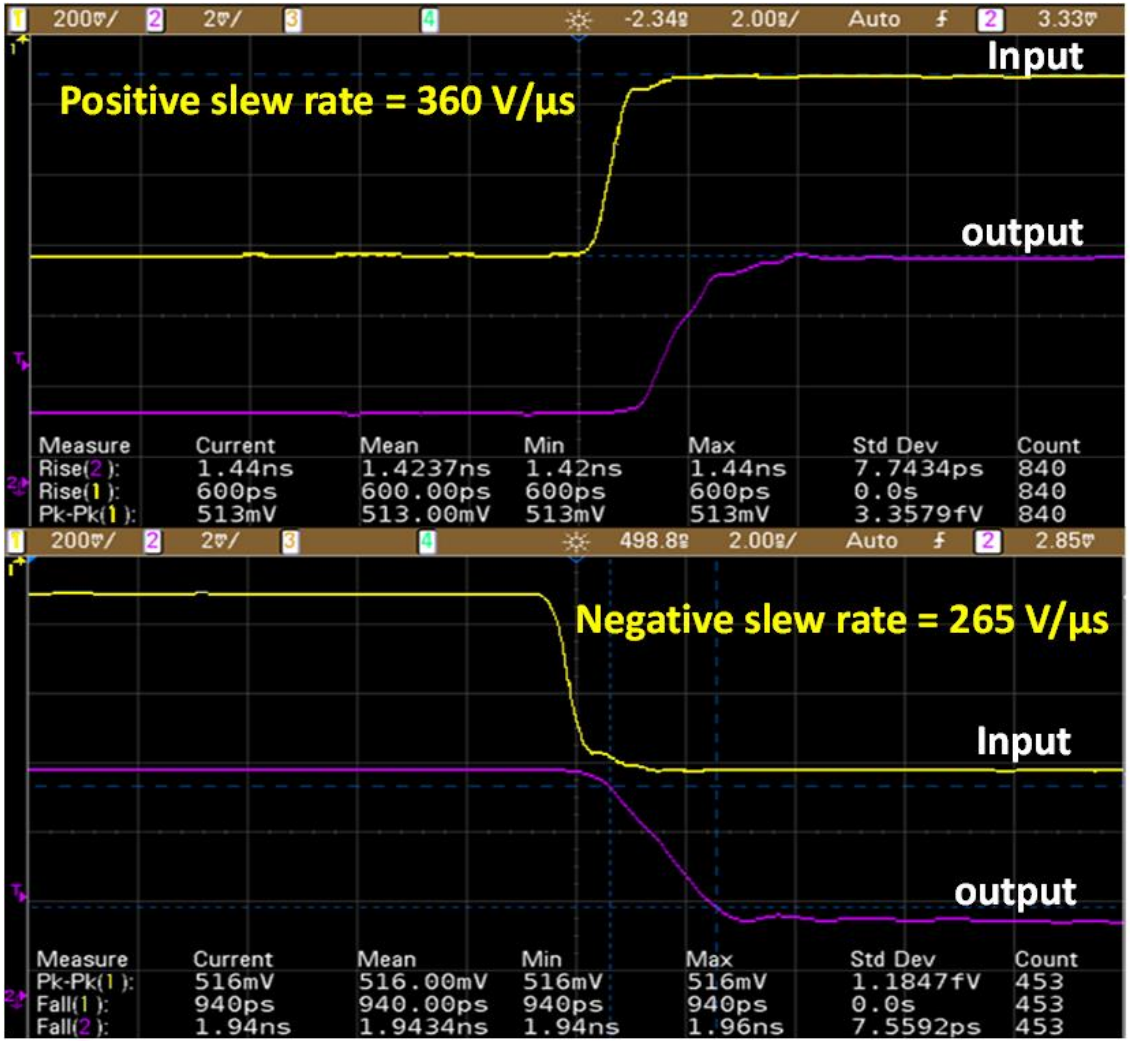
Inverter Based OTA: Measurement Results

- **Inverter based OTA fabricated in TSMC 40nm CMOS**
  - Biased using metastable biasing (traditional technique)
  - To demonstrate cascading and CMRR
  - Power supply 0.9V
  - UGB 1GHz
  - CMRR 97dB
  - PSRR 61dB



Inverter Based OTA: Measurements (II)

- **Class AB operation allows for high slew rate**



Cload=2pF
PQ=1.1mW
Vdd=0.9V

OTA Measurements: Design Summary

	[1]	[2]	[3]	[4]	This work
Tech (nm)	180	350	180	180	**40**
Supply (V)	0.5	3.3	1.5	1.8	**0.9**
Power (mW)	0.08	10.5	9.5	5.0	**1.1**
Noise (nV/$\sqrt{Hz}$)	70	149	23	-	**12**
Swing ($V_{pp\text{-}diff}$)	0.7	1.3	0.9	1.6	**0.9**
THD (dB)	-57	-69	-60	-	**-91**
GBW (MHz)	10	~50	~60	150	**1000**

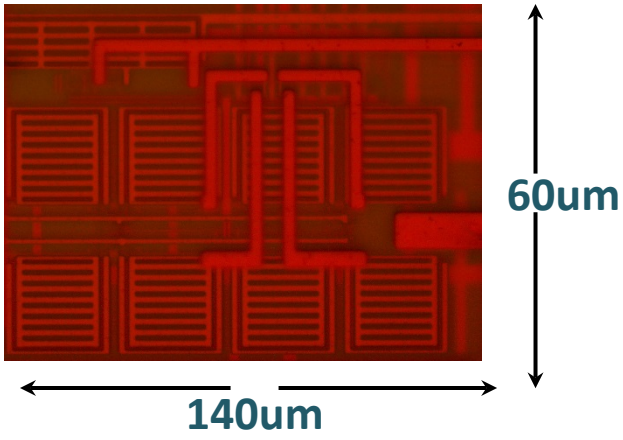
TSMC 40nm GP
Nominal Vdd 0.9V

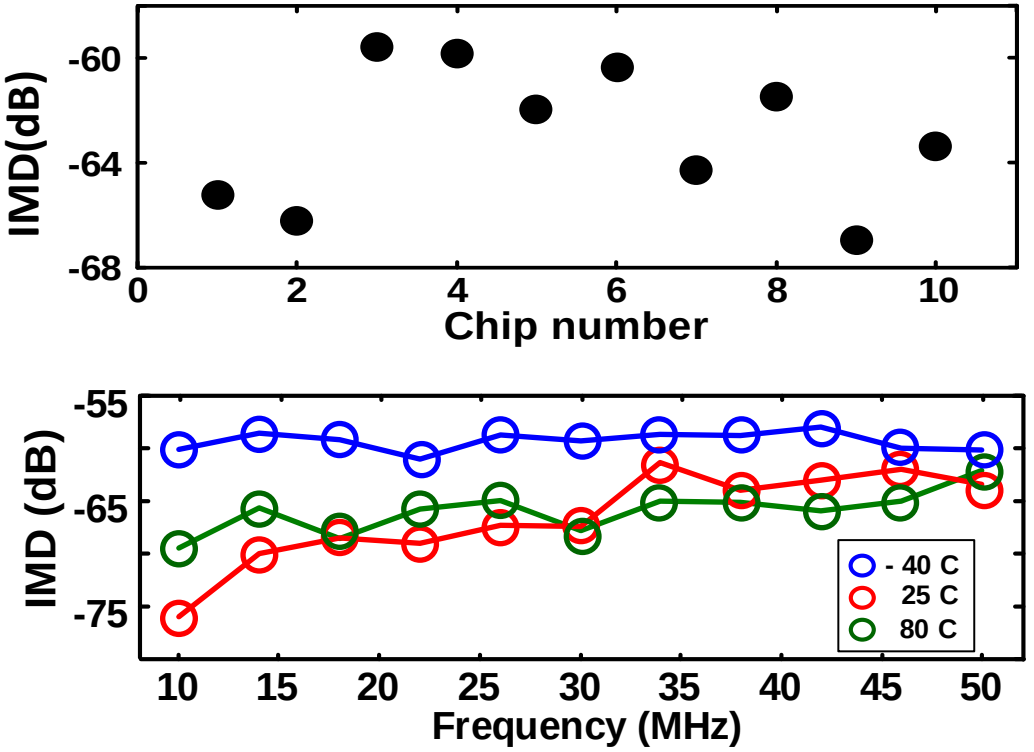
Lowest V_{dd} with all transistors in strong inversion
Highest THD for maximum swing

[1] JSSC 2005
[2] CICC 2003
[3] ASSCC 2006
[4] VLSI 2007

Other Inverter Based Circuits: Measurements

- **ADC driver**
  - Inverter based amplifier with sample and hold
  - SCCB biased for PVT tolerance and linearity

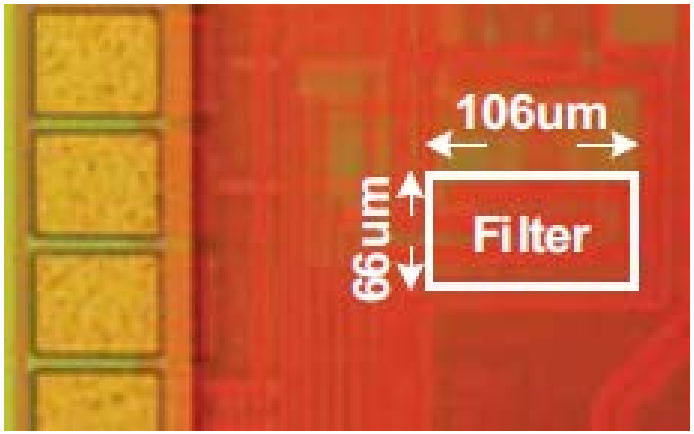


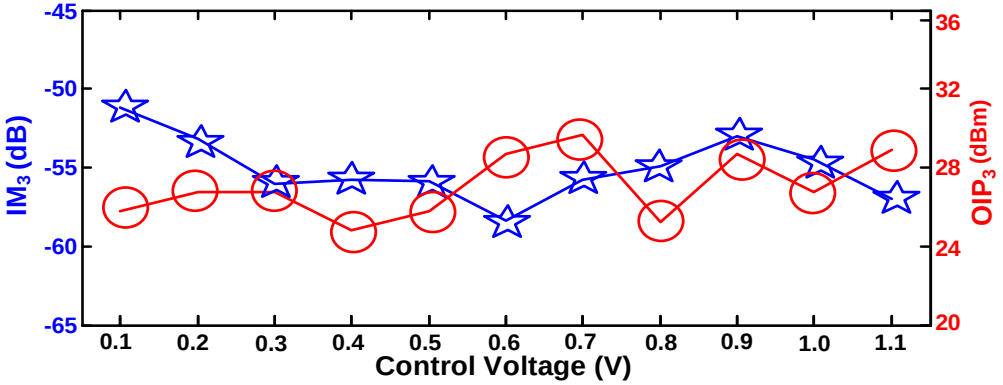


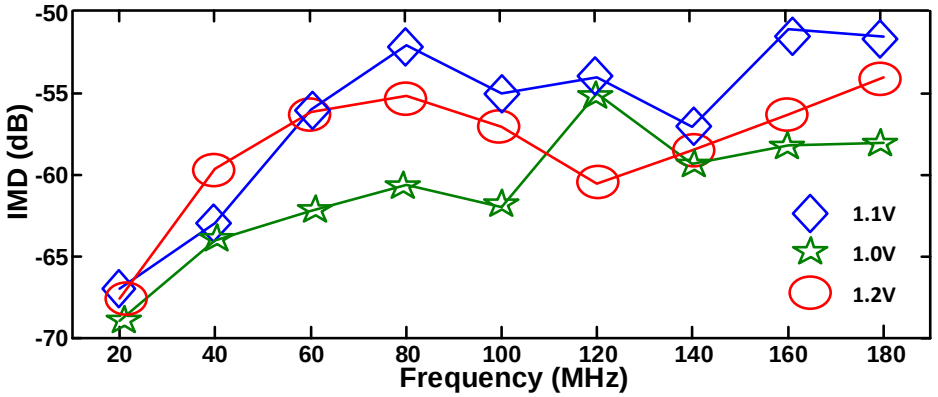
Ref: [15] Palani & Harjani, CICC 2014

Other Inverter Based Circuits: Measurements

- **Tunable channel select filter**
  - All MOSCAP and inverter based design
  - SCCB biased for PVT tolerance and linearity







Ref: Palani & Harjani, CICC 2015

Conclusions

- **Inverter based designs**
  - Inevitable at lower technologies and supply voltages
  - Are highly linear and have lower noise
  - Have poor CMRR, PSRR and PVT tolerance
- **Design techniques introduced**
  - 3 Biasing techniques → SCCB, CCB, constant gm
  - Cascode biasing for inverter amplifiers
  - Common mode rejection in inverter amplifiers
- **Circuits developed as proof of concept**
  - Simulation results of constant gm biased OTA
  - Measurement results for inverter based OTA
  - Measurement results for ADC driver & channel select filter

Acknowledgement

- Research supported by the DARPA CLASIC program

- Authors thank Dr. Sanjay Raman, Dr. Bill Chappell and Dr. Troy Olson all of DARPA MTO

Thank You

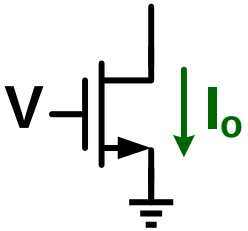
Backup slides
Non Linearity Cancellation

Nonlinearity vs Noise Tradeoff

$$I_o = f(\mathrm{V} - \mathrm{V}_T) \rightarrow \quad I_o + \Delta I = f(\mathrm{V} + \Delta V - \mathrm{V}_T)$$

$$\Delta V < \mathrm{V} - \mathrm{V}_T \quad \rightarrow \quad \Delta I = \Delta V f'(\mathrm{V} - \mathrm{V}_T)$$

(Taylor series approximation)



- **Higher overdrive voltage (V-V_T) → higher linearity**
- **Input referred noise →** $v_n^2 = \dfrac{2kT}{I_o}(\mathrm{V} - \mathrm{V}_T)$
  - Higher overdrive voltage → higher noise
- **Any linearization attempts increases noise**
- **Nonlinear cancellation breaks this trade-off**

Nonlinearity cancellation is exploited in SCCB

Nonlinearity Cancellation

- **If inverse function exists, then**

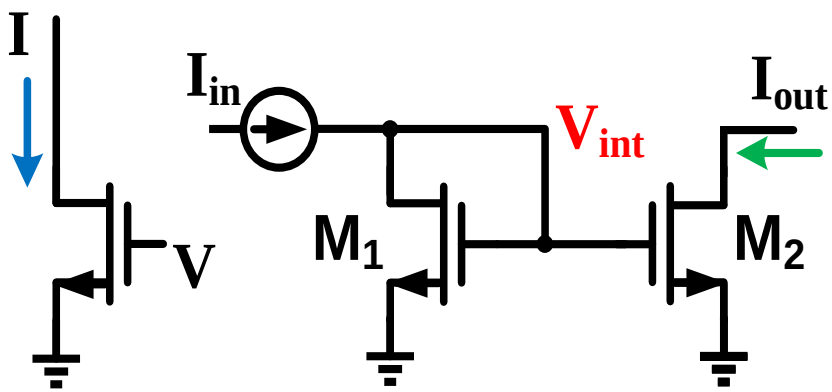
$$ff^{-1} = 1$$

- **In analog we always go from V →I ,I→V to get amplification, integration or differentiation**

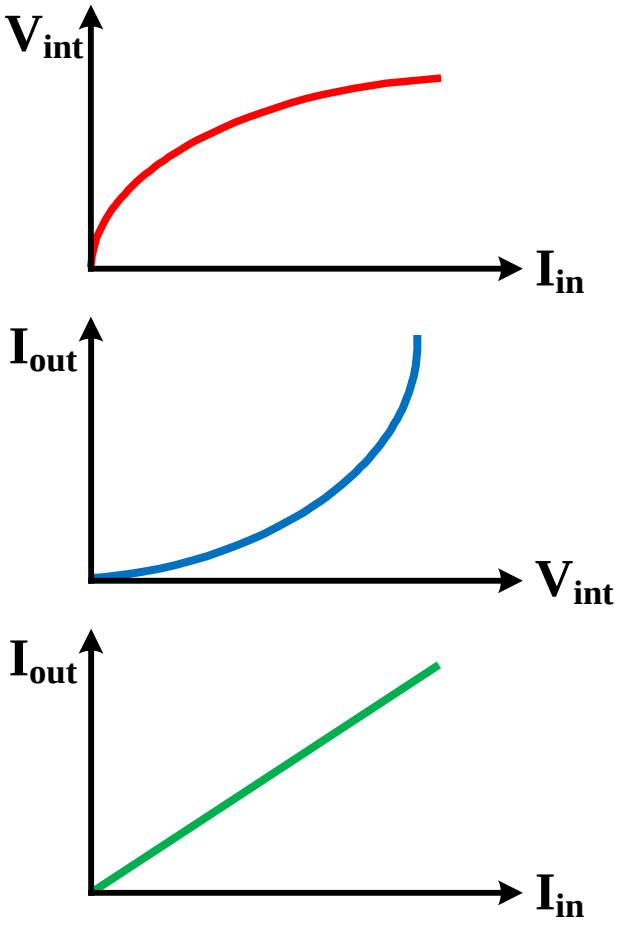
V→I	I→V	Function
Resistor/transistor	Resistor/transistor	Amplification
Resistor/transistor	Capacitor	Integration
Capacitor	Resistor/transistor	Differentiation

If V→I and I→V are performed by function and its inverse, any nonlinearity in function is cancelled

Nonlinearity Cancellation: Current Mirror

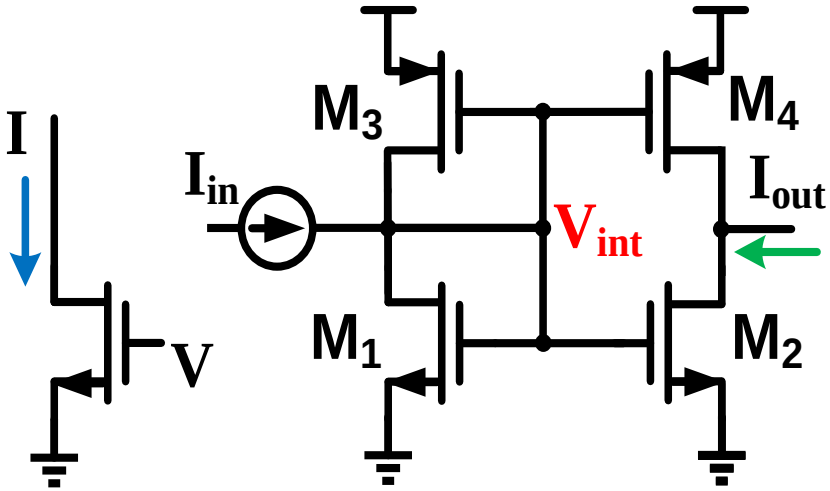


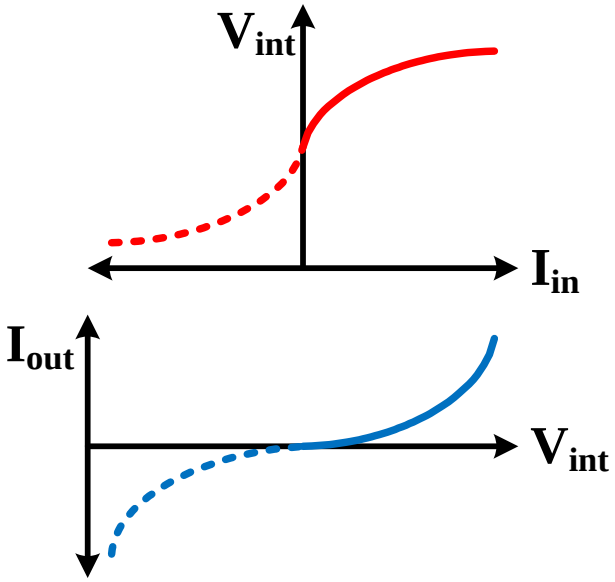
$$I \propto kV^2$$



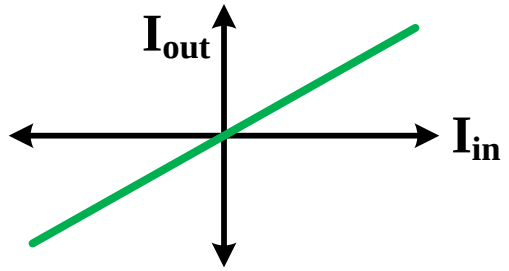
- M_1, M_2 are non-linear
- However, I_{out} is linear

Nonlinearity Cancellation: Current Mirror (II)





$$I \propto kV^2$$

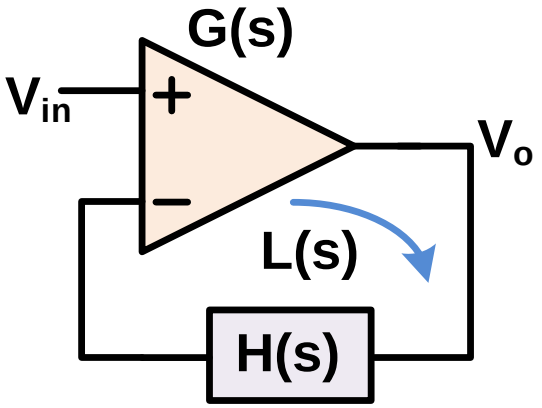


- M_3, M_4 → added for full swing
- Class-AB output

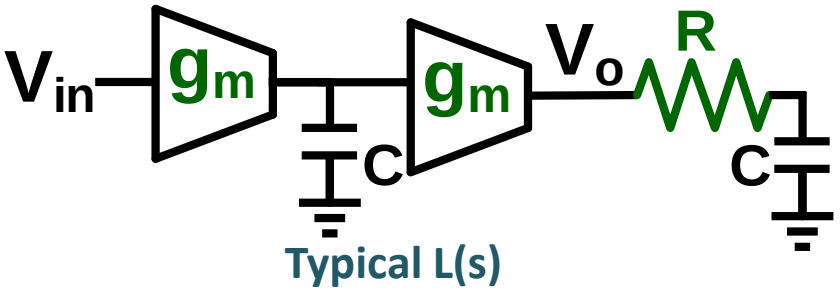
Exploited in design of ADC driver, anti alias filter

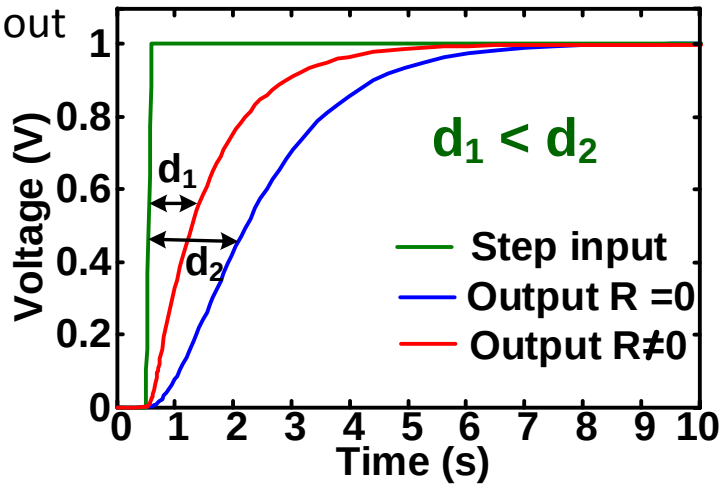
Self Compensation

- **Excess loop delay → instability**
- **Compensation**
  - Reduce the delay
  - Provide a fast path



- **Resistor converts current to voltage at high freq**
  - Reduce the delay between V_{in} and V_{out}





Exploited in ADC driver, anti-alias, channel select filter

Inverter Amplifier Transfer Characteristics

- **Vdd = 1.0, Vin = 0…1.0**