A Fully Synthesized 77dB SFDR SRMC Filter Using Digital Standard Cells

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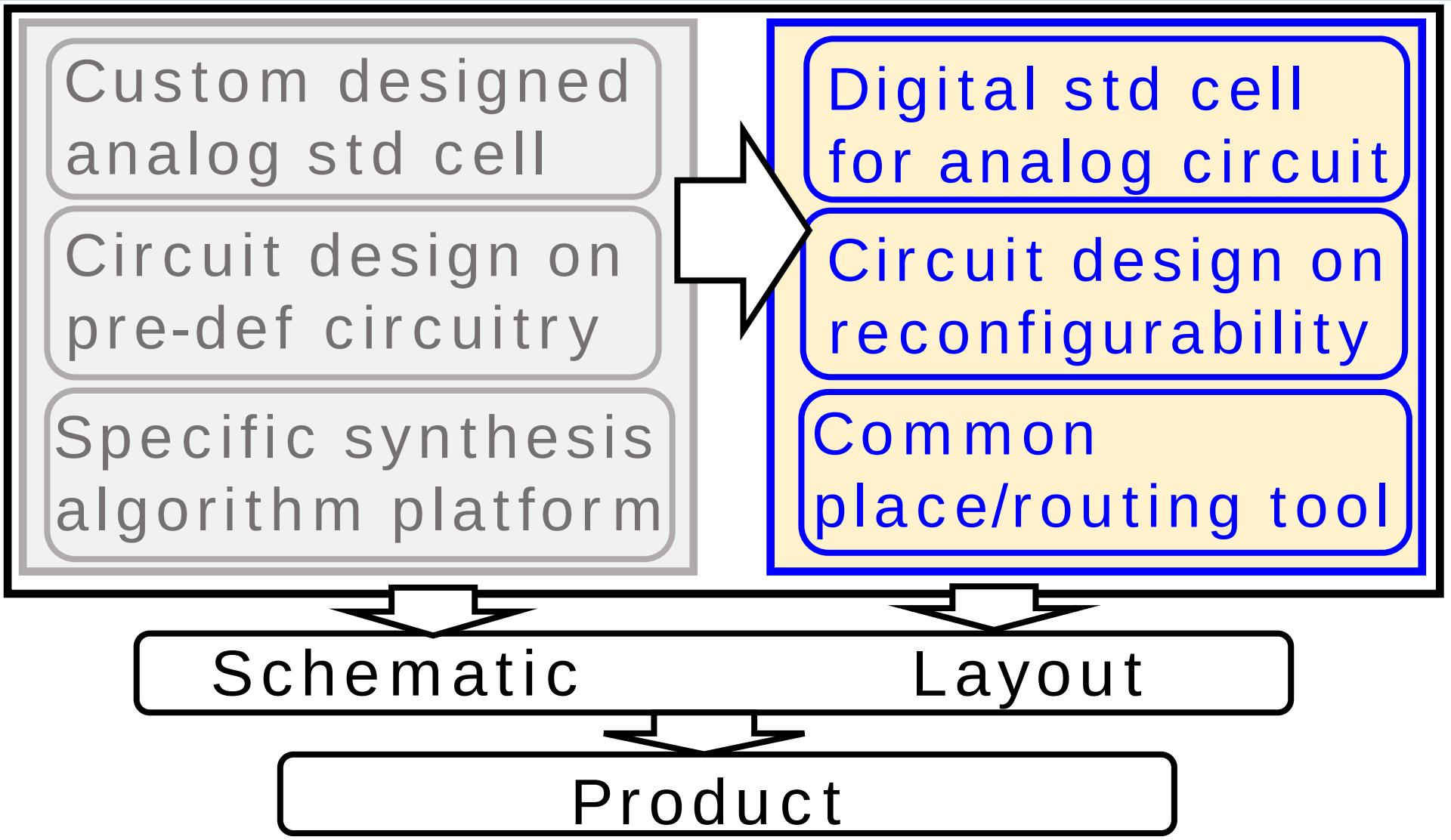
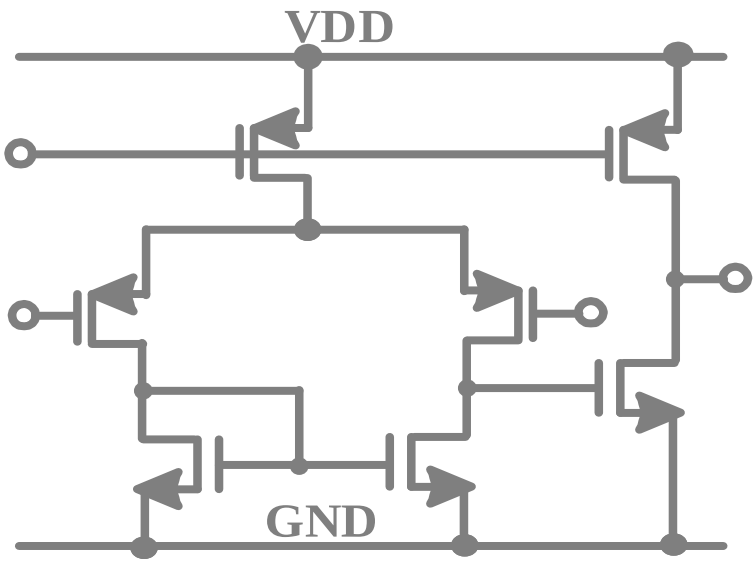
Outline

- Motivation
- Synthesizable OPAMP
- Synthesizable RC matched CLK
- Synthesizable SRMC filter
- Measurement results
- Acknowledgement

Motivation

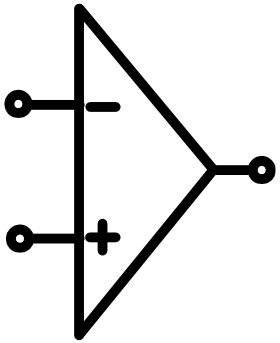

Custom designed analog std cell
Circuit design on pre-def circuitry
Specific synthesis algorithm platform
Digital std cell for analog circuit
Circuit design on reconfigurability
Common place/routing tool
Schematic
Layout
Product

Motivation



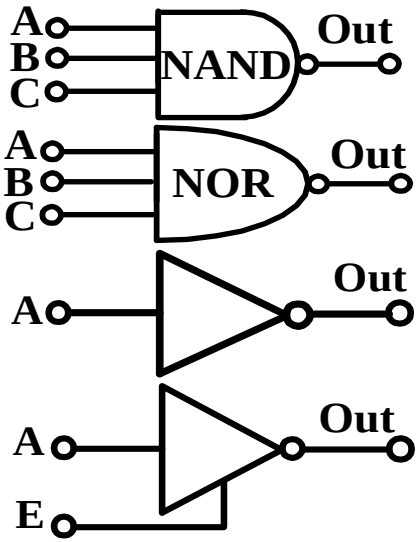
Analog std cell

- **Not available**
- **Pre-defined topology**
- **Process dependent**
- **Custom-design tool**



VS

Verilog Code



Digital std cell

- **Available**
- **Portable**
- **Synthesizable**
- **Programmable**

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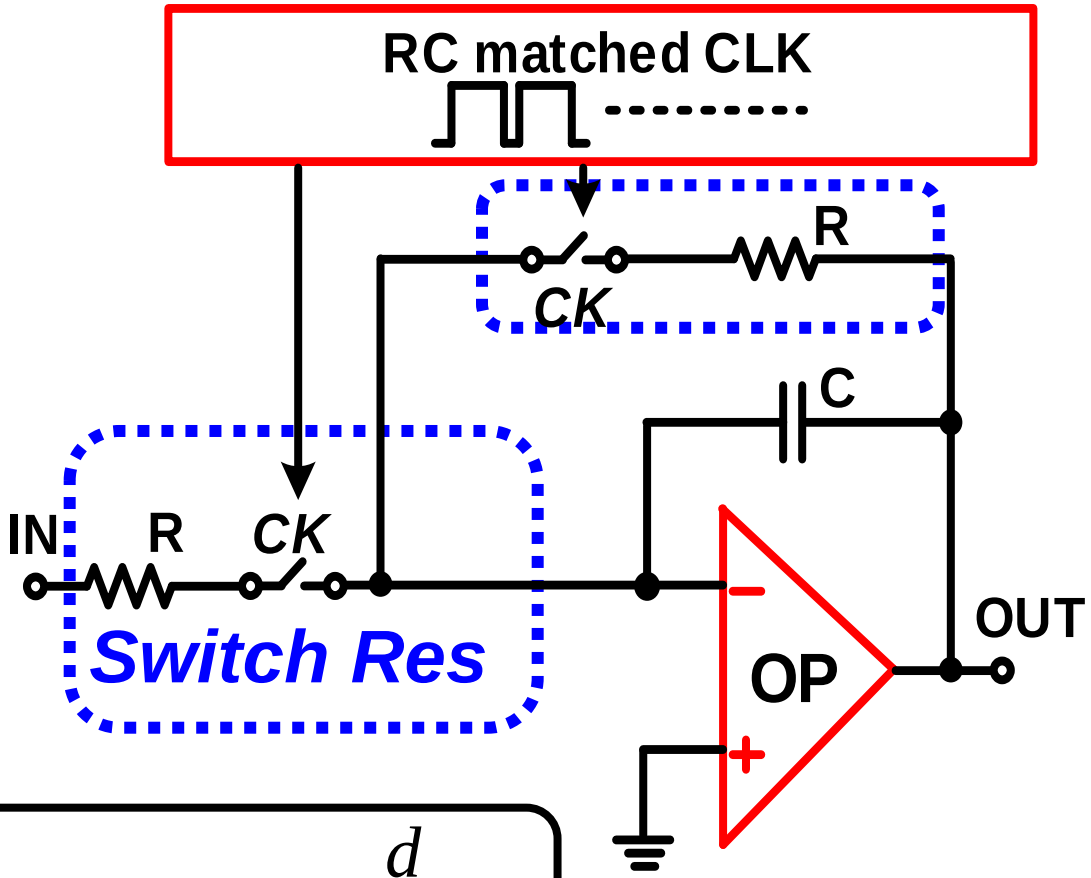
Example 1st SRMC Filter

Analog heavy circuitry

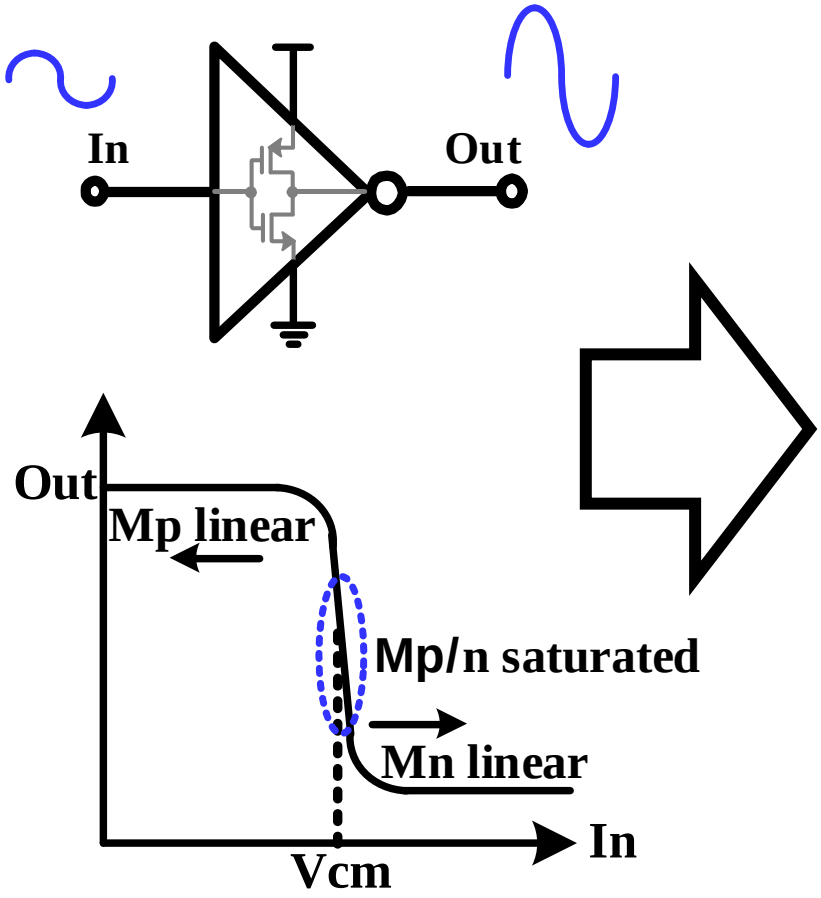


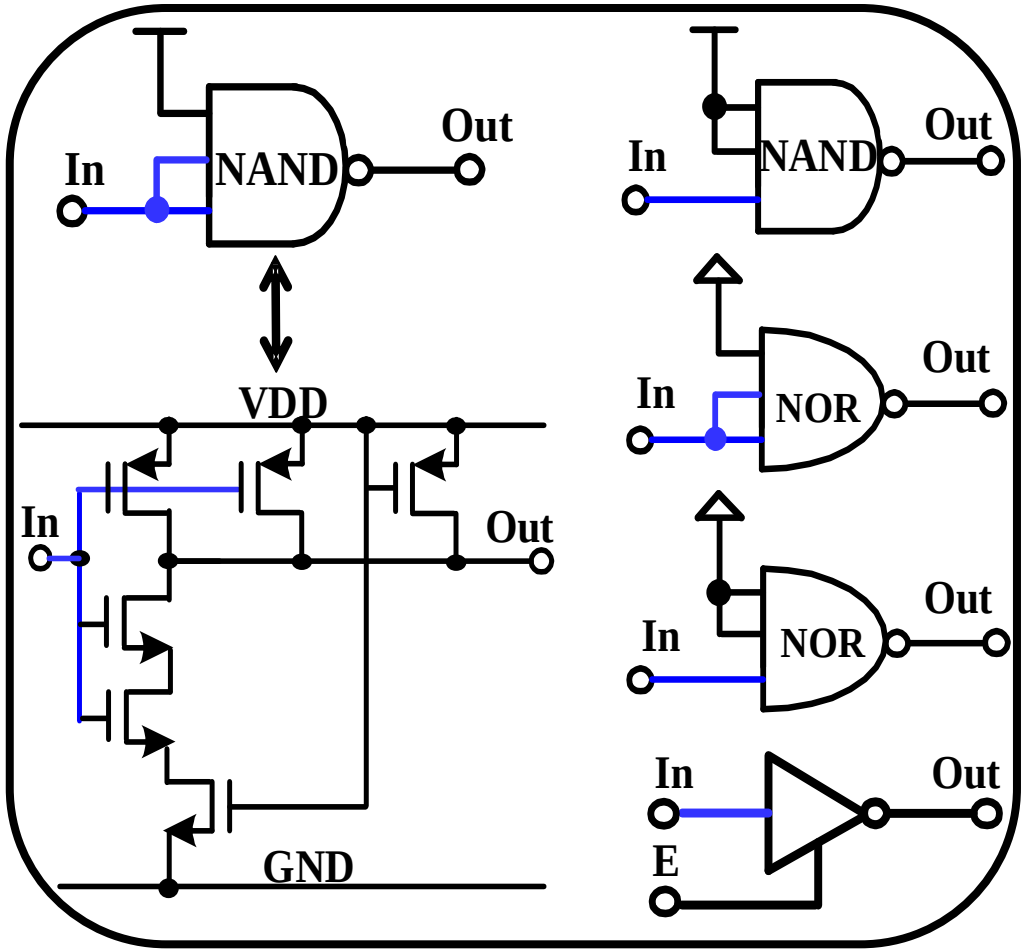
$$\omega_{cutoff} \approx \frac{d}{RC}$$

OPAMP	Analog
RC matched CLK	Analog heavy
Switch	-
Res (R)	Match
Cap (C)	Match

**Kurahashi.P, JSSC07*

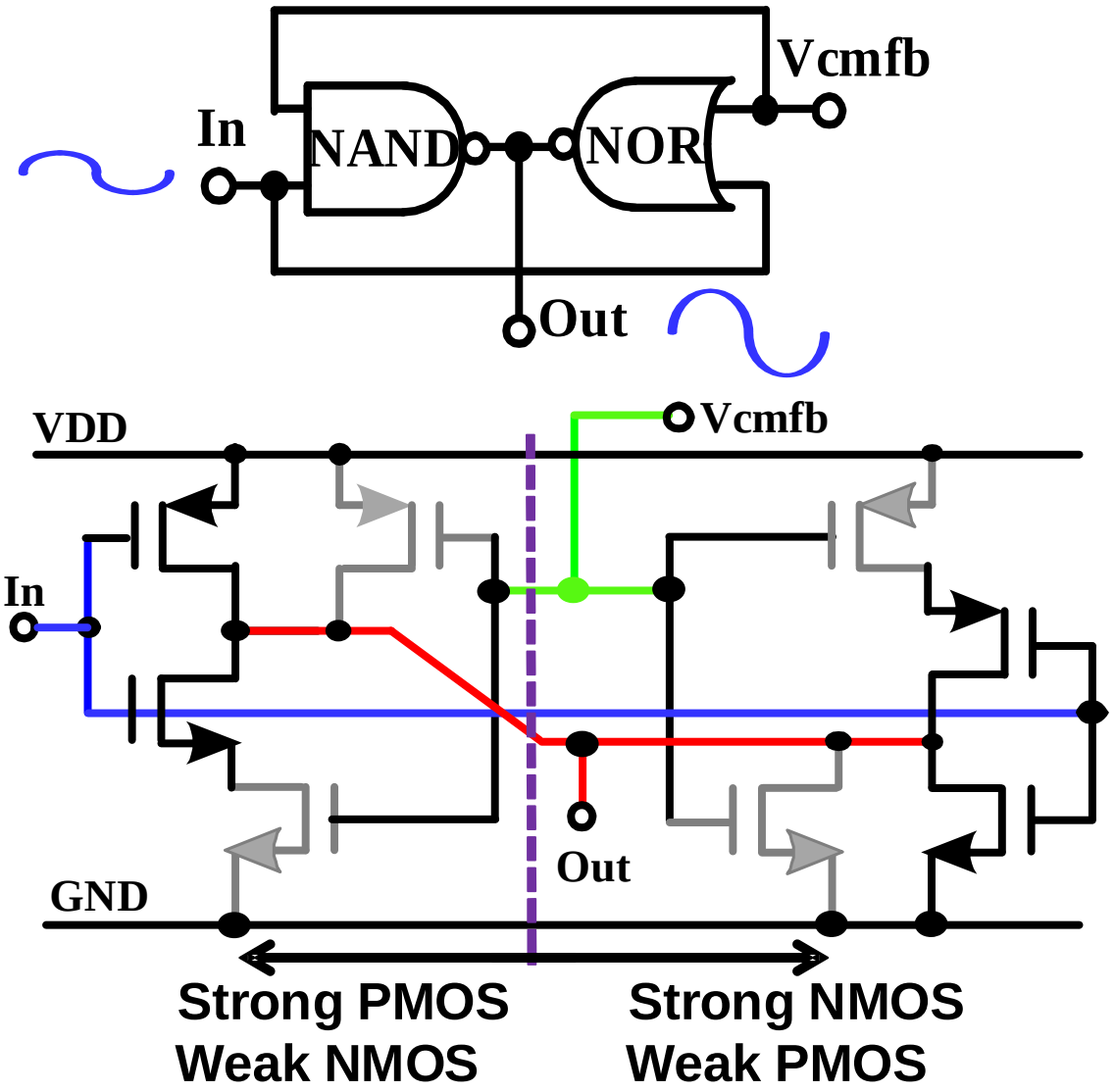
Extended INV Amplifier





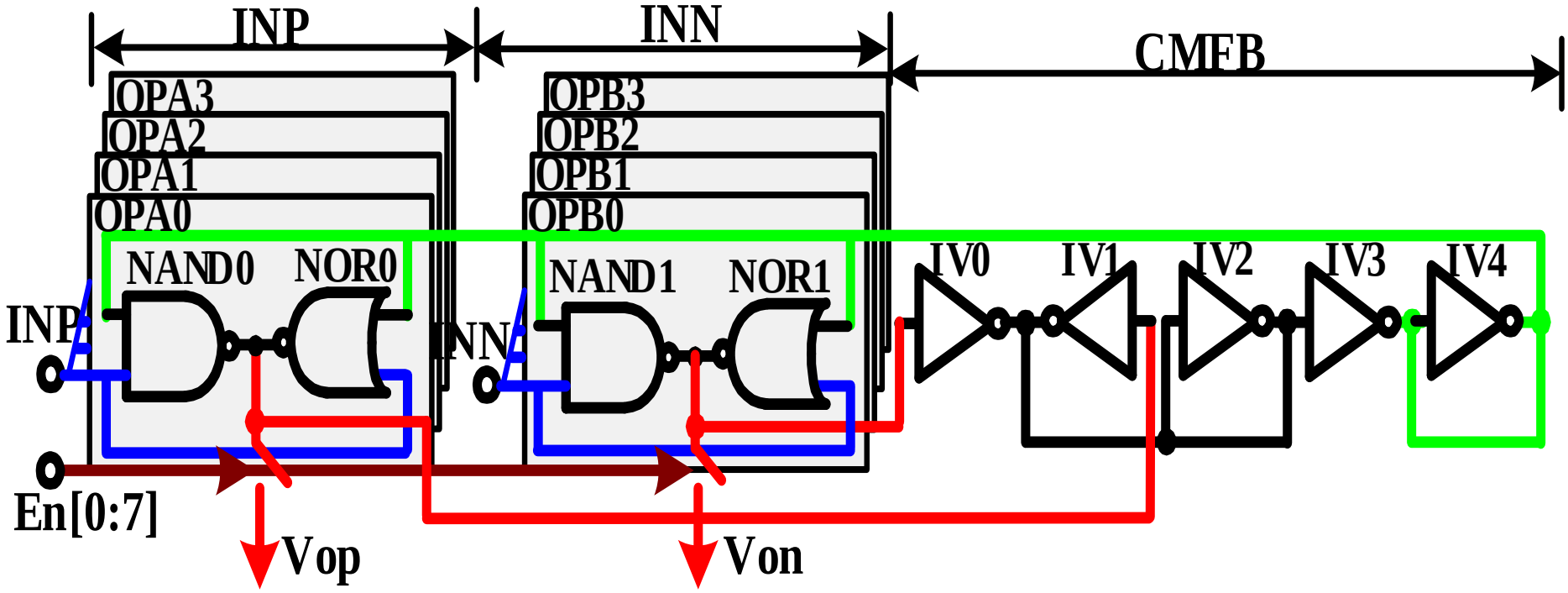
Single input vs multiple inputs

Proposed Amplifier



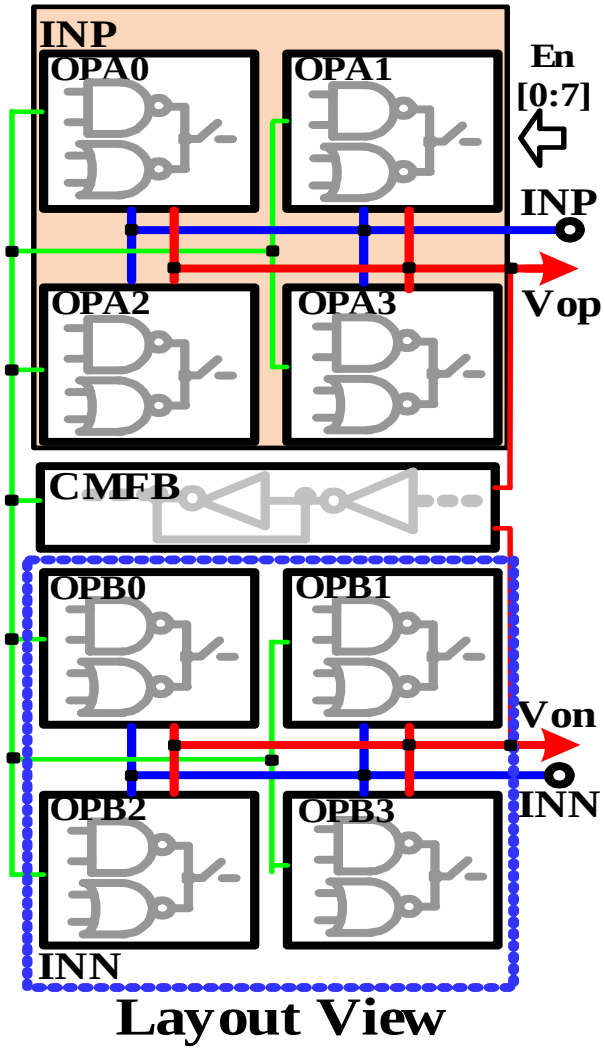
Benefit from different feature of NAND & NOR

Proposed Amplifier (uOP)

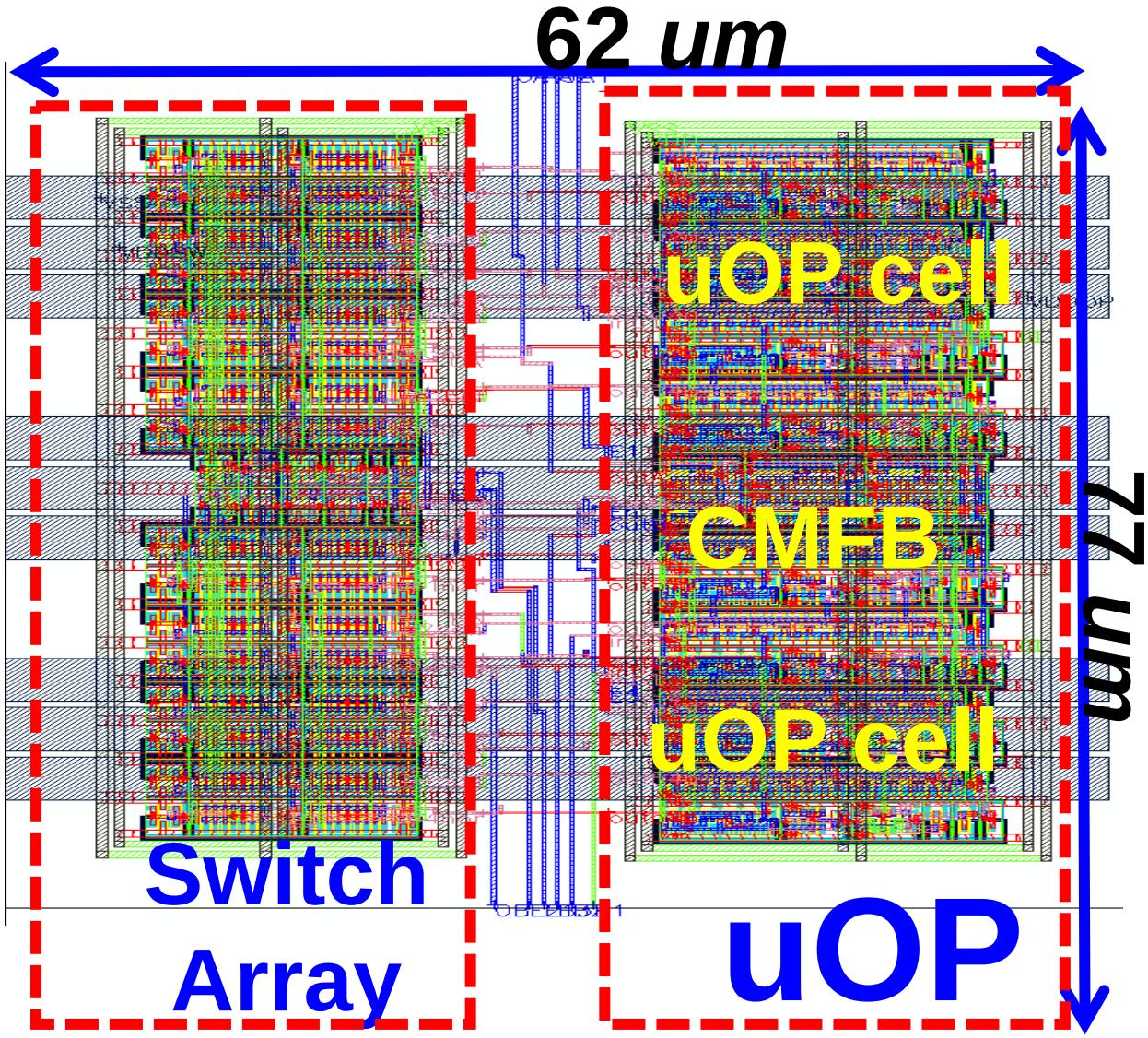


- **Multi-inputs in parallel of diff-in/out amplifier**
- **Shared CMFB on INV chain**
- **Symmetrical layout**

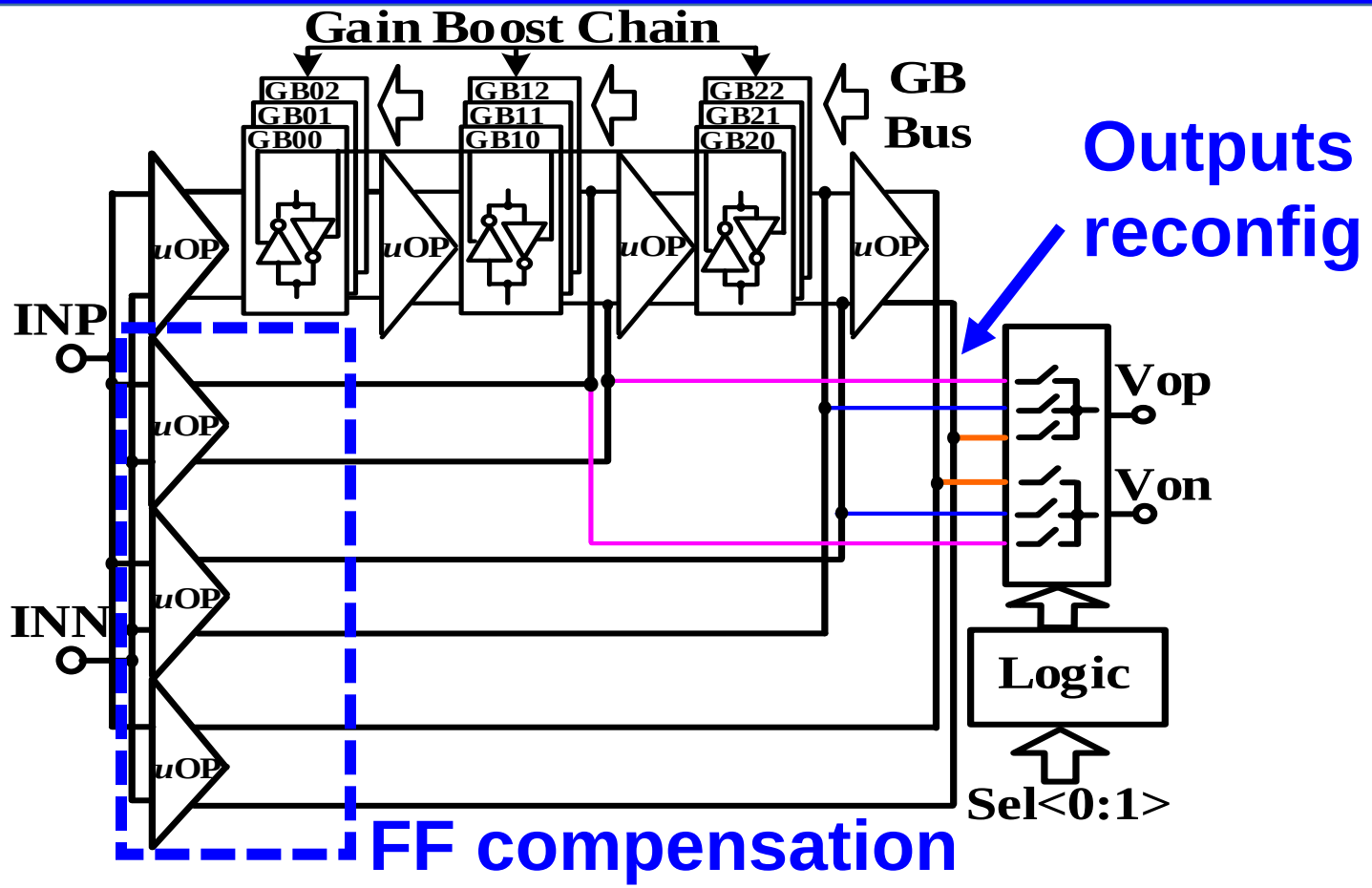
Proposed Amplifier (uOP)



Layout View

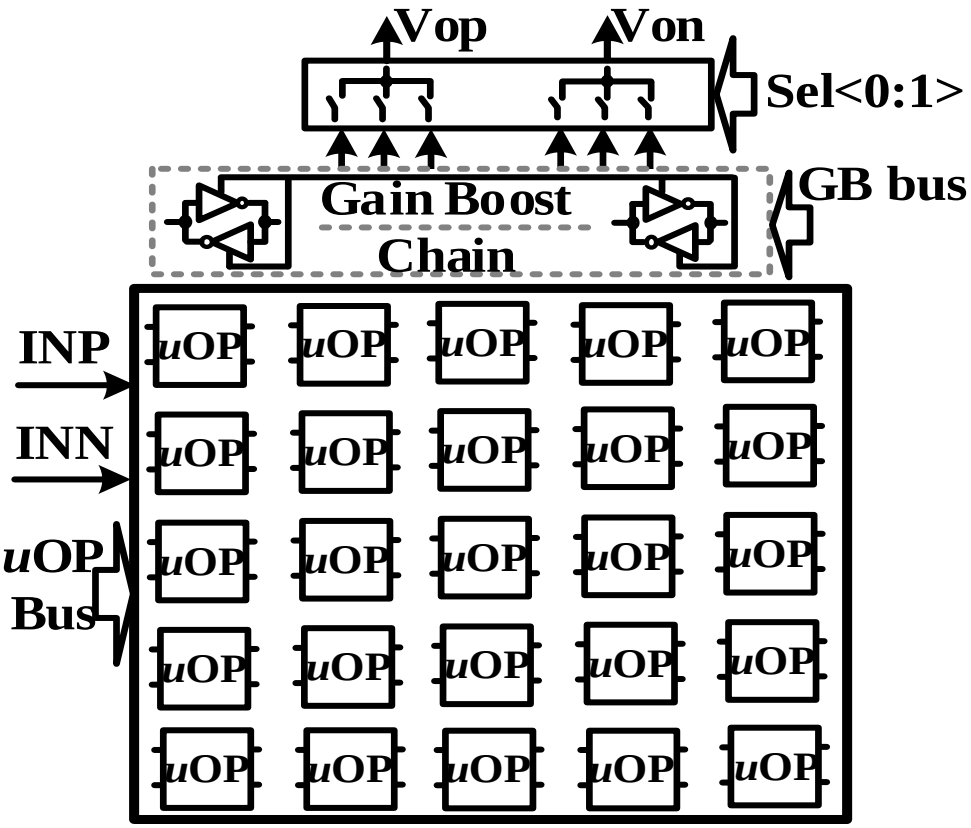


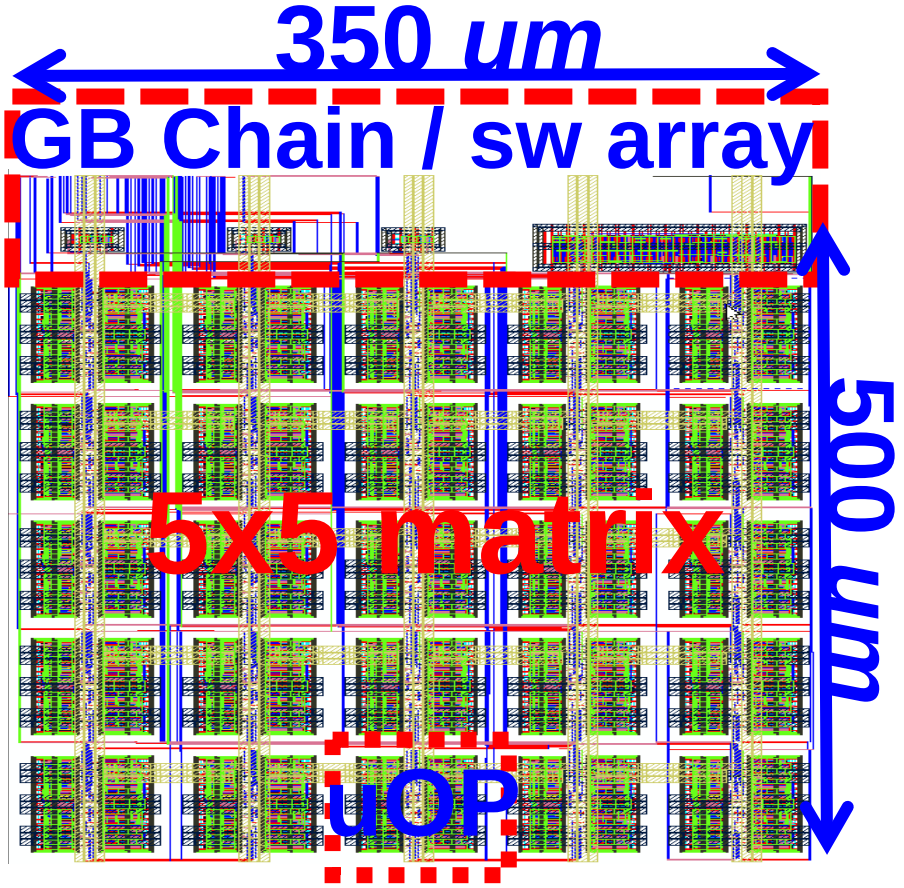
Proposed OPAMP (mOP)



- 2~4 stages reconfig-feedforward compensation
- Reconfig-tri-stage INV as gain boost

Proposed OPAMP (mOP)





- Instantiate from uOP
- 5x5 uOP symmetrical matrix

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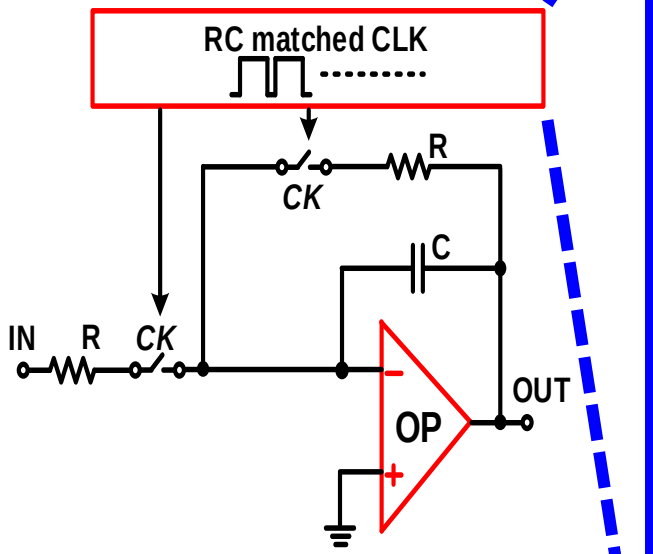
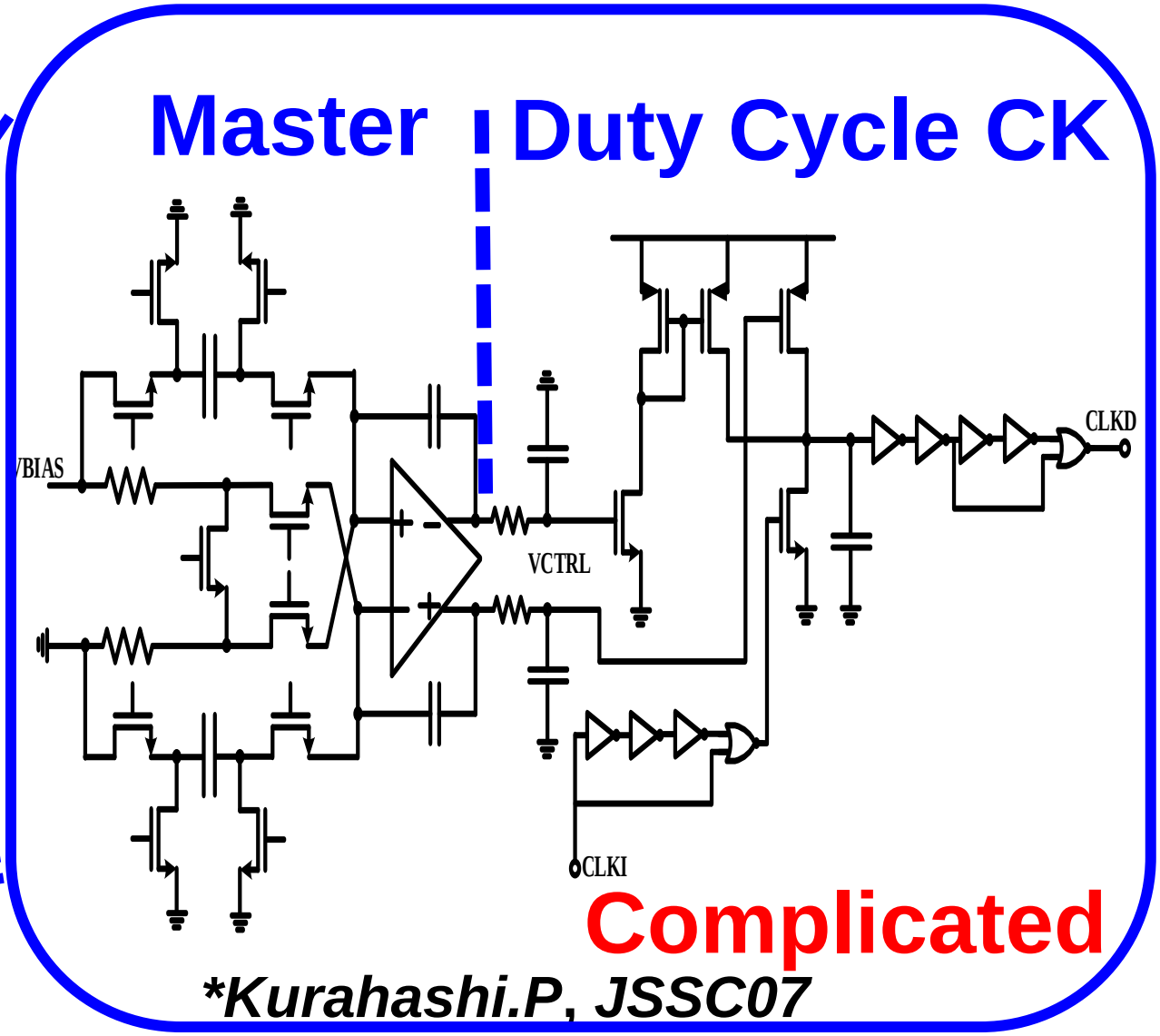
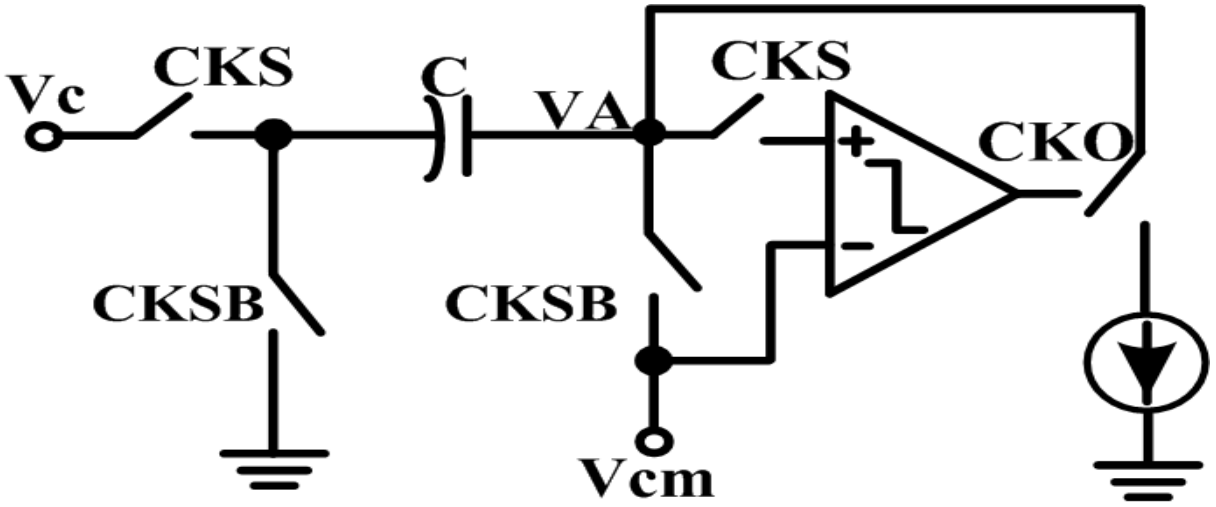
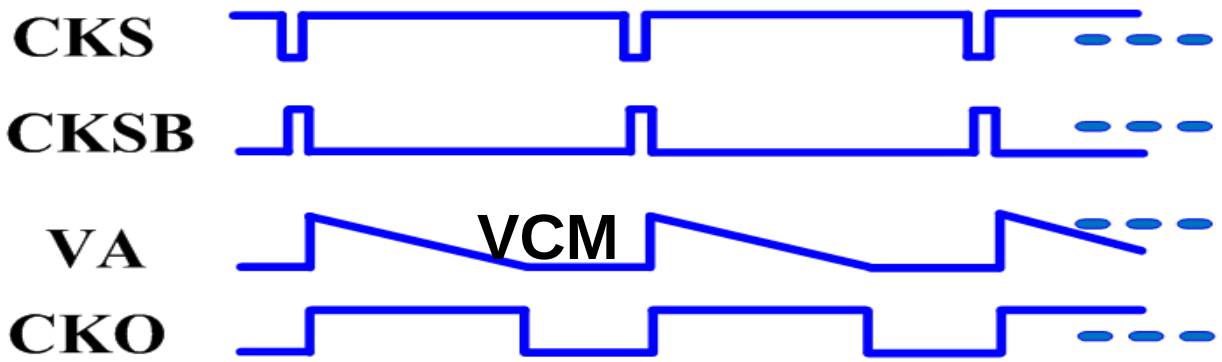
RC Matched CLK





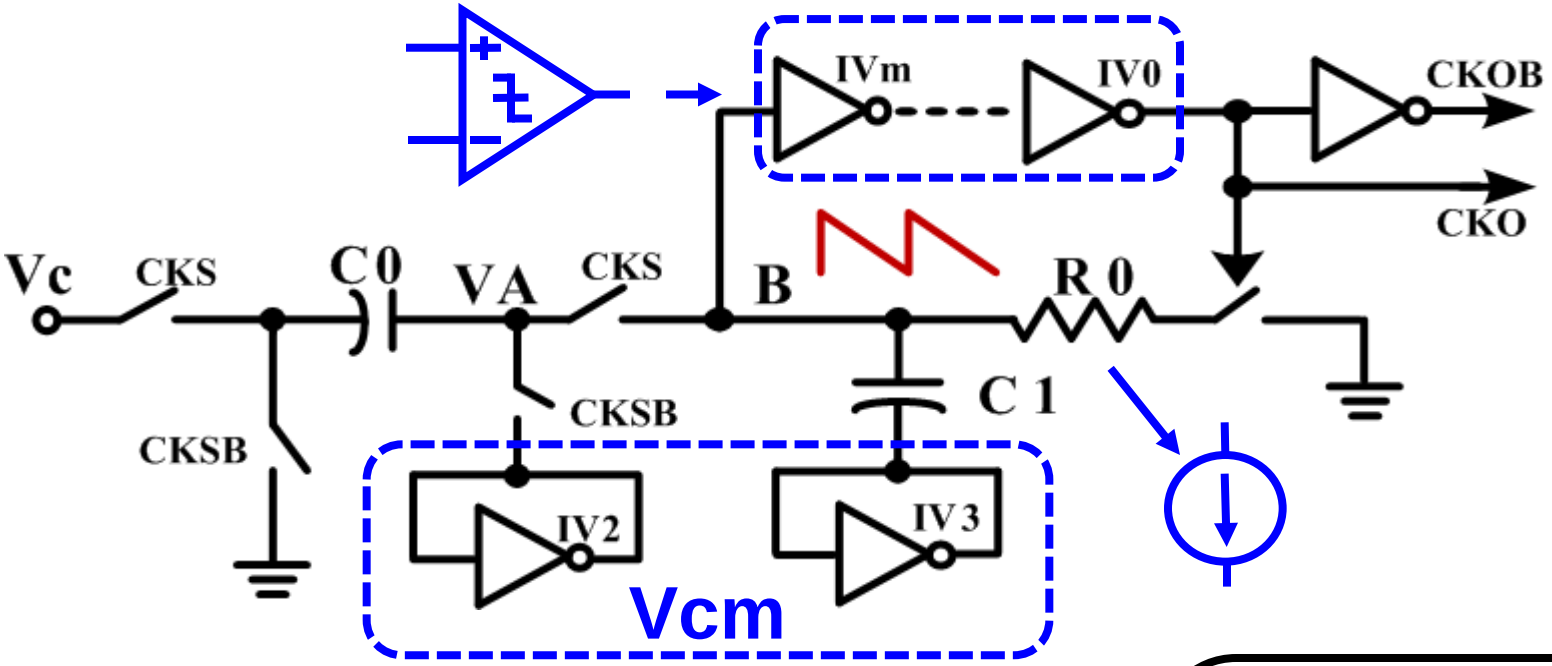
Proposed RC Matched CLK

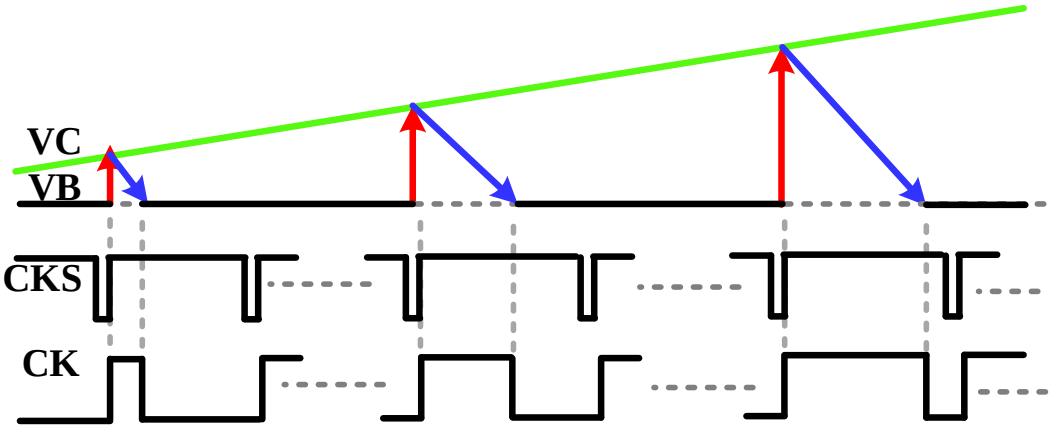




- **Analog voltage control**
- **SC based**

Proposed RC Matched CLK

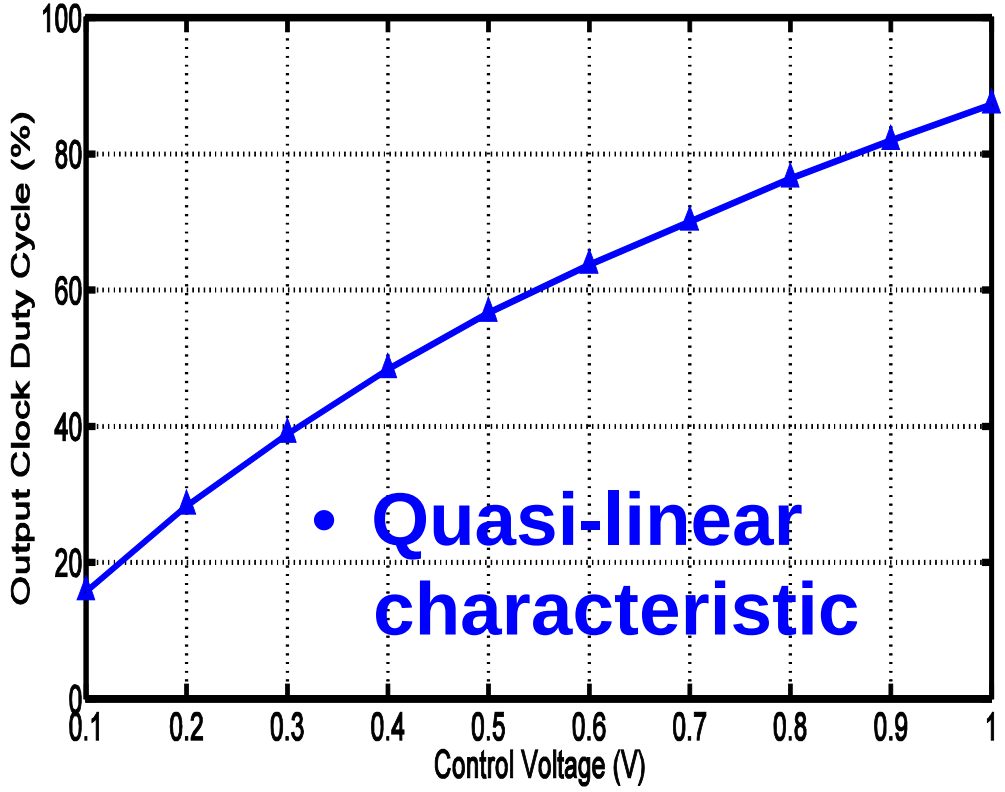


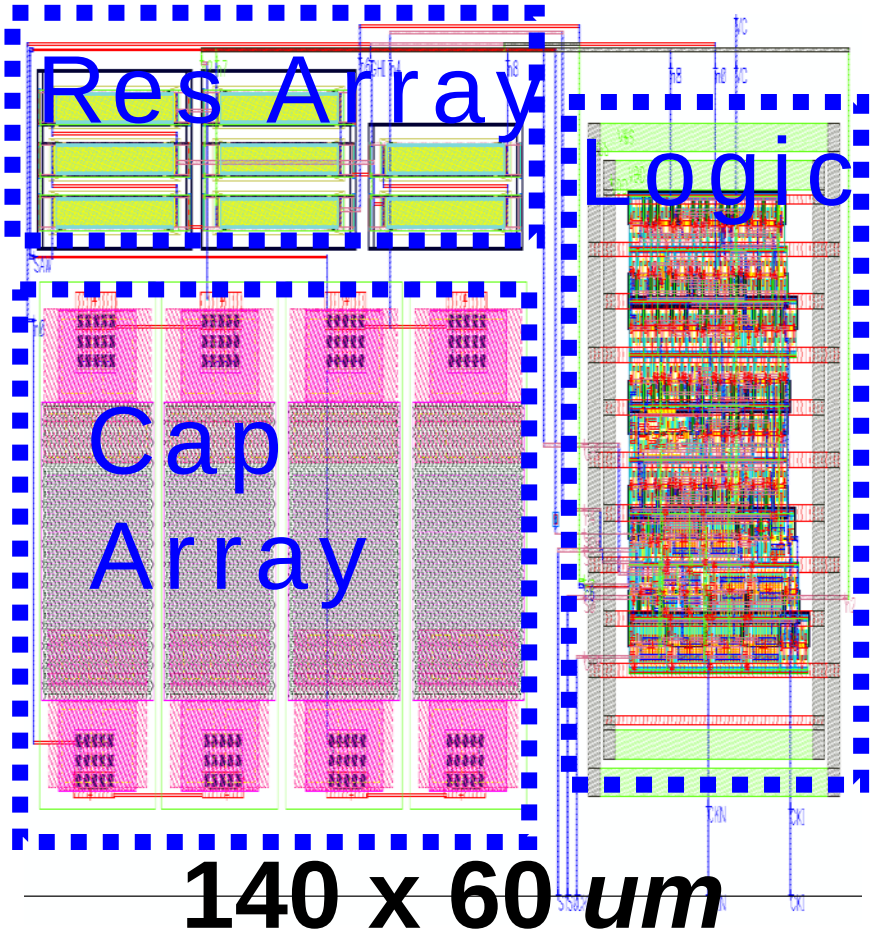


- SC duty-cycle generator
- Track the RC process variation in the filter

Proposed RC Matched CLK

Clock Duty Cycle vs Vc





140 x 60 *um*

Abstract the unit R/C as std cell in lib

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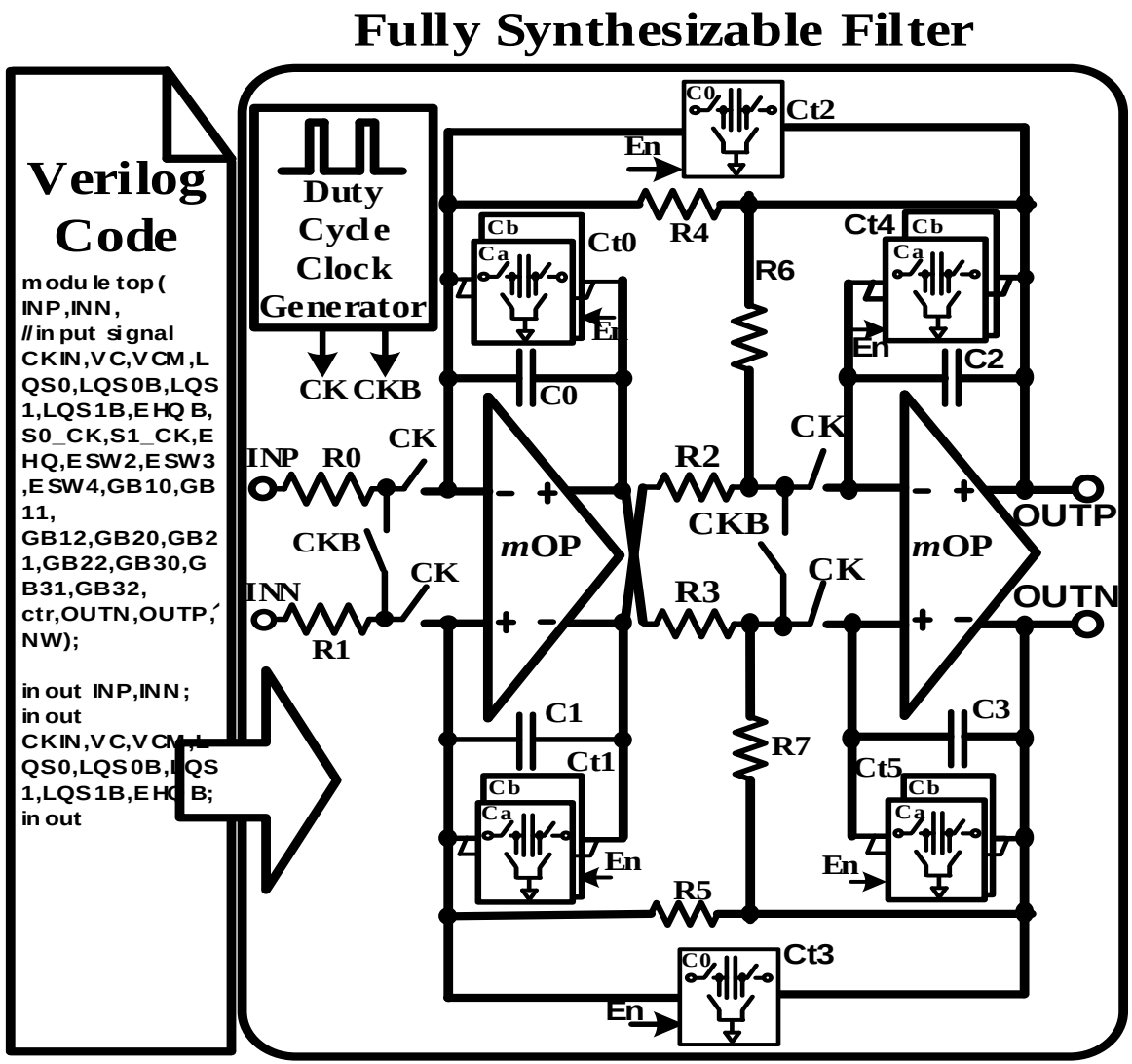
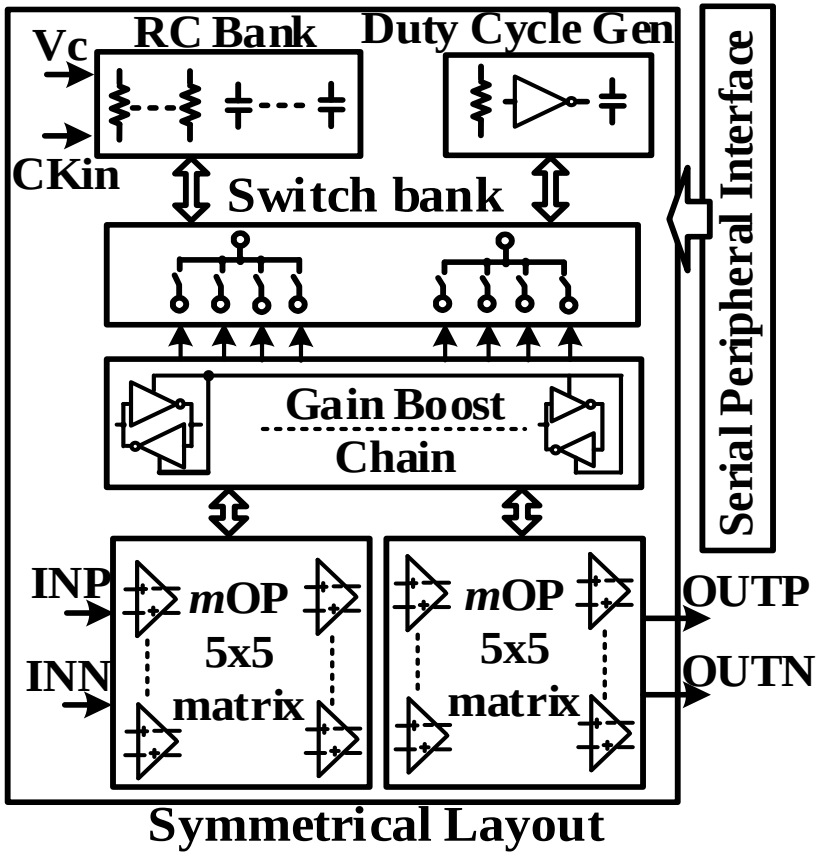
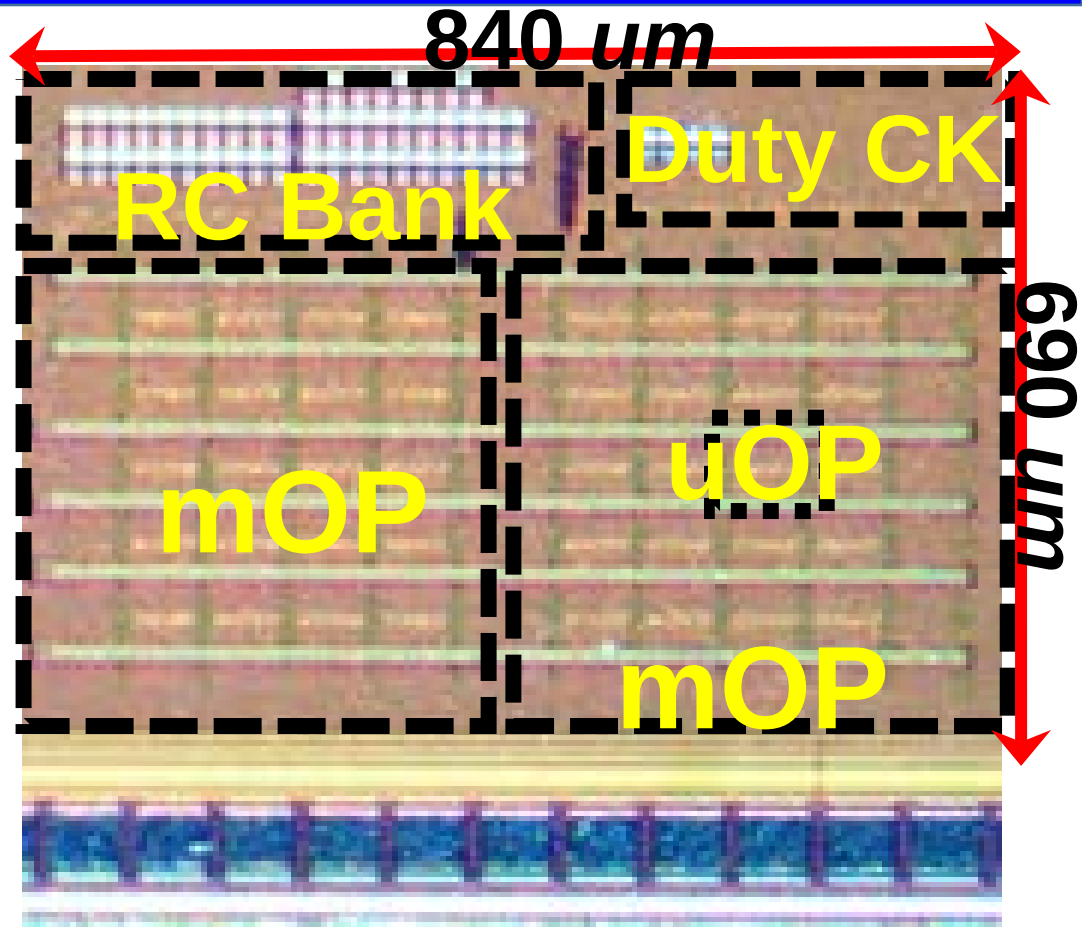
Syn-SRMC Filter



- 2nd SRMC filter
- Analog In/Output
- Instantiate on uOP
- BW varies as CK duty
- Programmable Q

Syn-SRMC Filter





- **0.13um CMOS process**
- **Bottom-up approach for synthesis**

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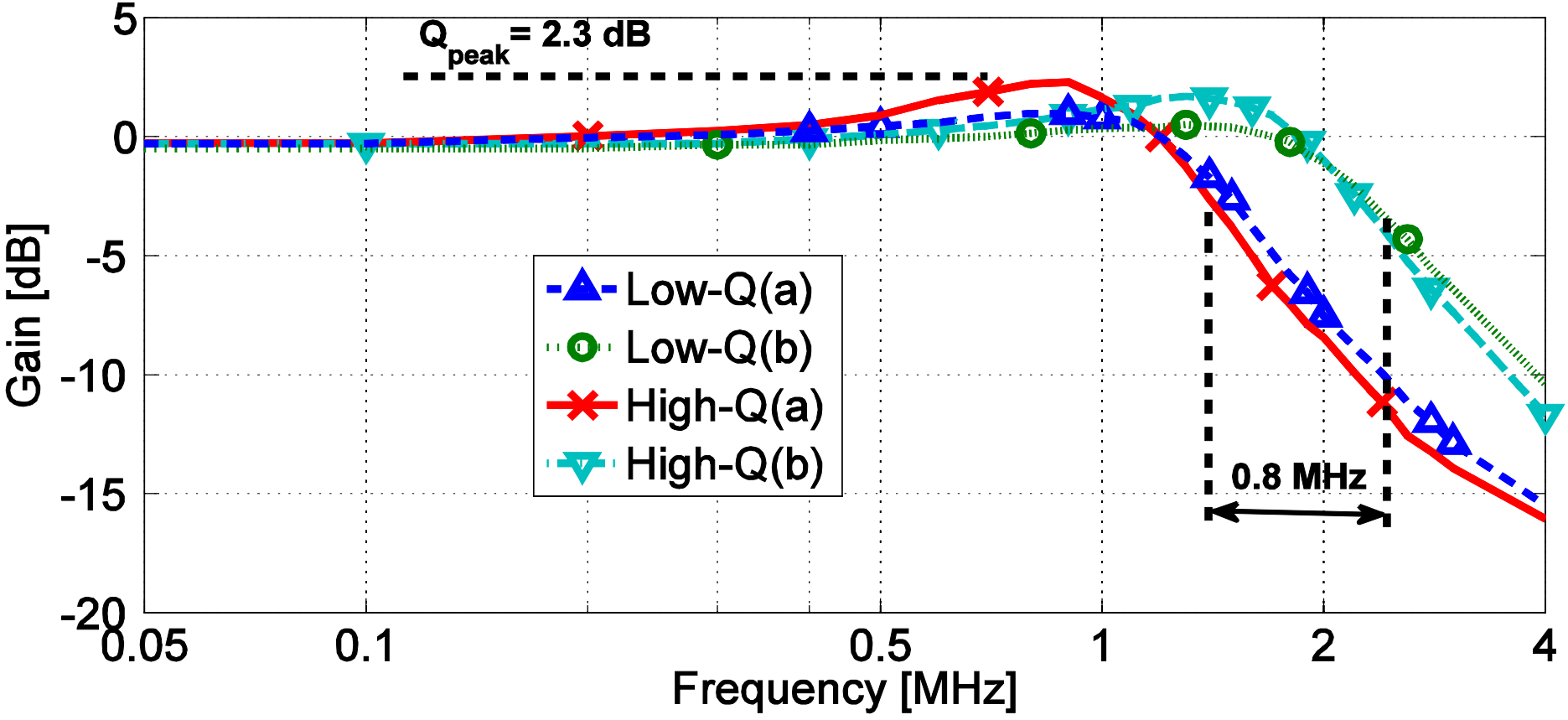
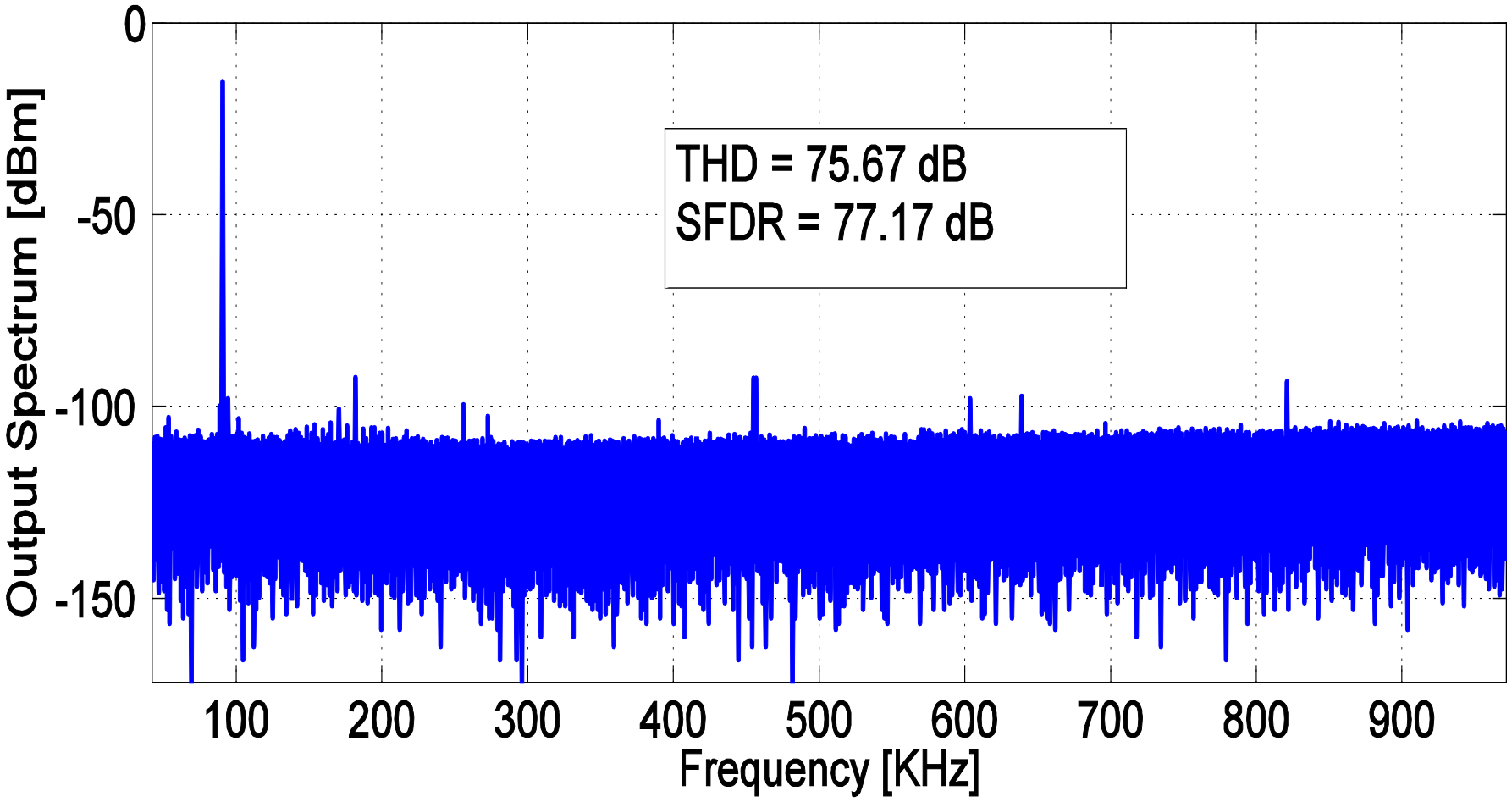
Measurement Results

Reconfig-Q & BW



Vdda=0.4V, Vdd_switch=1.0V, fs=50MHz, 0.1Vsine

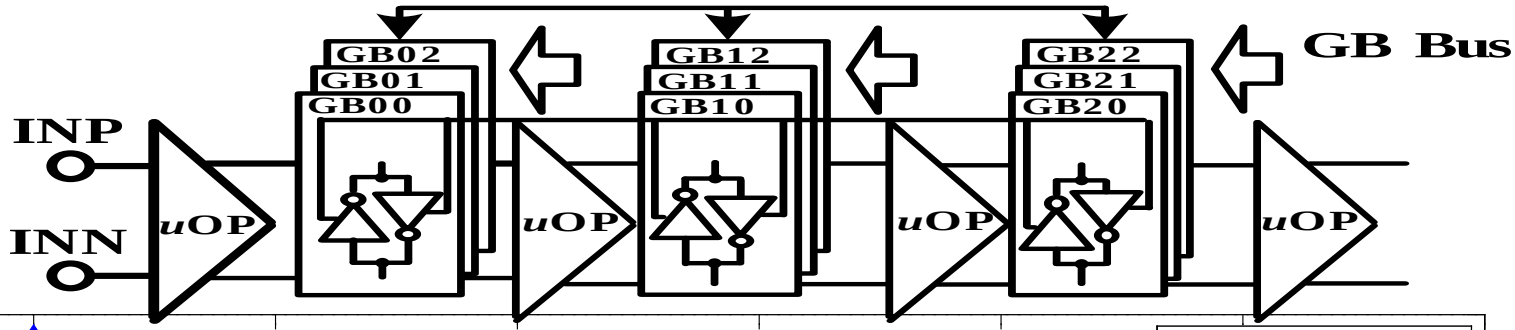
Measurement Results

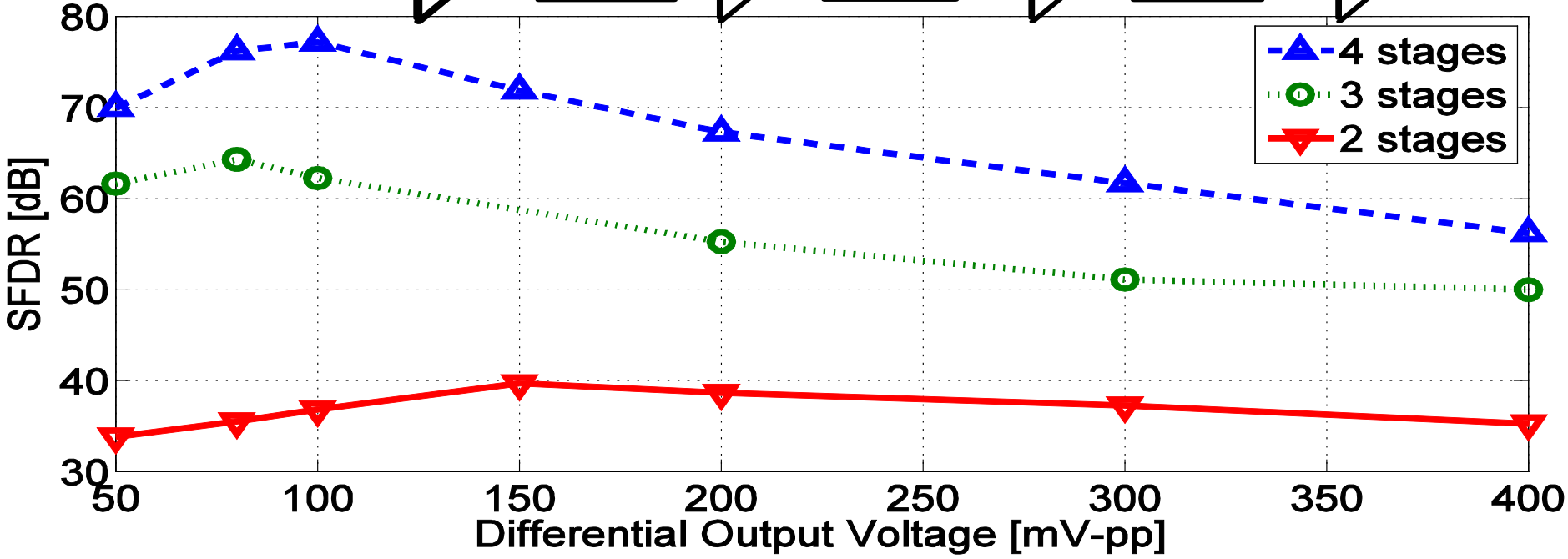


Vdda=0.4V, Vdd_switch=1.0V, fs=50MHz, 0.1Vsine

Measurement Results

Config-mOP

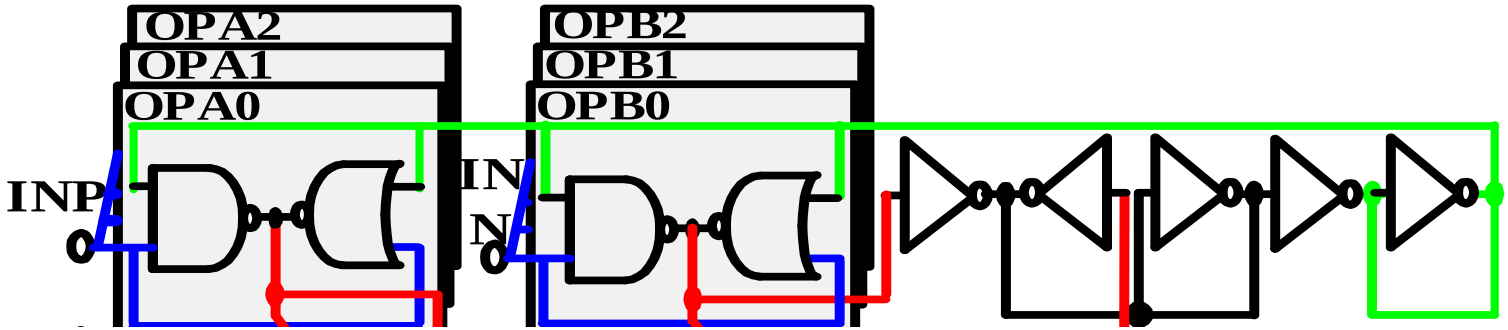


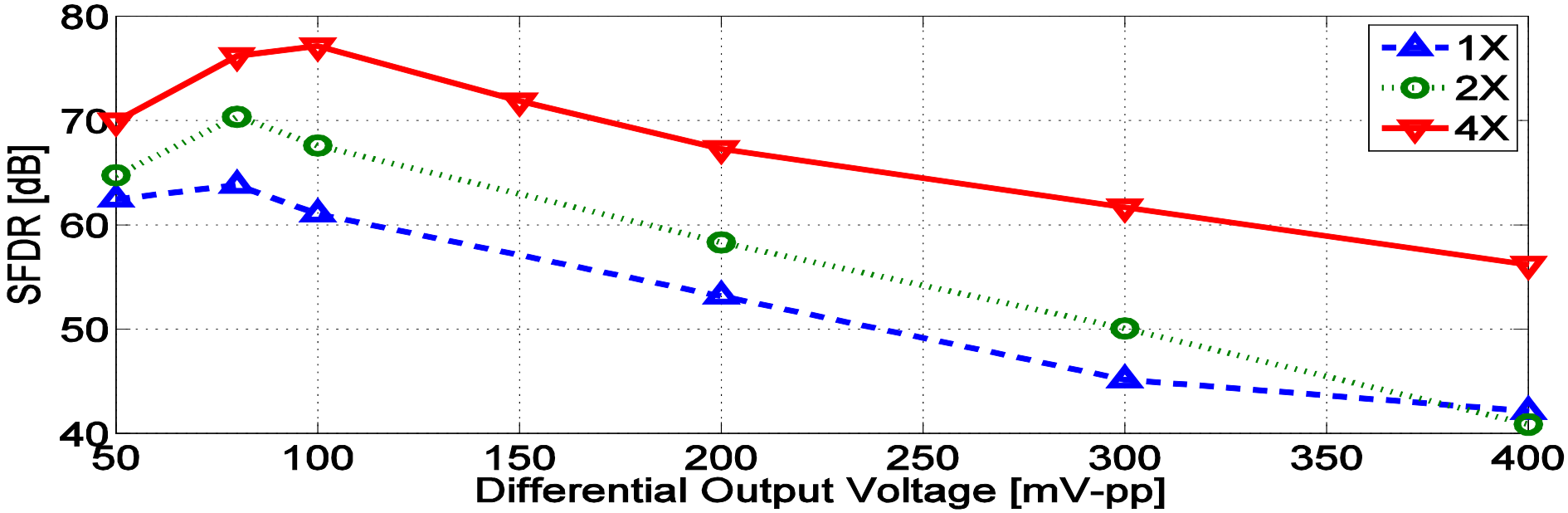


Vdda=0.4V, Vdd_switch=1.0V, fs=50MHz

Measurement Results

Config-uOP





Vdda=0.4V, Vdd_switch=1.0V, fs=50MHz

Comparison Table

	JSSC07	JSSC14	VLSI13	This work		
Supply A/D (V)	0.6	0.6	1.8	0.4 (uOP & mOP) 1.0 (switches)		
THD (dB)	77	60	69	4X	2X	1X
				75	70	63
Power (mW)	1	26.2	2	0.8	0.5	0.3
Filter order	2nd	4th	3rd	2nd		
BW (MHz)	0.135	70	0.5	1.7-2.5		
Size (mm^2)	0.7	0.38	0.68	0.58		
Technology	0.18um	65nm	0.5um	0.13um		

Conclusion

- **Proposed synthesizable uOP/mOP**
- **Proposed synthesizable RC matched CLK**
- **Synthesized programmable SRMC filter**

Acknowledgement

This work was supported by National Science Foundation (NSF) under Grant No. ECCS- 1128715.

Thank You.