Sub-Sampling PLL Techniques

Xiang Gao, Eric Klumperink*
Bram Nauta*

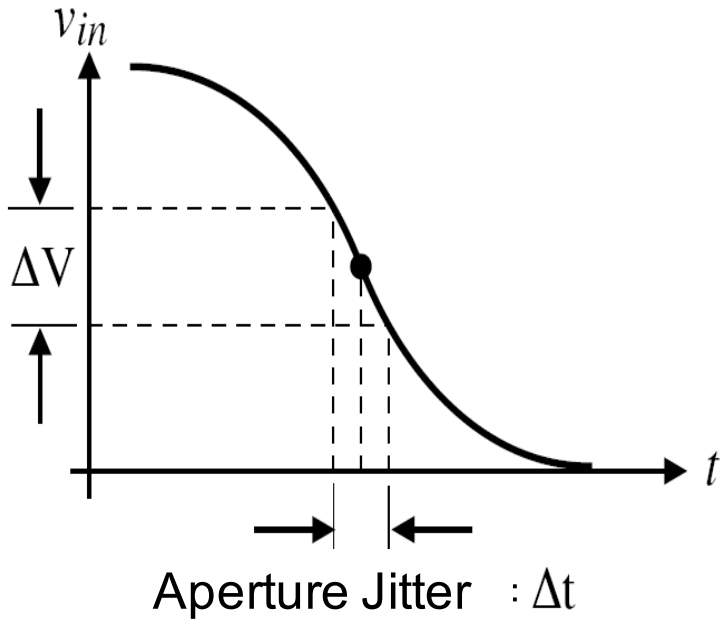
Marvell, Santa Clara, CA
***University of Twente, Enschede, The Netherlands**

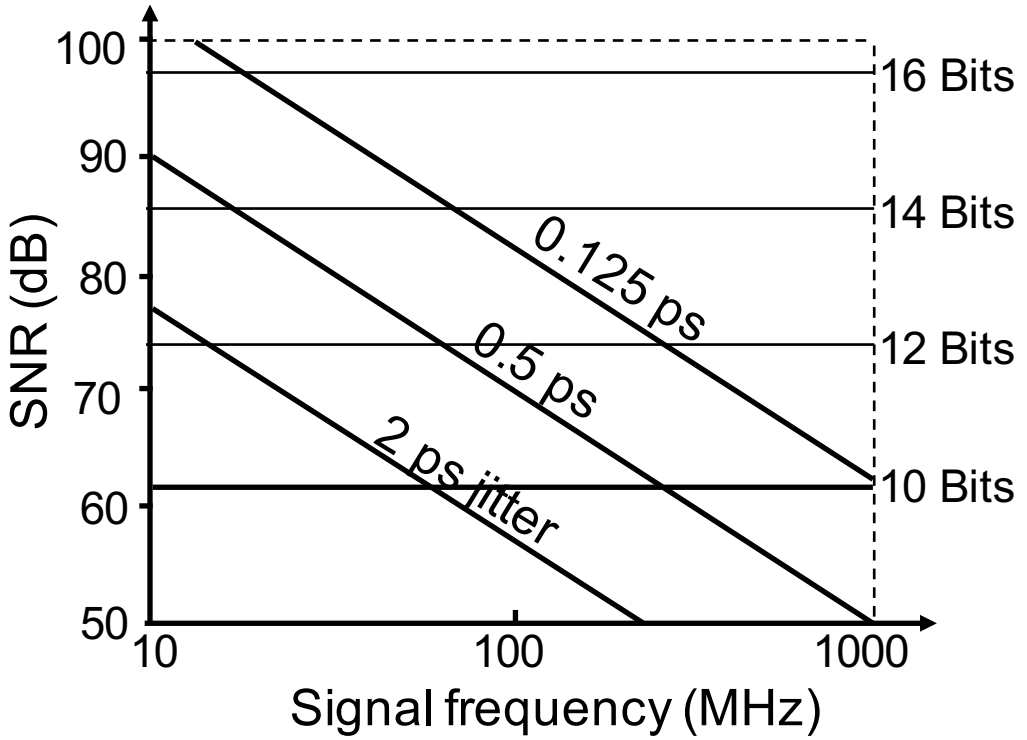
Outline

- Classical CP PLL and PLL FOM
- Sub-Sampling(SS) PLL
- SSPLL Power Reduction Techniques
- SSPLL Spur Reduction Techniques
- Recent SSPLL Development and Discussion

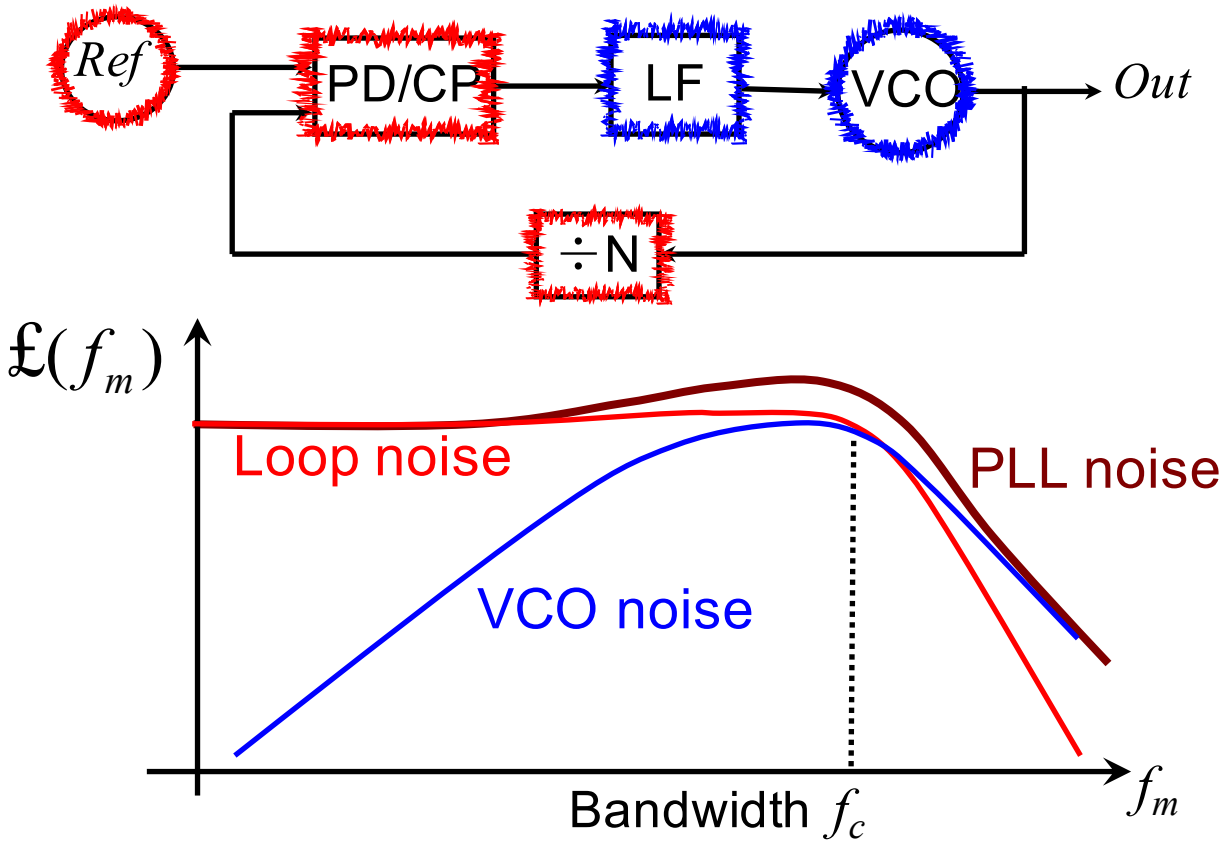
The Need For High Performance PLL

- **Low noise/jitter/power PLL applications**
  - Radio transceivers
  - Wireline and optical data links
  - Analog to Digital converters





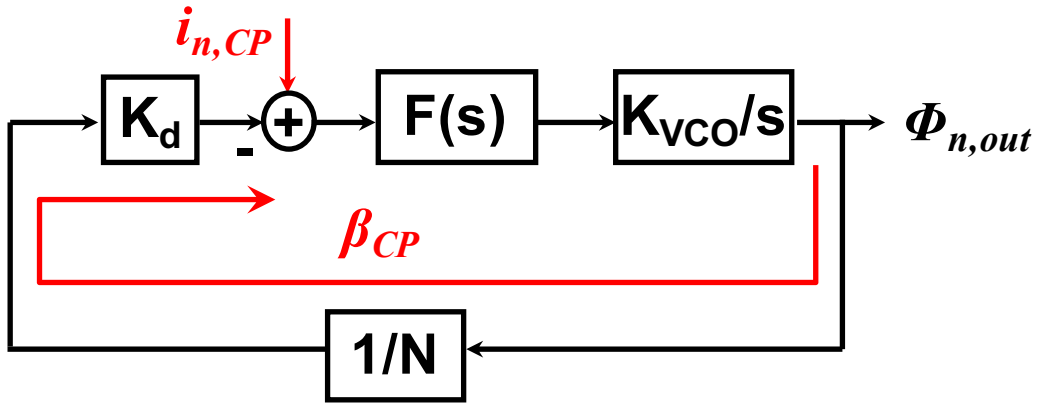
Classical PLL And Noise



- Loop noise low pass filtered, dominant in-band
- VCO noise high pass filtered, dominates out-band

CP Noise

- PD/CP usually major loop noise source in classical PLL



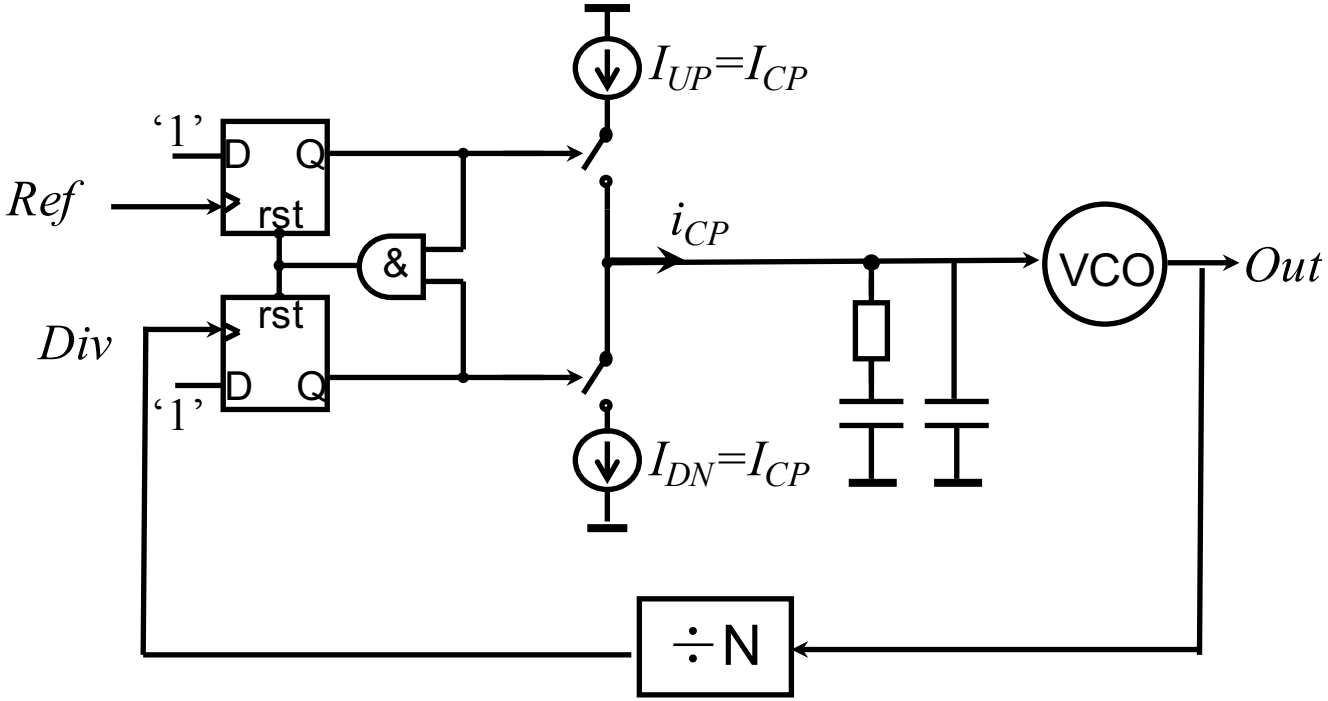
- Define CP feedback gain as: $\beta_{CP} = \dfrac{\Delta I_{out}}{\Delta \phi_{out}}$

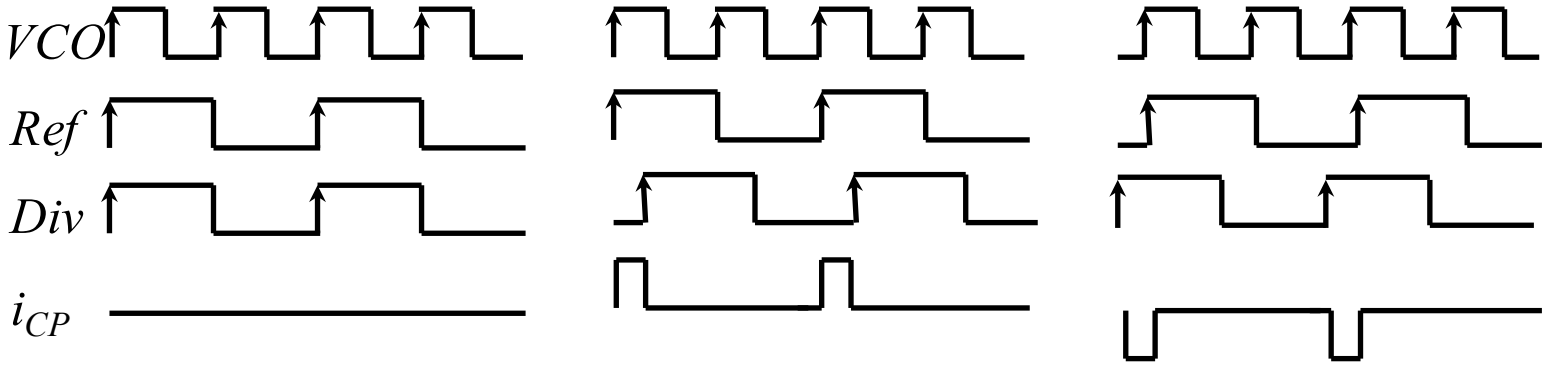
- Inside bandwidth, loop gain is large

$$\pounds_{\text{CP,in-band}} \approx \frac{S_{iCP,n}}{2\beta_{CP}^2}$$

CP noise suppressed by $(\beta_{CP})^2$, Large β_{CP} desired

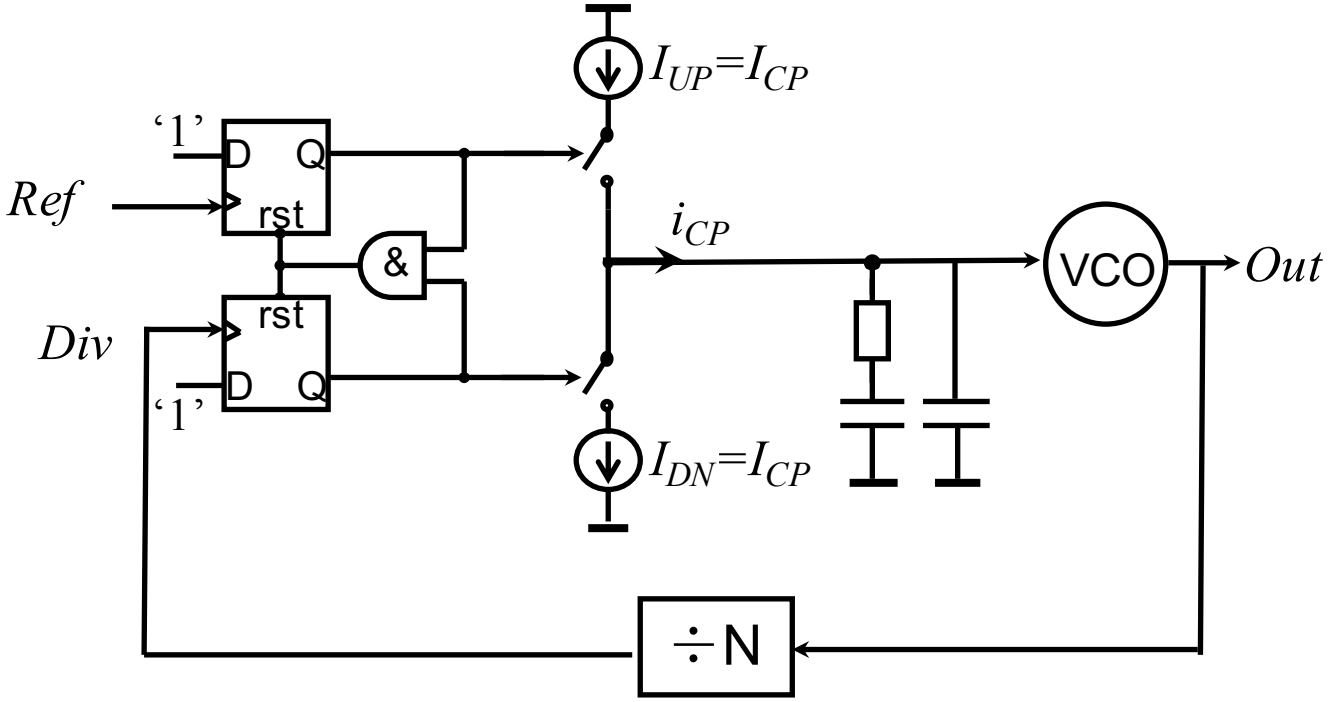
Classical 3-state PFD/CP PLL

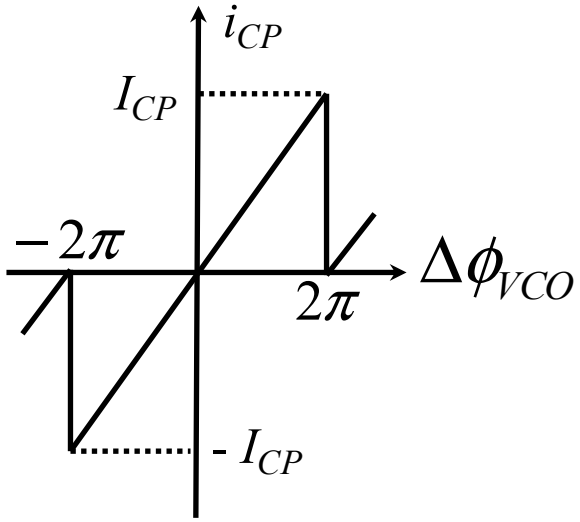




Phase Locked ***Ref* leads** ***Ref* lags**

Classical CP Feedback Gain





■ **CP feedback gain** $\beta_{CP,3state} = \boxed{\frac{1}{N}} \times \frac{I_{CP}}{2\pi}$

- β_{CP} reduced by N, thus CP noise amplified by N^2

Figure of Merit (FOM)

- Figure of Merit (FOM) useful in comparing relative merits and helping designers to approach fundamental limits
- Widely used VCO FOM takes into account fundamental tradeoff between various parameters

$$\mathrm{FOM_{VCO}} = 10\log \pounds(f_m) + 10\log\left(\frac{f_m^2}{f_{VCO}^2}\frac{P_{VCO}}{1\mathrm{mW}}\right)$$

- PLL performance involves more parameters: fref, fout, loop bandwidth, in-band/out-band noise, jitter, power…

PLL Loop FOM

- **Assuming all the fundamentally required power for loop component (PD/CP, divider, ref buffer) is dynamic and neglecting 1/f noise, [1] showed that:**

$$£_{loop,in-band} \propto N^2 \cdot f_{ref} \cdot \frac{f_{ref}}{P_{loop}} = \frac{f_{out}^2}{P_{loop}}$$

- **A FOM for PLL loop design is thus defined as:**

$$FOM_{loop} = 10\log £_{loop,in-band} + 10\log[(\frac{1Hz}{f_{out}})^2 \cdot \frac{P_{loop}}{1mW}]$$

- Independent on f_{ref}: larger f_{ref} reduces loop noise but also increases dynamic power

[1] X. Gao, E. Klumperink, P. J. F. Geraedts and B. Nauta, "Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops," *IEEE Trans. Circuits Syst. II*, vol. 56, no.2, pp. 117-121, Feb. 2009.

PLL FOM

■ **In optimized PLL, Loop/VCO contributes equally to both jitter and power, the minimum achievable jitter is [1]:**

$$\sigma^2_{t,PLL,\min} = \frac{1}{(1Hz)^2} \cdot \frac{1mW}{P_{PLL}} \cdot \frac{1}{\pi} \cdot 10^{\frac{FOM_{loop}+FOM_{VCO}}{20}}$$

■ **A PLL FOM is thus defined as:**

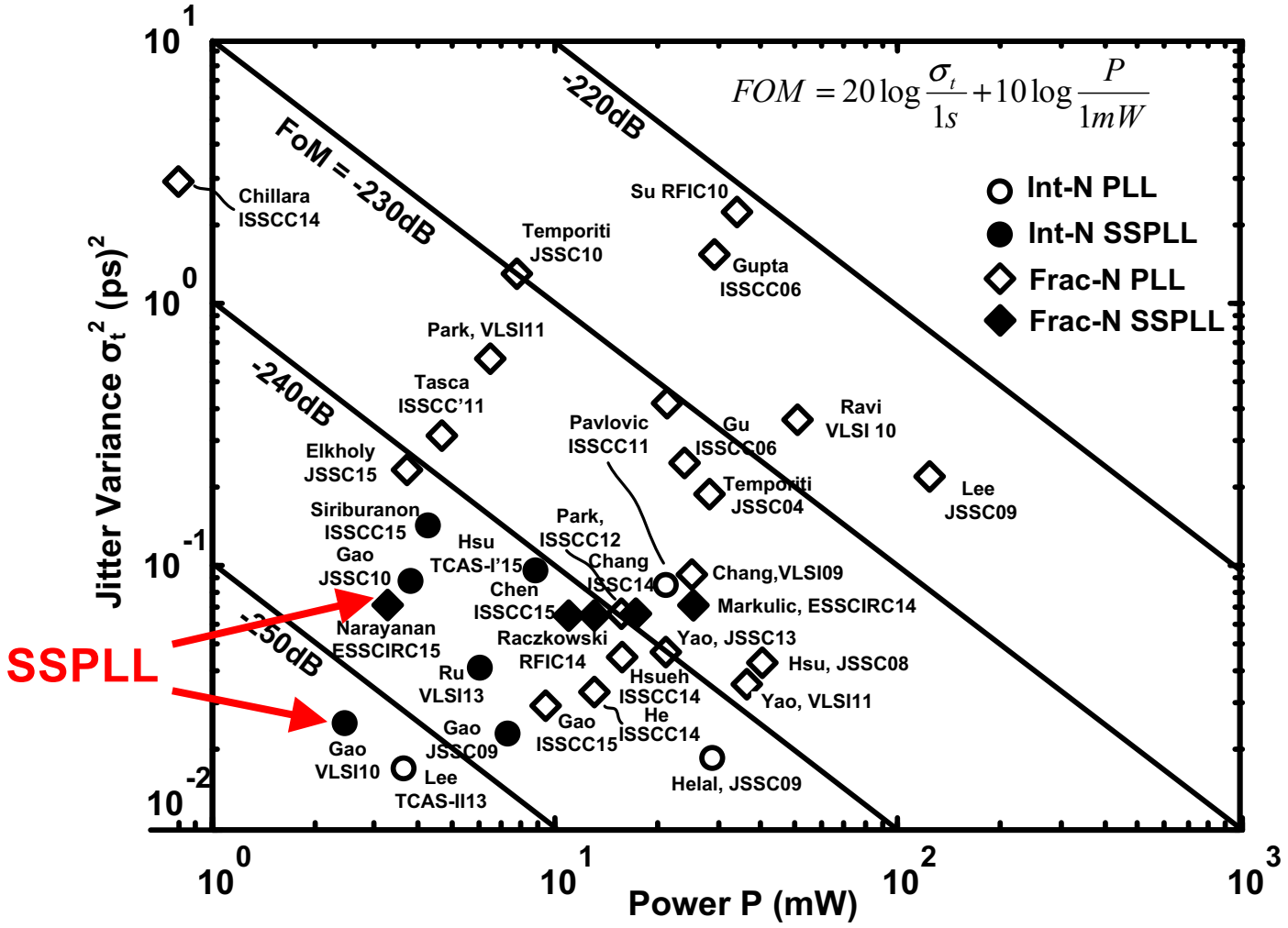
$$FOM_{PLL} = 10\log[(\frac{\sigma_{t,PLL}}{1s})^2 \cdot \frac{P_{PLL}}{1mW}].$$

- or:
$$FOM_{PLL} = \frac{FOM_{loop} + FOM_{VCO}}{2} + 10\log\frac{1}{\pi}.$$

- Design quality (FOM) of the loop and VCO are equally important in achieving good PLL FOM

State-of-Art PLLs

■ This PLL FOM has been widely adopted recently. The FOM generally improves over the years. The SSPLLs currently hold best FOM for both int-N and frac-N PLLs.



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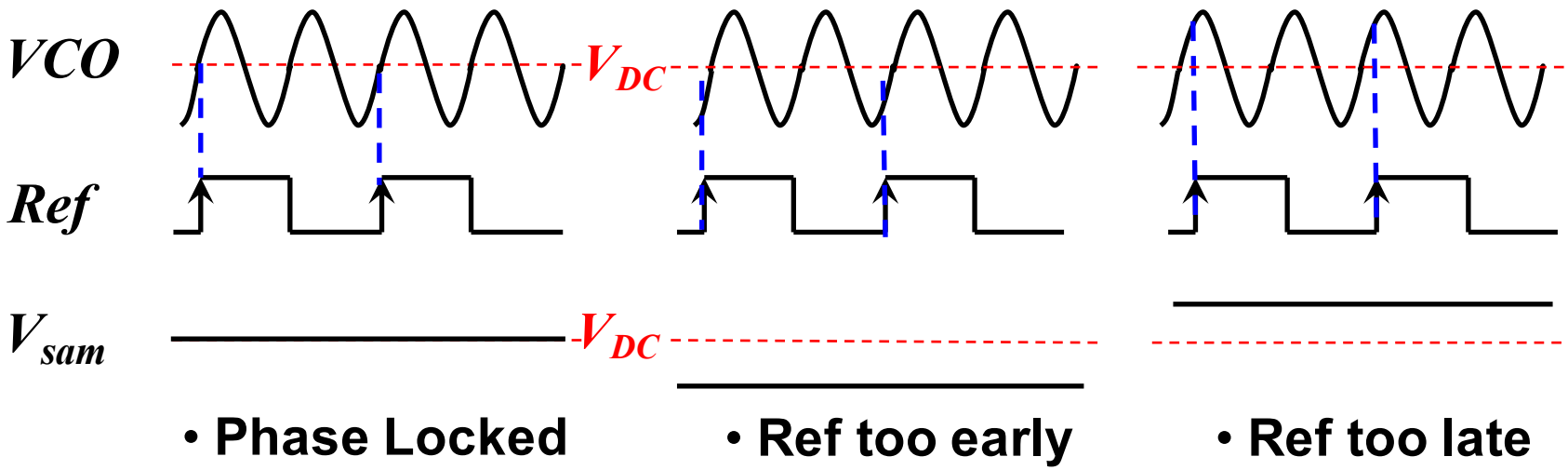
- **Sub-Sampling(SS) PLL**
- SSPLL Power Reduction Techniques
- SSPLL Spur Reduction Techniques
- Recent SSPLL Development and Discussion

Sub-Sampling Phase Detector (SSPD)

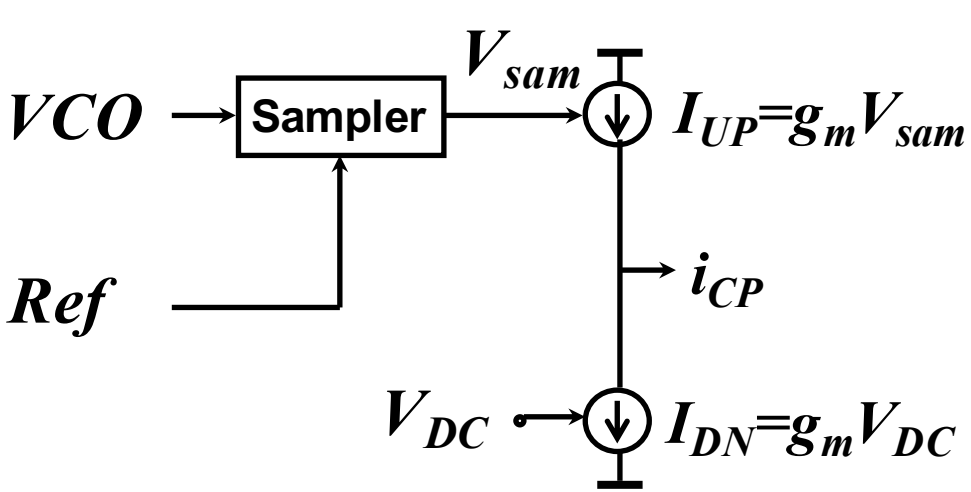
■ Sub-Sampling PD for Integer-N PLL

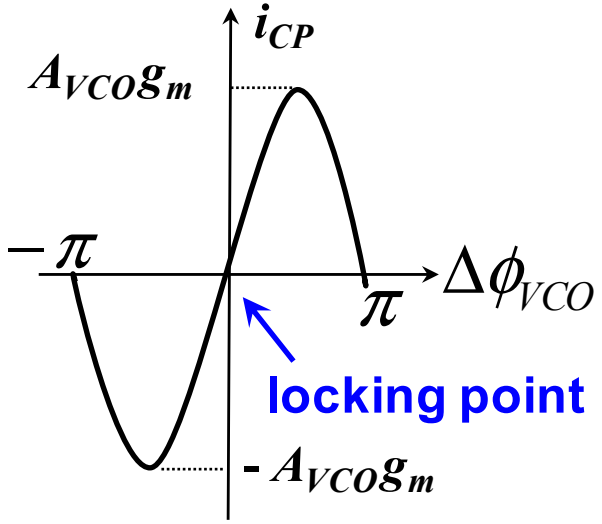


- VCO sub-sampled by Ref without going through divider
- Phase/Timing error converted into voltage error
- High phase detection gain due to high VCO dv/dt

[2] X. Gao, E. Klumperink, M. Bohsali and B. Nauta, "A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is not Multiplied by N^2," *IEEE J. Solid-State Circuits,* vol. 44, no.12, pp. 3253-3263, Dec. 2009.

Sub-Sampling PD/CP (SSPD/CP)





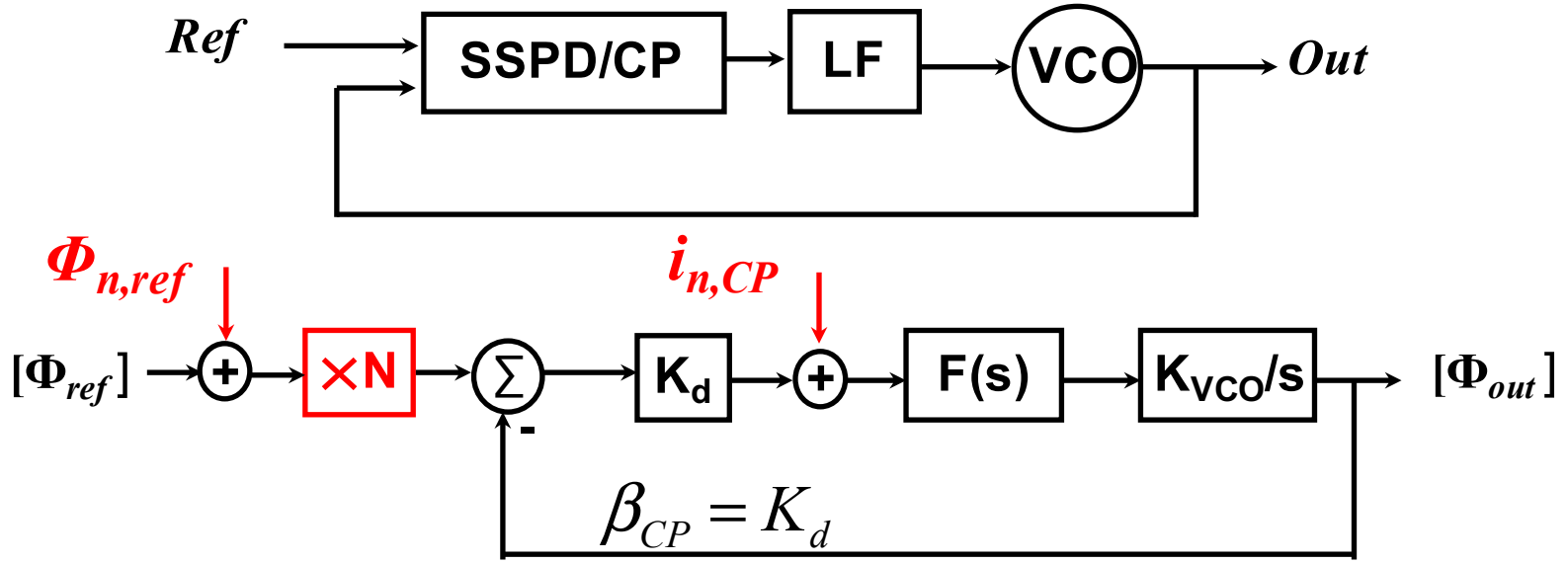
- Voltage controlled CP
- Ideal characteristic

■ Detection characteristic is fairly linear once in lock

$$\beta_{CP} = K_d = \frac{\Delta I_{out}}{\Delta\phi_{VCO}} = \frac{g_m \cdot A_{VCO}\sin(\Delta\phi_{VCO})}{\Delta\phi_{VCO}} \approx g_m A_{VCO}$$

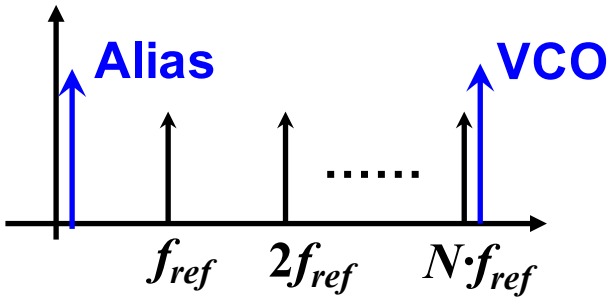
There is no N factor !

SSPLL And Modeling



- **No Divider but a virtual Multiplier**
  - **Sub-sampling process**

$$f_{alias} = f_{VCO} - N \cdot f_{ref}$$

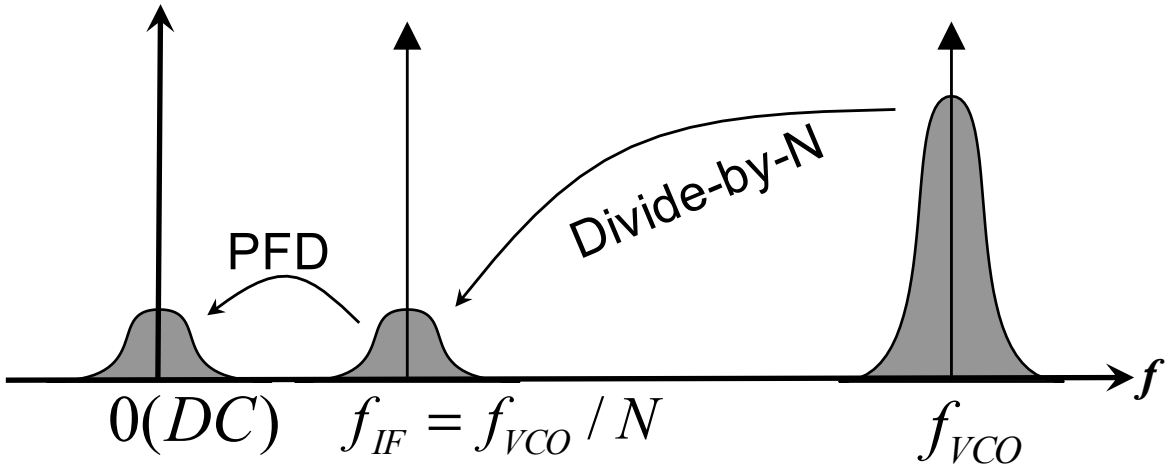


  - **Ref noise multiplied by N, same as in classical PLL**

CP noise *NOT* multiplied by N !!

N Factor On CP Noise: Another Angle

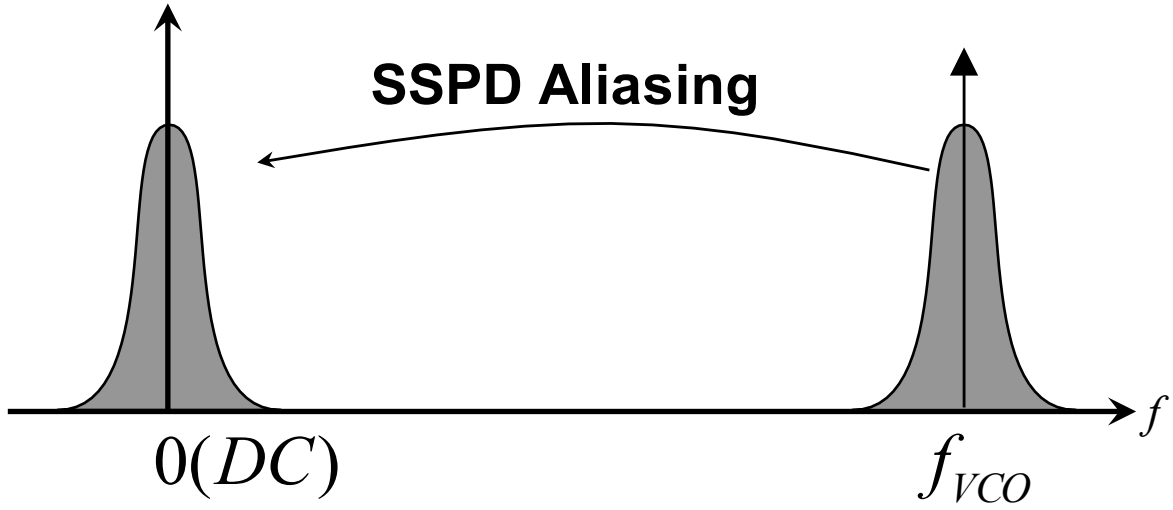
- PLL is a loop back transceiver: VCO transmits 'signal' (VCO noise), the Loop receive/process it and feed it back to cancel/suppress the VCO noise



- Classical PLL is analogous to a superheterodyne receiver
  - Divider: 1st down-converter, to low IF
  - PFD: 2nd down-converter, to DC
  - CP/LPF: Base Band (TIA/LPF)

- Divider as down-converter has 1/N attenuation and 20logN noise figure, PFD/CP noise thus amplified by N^2

Why no N Factor In SSPLL



- SSPLL is analogous to a direct conversion receiver
- SSPD down-converter has no attenuation but a gain of 1, thus better NF and no amplification for PD/CP noise

SSPLL VS Classical PLL

- SSPLL ideally has no divider noise
- SSPLL CP noise greatly suppressed by large β_{CP}
  - Comparing β_{CP} with 3-state PFD/CP assuming same I_{CP}

$$\frac{\beta_{CP,SSPD}}{\beta_{CP,3state}} = 4\pi \cdot N \cdot \frac{A_{VCO}}{2I_{CP}/g_m} = 4\pi \cdot N \cdot \frac{A_{VCO}}{V_{gs,eff}} \gg 1$$

e.g. $$= 4\pi \times 40 \times \frac{0.4V}{0.2V} \approx 1000$$

SSPLL has much larger β_{CP}, thus more CP noise suppression

SSPD Noise

■ In-band Phase Noise due to SSPD

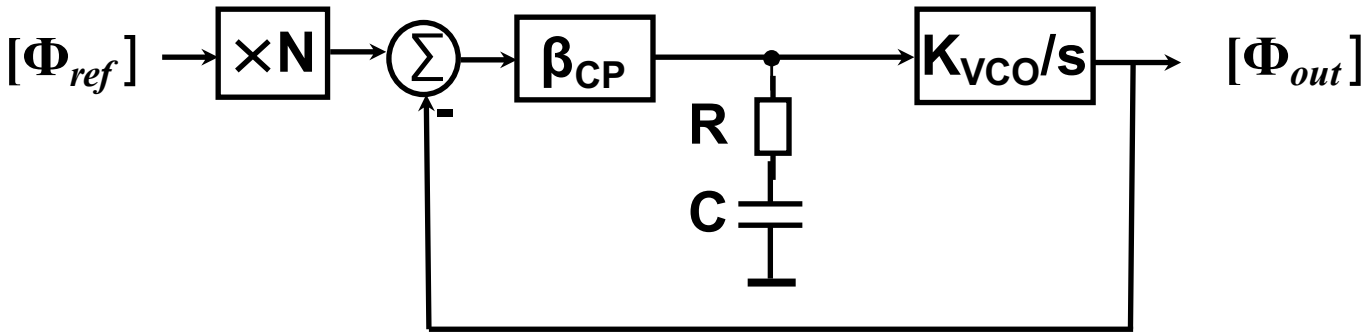
$$L_{in-band,SSPD} = \frac{kT}{C_{sam} \cdot f_{ref} \cdot A_{VCO}^2}$$

e.g. $$= \frac{4 \times 10^{-21}}{10f \times 40M \times 0.4^2} \approx -132 dBc/Hz$$

C_{sam} as small as 10fF enough for very low phase noise

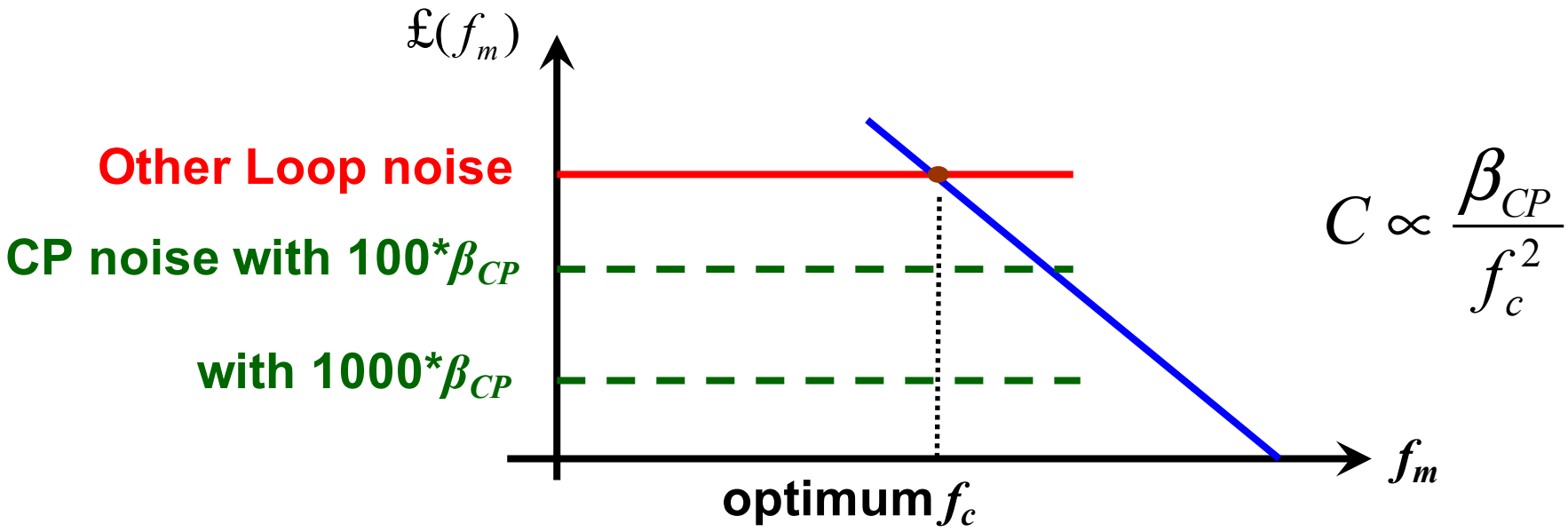
SSPLL Design Challenges

- SSPLL has no divider
  - May lock to any integer N
- SSPD/CP has very Large β_{CP}
  - May need Big Cap for stabilization



- For given phase margin and K_{VCO}: $C \propto \frac{\beta_{CP}}{f_c^2}$

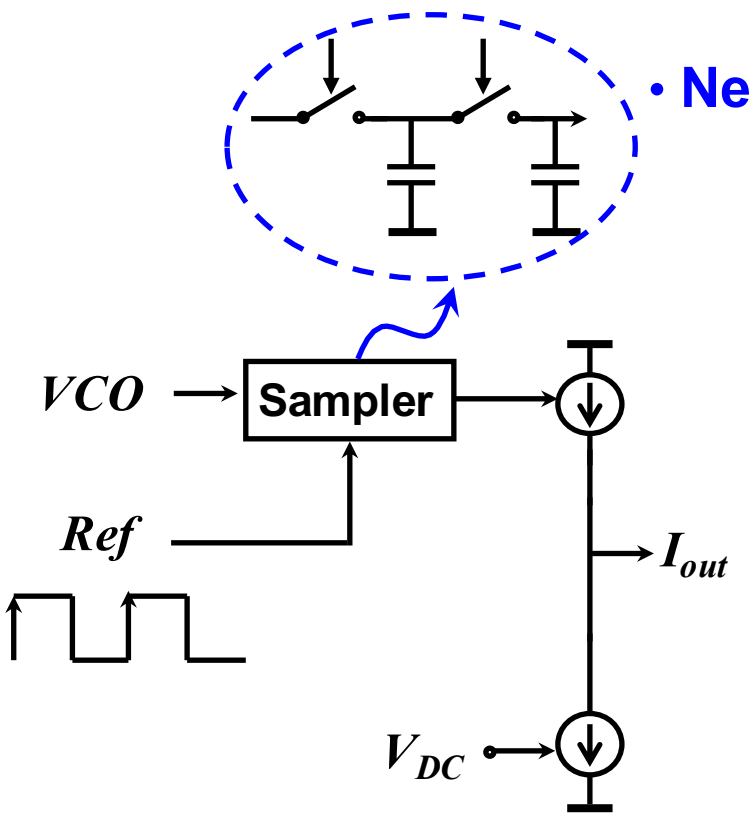
β_{CP} and Filter Cap Area



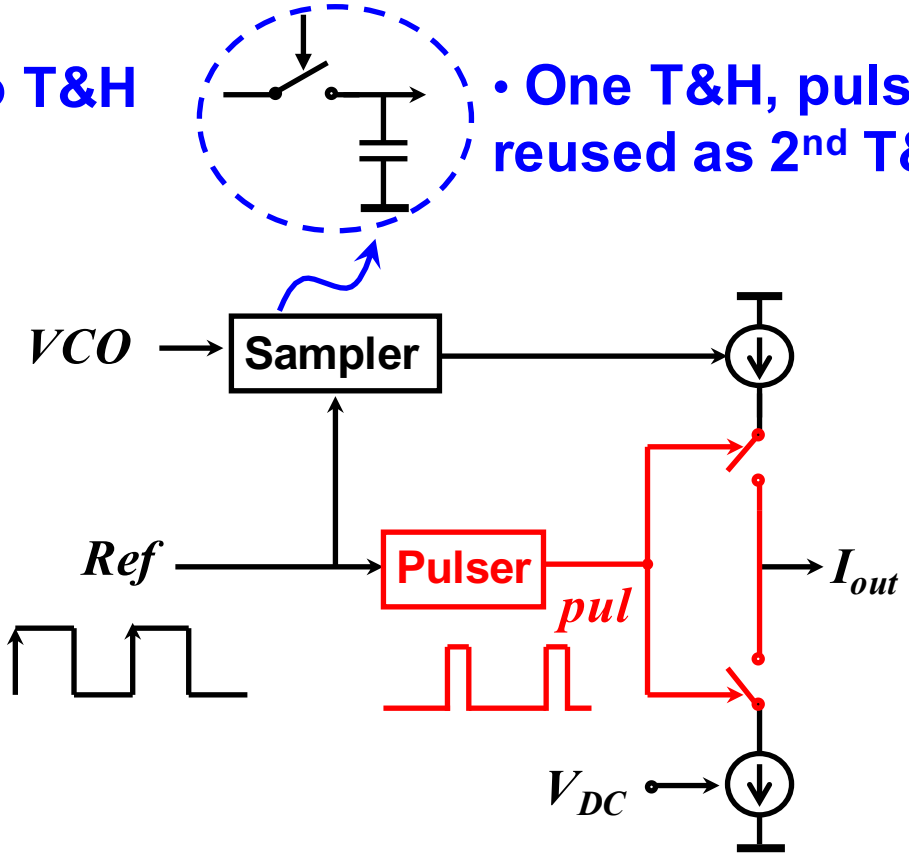
- Once CP noise is negligible, further Larger β_{CP} only wastes chip area (Big Cap)

β_{CP} control is desired for full integration

SSPD/CP with Gain Control



• Need two T&H

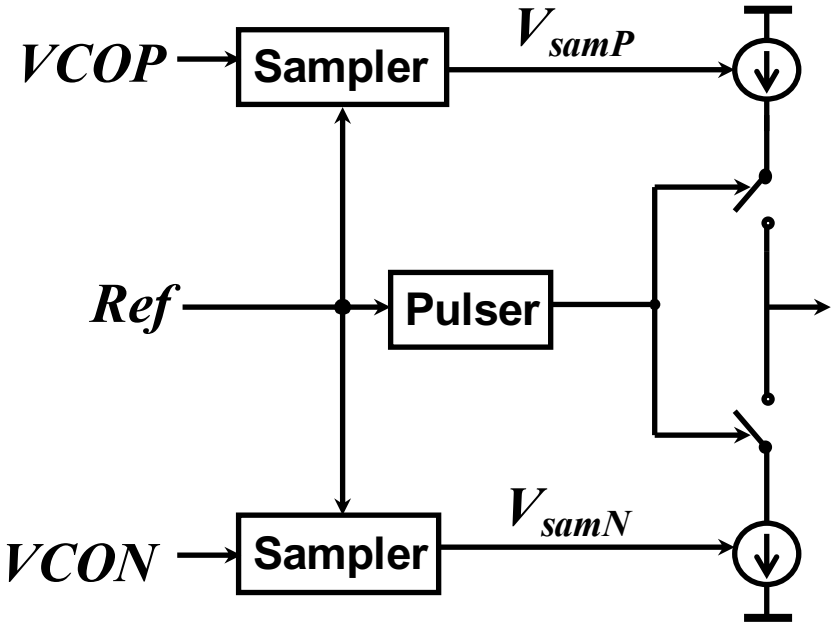


• One T&H, pulser reused as 2nd T&H

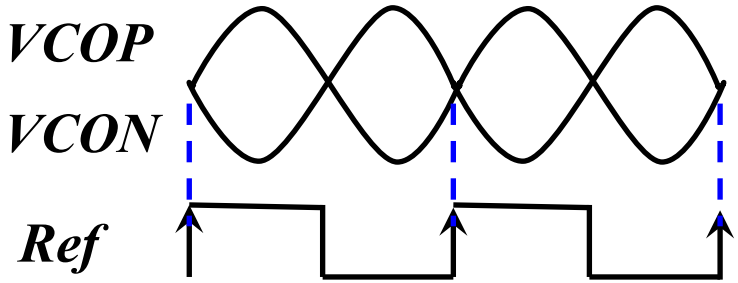
$$\beta_{CP} = A_{VCO} \cdot g_m \cdot DR_{pul}$$

A proper choice of DR_{pul} reduces Cap area while still keeps CP noise negligible

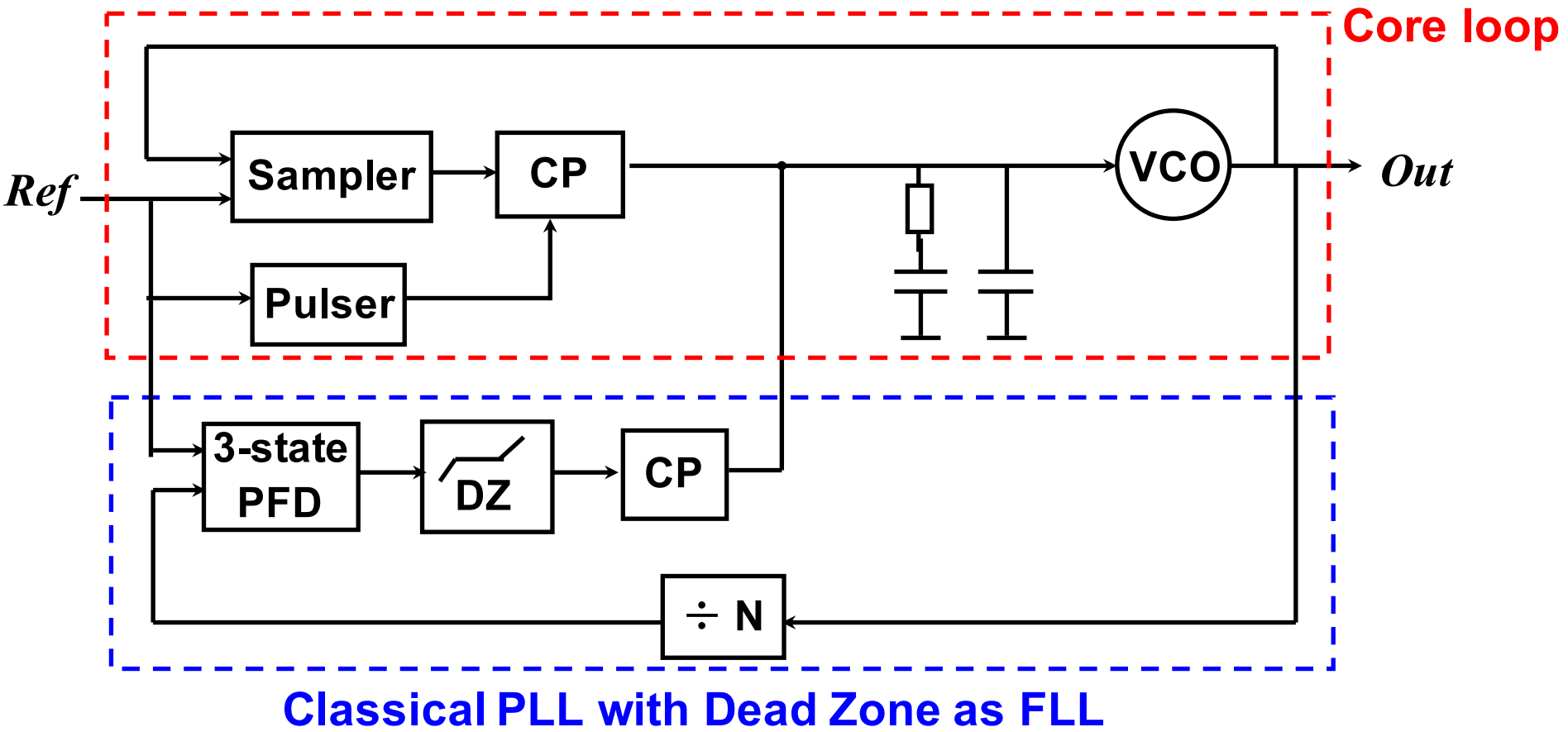
Differential Sampling



- Cancels clock feed-through & charge injection
- VCO crossing (most linear point) is locking point



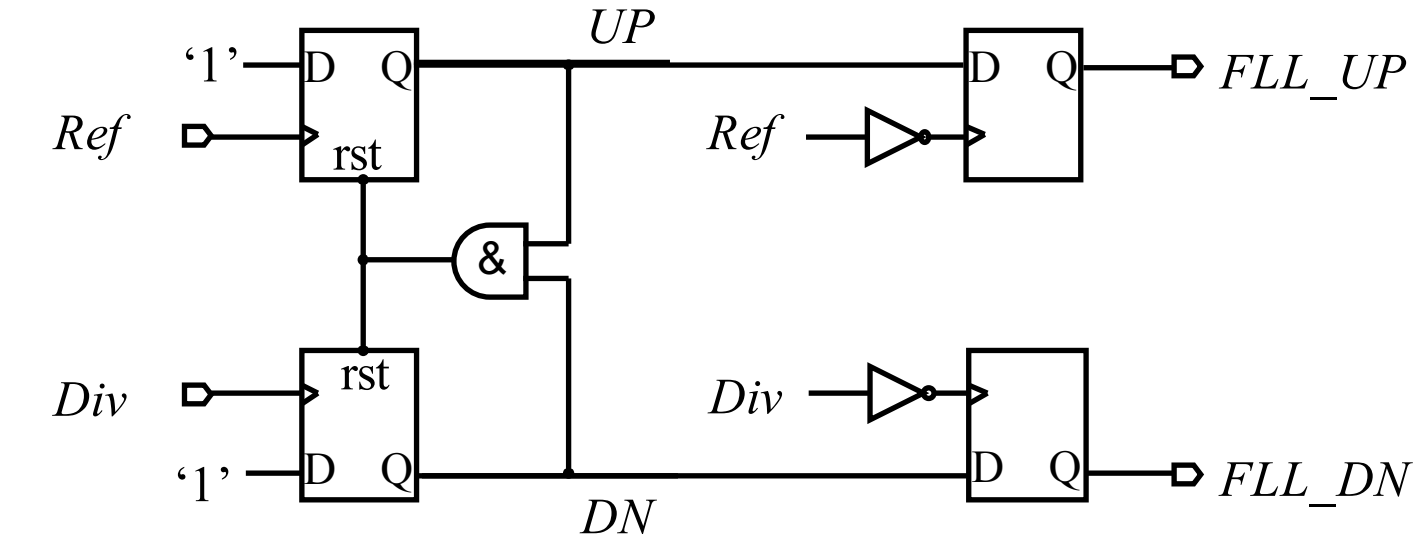
SSPLL With Frequency Locking Loop

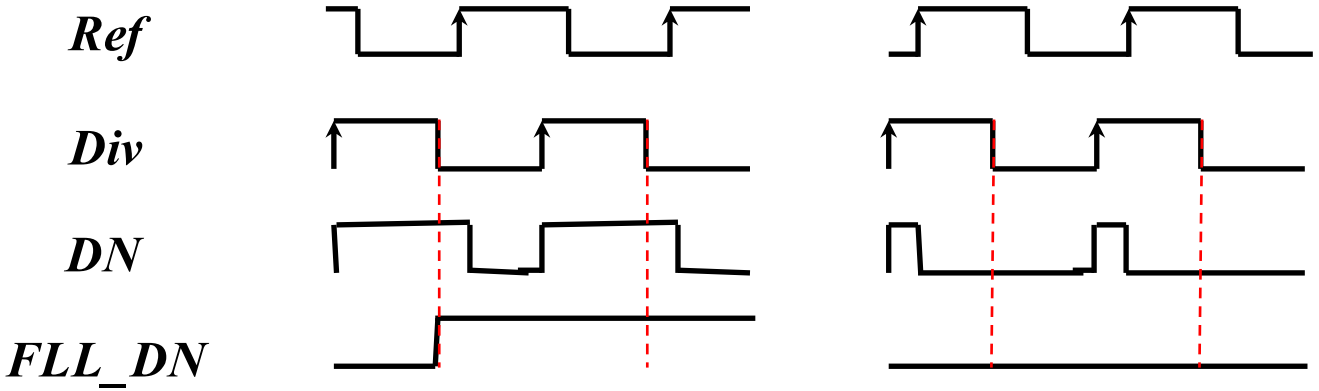


Classical PLL with Dead Zone as FLL

- During locking, ΔΦ > DZ, FLL has large gain, brings loop to lock
- Close to locking, ΔΦ < DZ, FLL has zero gain, not injecting noise
- FLL can also be disabled after locking to save power

Dead Zone Creator Example



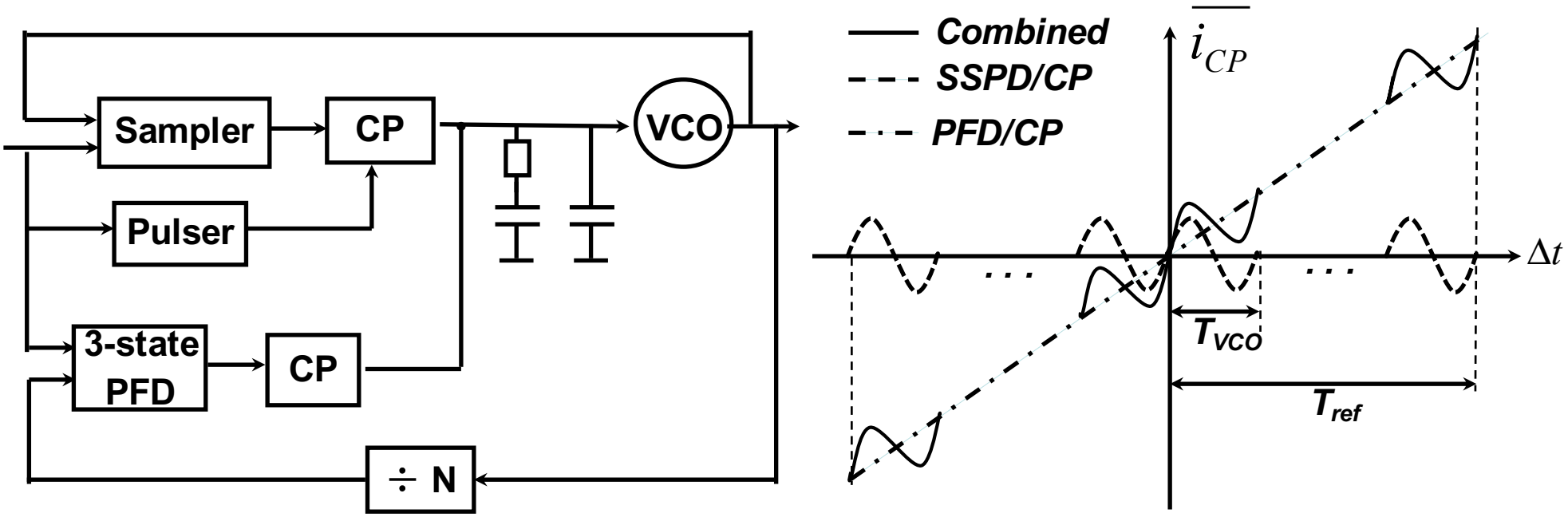


• Large phase error

• Small phase error

■ With 50% *Ref* and *Div* duty ratio, Dead zone is (-π, +π)

It Also Works Without Dead Zone



- FLL keeps running, more robust against disturbances
- Overall characteristic SSPD/CP and PFD/CP combined
- FLL PFD/CP injects noise but is attenuated by $(\beta_{CP,SS}+\beta_{CP,PFD})^2$

[3] C.-W. Hsu, K. Tripurari, S.-A. Yu and P. R. Kinget, "A Sub-Sampling-Assisted Phase-Frequency Detector for Low-Noise PLLs With Robust Operation Under Supply Interference," IEEE Trans. Circuits Syst. I, vol.62, no.1, pp.90-99, Jan. 2015.

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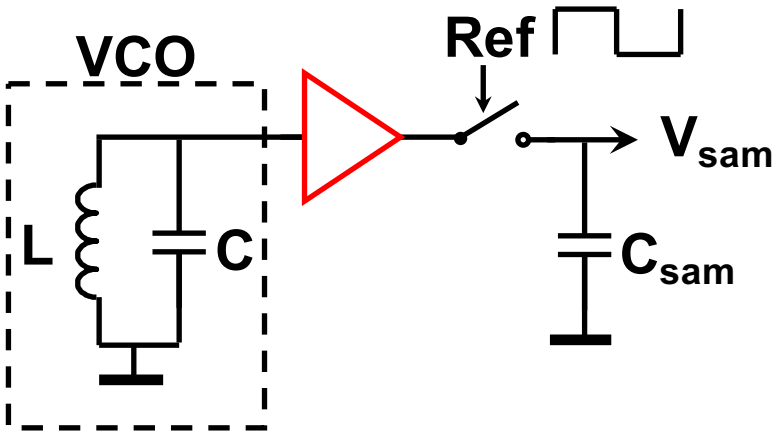
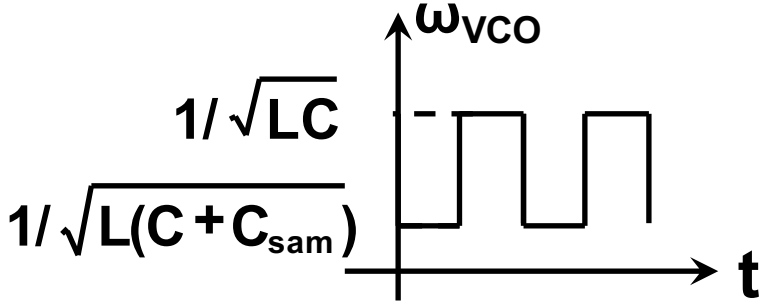
VCO-Sampler Buffer

- VCO buffer is power consuming, can we remove it?



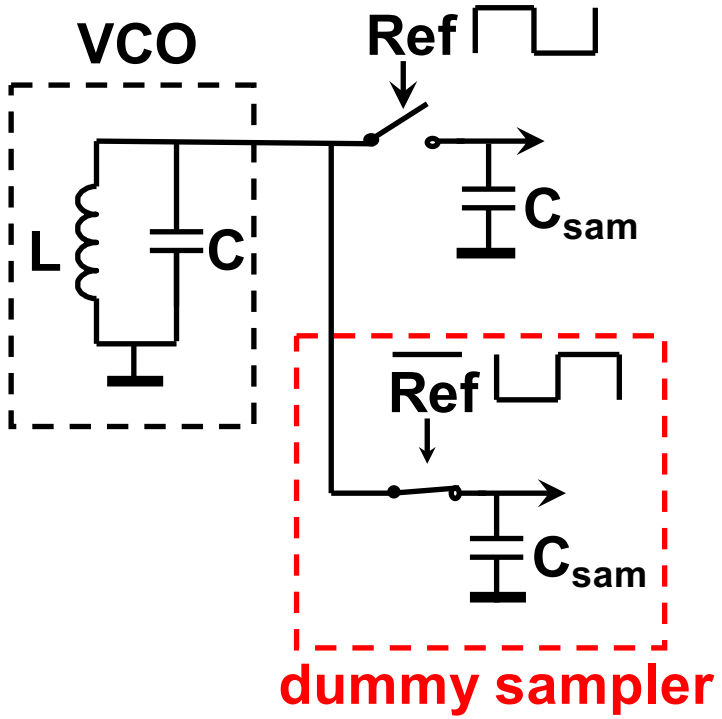


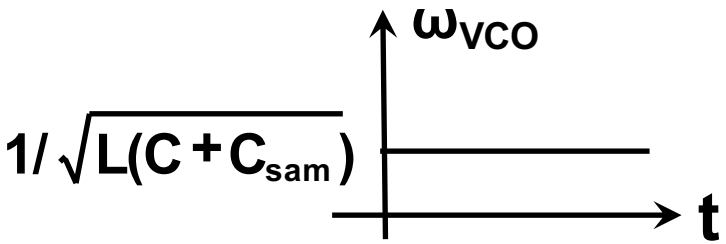
- VCO load and f_{VCO} changes, BFSK effect causes spur

$$SP = 20\log[\sin(\pi \cdot D_{ref}) \cdot \frac{N}{2\pi} \cdot \frac{C_{sam}}{C}]$$

Direct Sampling with Dummy Sampler

■ **Complementary switched dummy sampler**

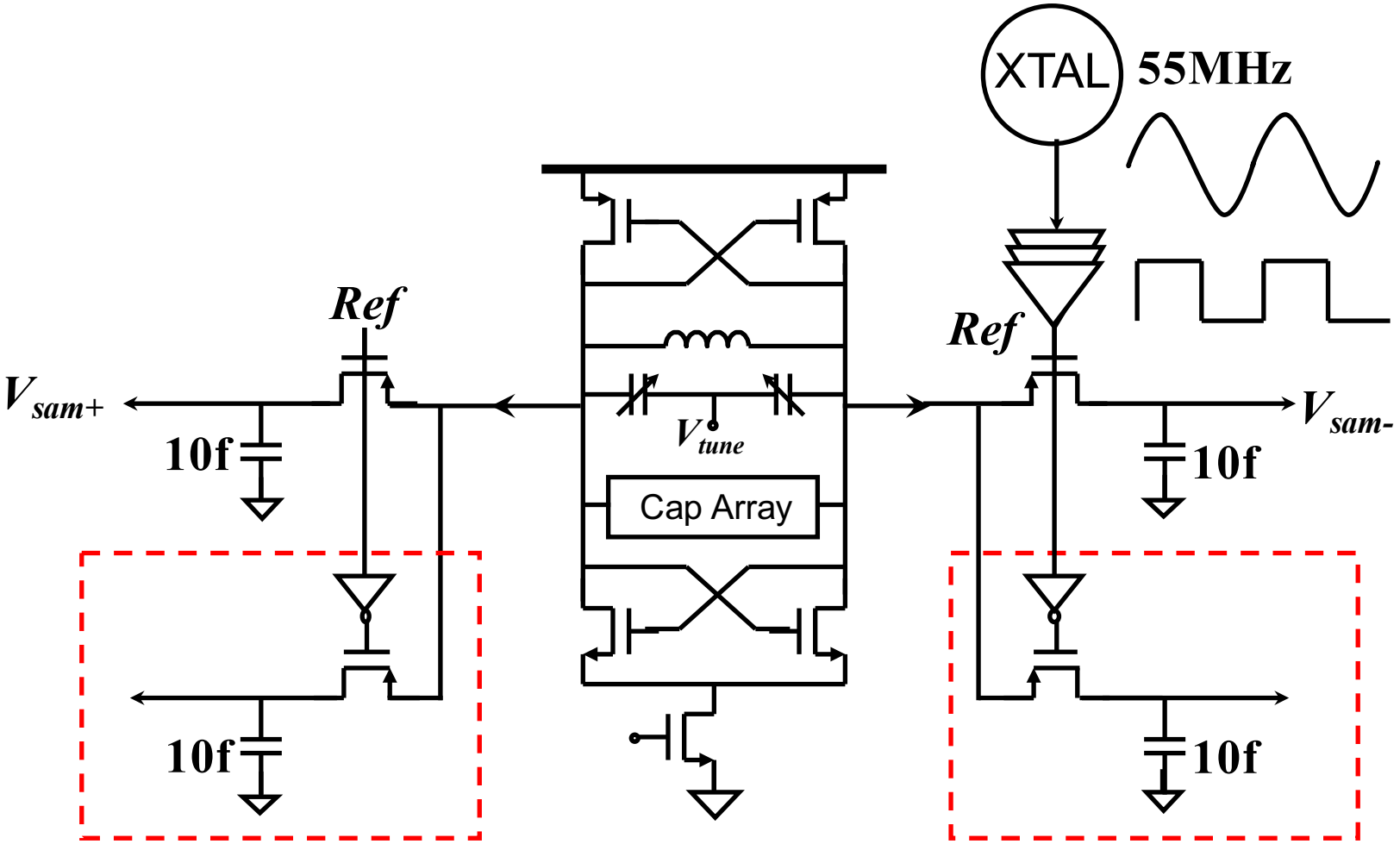




- Spur due to BFSK effect with mismatch

$$SP = 20\log[\sin(\pi \cdot D_{ref}) \cdot \frac{N}{2\pi} \cdot \frac{A_C\sqrt{2C_{sam}}}{C}]$$

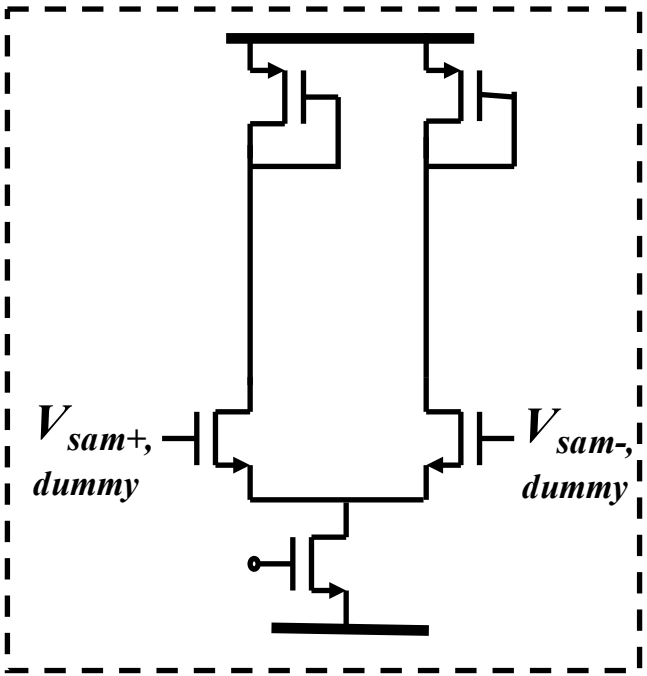
Direct VCO Sampling Design Example



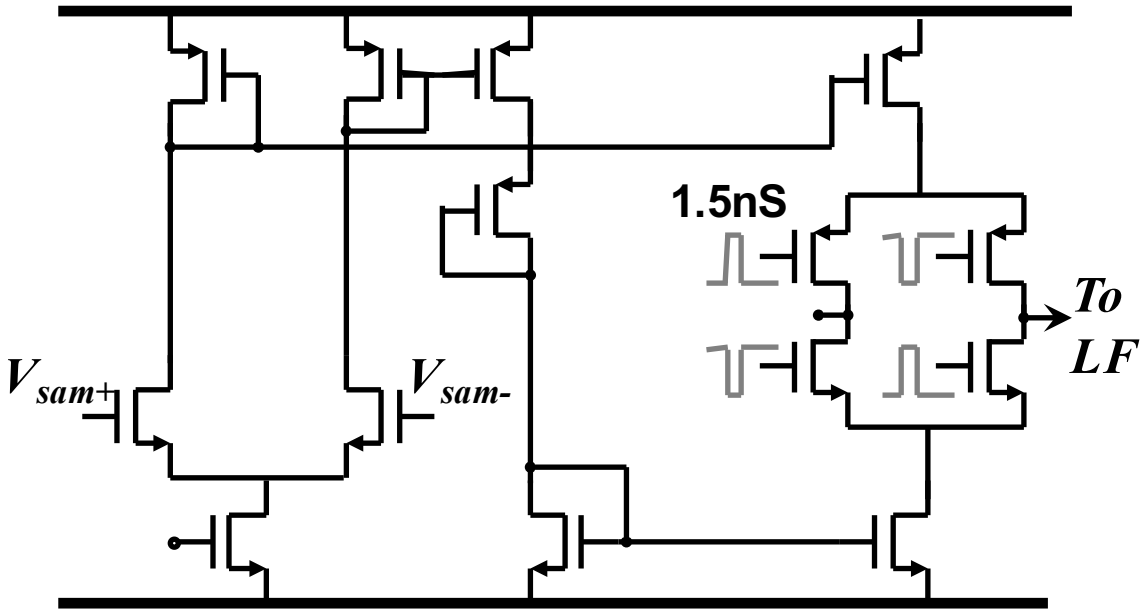
dummy sampler

[4] X. Gao, E. Klumperink, G. Socci, M. Bohsali and B. Nauta, "A 2.2GHz Sub-Sampling PLL with 0.16ps$_{rms}$ Jitter and -125dBc/Hz In-band Phase Noise at 700μW Loop-Components Power," *IEEE Symposium on VLSI Circuits*, pp. 139-140, Jun. 2010.

CP Design



dummy CP

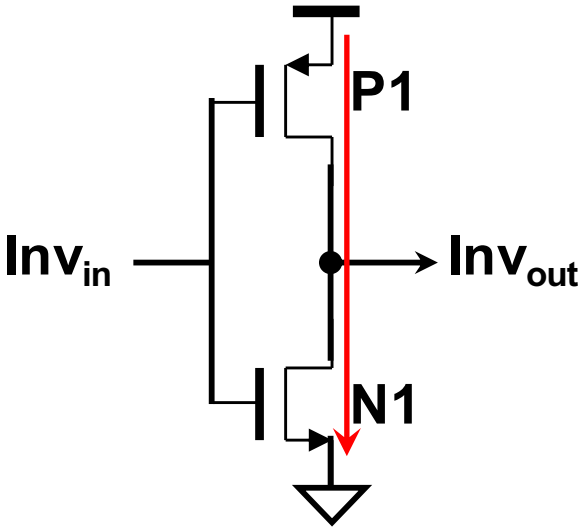


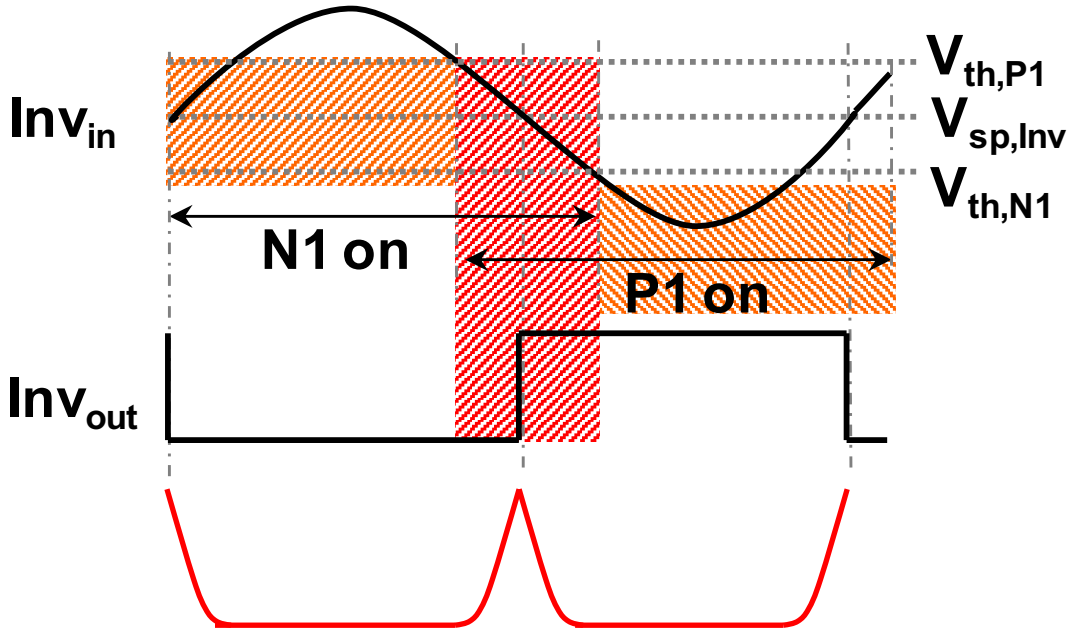
V → I

■ Due to superior CP noise suppression of SSPLL, a small I_{CP} of 30μA is enough to achieve very low phase noise

Inverter Ref Buffer

- XTAL outputs sine-wave, SSPD needs square-wave Ref



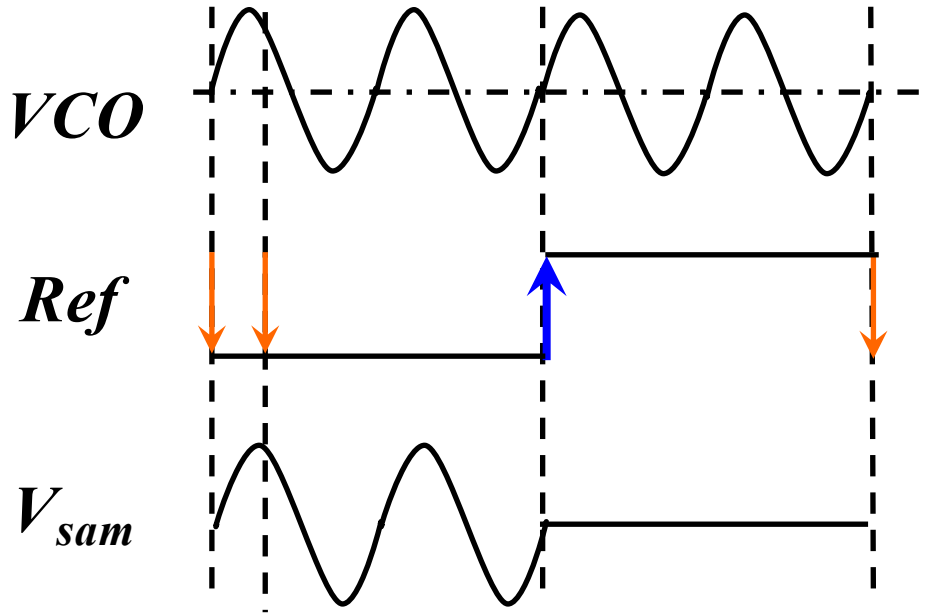


- Big size for low Ref noise
- Slow sine-wave input, N1 and P1 both on for long time
- Short-circuit current could be >90% of inverter power

- With so little I_{CP} and SSPD virtually consume no power, simple Ref buffer become major loop power dissipater

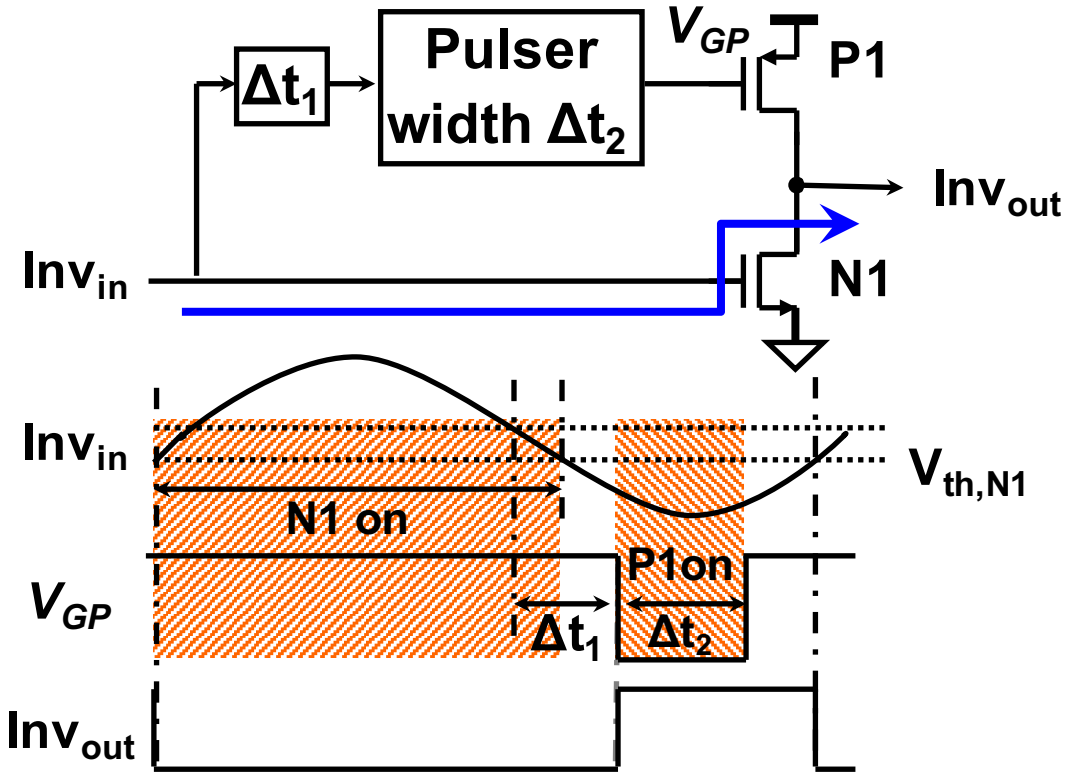
How to Reduce Short-Circuit Current?

- **Practical sampler: track-and-hold**



- Only the sampling edge (SE) is critical for noise
- The tracking edge (TE) can be noisy

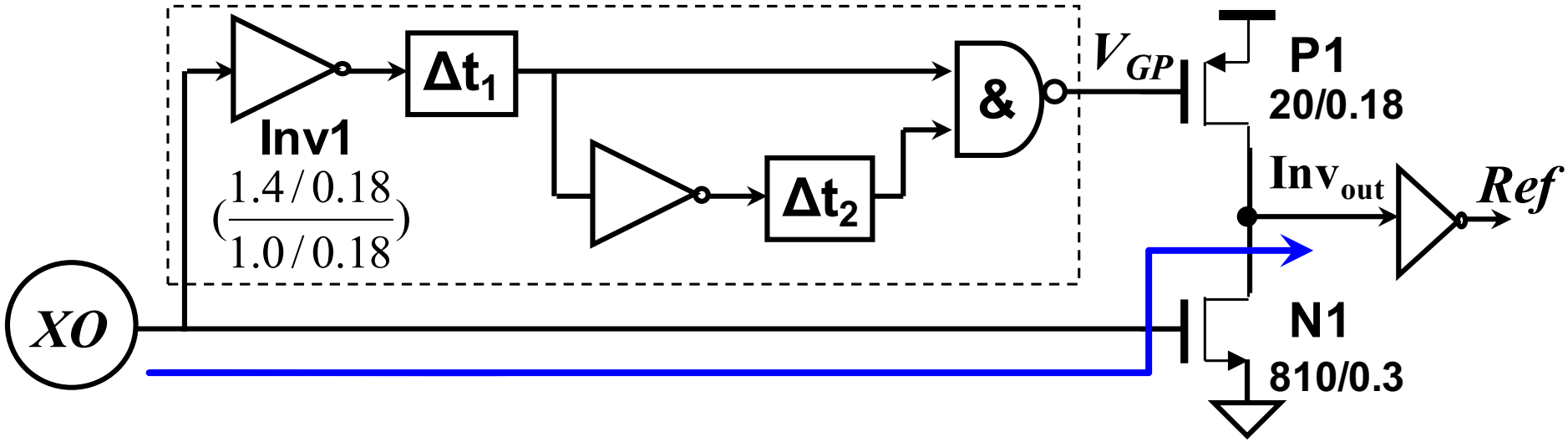
Low Power Sine-to-Square Ref Buffer



- N1 and P1 on-time guaranteed non-overlapping
- Critical path for SE is kept clean and short

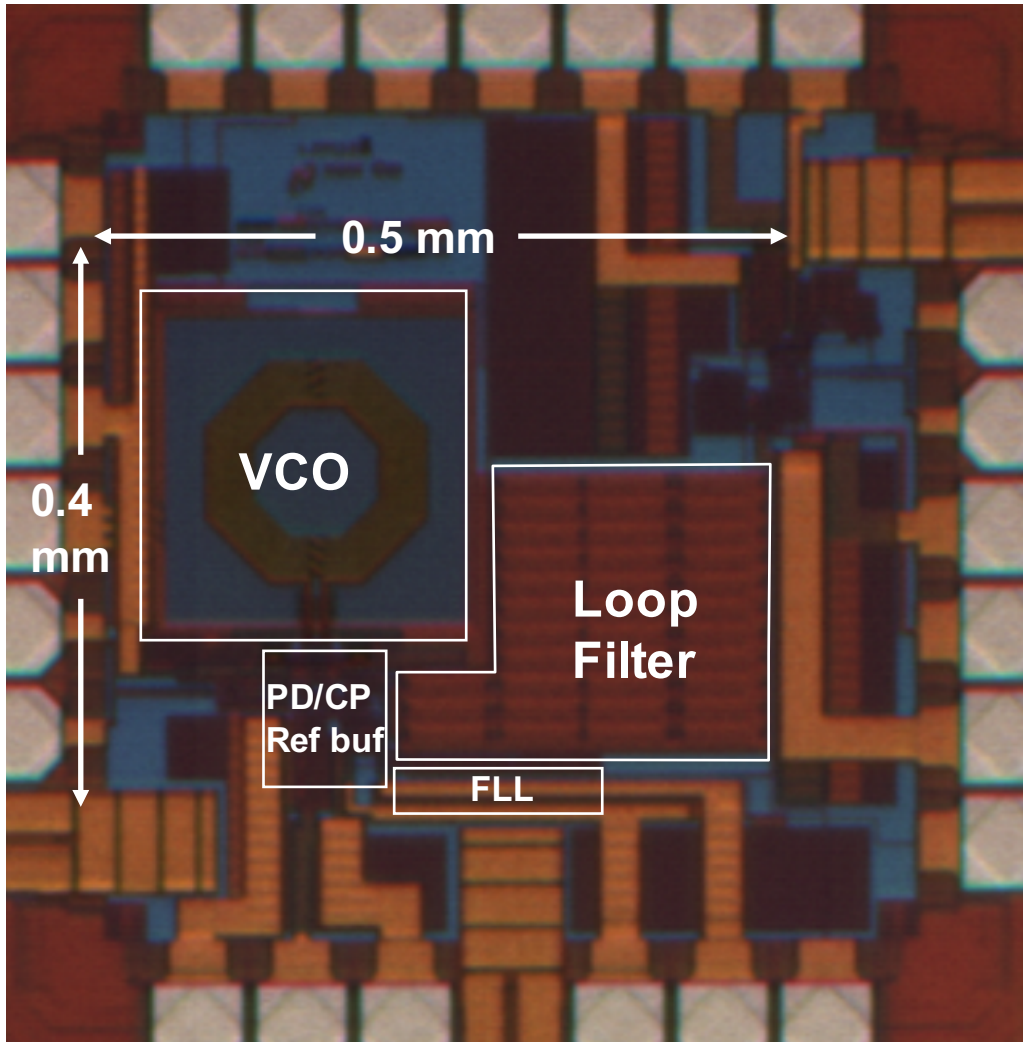
Short-circuit current eliminated

Low Power Ref Buffer Design Example



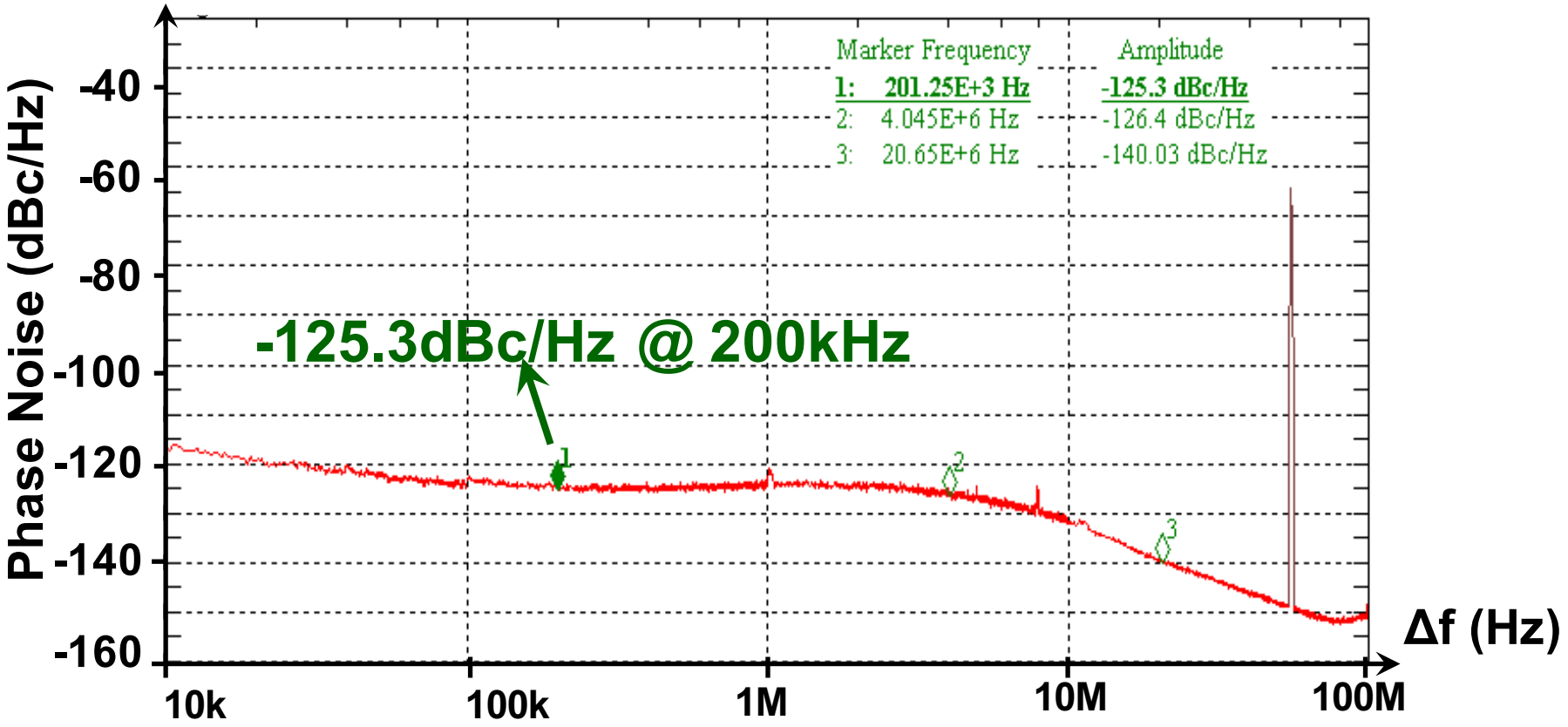
- Delays are implemented with shunt-C inverters
- Transistors in critical path are sized big, others are small to save power
- It draws 0.22mA (would be >2mA for simple inverter)

Die Photograph



- 0.18 μm CMOS
- Active Area: 0.2 mm^2
- 24-pin LLP package
- VDD: 1.8 V
- Power Consumption
  - VCO 1.0 mA
  - Loop 0.4 mA

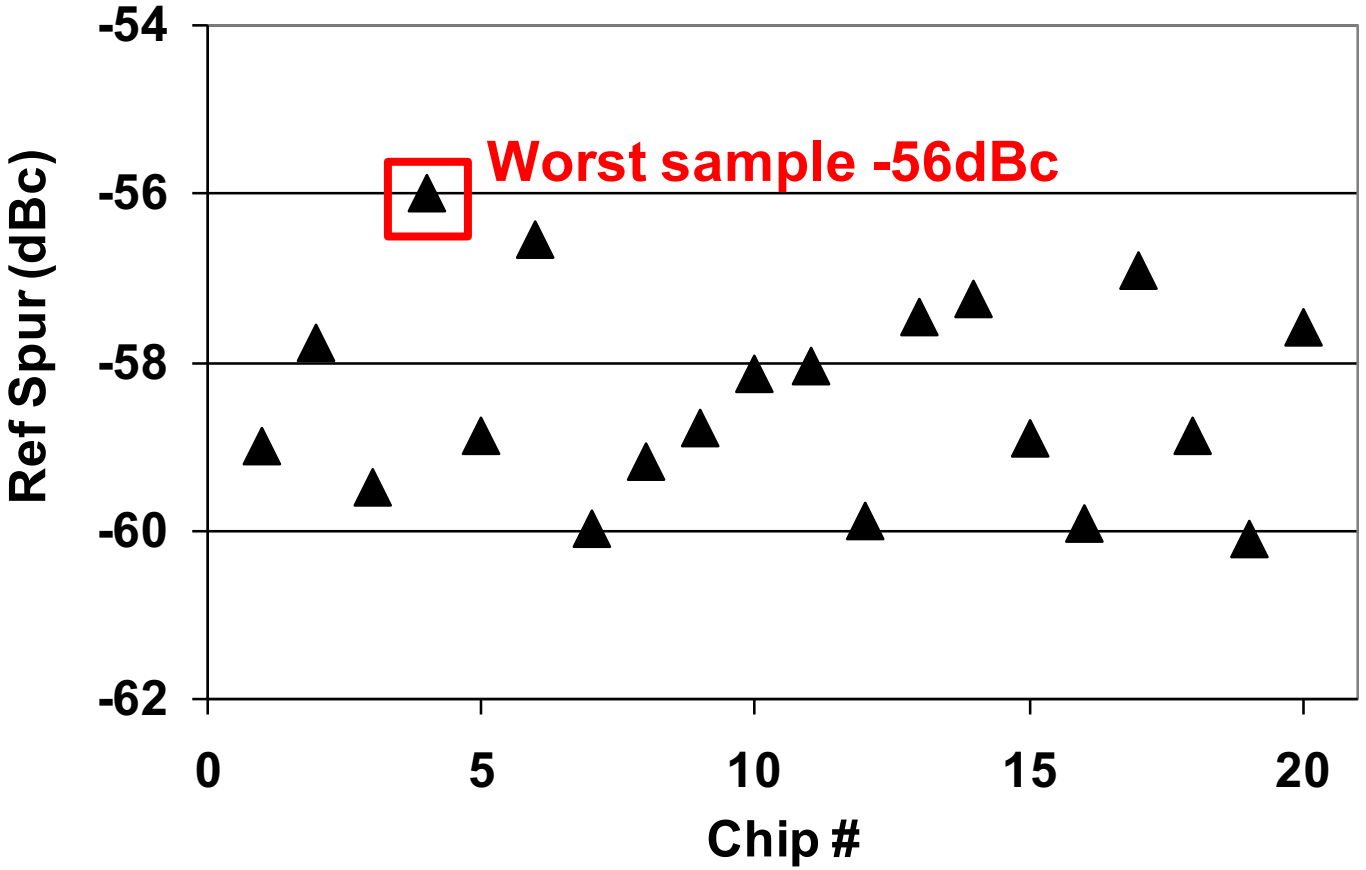
Measured Phase Noise



- 2.2GHz output with 55MHz XTAL
- In band noise -125.3dBc/Hz@200kHz
- Rms jitter 0.16ps [10k, 100M]

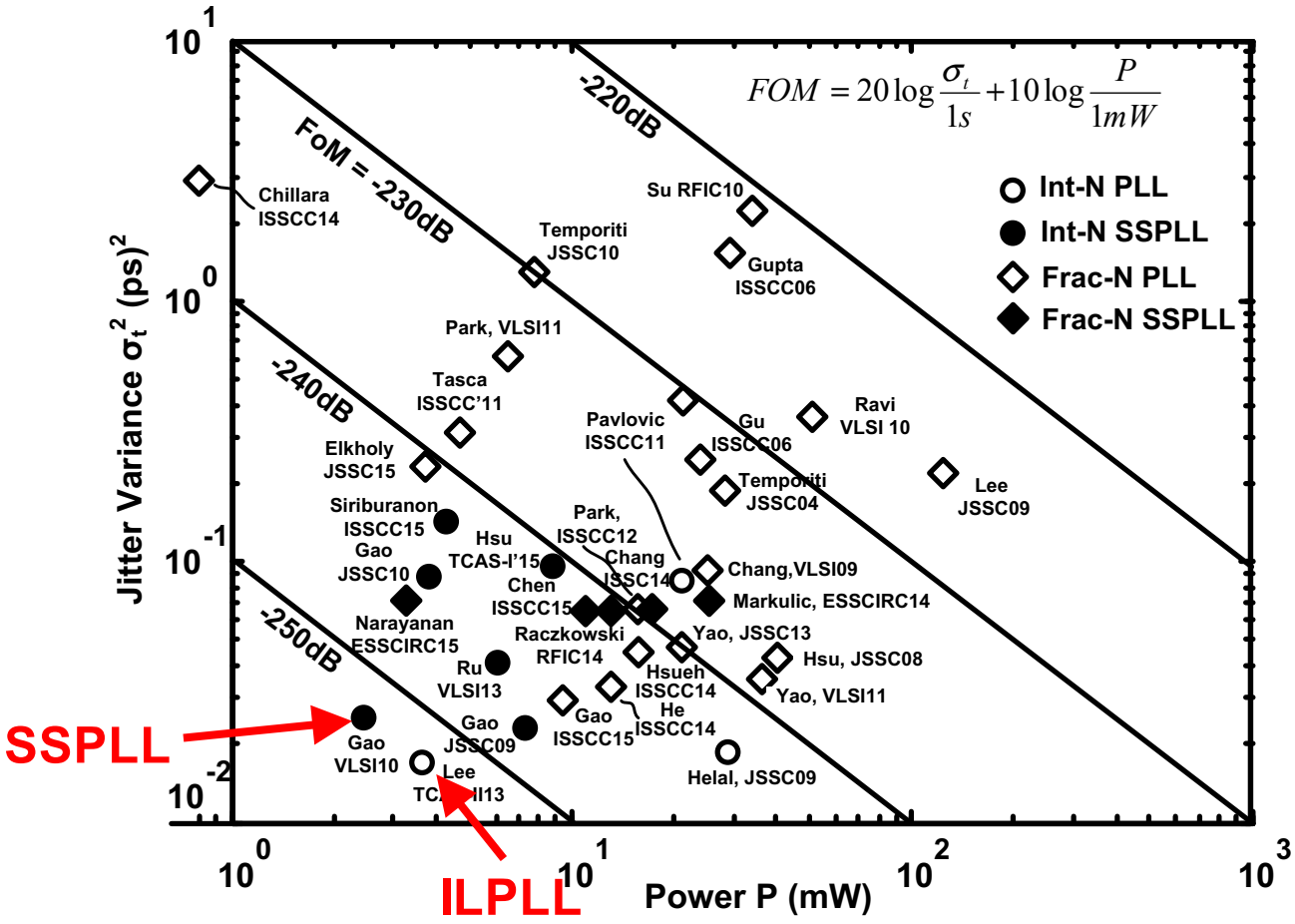
Measured Spur

- Spur from 20 chips from spectrum analyzer



PLL Utopia

- All PLL need Ref buffer. "PLL Utopia": only the Ref path contributes to loop noise and power.
- Both SSPLL and injection locked PLL can approach "Utopia" and they hold the PLL FOM record



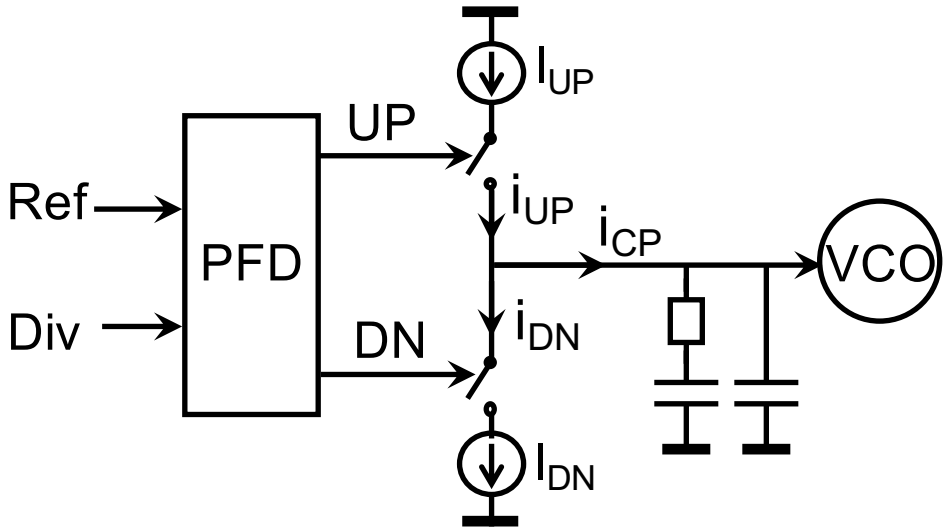
SSPLL vs ILPLL

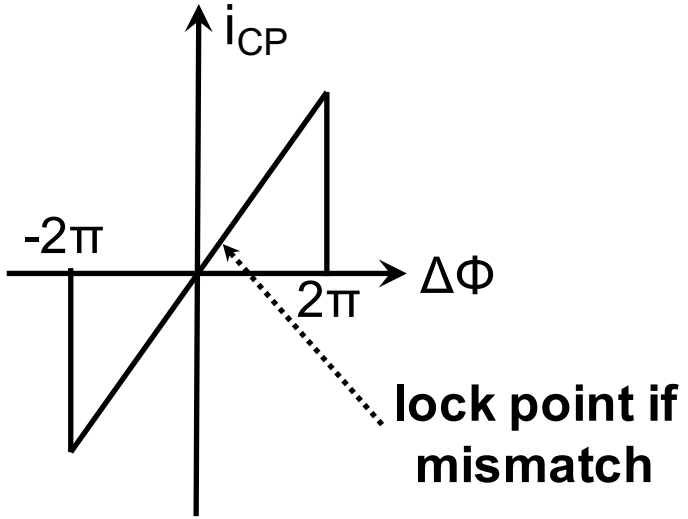
- SSPLL is more like a traditional PLL with a phase detector and a feedback loop
  - More robust bandwidth/loop-dynamic control
  - Lower reference spur
- ILPLL can achieve larger filtering bandwidth for VCO noise and can be beneficial e.g. when ring oscillator is used

Outline

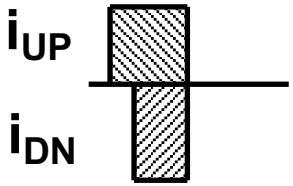
- Classical CP PLL and PLL FOM
- Sub-Sampling(SS) PLL
- SSPLL Power Reduction Techniques
- **SSPLL Spur Reduction Techniques**
- Recent SSPLL Development and Discussion

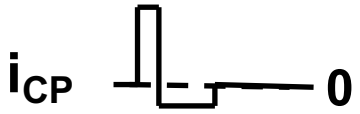
Classical CP





- **UP/DN constant amplitude, variable on-time**
  - **Amplitude mismatch → UP or DN on-time mismatch→ CP ripple**

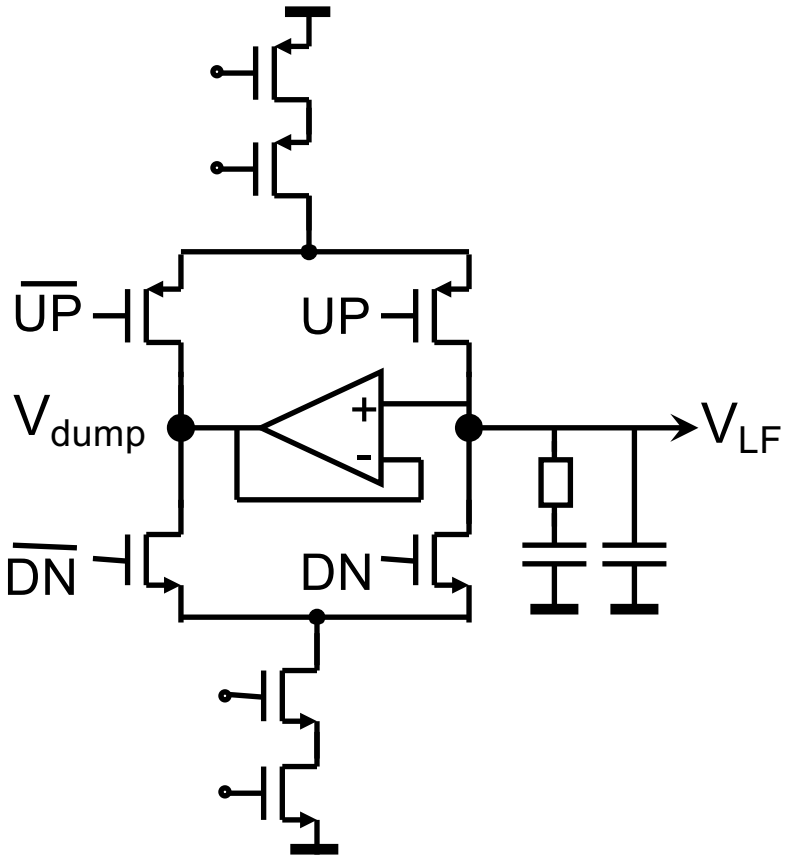




- **VCO Ref spur by CP ripple** $\propto i_{CP,\,fref} \cdot \left(\frac{f_{BW}}{f_{ref}}\right)^2$

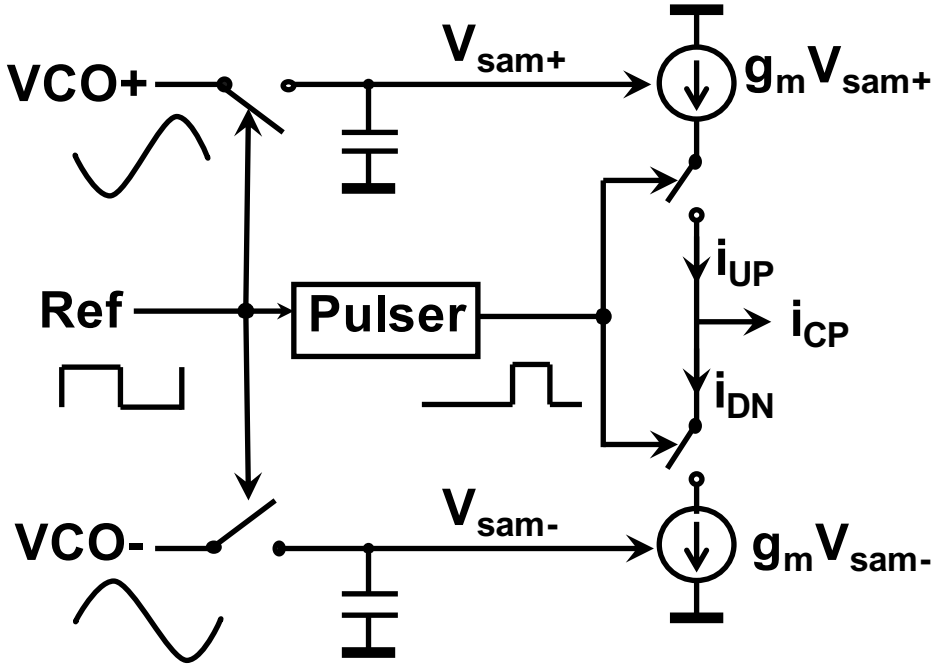
Sensitive to mismatch, low spur high BW tradeoff

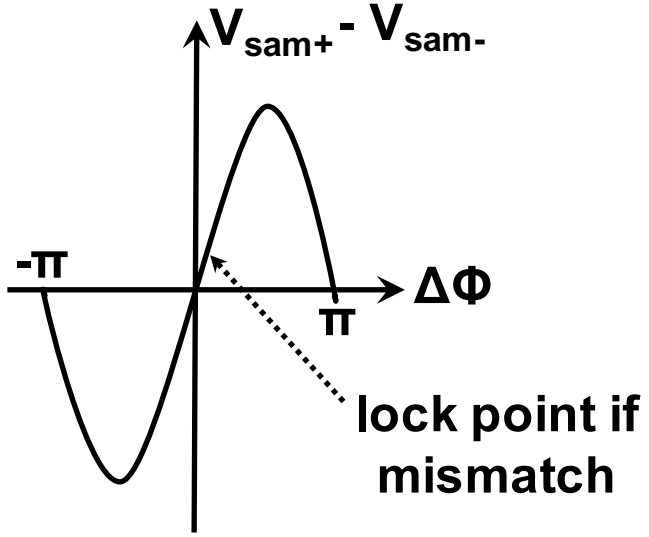
Classical Low Ripple CP Design



- Cascode transistors for high impedance, better matching
- Current steering, UGB for $V_{dump}=V_{LF}$ to keep node voltages

CP in SSPLL

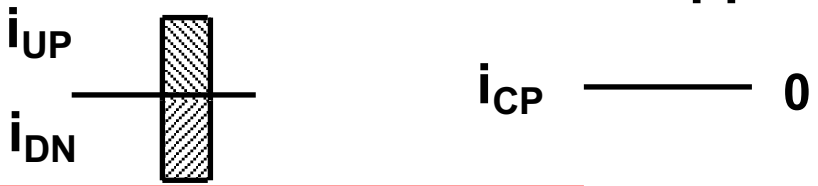




- Pulser is 2nd T&H and controls CP gain

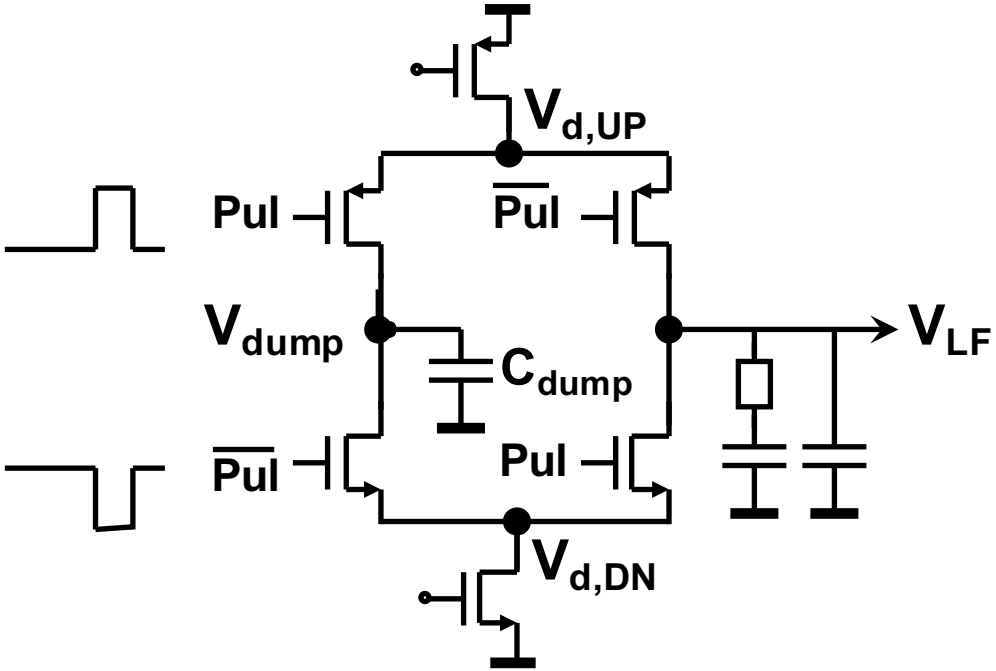
■ **UP/DN constant on-time, variable amplitude**

- Amplitude mismatch → UP/DN still same on-time → no ripple



UP/DN amplitude mismatch eliminated

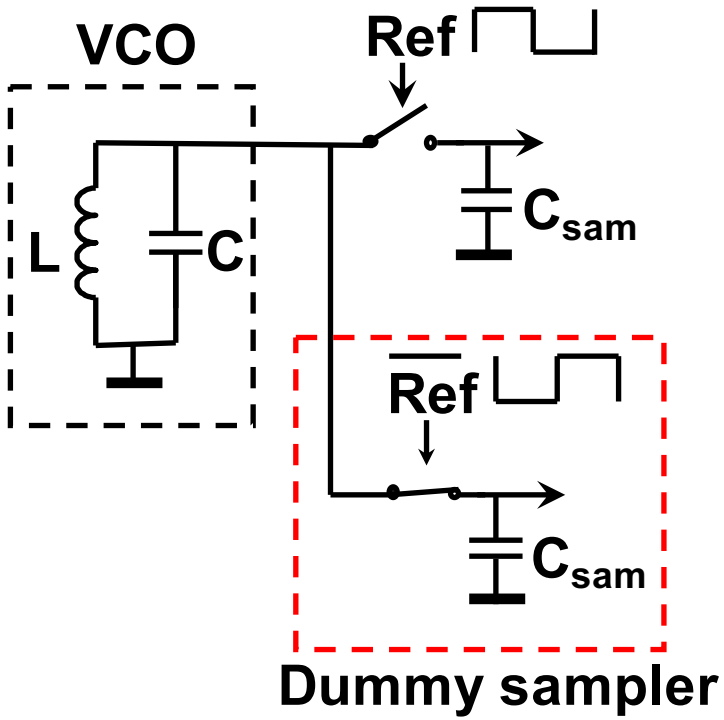
Simple Low Ripple CP Design



- No amplitude mismatch, single transistor enough
- Achieves $V_{dump}=V_{LF}$ without using UGB
  - Steer to filter: $I_{UP}=I_{DN}$ at $V_{d,UP}=V_{d,DN}=V_{LF}$
  - Steer to C_{dump}: $I_{UP}=I_{DN}$ at $V_{d,UP}=V_{d,DN}=V_{dump}$

  $\Longrightarrow$ Due to finite output impedance, $V_{dump}=V_{LF}$

SSPD Also Induces Spur



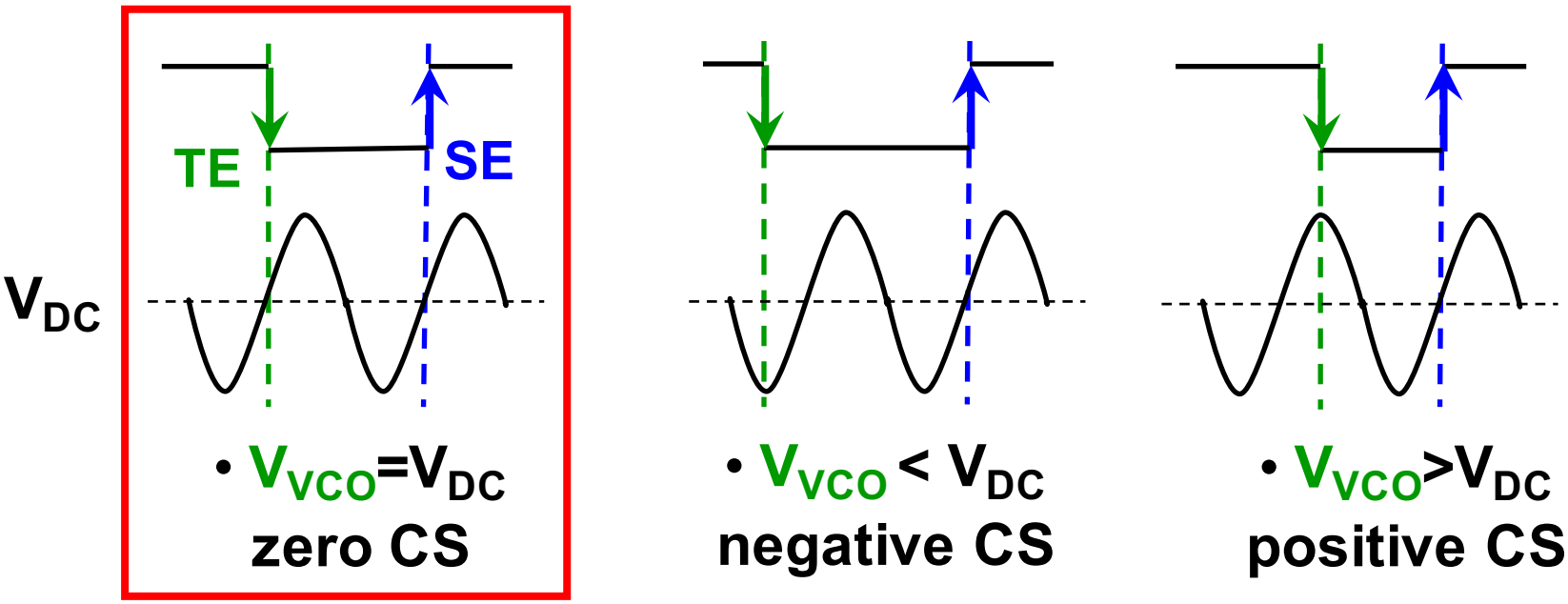
compensated

1. VCO load and f_{VCO} changes, BFSK
2. Charge injection from switch to VCO

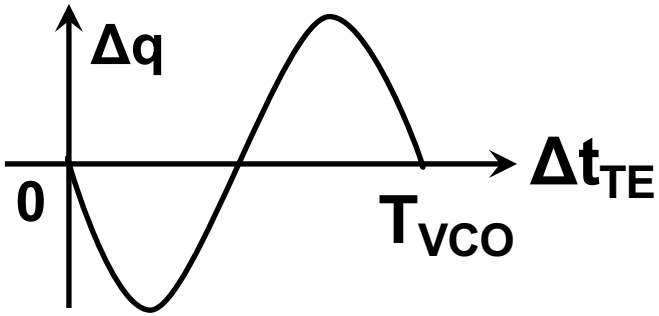
3. Charge Sharing between C_{sam} and VCO

- All spur mechanisms doesn't go through loop filtering, so no spur/BW tradeoff
- Complementary sampling helps but not enough

VCO/Csam Charge Sharing



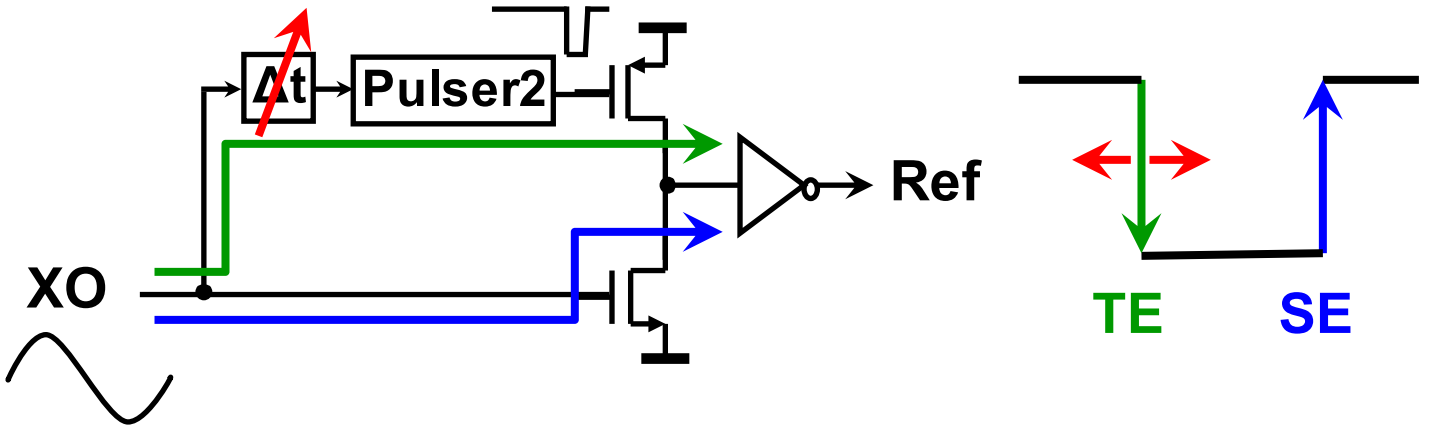
■ Δq depends on Tracking Edge (TE) timing, has sign



No charge sharing by aligning TE to VCO zero-crossing

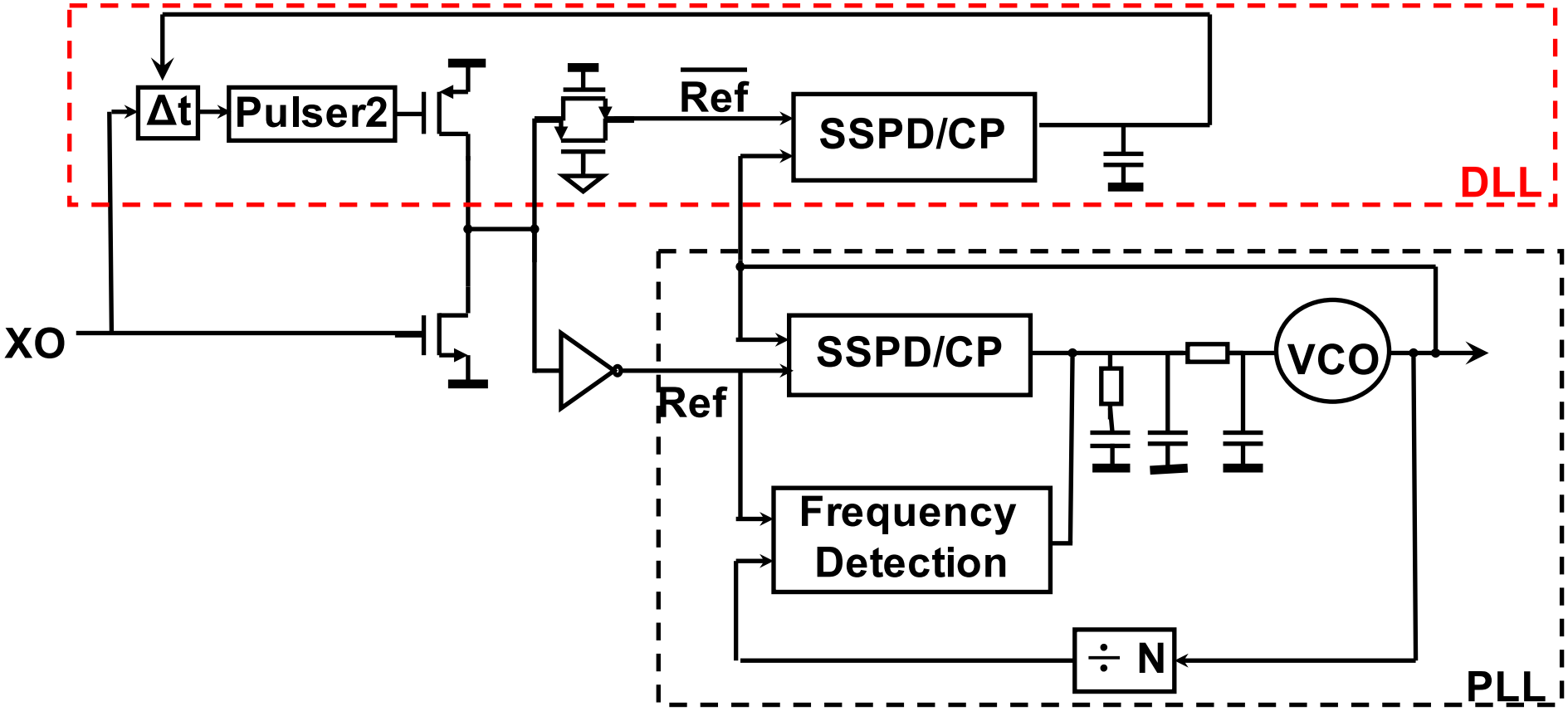
Align Ref TE and VCO

- **Phase detector for Ref TE**
  - Use dummy sampler as it samples VCO with Ref TE
- **Ref TE tuning scheme**



  - Separate gate control for TE/SE
  - Critical SE path kept short and un-affected
  - No short circuit current if N/PMOS on time non-overlap

Low Spur SSPLL Architecture



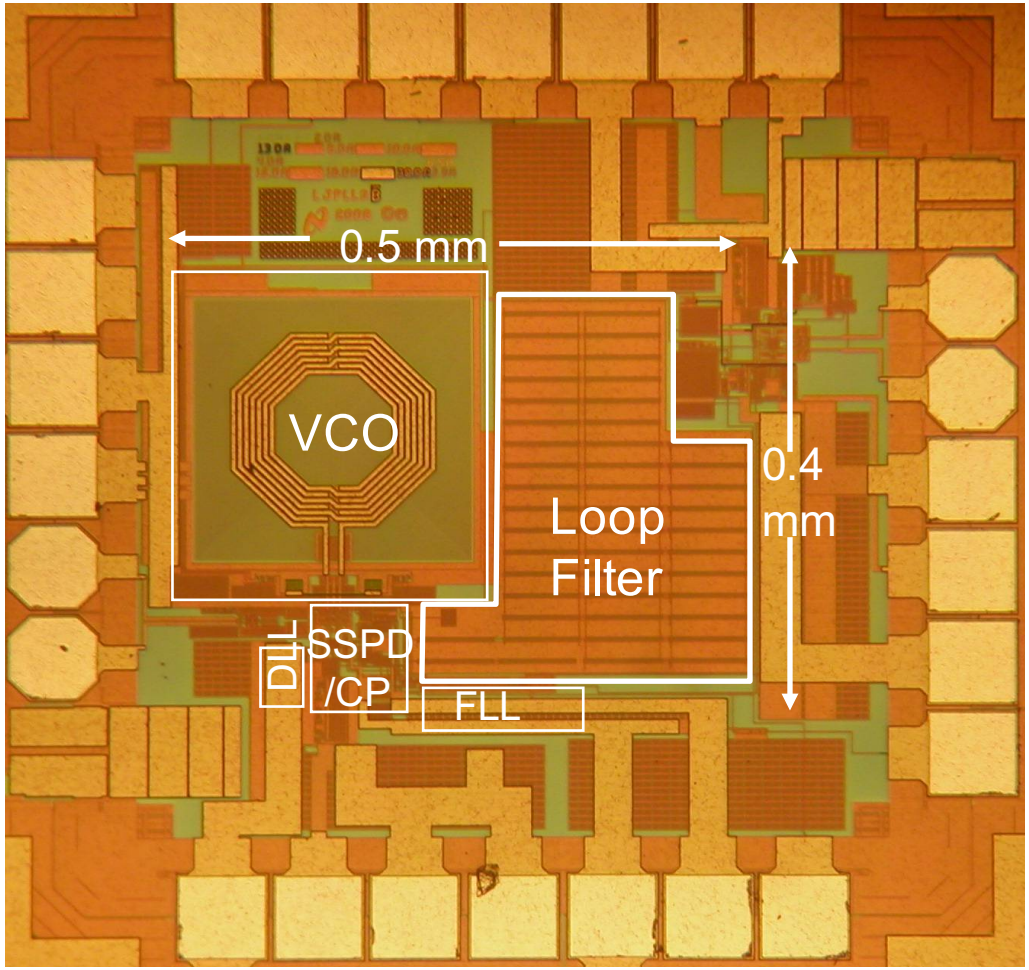
1. BFSK
2. Charge injection

} compensated by dummy

3. Charge sharing → minimized by DLL tuning

■ VCO buffer can be used for even lower spur (power penalty)

Die Photograph

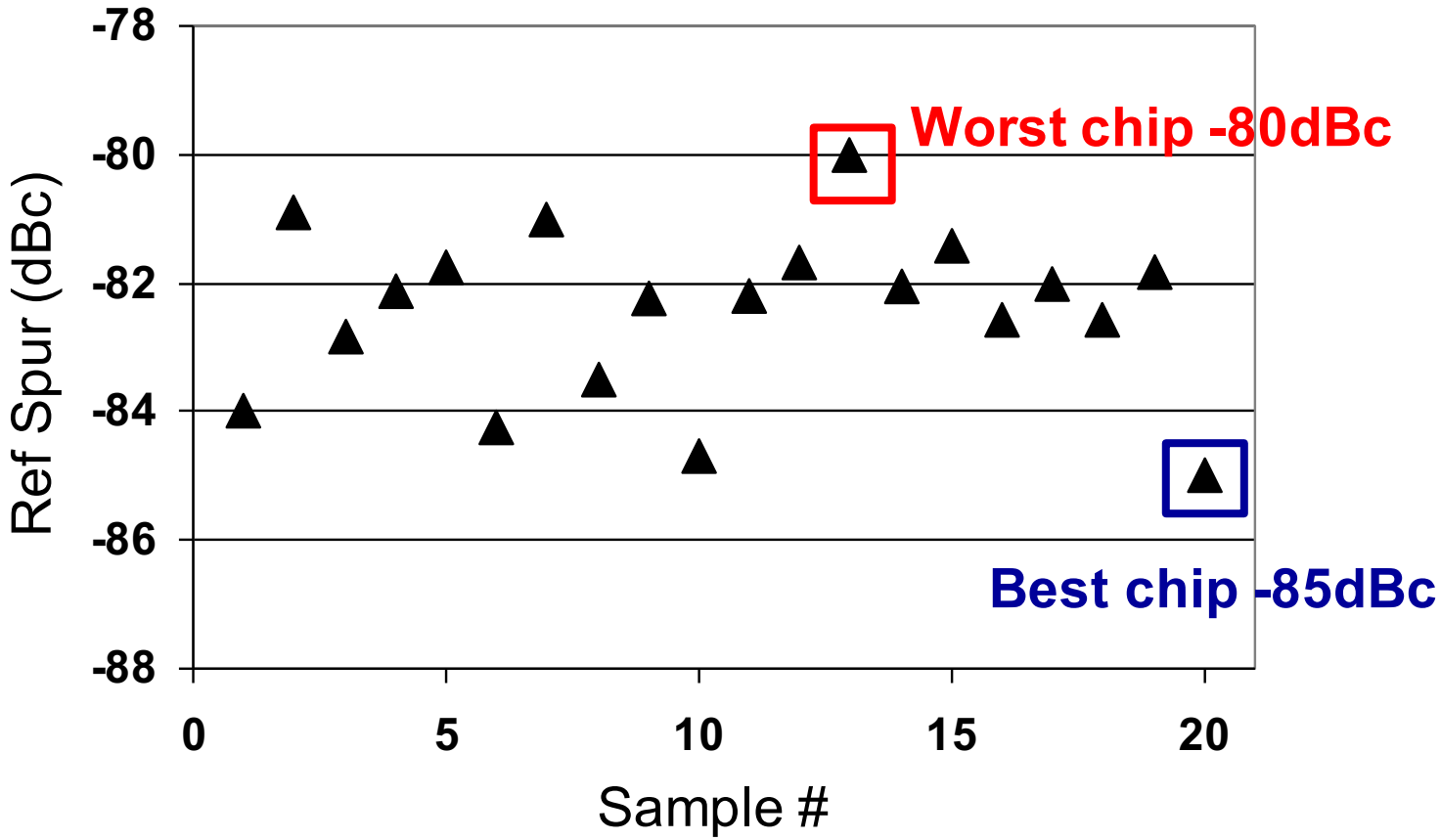


- 0.18um CMOS
- Active Area: 0.2mm^2
- 24-pin LLP package
- VDD: 1.8V
- Power Consumption
  - Whole PLL 2.1mA
  - DLL <5%

[5] X. Gao, E. Klumperink, G. Socci, M. Bohsali and B. Nauta, "Spur Reduction Techniques for Phase-Locked Loops Exploiting a Sub-Sampling Phase Detector," *IEEE J. Solid-State Circuits,* vol. 45, no.9, pp. 1809-1821, Sept. 2010.

Spur Statistics

- Spur from 20 chips with a large f_{BW}/f_{ref} =1/20



Outline

- Classical CP PLL and PLL FOM
- Sub-Sampling(SS) PLL
- SSPLL Power Reduction Techniques
- SSPLL Spur Reduction Techniques
- **Recent SSPLL Development and Discussion**

SSPLL Generalized

■ The sampled waveform does not need to be sine-wave. The key is high detection gain by sampling high dv/dt slope.

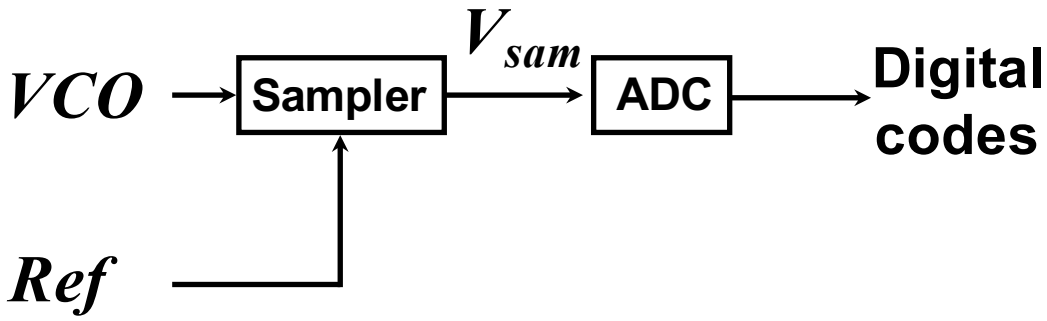
■ It works with any waveform, can also be applied to e.g. ring oscillators [7-8]. Just the phase detection gain need to be generalized:

$$\beta_{SSPD} = \frac{\Delta V_{sam}}{\Delta \phi_{VCO}} = \frac{SR_{sam}}{2\pi f_{VCO}}$$

■ In more advanced process, SSPD can sample faster and utilize steeper slopes, thus benefiting from scaling. SSPLLs working at 10s-of-GHz have been demonstrated [9-10].

Sub-Sampling TDC

■ If we digitize the sampled voltage with an ADC , it will effectively become a time-to-digital converter (TDC)



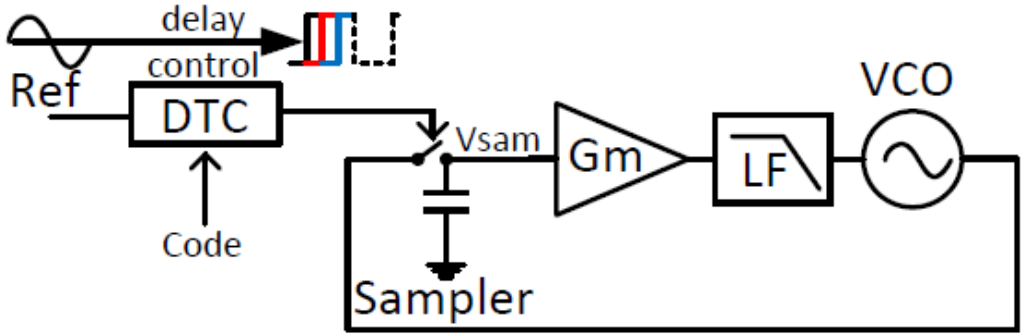
$$\Delta t_{TDC} = \frac{\Delta V_{ADC\,LSB}}{SR_{sam}}$$

e.g. $$= \frac{1mV}{10GV/s} = 0.1ps$$

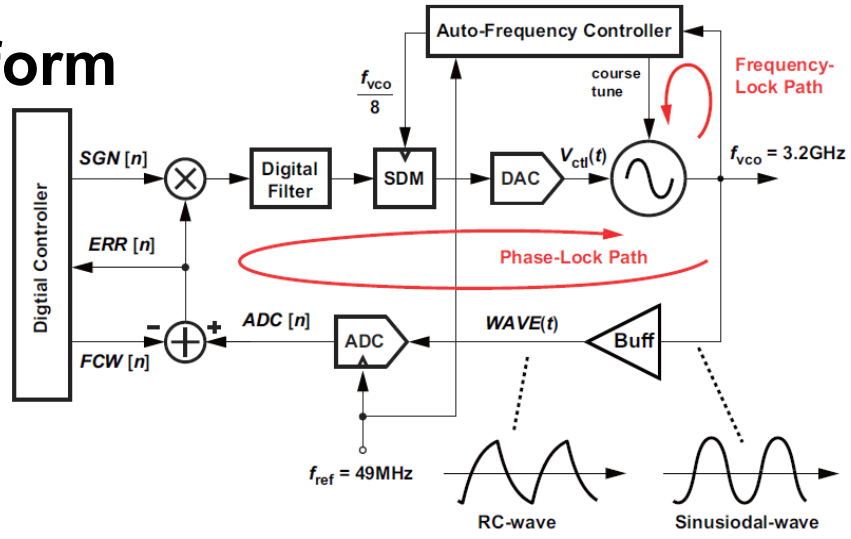
- The resolution is nearly two orders of magnitude finer than gate delay and is easily scalable.
- Can be used to implement digital SSPLLs [14-16]

Extend SSPLL to Fractional-N

- **DTC based frac-N SSPLL [17-19]**
  - Use DTC to modulate Ref edges and realize frac-N operation so SSPD onlv need to handle small phase error

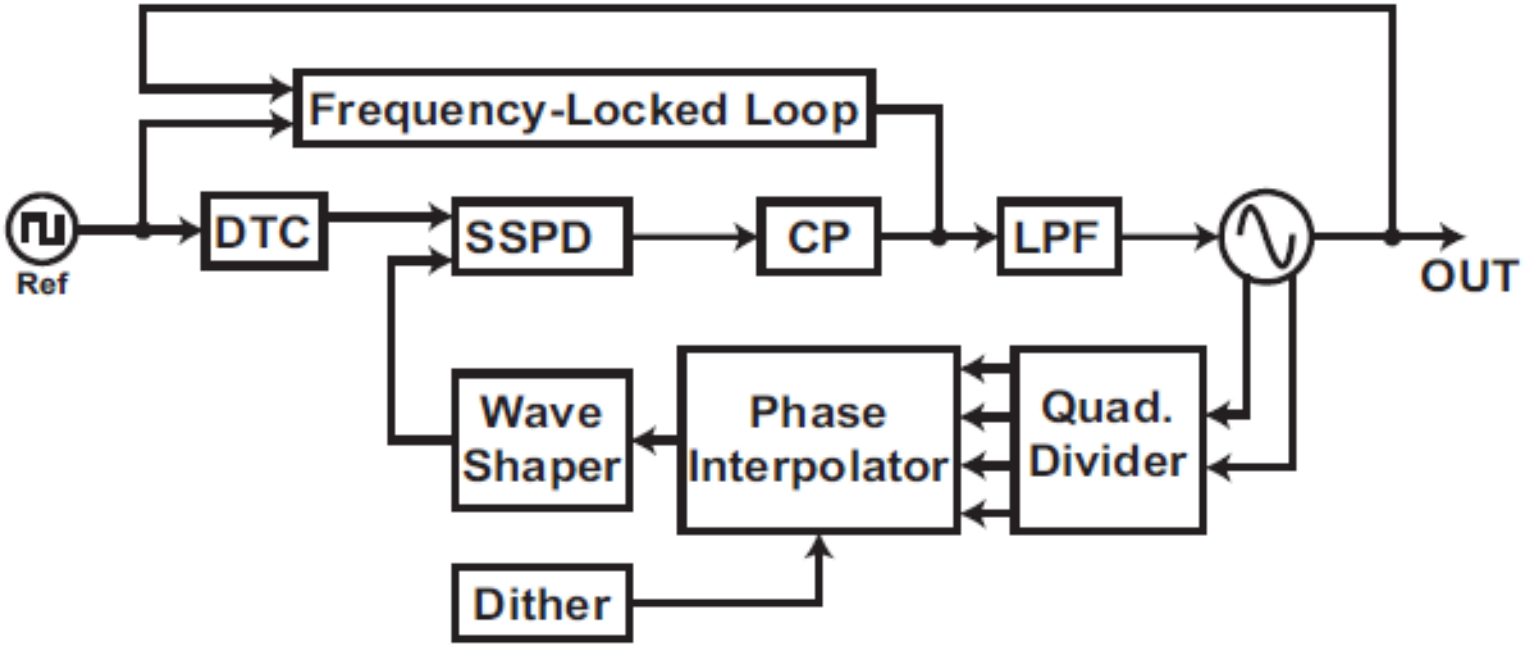


- **SSTDC plus extensive digital calibration [16]**
  - SSTDC digitizes entire waveform
  - Extensive digital calibration linearizes the SSTDC over a wide detection range



Extend SSPLL to Fractional-N, Cont'd

- **DTC + Phase Interpolator frac-N SSPLL [26]**
  - **The use of phase interpolator together with DTC relaxes the DTC's resolution and dynamic range requirement**
  - **Achieved -246dB FOM, current record for frac-N PLLs**



References

1. X. Gao, E. Klumperink, P. J. F. Geraedts and B. Nauta, "Jitter Analysis and a Benchmarking Figure-of-Merit for Phase-Locked Loops," *IEEE Trans. Circuits Syst. II*, vol. 56, no. 2, pp. 117-121, Feb. 2009.
2. X. Gao, E. Klumperink, M. Bohsali and B. Nauta, "A Low Noise Sub-Sampling PLL in Which Divider Noise is Eliminated and PD/CP Noise is not Multiplied by N^2," *IEEE J. Solid-State Circuits,* vol. 44, no. 12, pp. 3253-3263, Dec. 2009.
3. C.-W. Hsu, K. Tripurari, S.-A. Yu and P. R. Kinget, "A Sub-Sampling-Assisted Phase-Frequency Detector for Low-Noise PLLs With Robust Operation Under Supply Interference," *IEEE Trans. Circuits Syst. I,* vol. 62, no. 1, pp. 90-99, Jan. 2015.
4. X. Gao, E. Klumperink, G. Socci, M. Bohsali and B. Nauta, "A 2.2GHz Sub-Sampling PLL with 0.16ps_{rms} Jitter and -125dBc/Hz In-band Phase Noise at 700μW Loop-Components Power," *IEEE Symposium on VLSI Circuits*, pp. 139-140, Jun. 2010.
5. X. Gao, E. Klumperink, G. Socci, M. Bohsali and B. Nauta, "Spur Reduction Techniques for Phase-Locked Loops Exploiting a Sub-Sampling Phase Detector," *IEEE J. Solid-State Circuits,* vol. 45, no. 9, pp. 1809-1821, Sept. 2010.
6. D. Cai, *et. al.*, "A Dividerless PLL With Low Power and Low Reference Spur by Aperture-Phase Detector and Phase-to-Analog Converter," *IEEE Trans. Circuits Syst. I*, vol. 60, no. 1, pp. 37-50, Jan. 2013.
7. S. D. Vamvakos, *et. al.*, "A 8.125–15.625 Gb/s SerDes using a sub-sampling ring-oscillator phase-locked loop," *IEEE Custom Integrated Circuits Conference (CICC)*, paper 10.1, Sept. 2014.
8. K. Sogo, A. Toya and T. Kikkawa, "A ring-VCO-based sub-sampling PLL CMOS circuit with –119 dBc/Hz phase noise and 0.73 ps jitter," *IEEE European Solid State Circuits Conference (ESSCIRC),* pp. 253-256, Sept. 2012.
9. X. Yi, C. C. Boon, J. Sun, N. Huang and W. M. Lim, "A low phase noise 24/77 GHz dual-band sub-sampling PLL for automotive radar applications in 65 nm CMOS technology," *IEEE Asian Solid-State Circuits Conference (A-SSCC),* pp. 417-420, Nov. 2013.
10. T. Siriburanon, *et. al.*, "A 60-GHz sub-sampling frequency synthesizer using sub-harmonic injection-locked quadrature oscillators," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, pp. 105-108, Jun. 2014.
11. C.-F. Liang and K.-J. Hsiao, "An Injection-Locked Ring PLL with Self-Aligned Injection Window", *IEEE Int. Solid-State Circuits Conference (ISSCC)*, pp. 90-92, Feb. 2011.
12. I.-T. Lee, *et. al.*, "A divider-less sub-harmonically injection-locked PLL with self-adjusted injection timing," *IEEE Int. Solid-State Circuits Conference (ISSCC),* pp. 414-415, Feb. 2013.
13. X. Gao, "Low Jitter Low Power Phase Locked Loops Using Sub-Sampling," PhD thesis, University of Twente, ISBN-978-90-365-3022-4, 2010.

References Cont'd

14. T. Siriburanon, *et. al.*, "A 2.2GHz –242dB-FOM 4.2mW ADC-PLL using digital sub-sampling architecture," *IEEE Solid- State Circuits Conference - (ISSCC)*, paper 25.2, Feb. 2015.
15. Z. Ru, P. Geraedts, E. Klumperink and B. Nauta, "A 12GHz 210fs 6mW Digital PLL with Sub-sampling Binary Phase Detector and Voltage-Time Modulated DCO," IEEE Symp. VLSI Circuits, pp. 194-195, June 2013.
16. Z.-Z. Chen, *et. al.*, "Sub-sampling all-digital fractional-N frequency synthesizer with –111dBc/Hz in-band phase noise and an FOM of –242dB," *IEEE Solid- State Circuits Conference - (ISSCC)*, paper 14.9, Feb. 2015.
17. K. Raczkowski, N. Markulic, B. Hershberg, J. Van Driessche, and J. Craninckx, "A 9.2–12.7 GHz wideband fractional-N subsampling PLL sin 28nm CMOS with 280fs RMS jitter," *IEEE Radio Frequency Integrated Circuits Symposium (RFIC),* pp. 89-92, Jun. 2014.
18. W.-S. Chang, P,-C, Huang and T.-C. Lee, "A Fractional-N Divider-Less Phase-Locked Loop With a Subsampling Phase Detector," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2964-2975, Dec. 2014.
19. N. Markulic, K. Raczkowski, P. Wambacq and J. Craninckx, "A 10-bit, 550-fs step Digital-to-Time Converter in 28nm CMOS," *IEEE European Solid State Circuits Conference (ESSCIRC),* pp. 79-82, Sept. 2014.
20. S. Ikeda, S.-Y. Lee, H. Ito, N. Ishihara and K. Masu, "A 0.52-V 5.7-GHz low noise sub-sampling PLL with dynamic threshold MOSFET," *IEEE Asian Solid-State Circuits Conference (A-SSCC),* pp. 365-368, Nov. 2014.
21. J. Liang, Z. Zhou, J. Han and D. G. Elliott, "A 6.0–13.5 GHz Alias-Locked Loop Frequency Synthesizer in 130 nm CMOS," *IEEE Trans. Circuits Syst. I*, vol. 60, no. 1, pp. 108-115, Jan. 2013.
22. P. Kinget, "Integrated GHz voltage controlled oscillators," *Analog Circuit Design: (X)DSL and Other Communication Systems; RF MOST Models; Integrated Filters and Oscillators*, Kluwer, 1999, pp. 353-381.
23. C. S. Vaucher, *Architectures for RF Frequency Synthesizers*. Boston, MA: Kluwer, 2002.
24. I.-T. Lee, K.-H. Zeng and S.-I. Liu, "A 4.8-GHz Dividerless Subharmonically Injection-Locked All-Digital PLL With a FOM of -252.5 dB," *IEEE Trans. Circuits Syst. II*, vol. 60, no. 9, pp. 547-551, Sept. 2013.
25. Z. Ru, C. Palattella, P. Geraedts, E. Klumperink and B. Nauta, "A High-Linearity Digital-to-Time Converter Technique: Constant-Slope Charging", *IEEE J. Solid-State Circuits*, vol. 50, no. 6, pp. 1412-1423, Jun. 2015.
26. A. T. Narayanan, et. al., "A Fractional-N Sub-Sampling PLL using a Pipelined Phase-Interpolator with a FoM of -246dB", *IEEE European Solid State Circuits Conference (ESSCIRC),* pp. 380-383, Sept. 2015.