A 2-24GHz 360° Full-Span Differential Vector Modulator Phase Rotator with Transformer-Based Poly-Phase Quadrature Network

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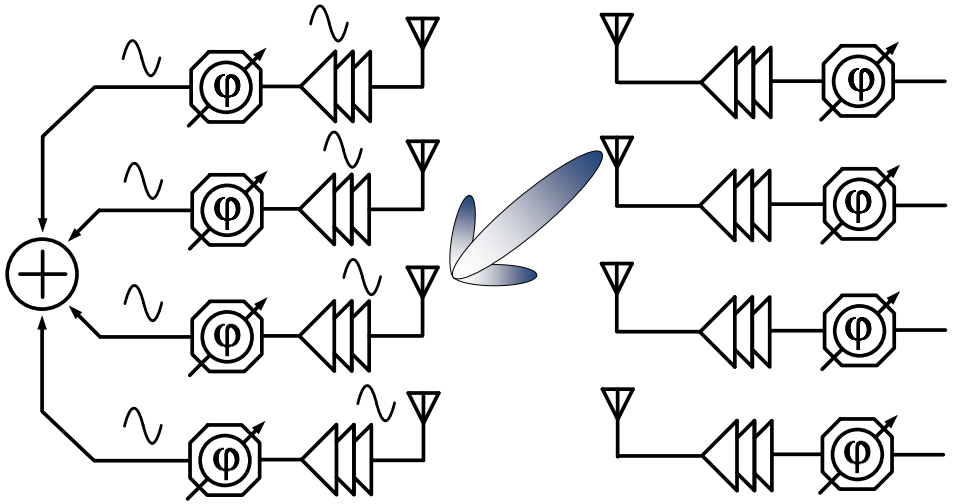
Outline

- Introduction
- Circuit Design and Simulation Results
- Measurement Results
- Conclusion

Introduction

Phased-arrays system have been widely used in radar and communication systems due to its inherent advantages.



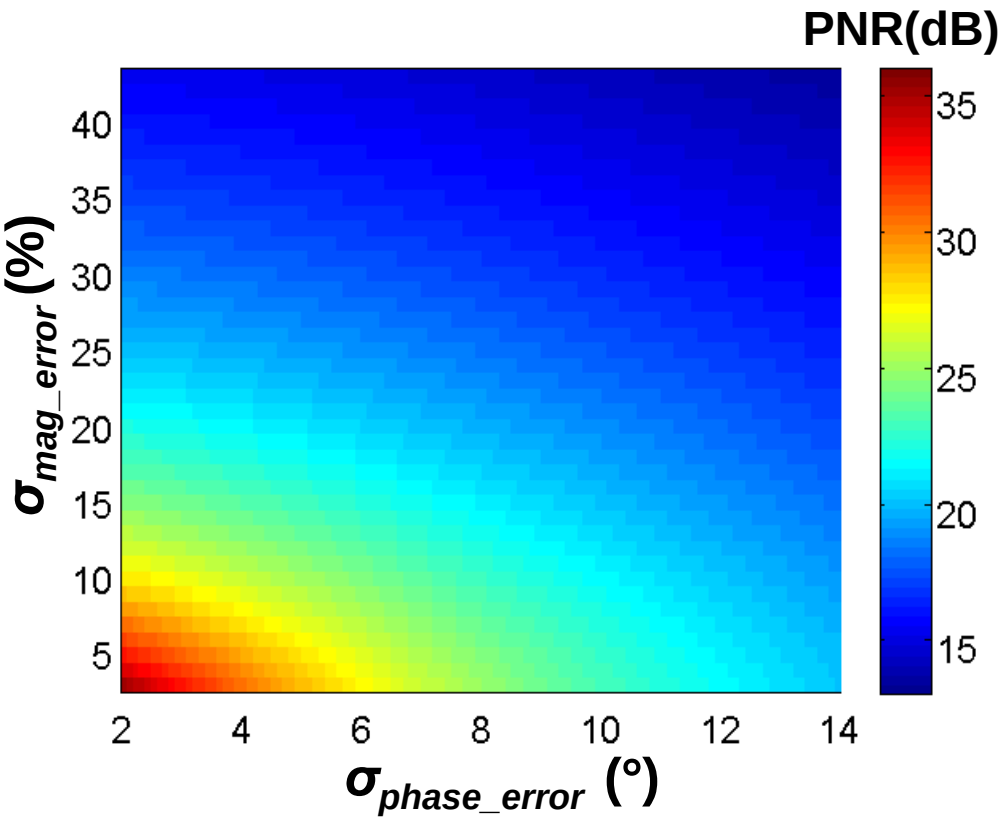
SNR Improvement: 10log(N) **EIRP: 20log(N)**

N: Number of array element

- Signal-to-noise ratio (SNR) improvement (10logN)
- High equivalent isotropic radiated power (EIRP)
- Beam forming/steering for spatial filtering

Introduction

4-element-array Peak to Null Ratio (PNR) vs σ_{mag_error} and σ_{phase_error}

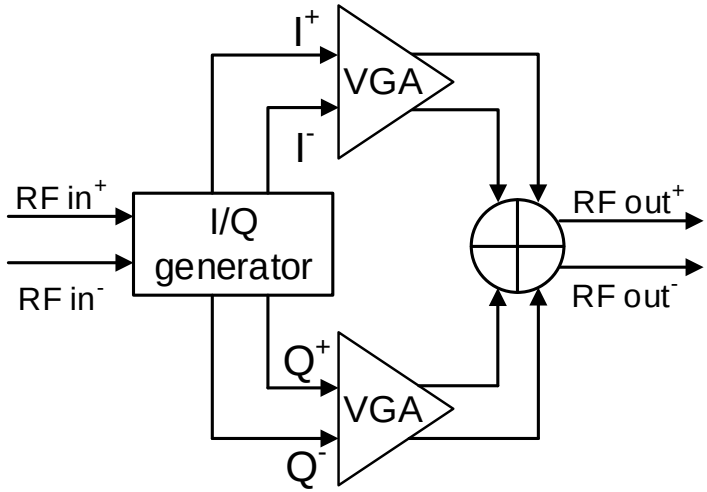


A high precision phase rotator is essential in the phased-array system.

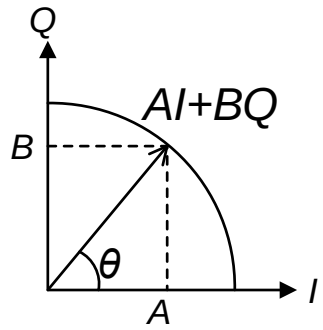
Introduction

I/Q vector modulator phase rotator block diagram

- Full span phase shifting range (0° to 360°)
- Wide bandwidth
- Signal amplification
- Compact chip area



$$\theta = tan^{-1}\left(\frac{B}{A}\right)$$



- No fundamental tradeoff between insertion loss and phase shift range, unlike passive phase shfiter

The I/Q generation is critical part of the vector modulator phase rotator for the phase interpolation accuracy and bandwidth.

Introduction

The I/Q generation schemes are evaluated by passive loss, I/Q magnitude/phase balance, bandwidth, and robustness to mismatches.

Key performance	Loss	I/Q amplitude/phase balance	Bandwidth	Robustness to mismatches	Loading Effect	Size
RCCR pairs	✗	✓	✗	✗	✗	✓
RCCR poly-phase network	✗	✓	✓	✓	✗	✓
Transformer	✓	✓	✗	✓	✓	✗
Folded transformer	✓	✓	✗	✓	✓	✓

The bandwidth of transformer-based approach is often limited to 20%.

Introduction

In order to extend bandwidth, we employ fully differential transformer-based poly-phase network in vector modulator phase rotator to achieve first-ever a decade bandwidth.

- Compact chip area (differential folded transformer)
- Low loss
- Robustness to process variation
- Over-a-decade bandwidth
- High precision I/Q magnitude/phase balance
- Input matching and robustness to loading effect

Outline

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- **Circuit Design and Simulation Results**
- Measurement Results
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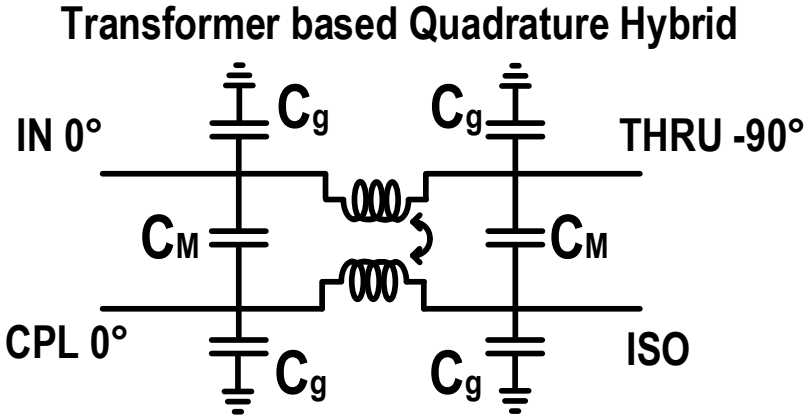
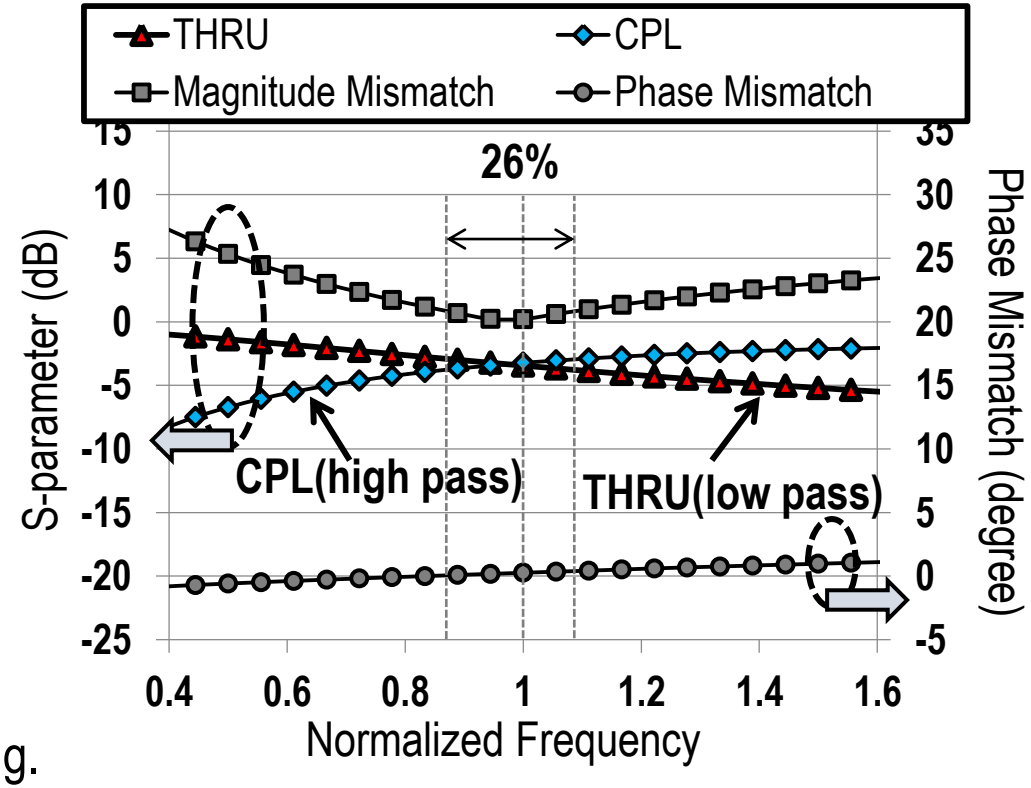
Circuit Design and Simulation Results

Transformer-based quadrature hybrid



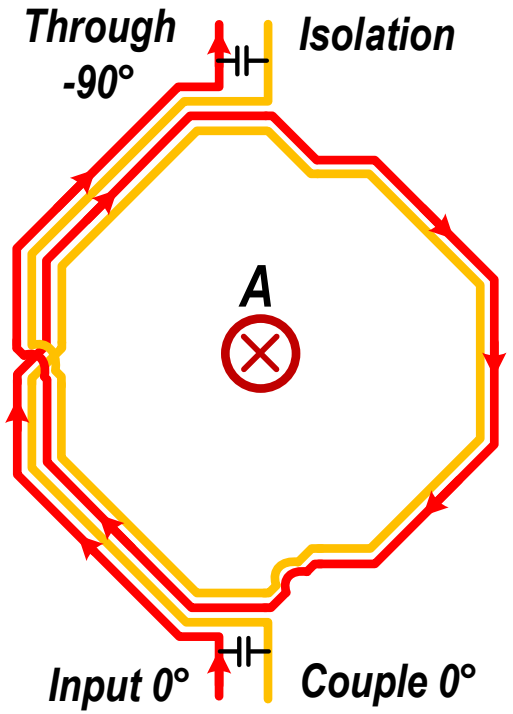


- Utilizing inductive and capacitive coupling.
- CPL and THRU with an accurate 90°phase matching for wide bandwidth.
- 1dB magnitude mismatch bandwidth is 26%.

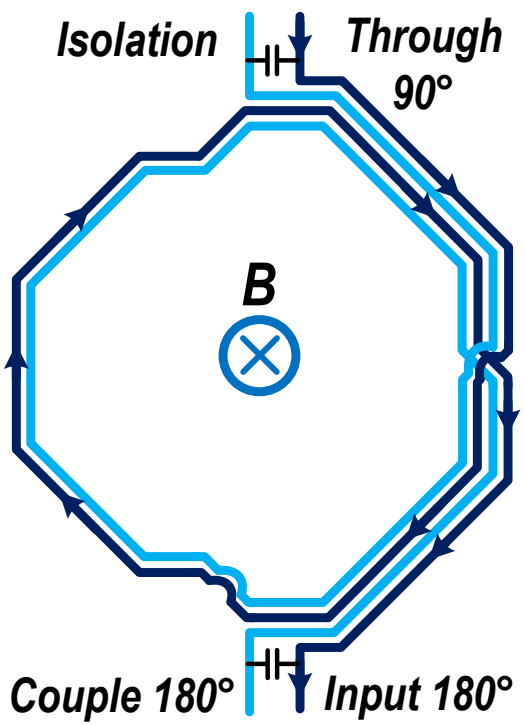
→ Magnitude mismatch is limiting factor and should be compensated for broad band operation.

Circuit Design and Simulation Results

Differential 8-port folded transformer-based quadrature hybrid



Single-ended transformer based quadrature hybrid A



Single-ended transformer based quadrature hybrid B

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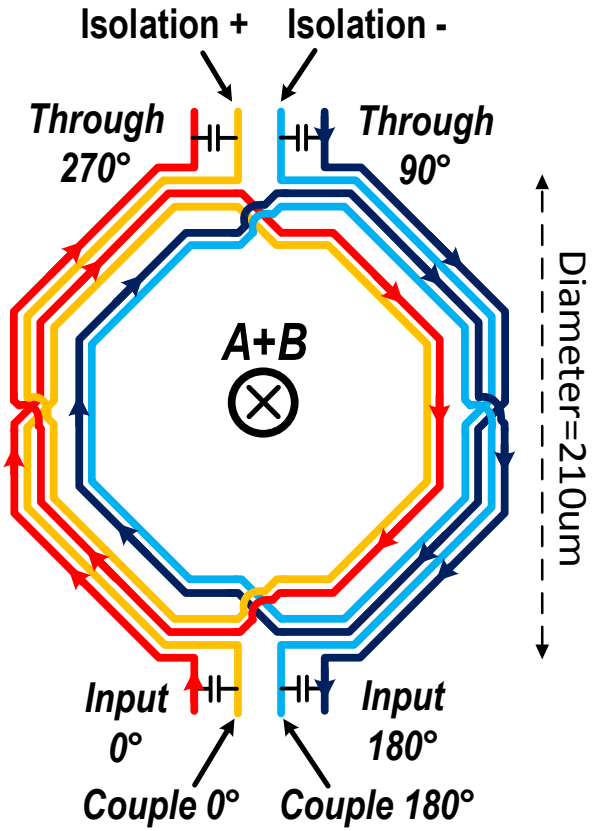
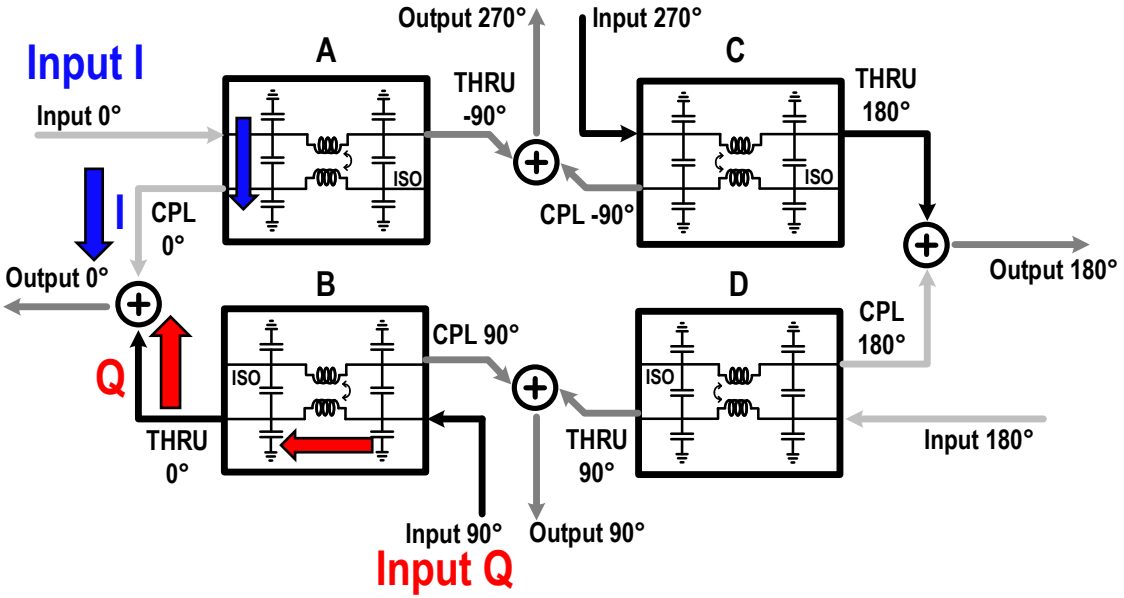


8-port folded transformer-based quadrature hybrid

Circuit Design and Simulation Results

The transformer-based poly-phase unit stage



The transformer-based poly-phase unit stage

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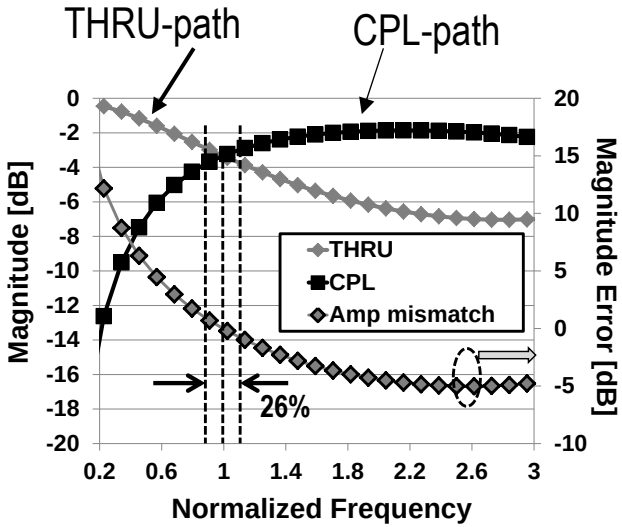
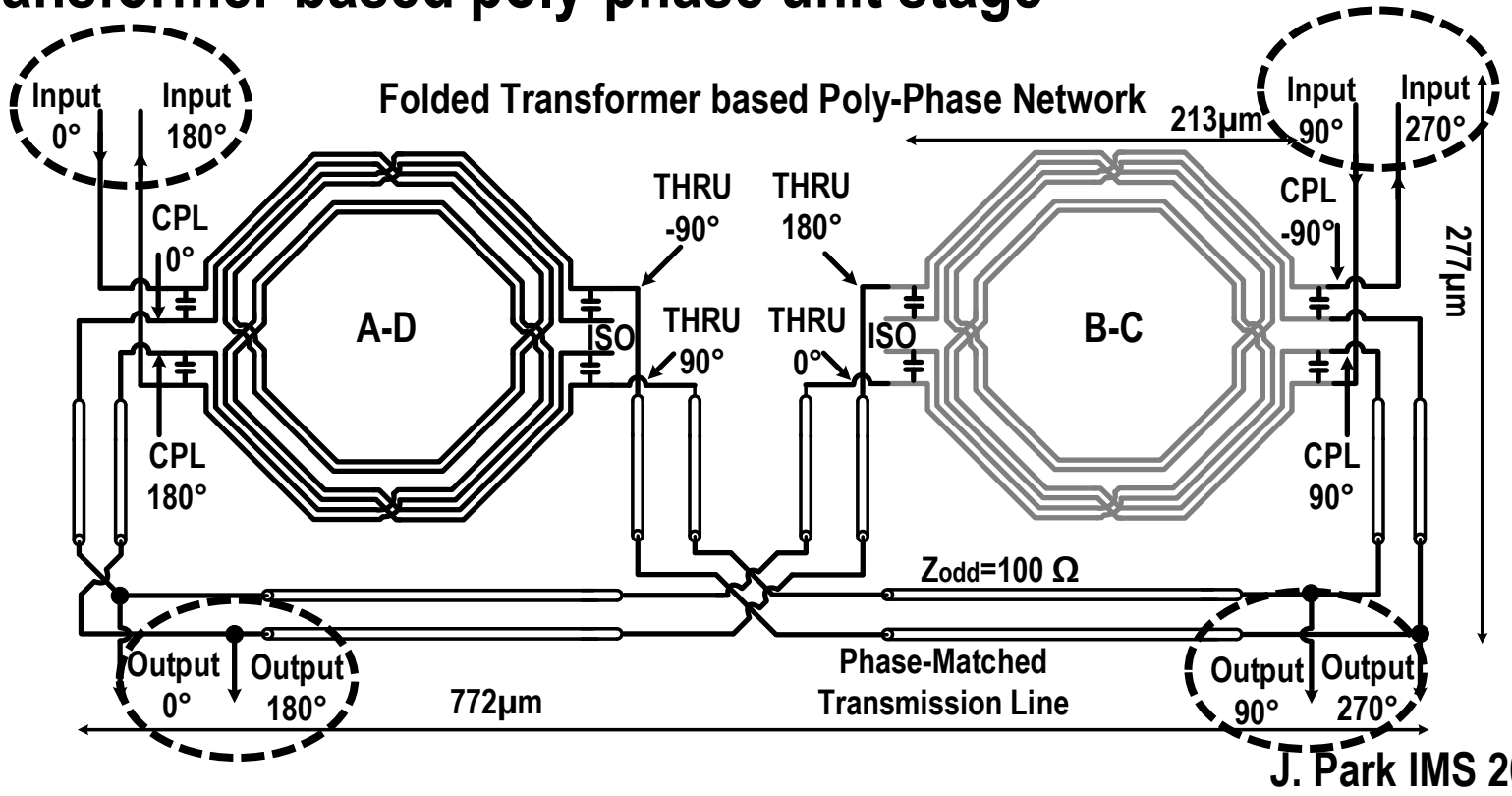


- Two signals (one from input I and the other from input Q) are combined at the output
→ the I/Q magnitude mismatches at the inputs are suppressed at the outputs.
- Transformer-based quadrature hybrid A and B have differential relation with transformer-based quadrature hybrid D and C, respectively.

Circuit Design and Simulation Results

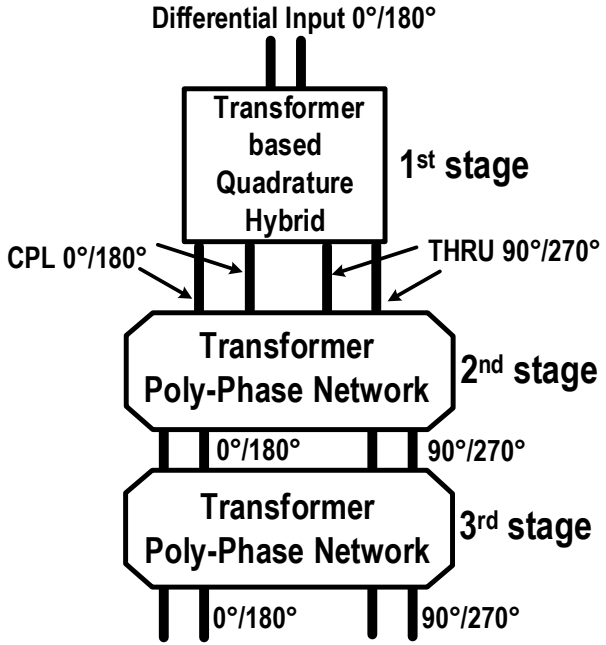
The transformer-based poly-phase unit stage



- The transformer poly-phase unit stage is implemented with two folded transformer-based quadrature hybrids.
- 100Ω differential transmission line is employed for proper parallel in-phase power combining.

Circuit Design and Simulation Results

3-stage transformer-based poly-phase network

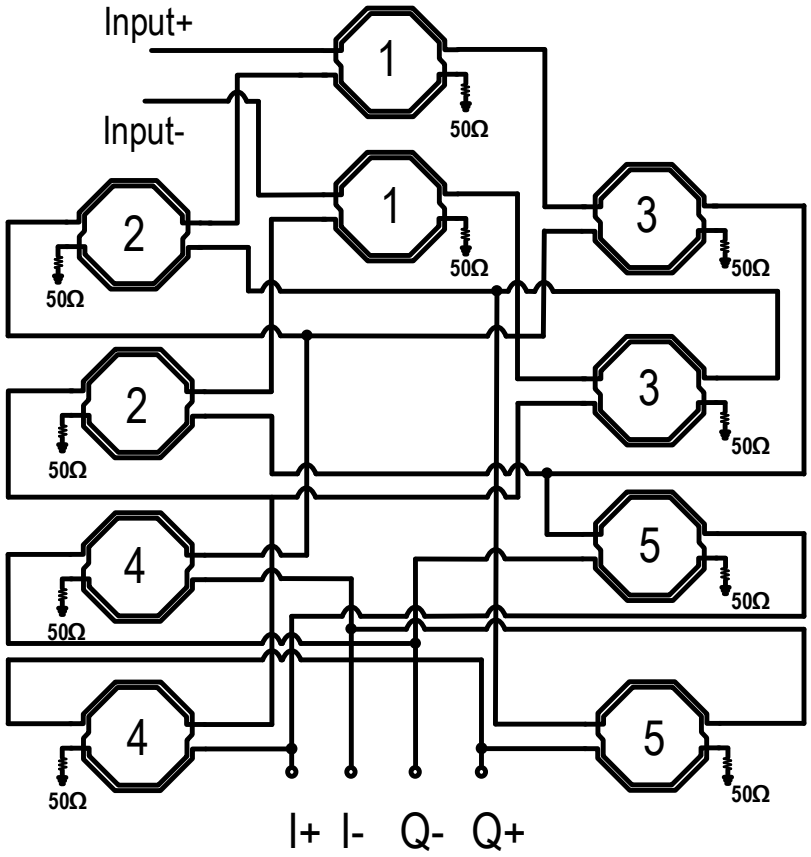


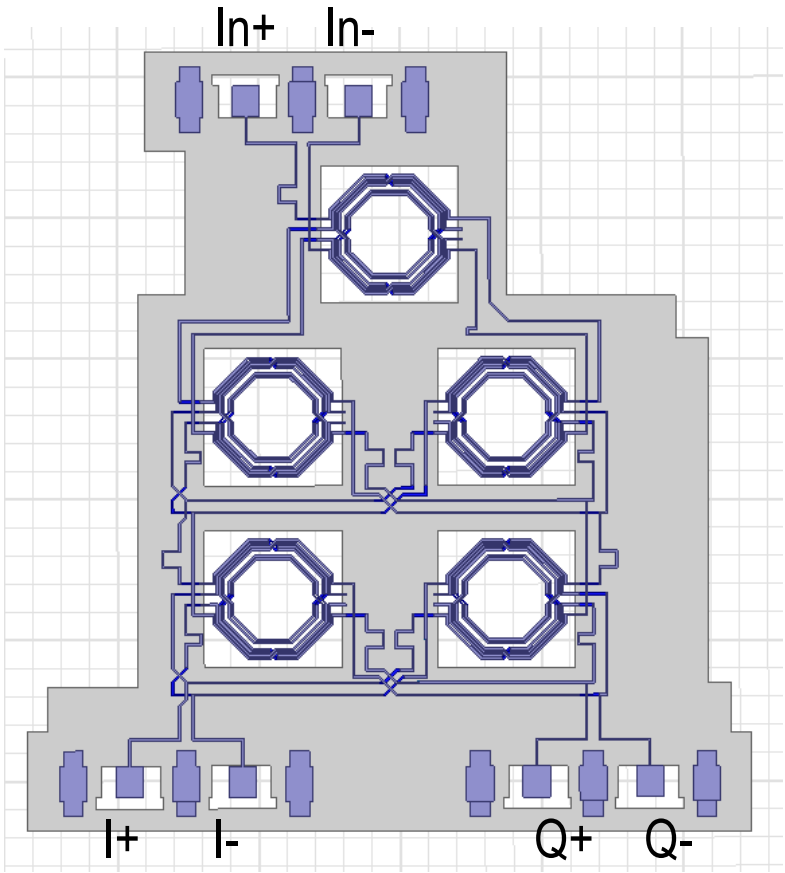
3-stage transformer-based poly-phase network

- The differential quadrature signals are generated at 1st stage.
- The I/Q magnitude/phase mismatches are compensated by the transformer-based poly-phase unit stage at 2nd stage.
- The transformer-based poly-phase unit stage further suppresses the I/Q magnitude/phase mismatches at 3rd stage.

Circuit Design and Simulation Results

3-stage transformer-based poly-phase network

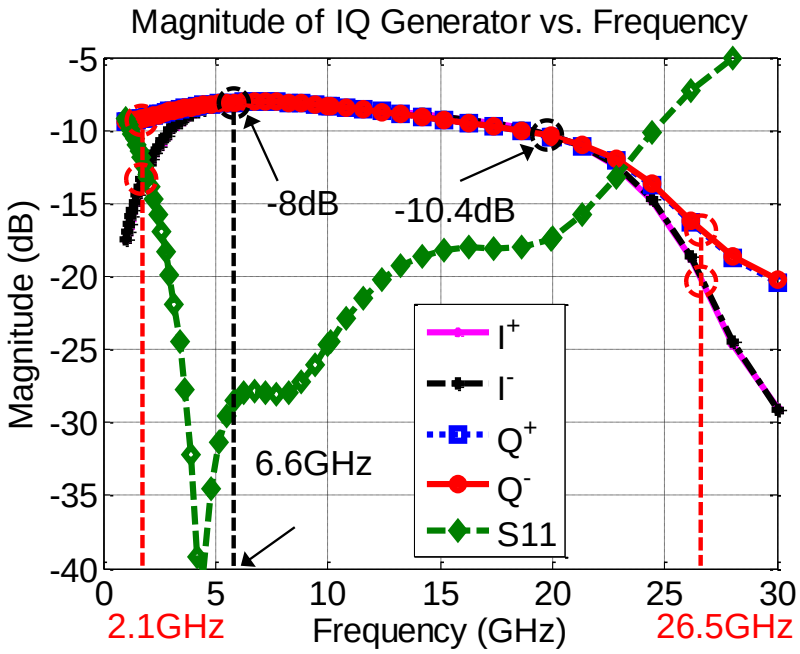


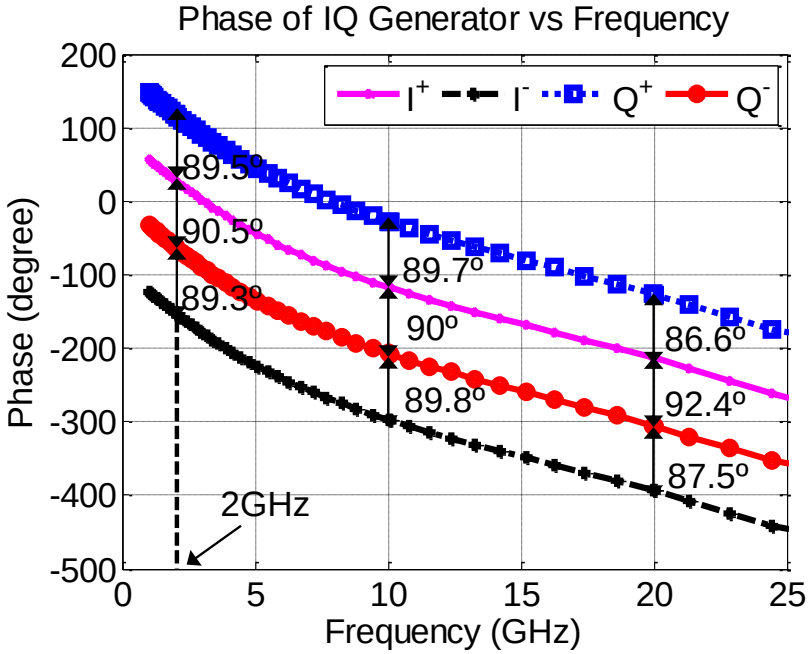


• 3-stage transformer poly-phase network implemented with (a) singled-ended transformer-based quadrature hybrid and (b) folded transformer-based quadrature hybrid.

Circuit Design and Simulation Results

EM simulated magnitude/phase response of the 3-stage transformer poly-phase network

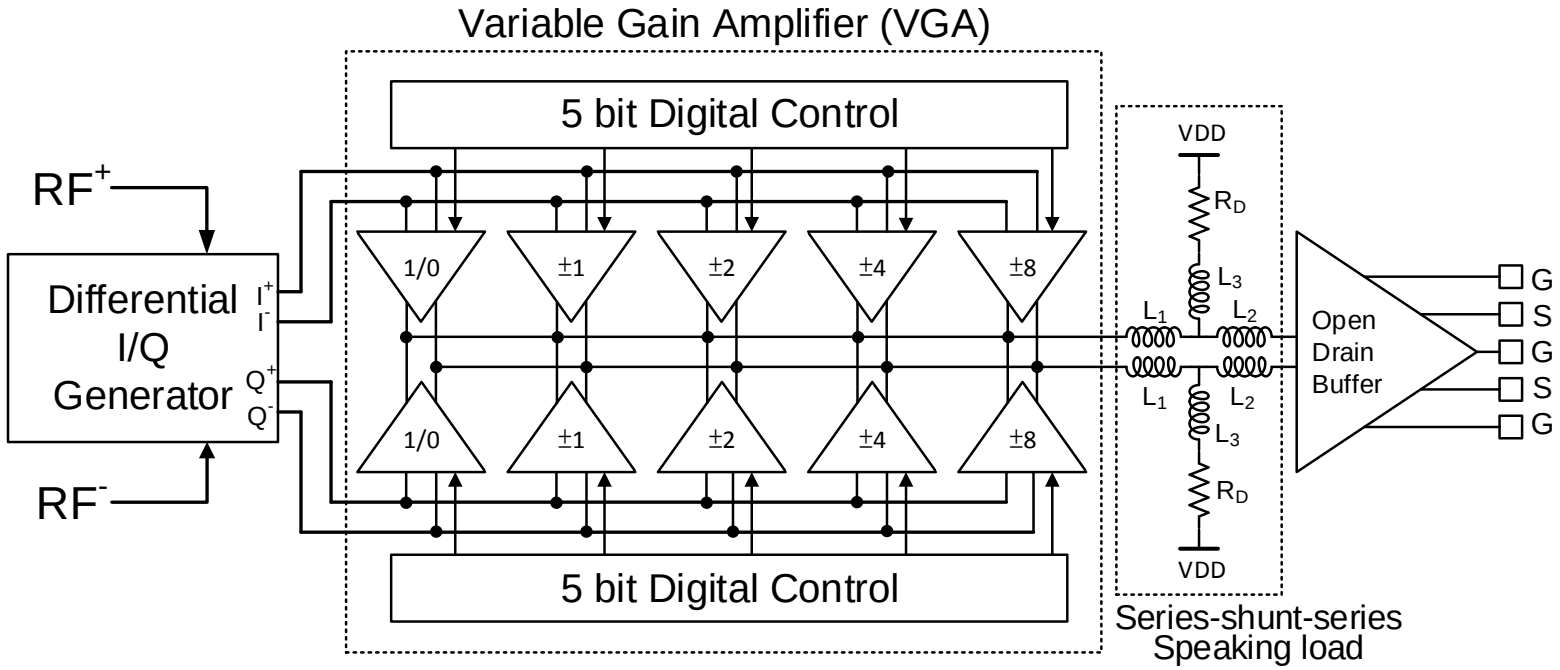




- The simulated best in-band insertion loss of 2dB (-6dB loss due to power splitting).
- I/Q magnitude mismatch ≤3dB from 2.1GHz to 26.5GHz with maximum phase error of 5°
- **It achieves world first decade bandwidth.**

Circuit Design and Simulation Results

Proposed I/Q vector modulator phase rotator



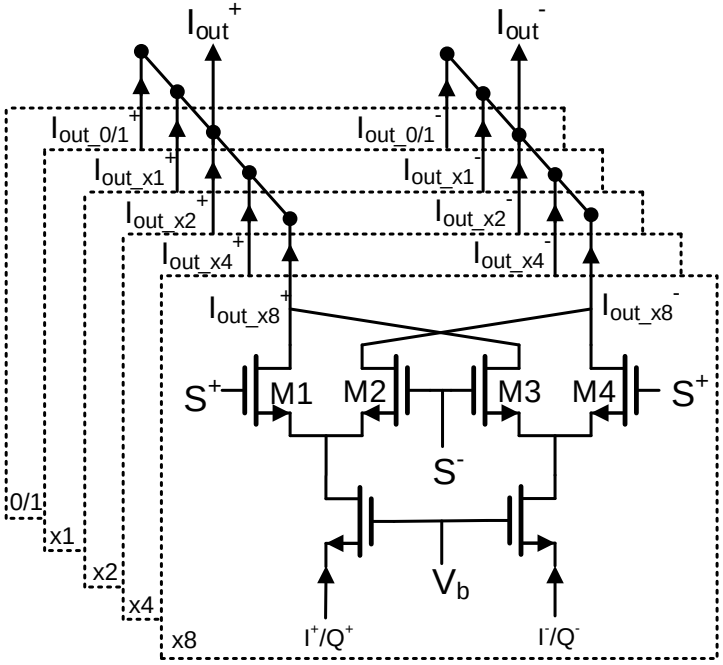
• The I/Q outputs of the 3-stage transformer-based poly-phase network are independently amplified by two 5-bit I/Q Variable Gain Amplifiers (VGA).

• Series-shunt-series peaking loads (Ind. L_1-L_3 and res. R_D) achieve bandwidth extension.

• An output differential open-drain buffer facilitates the measurement.

Circuit Design and Simulation Results

5-bit binary weighted Variable Gain Amplifiers (VGA)



5 bit VGA

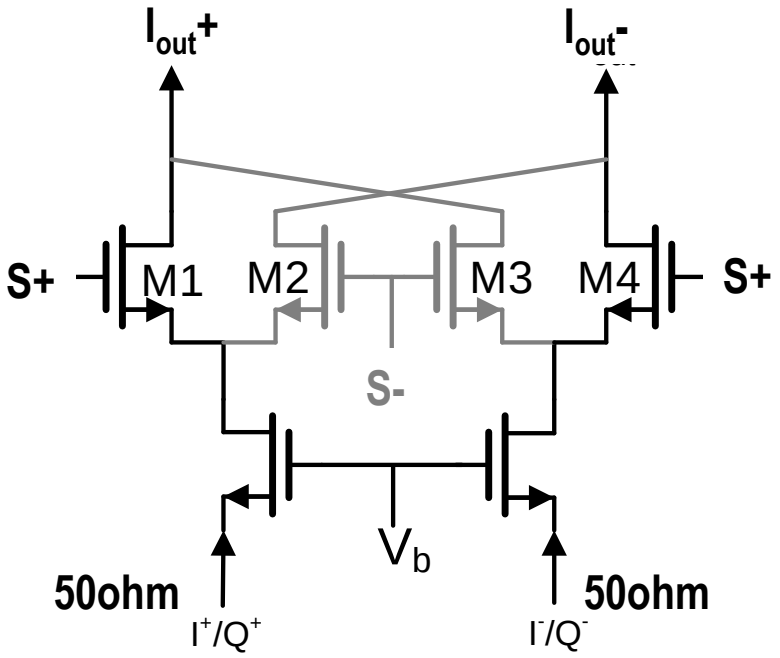
$$I_{out} = A_0 \times I_0 + A_1 \times I_1 + A_2 \times I_2 + A_4 \times I_4 + A_8 \times I_8$$

- A common-gate (CG) topology provides broadband matching.
- The 5-bit binary weighted cells are employed as polarity selectors with CG differential cascode amplifier (x1, x2, x4, and x8) **for -15 to +15 relative weighting.**
- Additional x1 cell (half-bit) provides “+1” or “0” weighting.

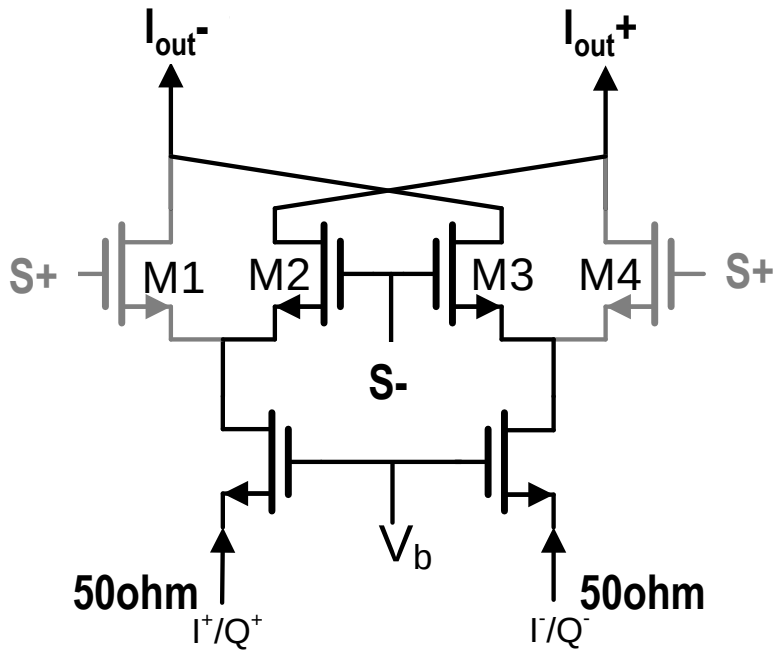
Circuit Design and Simulation Results

X1 unit cell in Variable Gain Amplifier (VGA)

"+1" (S^+=high, S^-=low)



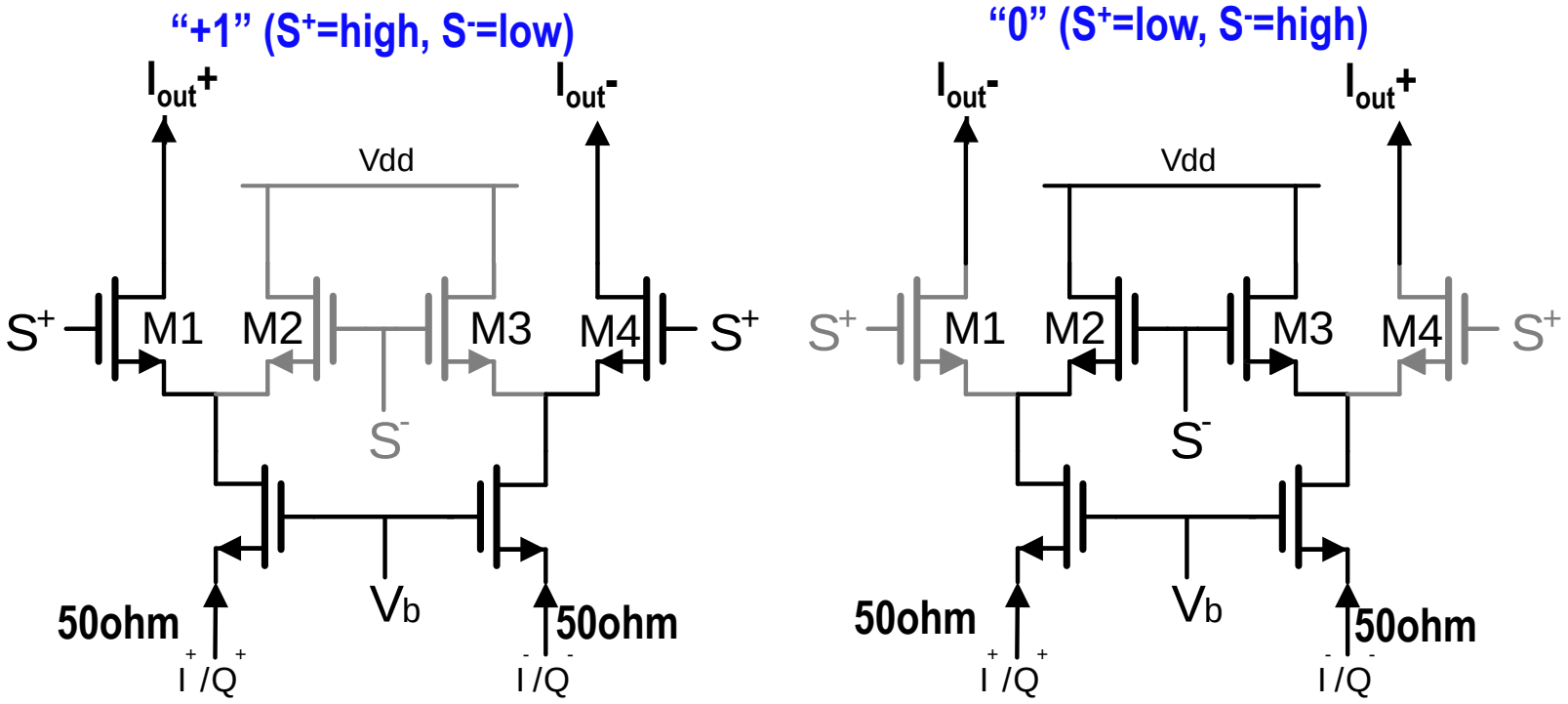
"-1" (S^+=low, S^-=high)



- CG differential cascode amplifier serves as a polarity selector.
- The input impedance of combined VGA cells and DC current are constant regardless of the control bit settings.

Circuit Design and Simulation Results

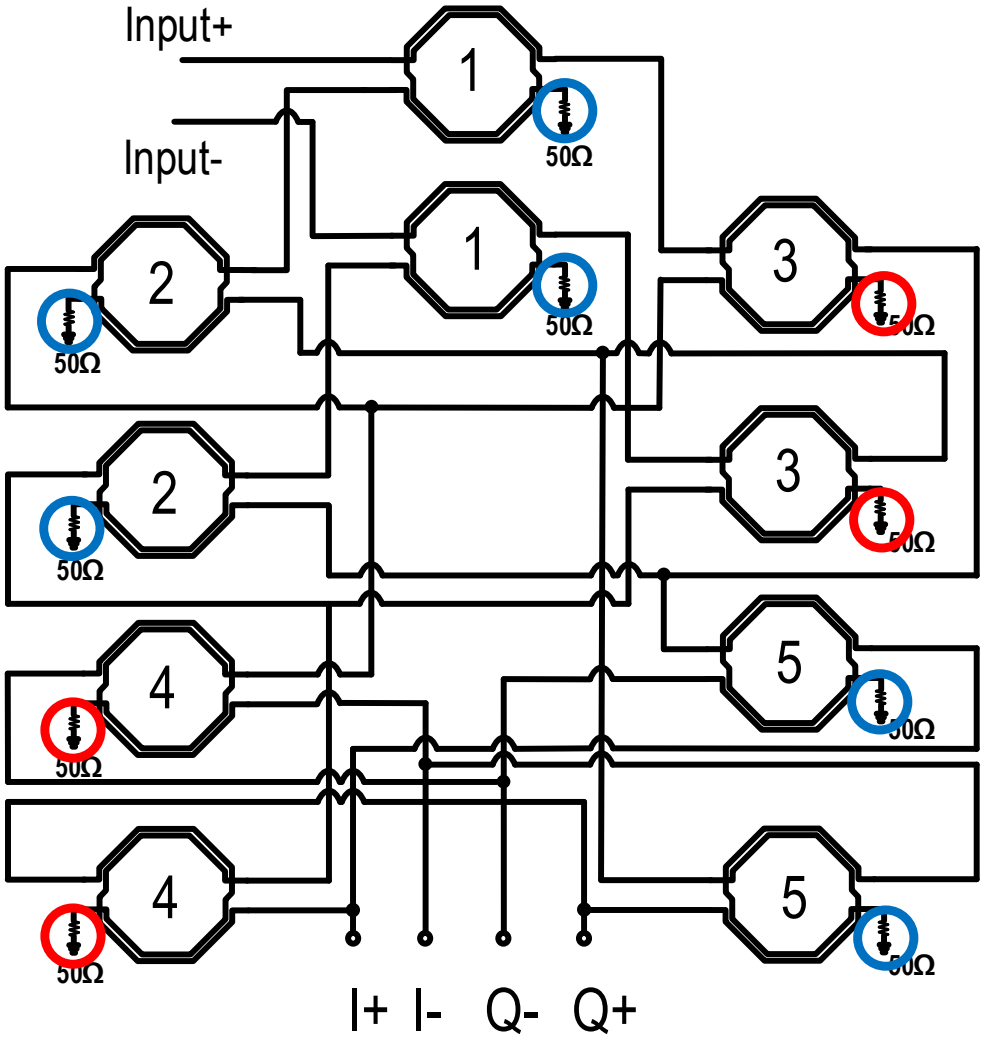
Additional half-bit cell in the Variable Gain Amplifier (VGA)



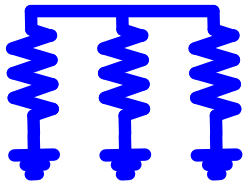
- Additional x1 cell provides "+1" or "0" to achieve a normalized weighting range from +15 to -15 including the zero weighting.
- M2 and M3 are tied to DC supply.

Circuit Design and Simulation Results

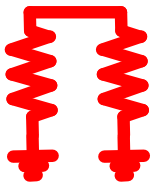
VGA and 3-stage transformer-based poly-phase network interface



• I path (I+/I-) has 3 parallel isolation 50Ω terminations.



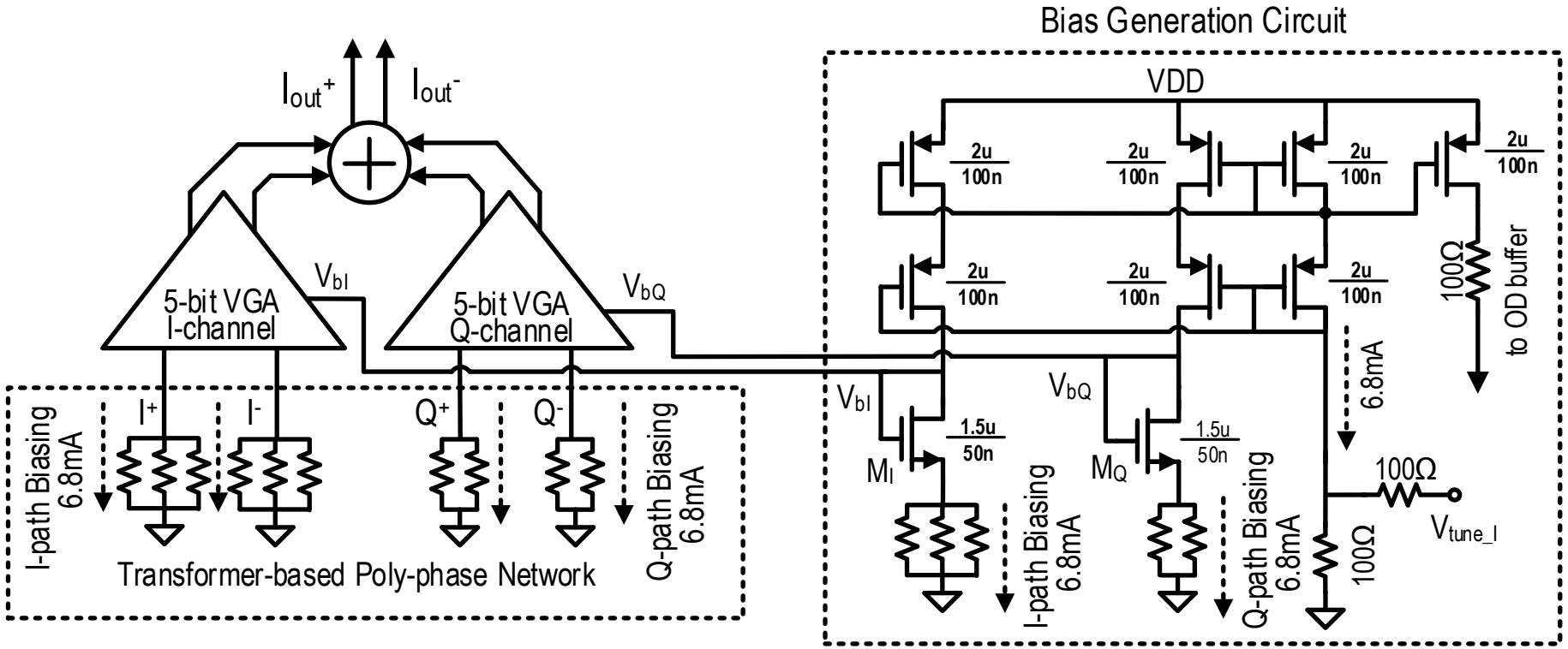
• Q path (Q+/Q-) has 2 parallel isolation 50Ω terminations.



In: input **Tr: through**
Cp: couple **Is: isolation**

Circuit Design and Simulation Results

Bias generation circuit for the I/Q VGAs



- The bias generation circuit ensures the identical biasing current between I/Q VGAs.

Outline

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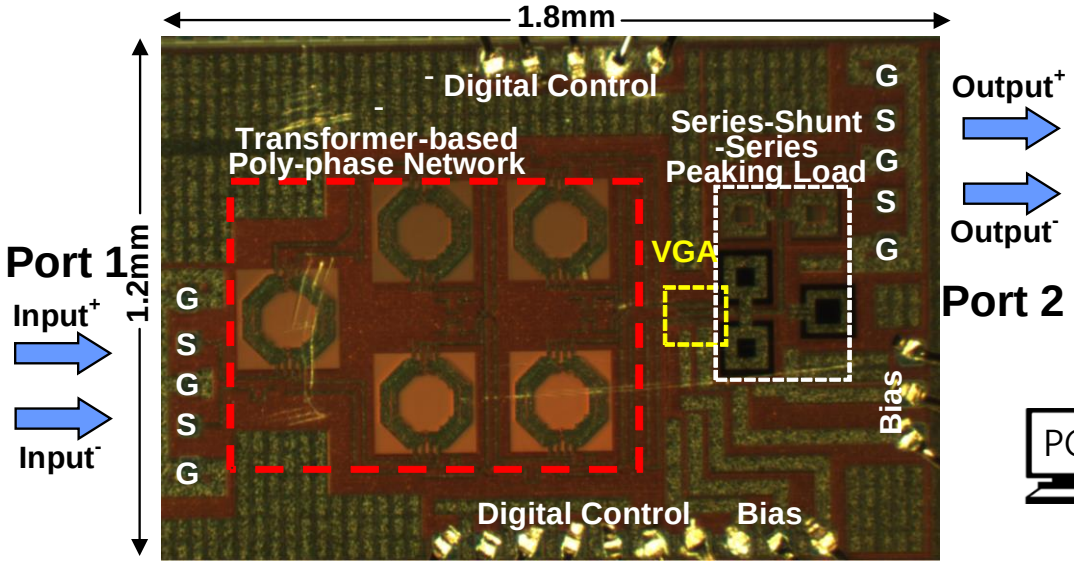
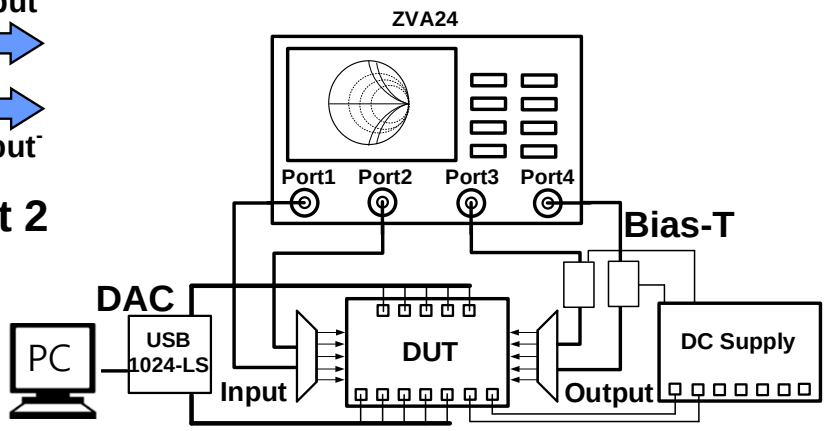
- **Measurement**
- Conclusion

Measurement

The chip microphotograph and measurement setup



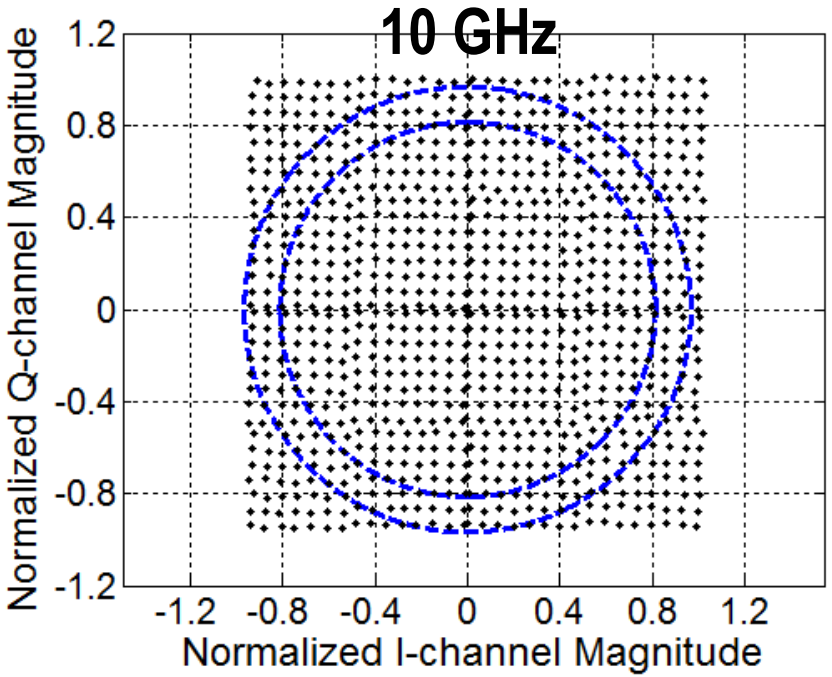


- Standard 65nm CMOS process
- Compact chip size (1.8mm by 1.2mm)
- The size of the 3-stage transformer-based poly phase network is 772μm×925μm.
- Phase rotator consumes 26.8mA from 2V and 13.4mA from 1.5V for open drain buffer

- A 4-port vector network analyzer for differential S-parameter measurement
- Off-chip DAC for digital programming
- Open drain buffer for measurement

Measurement

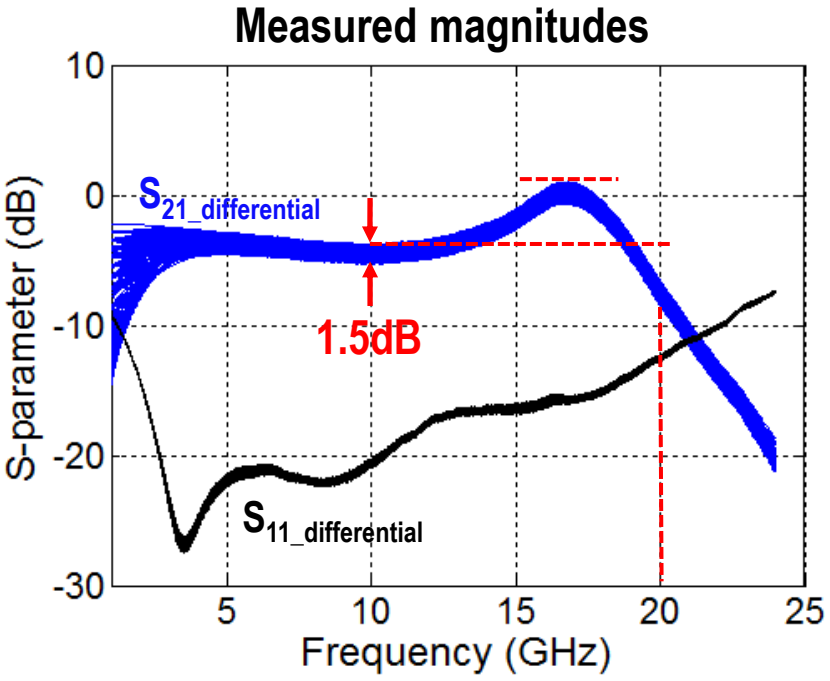
Measurement results

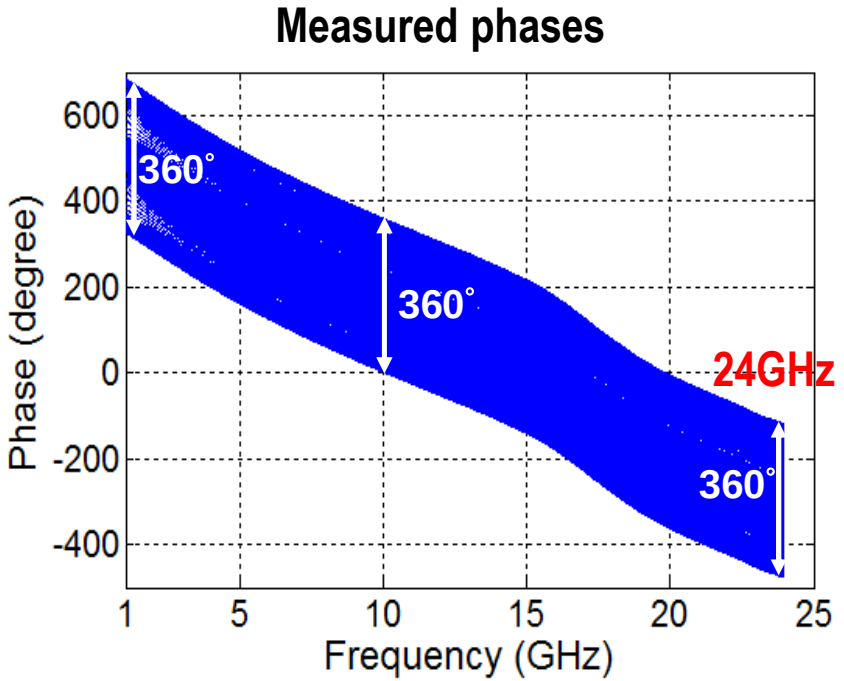


- Measured phase interpolation points on the normalized I/Q coordinates (31×31=961 points).
- High precision I/Q magnitude/phase balance and I-VGA/Q-VGA matching are achieved.
- Dense phase interpolation points are achieved.

Measurement

Measurement results

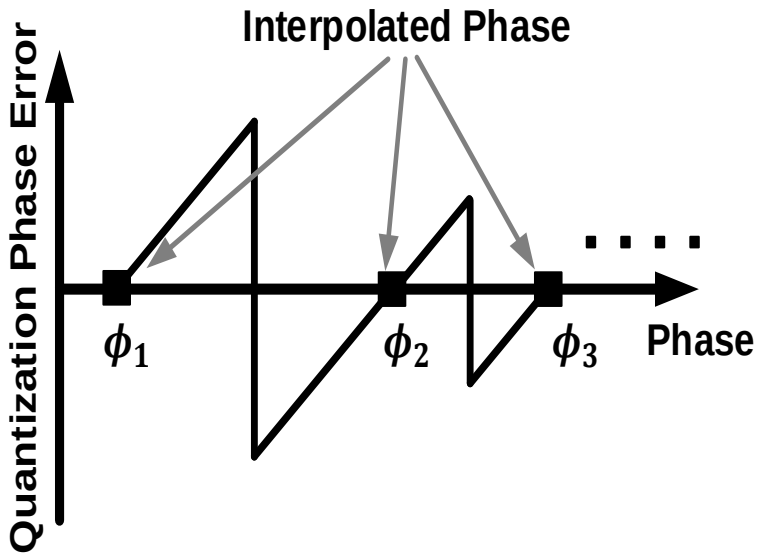


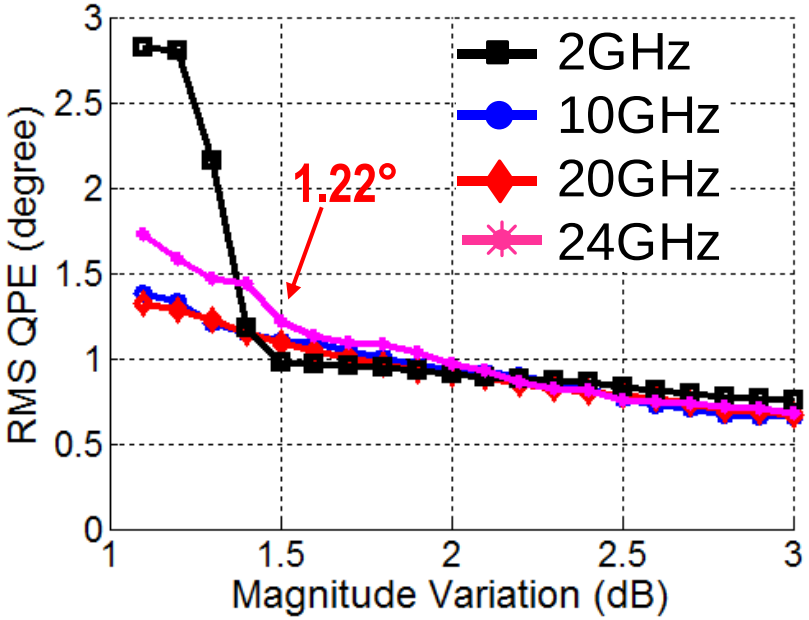


- Within 1.5dB amplitude variation, the phase rotator achieves 360-degree phase interpolation with max phase step of 2.5°.
- 3dB amplitude BW is from 2GHz to 20GHz.
- **It achieves world first phase rotator with an instantaneous one-decade bandwidth and 360° phase interpolation**

Measurement

Measurement results

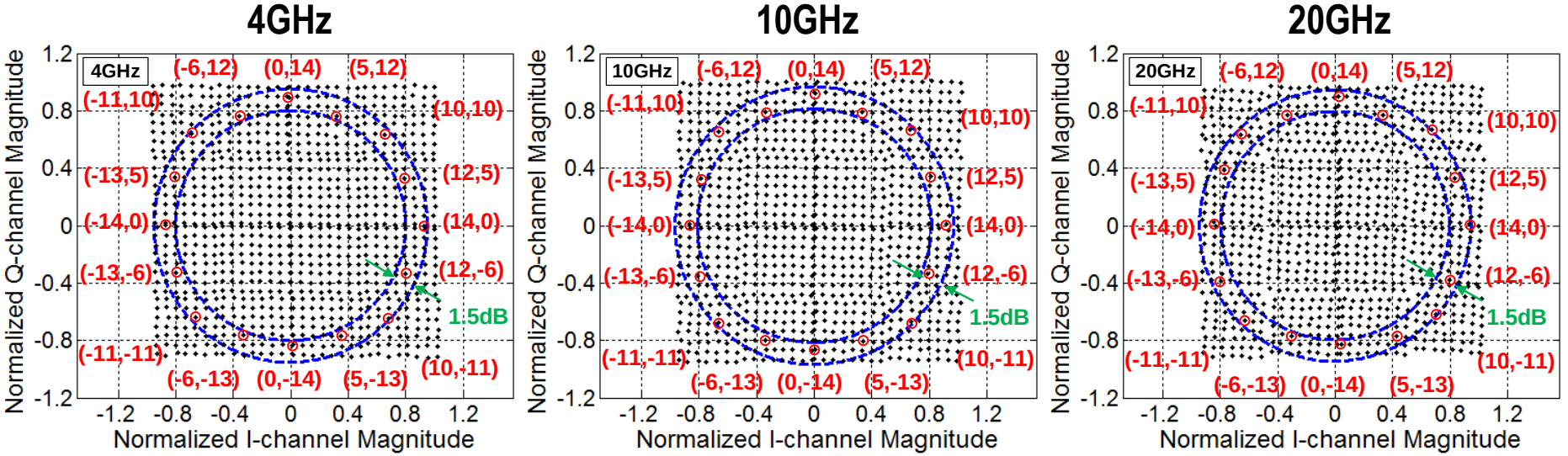




- Quantization Phase Error (QPE) is defined as phase error between desired phase and interpolated phase.
- Within 1.5dB magnitude variation, our phase rotator achieves measured RMS phase quantization errors <1.22° for 360° full-span interpolation from 2GHz to 24GHz.
- **One decade bandwidth and ultra-low RMS phase quantization errors are achieved simultaneously.**

Measurement

Measurement results



- Measured phase interpolation points with 45° steps at 4GHz, 10GHz, and 20GHz.
- **Our unique advantage**
  1) **The same VGA code setting can achieve the target phase for all frequencies.**
  2) **No need tuning components, code compensation, or frequency-dependent lookup table**

➡ **One-code-for-all frequency solution**

Normalized amplitude and phases at 4GHz

Code (I,Q)	(14,0)	(10,10)	(0,14)	(-10,10)	(-14,0)	(-10,-10)	(0,-14)	(10,-10)
Normalized amplitude	0.93	**0.92**	0.91	0.96	0.87	0.92	0.85	0.96
Phase (°)	0.2	**45.0**	90.7	135.6	179.2	225	271.8	315.9
Phase err. (°)	0.2	**0**	0.7	0.6	0.8	0	1.8	0.9

Normalized amplitude and phases at 10GHz

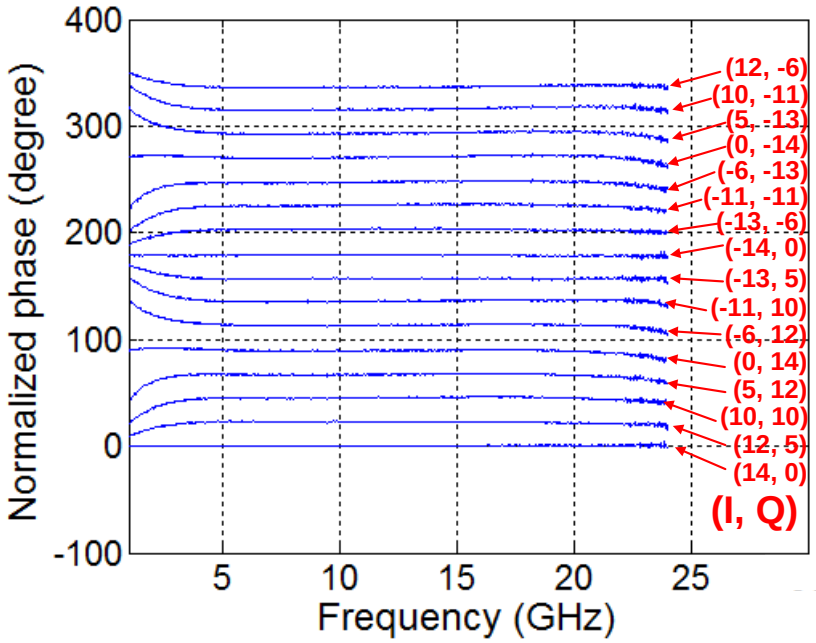
Code (I,Q)	(14,0)	(10,10)	(0,14)	(-10,10)	(-14,0)	(-10,-10)	(0,-14)	(10,-10)
Normalized amplitude	0.94	**0.98**	0.97	0.98	0.89	0.98	0.9	0.99
Phase (°)	0.66	**46.4**	89.3	134.8	180	227	270.8	315
Phase err. (°)	0.66	**1.4**	0.7	0.2	0	2	0.9	0

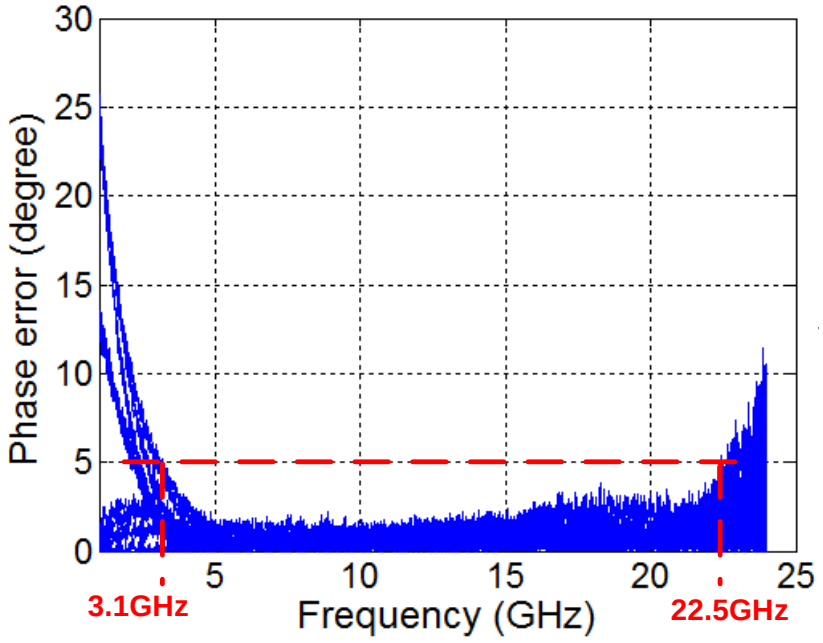
Normalized amplitude and phases at 20GHz

Code (I,Q)	(14,0)	(10,10)	(0,14)	(-10,10)	(-14,0)	(-10,-10)	(0,-14)	(10,-10)
Normalized amplitude	0.93	**0.97**	0.95	0.98	0.88	0.97	0.89	0.98
Phase (°)	0.4	**44.5**	87.3	134	178.2	225	271	314.9
Phase err. (°)	0.4	**0.5**	0.7	1	0.8	0	1	0.1

Measurement

Measurement results





- Measured normalized phase from 0.1GHz to 24GHz with constant I/Q control codes for phase interpolation with 22.5° step.
- I/Q VGA control codes are kept constant over the frequency and the intrinsic delay of the phase rotator is removed.
- Max phase error ≤ 5° for 3.1GHz-22.5GHz, **achieving a broadband operation without any tuning components, code compensation, or frequency-dependent look-up tables.**

Comparison Table

	K. Koh JSSC, 2007	J. Park RFIC, 2014	S. Sah TMTT, 2014	This Work
Frequency range (GHz)	5-18 (1:3.6) 15-26 (1:1.73)	20-27 (1:1.35)	15-35 (1:2.3)	**2-24 (1:12)**
Resolution (bit)	8	10	8	**10**
RMS phase error (degree)	<10 6.5-13	<2	<6.38	**<1.22**
Magnitude tolerance (dB)	2.4 3.5	1.5	2	**1.5**
Quadrature generation type	Quadrature All-pass filter	Folded transformer quadrature generation	RC-CR poly- phase filter + inductor	**Transformer-poly-phase network**
Look-up table or code compensation	Yes	Yes	-	**No**
Technology	130nm CMOS	90nm BiCMOS	180nm BiCMOS	**65nm CMOS**

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Conclusion

- I/Q vector modulator phase rotator with 3-stage transformer poly-phase network achieves world first decade instantaneous bandwidth.
- Measured 961 phase interpolation points demonstrate high precision I/Q magnitude/phase balance and good I/Q VGA matching.
- Within 1.5dB magnitude variation, measured RMS phase quantization errors <1.22° for 360° full-span interpolation from 2GHz to 24GHz are achieved.
- Our phase rotator don't require frequency tuning elements, band selection switches, frequency-dependent code compensation, or frequency-dependent look-up tables.

Acknowledgment

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- The authors would like to acknowledge Toshiba Corporation for chip fabrication.

- The authors also thank members of Georgia Tech Electronics and Micro-System Lab (GEMS) for technical discussions and design support.