

CICC 2015

Session 4.3

# **A 3.9 mW, 35-44 / 41-59.5 GHz Distributed Injection-Locked Frequency Divider**

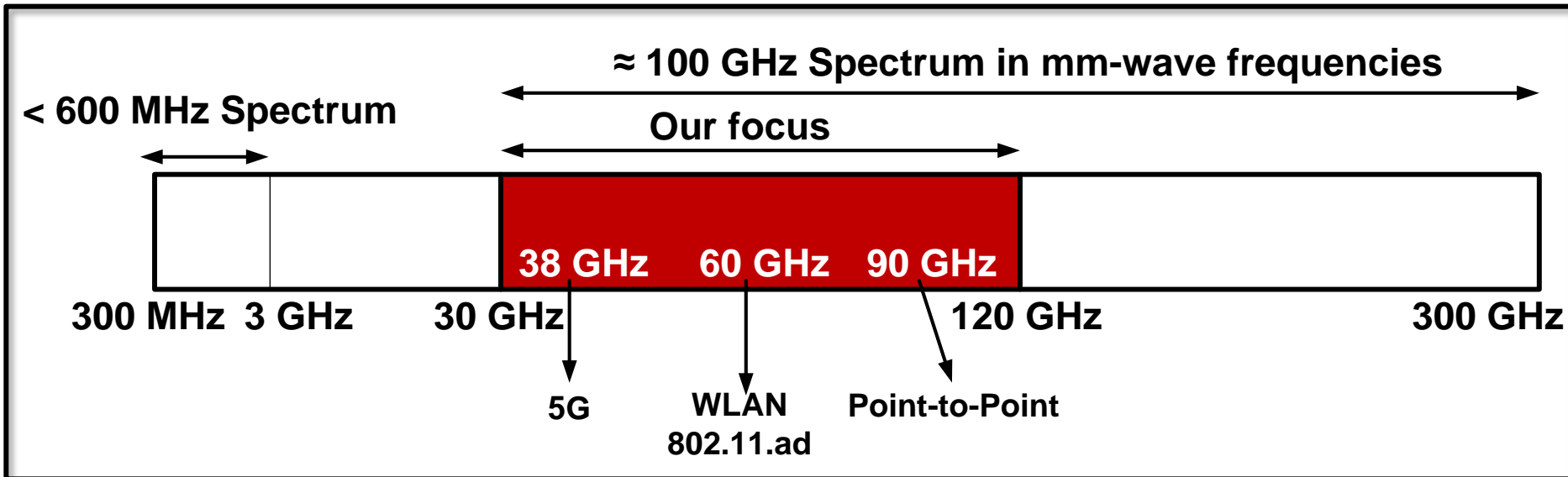
Alireza Imani and Hossein Hashemi

*University of Southern California*

# Outline

- Motivation
- Concept
- Implementation
- Conclusion

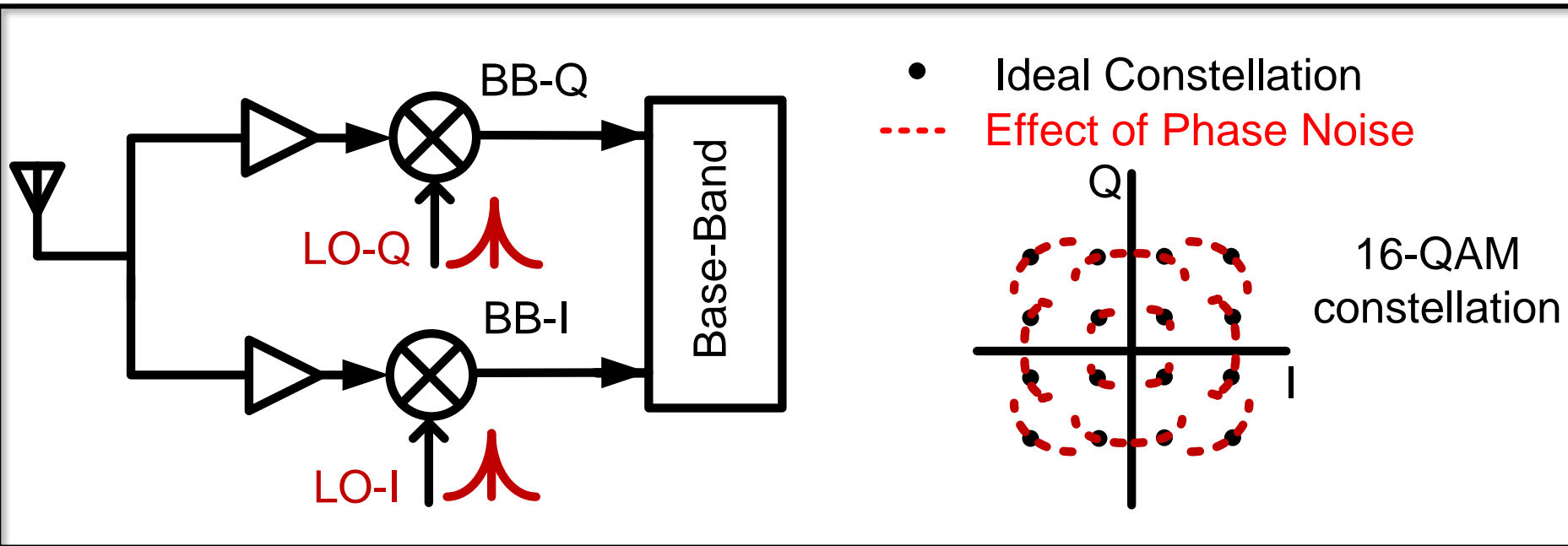
# Motivation: mm-Wave SDR



- ✓ Demand for higher data-rates
- ✓ Interference tolerance through beam-forming

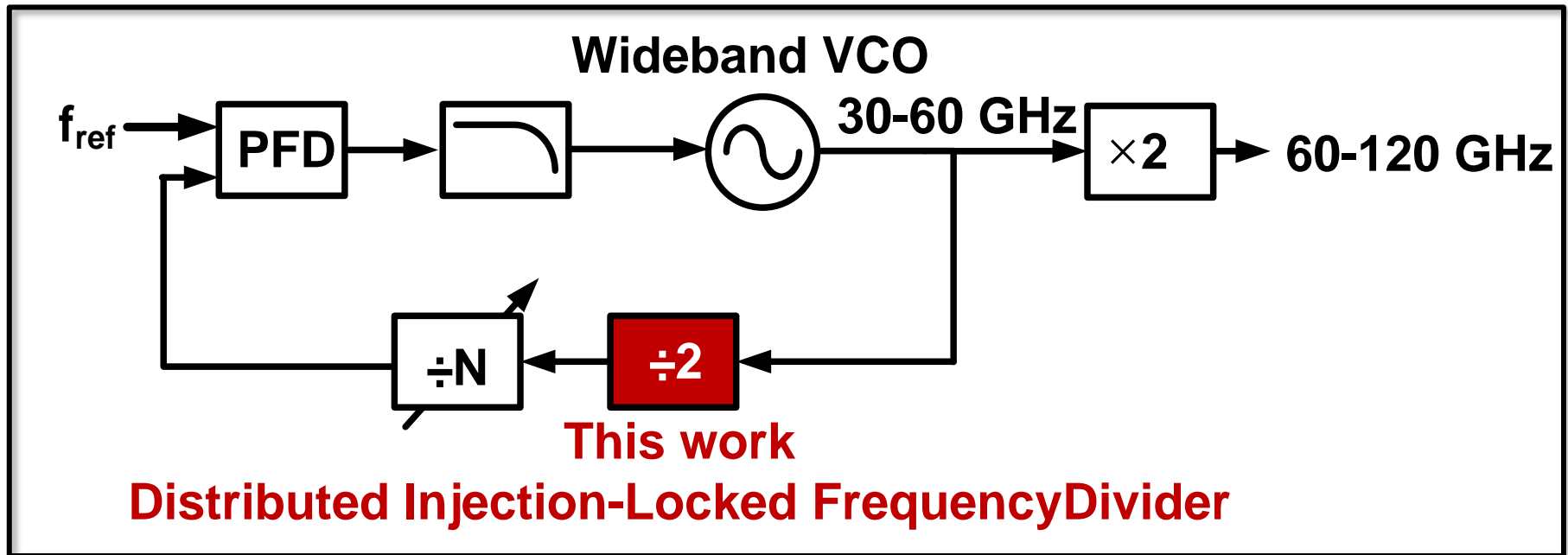
**mm-wave Software Defined Radio is a meaningful proposition.**

# Frequency Synthesizer in SDR



**High-data-rate spectrally-efficient mm-wave Software Defined Radio requires low phase- noise wideband frequency synthesizer.**

# Proposed mm-Wave Wideband Frequency Synthesizer

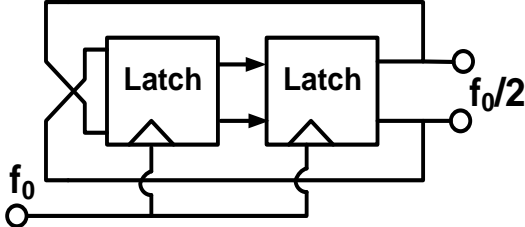
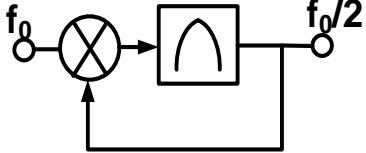
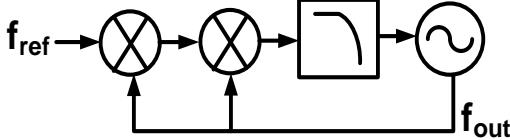
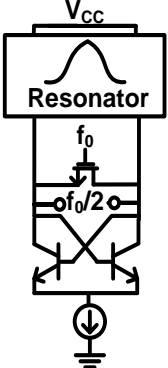


The frequency synthesizer architecture and frequency planning is chosen to minimize power consumption considering transistor  $f_{\text{max}}$ , phase noise of  $f_{\text{ref}}$ , etc.

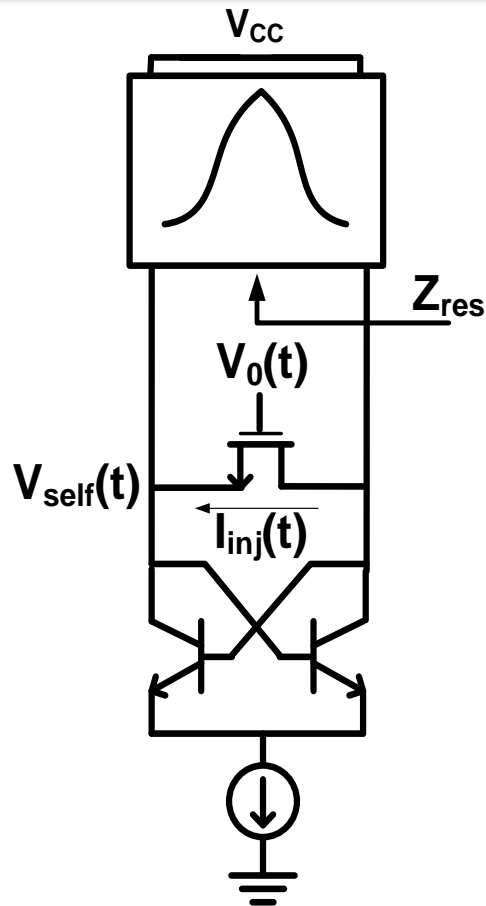
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# Frequency Divider Topologies

Type	Schematic	Area	Locking Range	Max Frequency	Power
Flip-Flop Based		Smallest	<b>Widest</b>	Low	Frequency Dependent
Miller		Medium	Narrow	High	Medium
Heterodyne PLL		Small	Medium	High	High
Injection Locked		Medium	Narrow	<b>Highest</b>	Low

# Injection Locked Frequency Divider



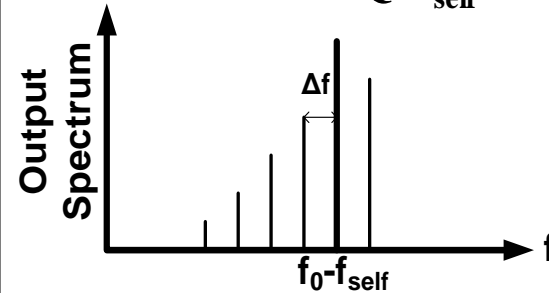
$$V_0(t) = a_0(t) \sin(\omega_0 t + \theta)$$

$$V_{\text{self}}(t) = a_{\text{self}}(t) \sin(\omega_{\text{self}} t + \theta)$$

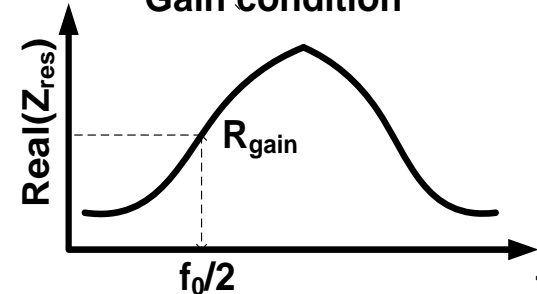
$$\omega_0 = 2\omega_{\text{self}} + \Delta\omega$$

Adler Phase Condition

$$\frac{d\theta}{dt} = \omega_{\text{self}} - \frac{\omega_0}{2} - \frac{\omega_{\text{self}}}{2Q} \frac{\alpha V_0}{V_{\text{self}}} \sin(\theta)$$



Gain condition



$$\text{Real}\left(Z_{\text{res}}\left(\frac{f_0}{2}\right)\right) = R_{\text{gain}} < \frac{2}{g_m}$$

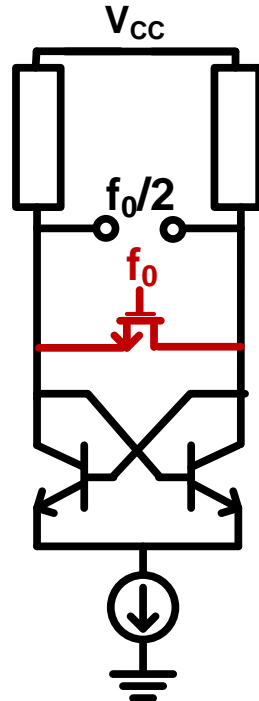
$$g_m = f(V_0)$$

Oscillation dies!

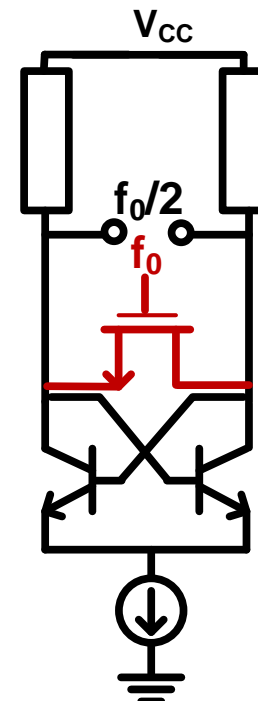


# Injection Locked Frequency Divider

## Locking Range



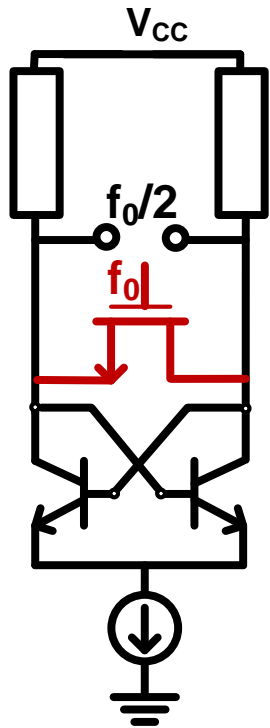
Small injection device:  
✗ Limited Locking range  $\propto I_{inj}/Q$   
(Adler phase condition)



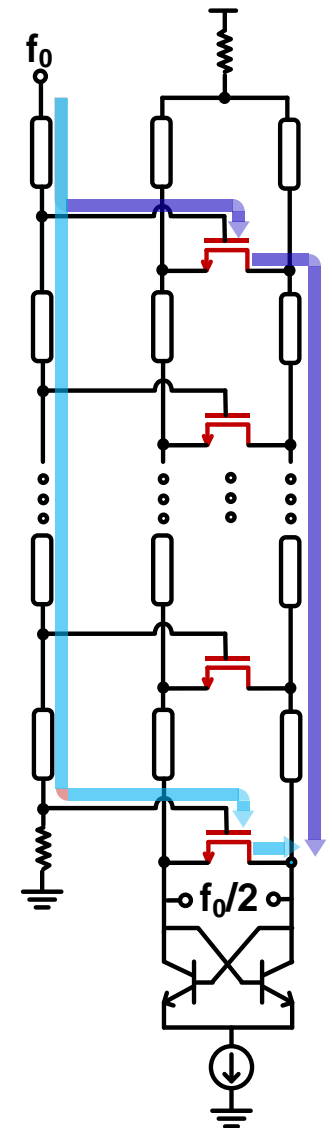
Large injection device: Small  $R_{on}$   
✗ Prevent oscillation start-up  
(Gain condition)

The trade-off limits locking range for a given power consumption.

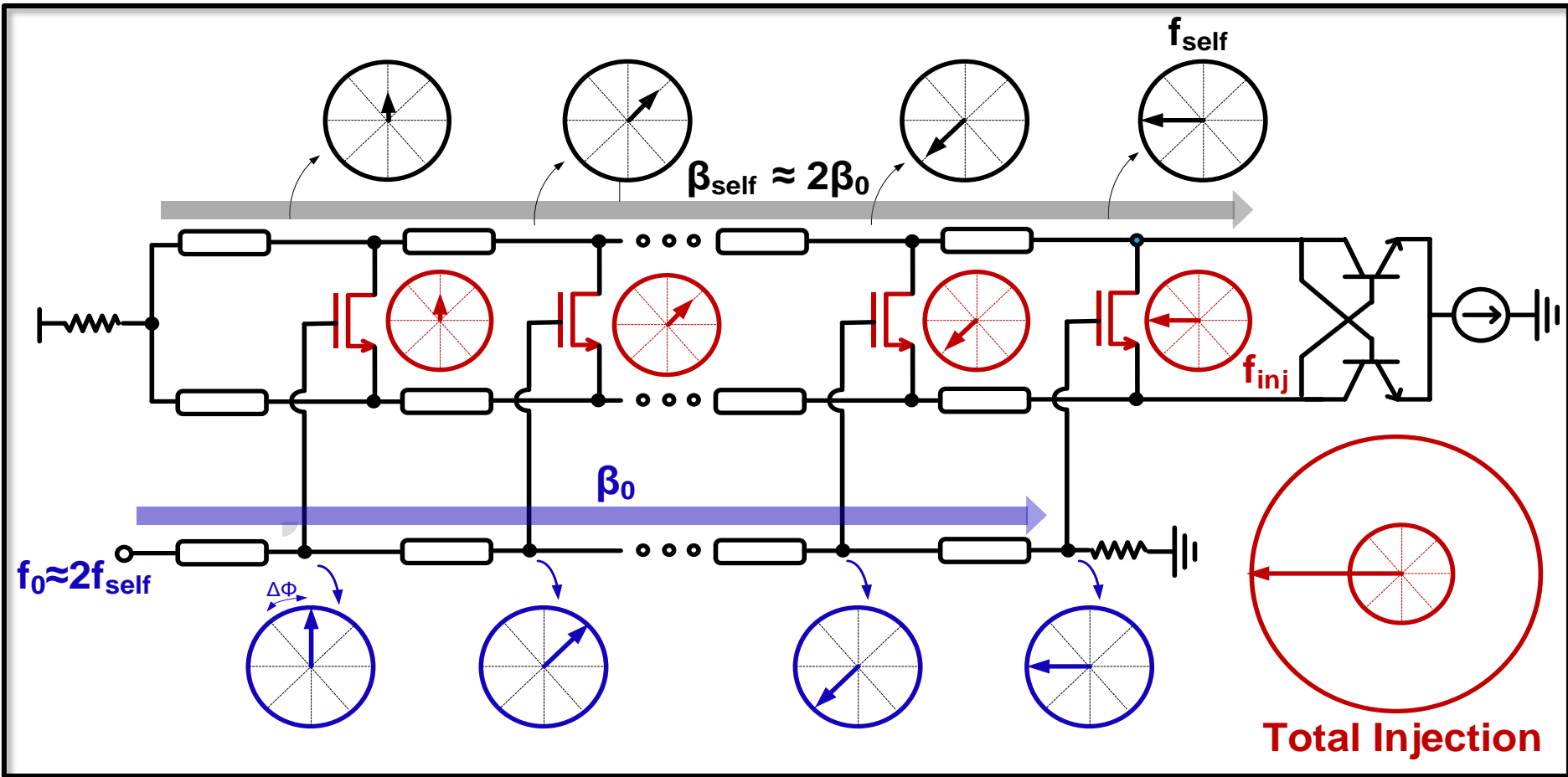
# Distributed Injection Locking



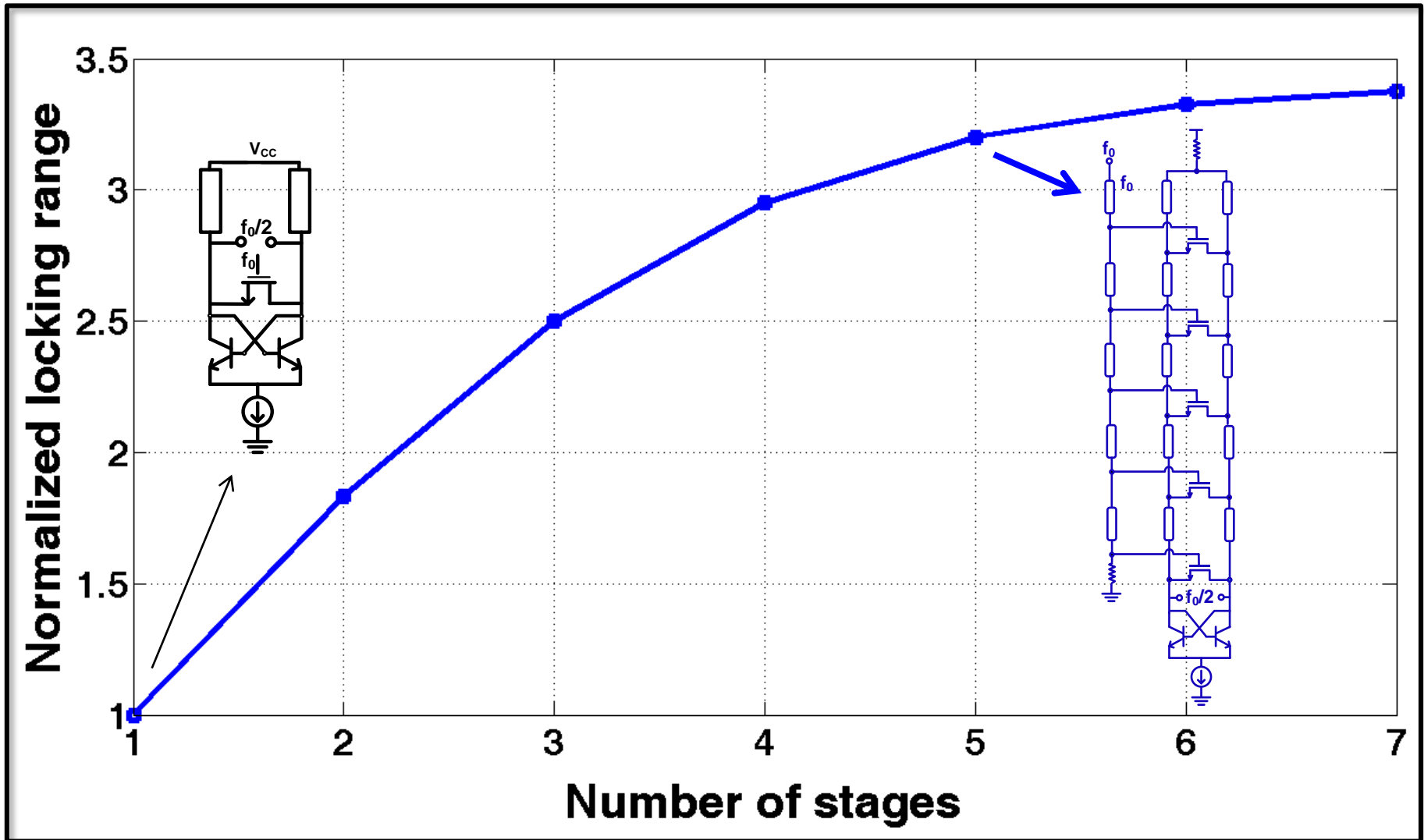
- ✓ Smaller switches with strong injection
- ✓ Wide locking range.
- ✓ Wideband input matching.



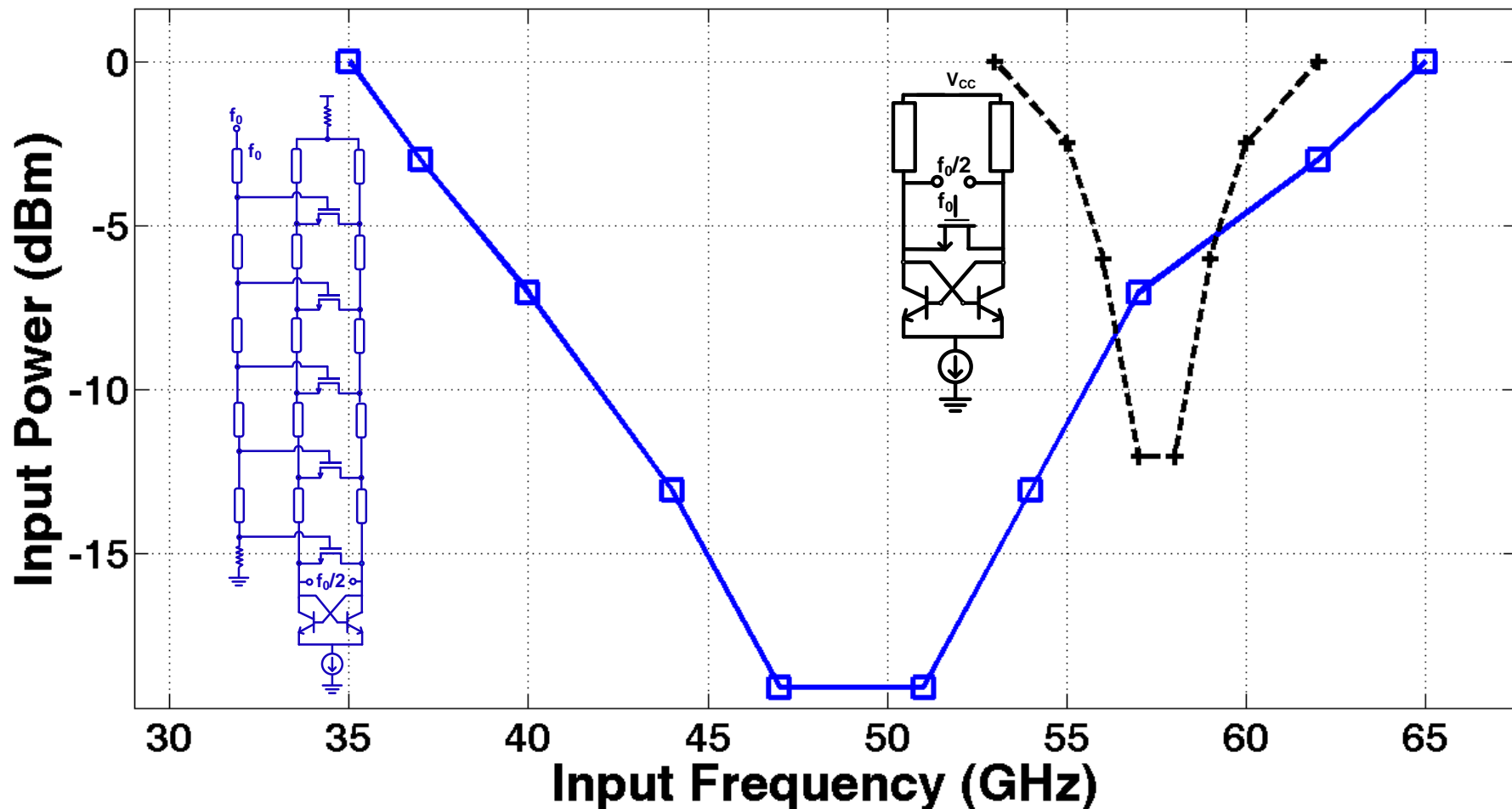
# Operation Principle



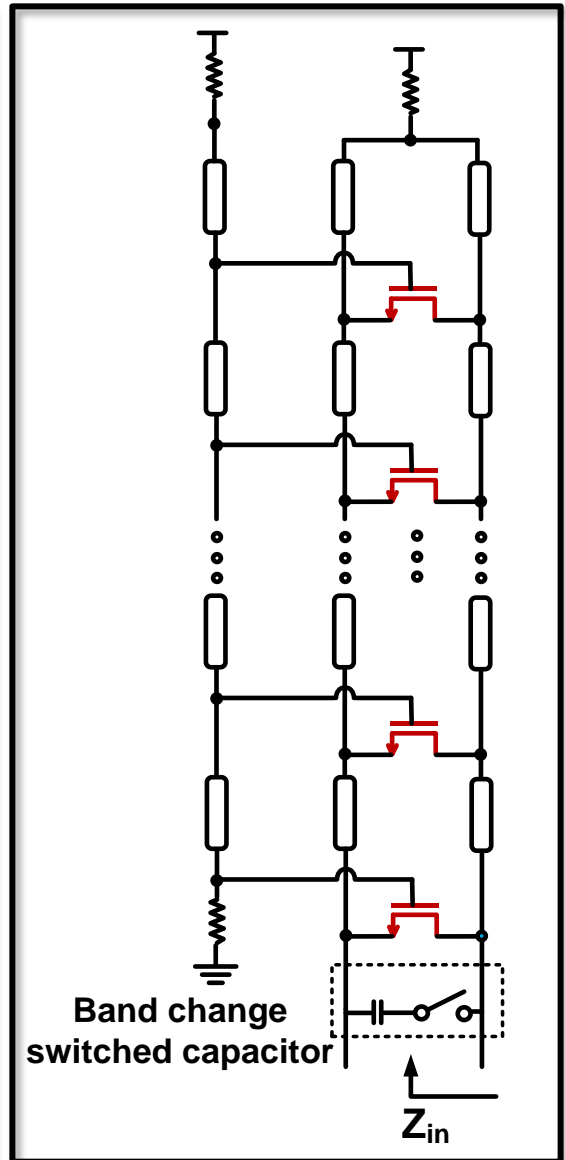
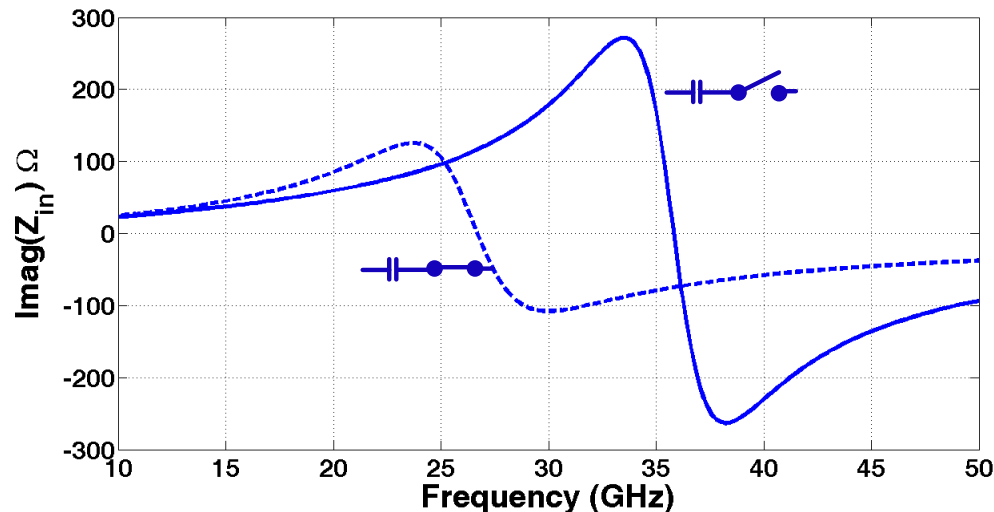
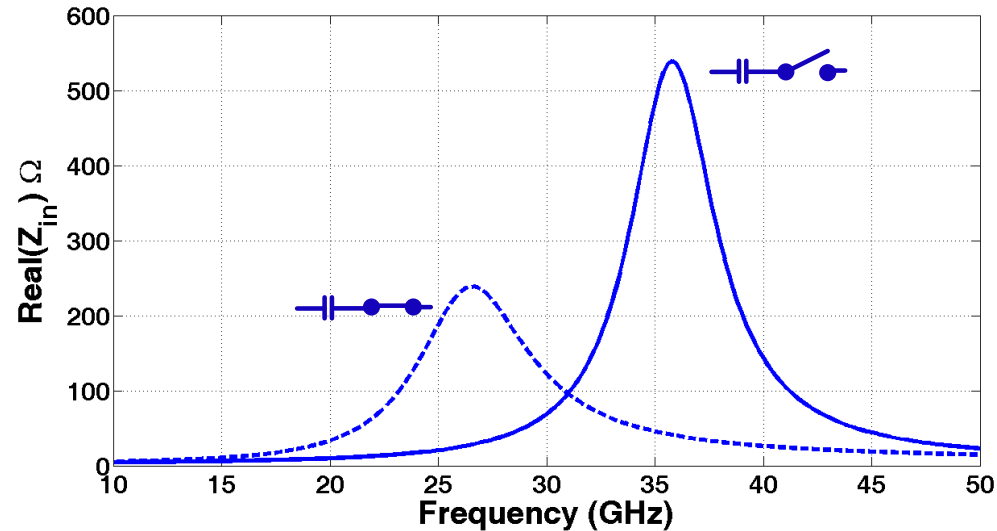
# Optimum Number of Stages



# Comparison (Simulations)



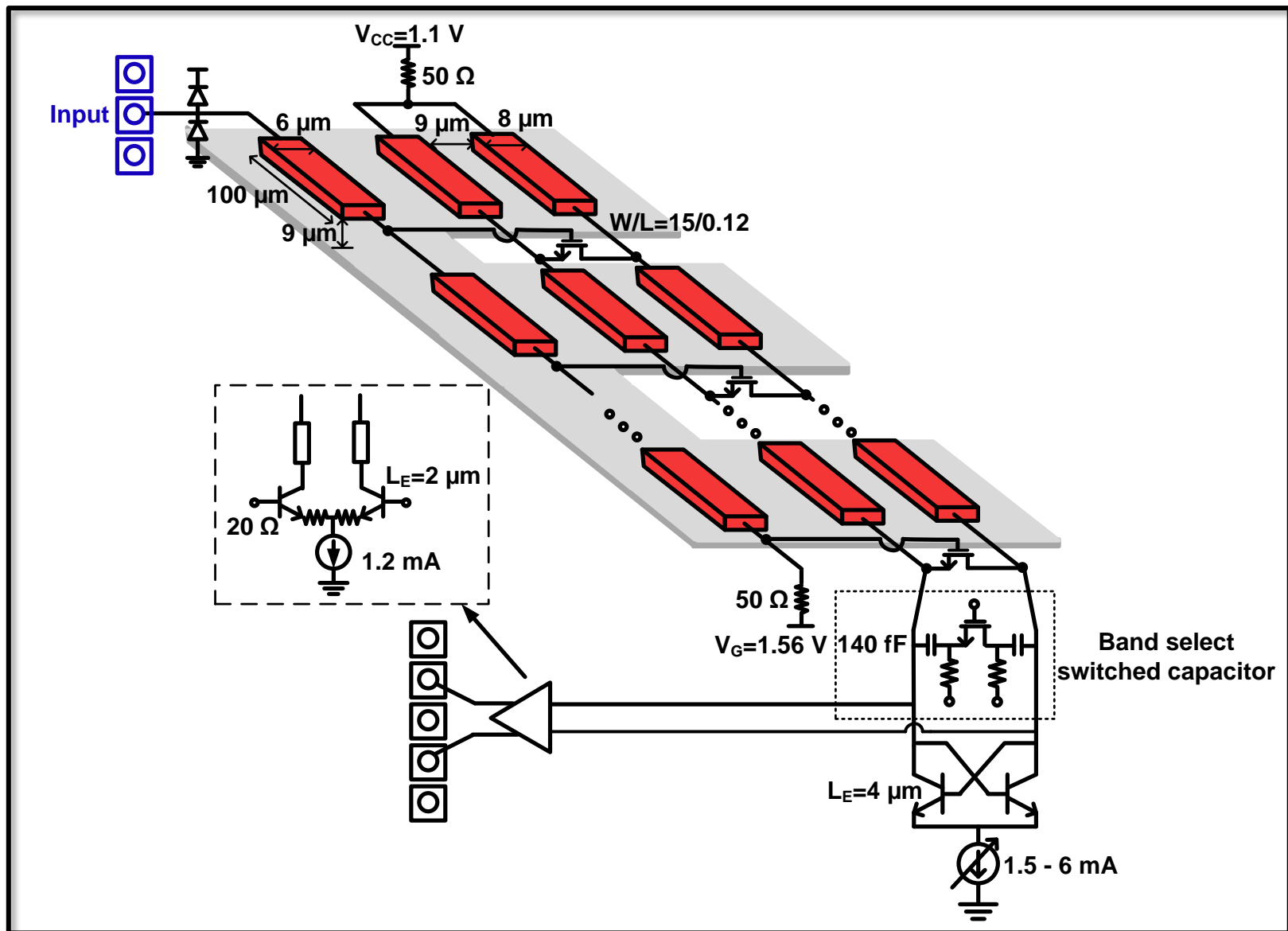
# Load Frequency Shifting



# Outline

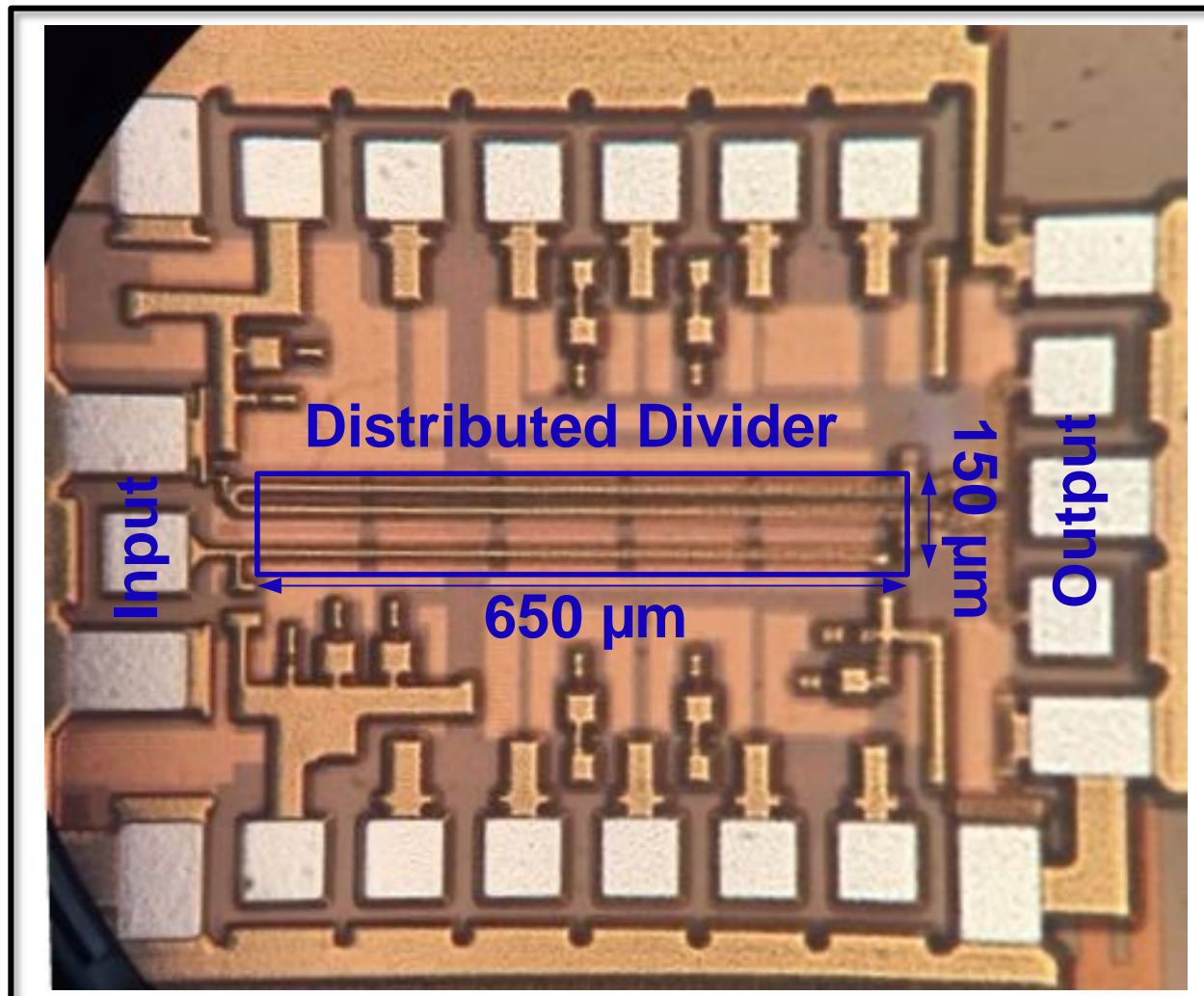
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# Schematics



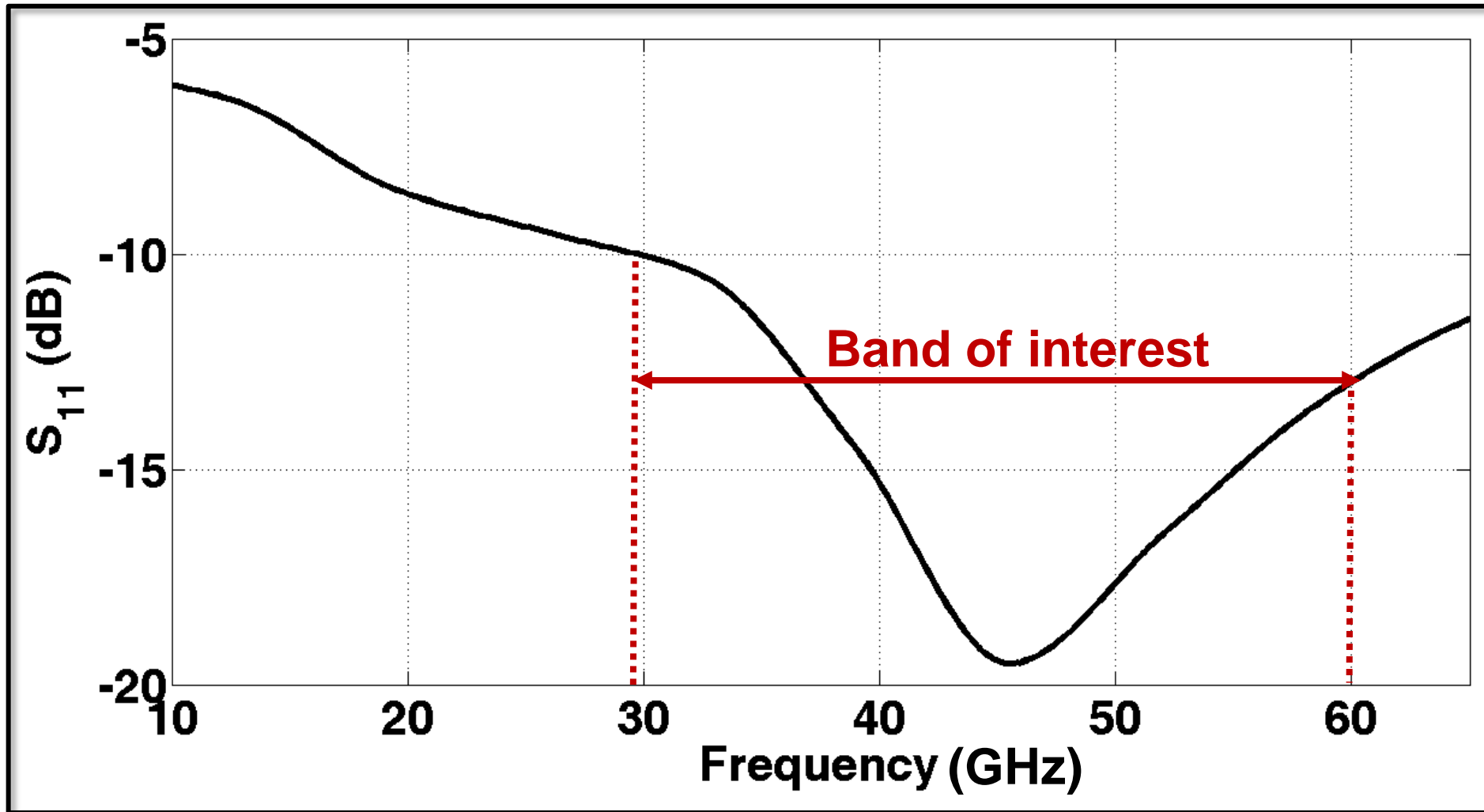


# Chip Micrograph



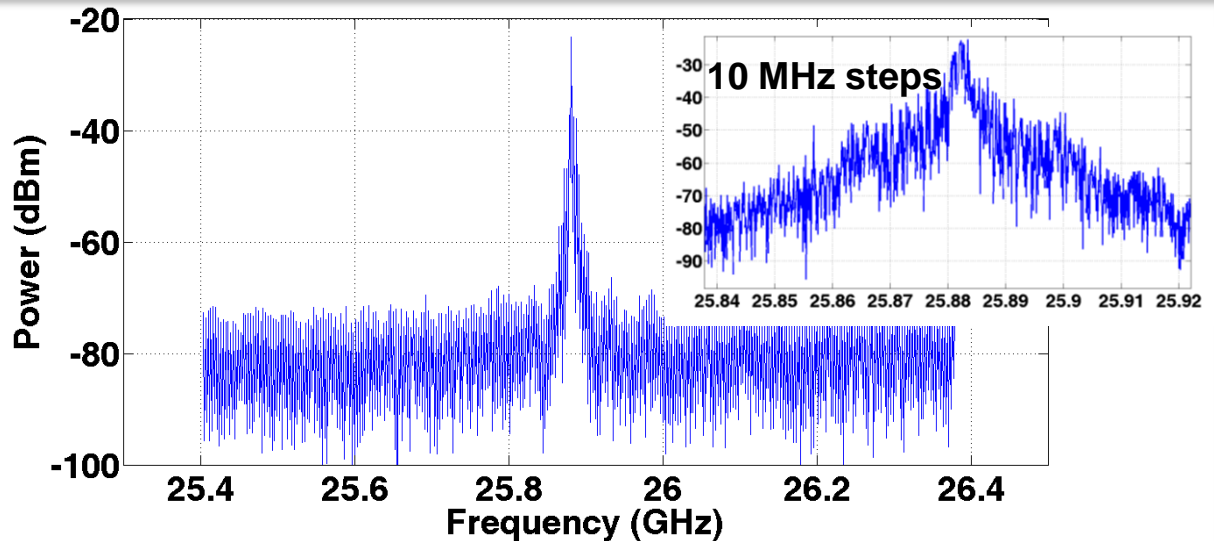
**0.13  $\mu\text{m}$  SiGe BiCMOS (IBM 8HP)**

# Input Reflection Coefficient

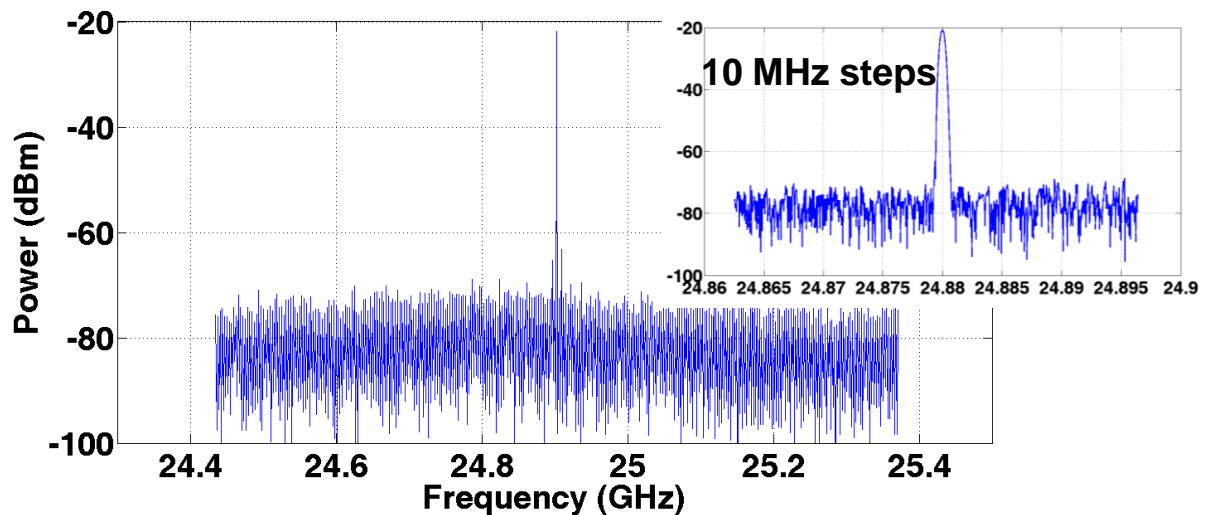


# Output Spectrum

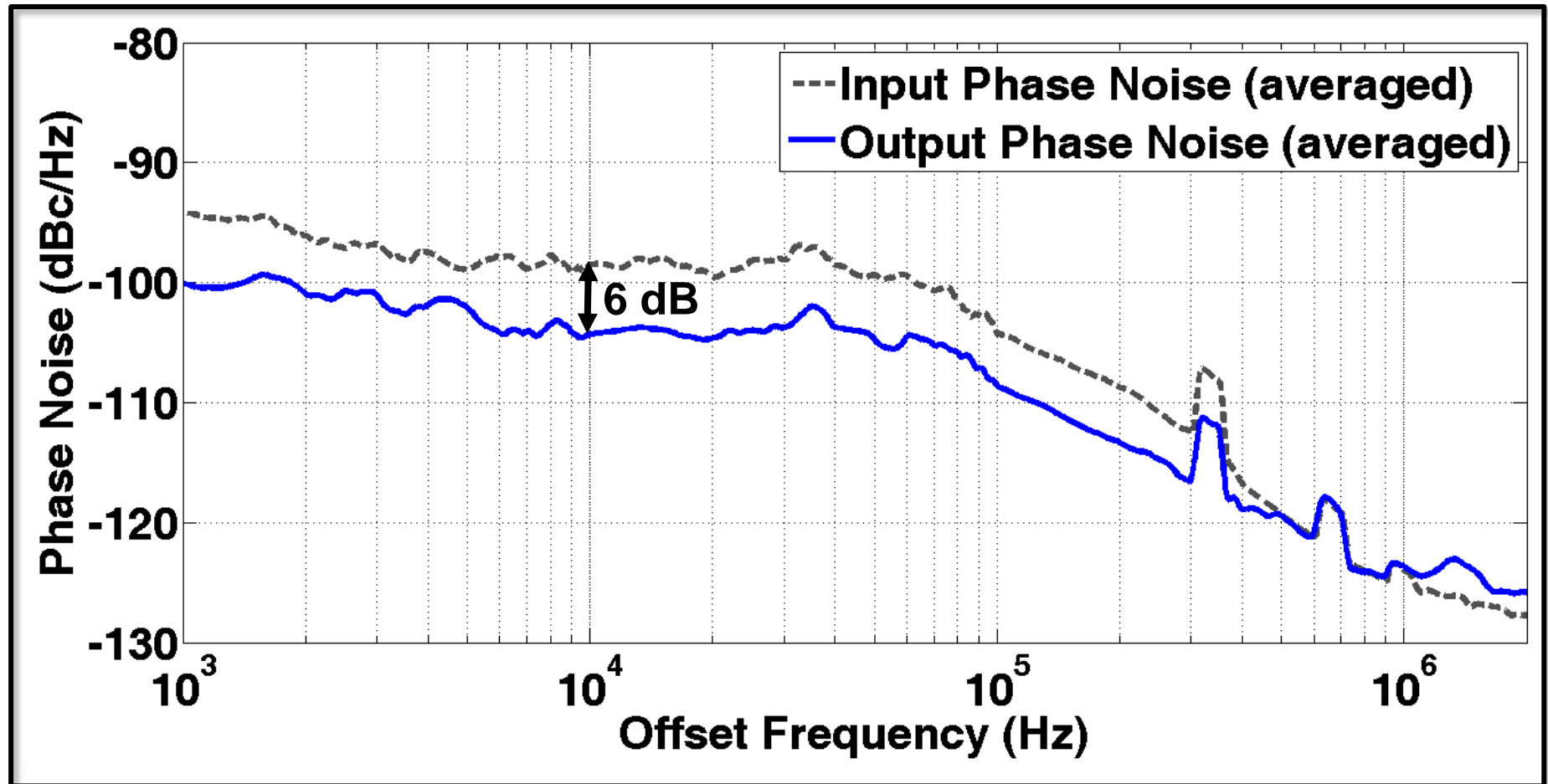
## Self-Oscillation



## Injection-Locked

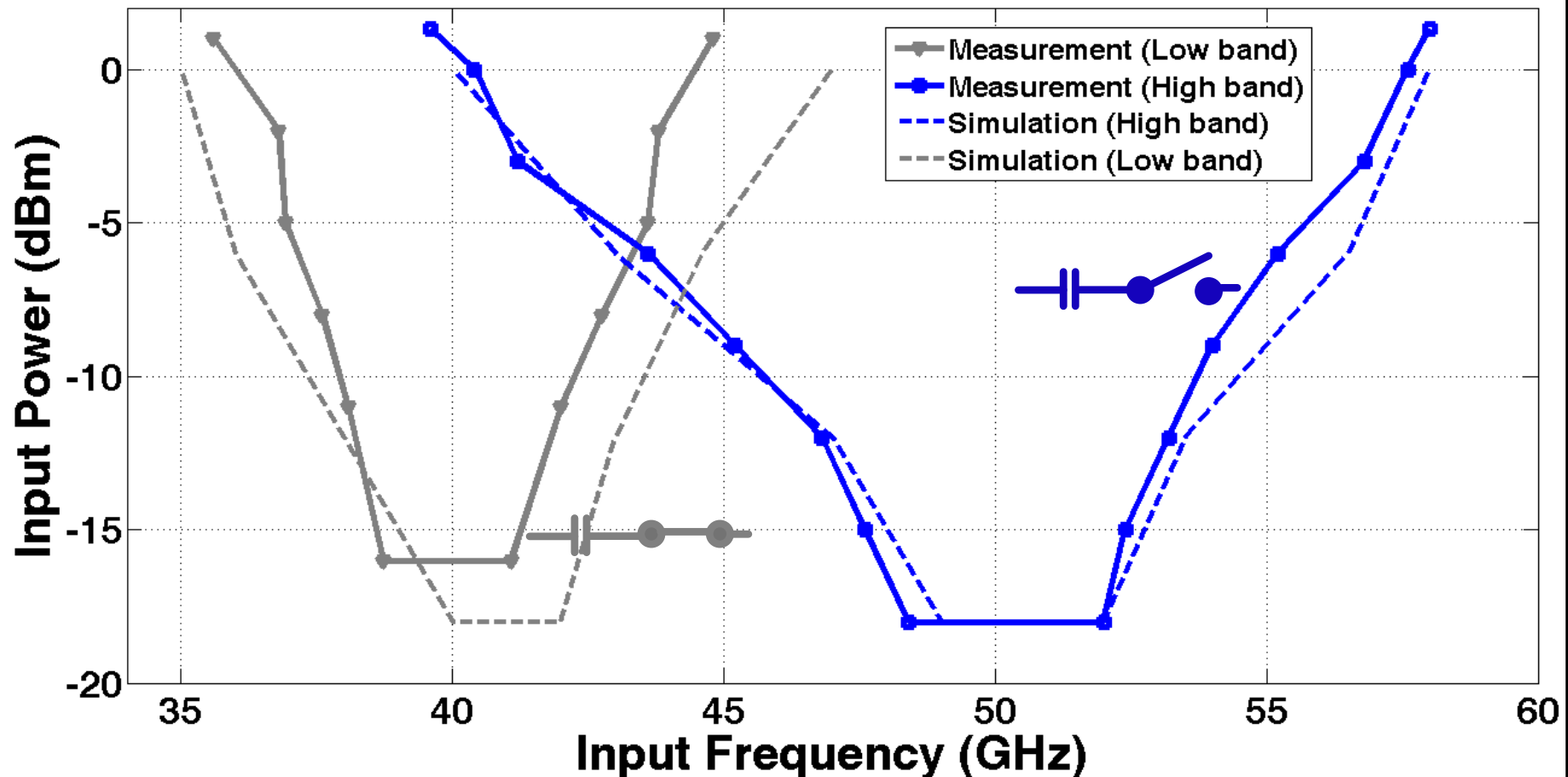


# Measured Locked Phase Noise



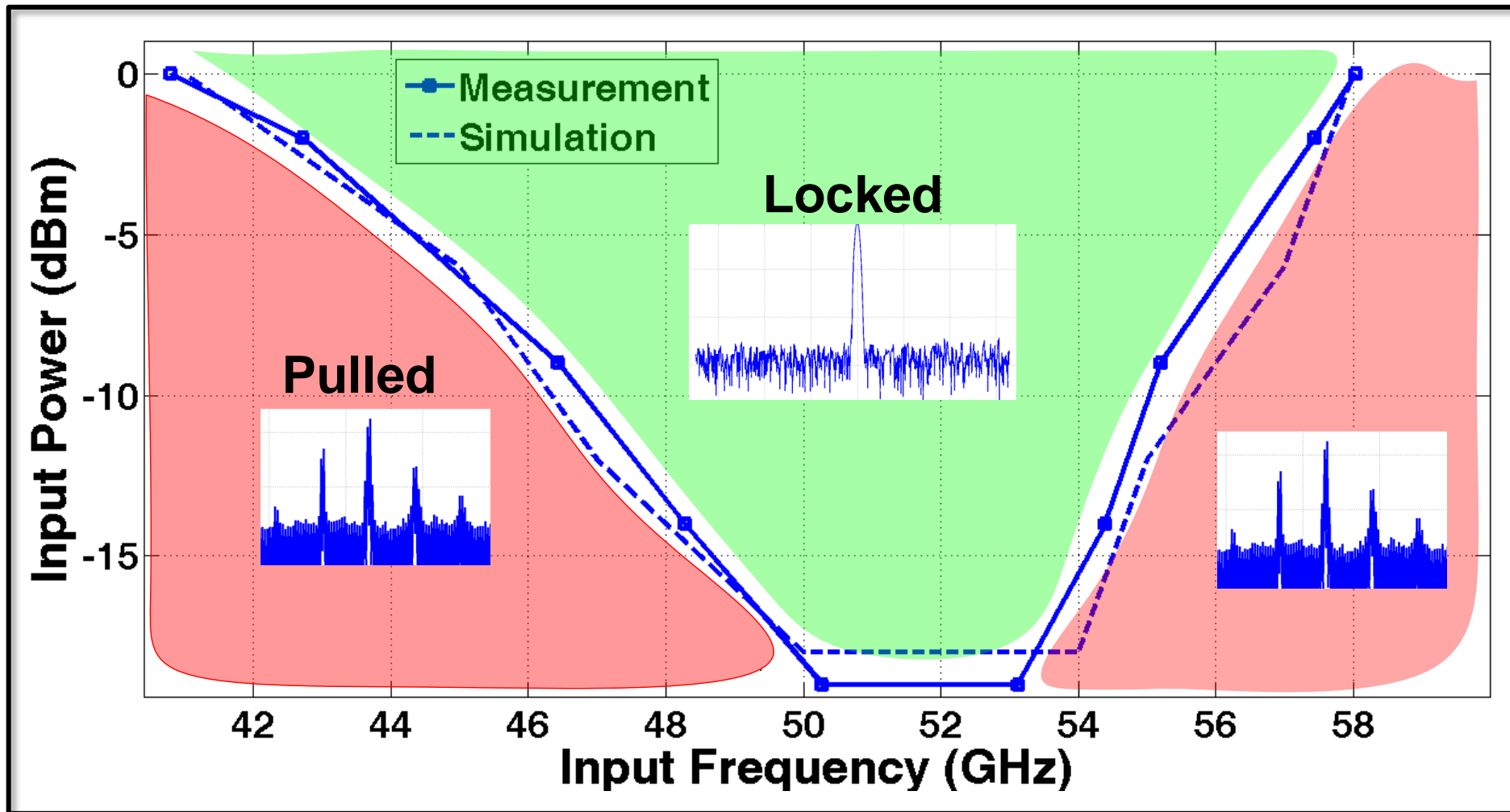
# Sensitivity Curve

( $I_{\text{core}}=4\text{ mA}$ ,  $I_{\text{buf}}=1\text{ mA}$ )



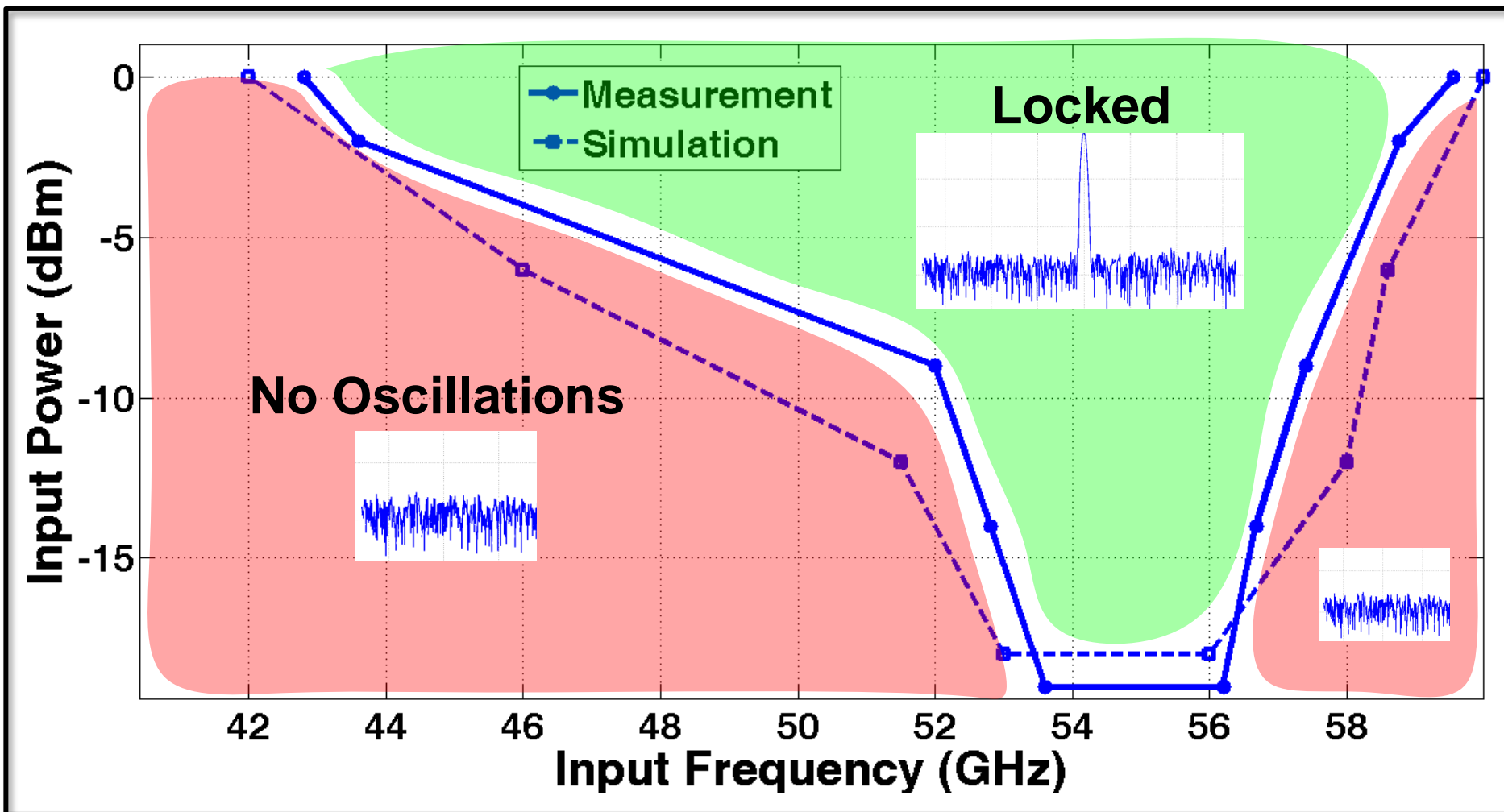
# Sensitivity Curve

( $I_{\text{core}}=5 \text{ mA}$   $I_{\text{buf}}=0.6 \text{ mA}$ )



# Sensitivity Curve

( $I_{\text{core}}=2.5 \text{ mA}$ ,  $I_{\text{buf}}=0.6 \text{ mA}$ )



# Performance Summary

	<b>This Work</b>	<b>ISSCC 2007</b>	<b>ISSCC 2009</b>	<b>JSSC May 2013</b>	<b>RFIC 2012</b>	<b>JSSC October 2013</b>
<b>Technology</b>	<b>0.13 <math>\mu\text{m}</math> BiCMOS</b>	<b>0.18 <math>\mu\text{m}</math> CMOS</b>	<b>0.13 <math>\mu\text{m}</math> CMOS</b>	<b>32nm CMOS</b>	<b>65 nm CMOS</b>	<b>65 nm CMOS</b>
<b>Operation Frequency (GHz)</b>	<b>35 - 44 41 - 60</b>	<b>37.5 - 49</b>	<b>59.6 - 67</b>	<b>40 - 70</b>	<b>53.7 - 72</b>	<b>53.4 - 79</b>
<b>Locking Range</b>	<b>Low band: 22% High band: 37% Total: 53%</b>	<b>26.6%</b>	<b>11.6%</b>	<b>54%</b>	<b>29%</b>	<b>39%</b>
<b>Power Consumption (mW)</b>	<b>3.8</b>	<b>6</b>	<b>1.6</b>	<b>4.8</b>	<b>1.9</b>	<b>2.9</b>
<b>Core Area (mm<sup>2</sup>)</b>	<b>0.07</b>	<b>0.428</b>	<b>0.017</b>	<b>0.001</b>	<b>0.021</b>	<b>0.126</b>
<b>Topology</b>	<b>Distributed IL</b>	<b>Regenerative</b>	<b>Class-B injection</b>	<b>Latch with load modulation</b>	<b>Frequency Tracking</b>	<b>Frequency Tracking</b>



# Conclusion

- Low power wideband low phase noise frequency synthesizer enables mm-wave software defined radio.
- Concept of distributed injection locking is introduced to increase locking range of frequency dividers for a given power consumption.
- Prototype with measured 35-60 GHz locking range was implemented in a 130 nm BiCMOS SiGe HBT technology.

# Acknowledgement

**This work was partially supported by**

- ONR

**Our Thanks to**

- Our group members, USC