Circuit Techniques for Mitigating Short-Term Vth Instability Issues in SAR ADCs

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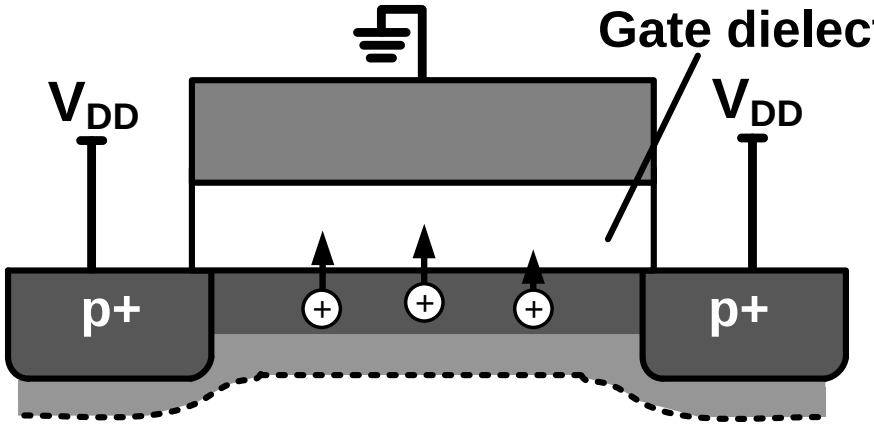
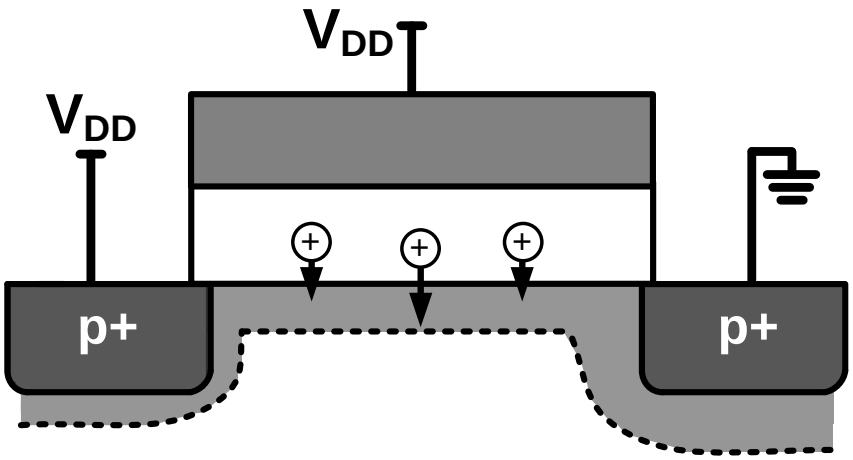
Agenda

- **Impact of Short-term Vth Instability on SAR ADC Operation**
- **Proposed Stress Mitigation Techniques**
- **SAR ADC Test-chip Measurement Results**
- **Conclusions**

Intro to Bias Temperature Instability (BTI)



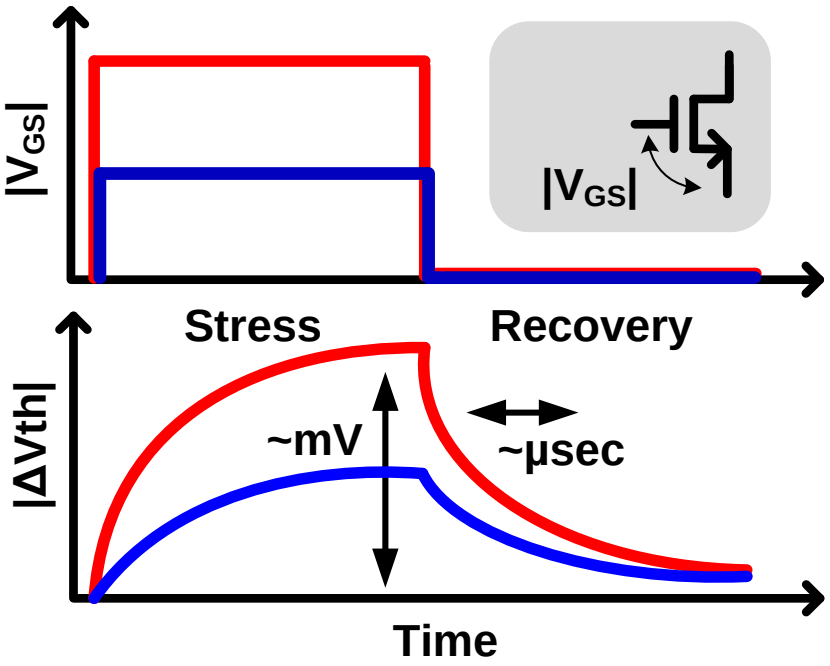


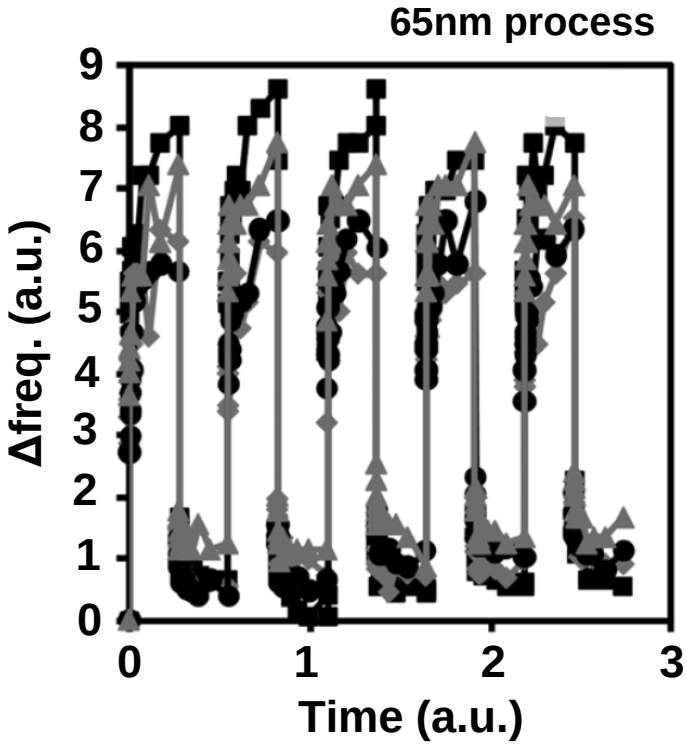
Stress (on-state)

Recovery (off-state)

- **Channel carriers interact with interface bonds and get captured in dielectric or interface**
- **Manifests as increase in |Vth| with time**
- **Partially recovers when FET is turned off**

Short-term Vth Instability due to BTI

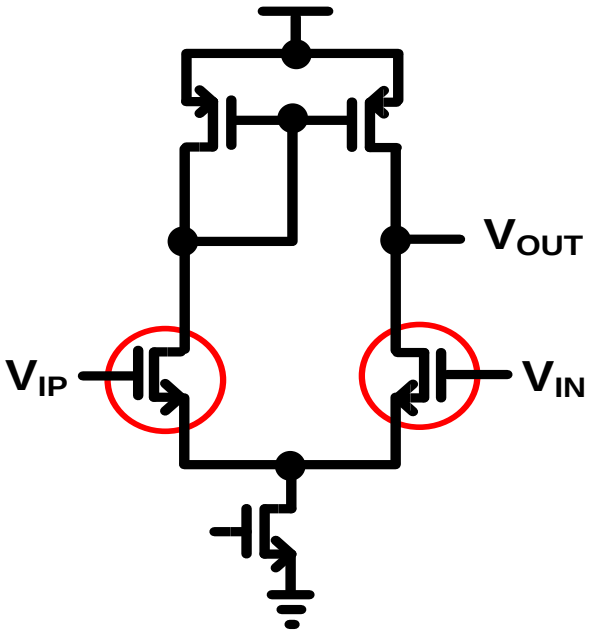




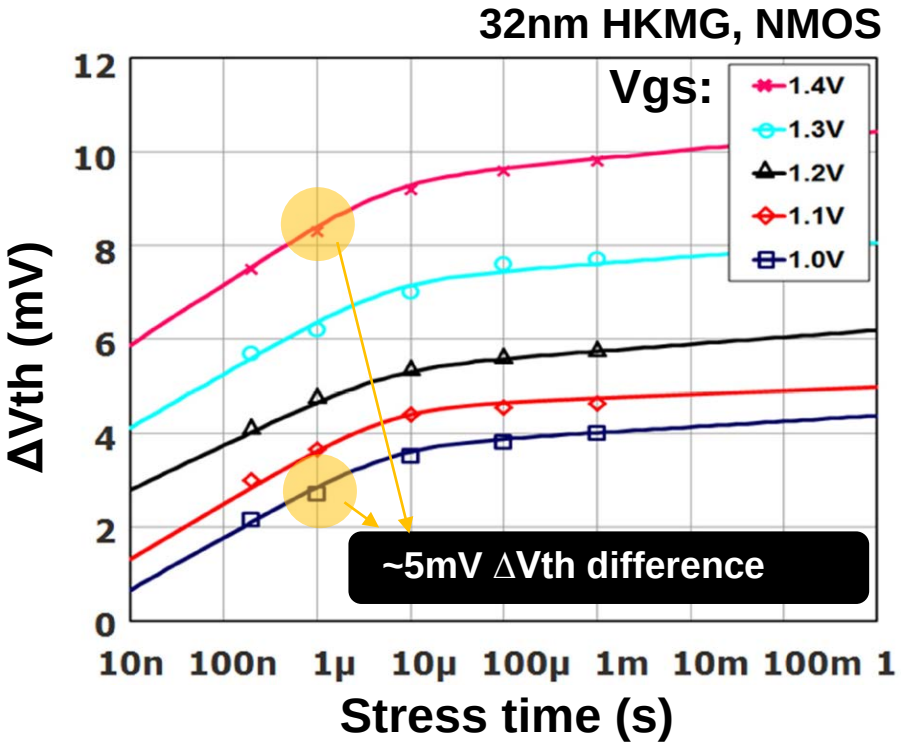
J. Keane, *et al.,* JSSC, 2011.

- **Short-term Vth degradation and recovery occur due to the BTI**
- **The amount of Vth shift depends on the stress voltage and stress time**

Impact on Comparator Circuit



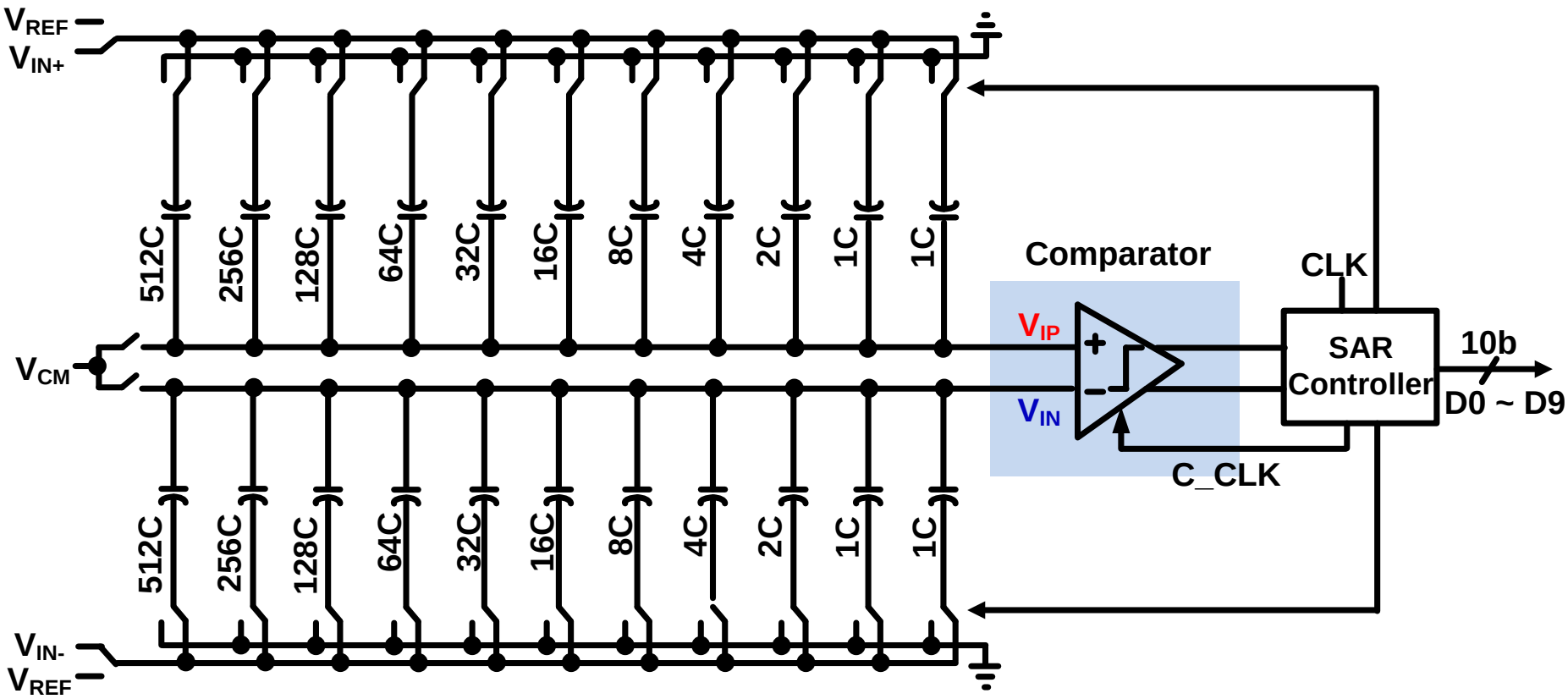
Stress-induced input offset



K. Rott, *et al.,* IIRW, 2012.

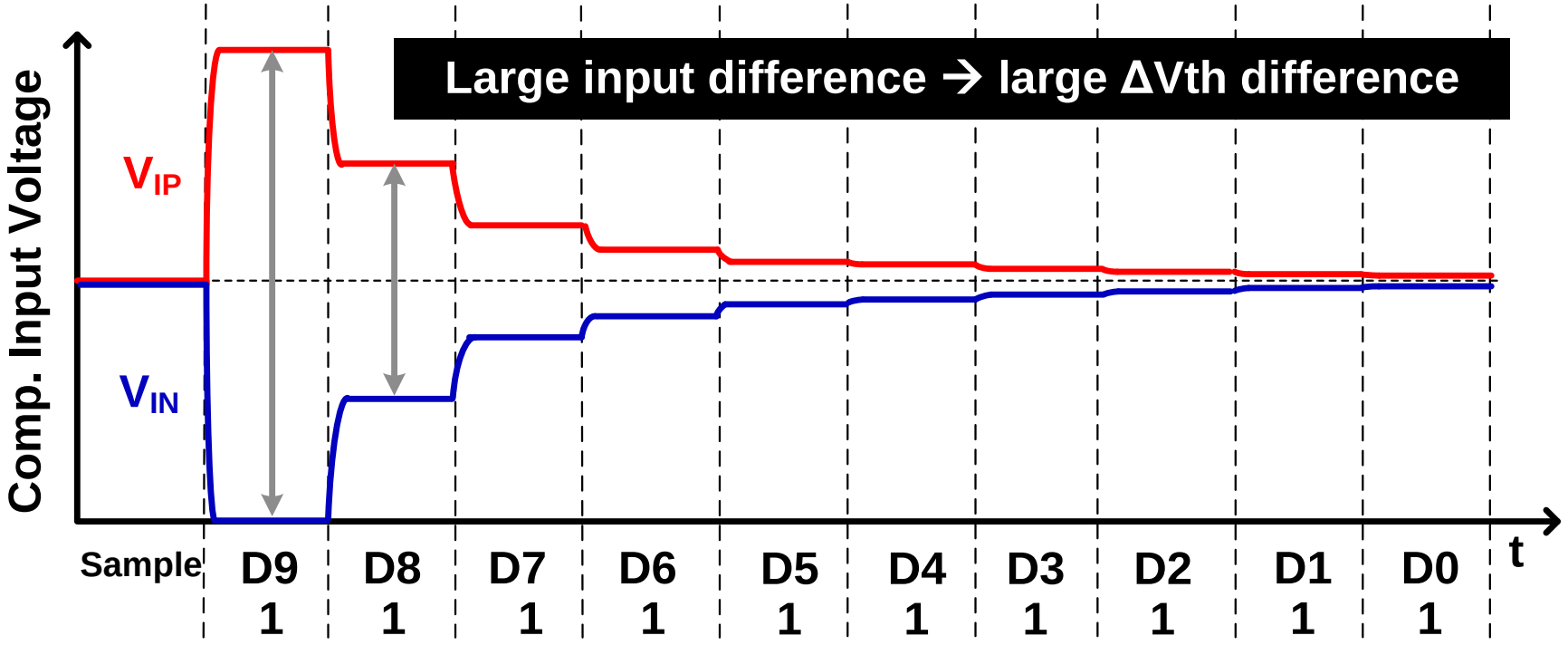
- **Asymmetric input voltage → asymmetric time-dependent Vth shift between input transistors → time-dependant input offset**

Case Study: 10-bit SAR ADC



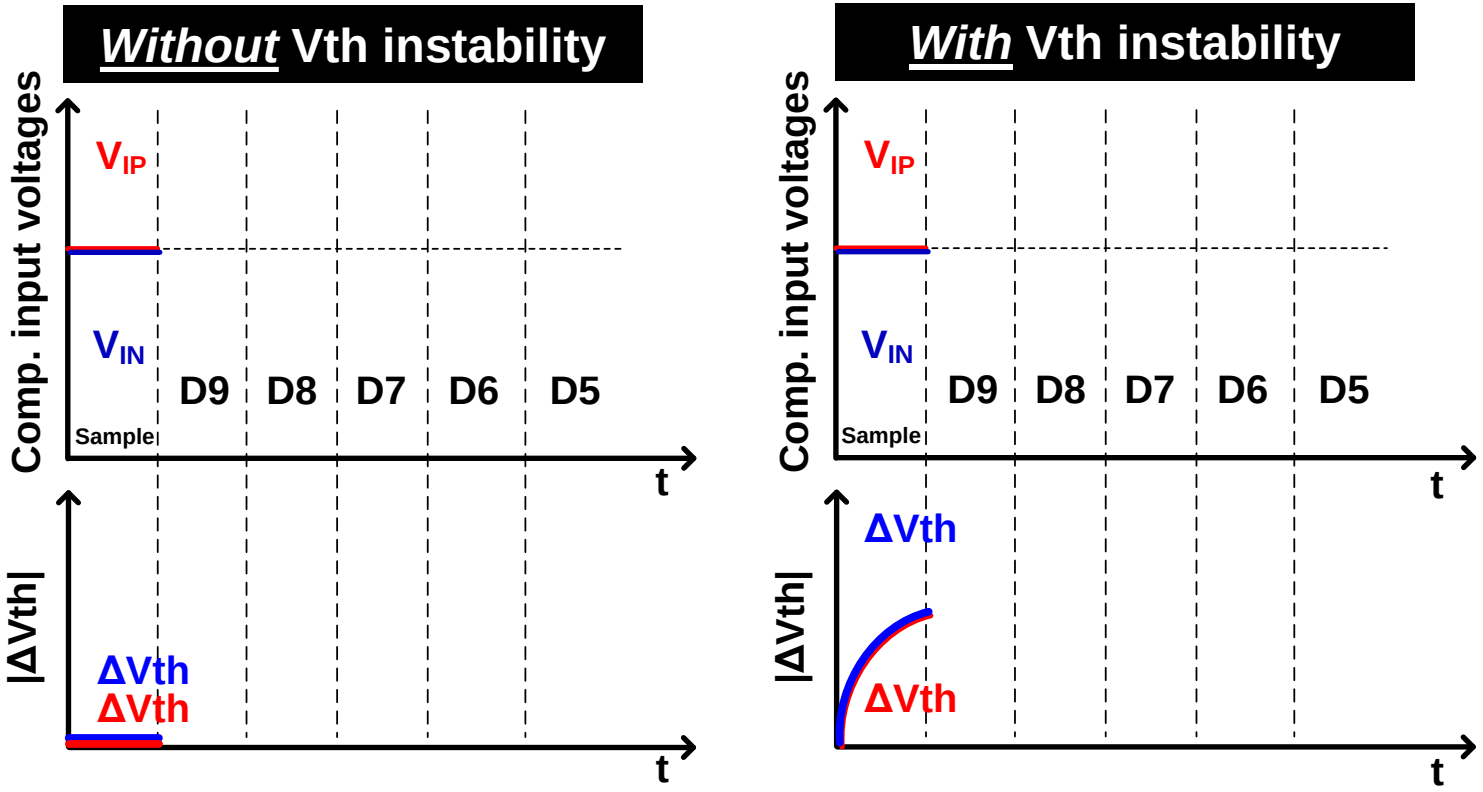
- **Stress-induced input offset of the comparator may degrade the resolution of a Successive Approximation Register (SAR) ADC**

Charge-redistribution based SAR-ADC



- **Large voltage difference in the comparator inputs during the initial SAR conversion steps causes stress-induced comparator offset**

Short-term Vth Instability during SAR Operation



- A 10-bit SAR ADC case study with and without short-term Vth instability
- PMOS-input comparator used for the case study

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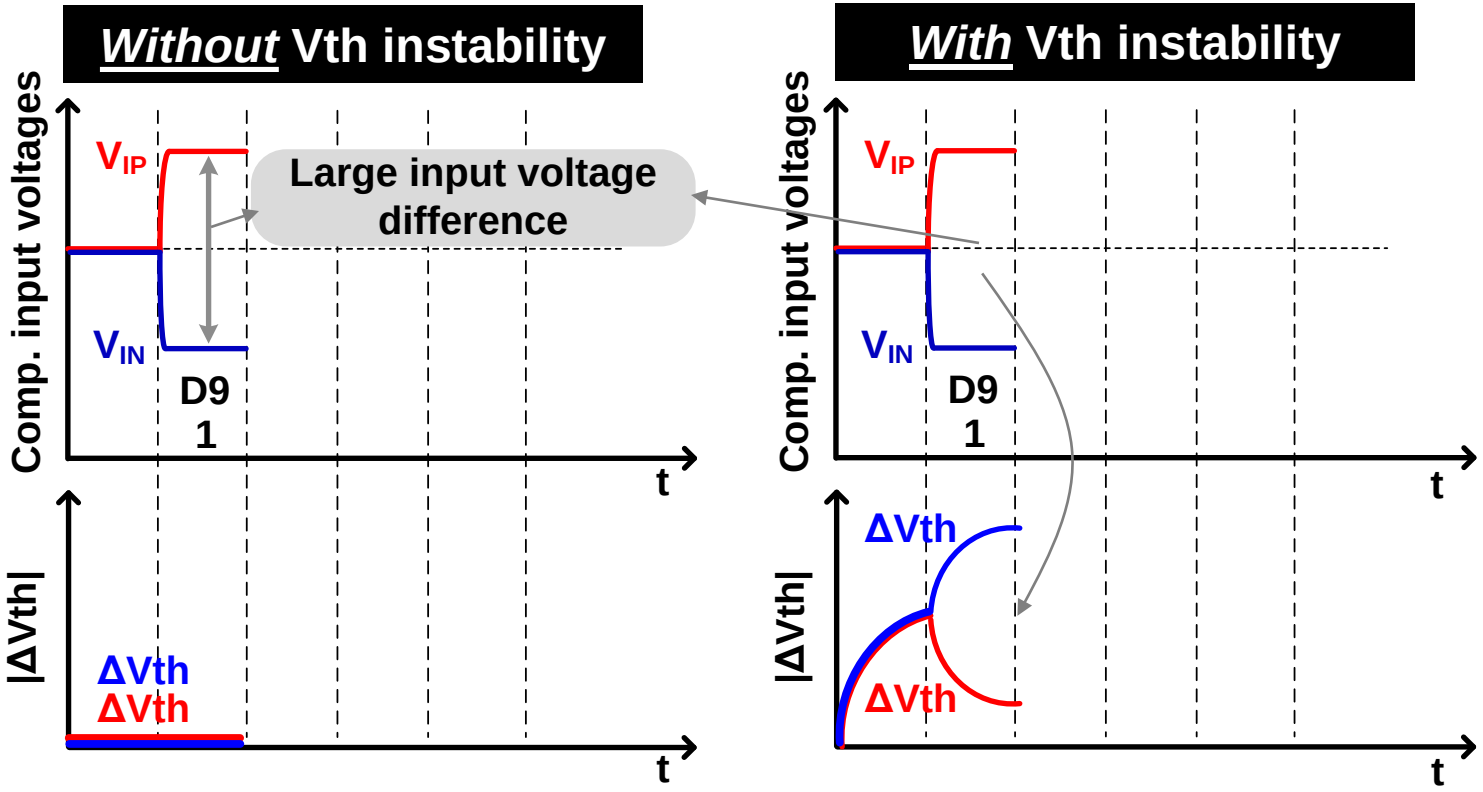
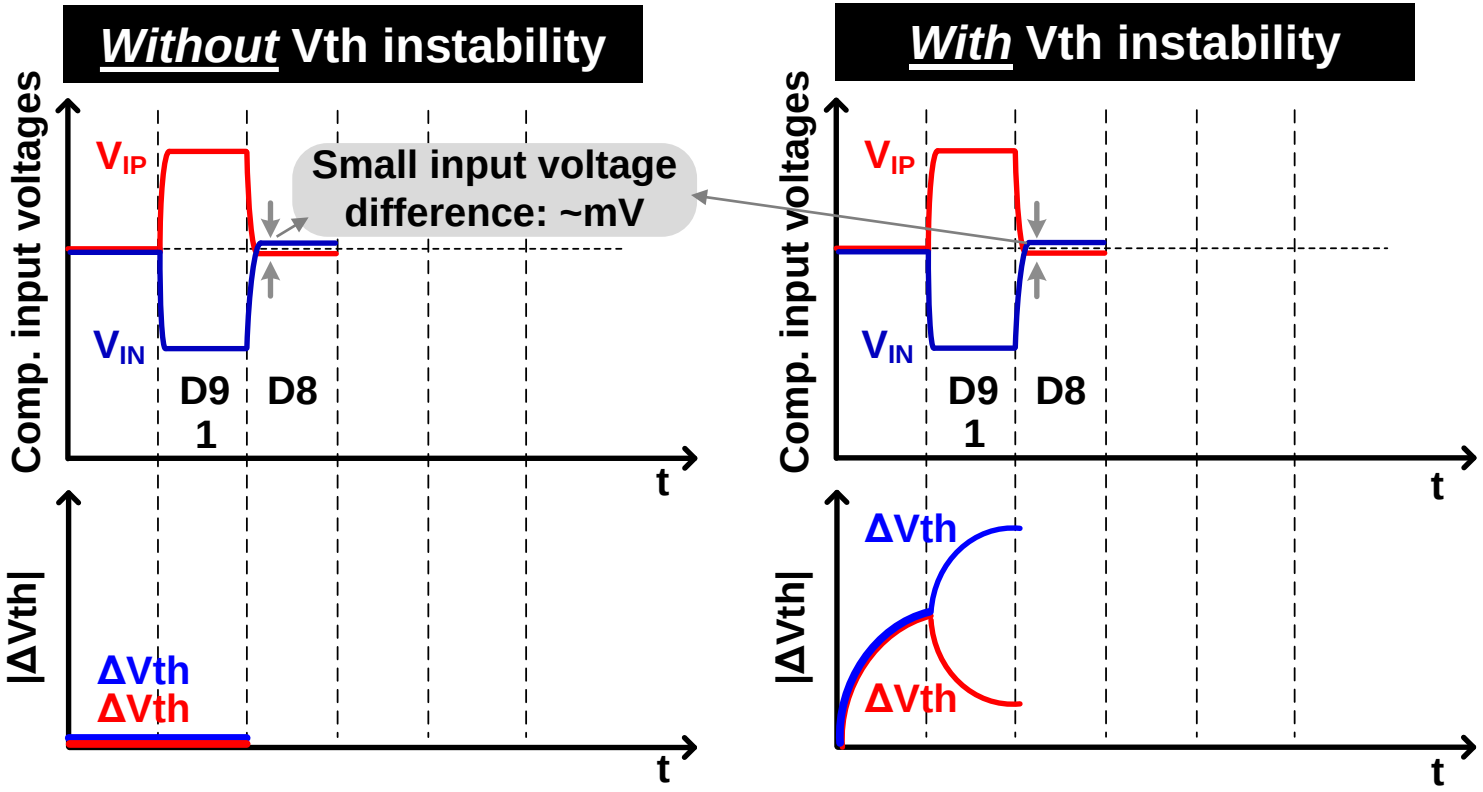


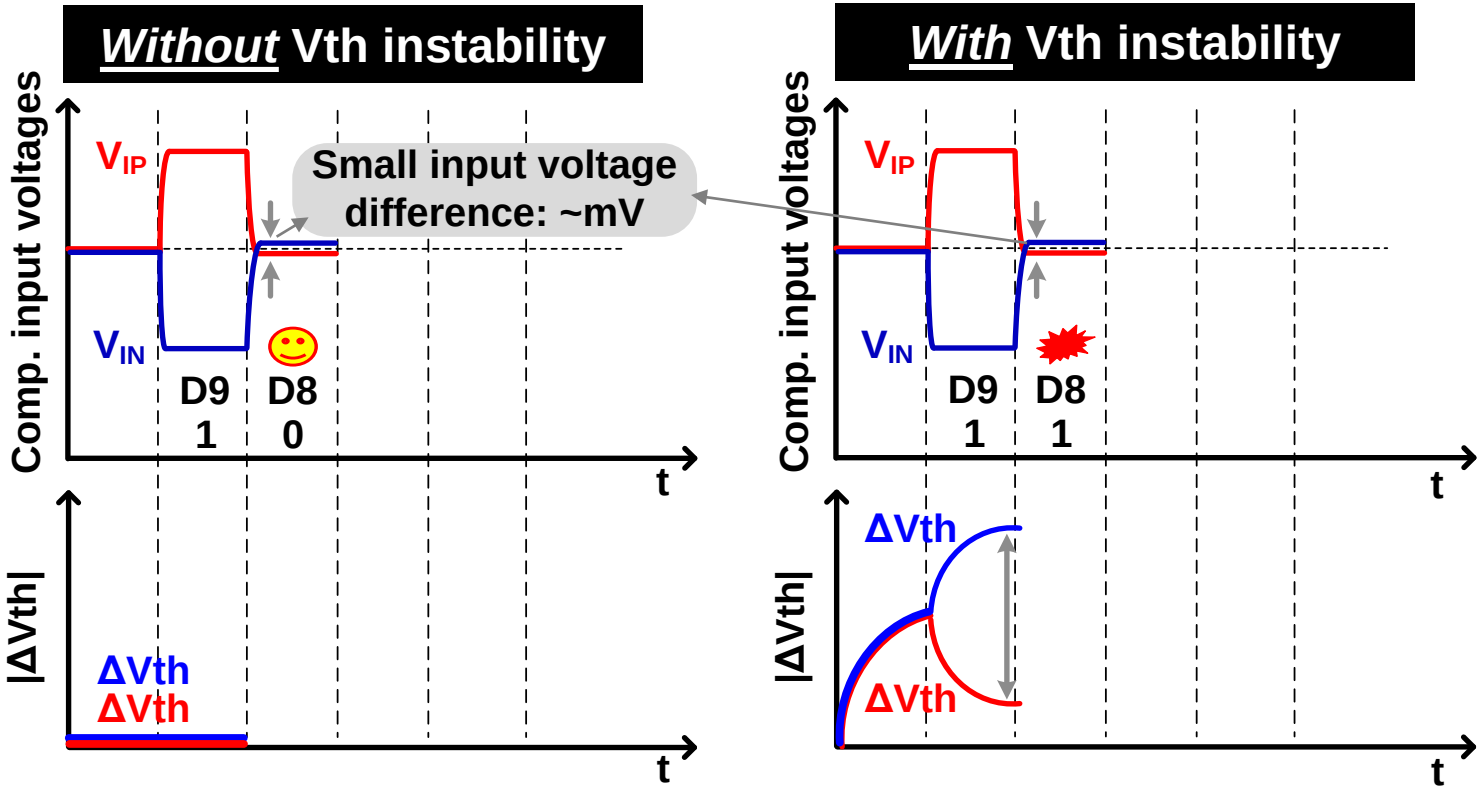
- **A large input voltage difference gives rise to a large difference in short-term Vth shifts**

Short-term Vth Instability during SAR Operation



- **If the input voltage difference in the next SAR conversion step (D8) is smaller than the Vth shift difference, it may lead to an incorrect decision**

Short-term Vth Instability during SAR Operation



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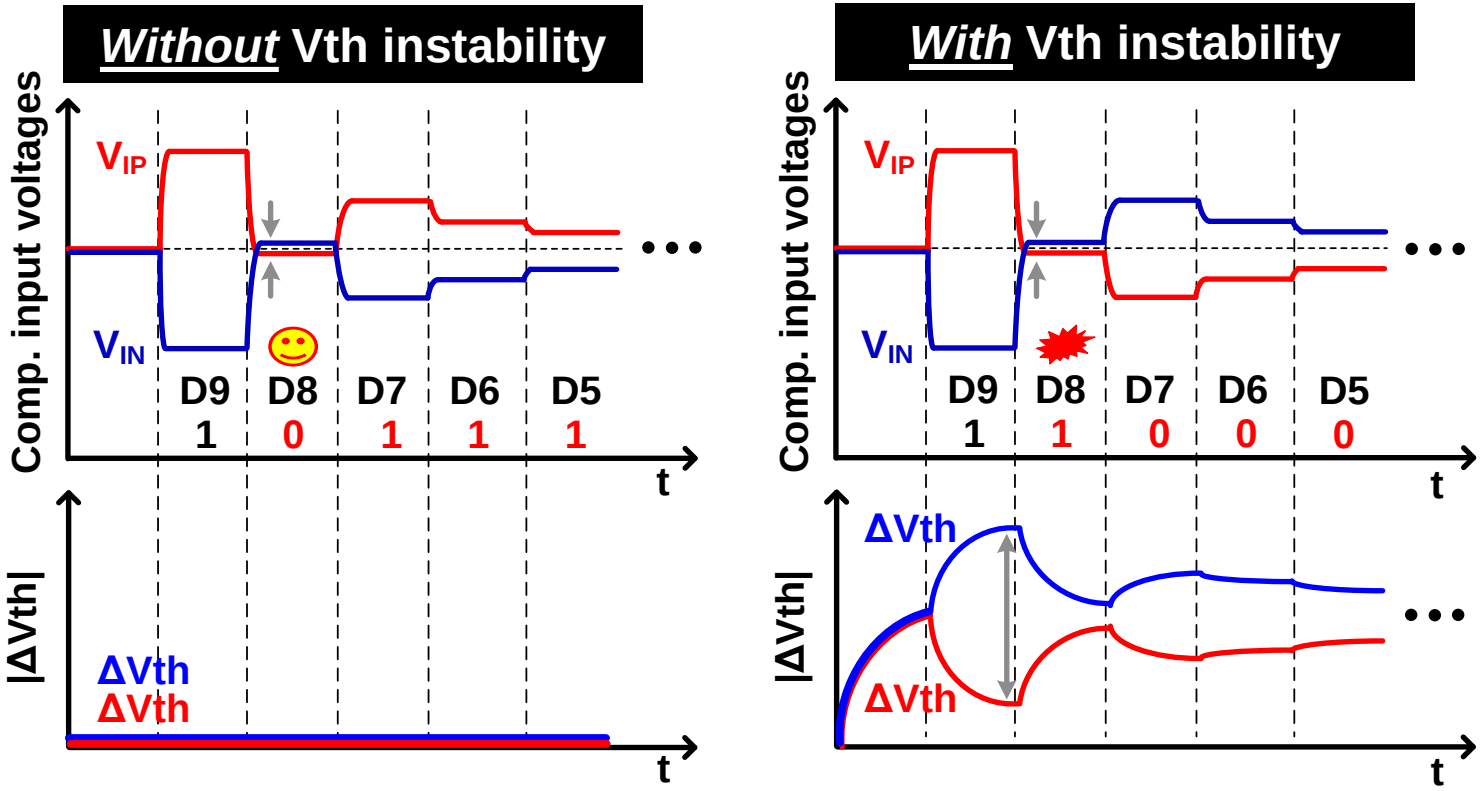
Short-term Vth Instability during SAR Operation



- The error cannot be corrected by the subsequent conversion steps (…0111 vs. …1000)
- An error of one LSB generated in the digital output

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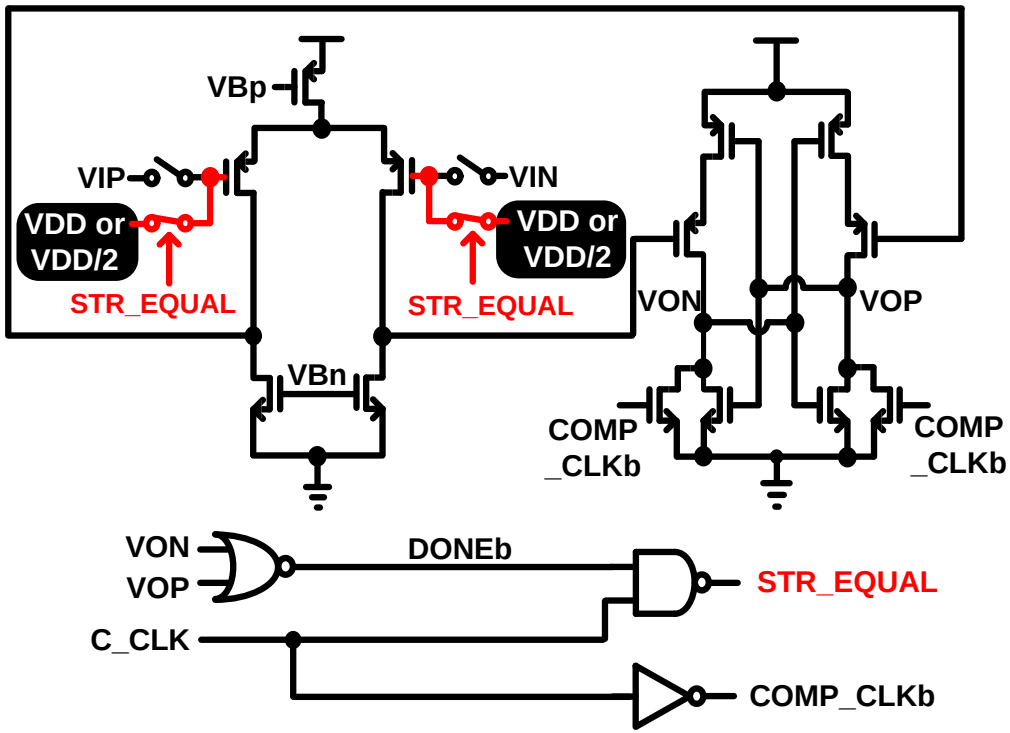
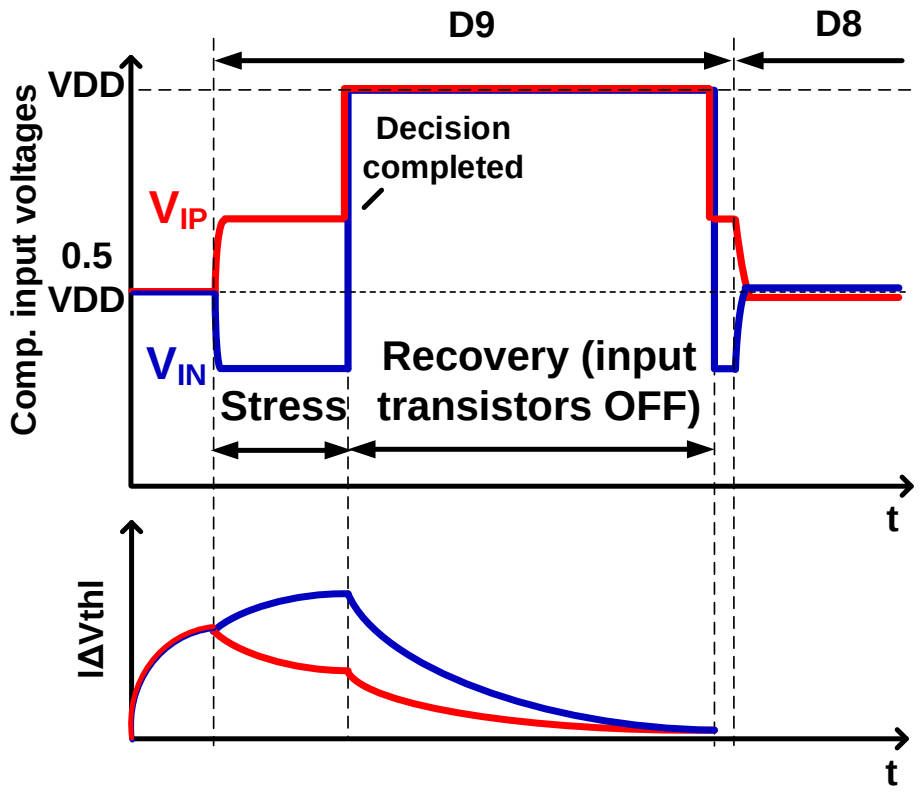
Proposed Dynamic Offset Cancellation Technique

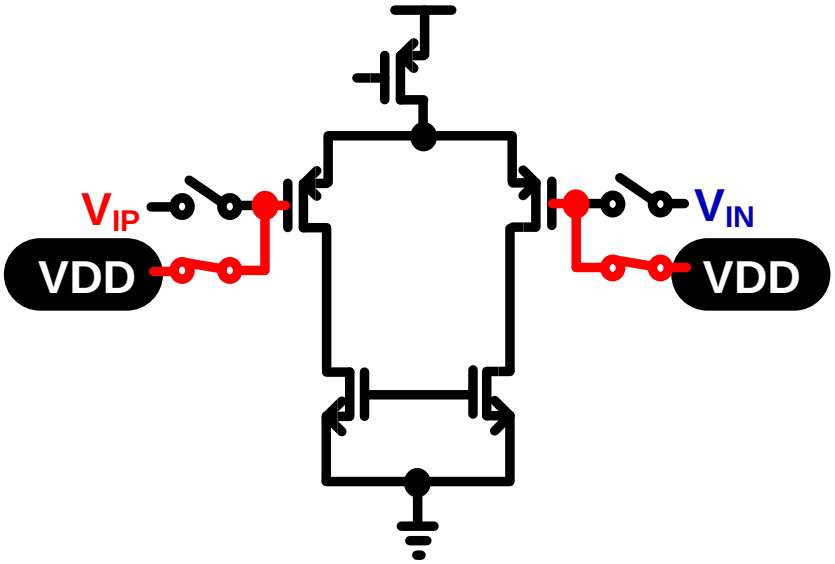


Comparator ref.: W. Liu, *et al.,* ISSCC, 2010.

- **Temporarily connects both comparator input voltages to the same level → equalizes Vth shift**

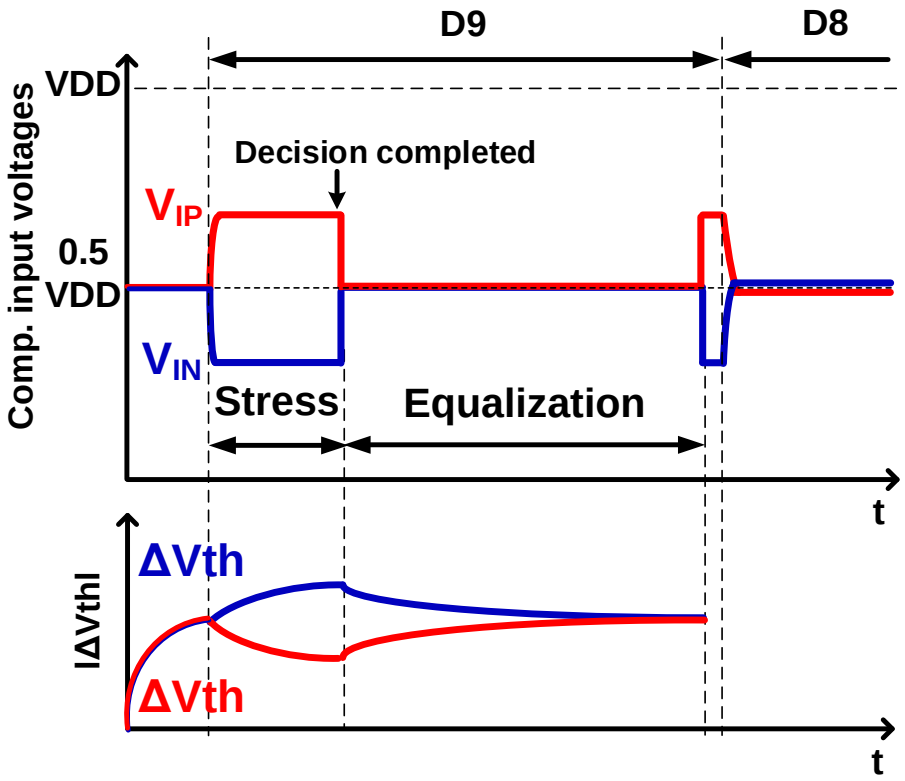
Technique #1: Stress Removal

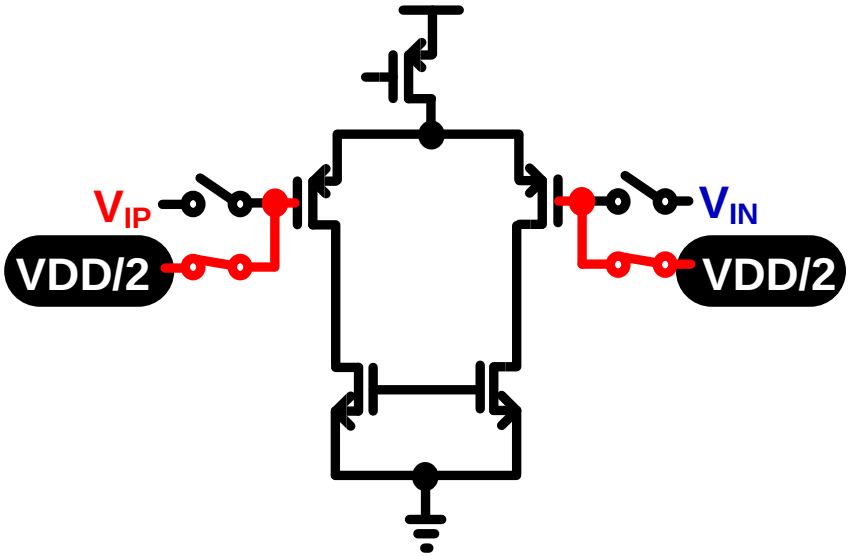




- **Proposed technique connects both input nodes to a recovery voltage (i.e. VDD for PMOS) right after the comparator makes a decision**

Technique #2: Stress Equalization





- **Proposed technique connects both input nodes to <u>the common mode voltage (i.e. VDD/2)</u> right after the comparator makes a decision**

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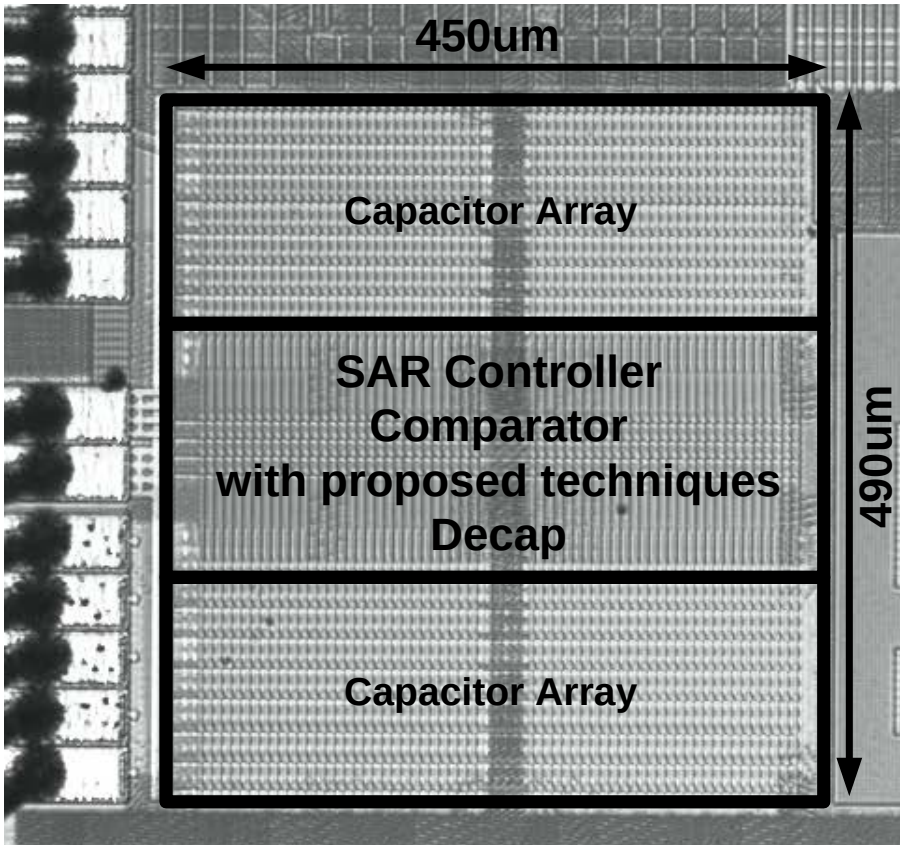
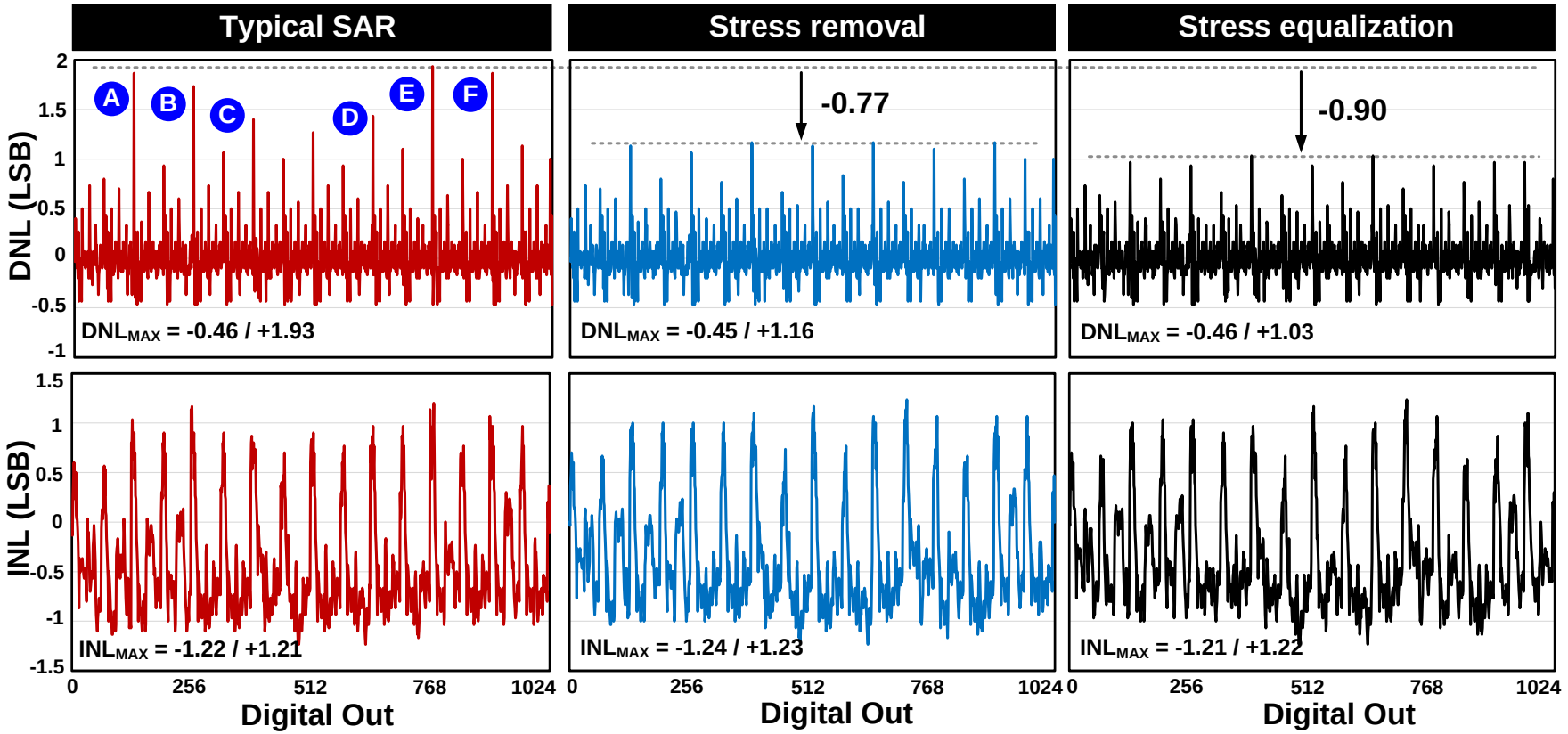
65nm SAR ADC Test Chip and Features



Process	65nm CMOS
Supply	1.2V
Resolution	10bit
Sample rate	80kS/s
DNL_{MAX} (LSB)	-0.46 / +1.03*
INL_{MAX} (LSB)	-1.21 / +1.22*
SNDR (dB)	50.79* @ 2.205kHz input
SFDR (dB)	65.65*
ENOB	8.14bit*
Power	305μW
Area	450x490μm^2

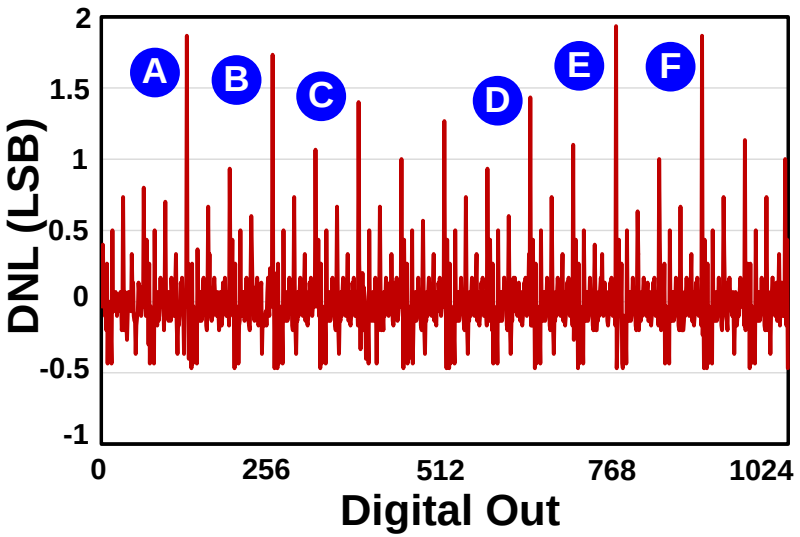
*w/ stress equalization technique

Measured DNL / INL



- **0.77 and 0.90 LSB improvement in DNL using stress removal and stress equalization, respectively**
- **Digital codes A~F show a large improvement in DNL**
- **INL remains relatively constant**

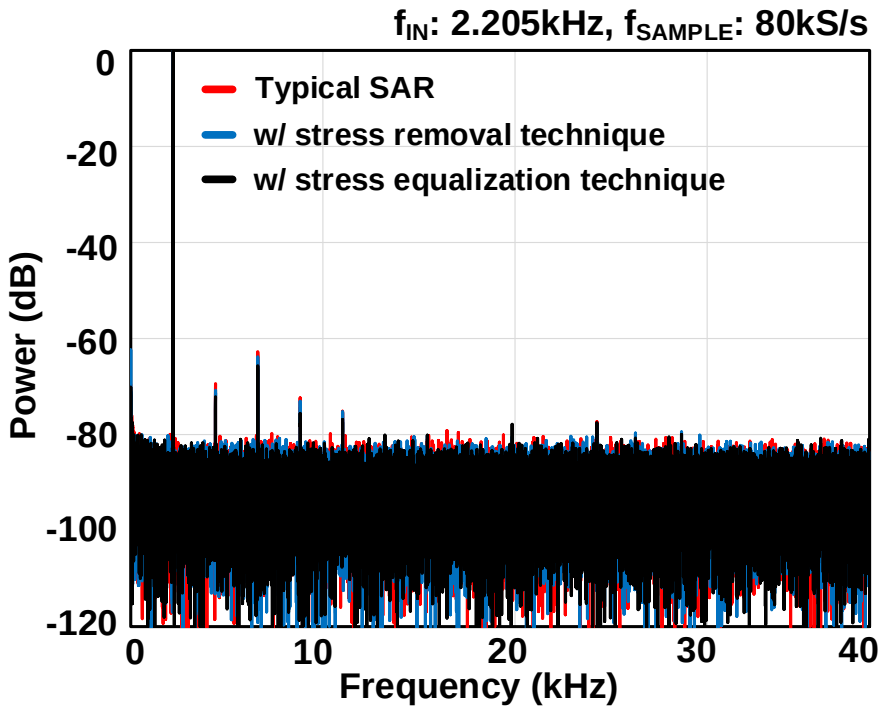
Output Codes Most Vulnerable to Short-term Vth Instability



	Digital out							Conv. step generating error
	Decimal value	Binary D9	D8	D7	D6	D5	···	
A	127 =	0	0	0	1	1	···	D7
	128 =	0	0	1	0	0	···	
B	255 =	0	0	1	1	1	···	D8
	256 =	0	1	0	0	0	···	
C	383 =	0	1	0	1	1	···	D7
	384 =	0	1	1	0	0	···	
D	639 =	1	0	0	1	1	···	D7
	640 =	1	0	1	0	0	···	
E	767 =	1	0	1	1	1	···	D8
	768 =	1	1	0	0	0	···	
F	895 =	1	1	0	1	1	···	D7
	896 =	1	1	1	0	0	···	

- **The digital codes most vulnerable to short-term Vth instability have the following attributes**
  - **The correct code has a pattern of 011111…**
  - **The incorrect code has a pattern of 100000… due to the error in the early conversion step**

Measured FFT Results



	SNDR (dB)	ENOB (bit)	SFDR (dB)
Typical SAR	50.10	8.02	62.74
Stress removal	50.36	8.07	63.79
Stress equalization	50.79	8.14	65.65

- **Subtle improvements in SNDR, ENOB, and SFDR observed after applying the proposed techniques**

Conclusions

- **Stress mitigation techniques are proposed for alleviating short-term Vth instability issues in SAR ADCs**
- **The proposed techniques temporarily connect the comparator input nodes to the same voltage level right after the comparator's decision is complete**
- **Measured data from a 65nm SAR-ADC test chip shows improvements in DNL using the proposed techniques**

Acknowledgement

- **Dr. Vijay Reddy at Texas Instruments for technical feedback and encouragement**