An Electrical and Optical Concurrent Design Methodology for Enlarging Jitter Margin of 25.8-Gb/s Optical Interconnects

Takashi Takemoto, Hiroki Yamashita,

Yasunobu Matsuoka, Yong Lee,

and Masaru Kokubo

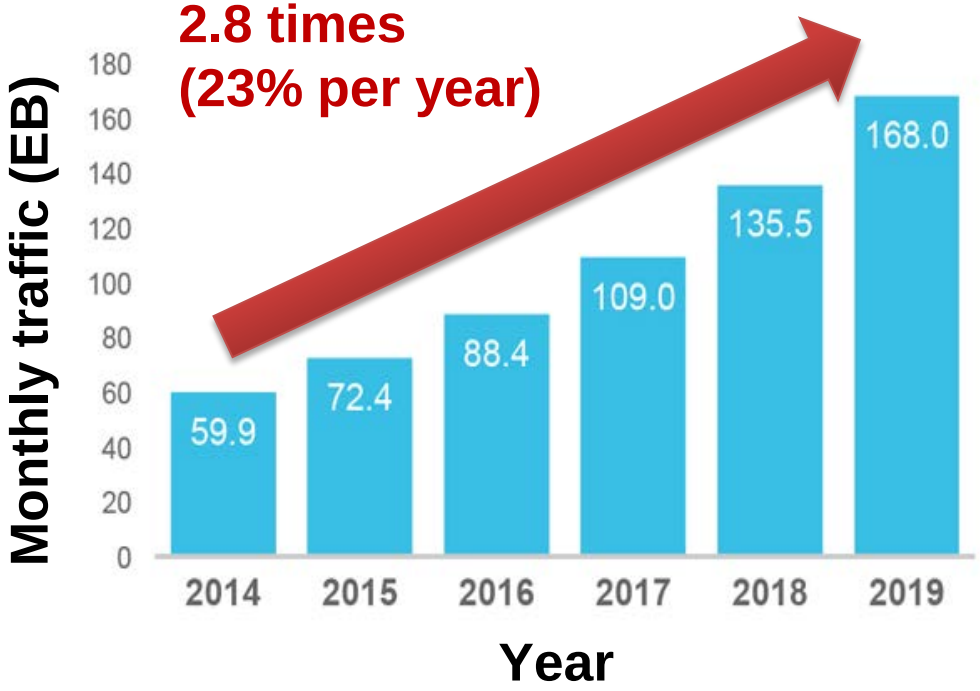
Hitachi, Ltd., Research & Development Group,
Center for Technology Innovation - Electronics

Outline

- **Motivation**
- **Challenges and Approaches**
  - **Loss management**
  - **Jitter management**
- **Elec. and Opt. Concurrent Design Method**
  - **Step-response-based LD modeling**
- **Fabricated Opt. Link between FPGAs**
  - **Enlarged jitter margin (deterministic jitter)**
  - **Reduced random jitter of LD**
- **Conclusions**

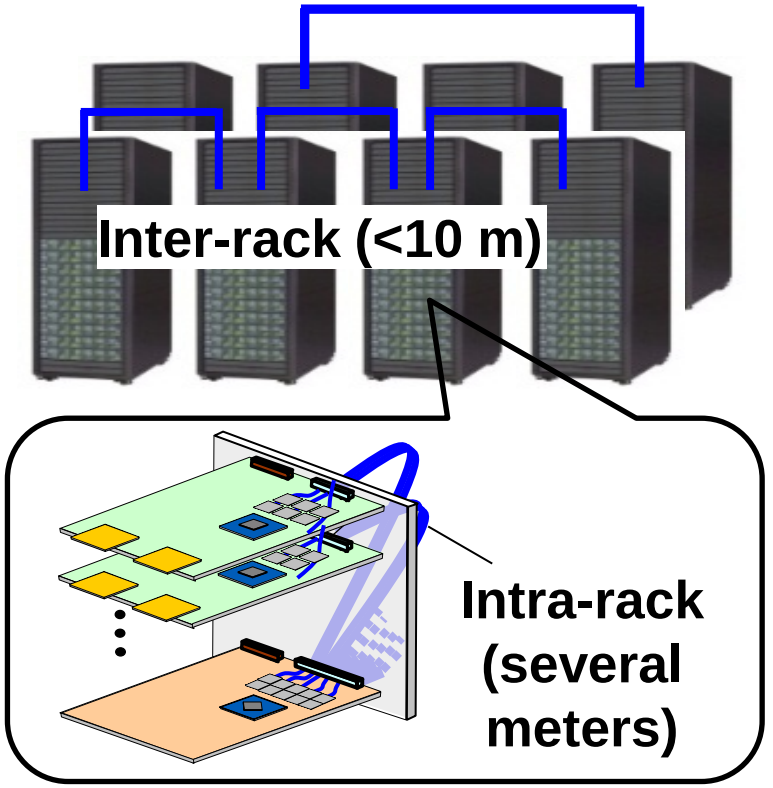
Growing Throughput of ICT Systems

Global IP traffic forecast



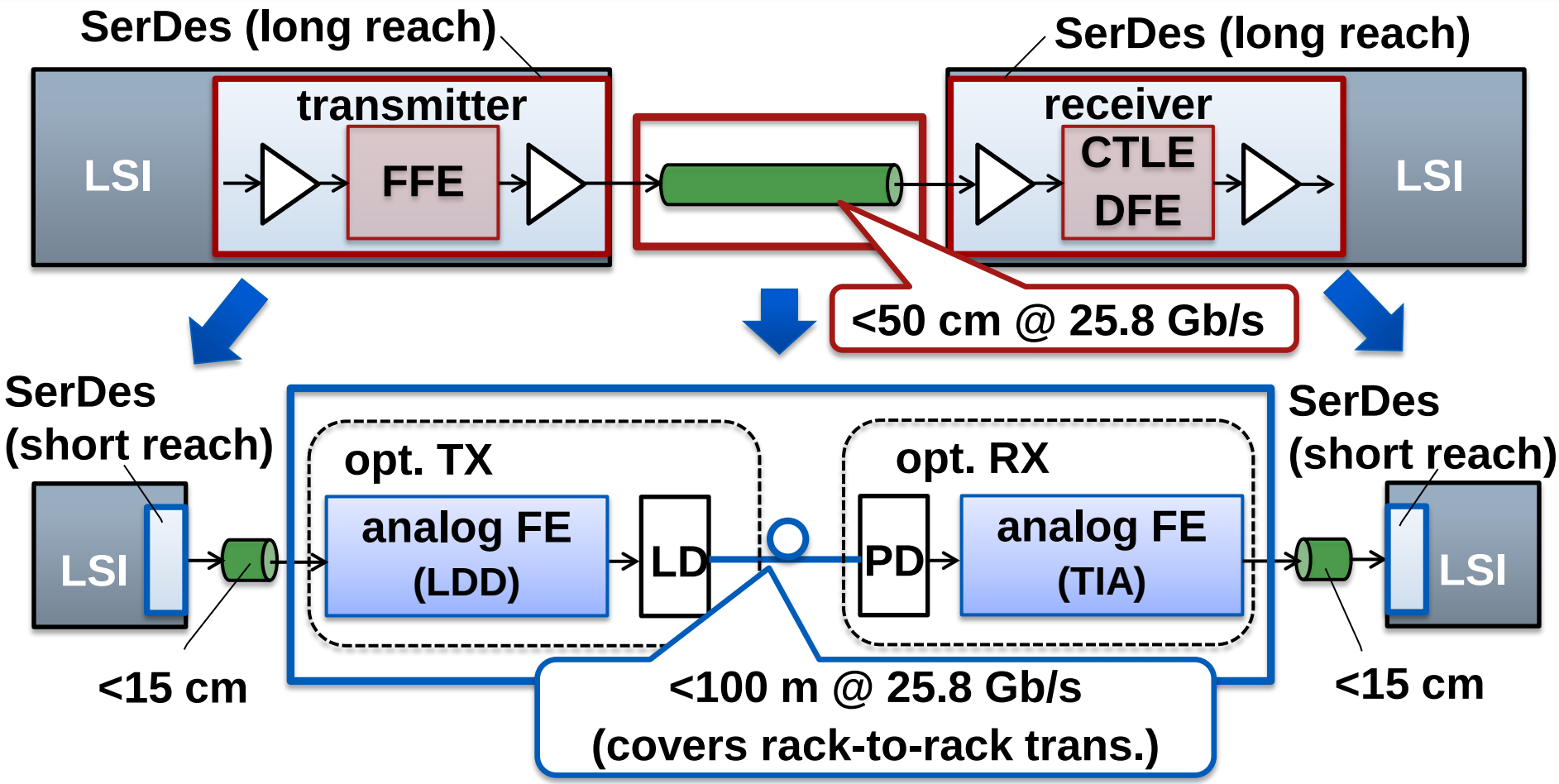
Cisco VNI 2015 Global Traffic Forecast

Inter-rack (<100 m)



- Rapid growth of IP traffic: higher speed (over 25 Gb/s) interconnects
- Inter-/intra- rack trans. (<100 m) inside DCs: Much more important today and in future

4 Targeted Optical Interconnects

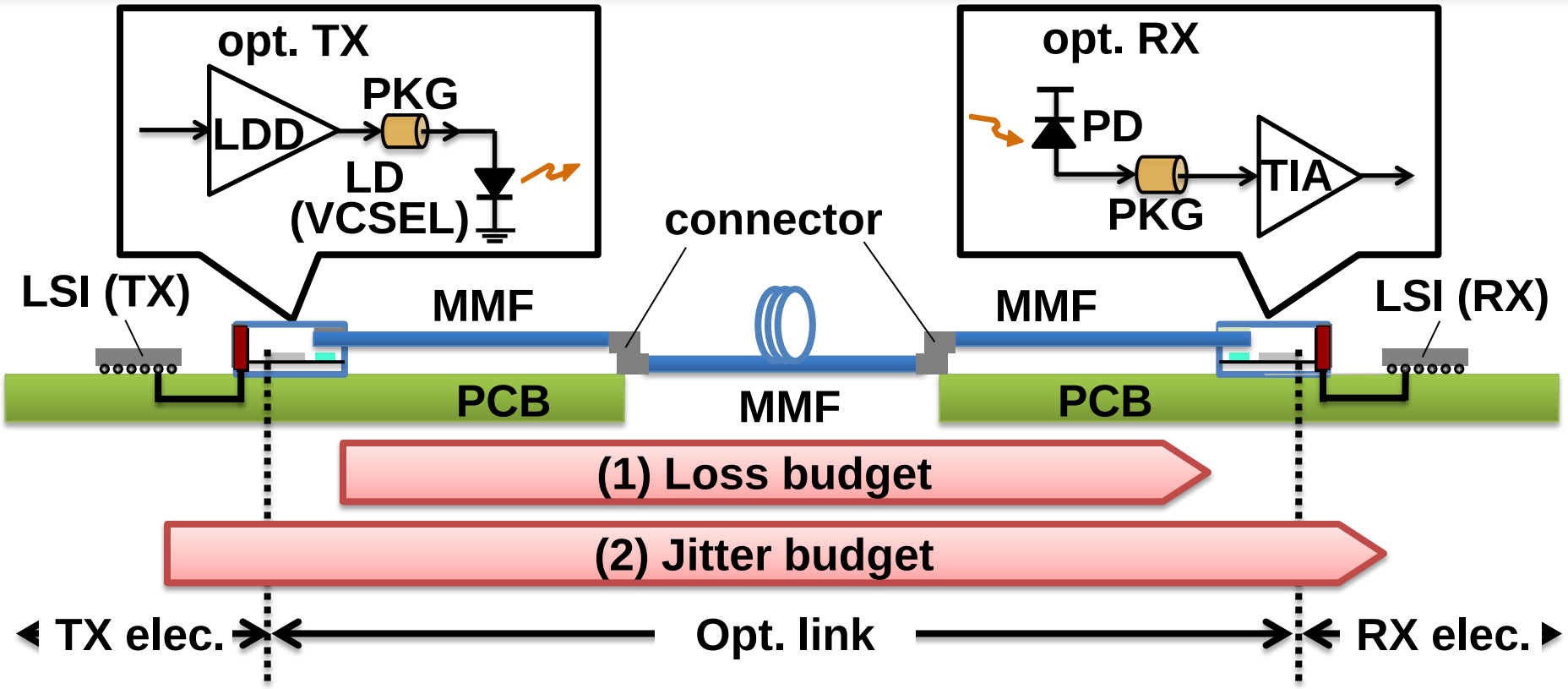


- Opt. interconnects: lower-power 25-Gb/s inter-/intra-rack trans. (negligible loss & reflection free)

Outline

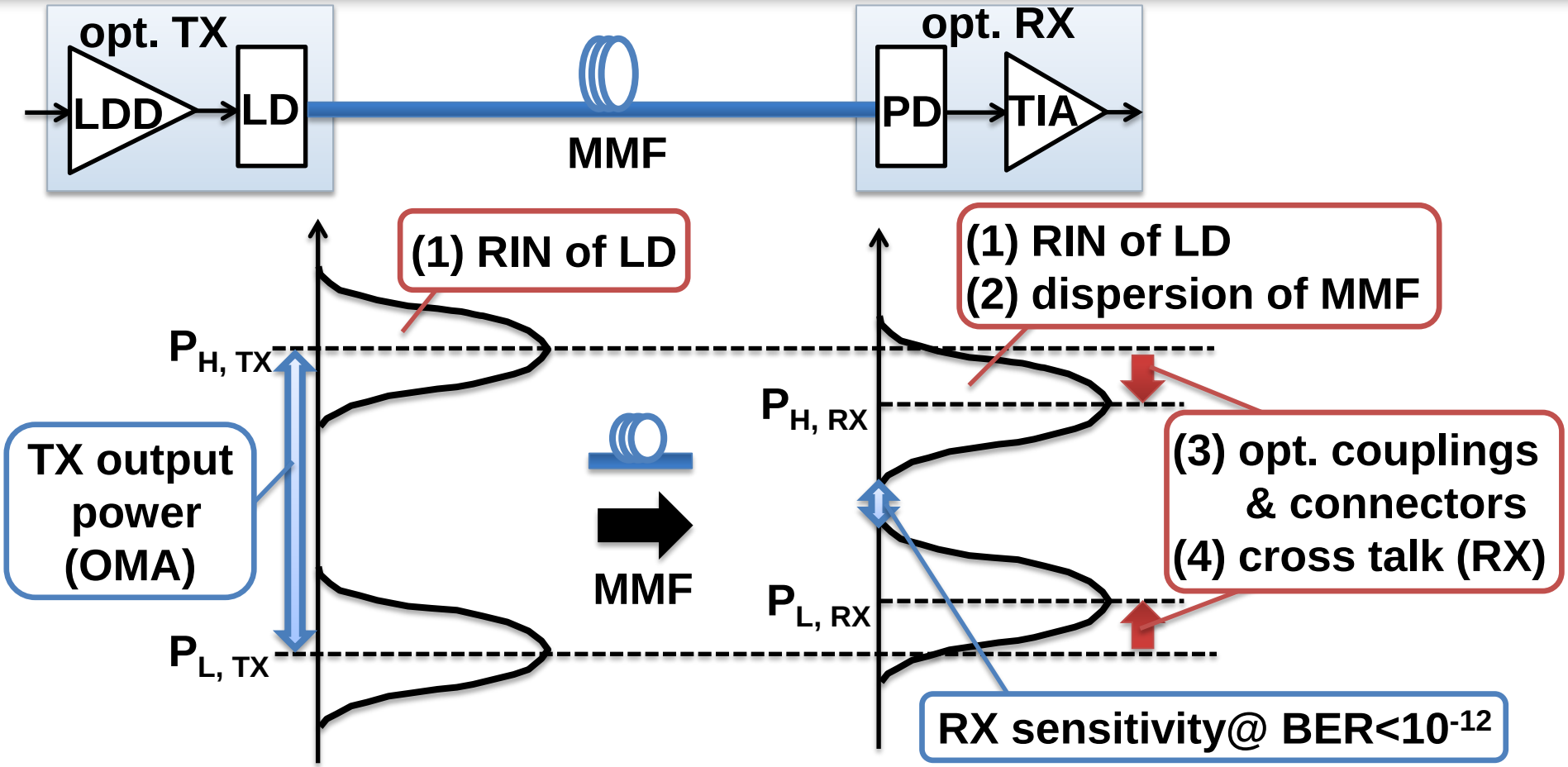
- Motivation
- **Challenges and Approaches**
  - **Loss management**
  - Jitter managements
- Elec. and Opt. Concurrent Design Method
  - Step responses based LD modeling
- Fabricated Opt. Link between FPGAs
  - Enlarged jitter margin (deterministic jitter)
  - Reduced random jitter of LD
- Conclusions

Challenges facing Opt. Interconnects



- Challenges facing designing opt. interconnects:
  1. **Loss budget:** determined by only opt. link
  2. **Jitter budget:** consider TX/RX electrical I/F & opt. link as one (elec. losses degrade opt. link)

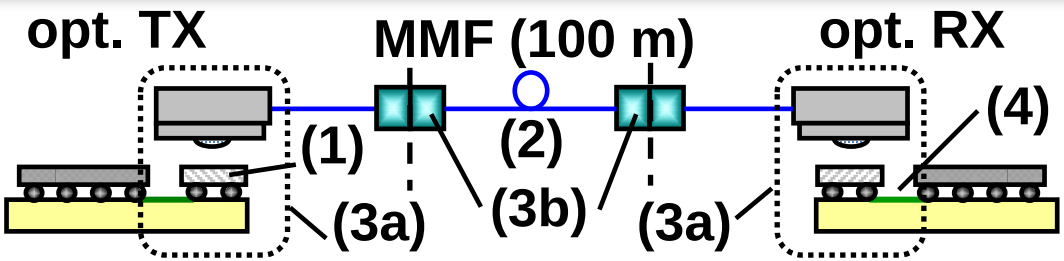
7 Loss Managements



- Total losses: determined by (1)(2) random & (3)(4) deterministic components
- Minimum TX output power: determined by RX sensitivity

*) RIN: Relative intensity noise

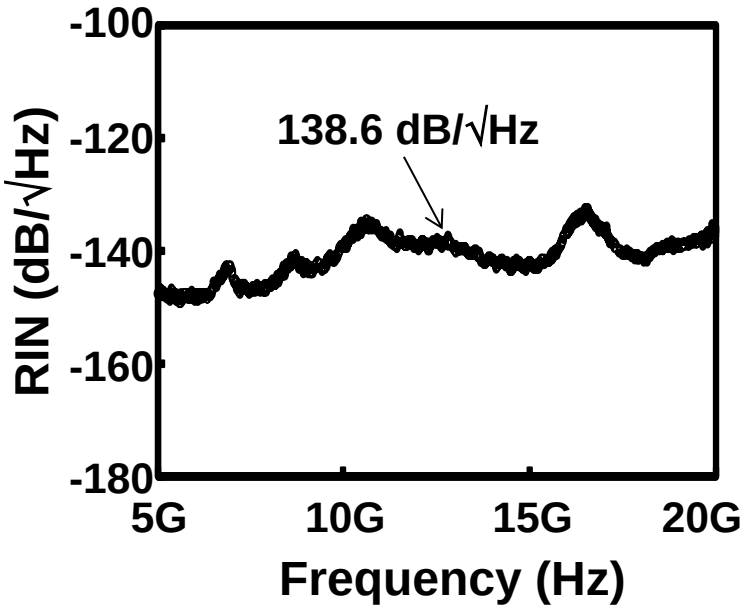
8 Loss Budget



opt. TX	OMA	4.5 dBm
	(1) RIN	–0.07 dB
	(3a) opt. coupling	–2 dB
MMF (100 m)	(3b) opt. connectors	–1 dB
	(2) dispersion	–4.5 dB
opt. RX	(3b) opt. coupling	–2 dB
	(4) cross talk	–1 dB
	RX sensitivity	–6.0 dBm

Total losses: about –10.5 dB

Measured RIN of VCSEL



- Inter-rack trans. (<100 m): dispersion reduces loss budget margin (in case of standard MMF)
- Sensitivity improvements: achieves longer trans. distance

Chromatic Dispersion of MMF

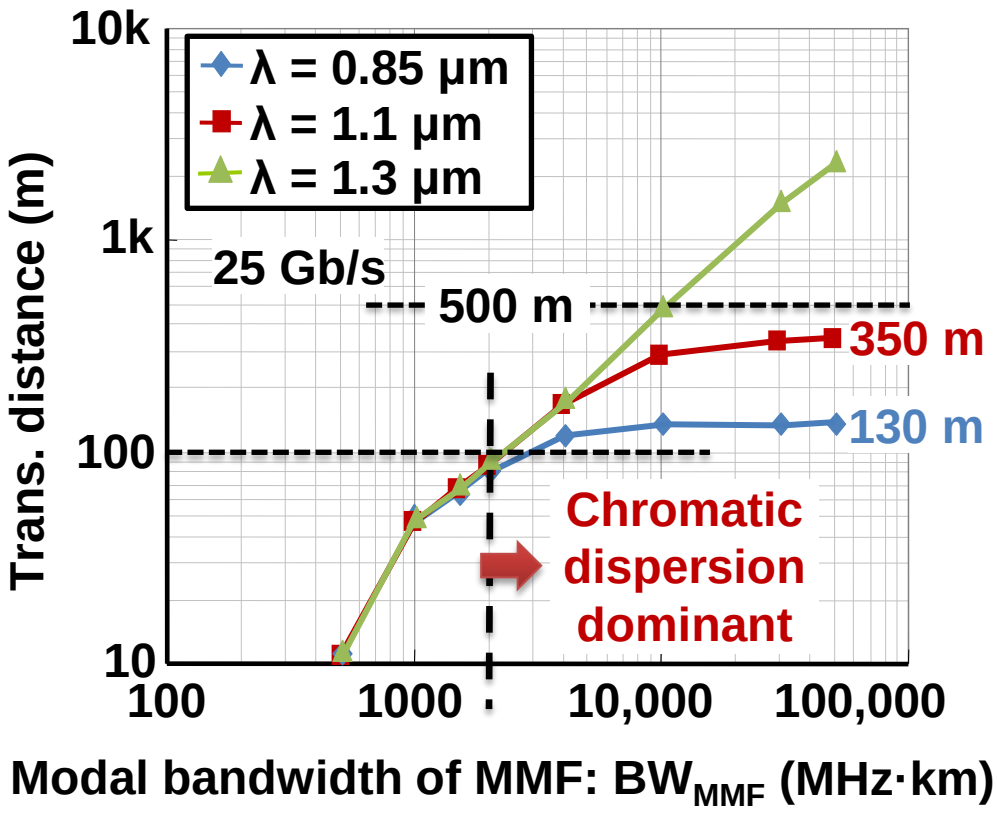
Total pulse RMS width

$$\sigma_{tot} = d\sqrt{\frac{\ln 2}{2\pi^2}\cdot\frac{1}{BW_{MMF}} + D_c^2\sigma_s^2}$$

Modal dispersion

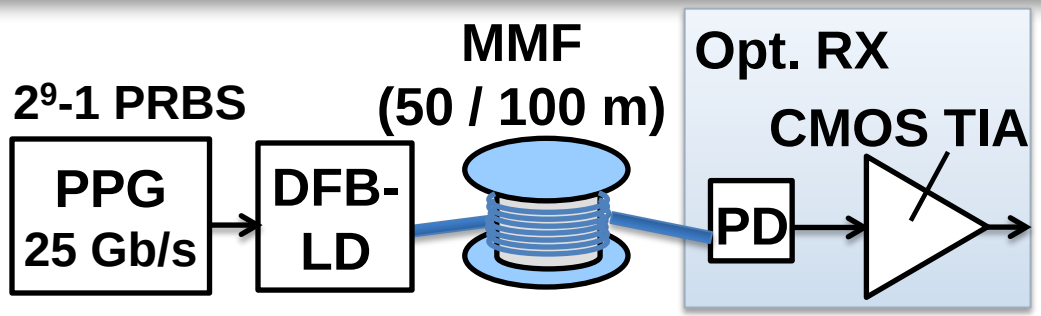
Chromatic dispersion

- BW_{MMF}: modal bandwidth of MMF
- σ_S: spectrum width of LD
- Dc: chromatic dispersion
  - 90 ps/nm·km @0.85 μm
  - 35 ps/nm·km @1.1 μm
  - 3 ps/nm·km @1.3 μm (negligible chromatic dispersion)

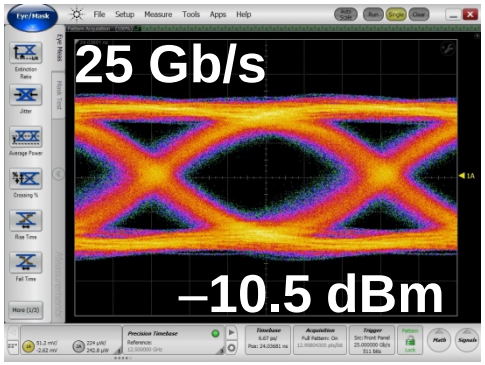


- Chromatic dispersion imposes MMF-trans. limits (over 100m): 130 m@ 0.85-μm/350 m@ 1.1 μm
- Short-reach trans. (< 100 m): independent of wavelength

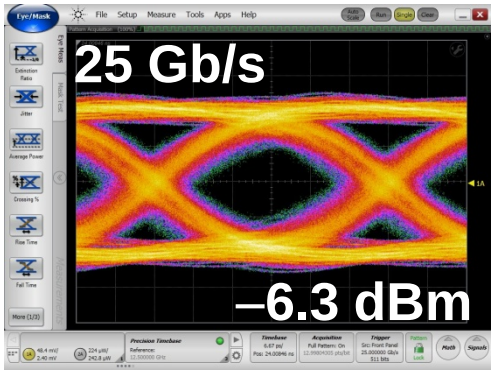
Measured Penalty of 100-m MMF Trans.



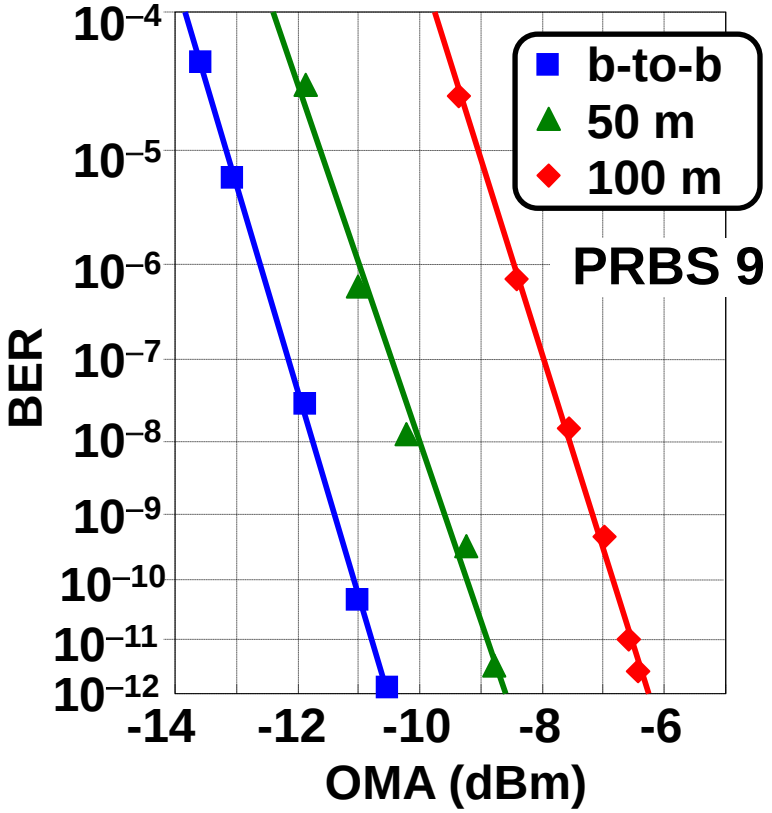
back-to-back



after 100-m trans.



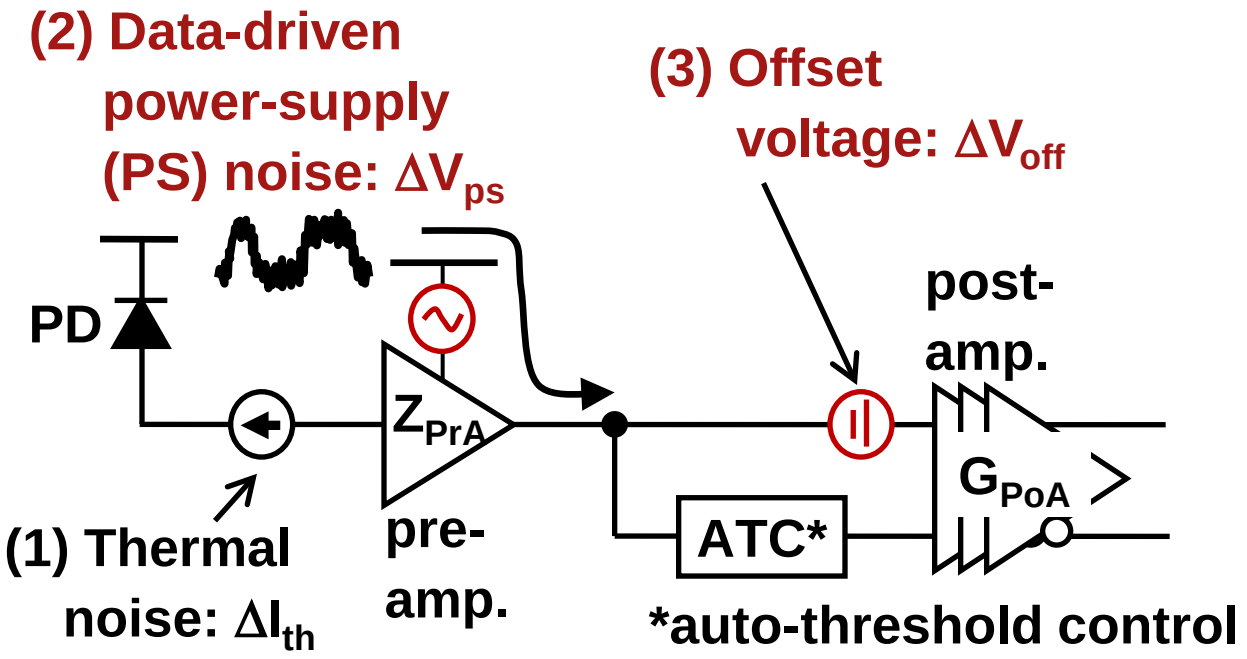
3.76-dB extinction ratio (ER)

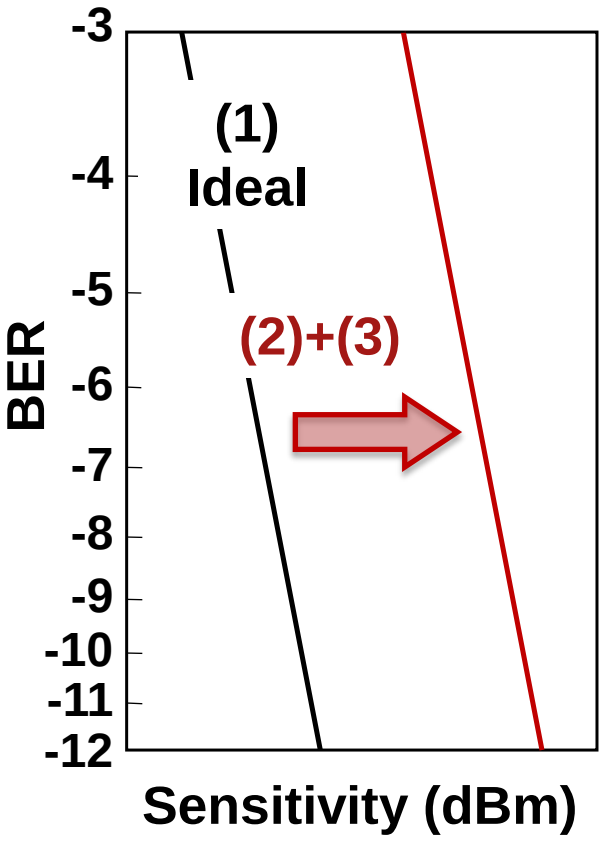


T. Takemoto et al., SPIE, 2014

- Sensitivity: –10.5 dBm@b-to-b; –8.6 dBm@50 m; –6.3dBm@100 m
- Power penalty: 1.9 dB@50 m; 4.2 dB@100 m (target<4.5 dB)

Challenges for High Sensitivity



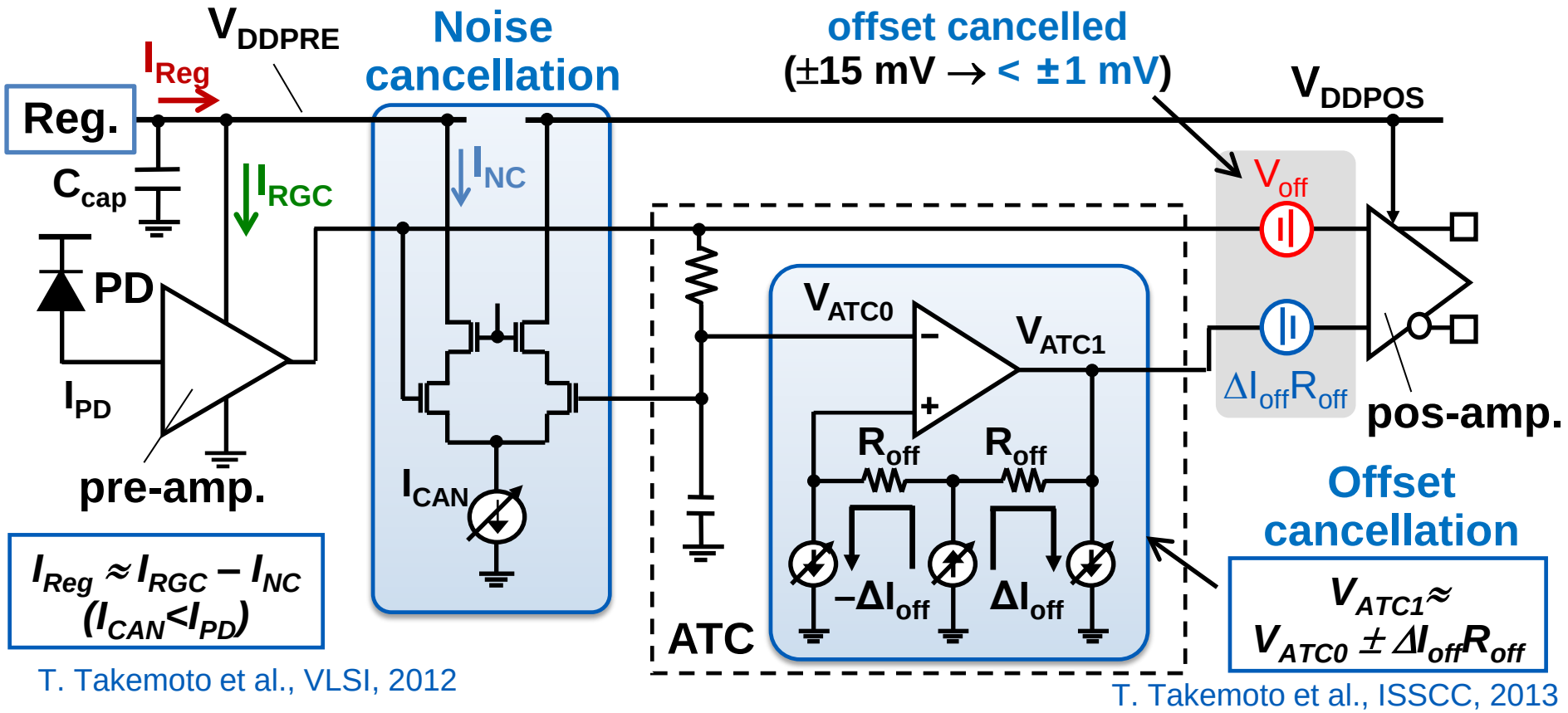


Sensitivity@ BER<10^{-12} (min. input current):

$$I_{in} \approx \underbrace{14 \cdot \Delta I_{th}}_{(1)} + \underbrace{(\Delta V_{ps}}_{(2)} + \underbrace{\Delta V_{off})}_{(3)} / Z_{PrA}$$

- PS noise & offset voltage [(2) and (3)] seriously deteriorate sensitivity (not only thermal noise)

Approaches for High Sensitivity

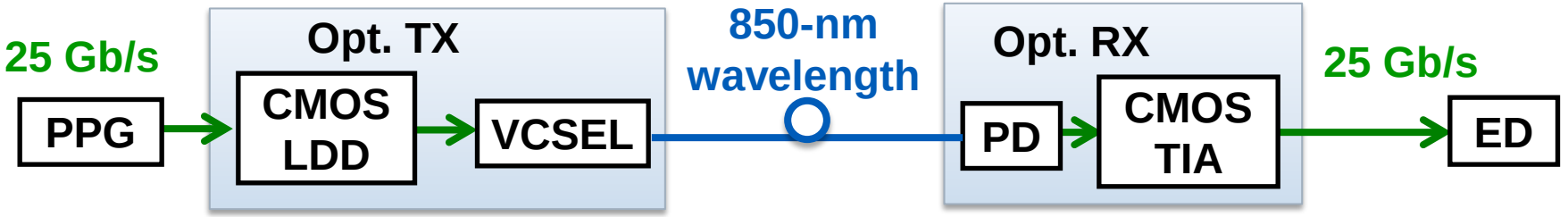


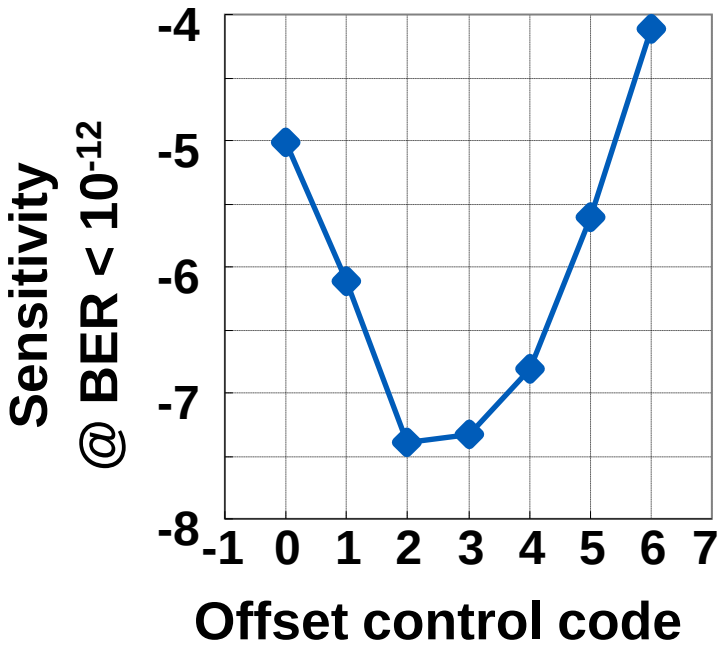
T. Takemoto et al., VLSI, 2012

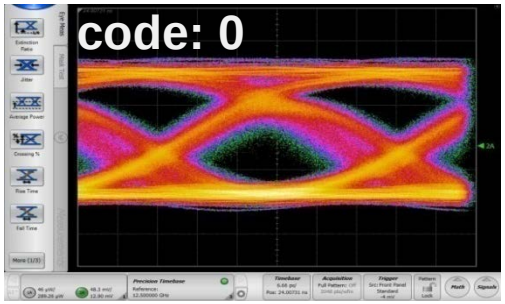
T. Takemoto et al., ISSCC, 2013

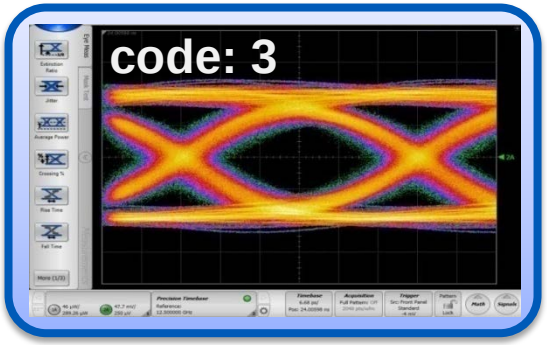
- Noise cancellation: PS variations suppressed down to 200 kHz without requiring larger C_{cap}
- Offset cancellation: Shifted threshold level (±15 mV→ ±1 mV)

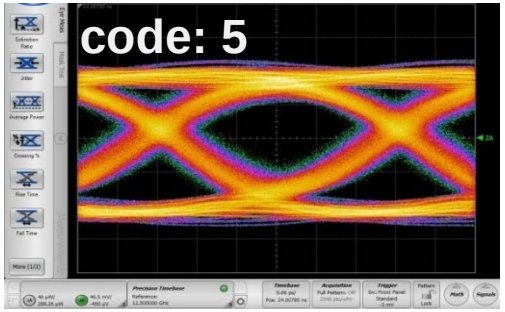
Measured Receiver Sensitivity

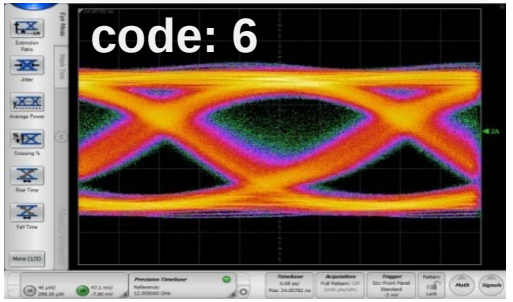












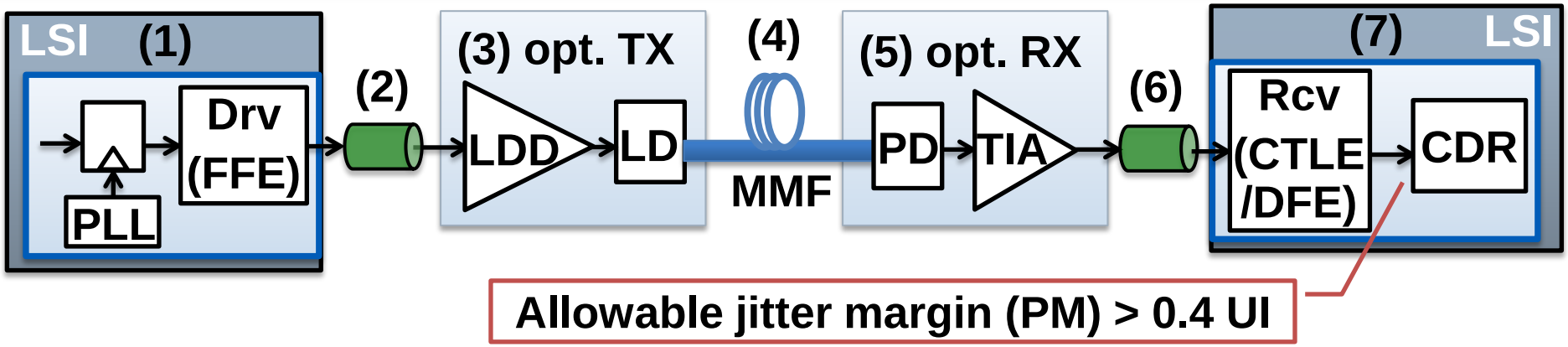
T. Takemoto et al., JSSC, 2014

- Improved sensitivity: –7.3 dBm (VCSEL -based link) by shifting cross points of eye pattern

Outline

- Motivation
- **Challenges and Approaches**
  - Loss managements
  - **Jitter management**
- Elec. and Opt. Concurrent Design Method
  - Step responses based LD modeling
- Fabricated Opt. Link between FPGAs
  - Enlarged jitter margin (deterministic jitter)
  - Reduced random jitter of LD
- Conclusions

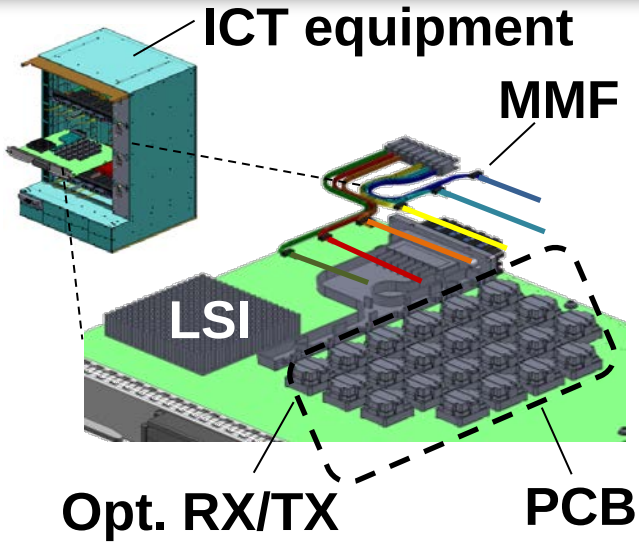
Targeted Jitter Budget

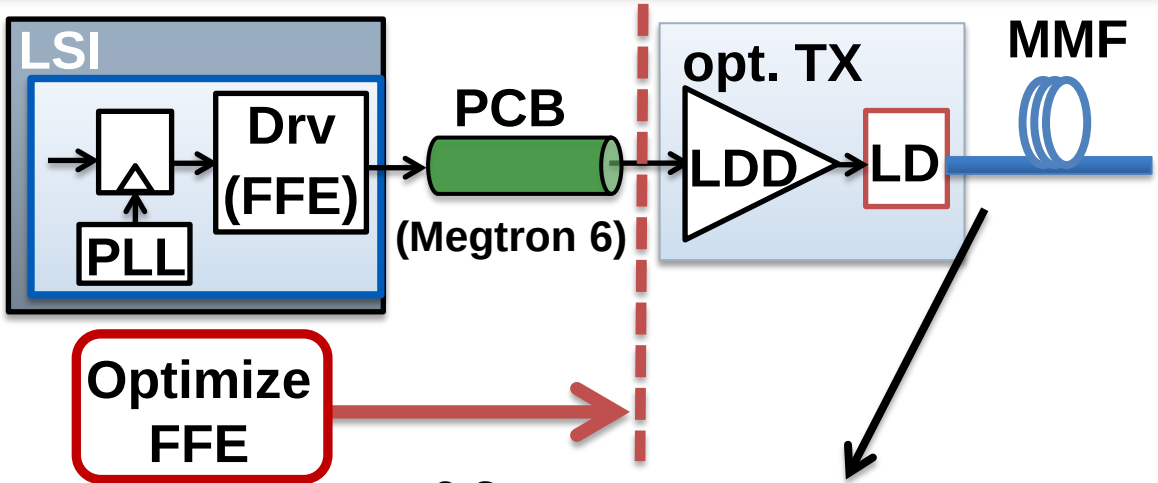


		DJ	RJ
(1)	PLL	-	thermal noise
	Drv	FFE / bandwidth	-
(2)	trans. line	losses & reflections	-
(3)	LDD	bandwidth	-
	LD	non-linearity	RIN
(4)	MMF	-	dispersion
TX total		0.25 UI	0.18 UI

		DJ	RJ
(5)	PD	bandwidth	-
	TIA	bandwidth	thermal noise
(6)	trans. line	losses & reflections	-
(7)	Rcv	CTLE / DFE / bandwidth	-
RX total		0.15 UI	0.08 UI
Total Jitter		0.4 UI	0.2 UI

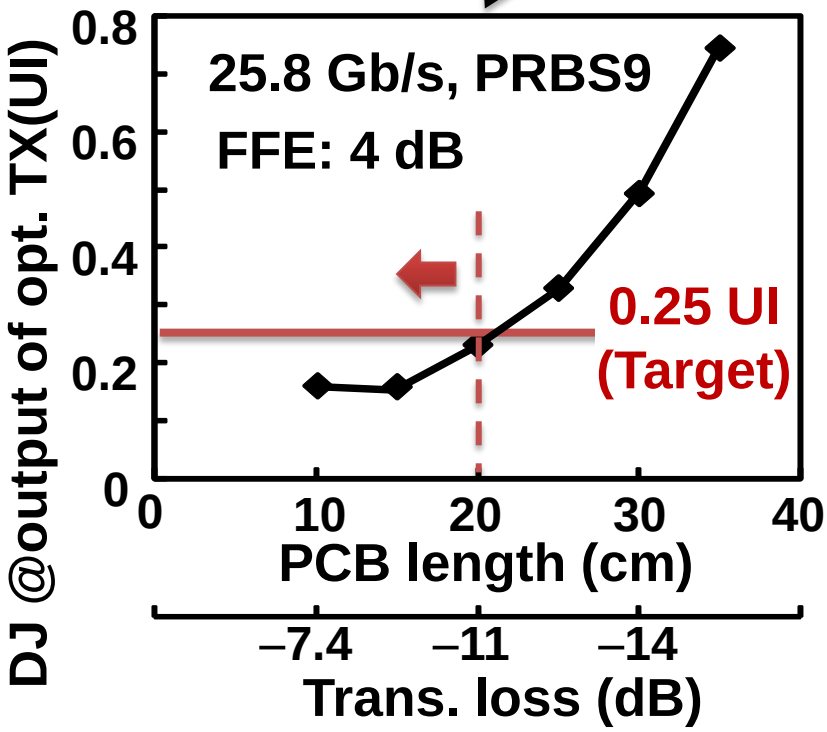
Challenges facing Jitter Management





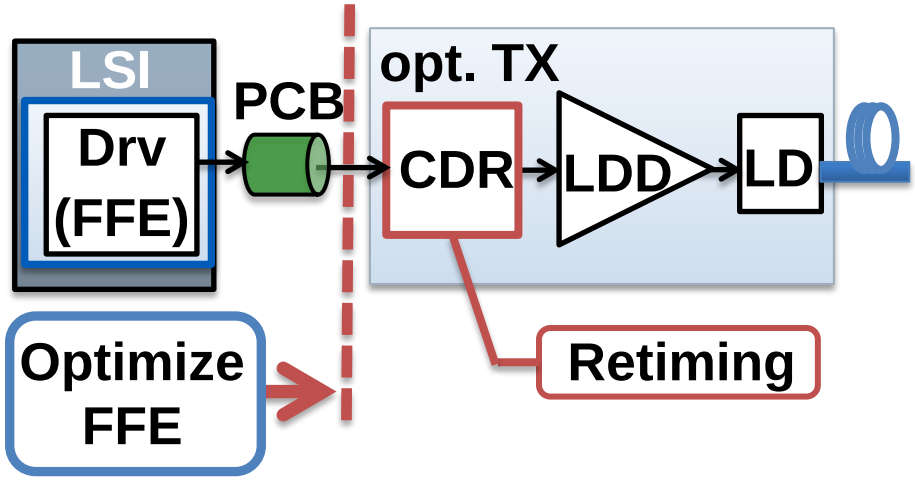
- Elec. losses: Reduced jitter margin for opt. link
- Restrict placements of opt. TX/RX (within about 20 cm):
  - Cooling problem
  - Difficult to increase trans. density due to parallel trans.

➡ Increased cost of ICT equipment

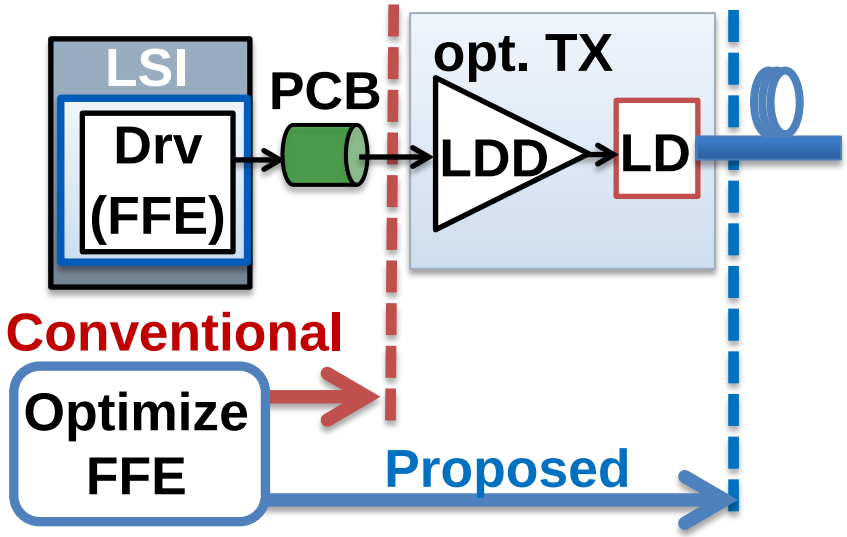


Approaches for Enlarging Jitter Margin

(i) Retiming inside opt. TX



(ii) Optimized FFE including opt. TX



(i) Retiming: Elec. I/F & opt. link considered separately

+ Elec. I/F & optical link considered separately

– Consumes large power

(ii) Expand reach of FFE: Compensate including opt. TX

+ W/o additional circuit block (opt. TX unchanged)

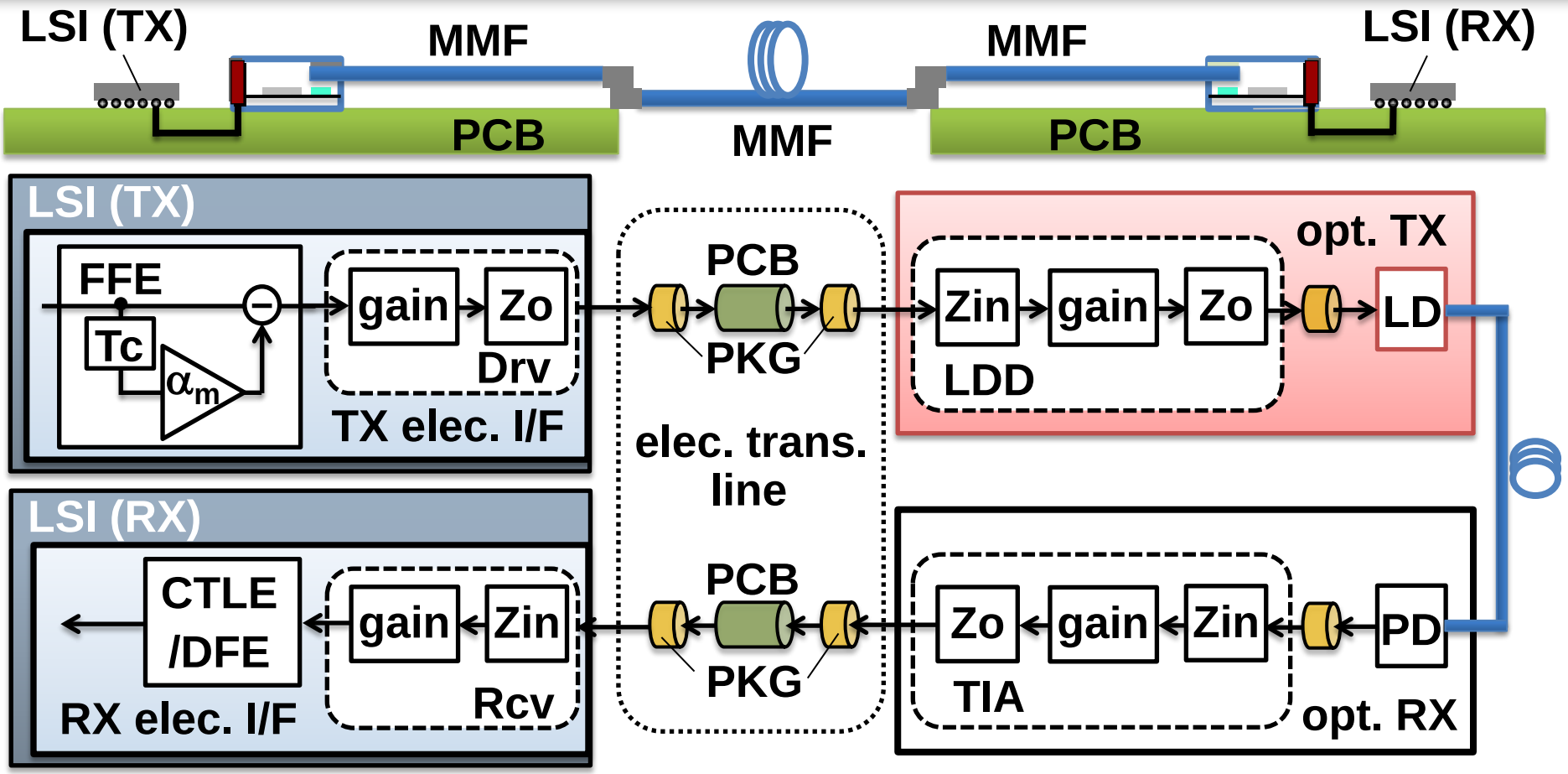
– Difficult to optimize FFE (elec. I/F & opt. link as one)

➡ Elec. & opt. concurrent design method required

Outline

- Motivation
- Challenges and Approaches
  - Loss managements
  - Jitter managements
- **Elec. and Opt. Concurrent Design Method**
  - **Step-response-based LD modeling**
- Fabricated Opt. Link between FPGAs
  - Enlarged jitter margin (deterministic jitter)
  - Reduced random jitter of LD
- Conclusions

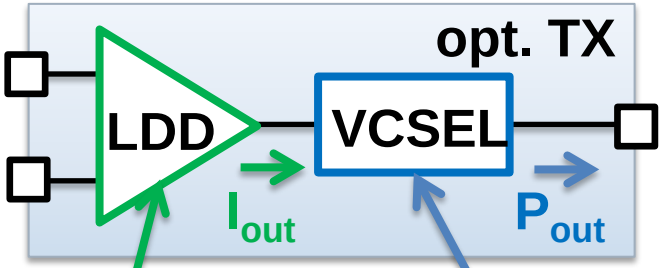
Overview of Elec. & Opt. Concurrent Design



- S parameter & behavior models: represents jitter characteristics of each components (excluding opt. TX)
- Opt. TX (LD): Another approach required

LD Modeling using Rate Equation

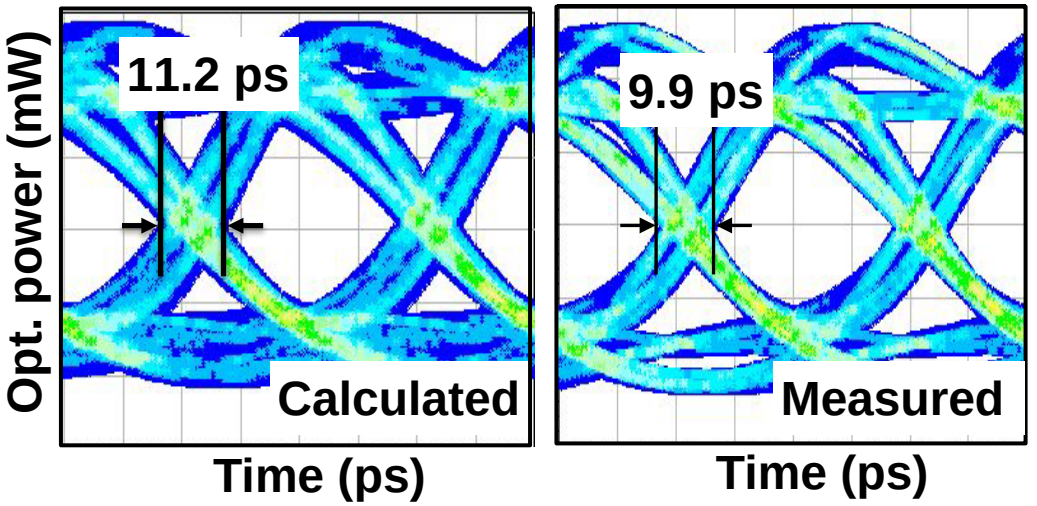
Opt. TX model (rate eq.)

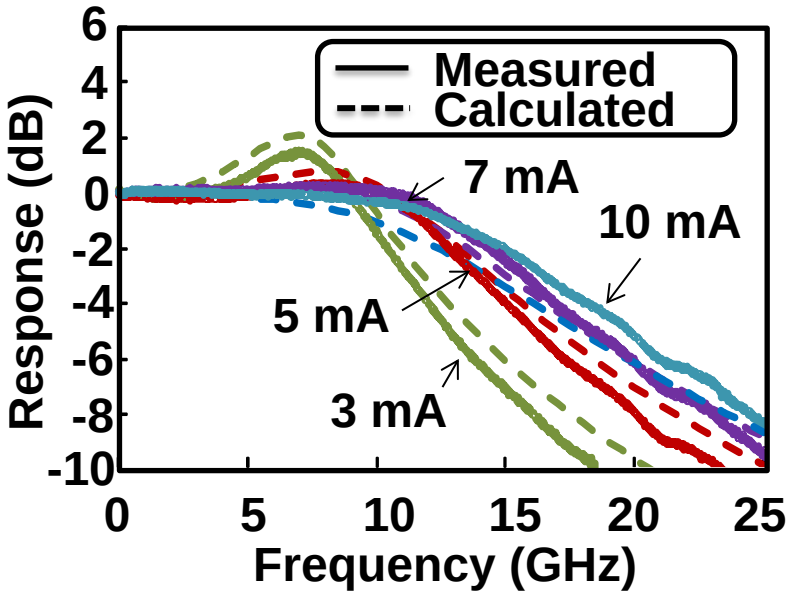


Measured S-param. / circuit sim.

Rate eq. based on measured rate-eq. params.

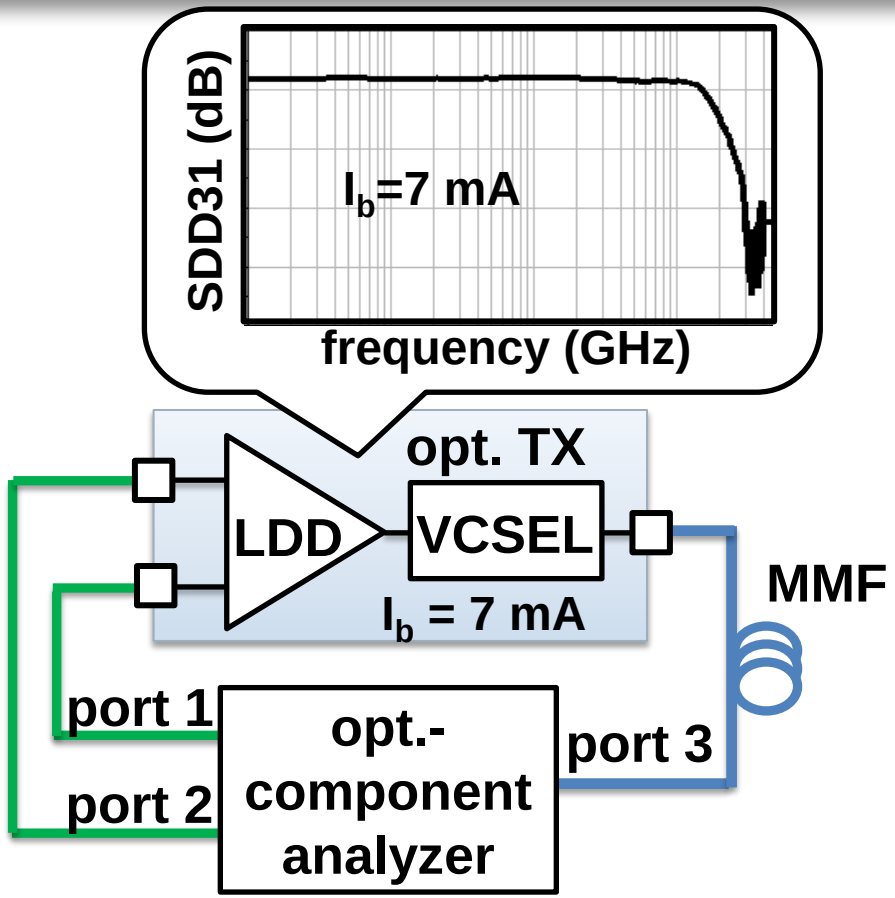
25-Gb/s eye diagrams (PRBS9)



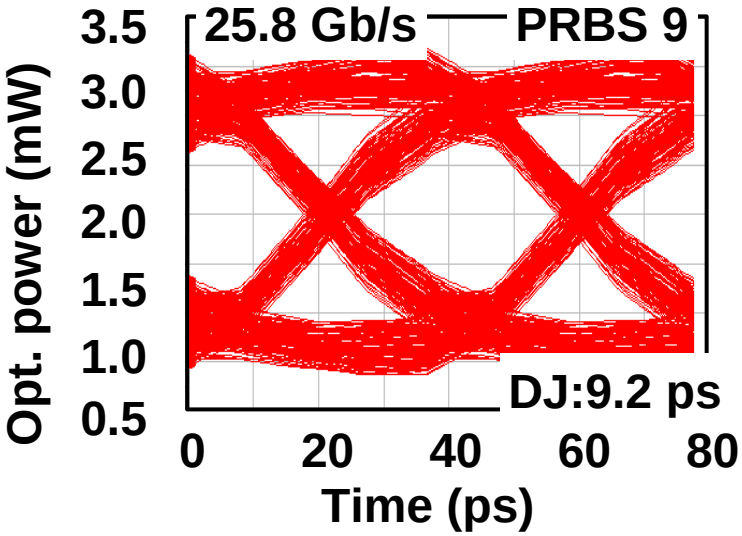


- Rate eq.: represents LD non-linearity (jitter error < 1.3 ps)
- Fully modularized opt. TX: difficult to obtain refined rate-eq. parameters & S-parameter of LDD

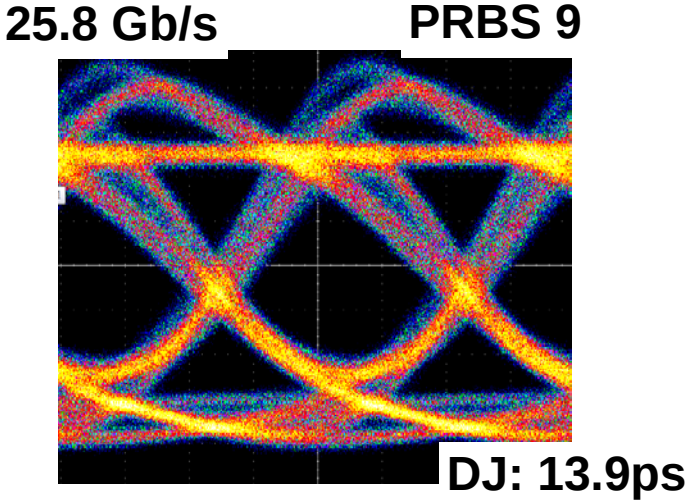
S-parameter-based Opt. TX Modeling



Calculated (S-parameter)



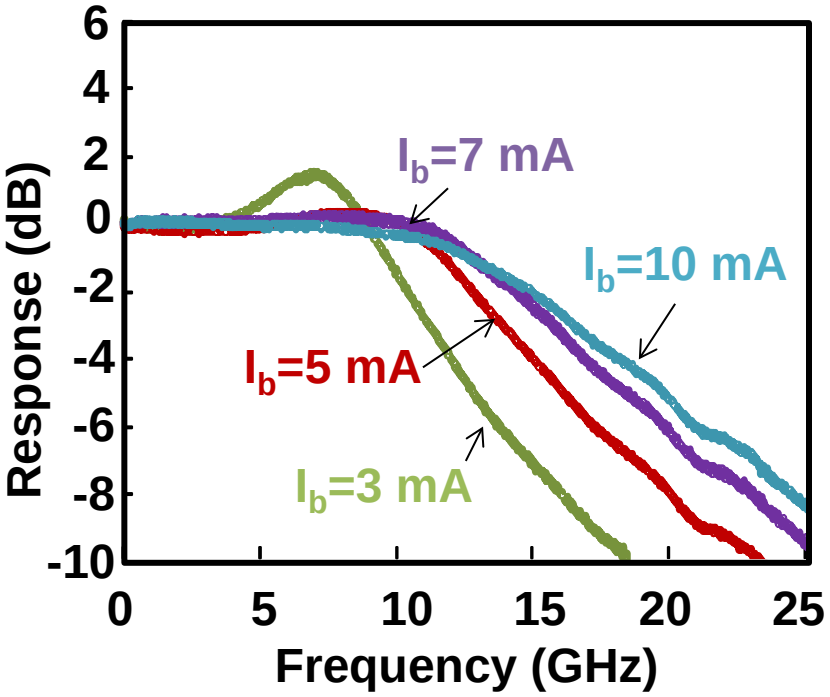
Measured



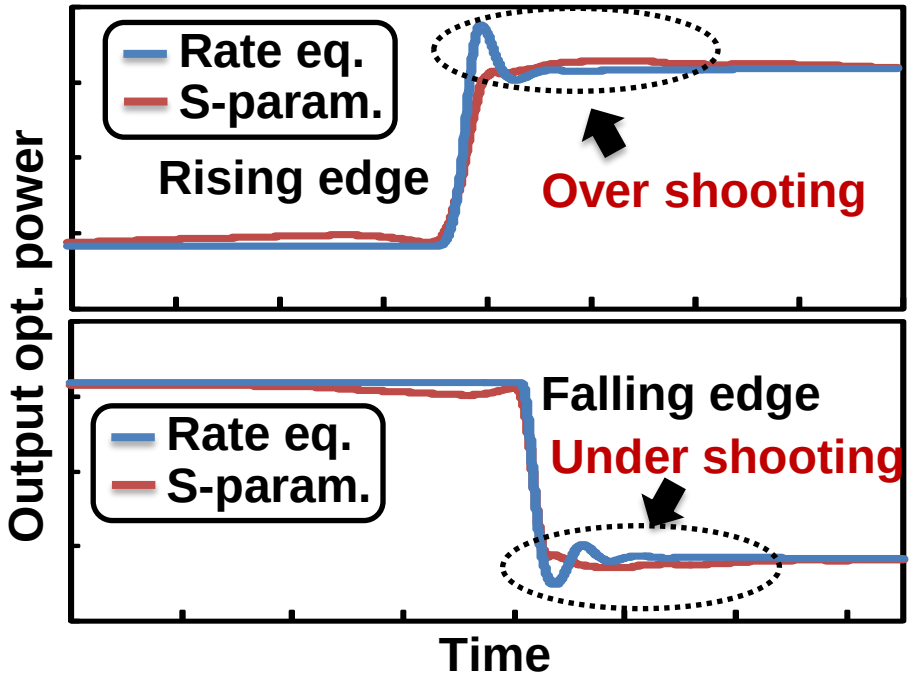
- S-parameter approach: Modeling for fully modularized opt. TX
- Measured eye exhibits larger jitter (jitter error: 4.7 ps)

Issues of S-param. Based LD Modeling

Bias current dependency of BW



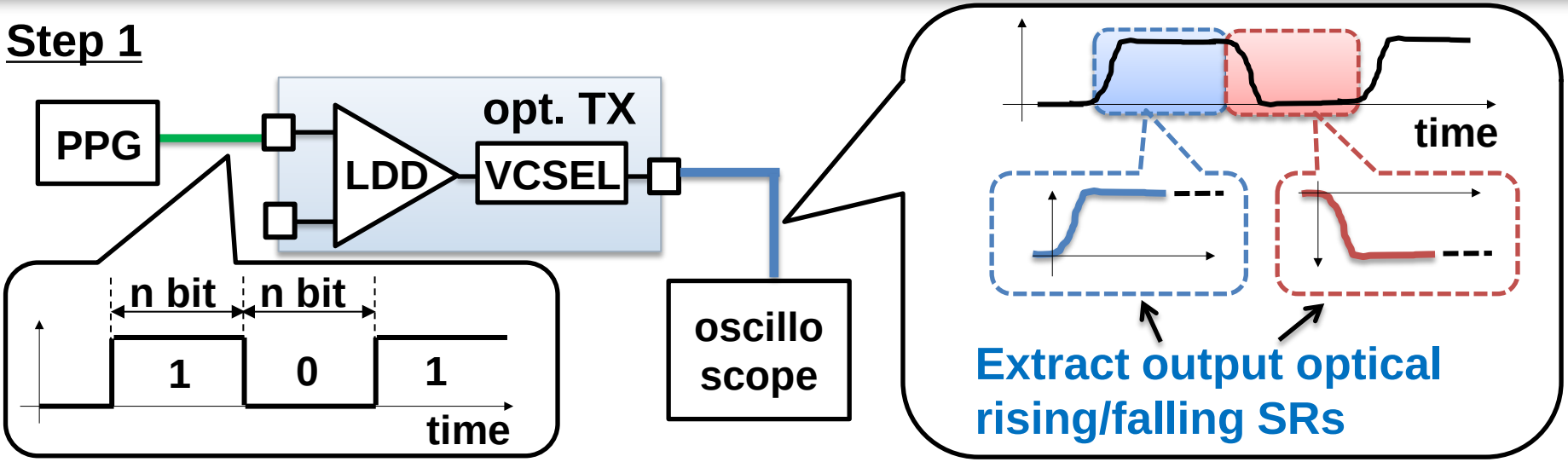
Over/under shooting



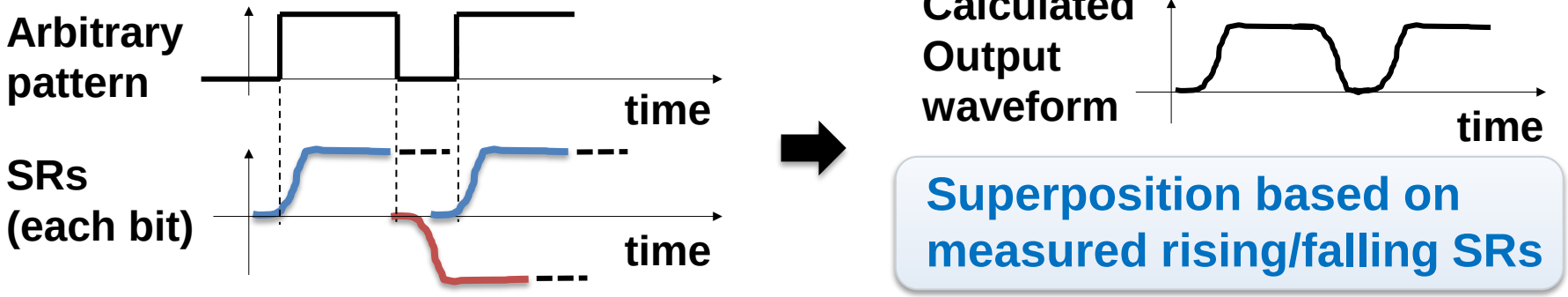
- LD bandwidth changed depending on bias current
- Convolution of impulse responses (S param.):
  Not represent over/under shooting at rising/falling edges
- Focuses on rising/falling step-responses (SRs) to represent over/under shooting

Step-response (SR)-based LD Modeling

Step 1

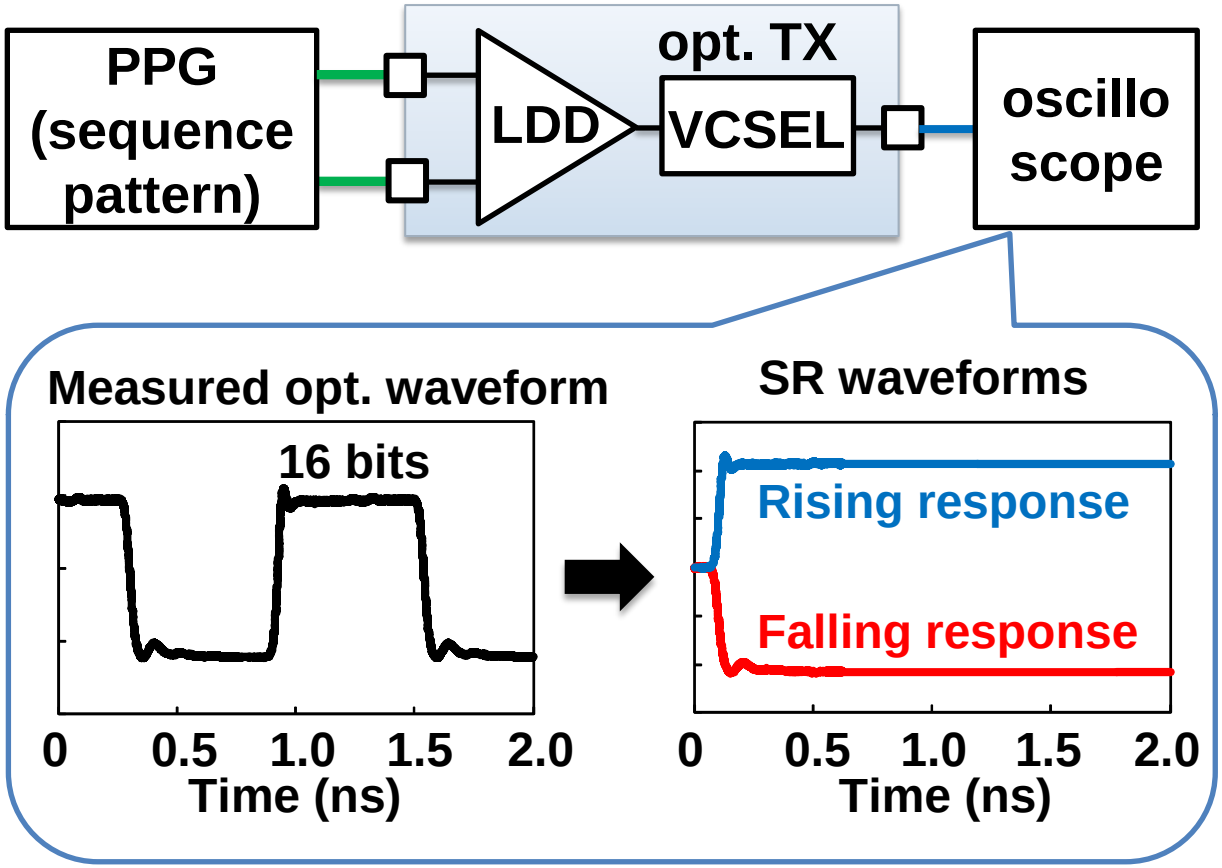


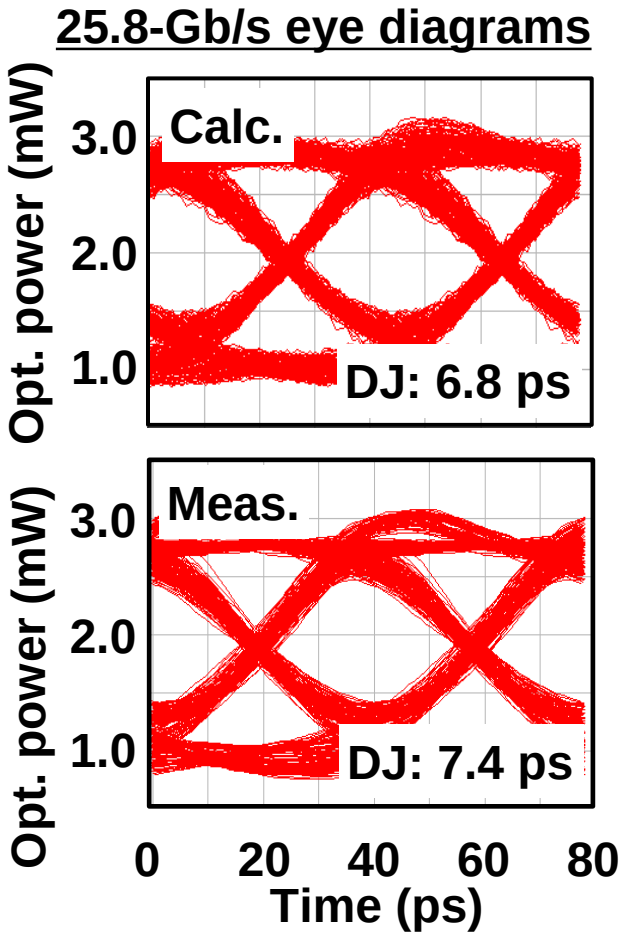
Step 2



- Step 1: Measured SR of opt. TX to extract rising/falling SRs
- Step 2: Calculated eye diagram (PRBS) based on measured rising/falling SRs

Results of SR-based LD Modeling

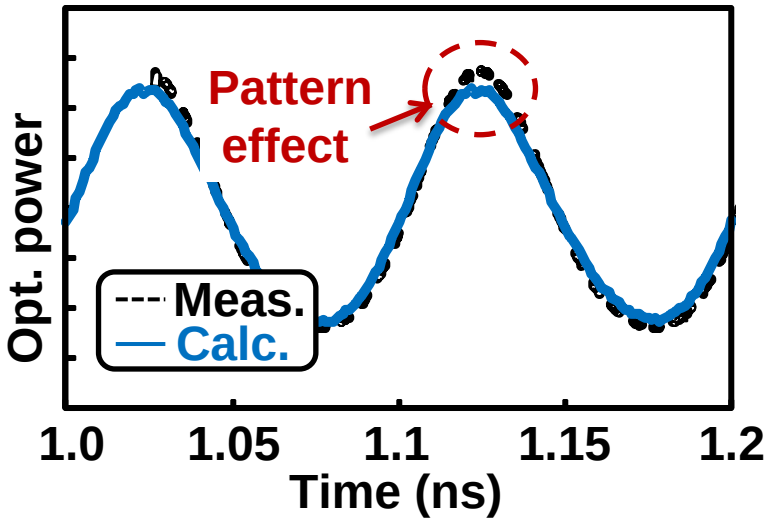




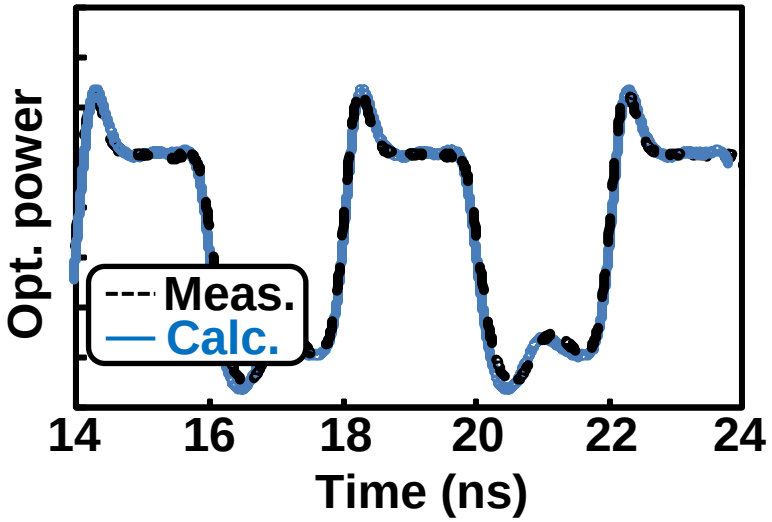
- Extracts rising/falling SRs from 16-bit sequence pattern
- Calculated eye pattern represents jitter characteristic with high accuracy (jitter error: 0.6 ps)

Issues of SR based LD Modeling

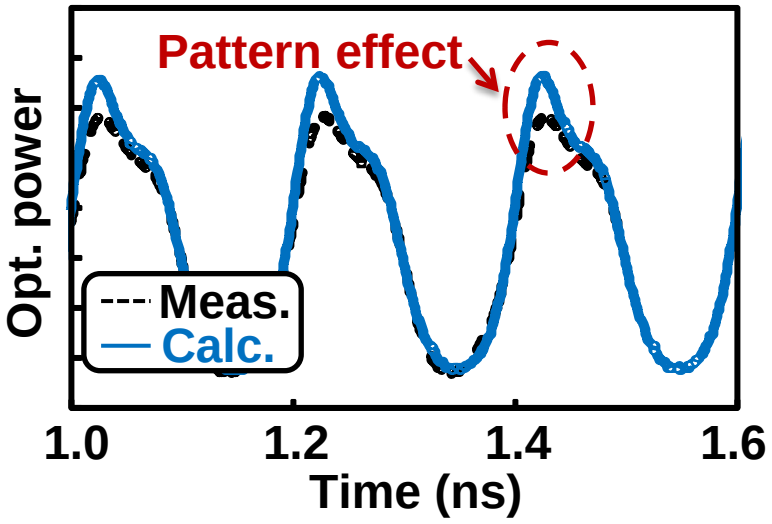
Repetitive 1 and 0 ("1010…")



4-bits sequence ("11110000…")



2-bits sequence ("1100…")



- **SR-based LD modeling:**
  - + Pattern from steady state (long sequence bit [>4bits])
  - – Pattern effect (due to time change of carrier density)
- **Corrected by adding error signal (if necessary)**

Comparison Summary of Opt. TX Modeling

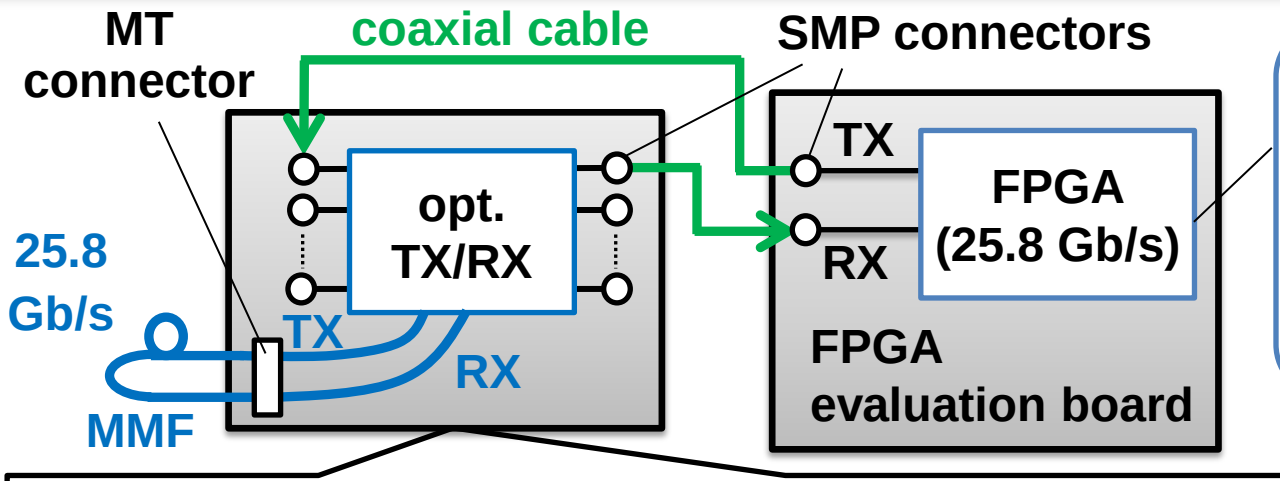
Method	Jitter error	LD nonlinearity	Pros & Cons	
Rate eq.	0.03 UI (1.3 ps)	•over/under shooting •bit-pattern effect	+ cover all LD nonlinearity – evaluate LD/LDD individually – optimization of multiple parameters	
S-param. (freq. domain)	0.12 UI (4.7 ps)	-	– large jitter error (impracticable)	+ treat modularized opt. TX as it is + simple evaluation
SR (time domain)	0.02 UI (0.6 ps)	•over/under shooting	– pattern effect (Required correction if necessary)	

- Rate eq. & SR: Practical for designing 25-Gb/s opt. Link
  - Rate eq.: Optics/circuit/opt. module designers
  - SR: ICT-equipment architecture/board designers (commercial opt. module applied)

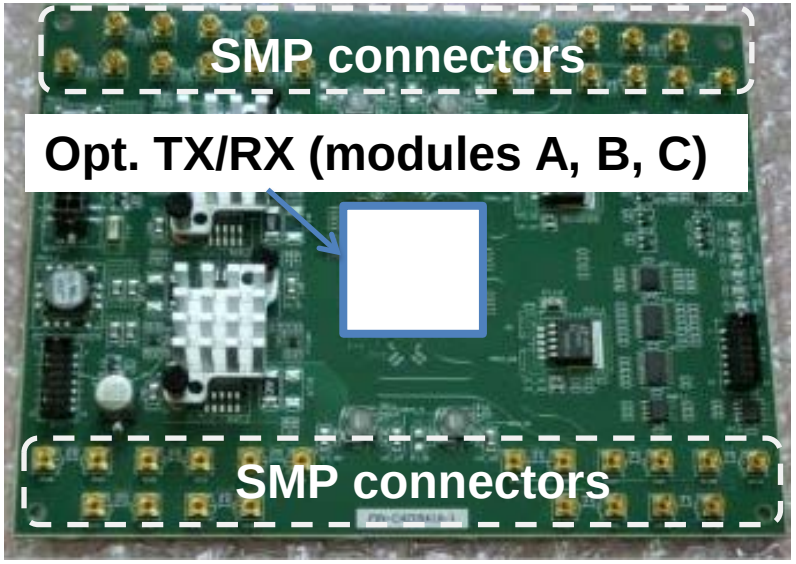
Outline

- Motivation
- Challenges and Approaches
  - Loss managements
  - Jitter managements
- Elec. and Opt. Concurrent Design Method
  - Step responses based LD modeling
- **Fabricated Opt. Link between FPGAs**
  - **Enlarged jitter margin (deterministic jitter)**
  - Reduced random jitter of LD
- Conclusions

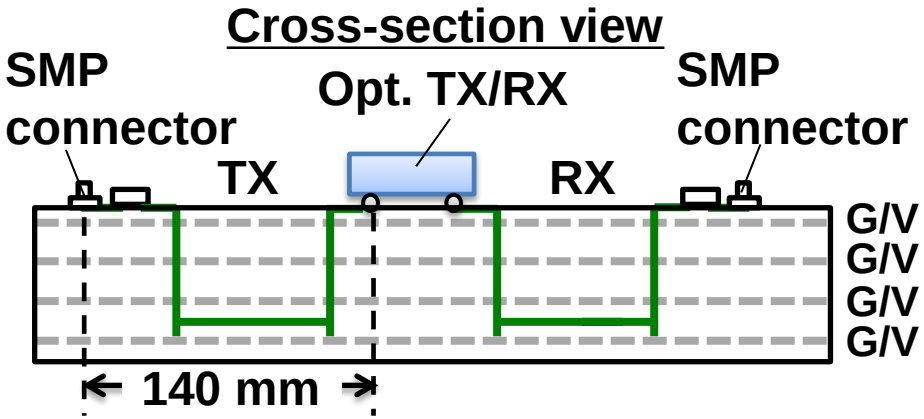
Fabricated Opt. Link between FPGAs



- Vertex-7 (Xilinx)
- 28-nm CMOS process
- w/ GTZ transceiver (max rate: 28.05 Gb/s)
  - •TX: FFE
  - •RX: CTLE & DFE



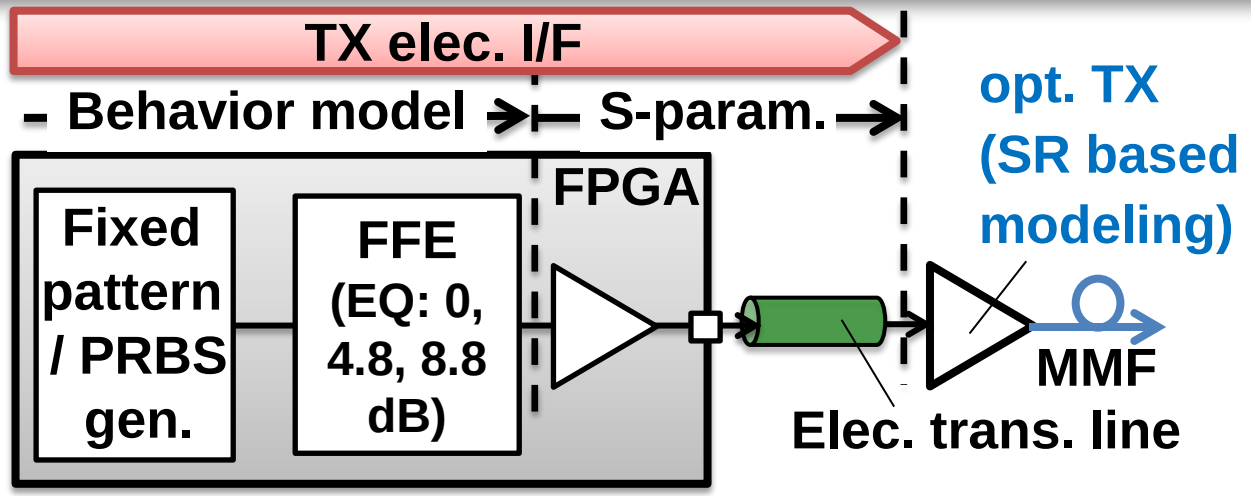
Fabricated evaluation board (mounted on opt. TX/RX)

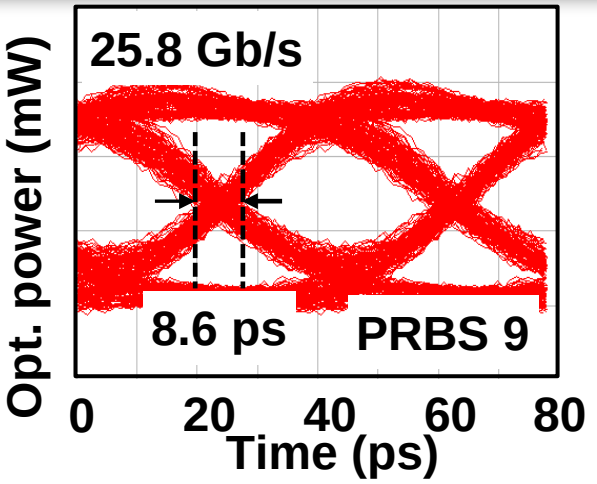


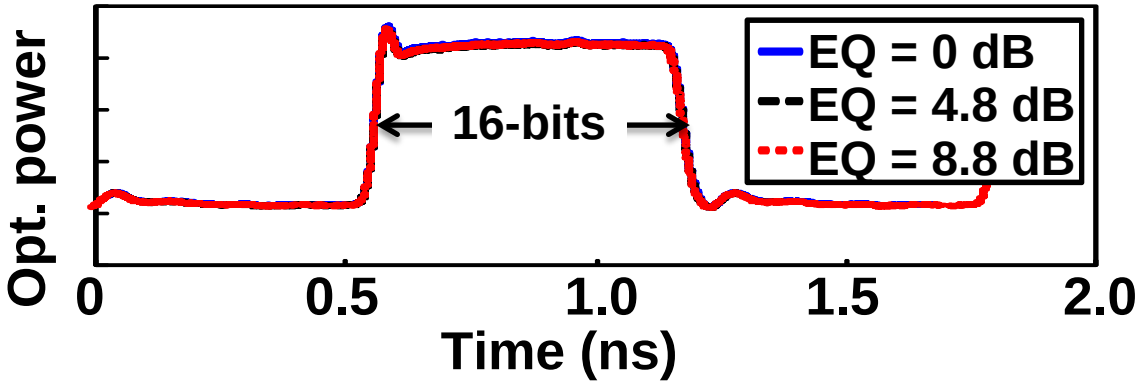
Insertion losses@ 12.9 GHz

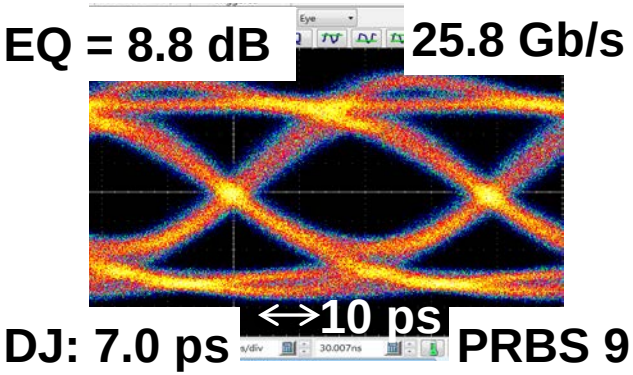
Opt. TX/RX to SMP connectors	–10 dB
SMP connectors to FPGA	–4 dB
Total	–14 dB

Applying SR-based Modeling to Opt. Link





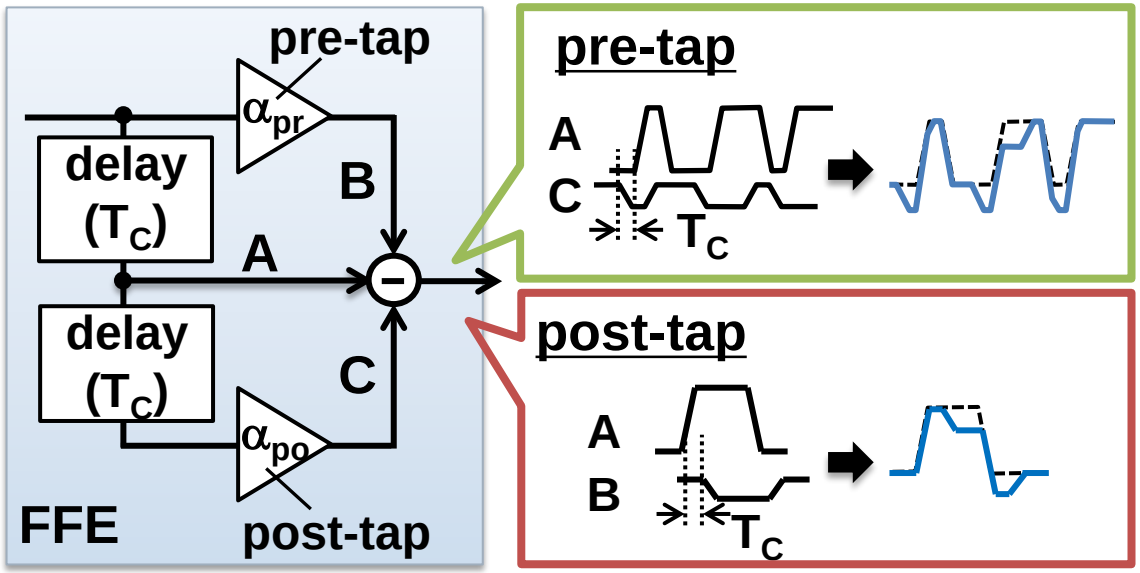




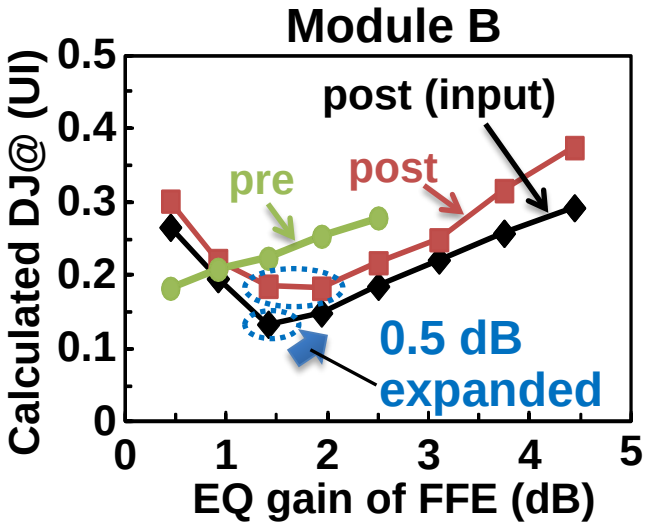
- SR-based LD modeling: Applicable to opt. link regardless of condition of TX elec. I/F
- Reproduce 25.8-Gb/s eye diagram with small jitter error (1.6 ps)

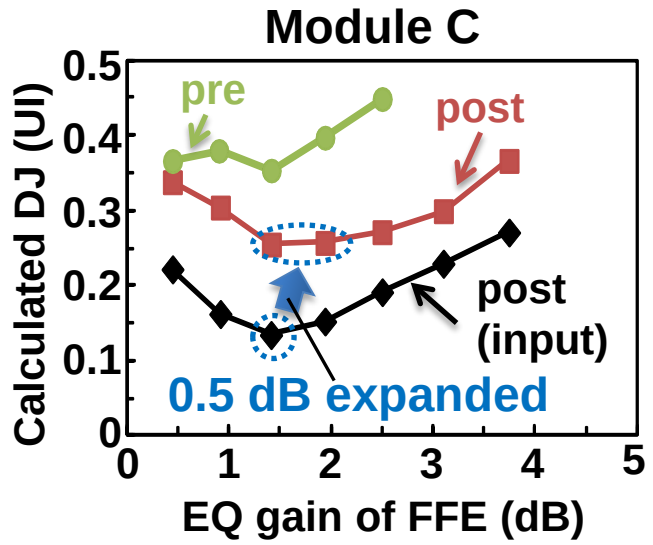
Reduced DJ due to FFE inside FPGA

Equalization of FFE (inside FPGA)



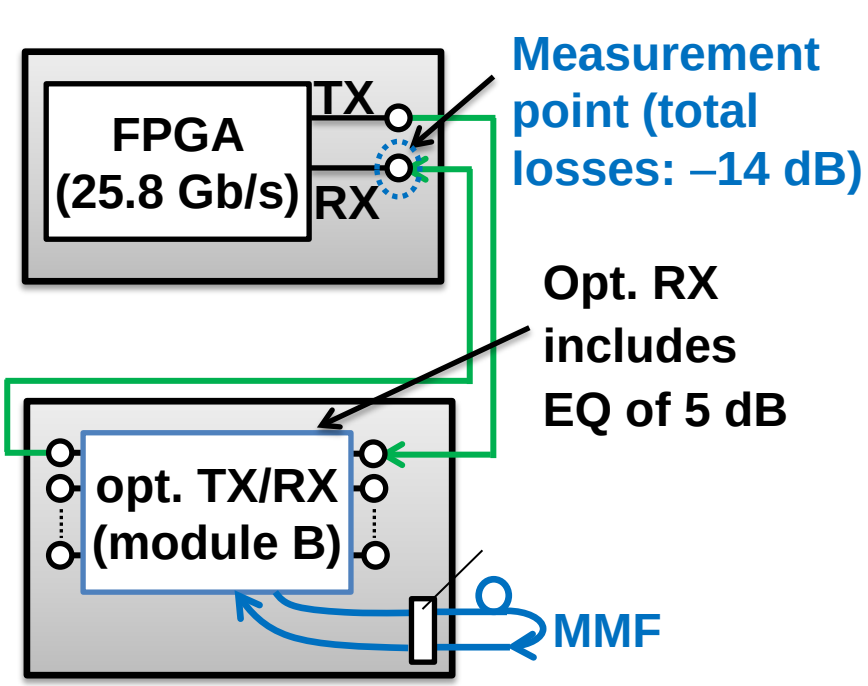
DJ@ output of opt. TX

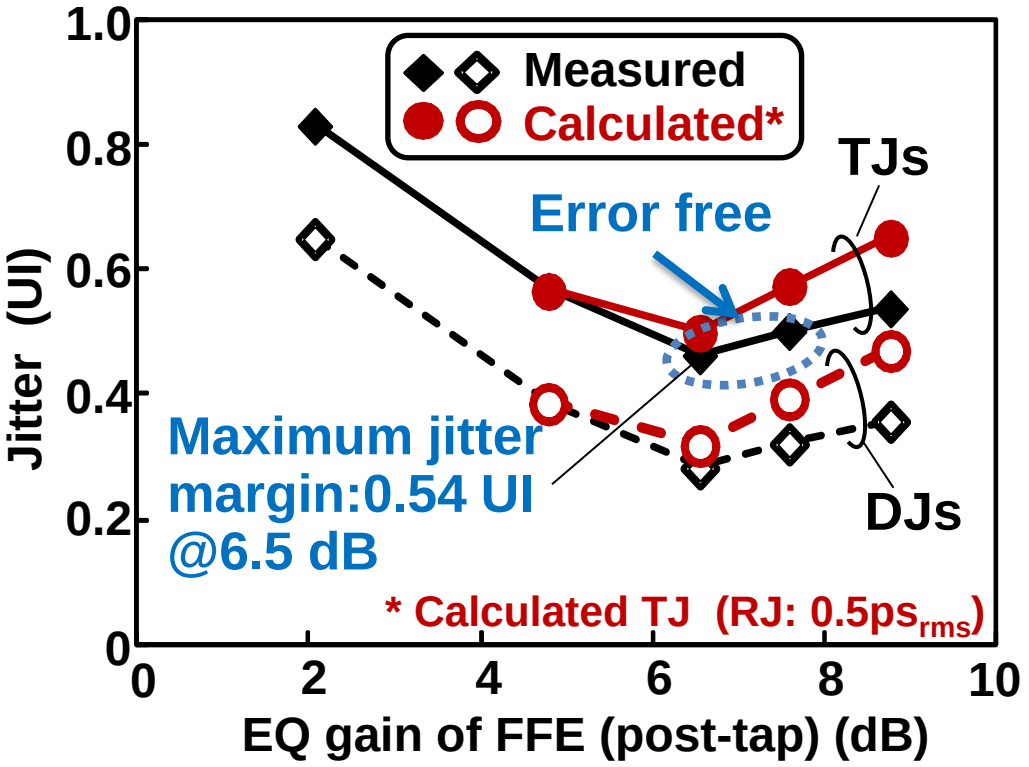




- DJ of opt. TX mainly reduced by effects of post-tap (pre-tap: shortens transition time)
- Optimized FFE including opt. TX: expand optimum equalization range (0.5 dB)

Results concerning Enlarging Jitter Margin



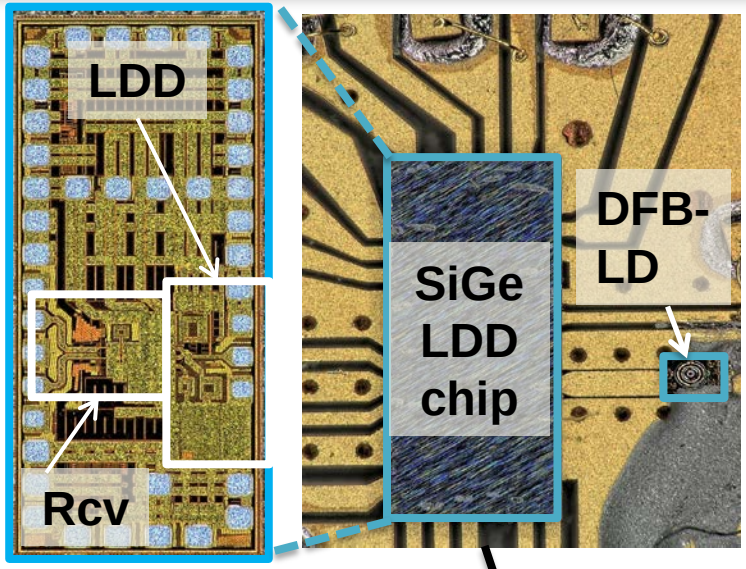


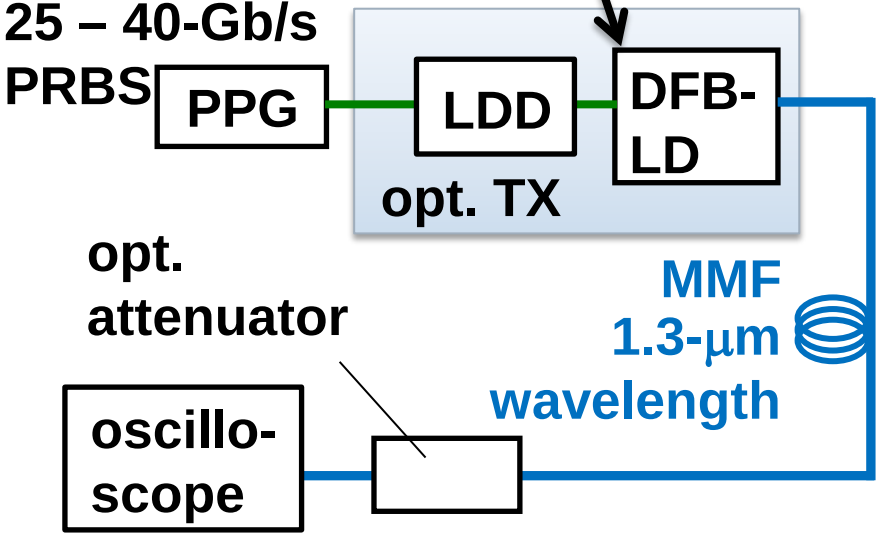
- Elec. & opt. concurrent design tool: optimized FFE inside FPGA (jitter margin:0.5 UI@ 6.5 dB)
- Measured opt. link between FPGA: maximum jitter margin (0.54 UI) at same EQ gain & error-free operation

Outline

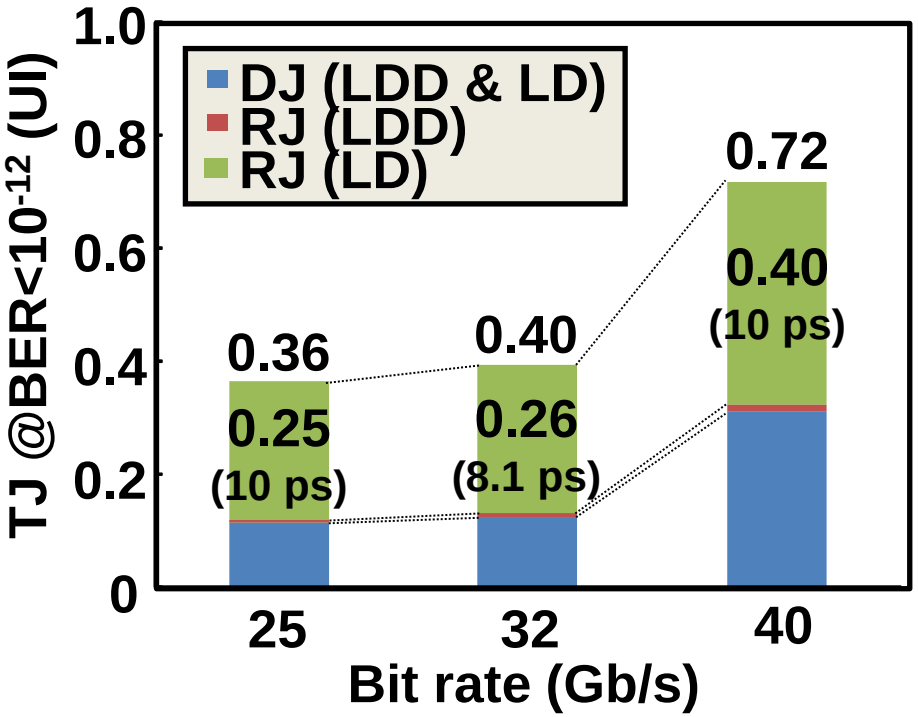
- Motivation
- Challenges and Approaches
  - Loss managements
  - Jitter managements
- Elec. and Opt. Concurrent Design Method
  - Step responses based LD modeling
- **Fabricated Opt. Link between FPGAs**
  - Enlarged jitter margin (deterministic jitter)
  - **Reduced random jitter of LD**
- Conclusions

RJ of LD (RJ_{LD}) Reduced Jitter Margin



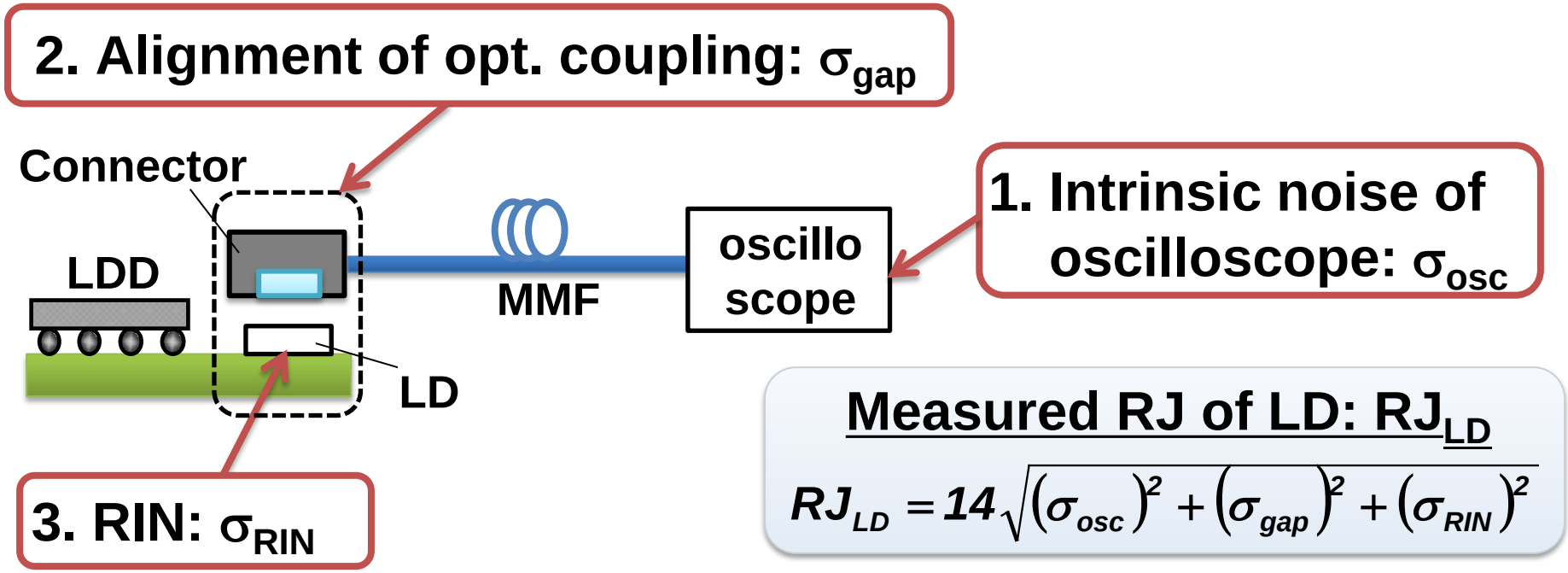


T. Takemoto et al., OFC, 2015



- Opt. TX consisting of DFB-LD & LDD (0.18-μm SiGe)
- Reduced RJ_{LD} (accounts for more 0.25 UI): Increased jitter margin (over 25 Gb/s)

Causes of Increased RJ_{LD}

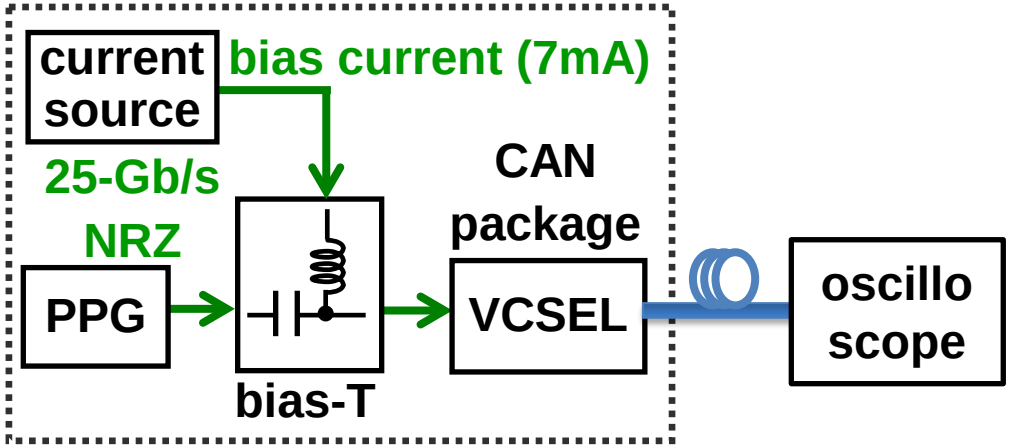


- Measured RJ_{LD} mainly determined by three components:
  1. Measurement system: RJ due to noise of oscilloscope
  2. Opt. coupling: misalignment increases RJ
  3. Opt. devices: RIN of LD

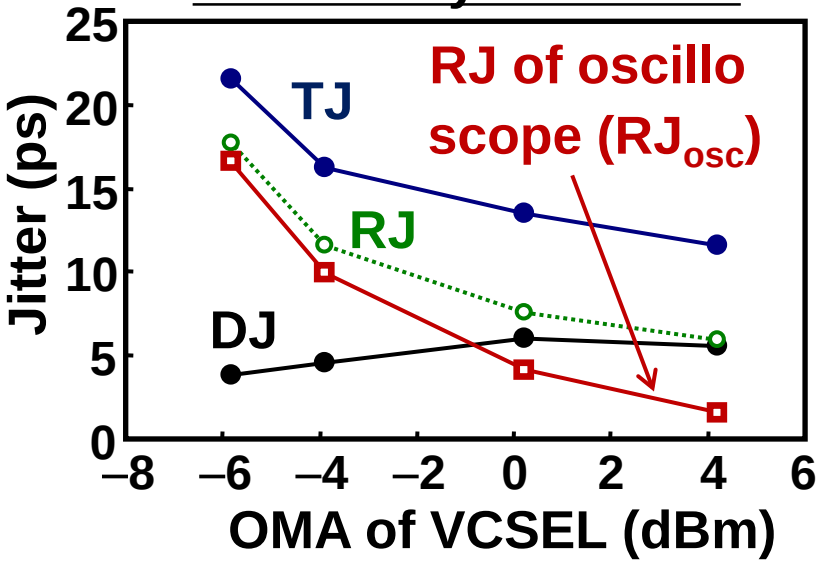
➡ Required meas. techniques to clarify their contributions

RJ Caused by Noise of Oscilloscope

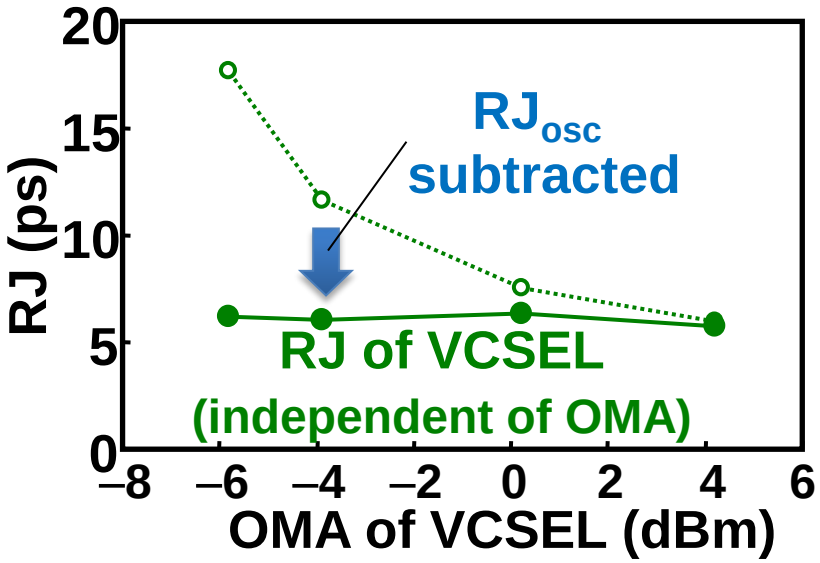
Measurement setup



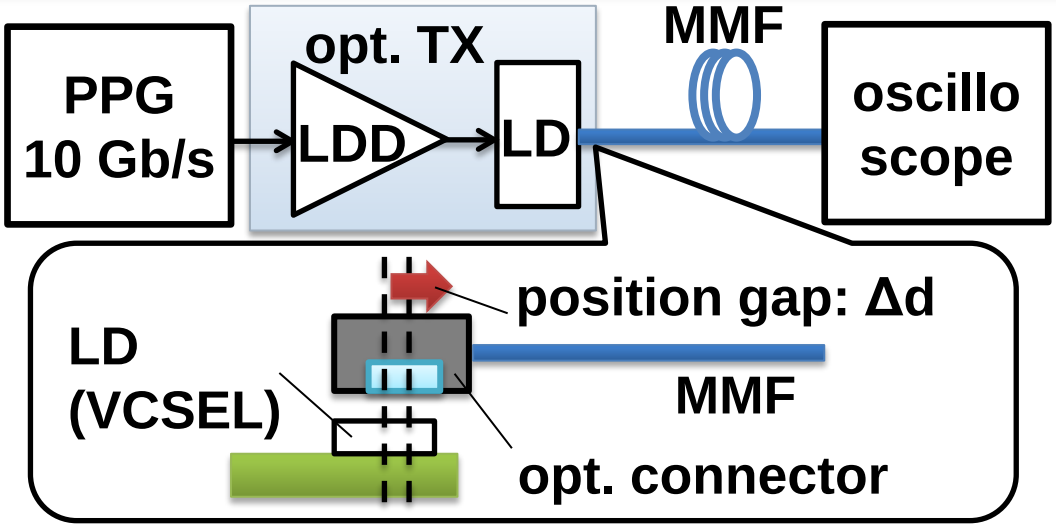
Jitter-analysis results

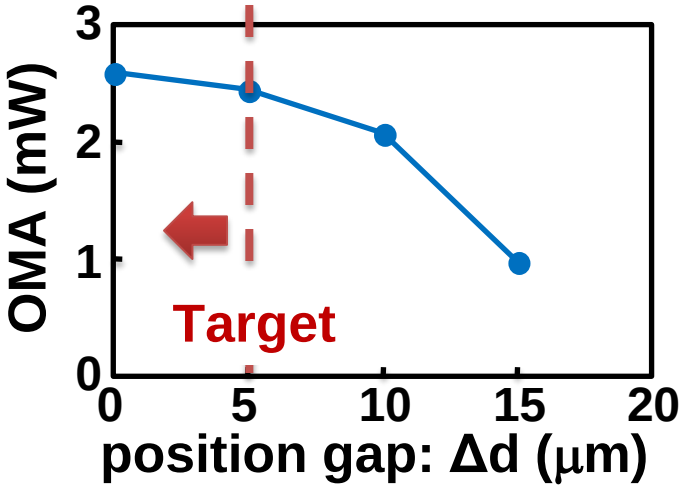


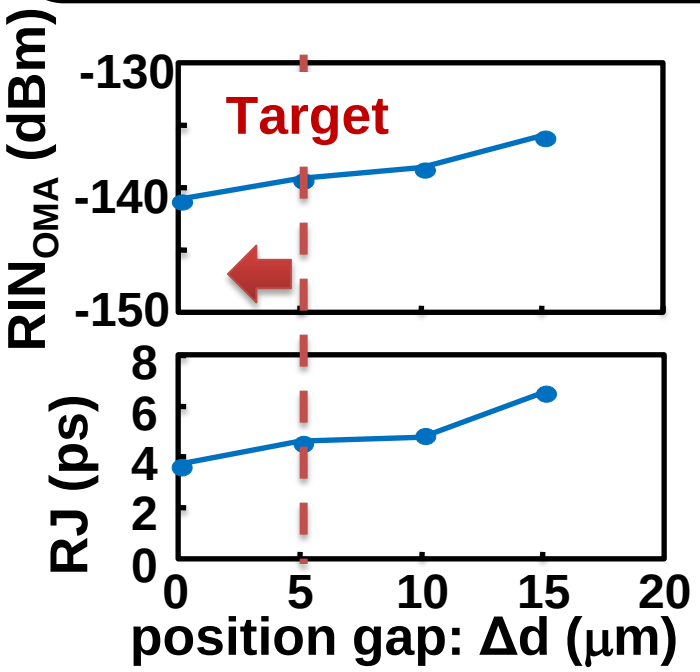
- RJ_{osc} accounts for much of measured RJ (in case of small OMA)
- RJ of VCSEL (subtracting RJ_{osc}): Constant regardless of OMA



Effects of Opt. Coupling on RJ



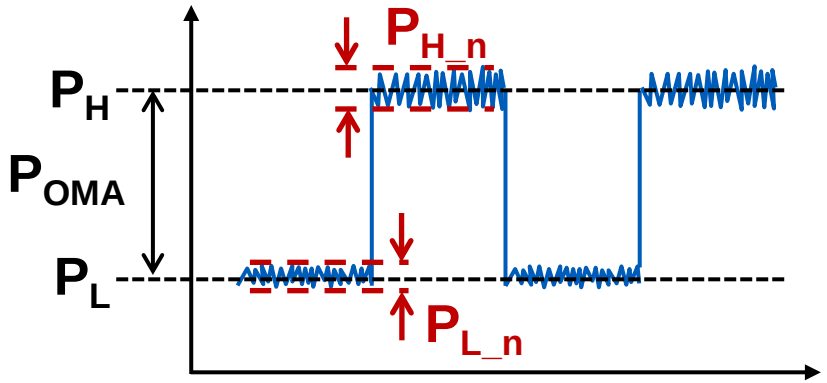


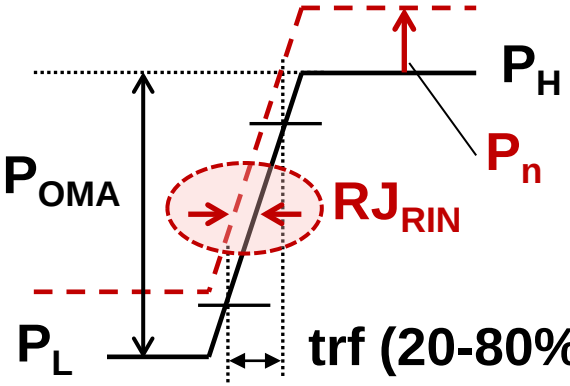


- Misalignment of opt. connector: Not only reduced OMA but also increased RIN_{OMA}/RJ
- Effects of position gap negligible ($\Delta d < 5\ \mu m$)

RJ due to RIN

- RJ of LD mainly determined by RIN_{OMA}
- RJ_{RIN} depends on rising/falling time & extinction ratio (ER)





$$RJ_{RIN} = 14\cdot(trf/0.6)\cdot[BW\cdot 10^{RIN_{OMA}/10}]^{1/2}$$

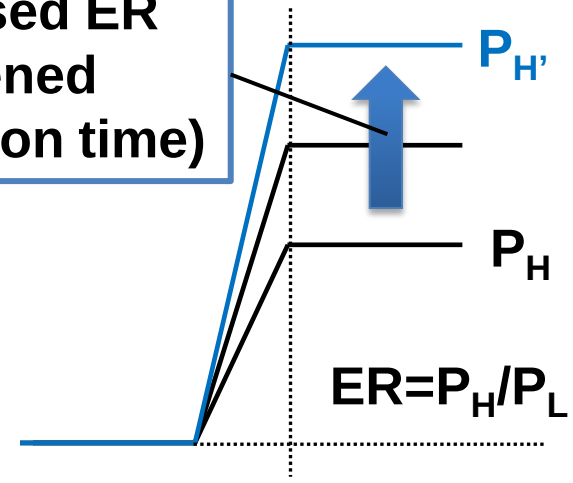
$$RIN_{OMA} = 10\log_{10}[(P_n/P_{OMA})^2/BW]\ (dB/Hz)$$

P_n: averaged noise power $[= (P_{H\_n} + P_{L\_n})/2]$ (W)

RIN: relative intensity noise

BW: 0.5 × bit rate

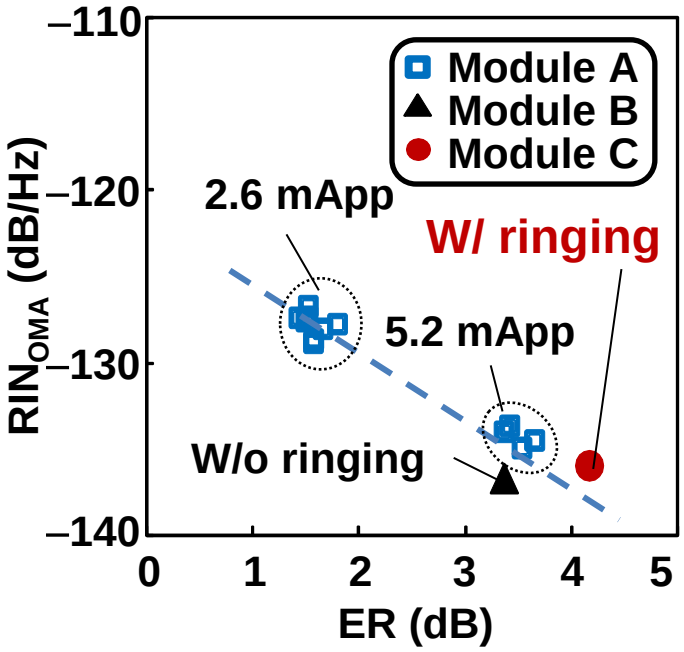
Increased ER (shortened transition time)

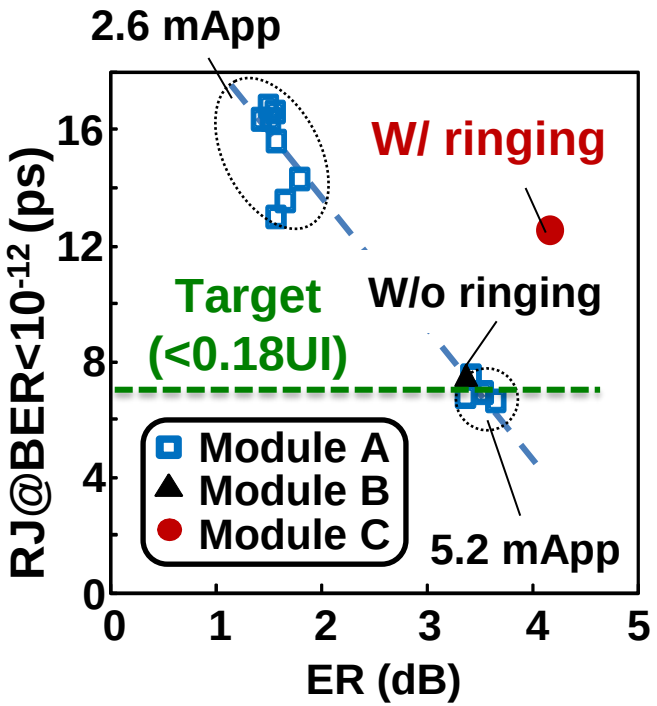


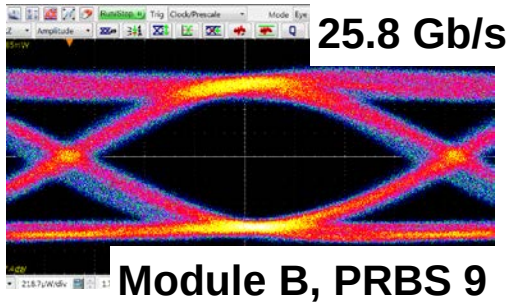
Maxim Integrated Products, Inc., Application Note: HFAN-9.1.0

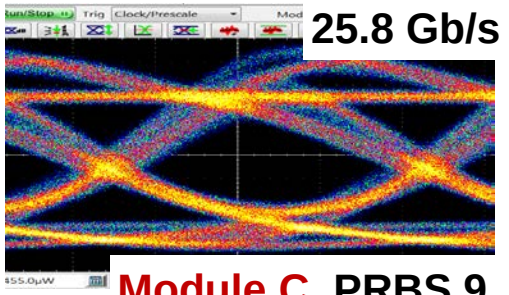
Measured Relationship between RJ and ER

Measured results using opt. link between FPGAs



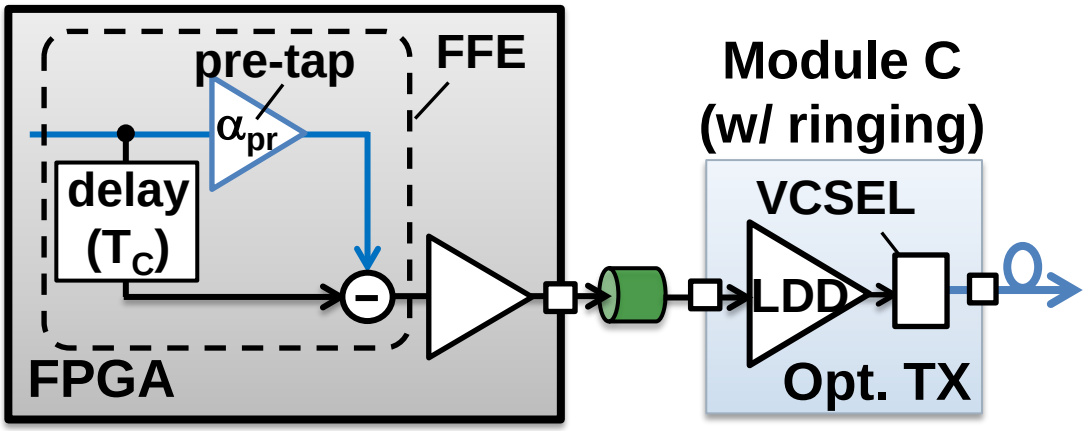


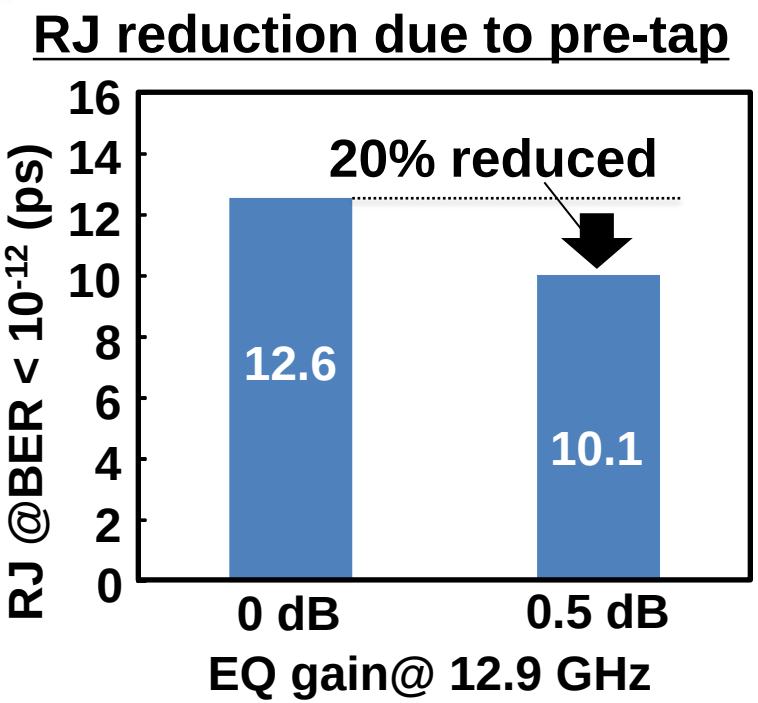


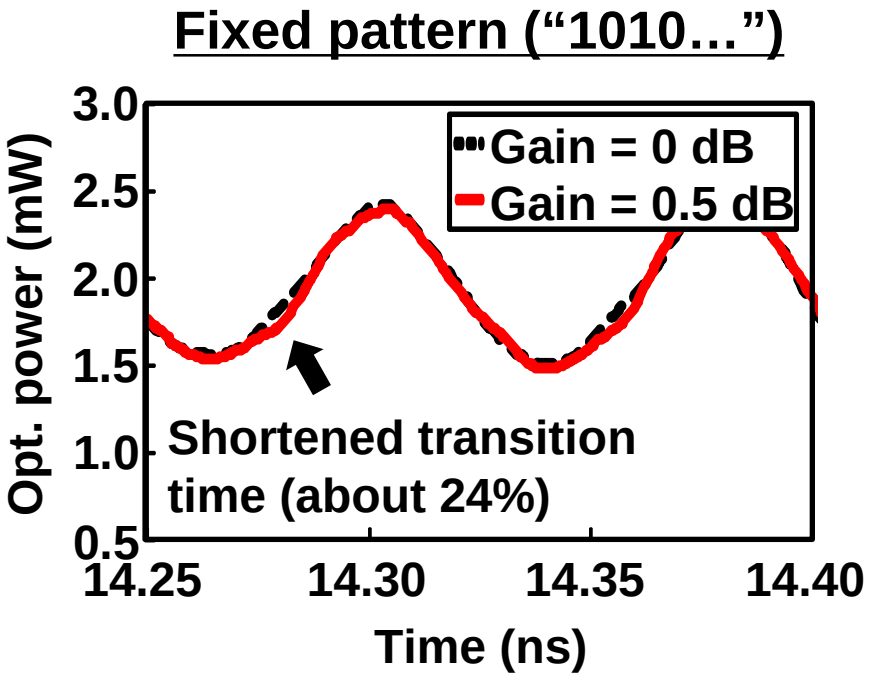


- Reduced RJ: Sufficient ER (>3.5 dB) required to suppress RIN$_{OMA}$
- Ringing (lengthen transition time): Increased RJ regardless of ER

Reduction of RJ using FFE inside FPGA







- Effect of reducing RJ using FFE inside FPGA
- Pre-tap shortens transition time of opt. TX (about 24%)
  - ➡ 20% reduction in RJ

Conclusions

- **25-Gb/s-class optical interconnects:**
  - **Accommodate sever jitter budgets**
- **Electrical & optical concurrent design method:**
  - **Step-response (SR)-based LD modeling: Reproduce eye with small jitter error (<0.6 ps)**
- **25.8-Gb/s optical transmission between FPGAs:**
  - **Enlarged jitter margin (0.54 UI) optimizing EQ gain of FPGA**
  - **Reduced RJ due to RIN by shortening transition time (20%)**
- **Determines optimized placements of opt. module inside ICT system if SR available at design phase**