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Timing in-situ monitors: implementation strategy and applications results

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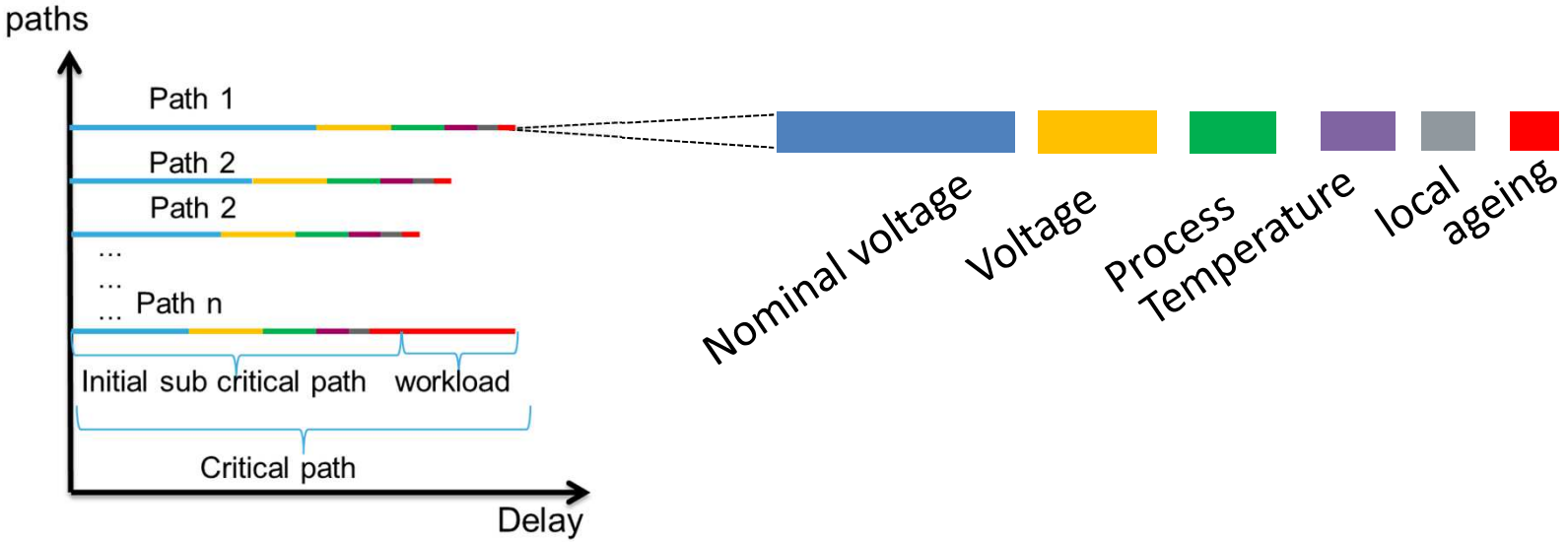
Reliability context

- Reliability aims at decrease the failure rate requirement for automotive, consumer, spatial market…
  - Decreasing fault occurrence
  - Improving process capability or design for reliability
- How to optimize the trade-off between reliability, performance and power?
- Innovative solutions: In-situ timing sensors

Context

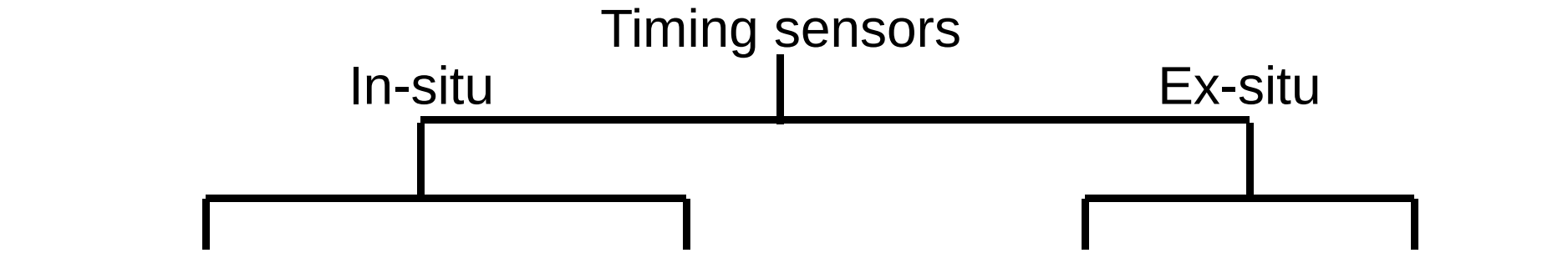
- Multi mode multi corners approach
  - Adding extra margin under worst case conditions

    → Huge performance-power-area penalty



- In-situ timing monitor could eliminate extra margin :
  - Provide warning prior to functional failures
  - Deal with environmental variations and aging

Contributions to the field



- Static pre-error detector [1]
- Dynamic pre-error detector [1]
- Crystal-ball circuit [2]
- transition detector[3]
- Step circuit [4]
- Slack Probe technique[5]

- Razor circuit [6]
- Timber circuit [7]
- Stability checker detector[8]
- Sampling data detector[9]
- Double sampling with time borrowing[10]
- Sense amplifier detector[11]

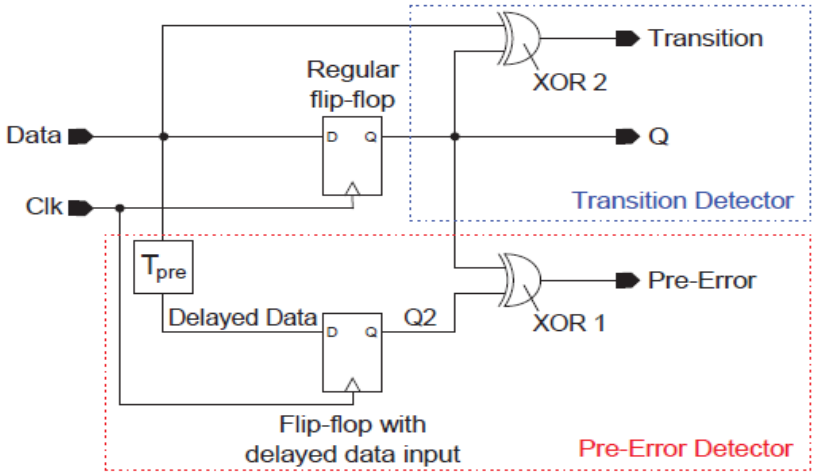
- Path-based ring oscillator[13]

- High-speed critical path monitor[12]

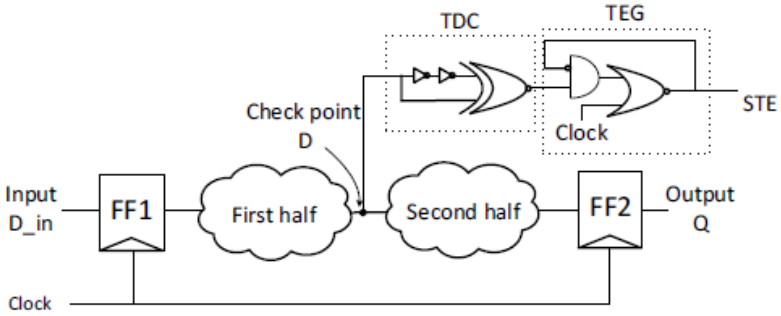
[1] N. Pour *Et al.* 2013
[2] S. Eireiner *Et* al., 2007
[3] D.Bull E*t al.* 2011
[4] S.YOUSHIDA 2014
[5] L.LAI P.Gupta 2013
[6] A. Bowman *Et al.* 2008
[7] R. Choudhury *Et al.* 2012
[8] P. Franco *Et al. 1994*
[9] M. Nicolaidis 1999
[10] A. Bowman, W. Tschanz 2008
[11] Y. Tsiatouhas, S. Matakias 2013
[12] J.Park , J.A Abraham 2011
[13] X. Xang 2008

Pre-error monitors

- Example 1: Static pre-error detector
  - Aging sensor: pre-error detection
  - Detected transition close to rising edge of clock
  - It detects also the activity on data path.
- Example 2: transition detector
  - Check point is placed in the middle of the critical-paths
    → Pre-error under-estimated if inserted on the first-half
    → Pre-error over-estimated if inserted on the second-half
  - Error signal if transition occurs after failing edge of clock
    → lack of pre-error prediction



[N. Pour 2013]



[S. Youshida 2014]

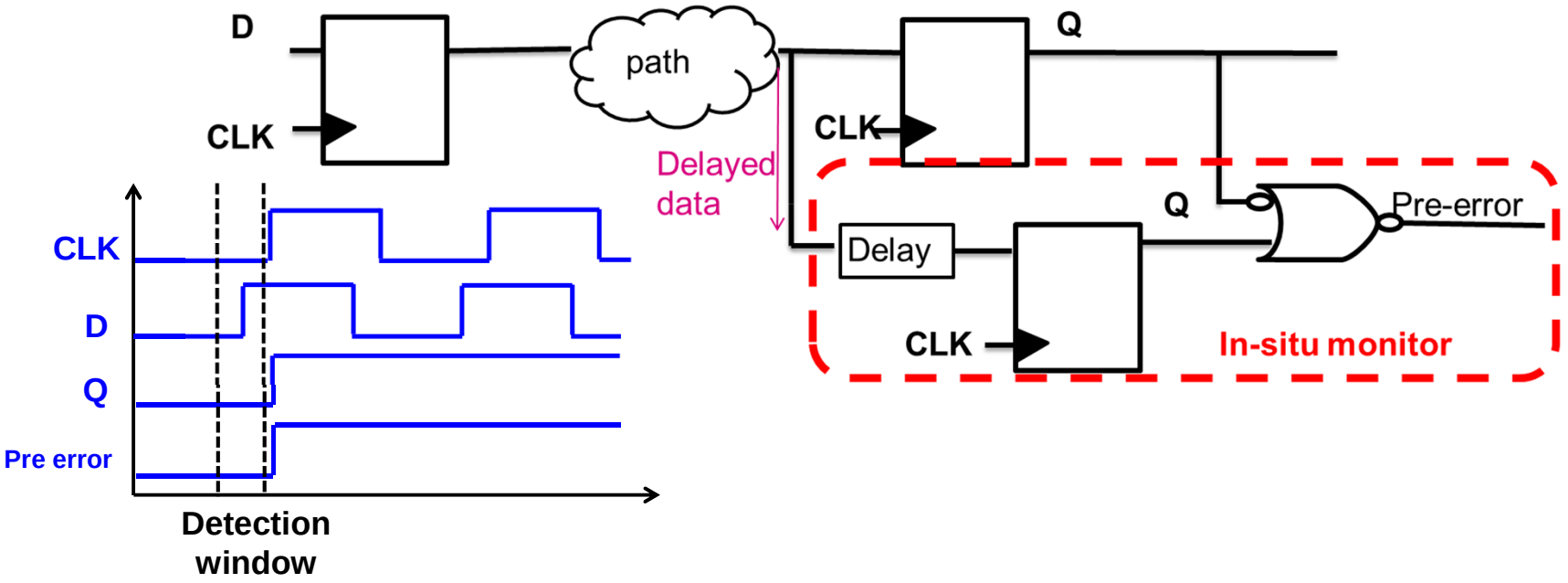
Outline

- Design for in-situ monitors
- Insertion flow for in-situ monitors
- Benchmark results after P&R
- Experimental silicon measurements
- Conclusion and prospects

In-situ monitors principle

Principle

- Data is delayed, latched and compared with the original one
- Detection window size is determined by the delay element

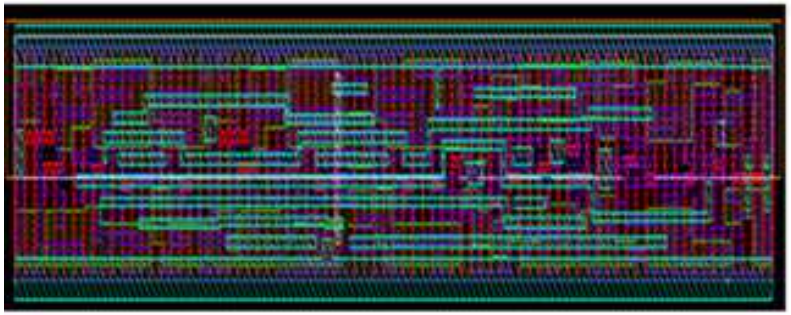


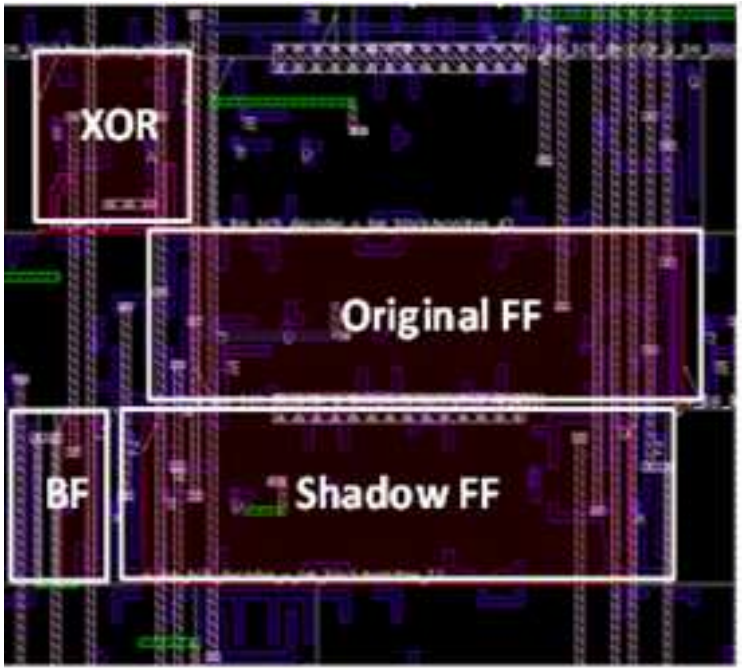
- Delay element : buffer = 30 ps * *M.Saliva 2015

- Pre-error is high if transition occurs on detection window

Layout strategies

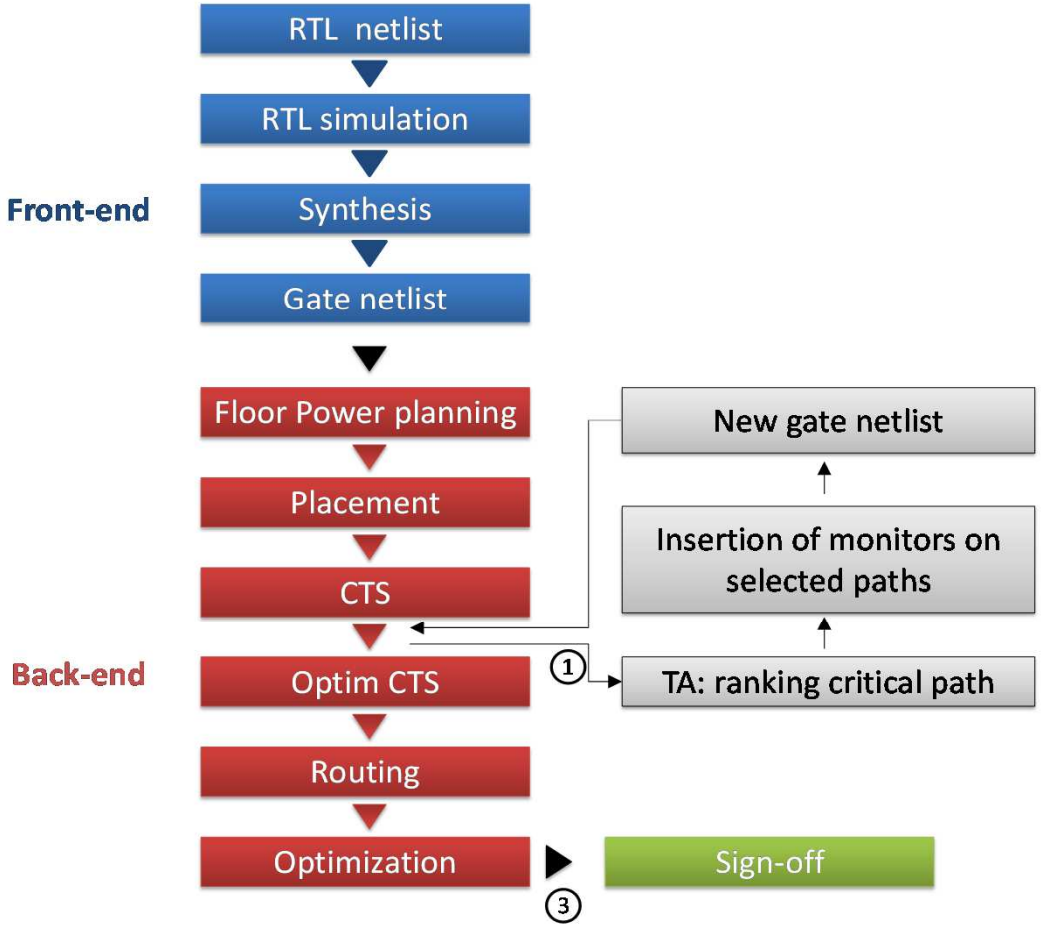
- Cell-based in-situ monitor
  - Need dedicated cell characterization compatible with industrial back-end flow
  - Optimal footprint area but :
    - → Difficulty to handle during the flow
    - → Routing congestion due to cell size
- Flow-based in-situ monitor
  - All components come from libraries
  - Schematic is flexible
  - Connectivity is managed during routing task
    - →Easy to handle during the flow
    - →No routing difficulty

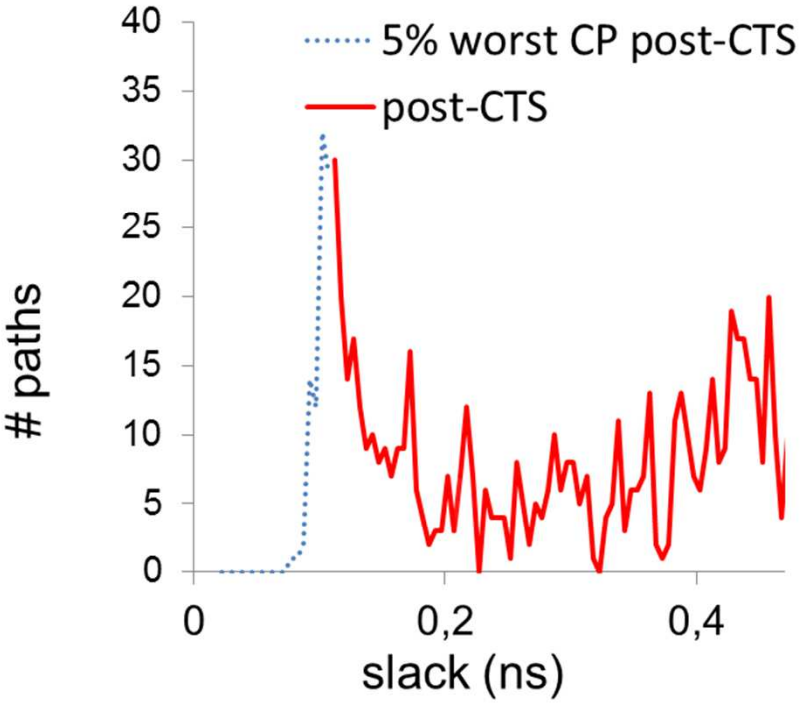




Insertion flow (1/2)

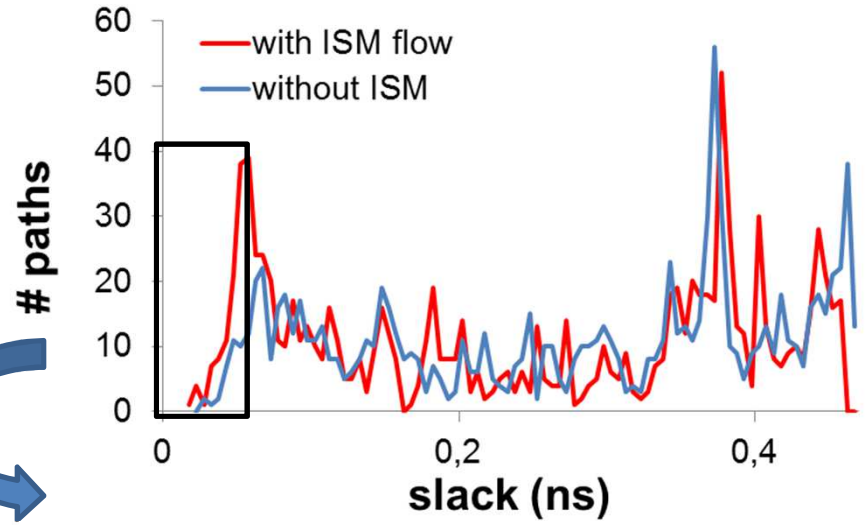
- Monitors are inserted after clock tree insertion step
- 5% of worst critical paths identified after clock tree synthesis step are monitored (dashed line)

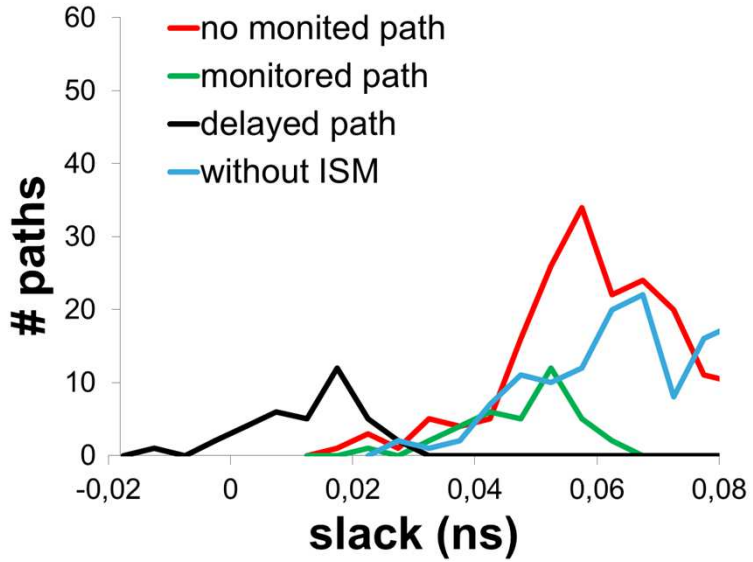




Flow insertion (2/2)

- After routing and optimization step
  - Path to monitor flop are false path
    → No penalty for original paths
  - 40% of initial paths monitored are inside 5% of critical paths considered
  - Path ranking change is due to routing optimization (setup, hold)
- Critical Path coverage
  - During long term application the probability to activate monitored path is high → **coverage during stress is guaranteed**





Benchmark area results

- 10% of critical paths are implemented with ISM
- Circuits
  - ITC99 [b19,b15,b14]
  - Bose, Ray-choudhury, Hocquenghem (BCH)* *V.Huard IRPS2014

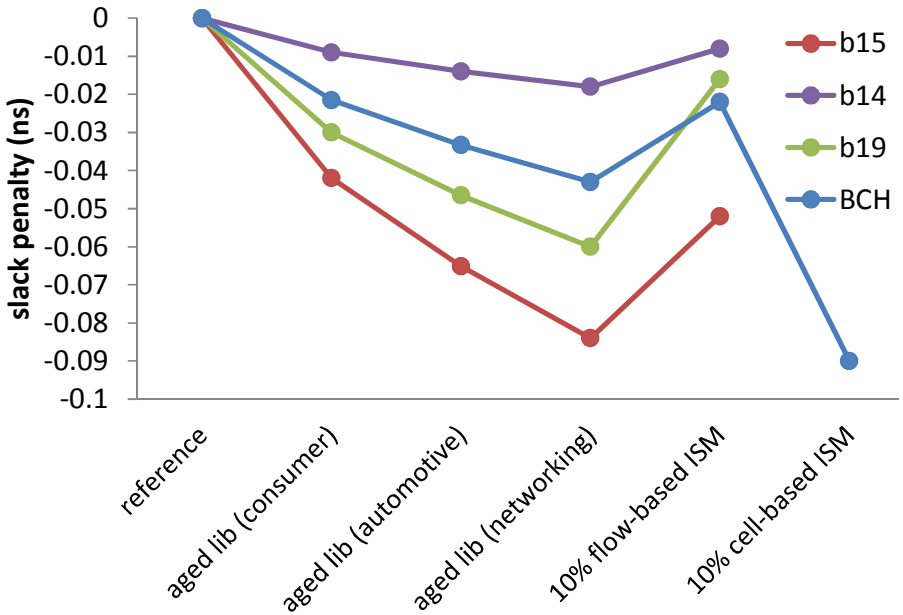
	# of gates	# of Flip-Flop	Area [µm2]	# of in-situ monitor	Area overhead [%]
B19	36211	2180	39429	218	4,16%
B14	7405	222	10139	22	2,01%
B15	14194	446	21769	44	3,58%
BCH	8469	869	11614	86	2,46%

→ Low area overhead for flow-based ISM

Benchmark performance

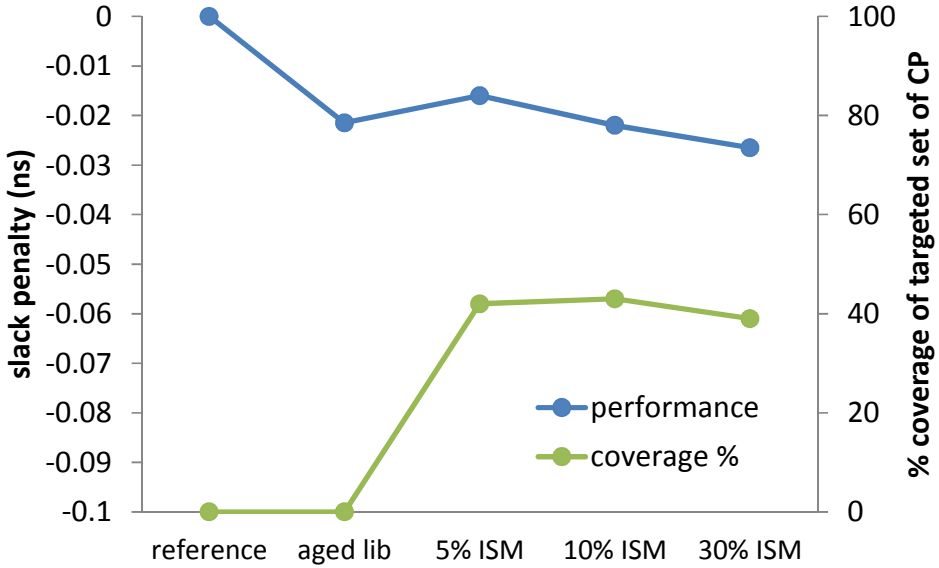
- Timing performance comparison for ITC circuits & BCH
  - Using fresh libraries and different ageing libraries
  - Using flow-based In-situ monitor for 10% of critical paths
  - Using cell-based In-situ monitor (only for BCH)

→ More penalty performance for ageing library comparing to in-situ monitor (flow-based)



Timing performance penalty

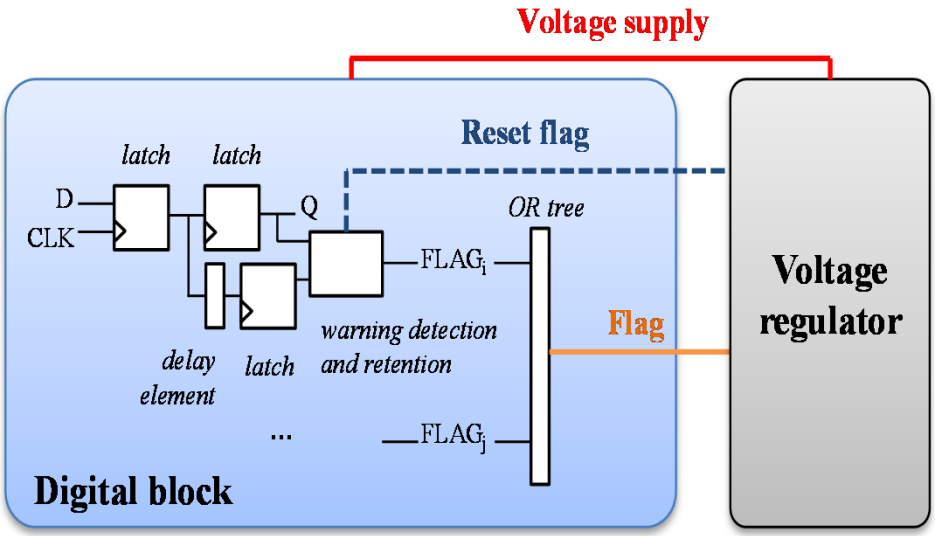
- Only for BCH
  - Using reference (fresh) and ageing library
  - For different percentage of critical path with in-situ monitor insertion

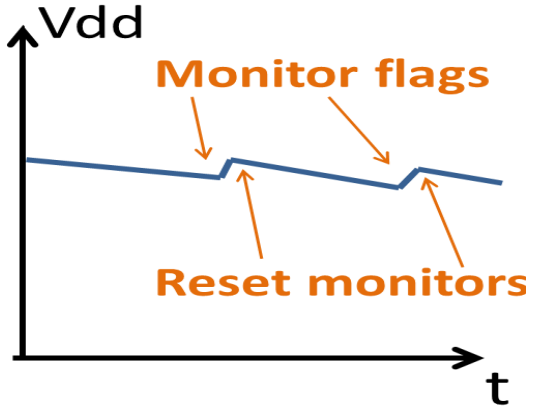


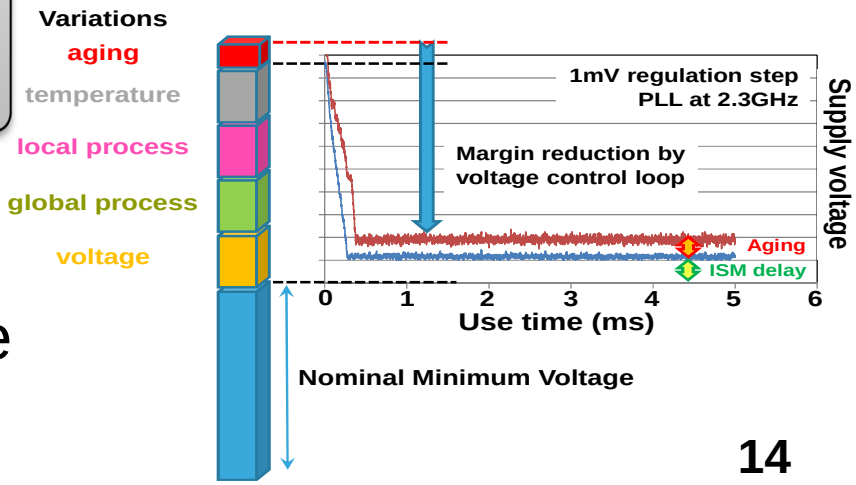
→ Performance penalty is slightly impacted with high number of in-situ monitor

Experimental results

- Application :18 independent cores of BCH implemented in 28nm Fully Depleted SOI (FDSOI) at 1GHZ



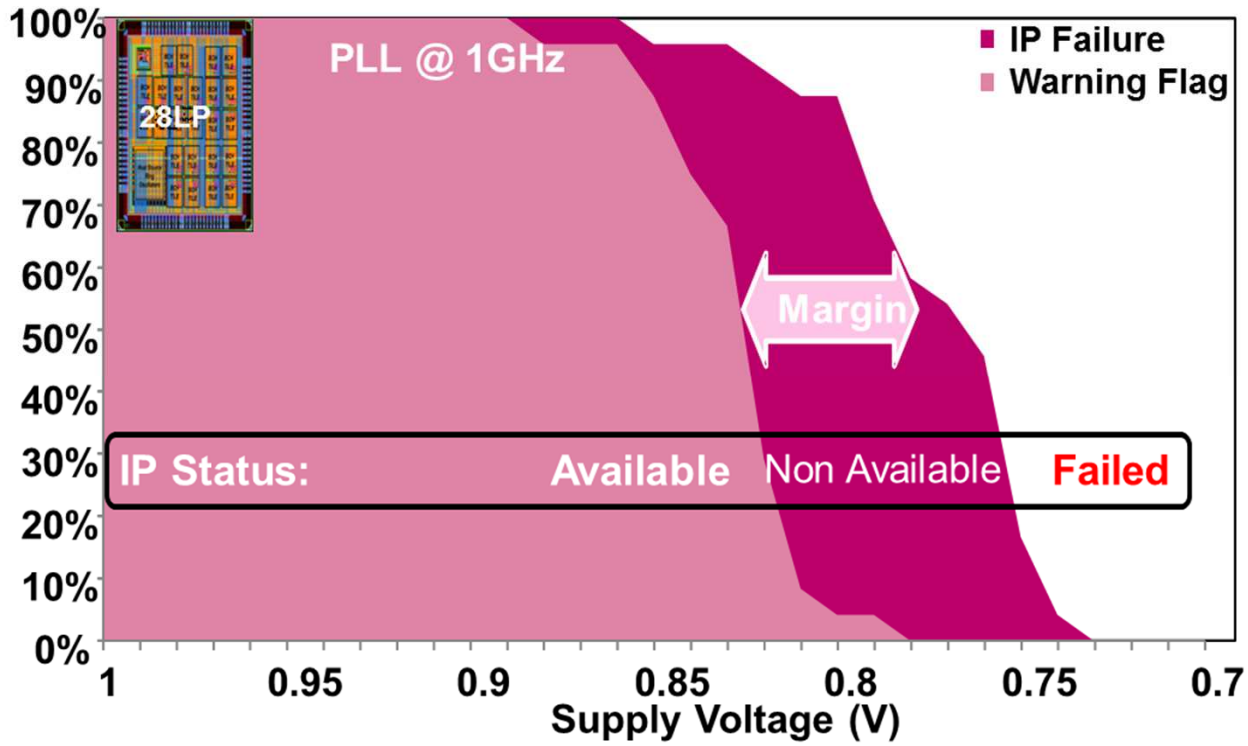




- Voltage regulation with 1mV step after first flag appearance

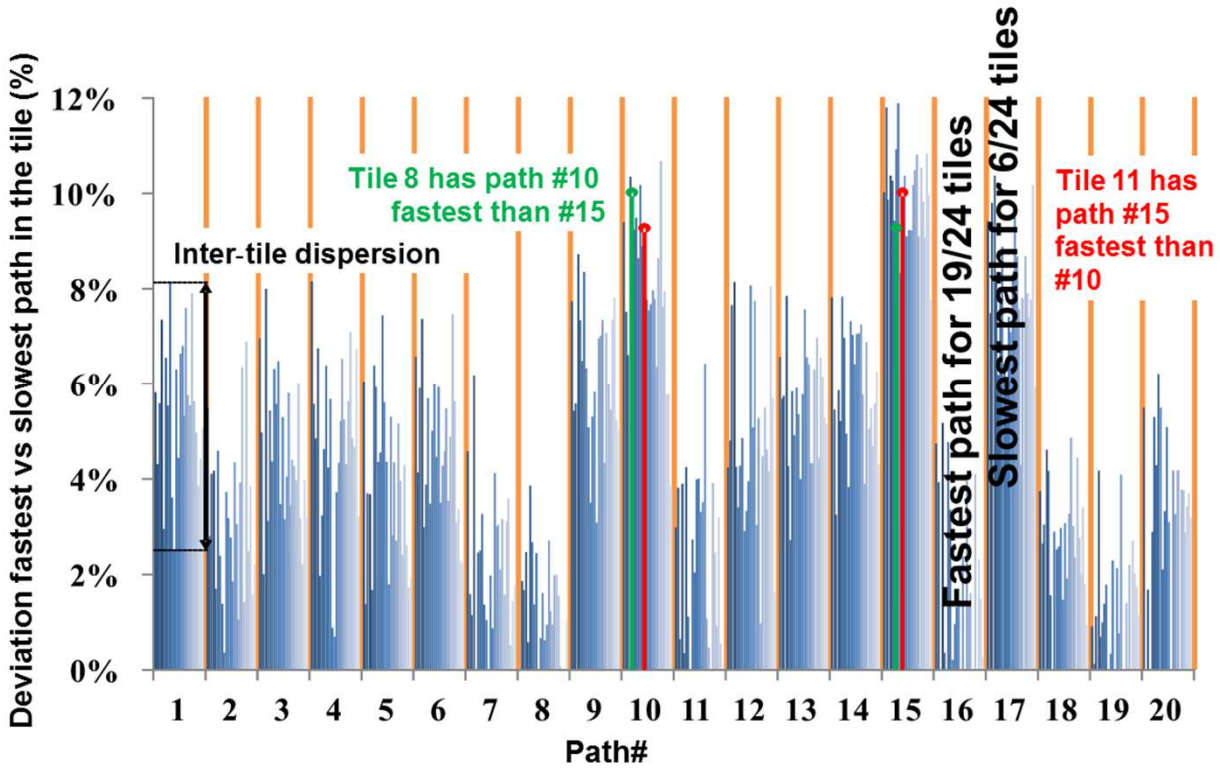
Flag warning in multicore

- Decrease V_{DD} by 1mV for all cores
  - First warning occurs at 0,89V
  - Vmin = 0,85V whereas sign-off condition (PLL@1GHz , Vmin@0,9V)
    → Extra margin of 50mV could be saved



Inter tile dispersion

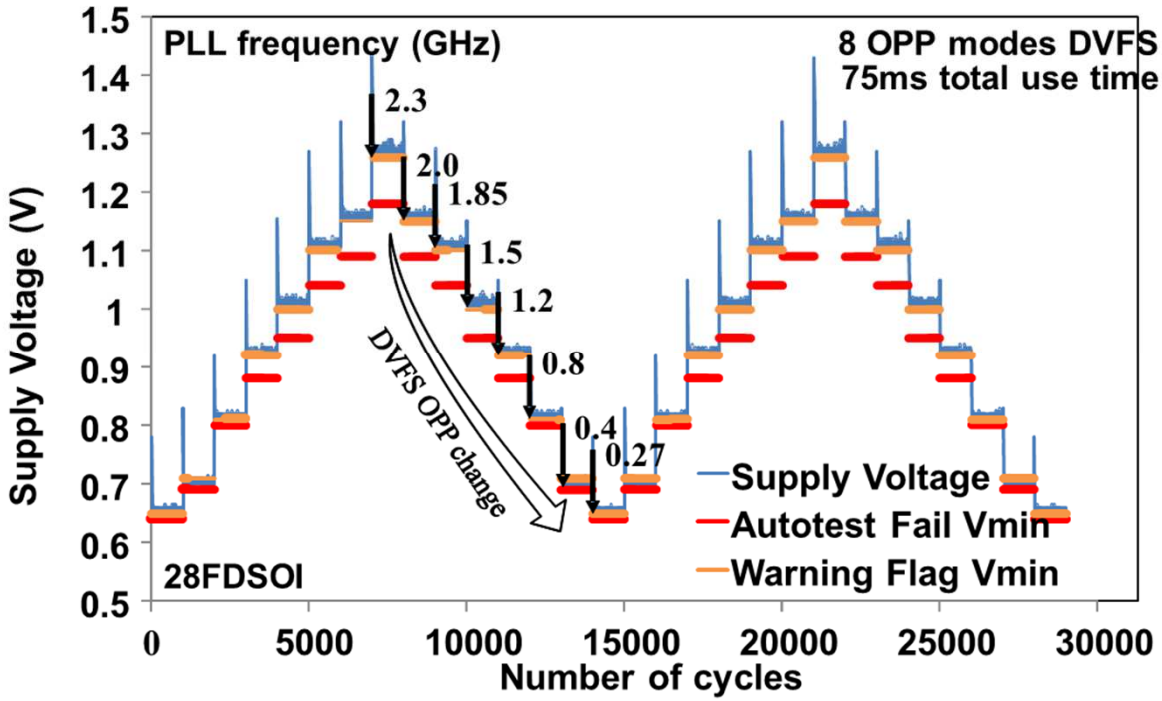
- Path timing analysis
  - Measurement of timing slacks for 20 paths in 18 tiles
    - → Each path slack differs from one tile to another
    - → Dispersion of timing slacks is due to local variations



→ Ability for in-situ monitors to cope with local variation

DVFS driven by ISM

- Each Operating Performance Point (OPP) is associated to one condition of frequency
- Clock frequency varies from 0,27 GHz to 2,3GHz
  - For each frequency, the voltage is decreased in order to avoid flags at minimal voltage

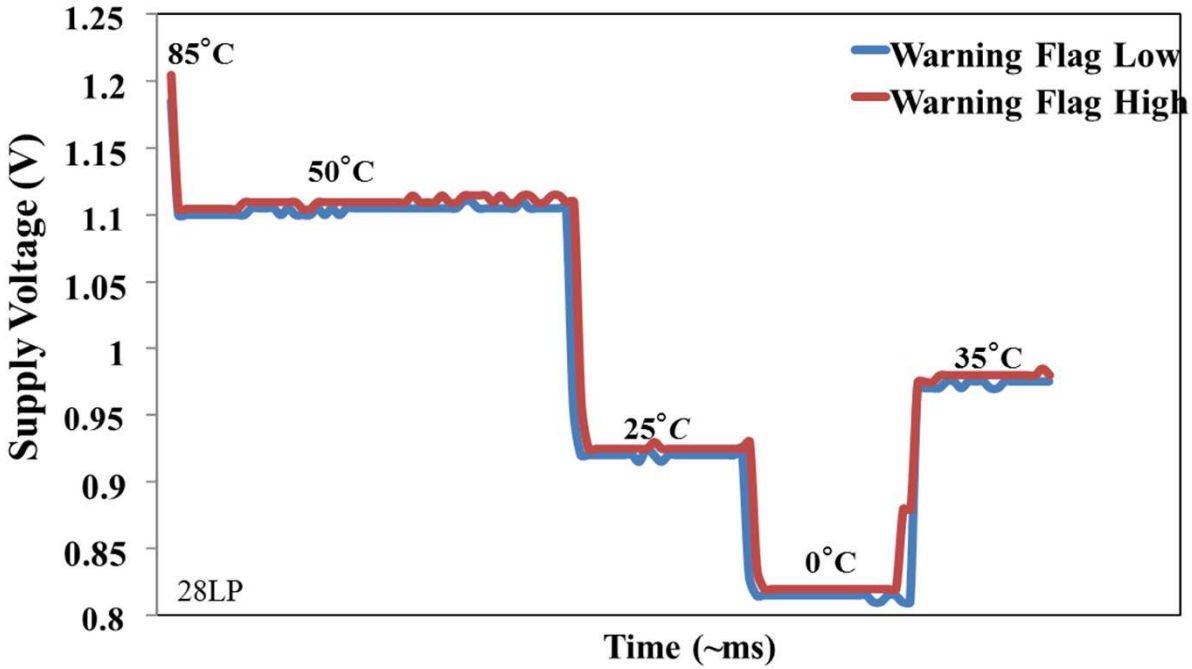


→ Ability to find minimum voltage at a given frequency without doing sign-off at each OPP

In-situ monitor and temperature change

- Application of temperature variations
  - Monitor flags to each temperature decrease

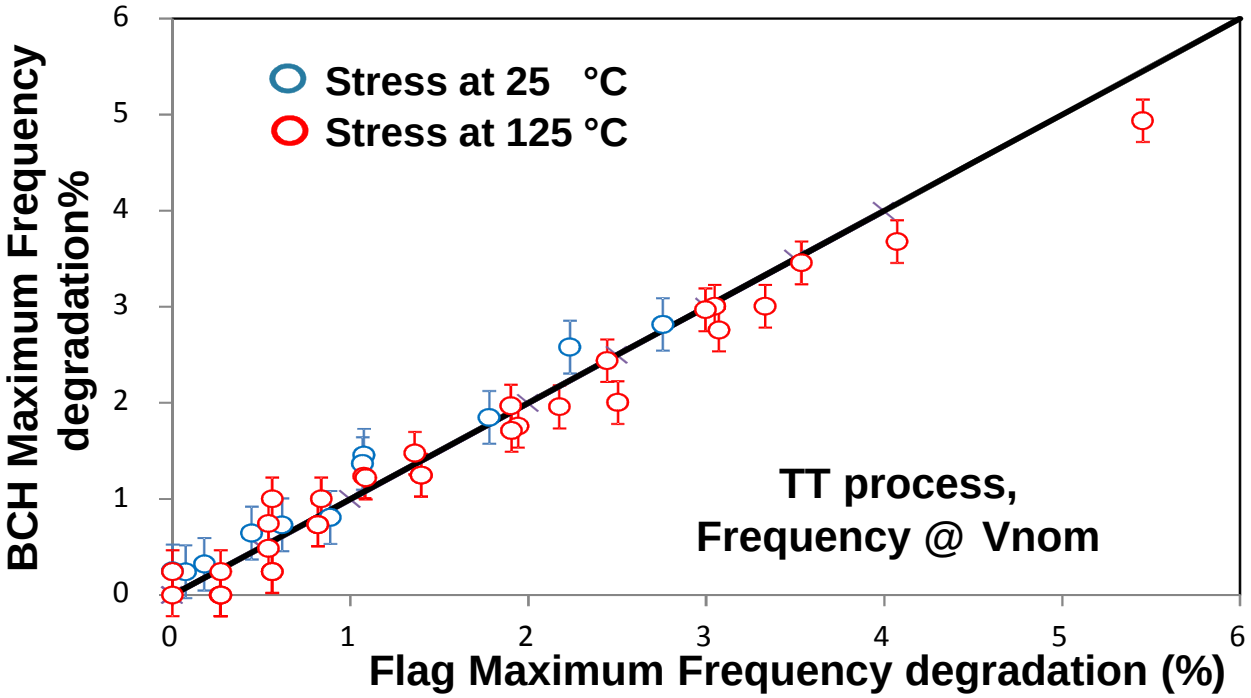
  → Voltage is adjusted accordingly



  - Support of abrupt temperature change
  - Good correlation between supply voltage and temperature variations

In-situ monitor behavior during ageing

- Aging conditions:
  - Dynamic pattern running at-speed (1GHz+)
  - V_{nom}+20 and +40% stress voltages and 25/125°C stress temperatures



- Good correlation between BCH Fmax and Flag Fmax

Conclusion

- In-situ monitor implementation solution is proposed
  - Minimum Area overhead
  - Limited timing impact
  - Industrial implementation
- Robustness of coverage investigated
  - 40% initial selection of path for ISM insertion is not a blocking point.
  - Decision taken after large number of warning alerts
- Experimental results are promising
  - ISM enables to control temperature, voltage, ageing variation
  - ISM enables to anticipate local/global process variation
- Prospects
  - Investigate the optimal number of ISM inserted