# Aging-Aware Adaptive Voltage Scaling in 22nm High-K/Metal-Gate Tri-Gate CMOS

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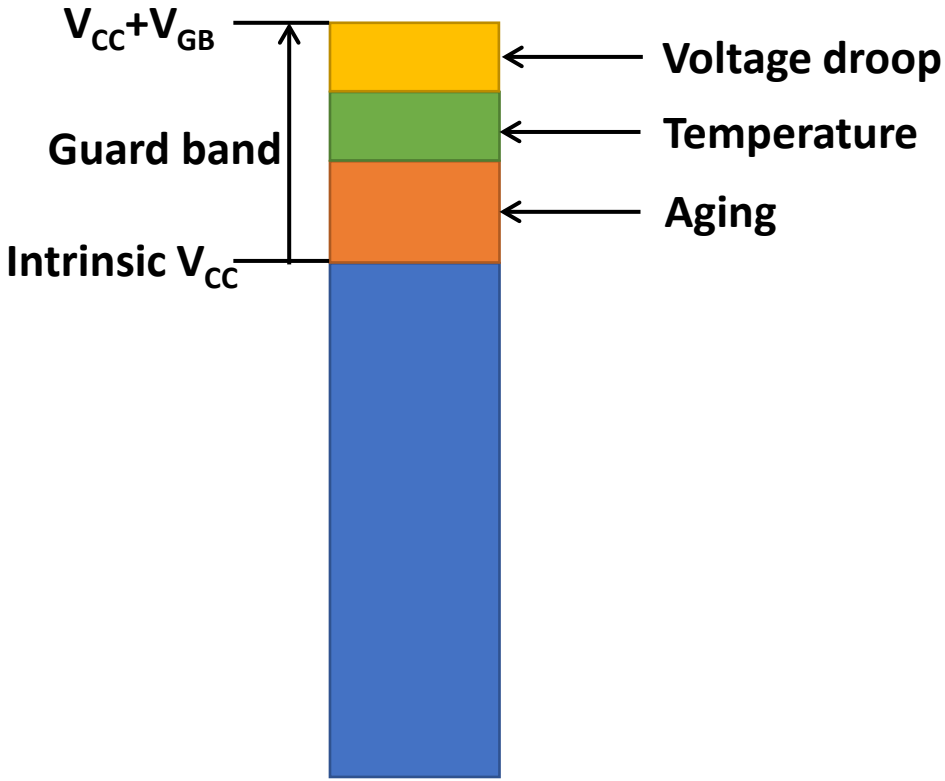
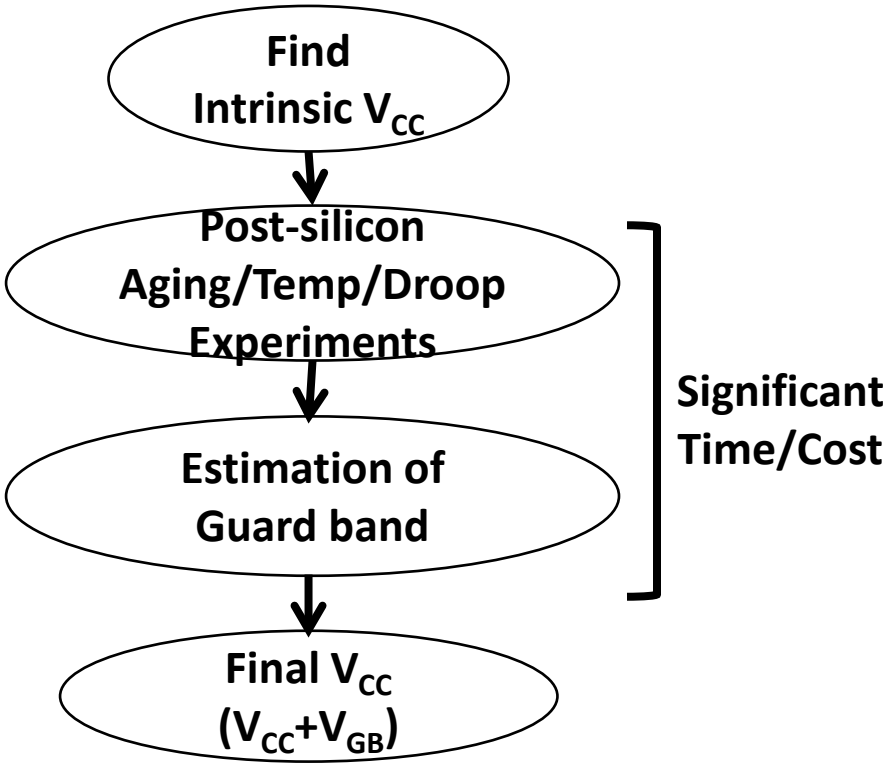
# Outline

- Conventional guard banding approach
- Proposed aging-aware Adaptive Voltage Scaling (AVS) approach
- Aging mechanism
- Aging-aware AVS design details
- Simulation results
- Testing and measurement results
- Conclusions

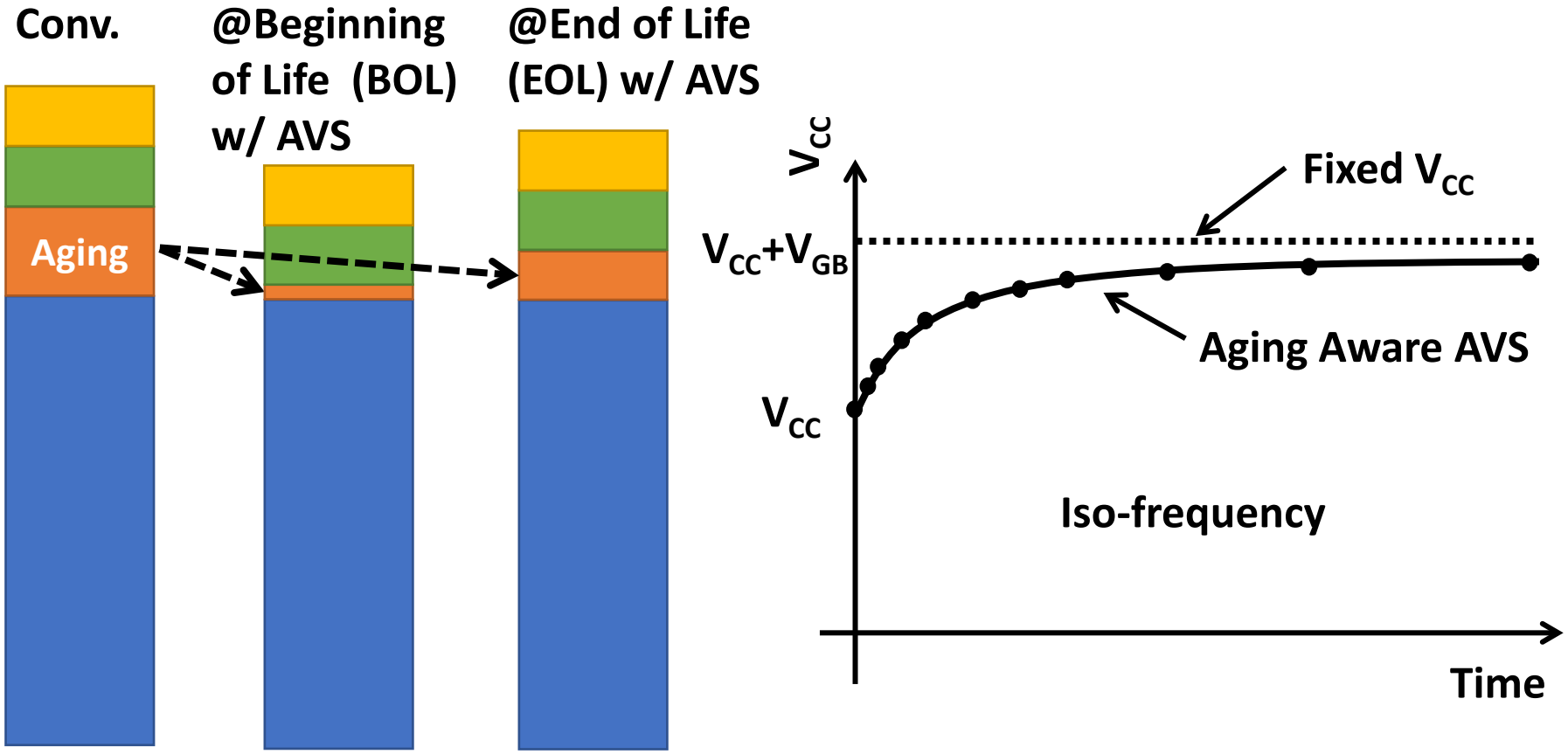
# Conventional Approach Using Fixed Voltage Guard band




- Conventional approach needs to estimate each guard band (Cost), unnecessary higher operating $V_{CC}$ (Power)

# Proposed Aging-Aware Approach
# Adaptive Voltage Scaling (AVS)




- The operating $V_{CC}$ is adjusted periodically to compensate for any aging-induced frequency degradation
- A given system can operate at minimum $V_{CC}$ during lifetime depending on actual stress cycles

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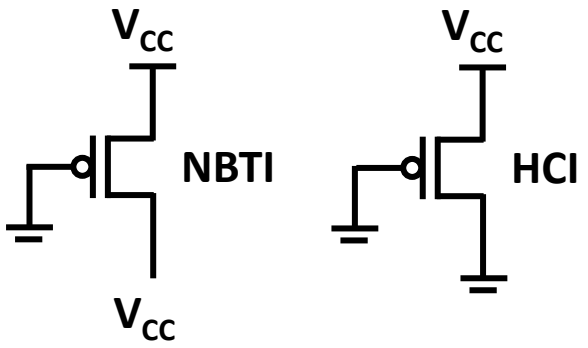
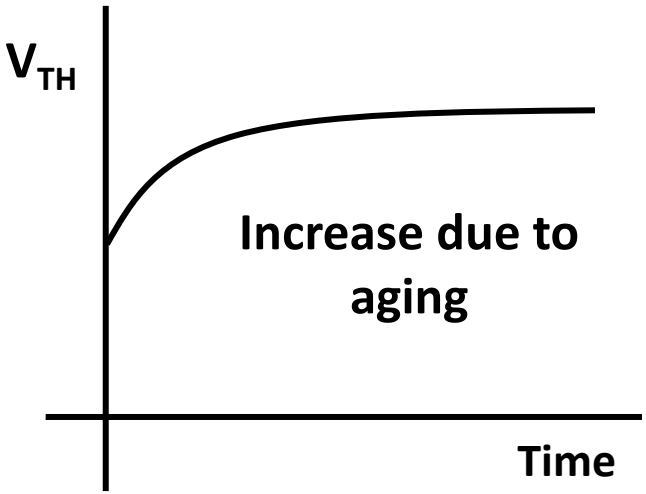
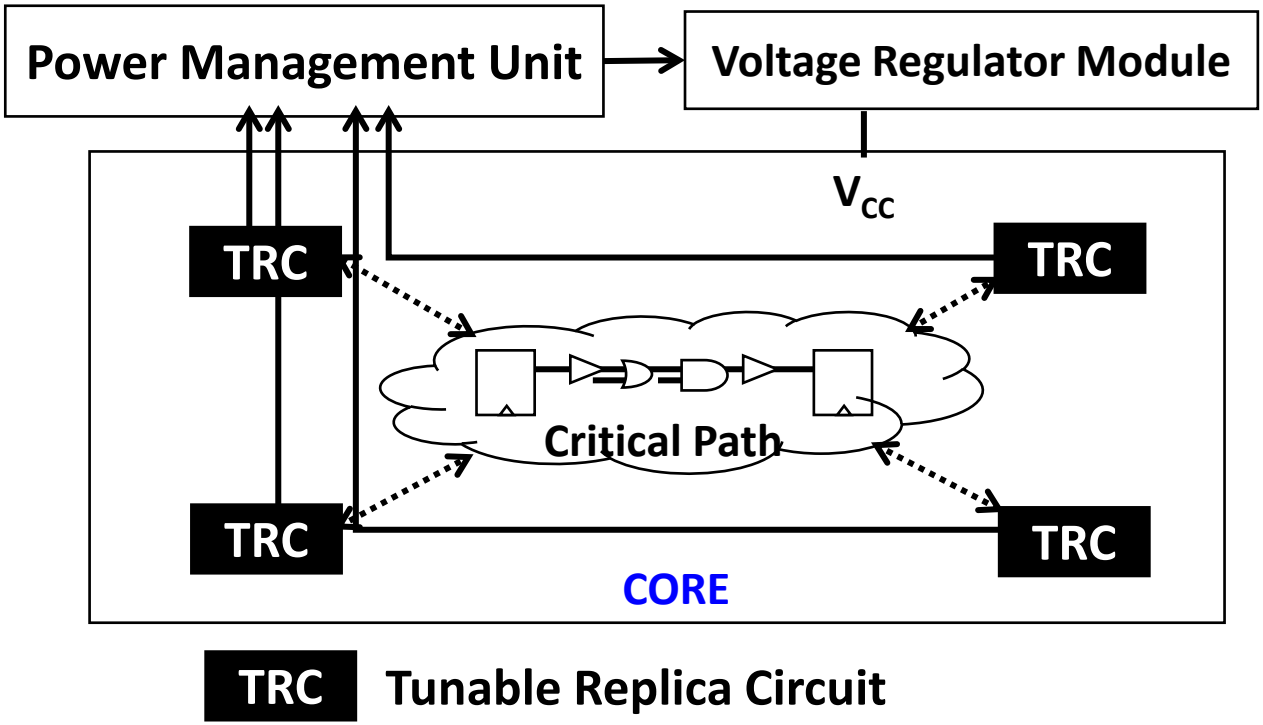
# Aging Mechanisms

- **Bias Temperature Instability (BTI)**
  - Primary aging cause
  - Device is biased in inversion mode
- **Hot Carrier Injection (HCI)**
  - Electron(Hole) gains sufficient kinetic energy → overcome potential barrier to break in interface
  - The switching characteristic of the transistor can be permanently changed
- **Time-dependent Dielectric Breakdown (TDDB)**
  - Oxide breakdown due to long-application of low electric field
- **All device aging mechanisms collectively contribute to performance degradation of digital circuits by effectively raising $V_{TH}$**



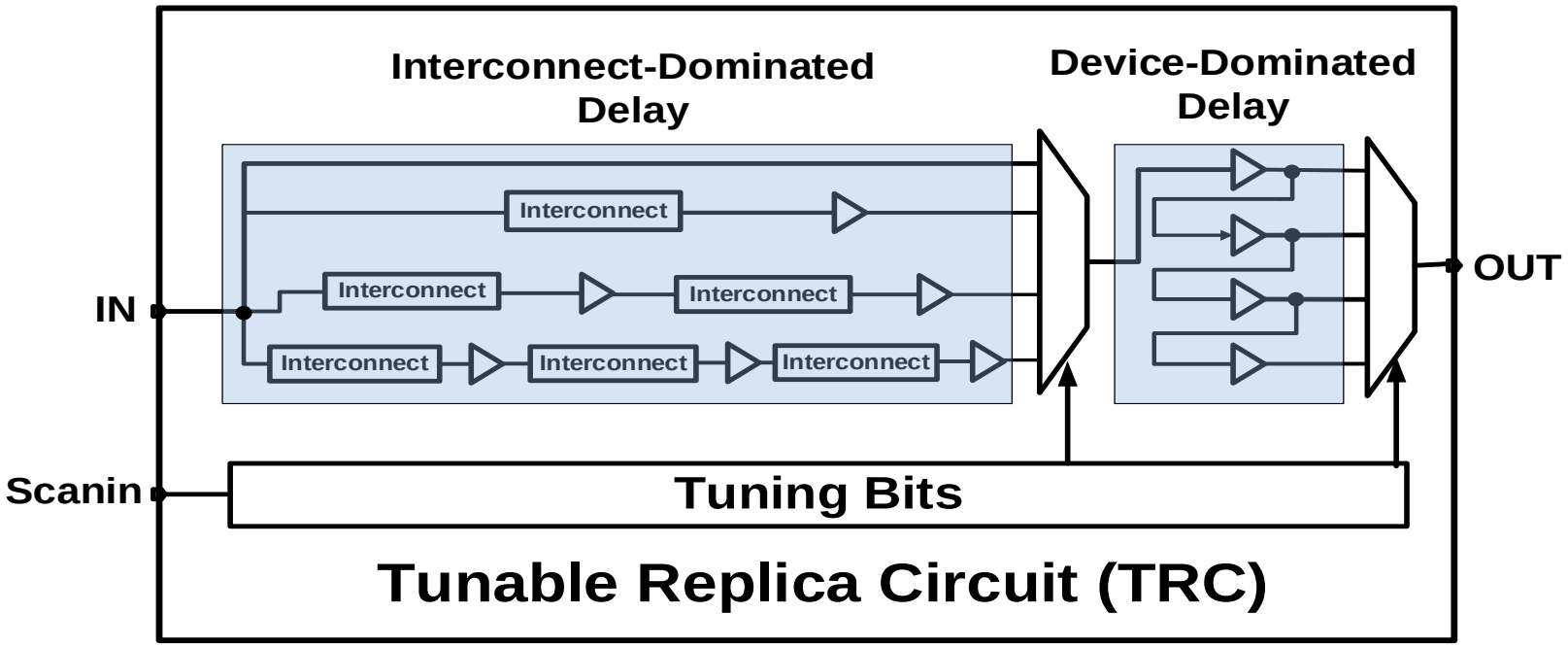



# Aging-aware Adaptive Voltage Scaling Usage Model




- TRC is calibrated to match critical path delay in the core through post-silicon tuning
- At runtime, TRCs monitor the operating conditions and performance of the core considering temperature and voltage stress condition

# Tunable Replica Circuit (TRC) Aging Monitor




- Tunable replica circuit mimics critical path in a core
- TRC consists of interconnect-dominated delay and device-dominated delay segments
- Post-silicon calibration of TRC is performed to track the critical path delay under aging from BOL to EOL

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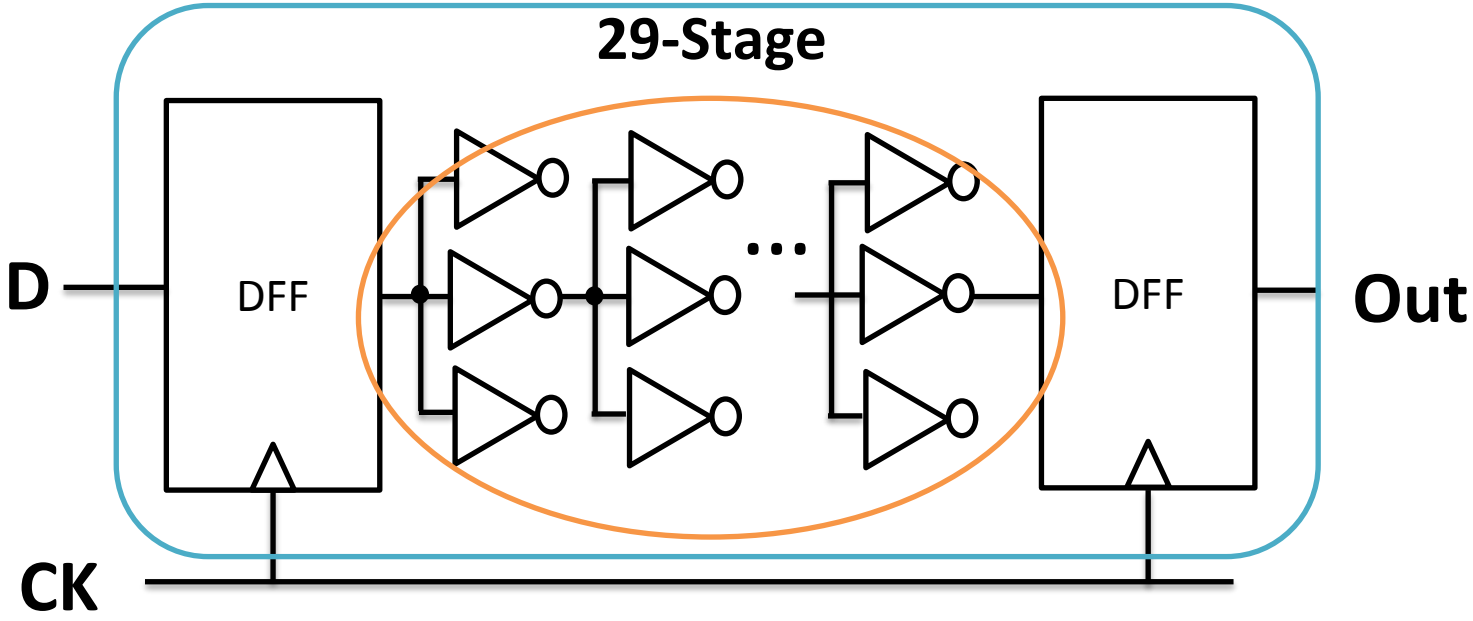
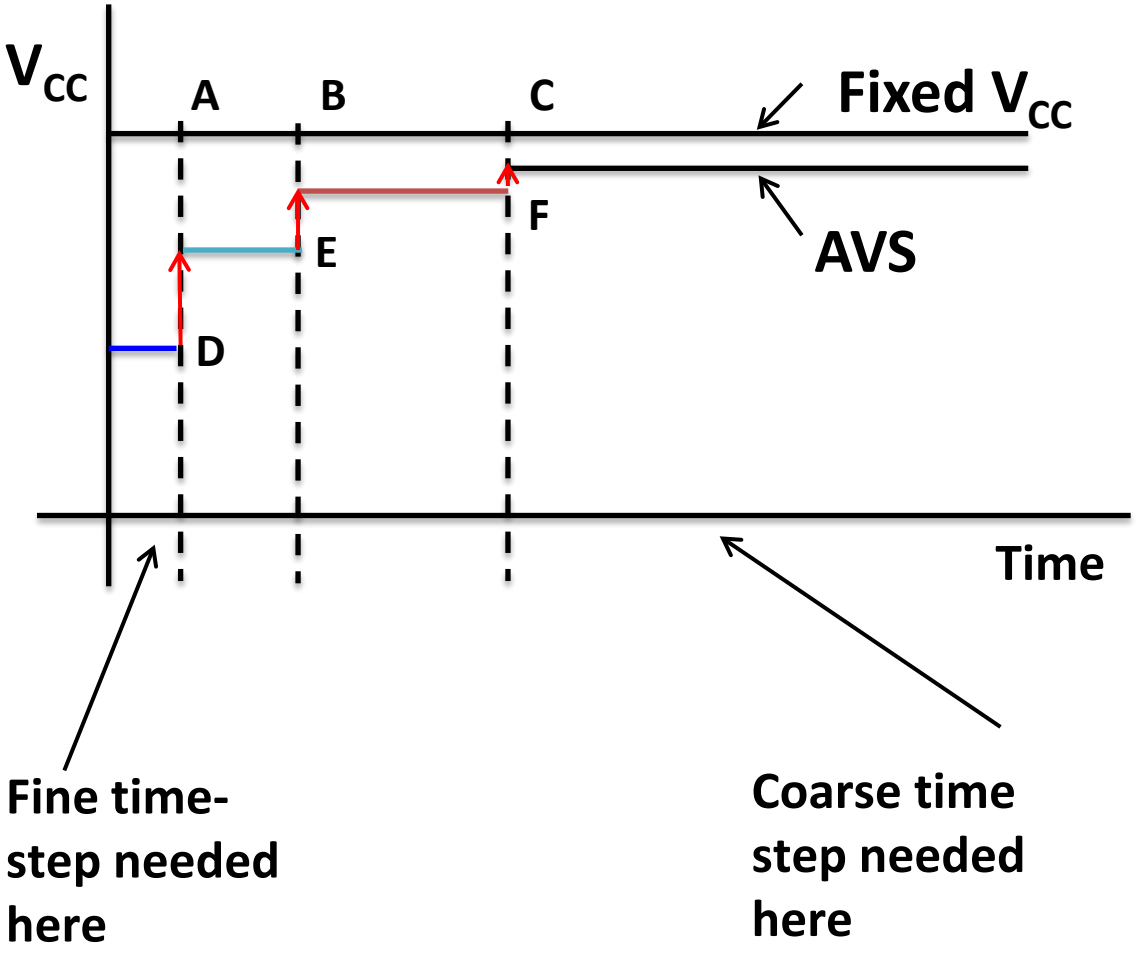
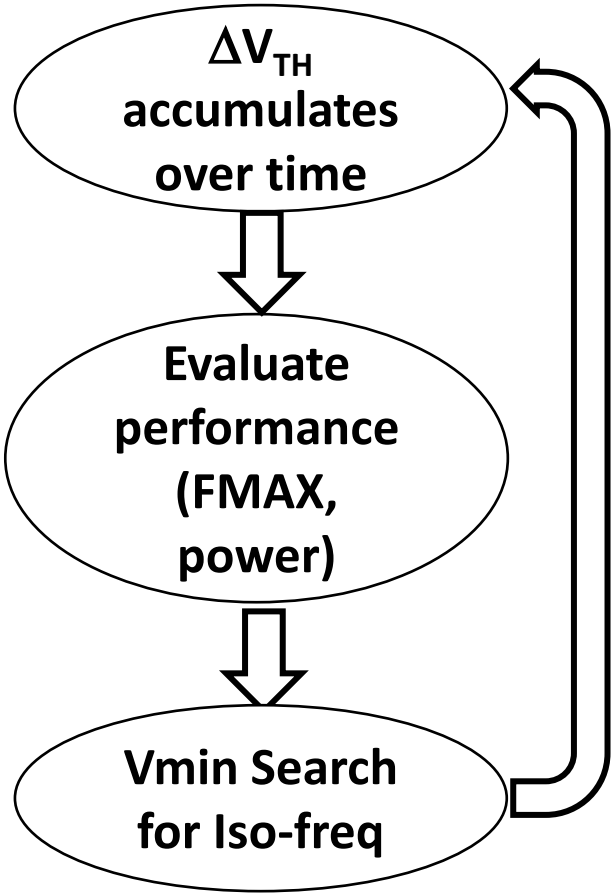
# Simulation for Adaptive Voltage Scaling




- Benchmark circuit: 29-Stage FO3 Inverter Chain + driving/receiving FFs
- Stress: Clock(toggling), Data(No toggling)
- In simulation, we consider both NBTI and PBTI stress

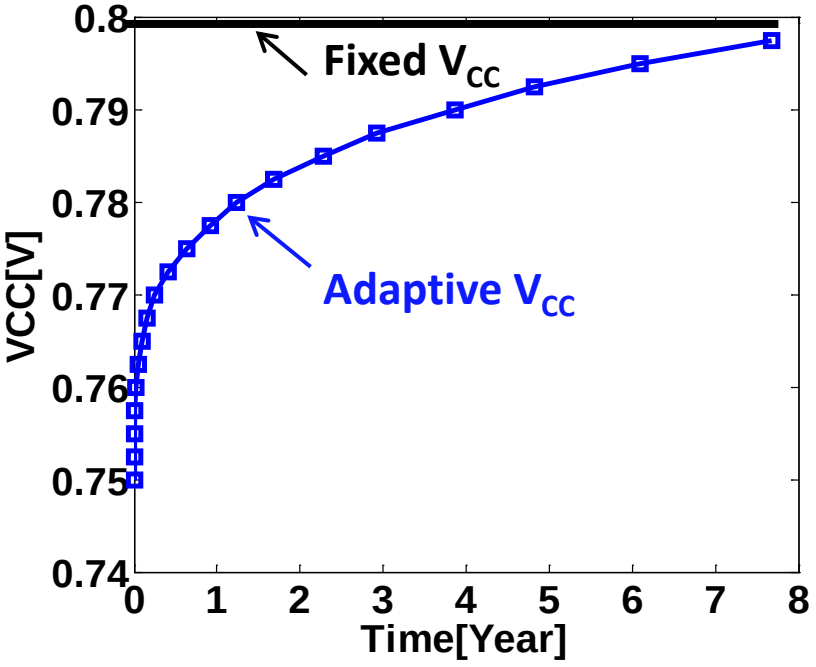
# Aging Simulation Flow

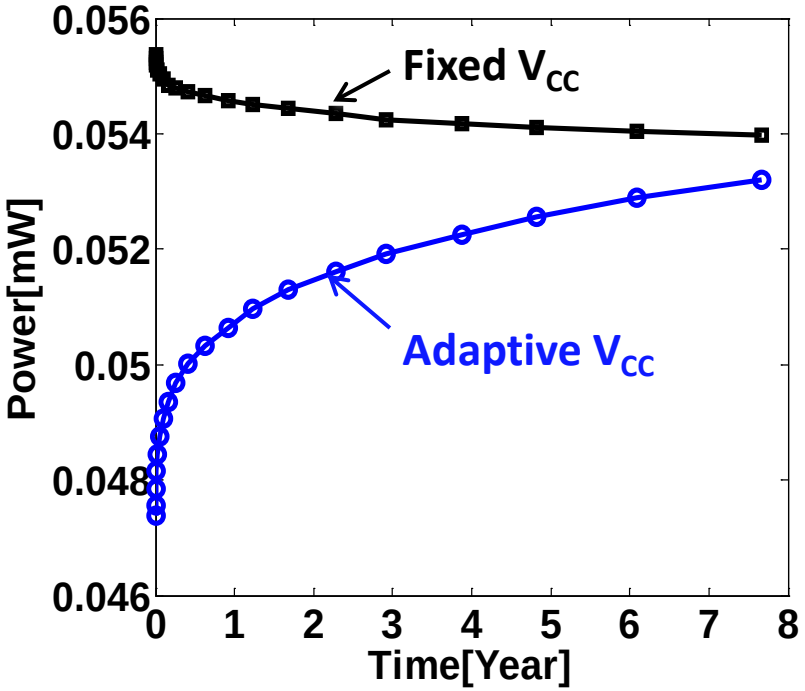



- Variable step-size is used for fast aging simulation

# Simulation for Adaptive Voltage Scaling




- <u>Fixed Vcc:</u> $V_{TH}$ increases with aging → leakage power reduces overtime → total power reduces
- <u>AVS:</u> stress is less @ BOL → aging is less → average $V_{CC}$ is less → power is lower throughout lifetime

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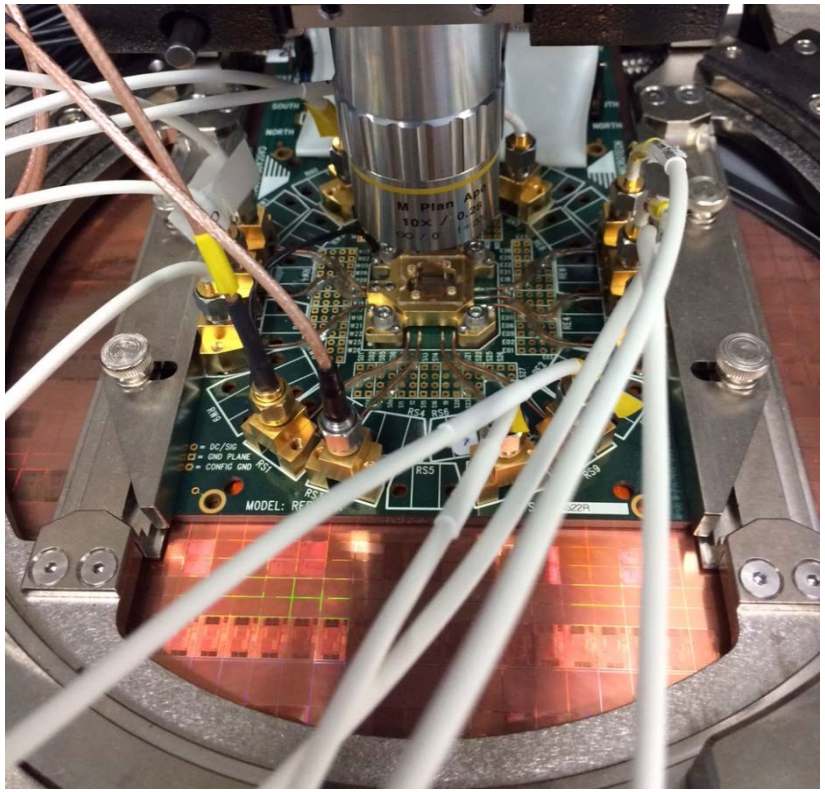
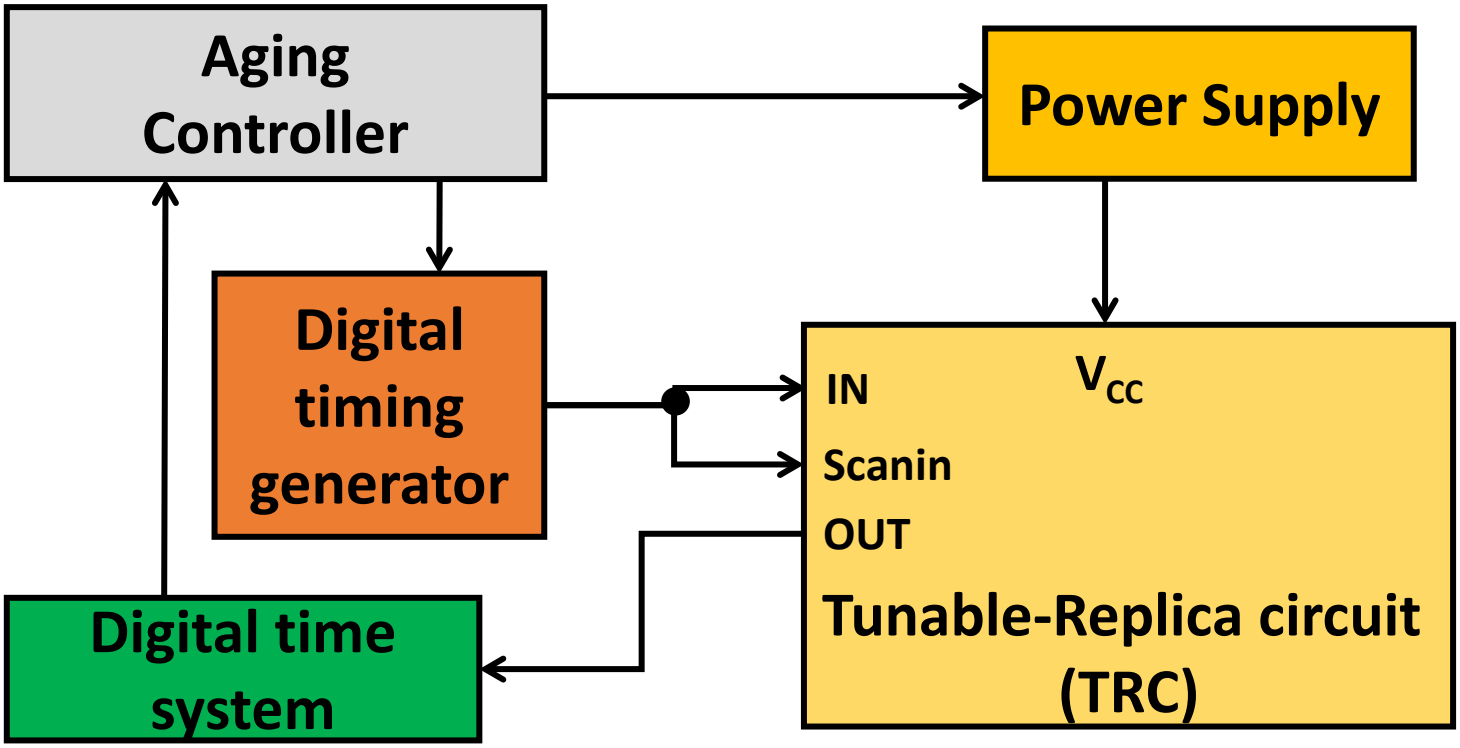
# Aging-Aware AVS Test Chip



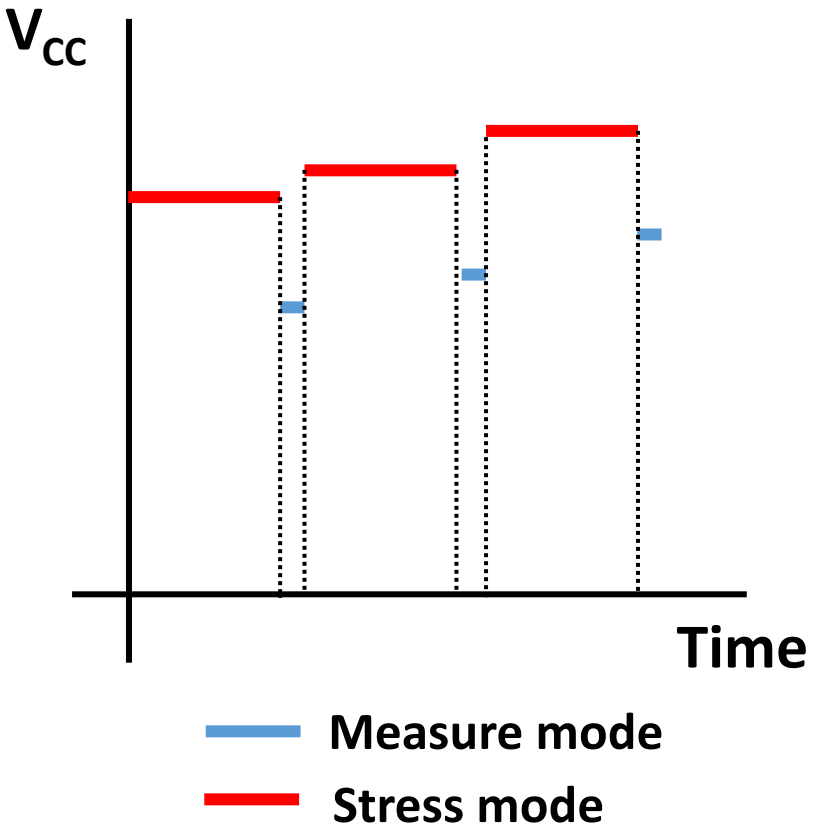

| | |
|---|---|
| Technology | 22nm tri-gate CMOS |
| Test interface | Membrane probe |
| Nominal $V_{CC}$ | 0.87V |
| Target frequency (delay) | 500 Mhz (2ns) |
| Supply voltage resolution | 5mV |

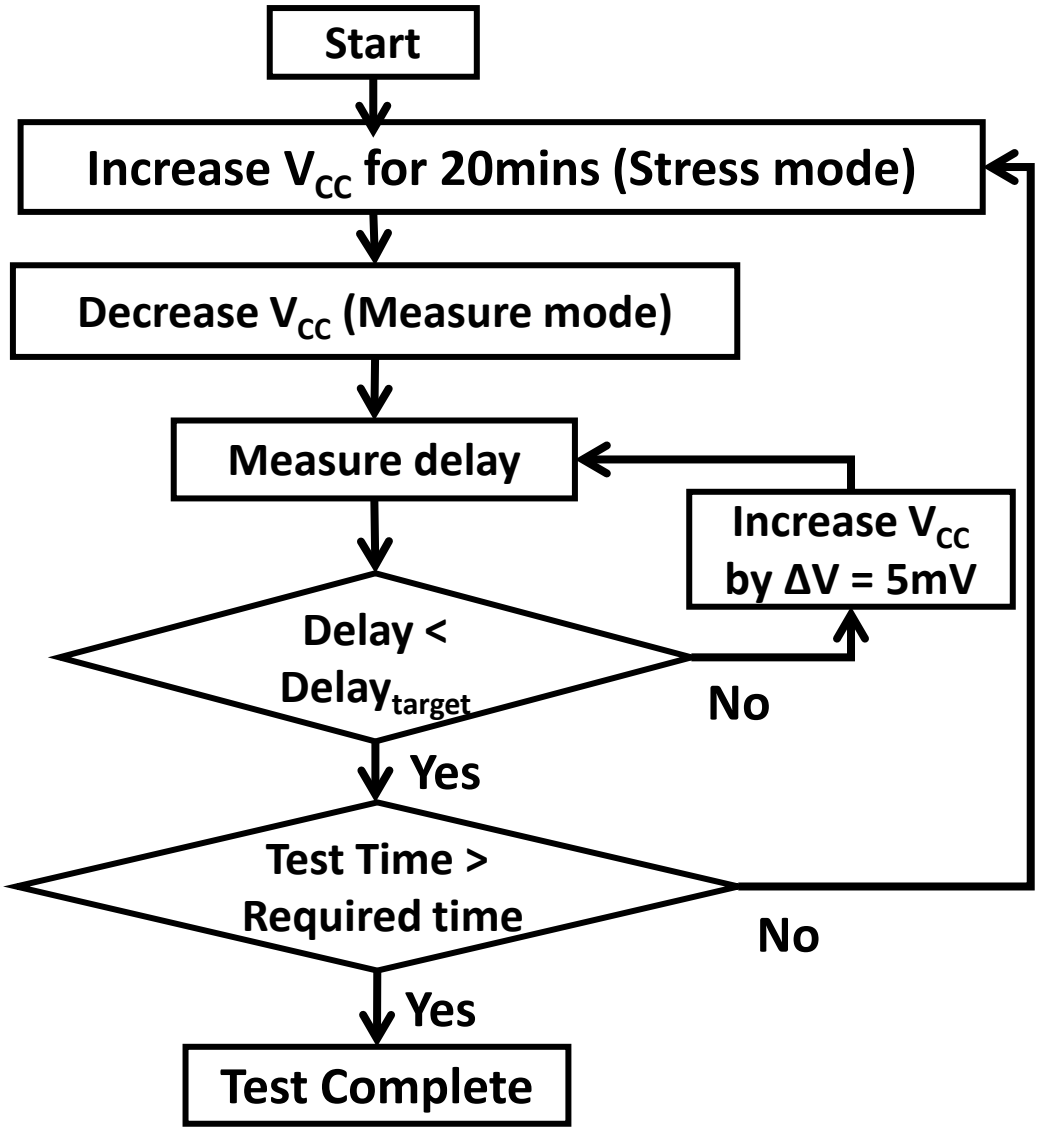
# Test Setup




- Digital timing generator: Control Clock, Scan chain
- Digital time system: Measure TRC delay with 1ps accuracy
- All equipment is controlled by GPIB, aging control is performed by external PC

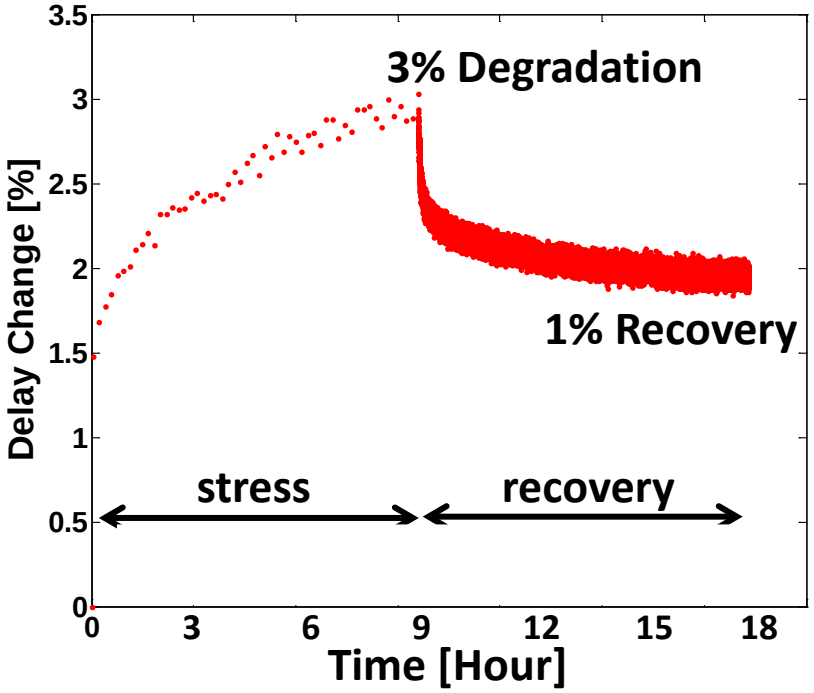
# Flow for Assessing Aging Impact with AVS

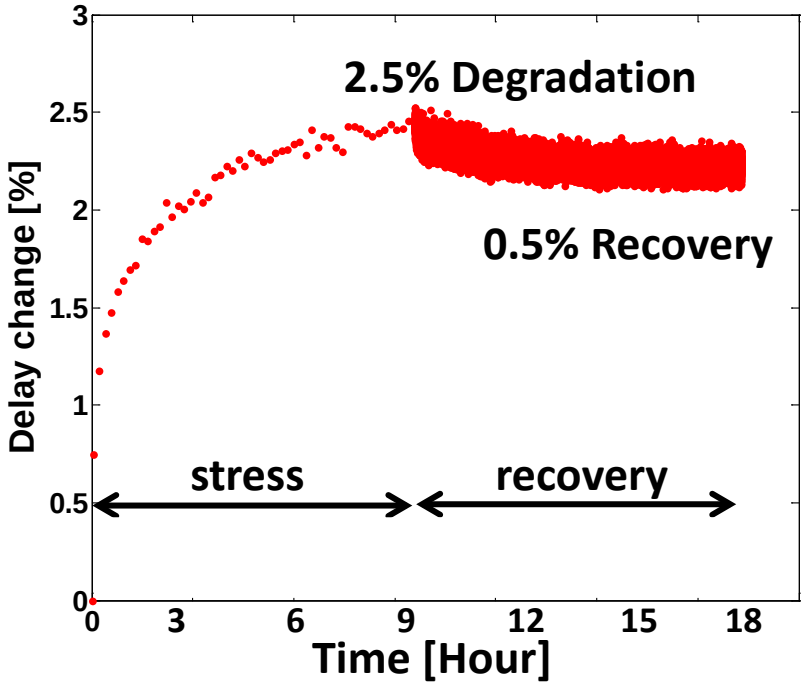


# Measured DC Versus AC Stress

**9 Hrs Stress → 9 Hrs Recovery**

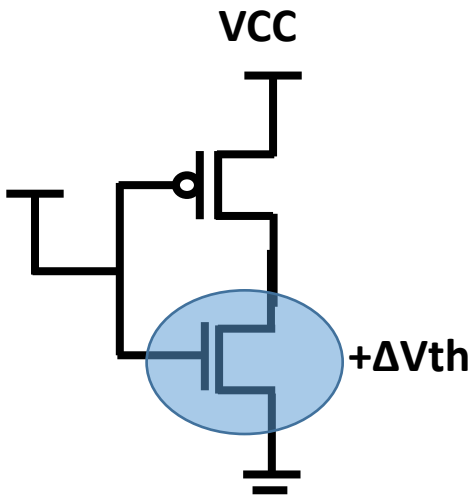


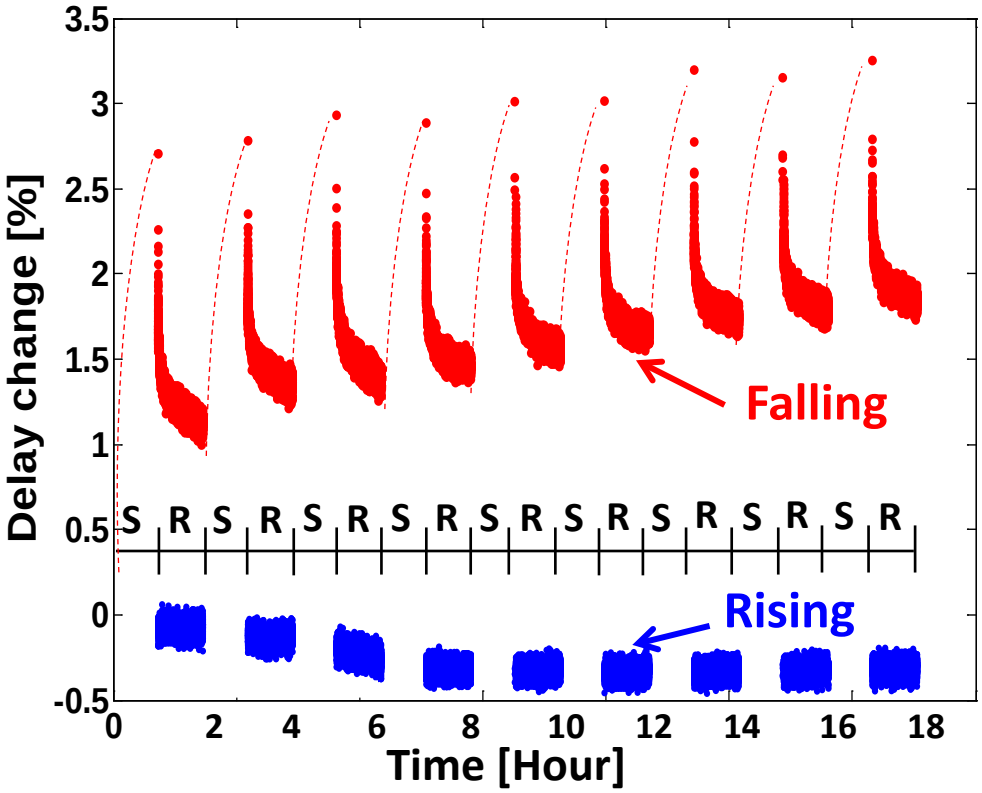

**DC stress (TRC input fixed)** **AC stress (TRC input @ 100MHz)**

- **DC stress is worse since devices are stressed 50% of the time during the AC stress case.**
- **After the stress is completely removed, some short-term delay degradation is recovered.**

# Measured Rising Versus Falling Delay



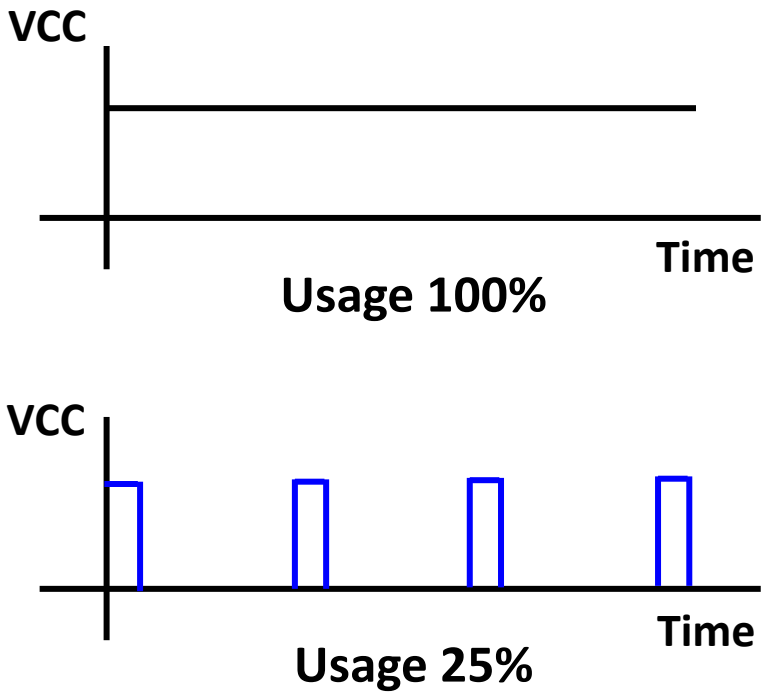

Falling → Slower
Rising → Faster

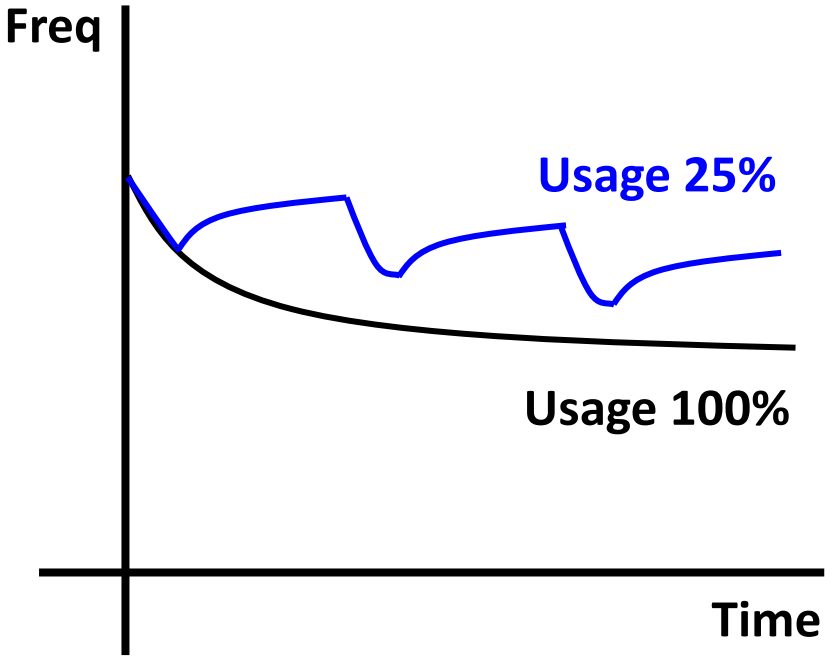



*S: Stress *R: Recovery

- Stress and recovery continues alternatively.
- While rising transition degrades, falling Transition improves.

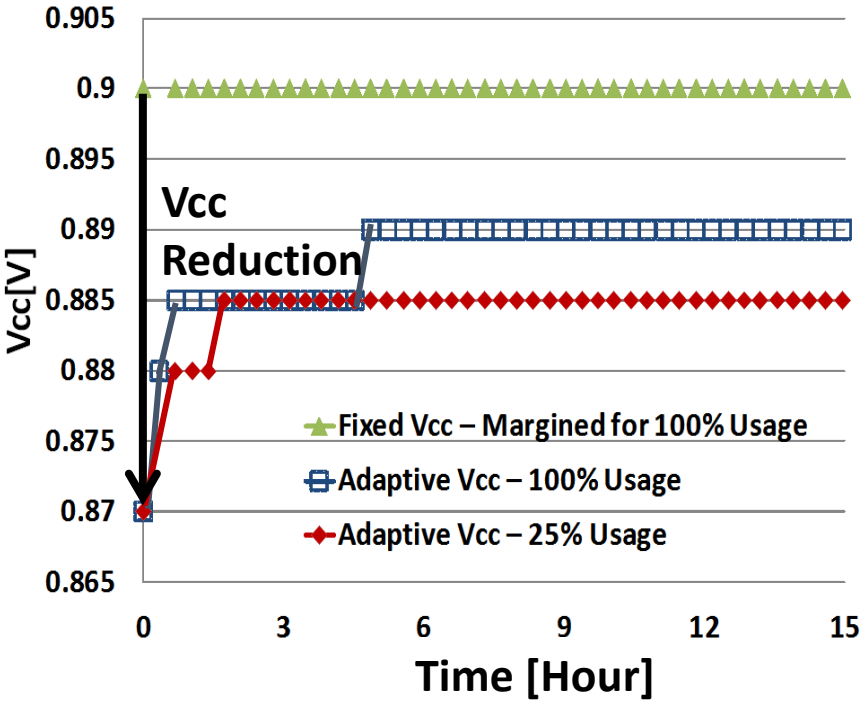
# Recovery and Usage

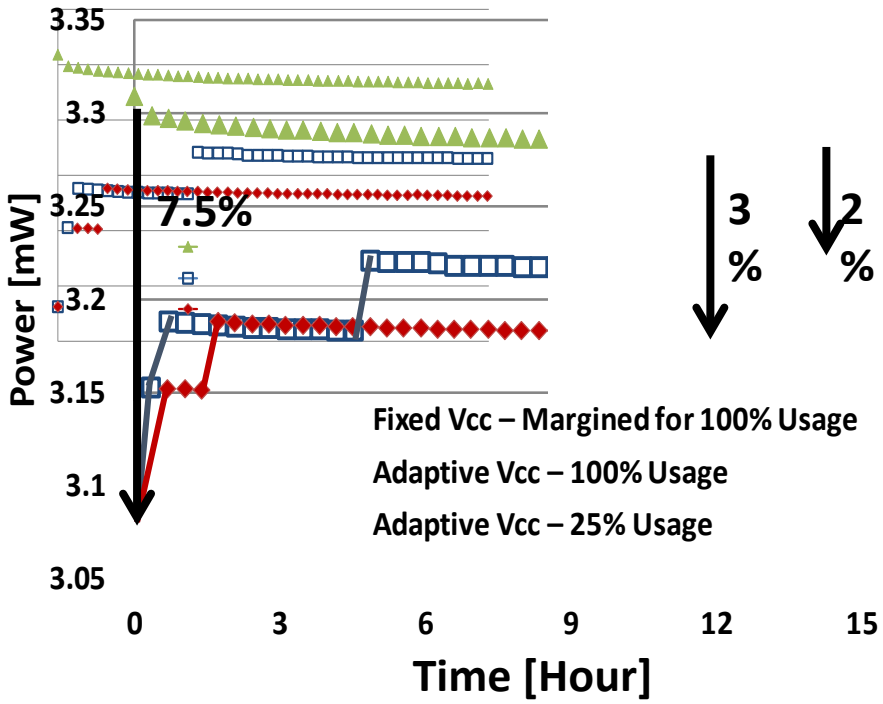



- Different usage (activity condition) causes different amount of frequency degradation
- Devices start to recover the frequency degradation with the removal of stress

# Measurement of Adaptive Voltage Scaling




- For 25% usage, the TRC is DC stressed for 25% of total test time and the stress is removed for 75% of time
- Aging-aware AVS scheme can achieve ~7.5% power reduction by eliminating aging guard band at BOL

# Conclusion

- **Aging-aware AVS using a Tunable-Replica Circuit (TRC) monitor is verified through simulation and measurement data**
- **Test-chip measurements in a 22nm high-k/metal-gate tri-gate CMOS process demonstrates up to 7.5% power reduction at BOL (3% at EOL) by an aging-aware AVS scheme**
- **Measurement results show that $V_{CC}$ adaptation is significant in early life and strongly dependent on usage**

# Any Question?