25-1:

A 20 Gb/s 0.3 pJ/b Single-Ended Die-to-Die Transceiver in 28 nm-SOI CMOS

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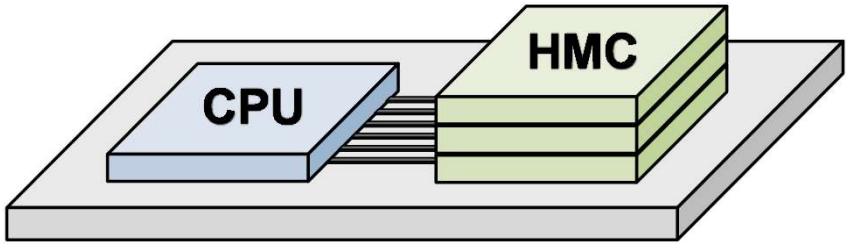
Outline

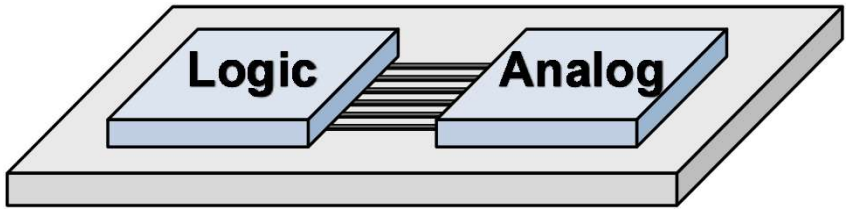
- Die-to-Die Links
- Proposed Link Architecture
- Transceiver Circuit Design
- Proposed Packaging Solution
- Measurement Results
- Conclusion

Die-to-Die Link Applications

- Two chips in different technologies that cannot be integrated onto a single chip.
- Interface between a large logic chip and an analog chip.



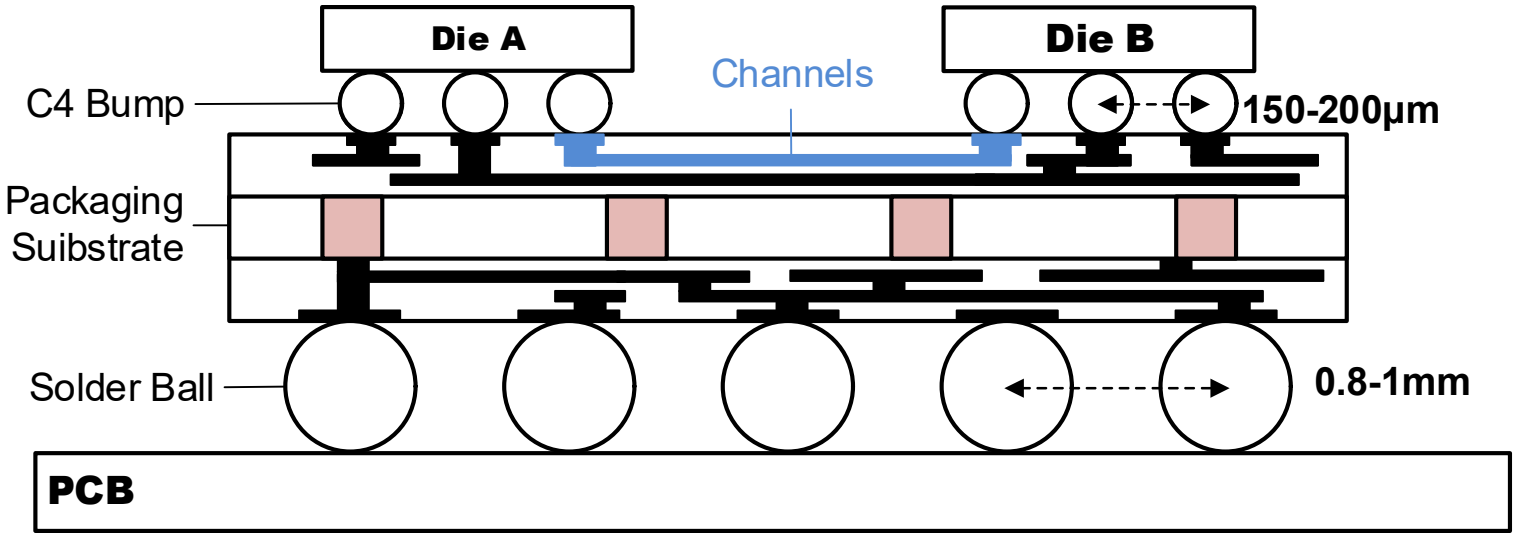
(a) CPU to Hybrid memory cube (HMC)



(b) Logic/FPGA to analog/Serdes

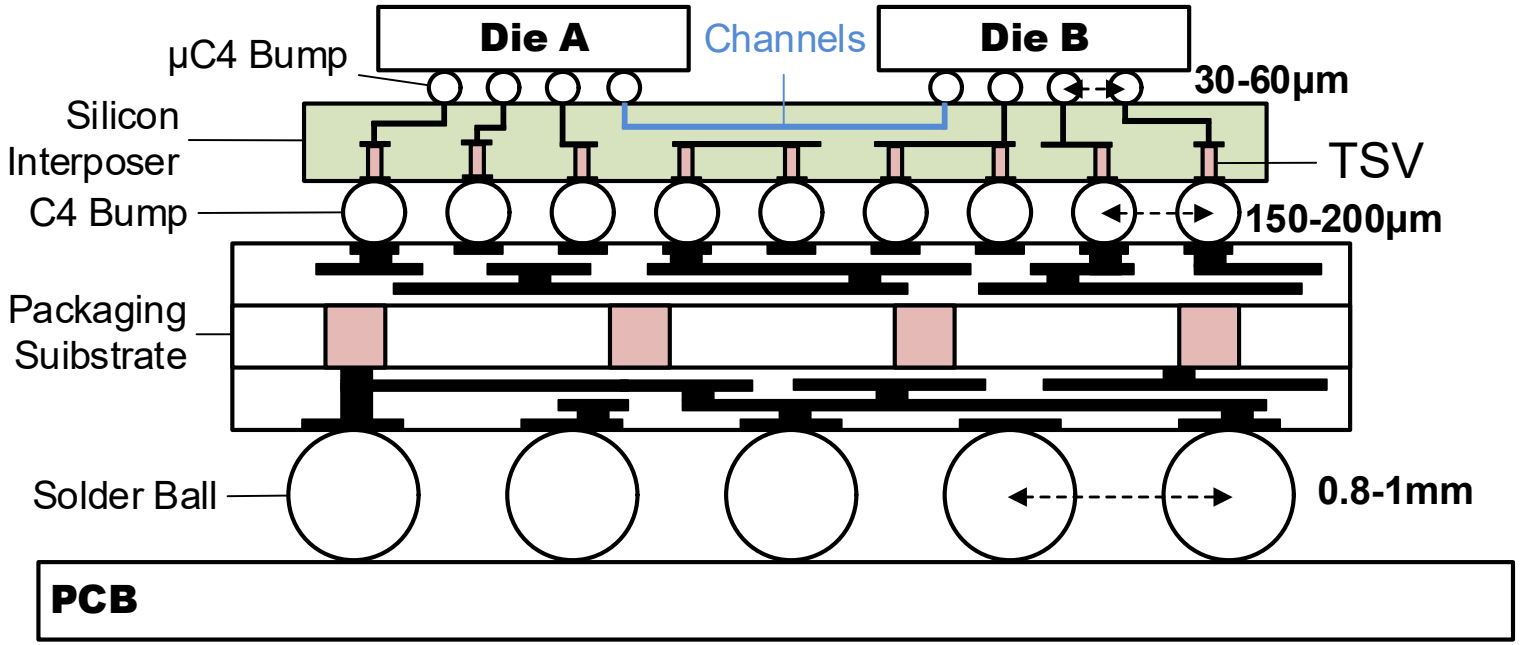
Die-to-Die Links on Organic Substrates

- Lower attenuation and Crosstalk and higher density in comparison with typical PCB channels.
- Example: 20Gb/s Links consuming 0.25pJ/bit over a 6mm interconnect with 67µm pitch, 1dB loss and 29dB NEXT. [JSSC13-Poulton]



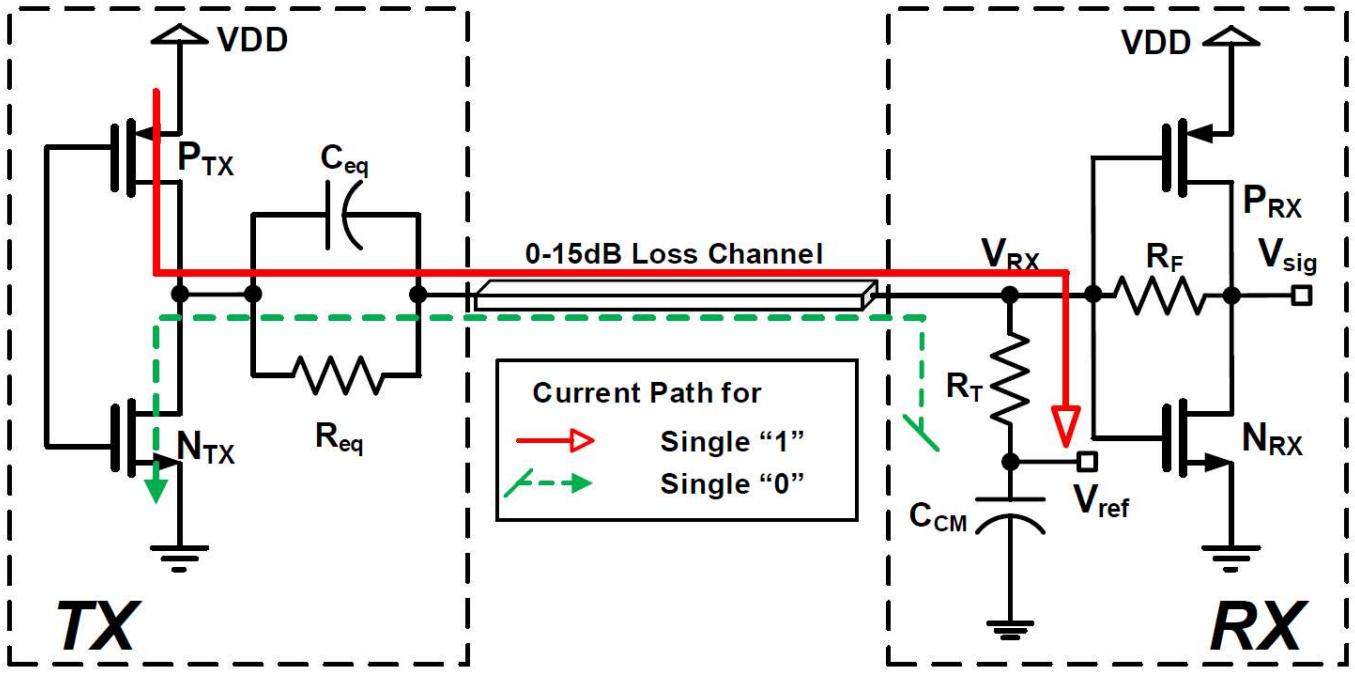
Die-to-Die Links on Silicon Interposers

- Higher bump/interconnect density but more RC losses in comparison with organic substrates.
- Example: 10Gb/s Links consuming 2.6pJ/bit over 0.5-4cm interconnects with 8-22µm pitch, 5-15dB loss and 35dB NEXT. [JSSC12-Dickson]



Single-Ended Link Architecture

- Good termination on receiver side (with large C_{CM}).
- Lack of proper termination in transmitter does not cause significant reflections because there are no major discontinuities along the channel.

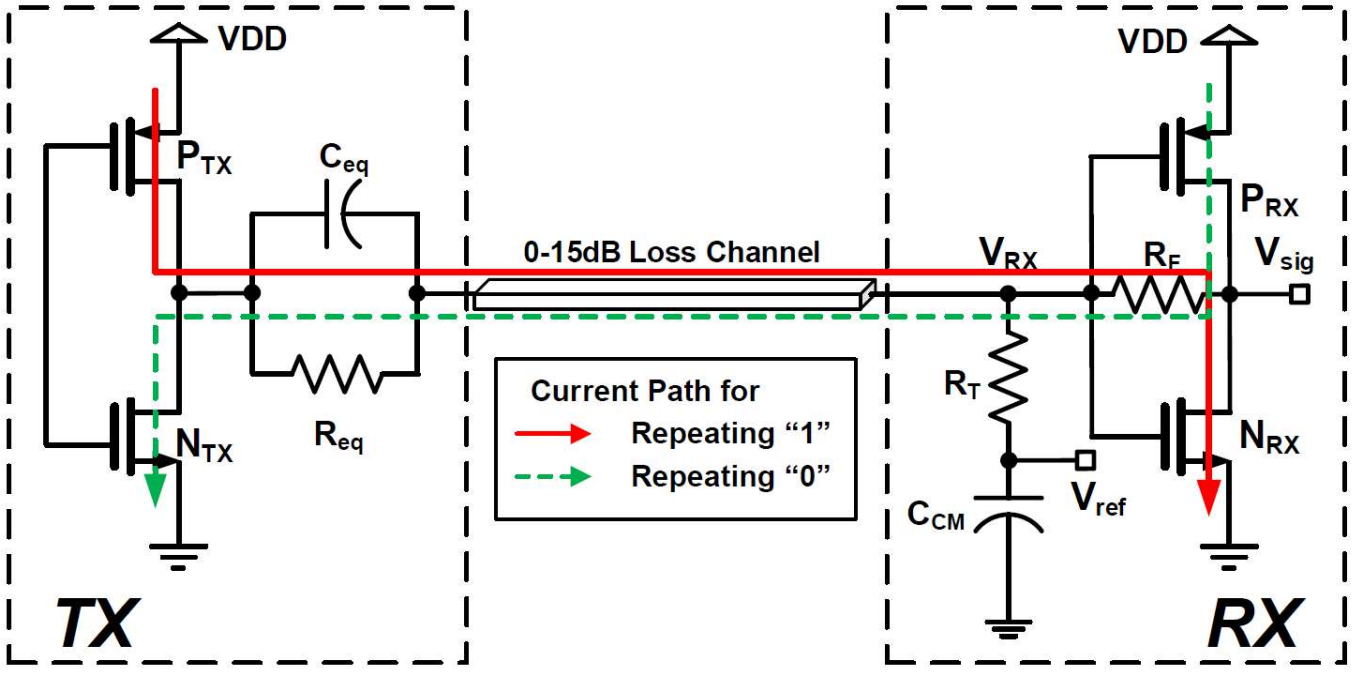


Reference Signal Extraction

- The reference voltage is extracted from the incoming signal and stored in C_{CM} capacitor.

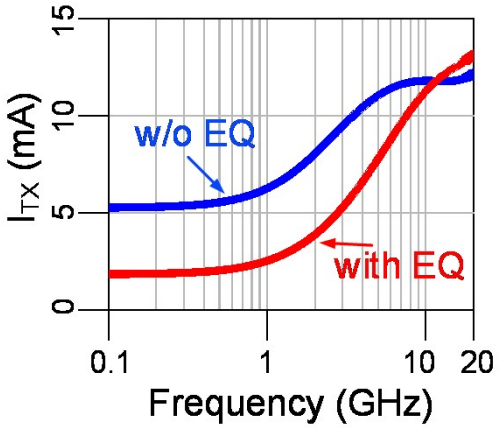
$$V_{RX1} = \frac{R_{NRX} + R_F}{R_{NRX} + R_F + R_{ch} + R_{eq} + R_{PTX}} \times V_{DD} \quad (1)$$

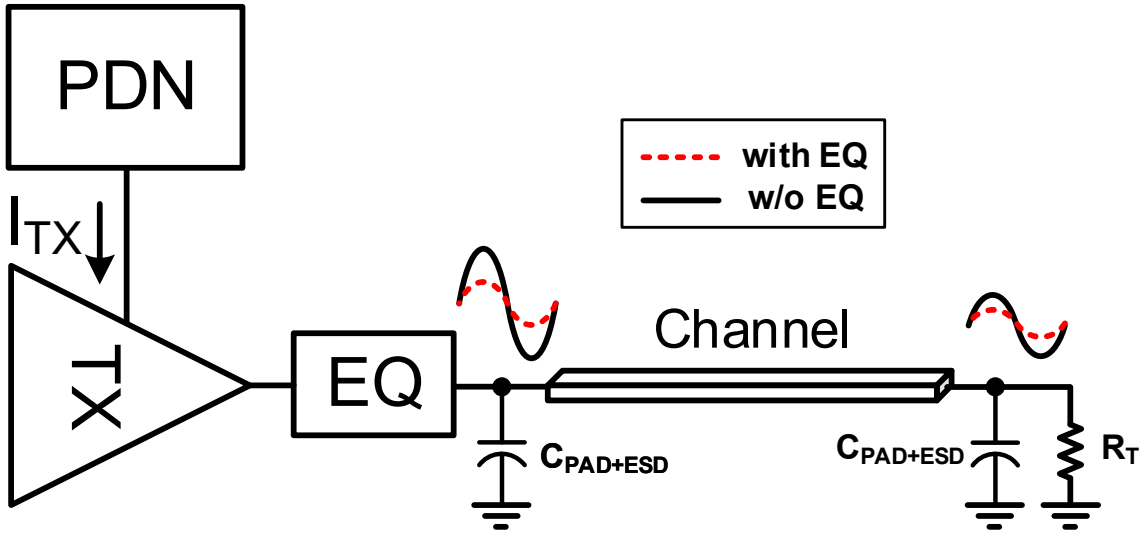
$$V_{RX} = \frac{R_{ch} + R_{eq} + R_{NTX}}{R_{NTX} + R_F + R_{ch} + R_{eq} + R_{PRX}} \times V_{DD} \quad (2)$$



Passive EQ and Power Saving

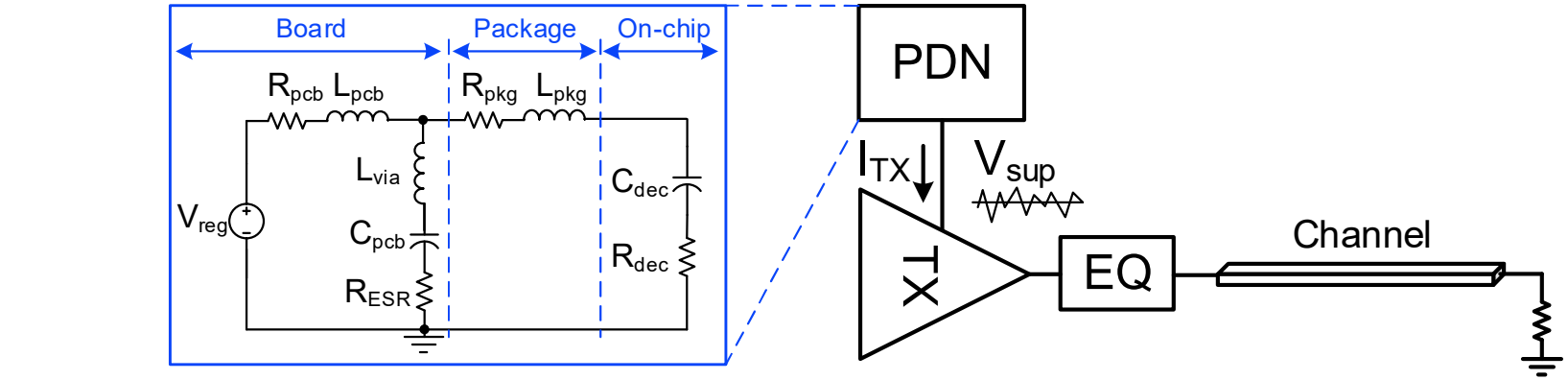
- Having the passive EQ in transmitter results in significant power saving:
  - Dynamic power reduction by decreasing the signal swings.
  - Static current reduction by increasing the resistance in the current path.

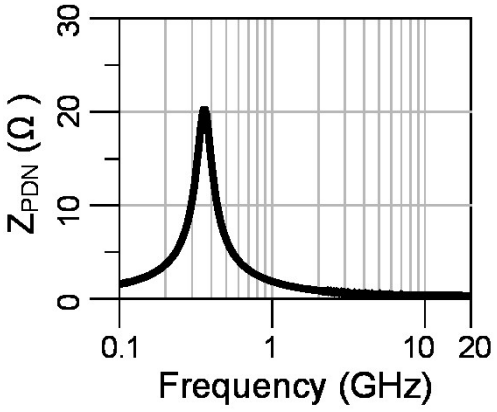


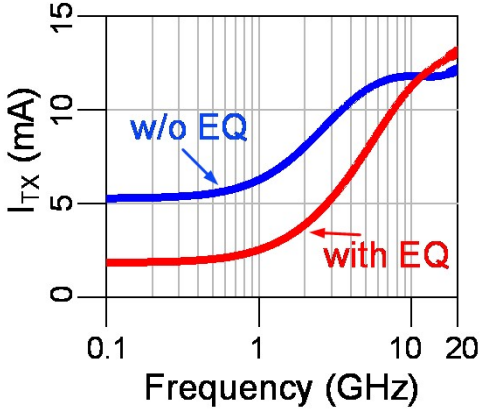


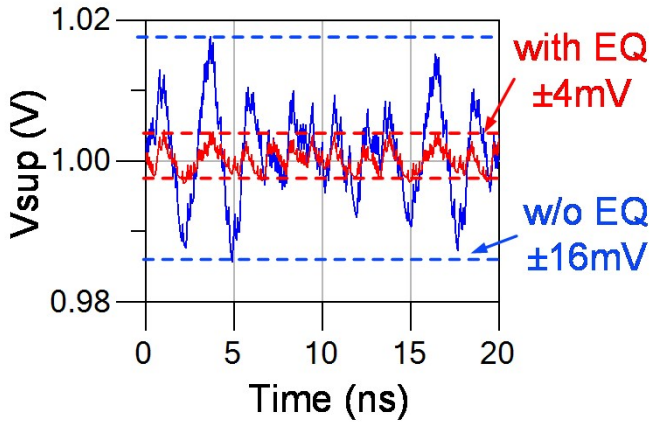
Passive EQ and Power Integrity

- Passive EQ shapes the transmitter current spectrum to higher frequencies that leads to lower supply ripples.



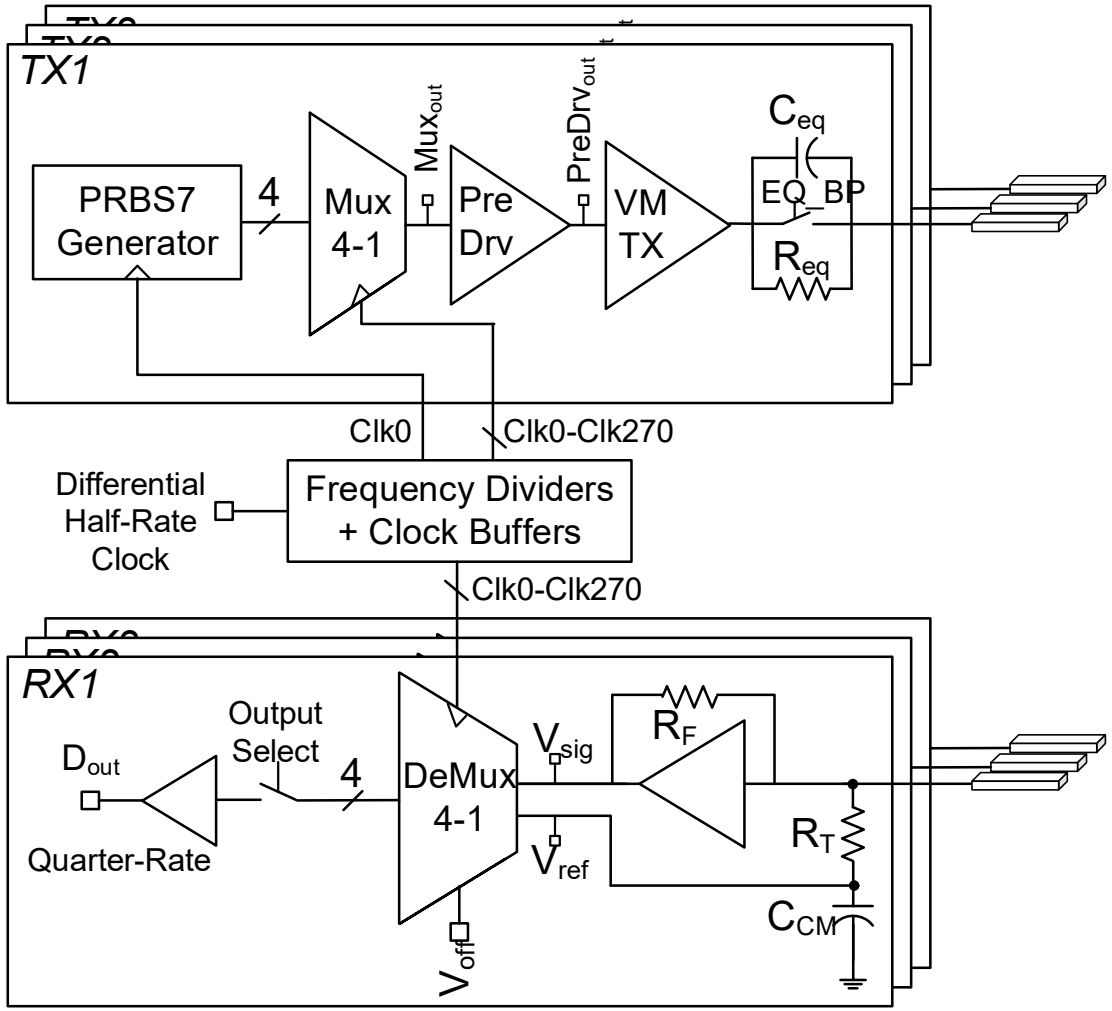






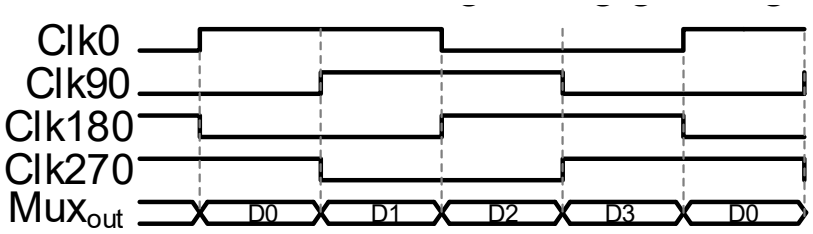
Transceiver Prototype Block Diagram

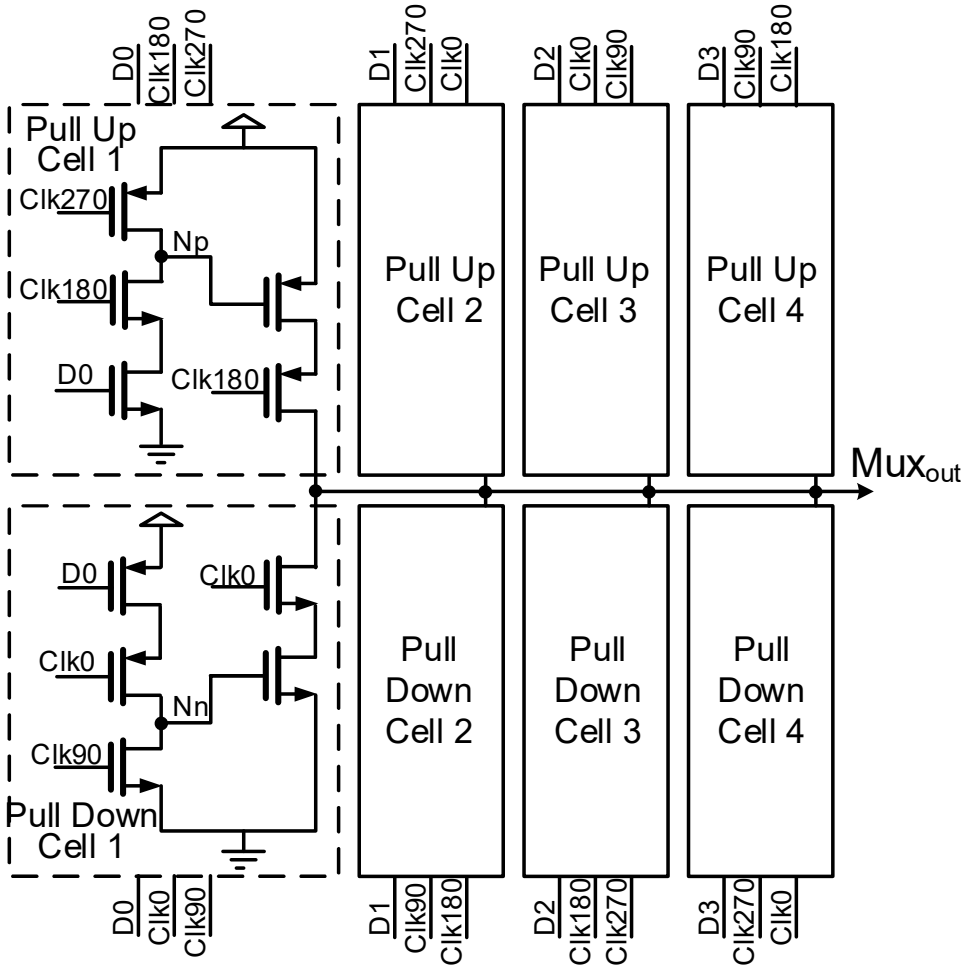
- On-chip PRBS generators and frequency dividers to provide quarter-rate data to the transmitter.
- CMOS Logic circuits to minimize power.
- 3 transceivers to capture the effect of crosstalk on link performance.



4-to-1 CMOS Multiplexer

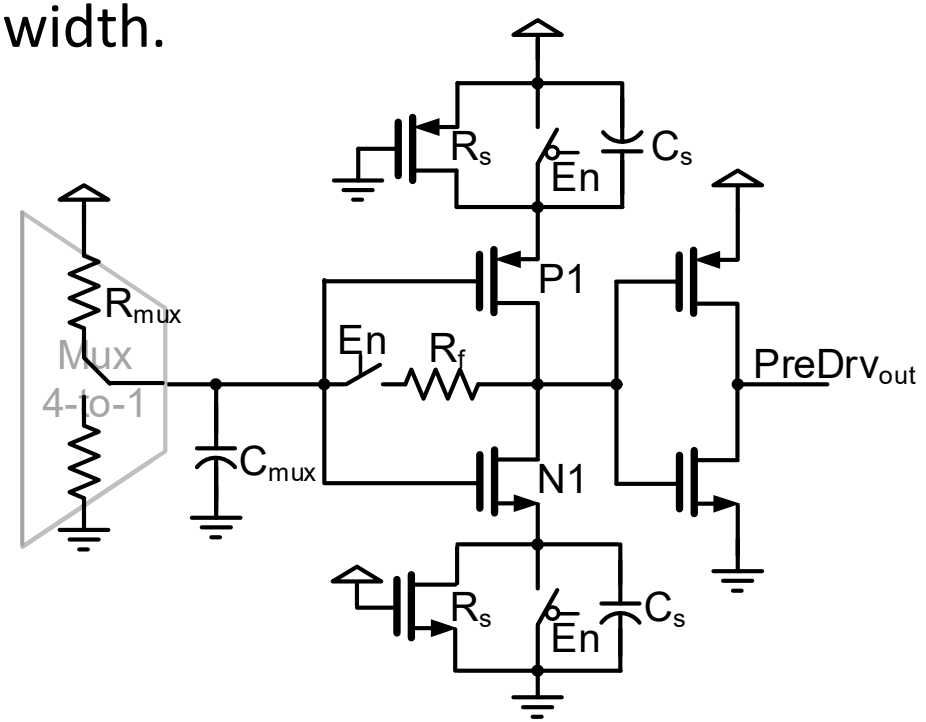
- Modified version of the CML multiplexer presented in [ISSCC13-Hafez].
- No static power consumption.
- More parasitic capacitance on the output node.



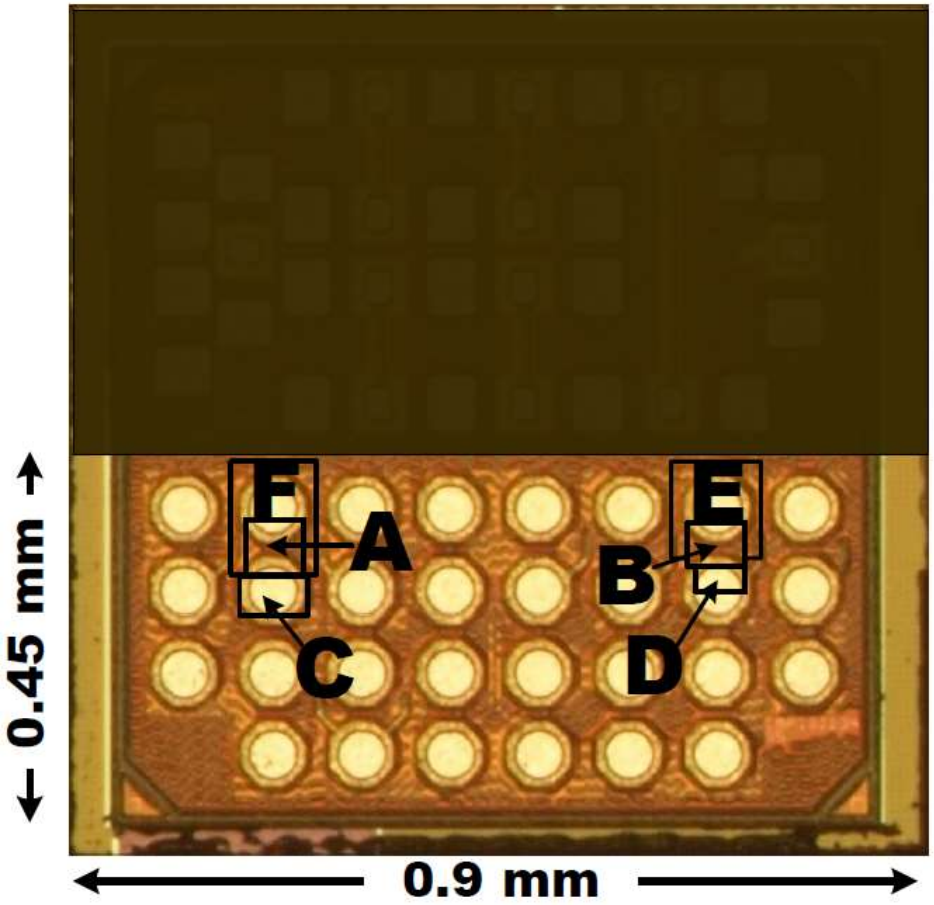


Pre-driver with Bandwidth Enhancement Technique

- CML multiplexers use inductive peaking as a bandwidth enhancement technique. What about CMOS circuits?
- A resistive feedback along with capacitive source degeneration are used to increase the bandwidth.
- Smaller signal swings at the output of multiplexer and inverter makes them more sensitive to supply noise. Therefore, this method is only useful for 0-5dB boost.



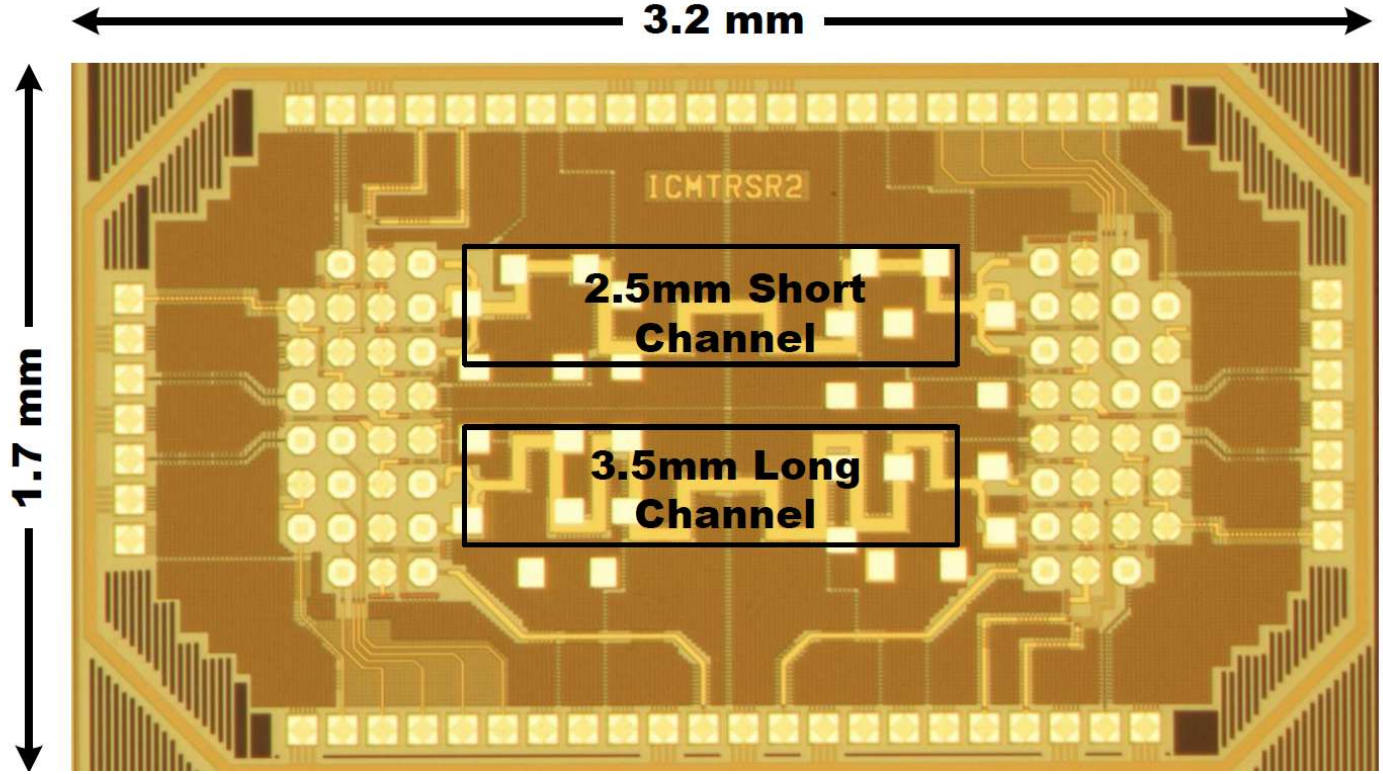
Transceiver Die Photo



Block Description		Area (µm²)
A	Transmitter	4556
B	Receiver	4374
C	PRBS Gen. & TX Clocking	3442
D	RX Clocking	1700
E	TX Decoupling Cap.	8019
F	RX Decoupling Cap.	7290

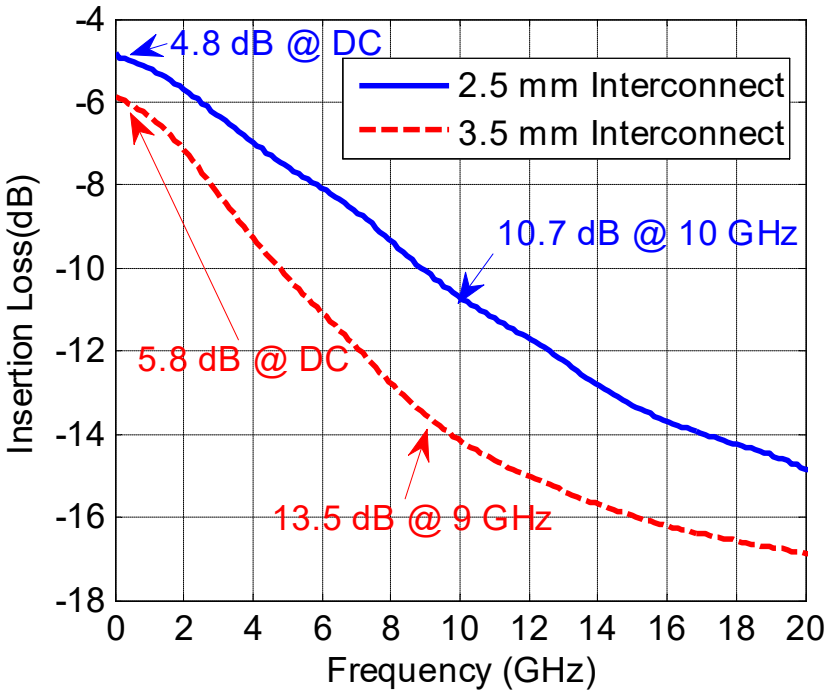
0.35µm Silicon Interposer Die Photo

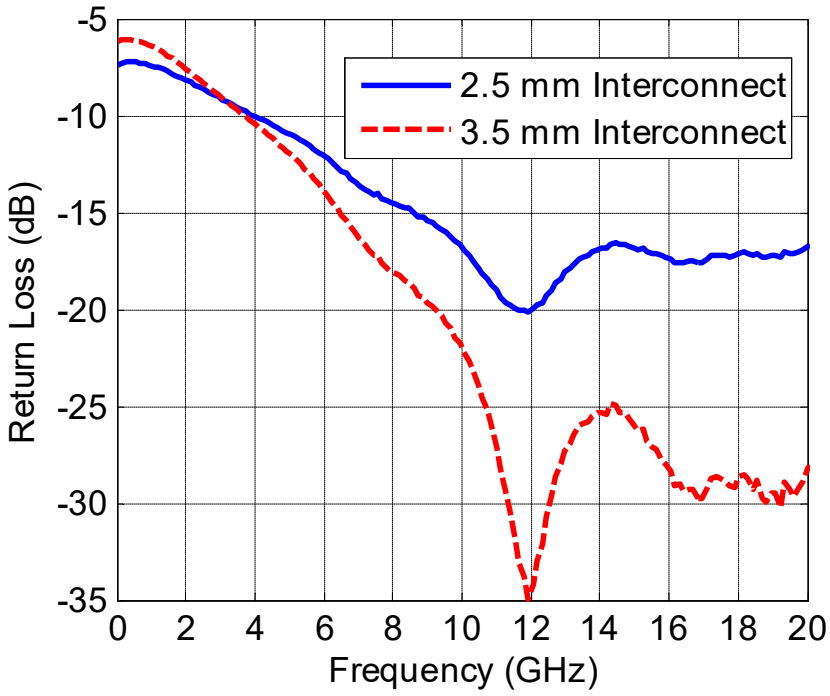
- The interconnects on the interposer are tapered striplines.
- The spacing between the channels is 6µm to have Xtalk<-40dB.
- The channel pitch is 10µm.



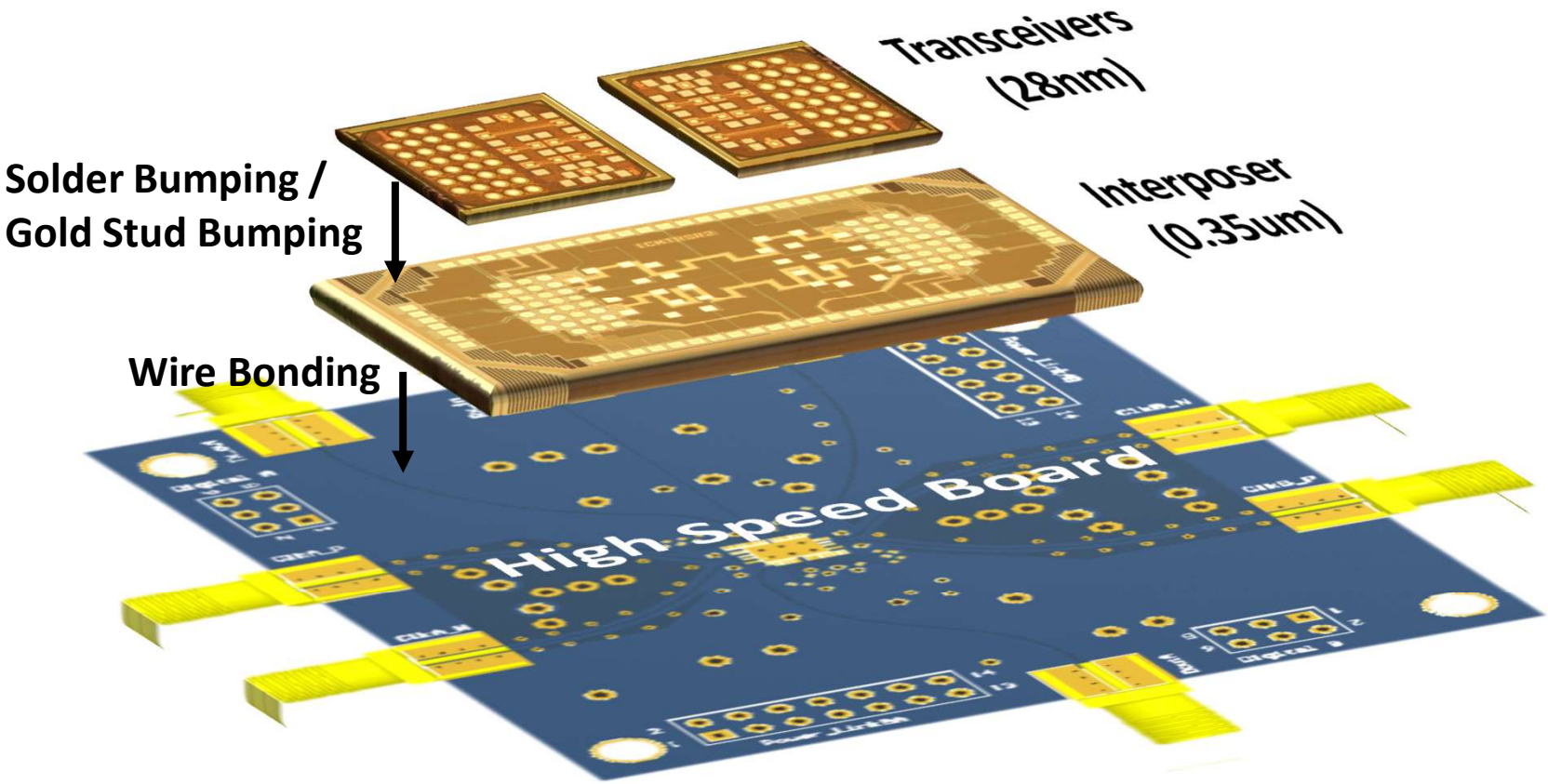
Silicon Interposer Channels

- The interconnects are made of Aluminum with only 0.64µm thickness which introduces 1.5-2dB/mm of DC loss and poor matching at low frequencies.

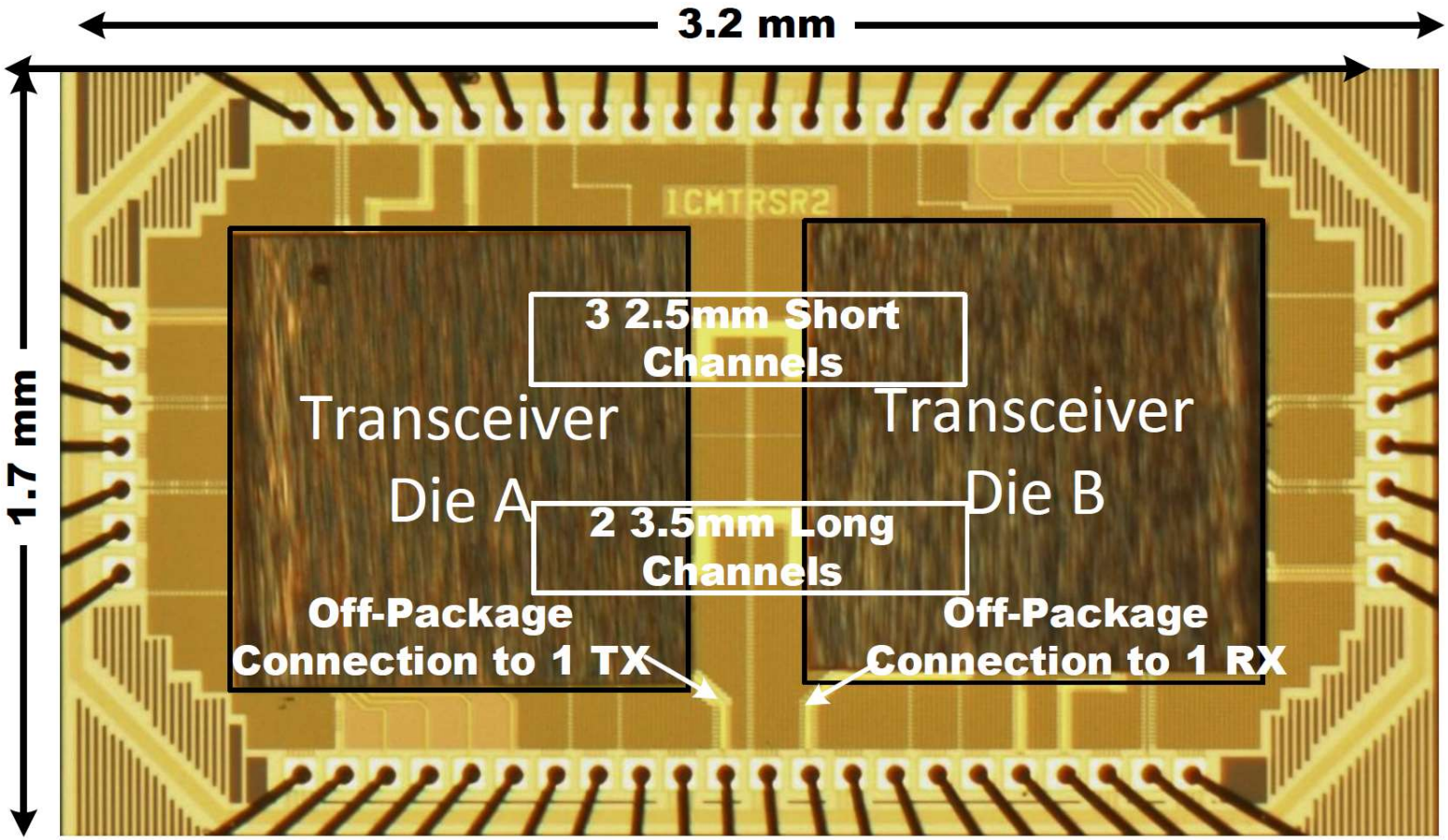




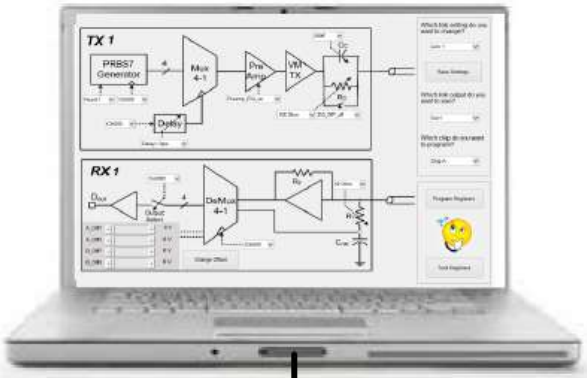
Proposed Packaging Solution



Packaged Die-to-Die Link Prototype



Test Setup



Keysight 4960A Clock Synthesizer

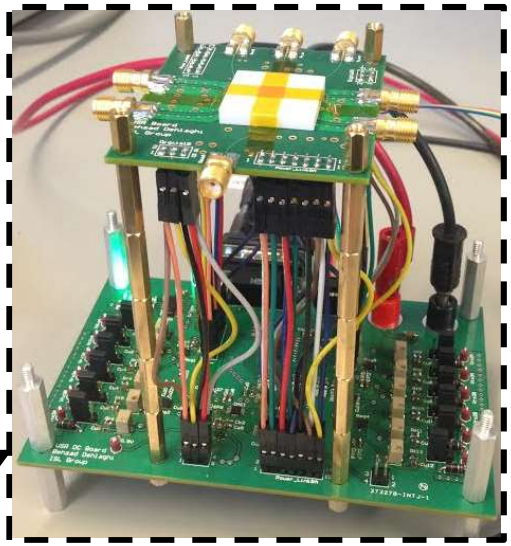
Differential Half-rate Clock

DUT

Die A

Die B

RS232 Interface to Board



Quarter-rate Receiver outputs

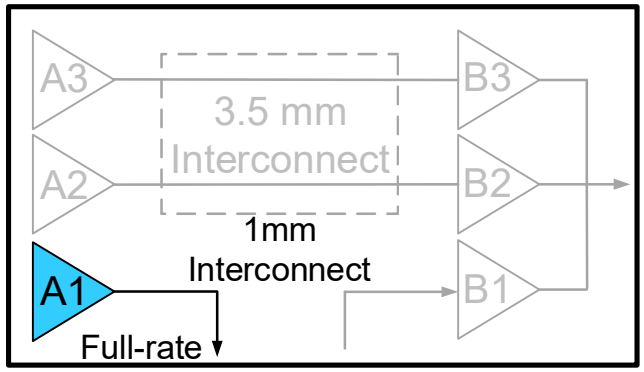
Full-rate TX1A output

Agilent 86100C Sampling Scope

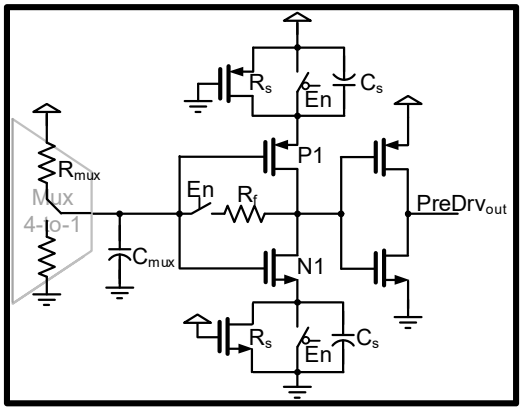
Keysight DSAX91604A Real-time Scope

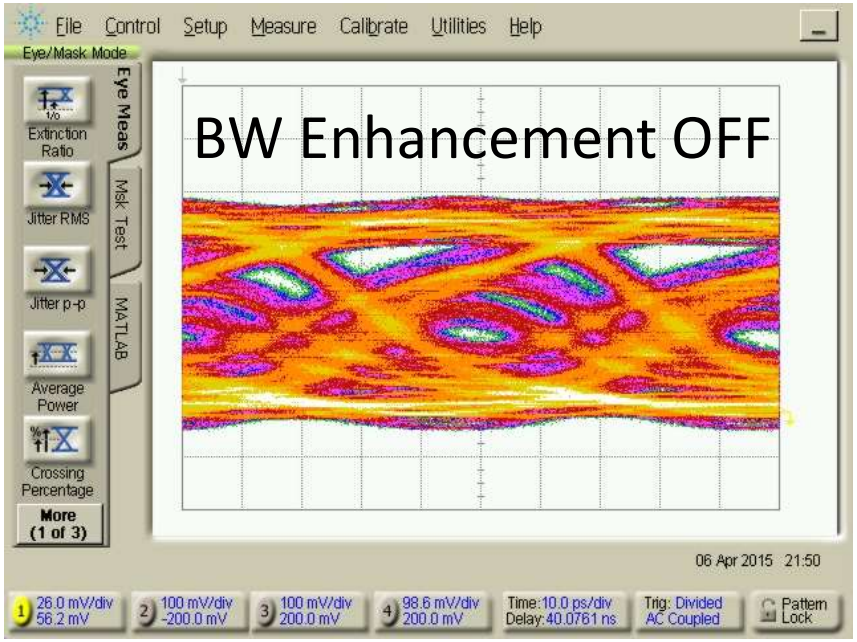
Centallax TG1B1-A BERT

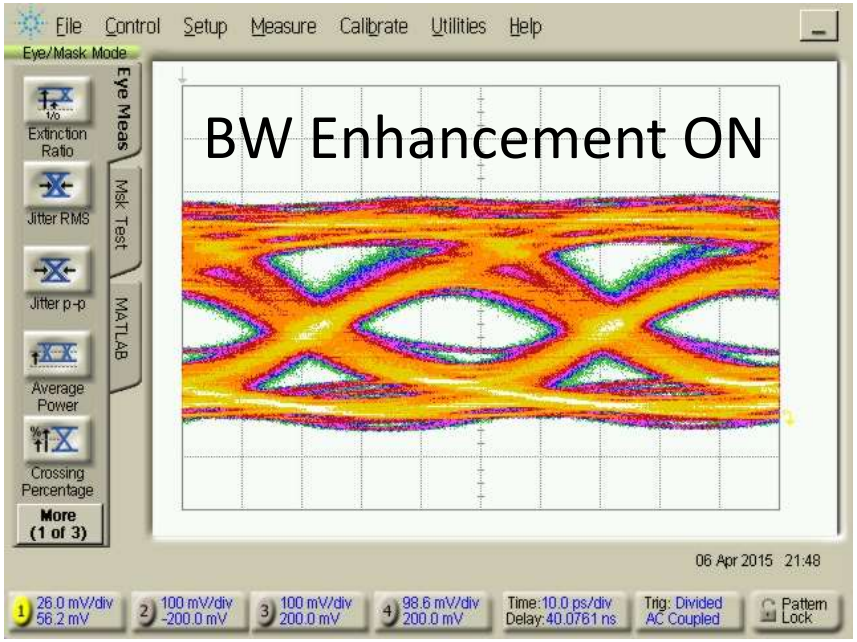
Pre-Driver Bandwidth Enhancement Technique at 20Gb/s



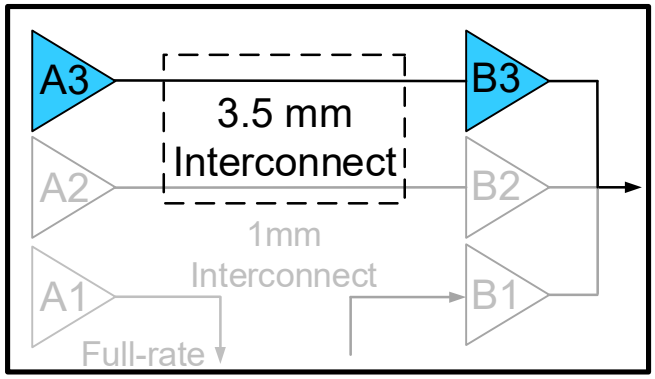
Transmitter Output

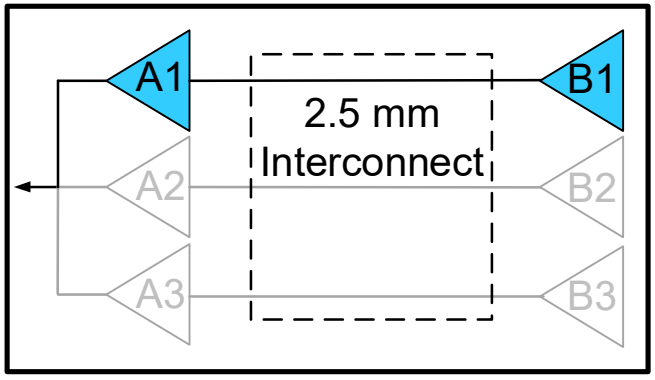




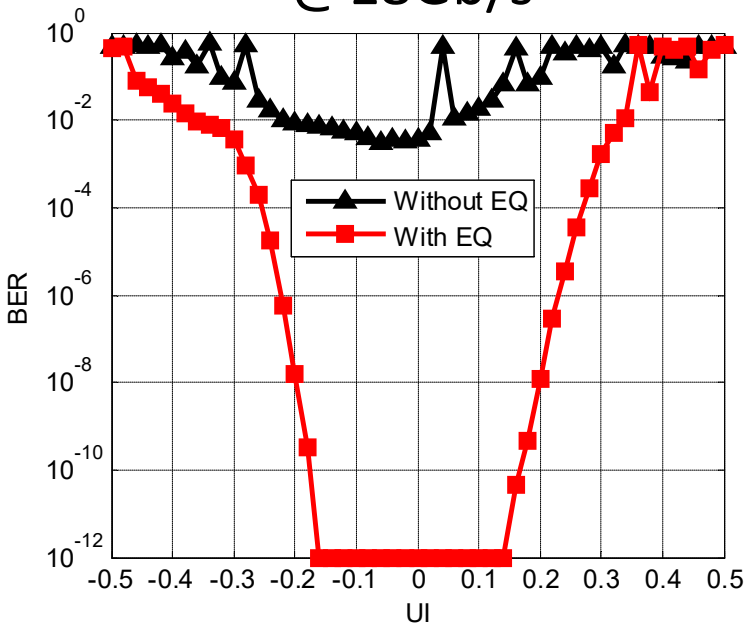


Bathtub curves with and without Transmitter Passive Equalizer

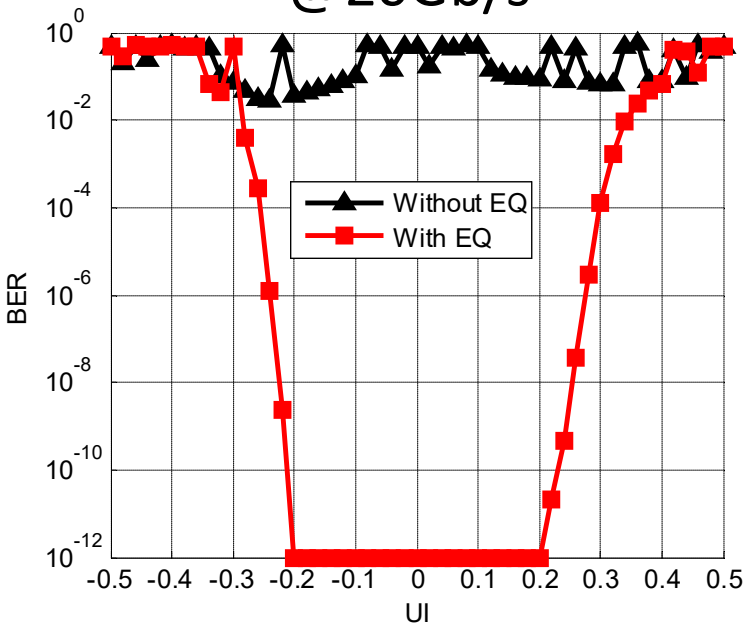




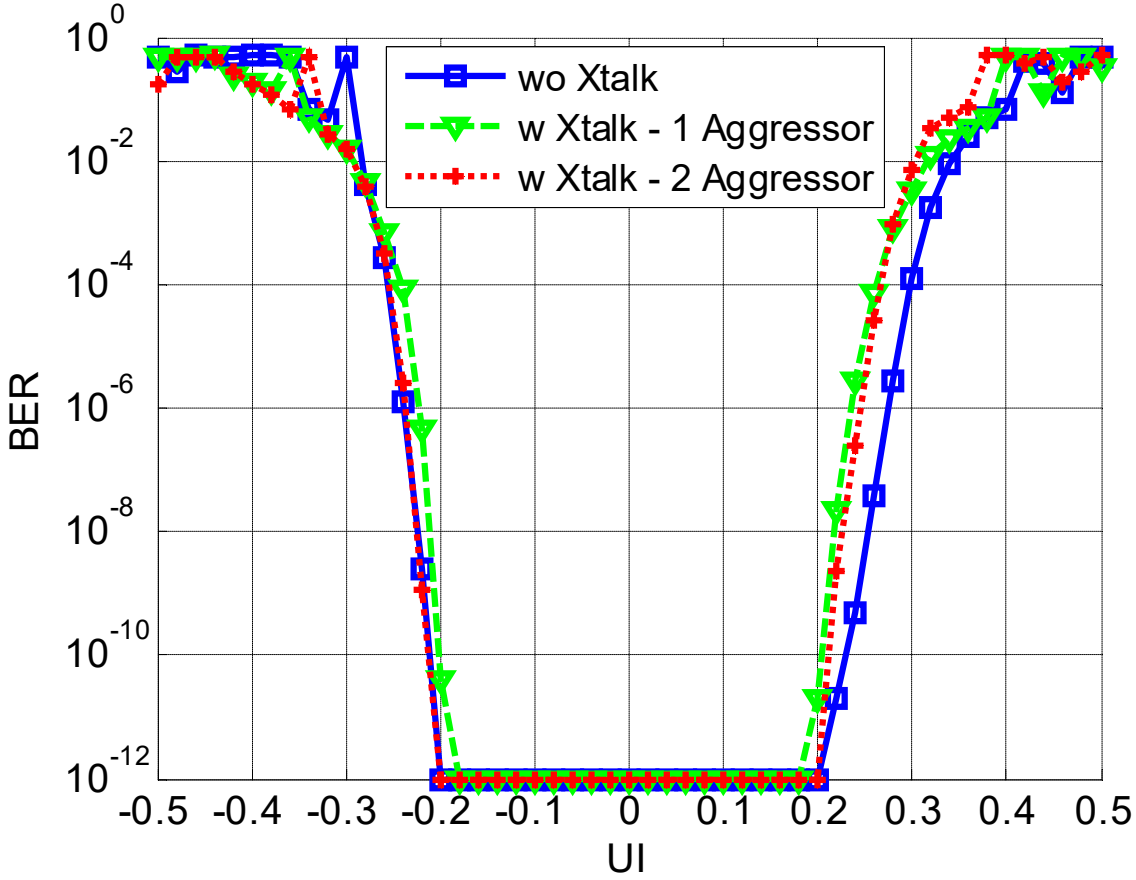
@18Gb/s

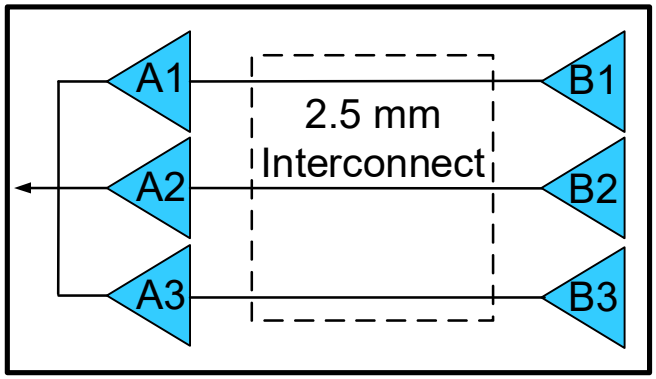


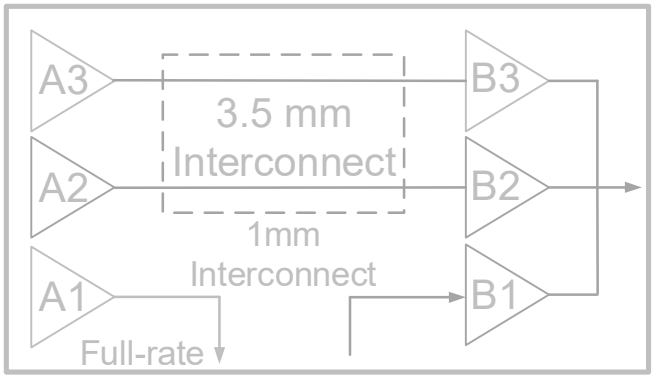
@20Gb/s



Bathtub Curves with and without Xtalk Over 2.5mm Interconnect at 20Gb/s

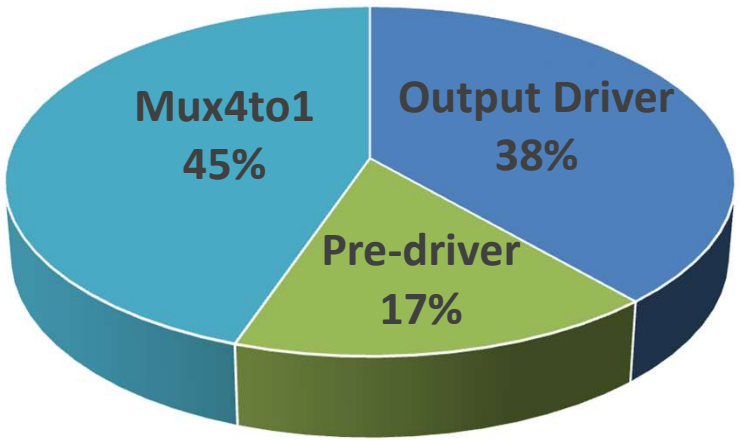




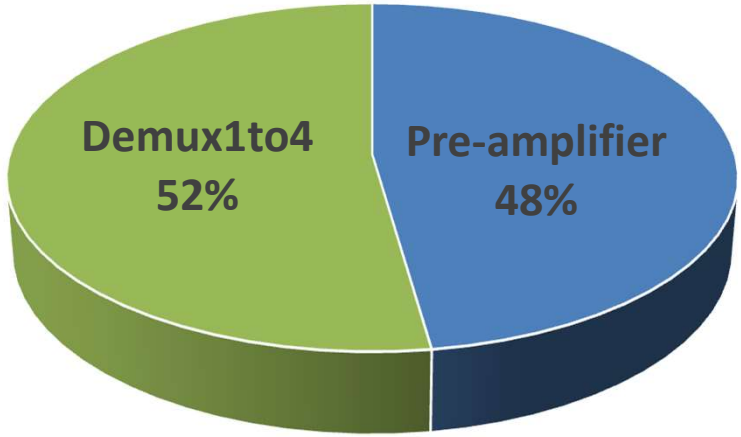


Link Power Breakdown

Transmitter Power Breakdown



Receiver Power Breakdown



Data Rate [Gb/s]	20	18	16.4
TX Total Power [mW]	2.8	2.7	2.6
RX Total Power [mW]	3.3	3.0	2.9
Link Energy Efficiency [pJ/bit]	0.30	0.32	0.33

Performance Summary

	JSSC12 [Dickson]	JSSC13 [Poulton]	JSSC12 [Amirkhani]	This Work	
Signaling	Diff. VM	SE Ground Referenced	SE VM	**SE VM**	
Channel	Si Int. 3µm-thick Cu	Organic Substrate	FR4	**Si Int. 0.64µm-thick Al**	
Equalization	IIR-DFE	-	TX FIR + RX CTLE + DFE	**TX Passive EQ**	
Technology	45-nm SOI	28-nm	40-nm	**28-nm SOI**	
Area [mm²]	0.023[a]	0.005	-	**0.009[b]**	
Channel Pitch	22µm	67µm	-	**10µm**	
Atten. @ Nyquist (Relative to DC)[dB]	- (11.1)	1 (1)	10 (10)	**13.5 (7.7)**	**10.7 (5.9)**
Data Rate [Gb/s]	10	20	12.8	**18**	**20**
Energy Efficiency [pJ/bit]	2.6[c]	0.255[c]	2.15[c]	**0.32**	**0.3**

[a] The transmitter area is calculated in a way to fit under 6 µC4 bumps [1].
[b] Does not include the decoupling capacitors, clocking and PRBS generator circuits.
[c] The energy efficiency of transceiver excluding the clocking is calcuted based on the reported power breakdown.

Conclusions

- A die-to-die transceiver for 0-15 dB loss channels on silicon interposer or organic substrate was introduced.
- Single-ended signaling was employed to maximize the pin/wire efficiency.
- A bandwidth enhancement technique for CMOS logic circuits was introduced.
- Energy efficiency of 0.3pJ/bit was achieved by using a passive EQ and CMOS logic circuitry in the transceiver building blocks.

References

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