# A 20Gb/s 0.77pJ/b VCSEL Transmitter with Nonlinear Equalization in 32nm SOI CMOS

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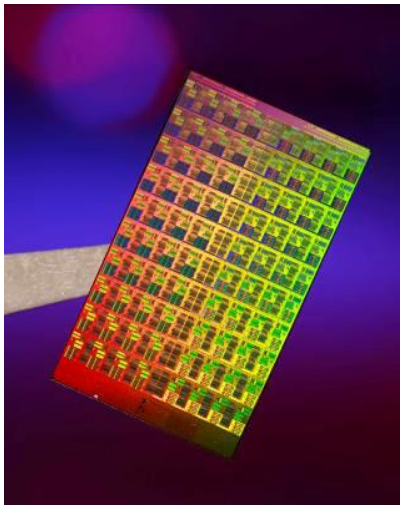
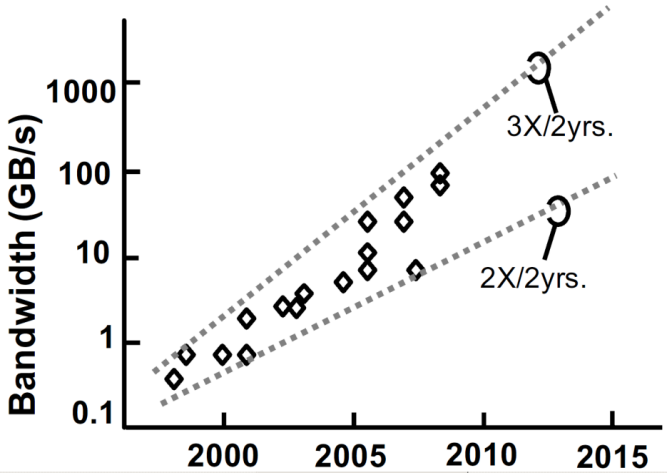
# Increasing I/O B.W.Demand

- **Multi-core μProcessors demand high aggregate bandwidth**
- **Bandwidth scaling with limited IO power budget**
- **Bandwidth of the electrical channels has not scaled similarly**

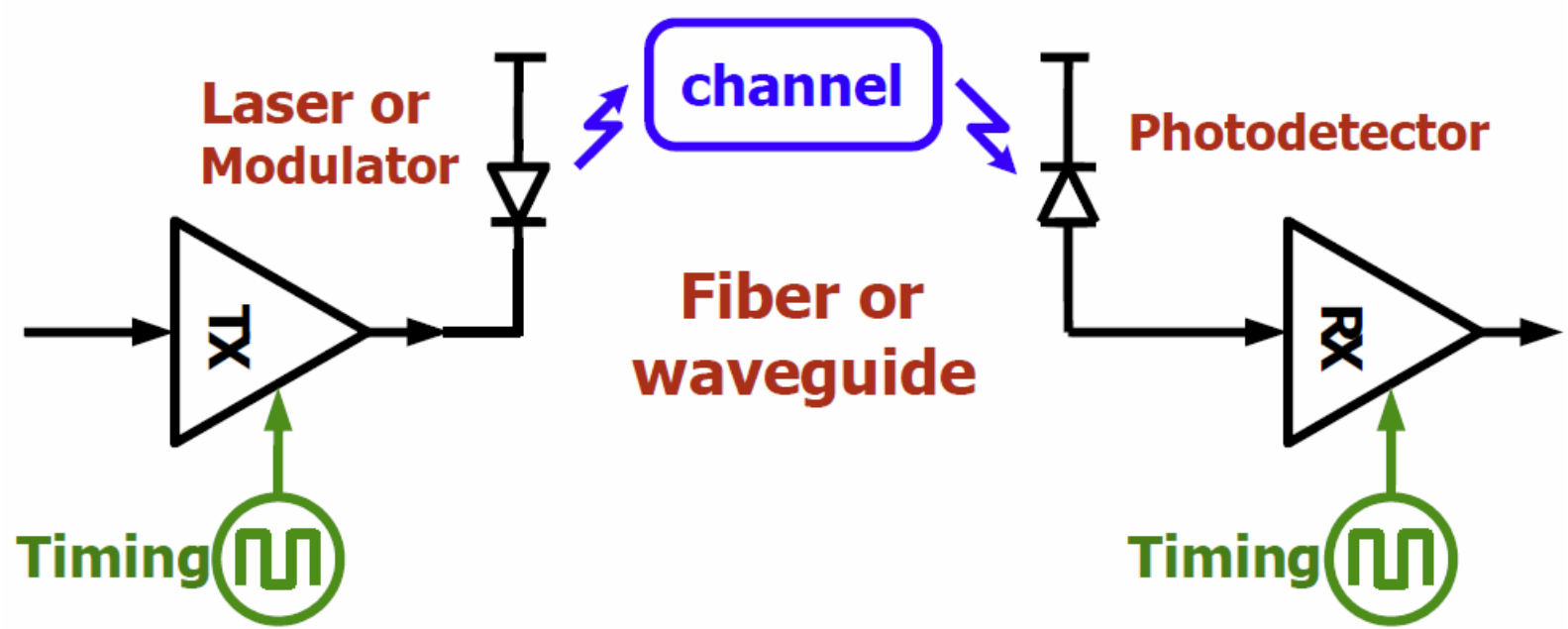


S. Vangal *et al.*, “An 80-Tile Sub-100W TeraFLOPS Processor in 65nm CMOS," *JSSC*, 2008.



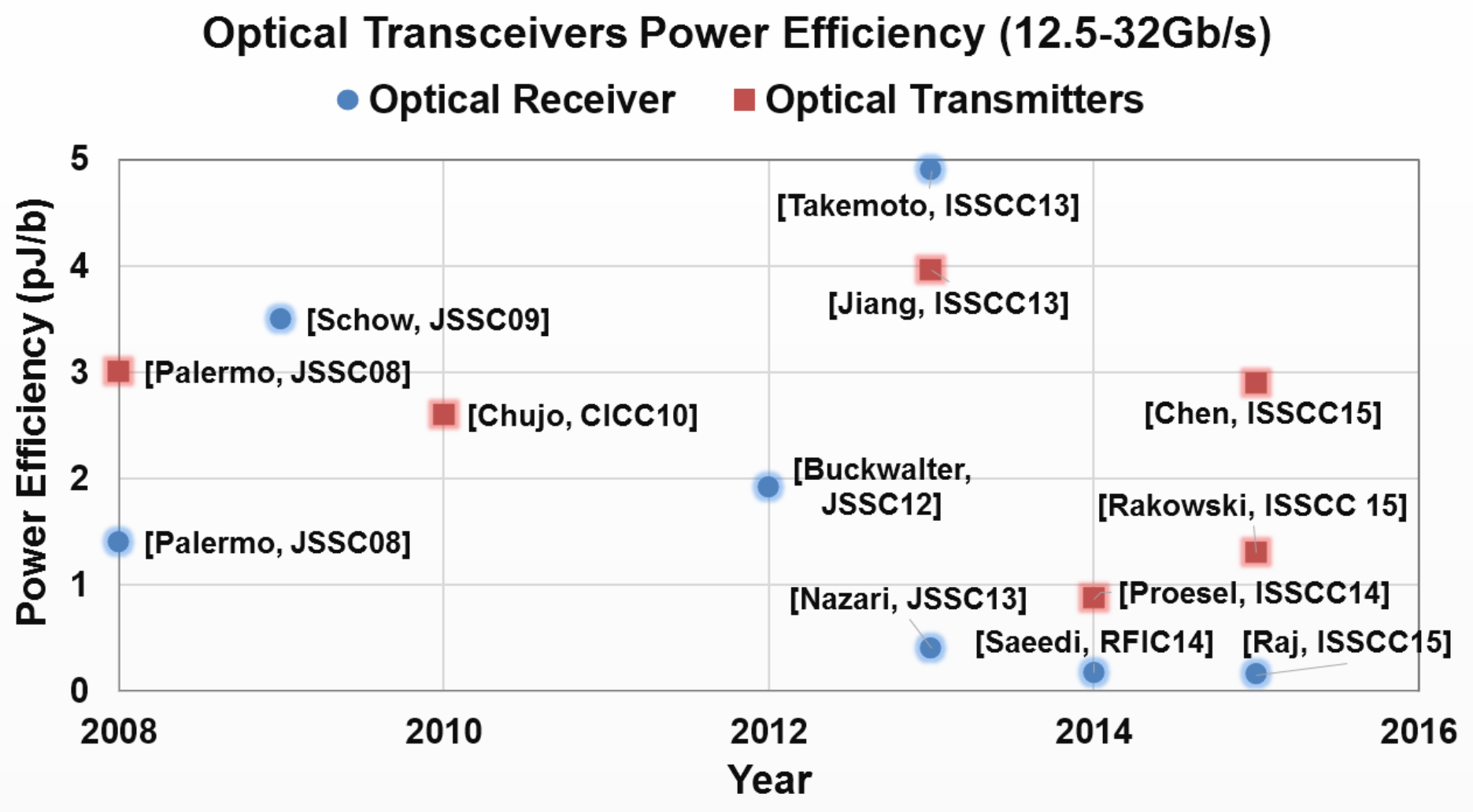

Frank O’Mahony, *et al.*, *VLSI Symposium,* 2009.

# Optical Interconnects




- Optical interconnects can remove many channel limitations
- Promising solution only if power saving is significant

# Optical Power Efficiency

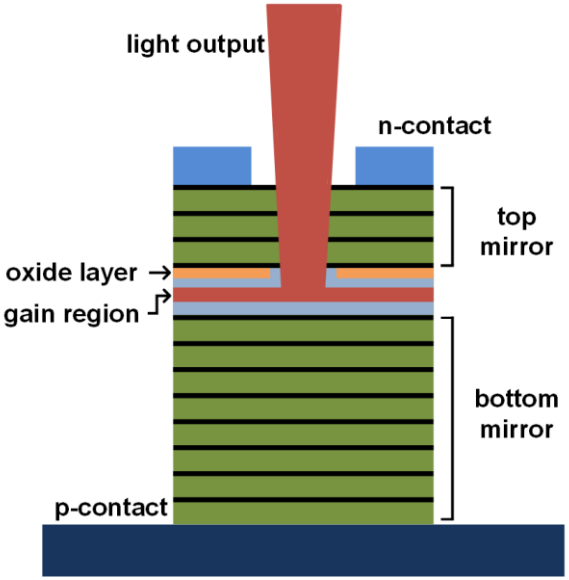


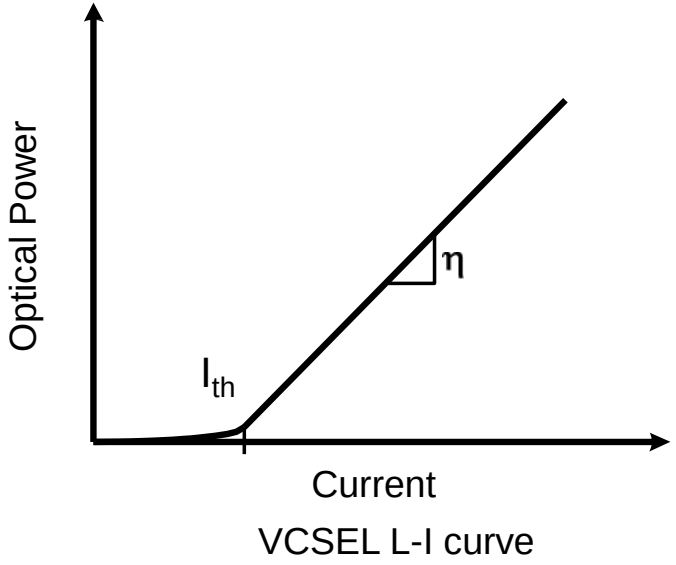

**Optical transmitters are mostly over 1pJ/b**

# Outline

- Introduction to VCSEL Speed Limitations
- Dynamic VCSEL modelling
- Proposed Equalization Technique
- Measurement Results
- Conclusions

# Why VCSELs?



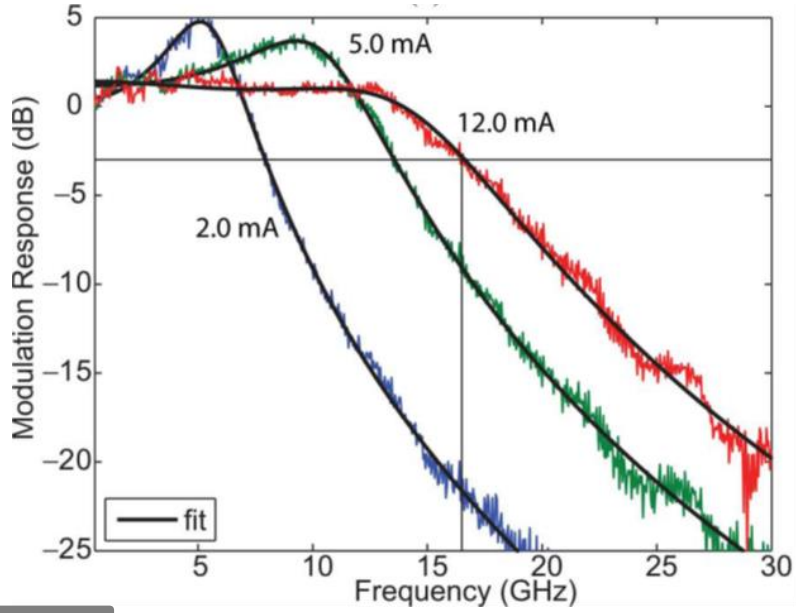




VCSEL L-I curve

- **Vertical Cavity Surface Emitting Laser**
- **Low cost**
- **Better integration**
- **Optical power linear function of current**

# VCSEL Speed Limitations

- **Inherent bandwidth limitations**
- **Second-order low-pass transfer function**
- **Not linear !**
- **Needs equalization**



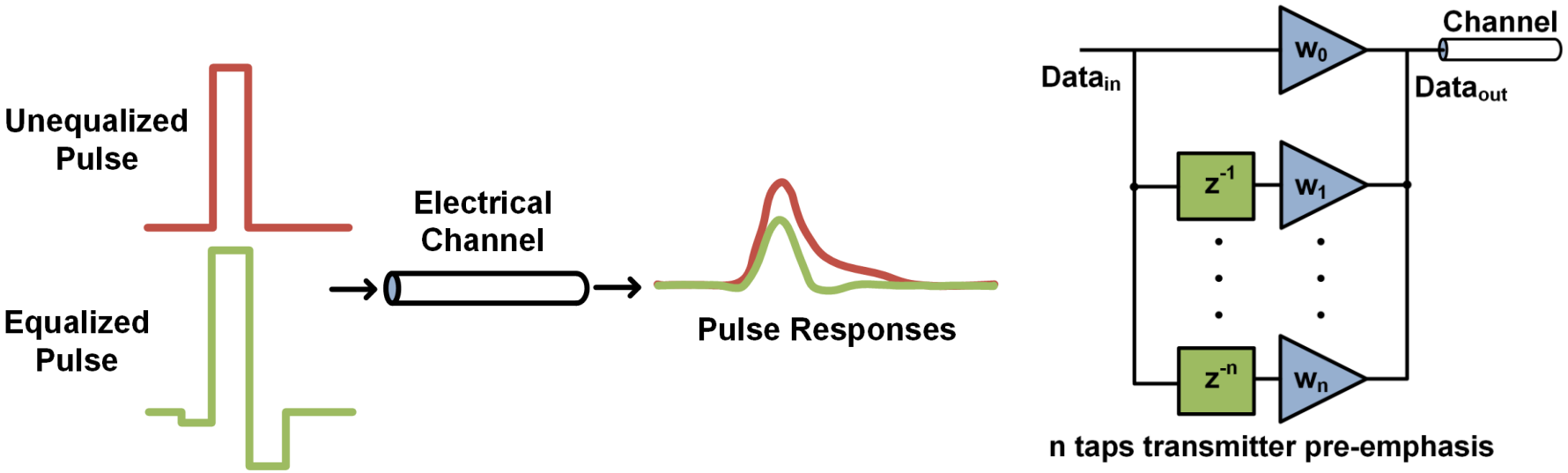

**VCSEL AC Characteristics***

$$H_i(f) = \frac{{f_r}^2}{{f_r}^2 - f^2 + j(\frac{f}{2\pi})\gamma}$$

$$f_r = D\sqrt{I_D - I_{th}} \qquad \gamma = Kf_r^2 + \gamma_0$$

*P. Westbergh, J. S. Gustavsson, Å. Haglund, M. Sköld, A. Joel, and A.Larsson, “High speed, low current density 850 nm VCSELs,” IEEE J.Sel. Top. Quantum Electron., vol. 15, no. 3, pp. 694–703, 2009.

# Conventional Equalization




- Pre-distorting the pulse over several bit times
- Based on an LTI channel model
- But is this the best strategy for a VCSEL?

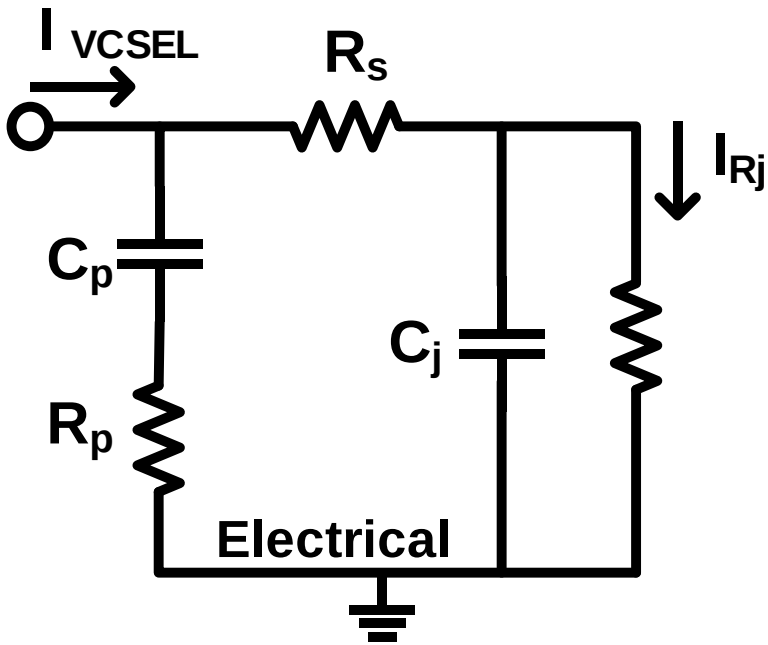
# VCSEL Electrical Model

$$\frac{I_{Rj}(s)}{I_{VCSEL}(s)} = H_1(s) \times H_2(s)$$

$$H_1(s) = \frac{1+sC_pR_p}{1+sC_p(R_p+R_s)+\frac{sC_pR_j}{1+sC_jR_j}}$$

$$H_2(s) = \frac{1}{1+sC_jR_j}$$

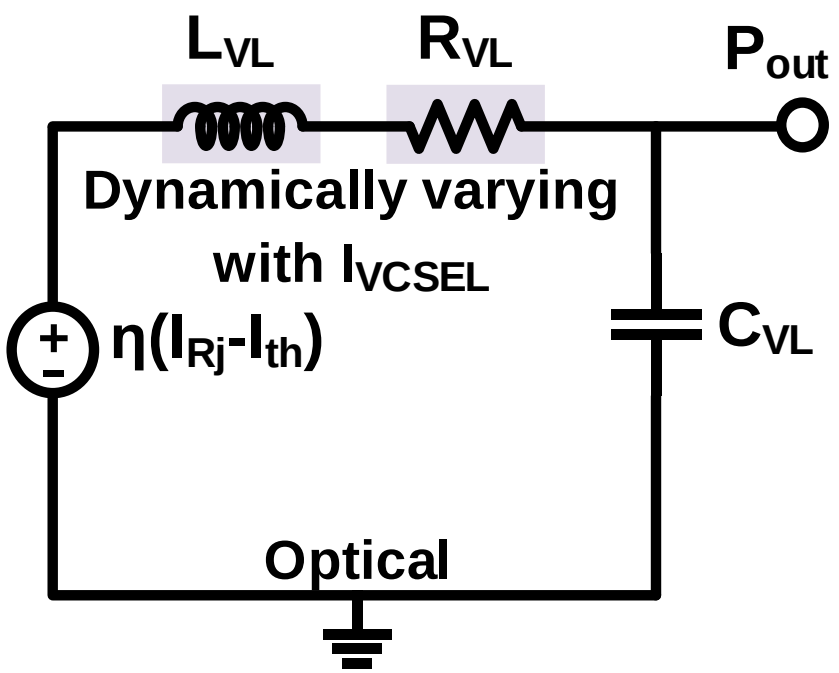
$$\frac{I_{Rj}(s)}{I_{VCSEL}(s)} \approx \frac{1}{1+sC_jR_j}$$




**Low pass filter with dominant pole at $C_jR_j$**

# VCSEL Optical Model

- $H_i(f)$ can be represented as a series RLC circuit
- Fix $C_{VL}$ then $R_{VL}$ and $L_{VL}$ are dependent on the current flowing through the VCSEL
- To take this effect into account $R_{VL}$ and $L_{VL}$ are modeled in VerilogA

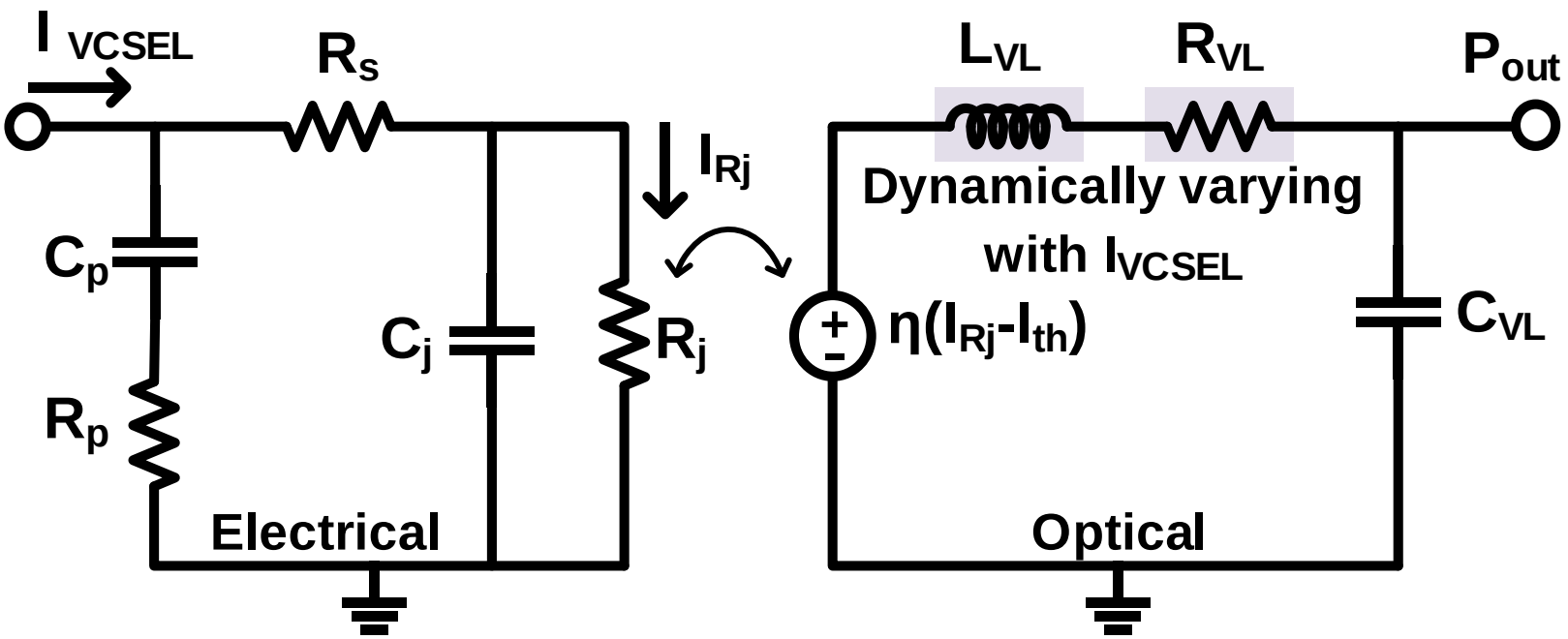



$$C_{VL}=100fF$$

$$L_{VL}=1/\{4\pi^2 C_{VL} D^2 (I_D-I_{th})\}H$$

$$R_{VL}=(Kf_r^2+\gamma_0)L_{VL}\Omega$$

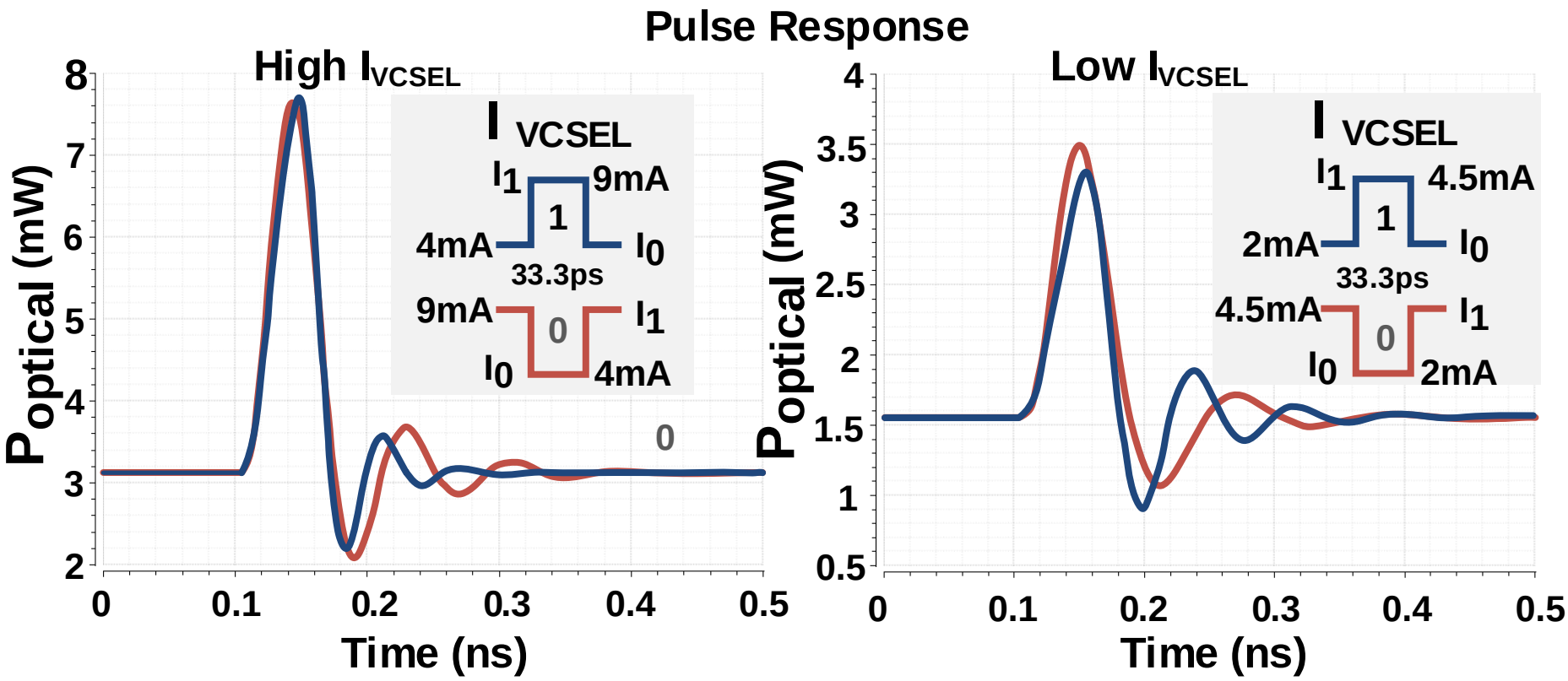
# VCSEL Complete Model




| Electrical Parameters | Value |
|---|---|
| Junction Capacitance ($C_j$) | 110fF |
| Junction Resistance ($R_j$) | 150Ω |
| DBR Resistance ($R_s$) | 50Ω |
| Pad Capacitance ($C_p$) | 10fF |
| Pad Resistance ($R_p$) | 1Ω |

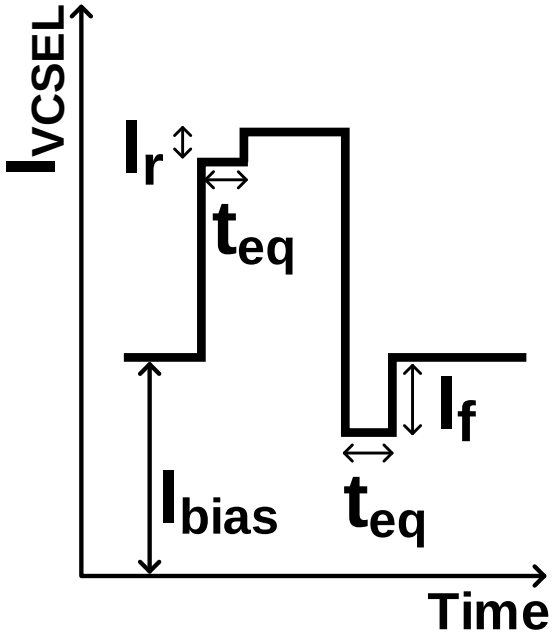
| Optical Parameters | Value |
|---|---|
| Threshold current ($I_{th}$) | 0.6mA |
| Slope efficiency (η) | 0.78mW/mA |
| D-factor (D) | 7.6GHz/mA$^{0.5}$ |
| K-factor (K) | 0.25ns |
| Damping factor offset ($\gamma_o$) | 37ns$^{-1}$ |

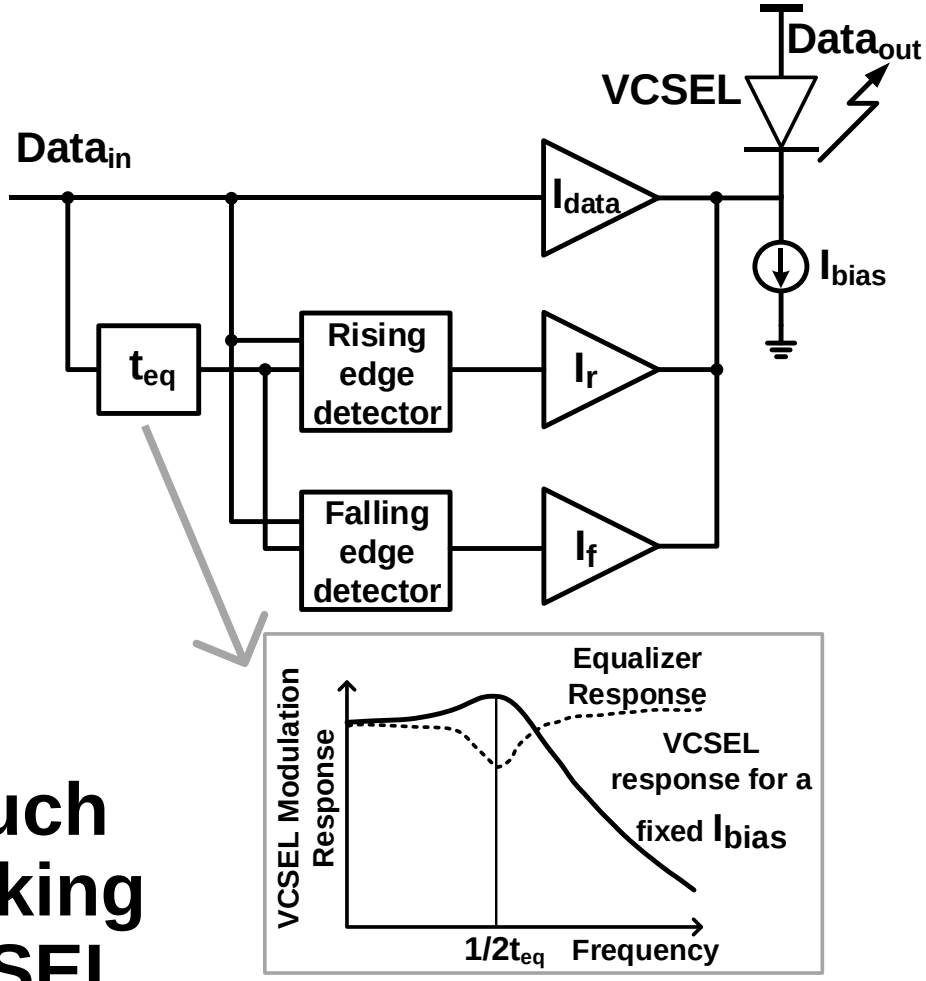
# Nonlinear VCSEL Response




- Responses do not match due to nonlinear nature of VCSEL
- Asymmetry becomes more pronounced as the bias current is reduced

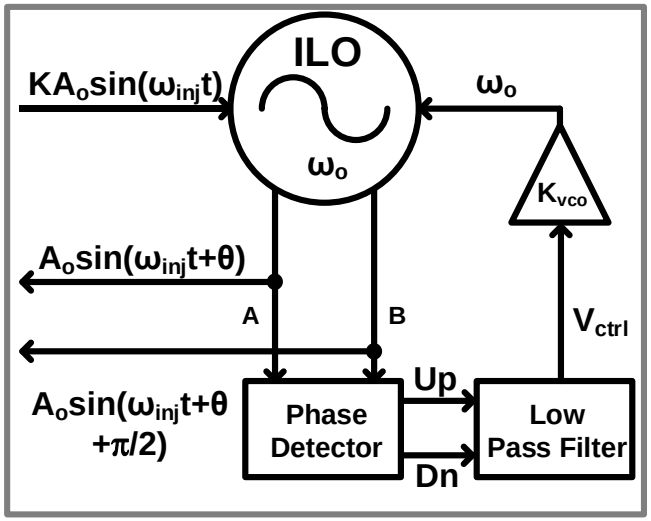
# Equalization Methodology



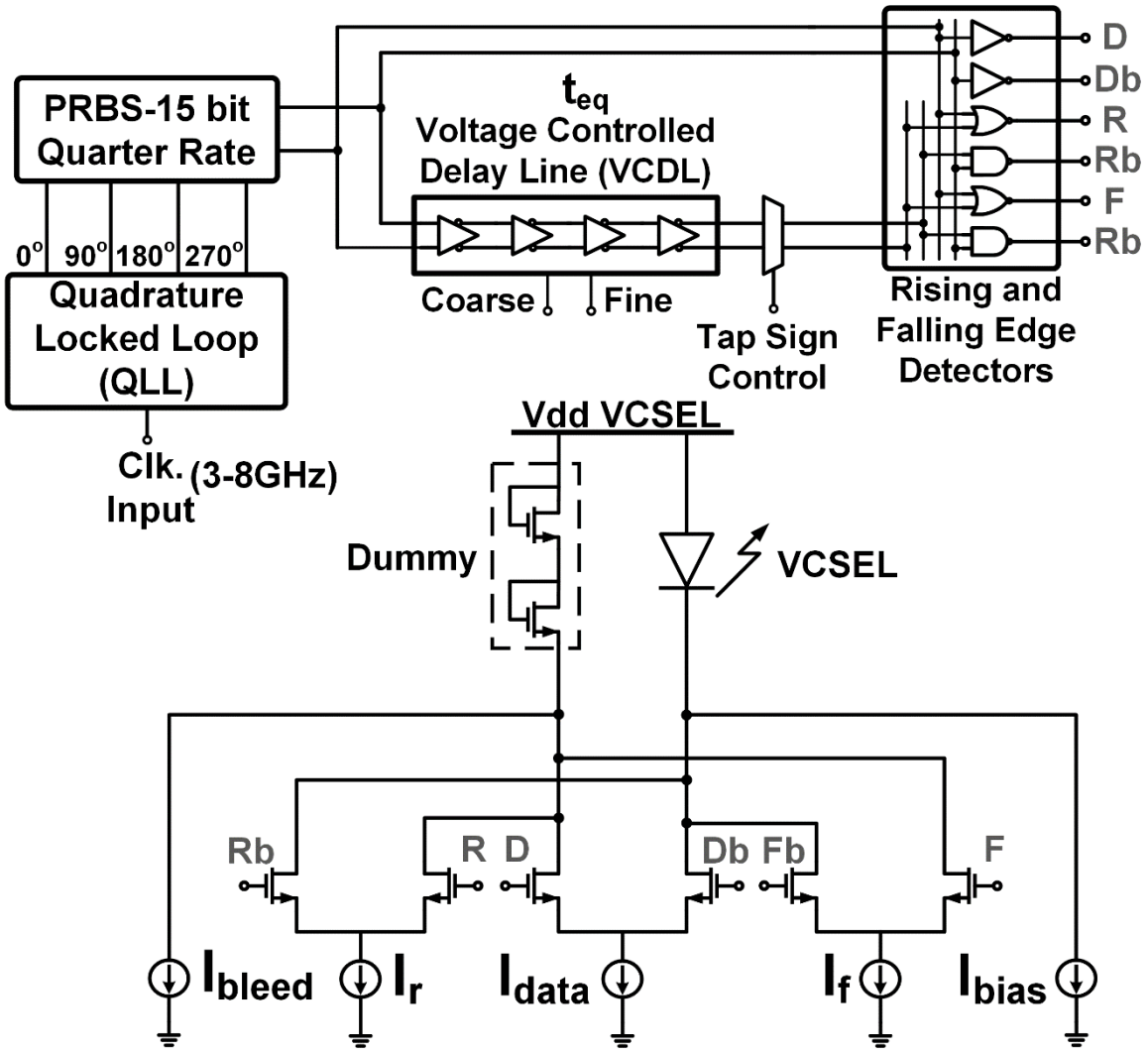




- **Asymmetric taps**
- **$t_{eq}$ should be chosen such that the location of peaking matches that of the VCSEL for the given $I_{bias}$**

# System Architecture



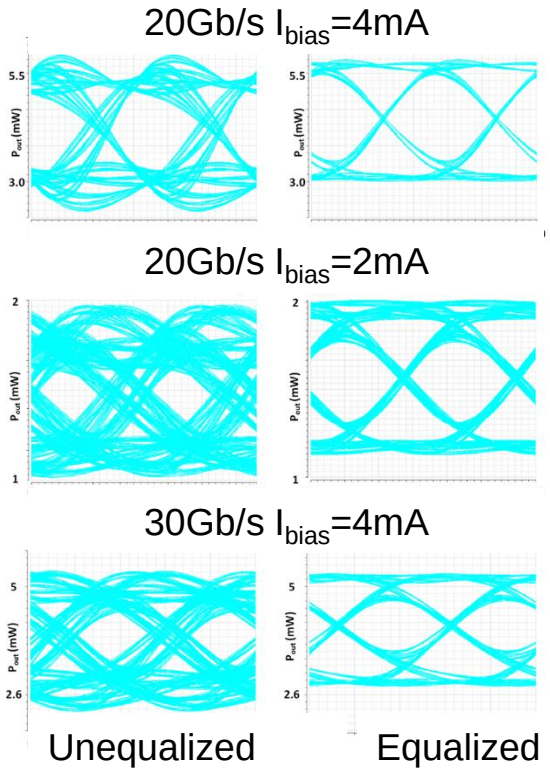

Raj, *et al.* ISSCC15



# Improvement in Optical Eye

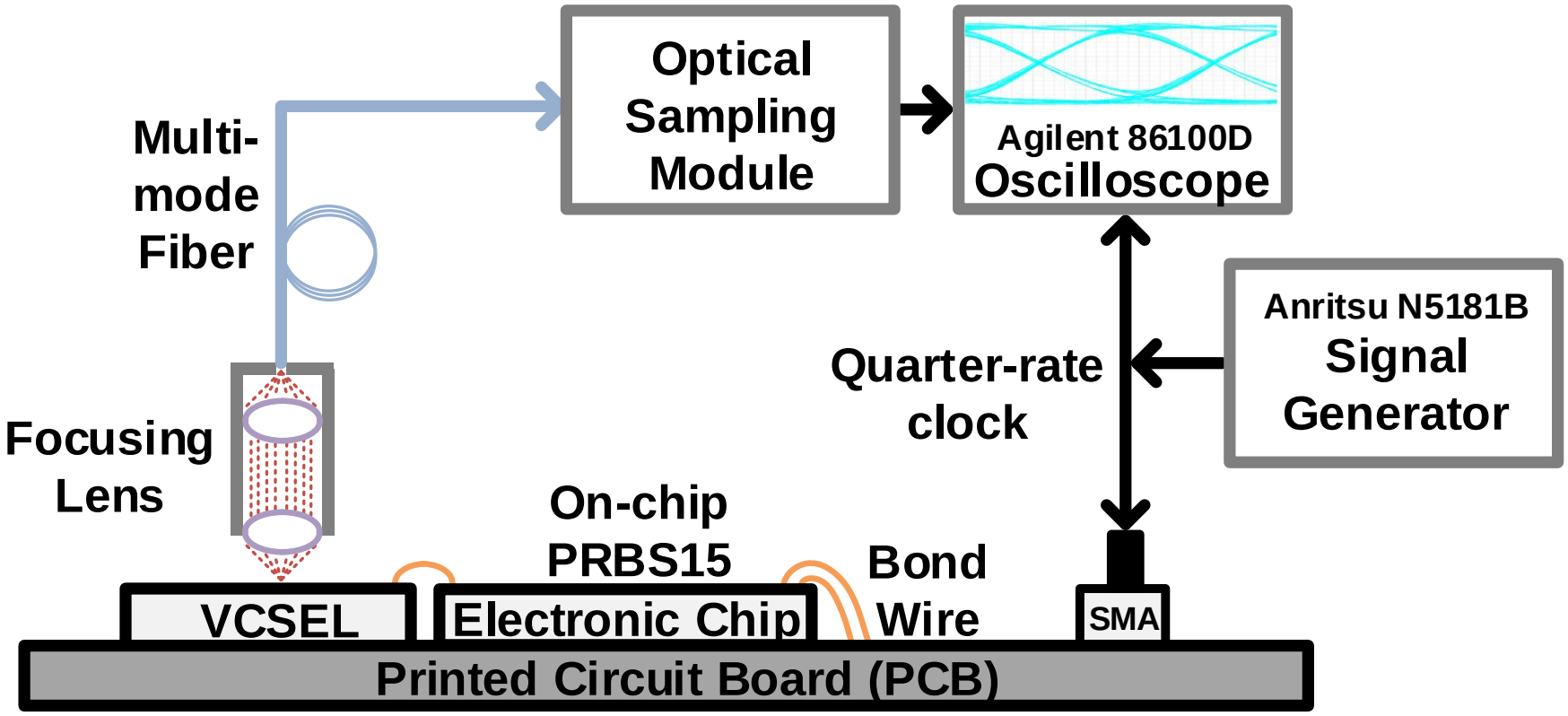
| Data Rate | $I_{bias}$ | Rise Tap ($I_r$/I) | Fall Tap ($I_f$/I) | $t_{eq}$ | % vertical improvement | % horizontal improvement |
|---|---|---|---|---|---|---|
| 20Gb/s | 4mA | 0.25 | 0.19 | 33ps | 16% | 22% |
| 20Gb/s | 2mA | 0.45 | 0.25 | 45ps | 70% | 38% |
| 30Gb/s | 4mA | 0.19 | 0.28 | 33ps | 10% | 33% |

- **Efficient VCSEL equalization the rise and fall taps must be asymmetric**
- **The proposed technique is more effective when the VCSEL is biased at a low current**
- **The $t_{eq}$ delay is independent of the data rate and is dependent on the bias current**



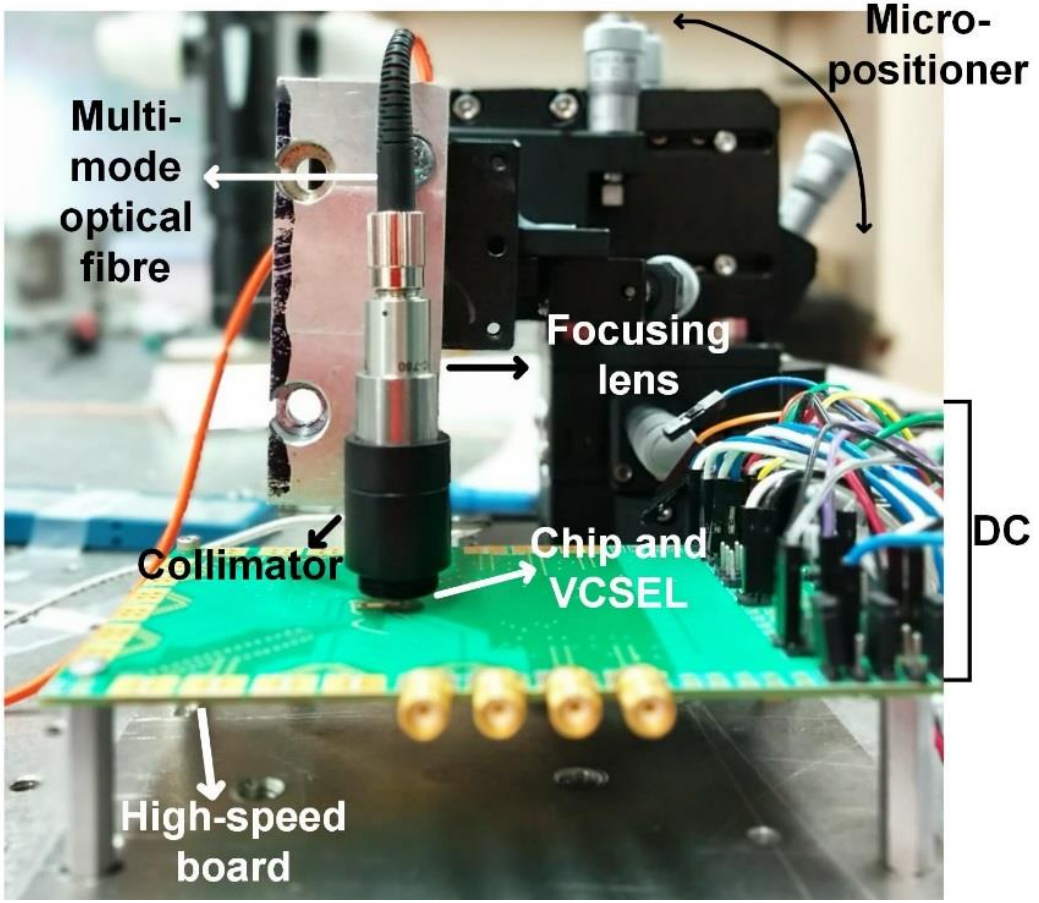

Simulated in 32nm IBM SOI

# Test Setup

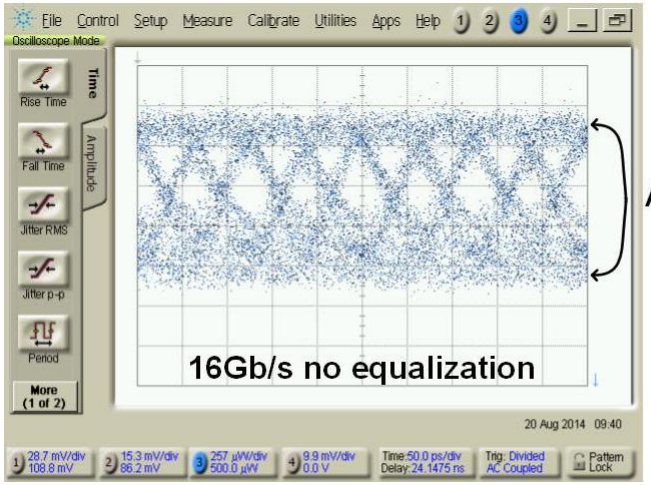

Optical Sampling Module
Agilent 86100D Oscilloscope
Multi-mode Fiber
Anritsu N5181B Signal Generator
Quarter-rate clock
Focusing Lens
On-chip PRBS15
Bond Wire
VCSEL
Electronic Chip
SMA
Printed Circuit Board (PCB)

# Test Setup (Optical)

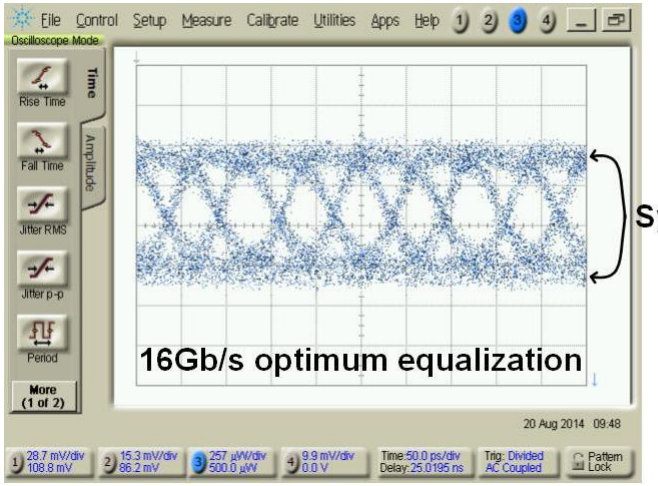
- Collimator followed by a focusing lens
- Focusing lens magnifies the image by 2x
- Reduces the divergence angle of the laser beam
- Better than butt coupling



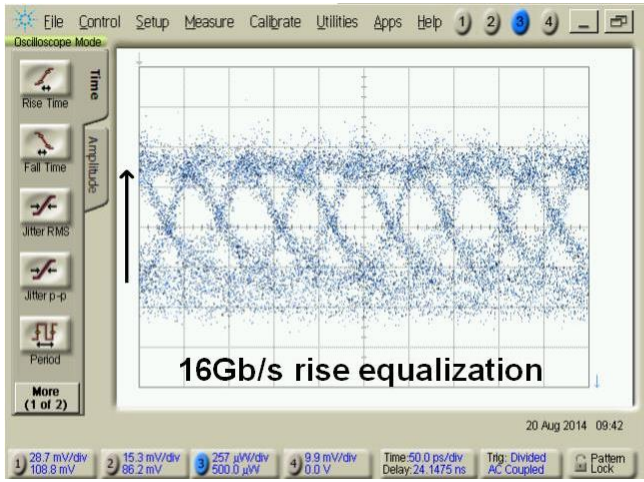
# Measured Optical Eye I

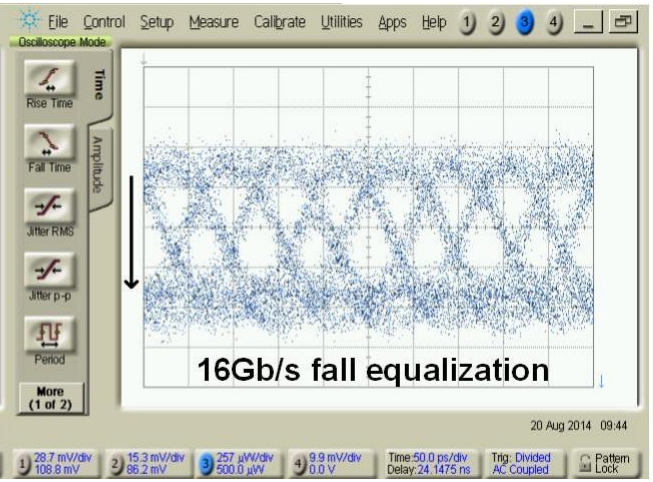



Assymetry

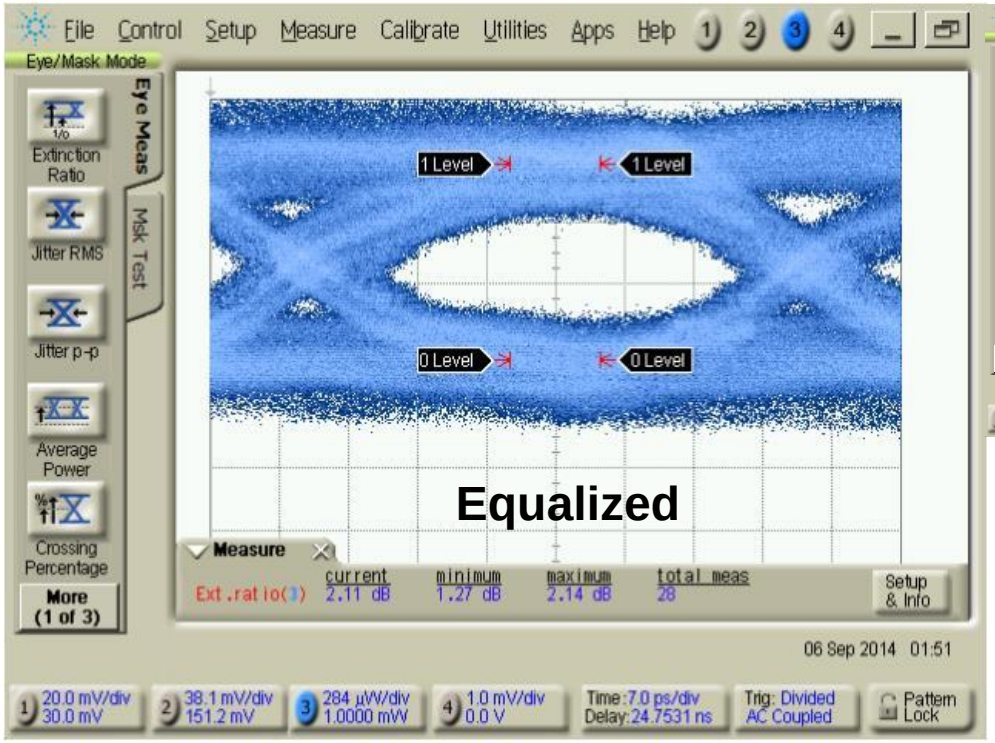


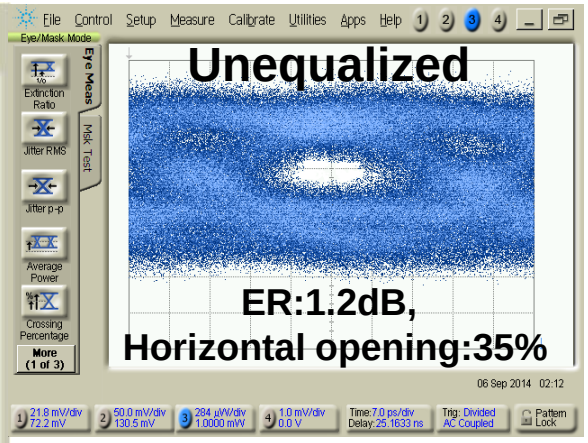

Symmetrical



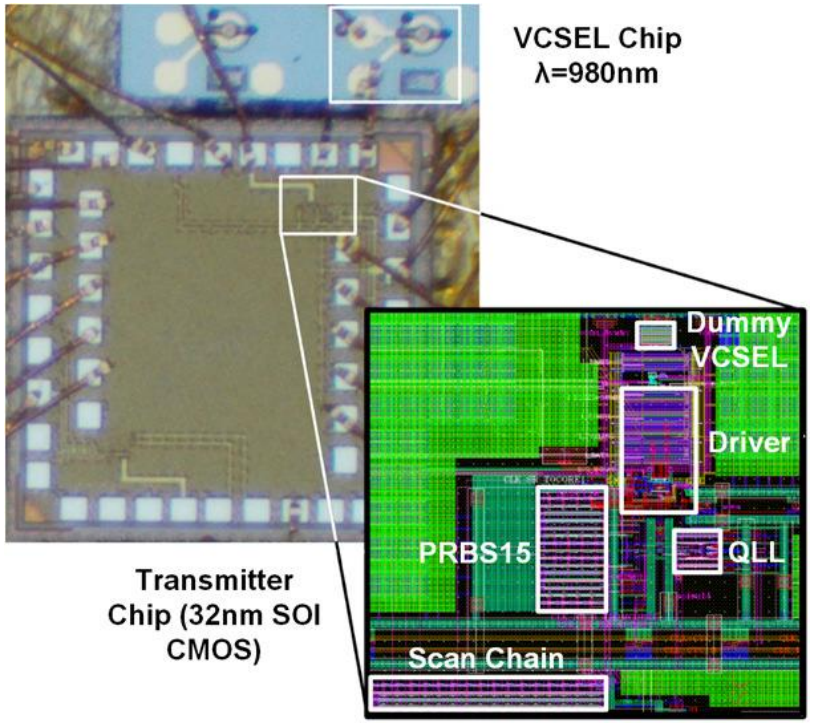



# Measured Optical Eye II




**20Gb/s PRBS 15**
**ER:2dB, horizontal opening 65%**
**0.77pJ/bit**




**32nm SOI IBM**

# Performance Comparison

| | **This Work** | JSSC 2008 | MTT 2010 | ISSCC 2013 | ISSCC 2014 |
|---|---|---|---|---|---|
| Technology | **CMOS SOI 32nm** | CMOS 90nm | CMOS 90nm | CMOS 65nm | SiGe 0.13µm |
| Supply (V) | **1.0/2.5** | 1.0/2.8 | 1.0/- | 1.2/3.6 | 2.5/3.3 |
| Data Rate (Gb/s) | **20** | 16 | 10 | 25 | 40 |
| Power (pJ/b) | **0.77** | 3.0 | 5.0 | 3.96 | 7.80 |
| OMA (dBm) | **0.9** | 1.4 | 2.5 | 0.8 | 2.3 |

# Summary

- Dynamic VCSEL modeling for an efficient non-linear equalization technique
- Variable equalization delay to match VCSEL characteristics
- Ultra-low power consumption (0.77pJ/bit at 20Gb/s)
- Scalable to higher data rates

# Acknowledgement


- Sandia National Labs for providing the VCSELs
- D.K. Serkland for helpful technical discussions
- IBM for chip fabrication
- MICS and CHIC Labs at Caltech