A 4×20-Gb/s 0.86pJ/b/lane 2-Tap-FFE Source-Series-Terminated Transmitter with Far-End Crosstalk Cancellation and Divider-less Clock Generation in 65nm CMOS

Shuai Yuan[1], Liji Wu[1], Ziqiang Wang[1], Xuqiang Zheng[1], Wen Jia[2], Chun Zhang[1], Zhihua Wang[1]

[1]Tsinghua University, Beijing, China

[2]Research Institute of Tsinghua University in Shenzhen, Shenzhen, China

Outline

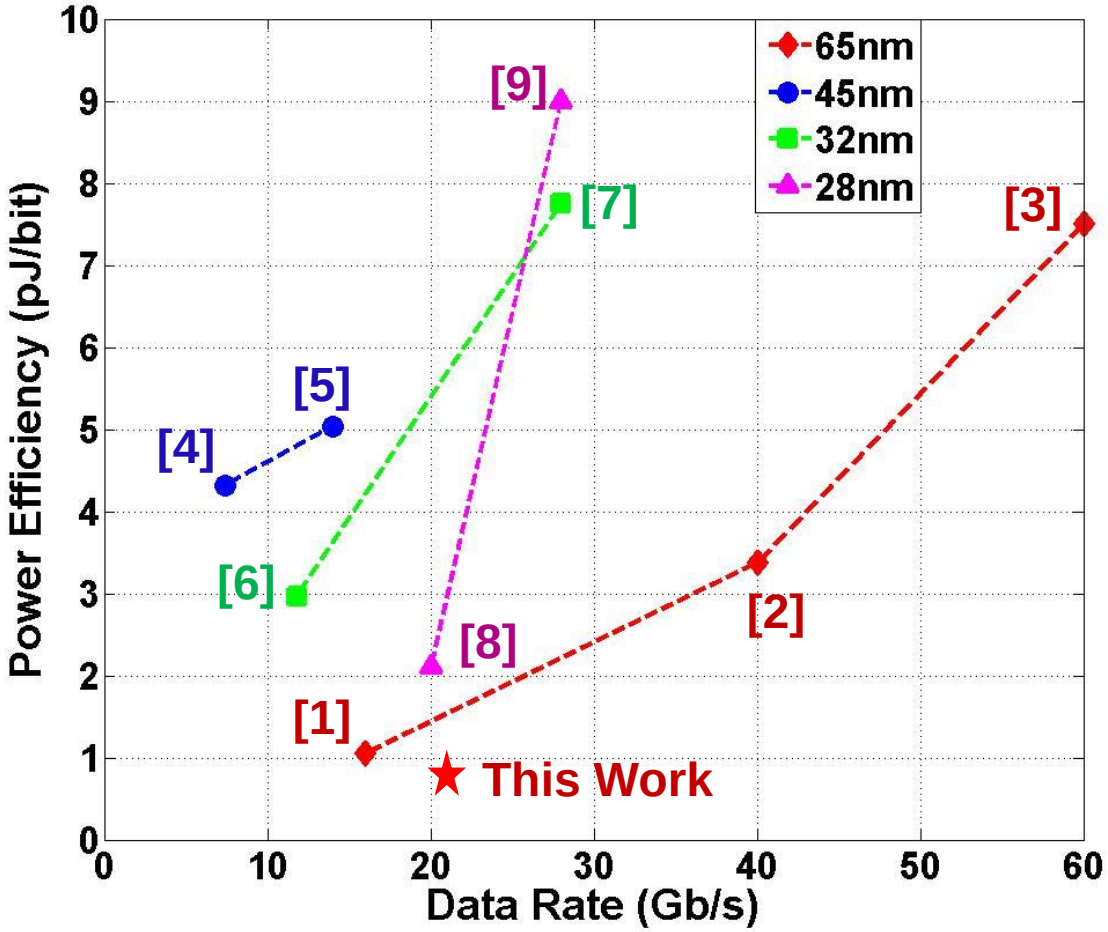
- Motivation
- Transmitter Architecture
- Circuit Implementation
- Measurement Results
- Conclusion

Outline

- **Motivation**
- Transmitter Architecture
- Circuit Implementation
- Measurement Results
- Conclusion

Motivation

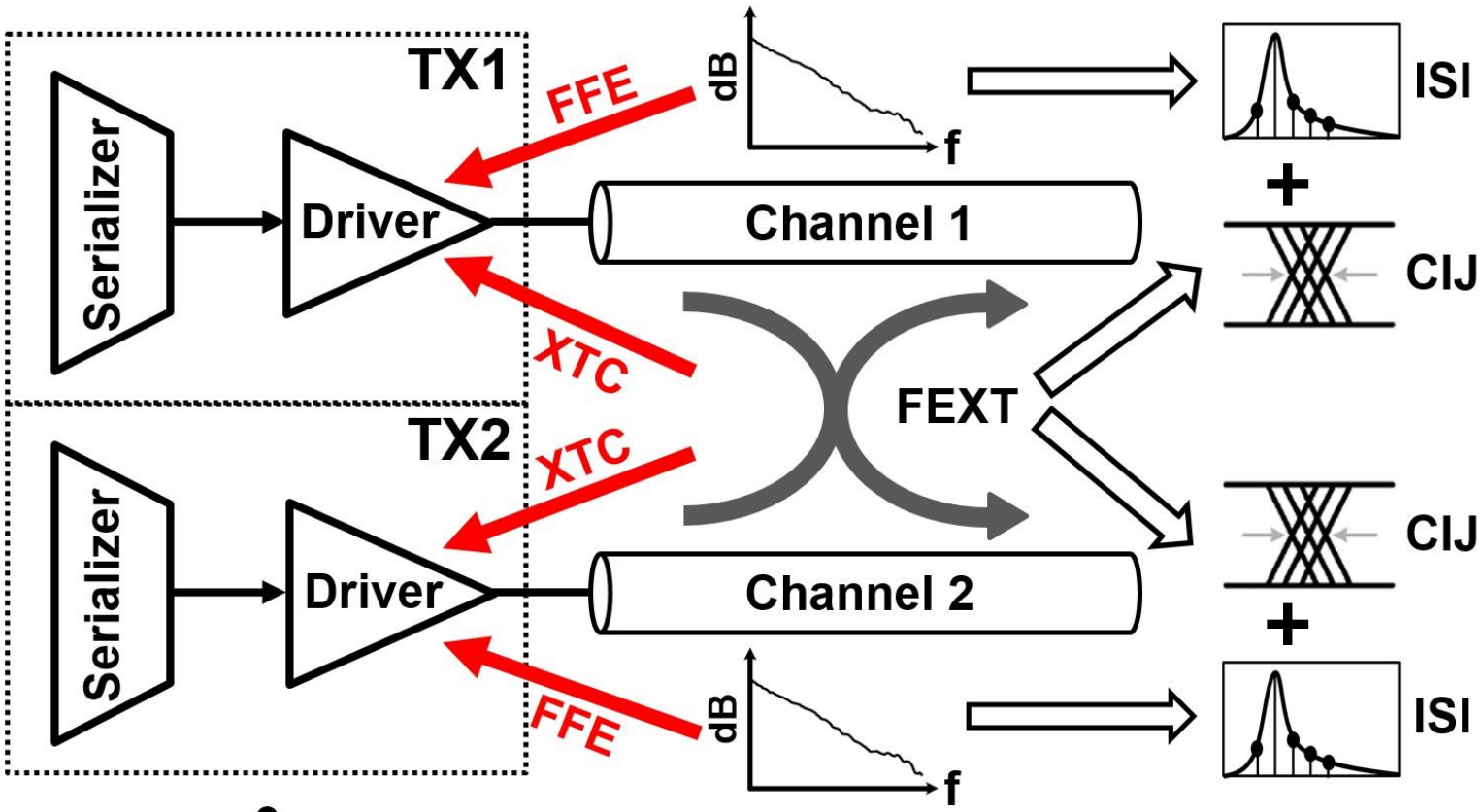
- To design a ≥ 20Gb/s serial-link transmitter with < 1pJ/bit power efficiency in 65nm CMOS



[1] ISSCC 2014
[2] ISSCC 2011
[3] ISSCC 2014
[4] ISSCC 2010
[5] ISSCC 2011
[6] ISSCC 2010
[7] ISSCC 2012
[8] ISSCC 2014
[9] ISSCC 2015

Motivation

- To design a low-power TX driver with FFE and XTC to compensate both ISI and FEXT

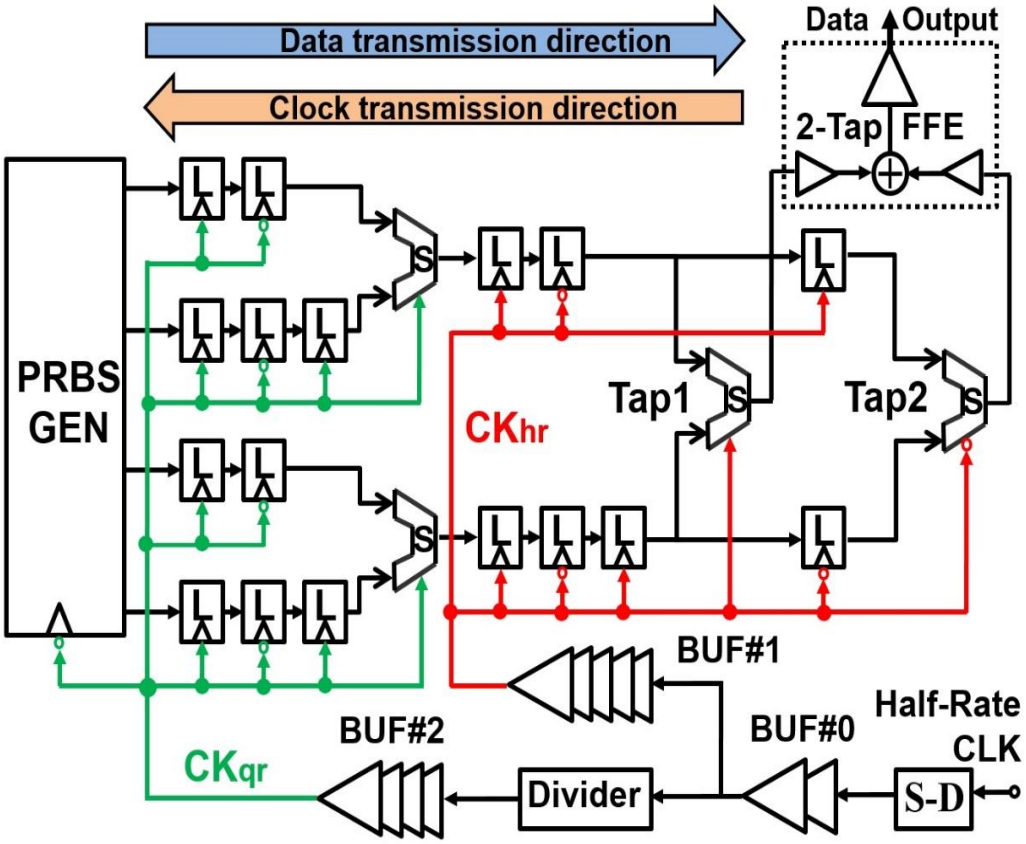


- Multi-channel TX application

Outline

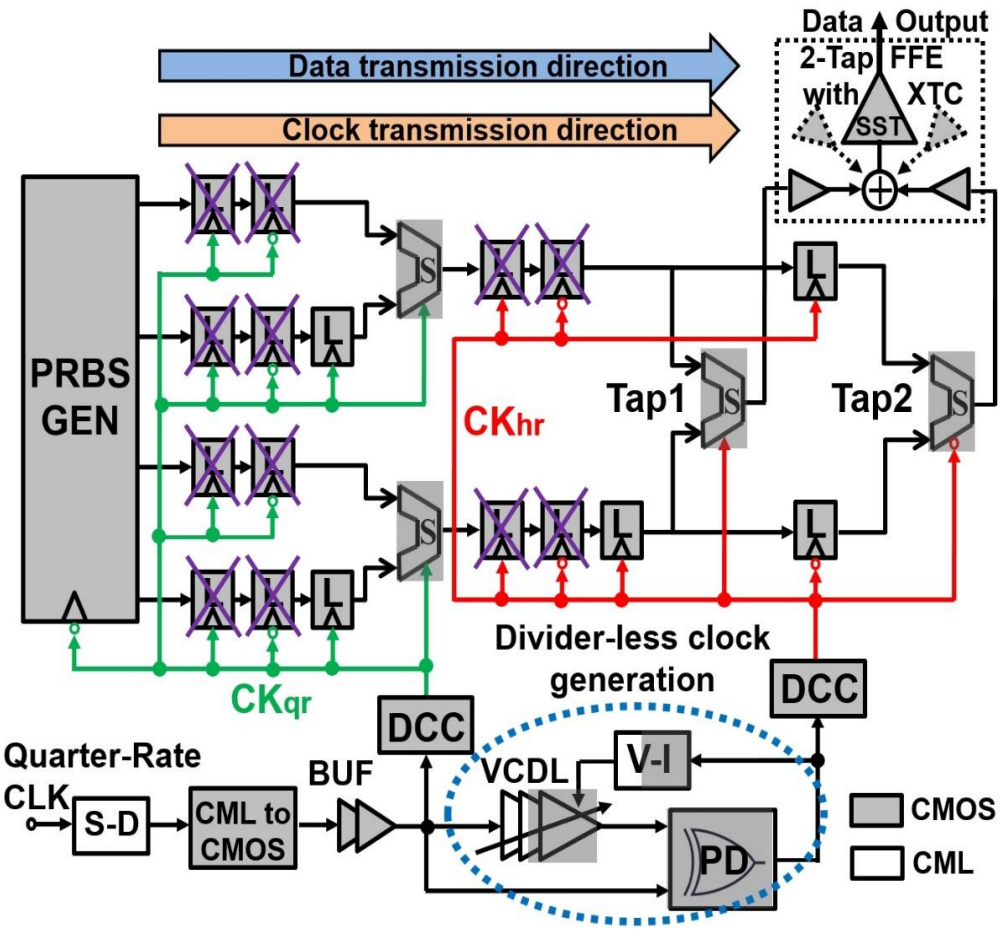
- Motivation
- **Transmitter Architecture**
- Circuit Implementation
- Measurement Results
- Conclusion

Traditional Transmitter Architecture



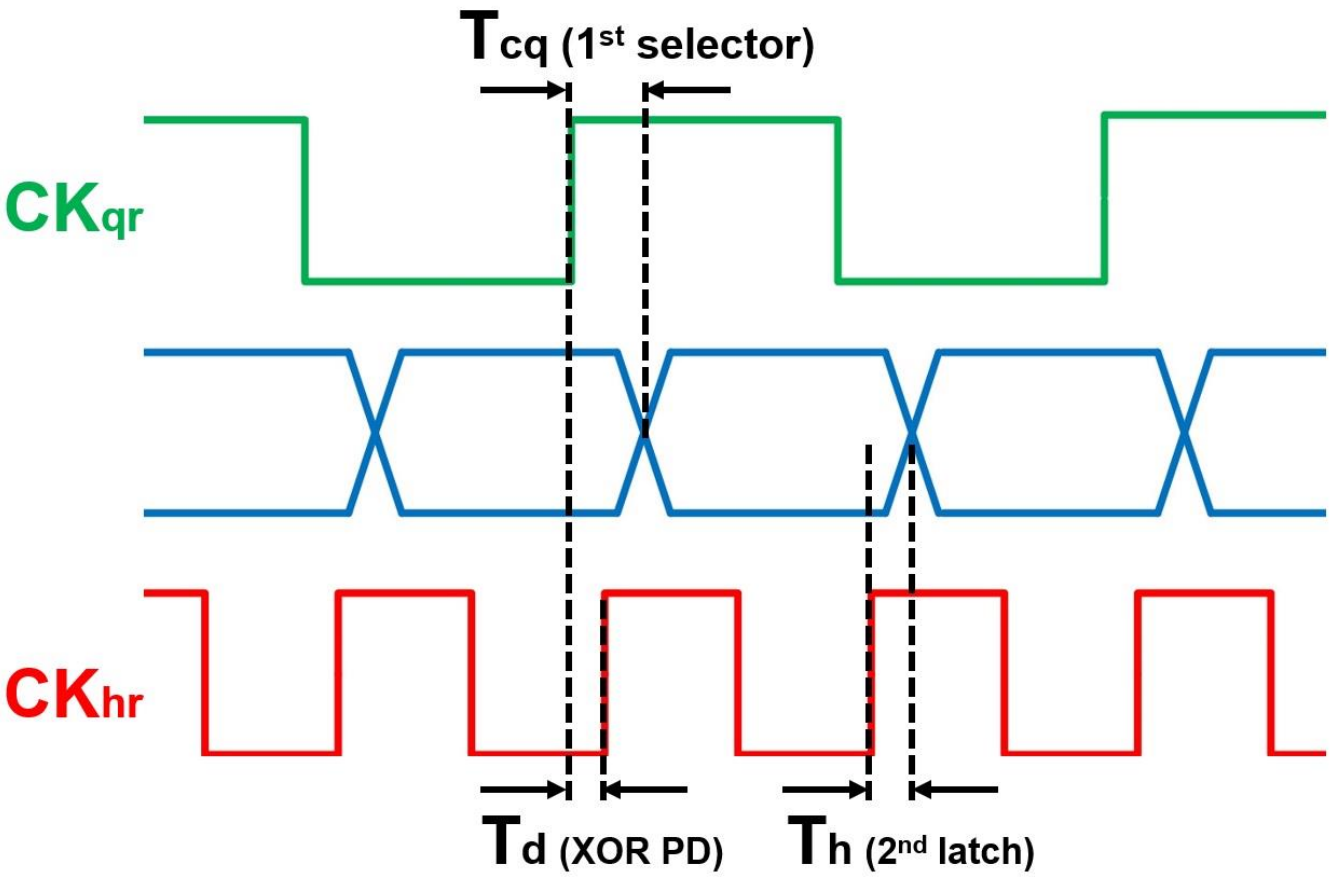
- Half-rate input clock
- The clock transmission direction is opposite to the data transmission direction
- The divider, BUF#1 and BUF#2 are power hungry
- Difficult for the delay matching under PVT variation
- A lot of retiming latches

Proposed Transmitter Architecture



- Quarter-rate input clock
- The clock transmission is in the same direction of the data transmission
- The divider and buffers are eliminated in the proposed divider-less clock generation
- Save 70% latches
- A SST driver merged with the FFE and XTC is proposed

Timing Diagram When Loop Locked



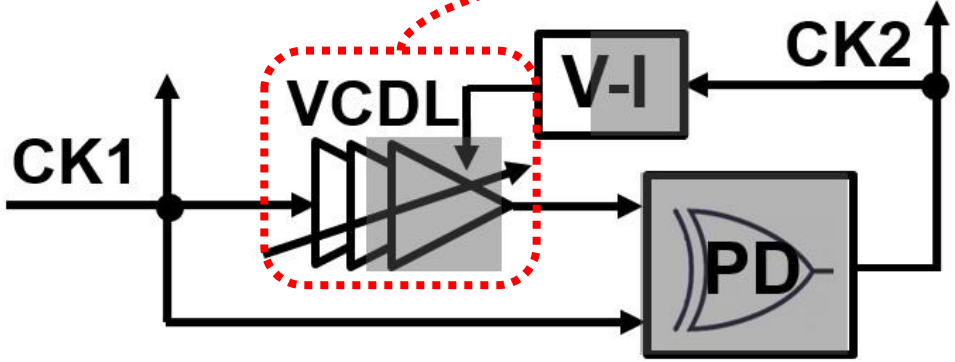
- $T_h = T_{cq}-T_d$ (5.7~9.5ps under PVT variation) is sufficient for the timing requirement

Outline

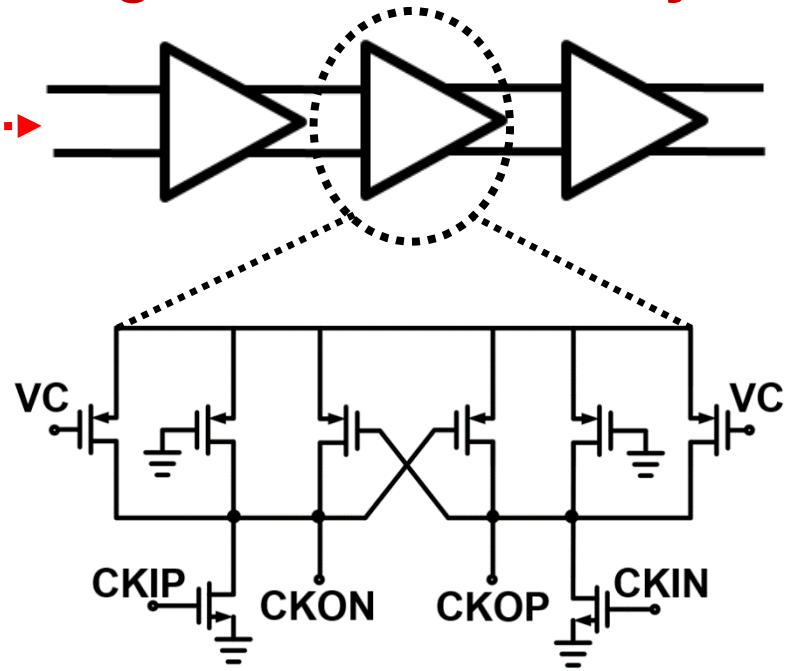
- Motivation
- Transmitter Architecture
- **Circuit Implementation**
- Measurement Results
- Conclusion

Divider-Less Clock Generation-VCDL

Divider-less clock generation



Voltage-controlled delay line



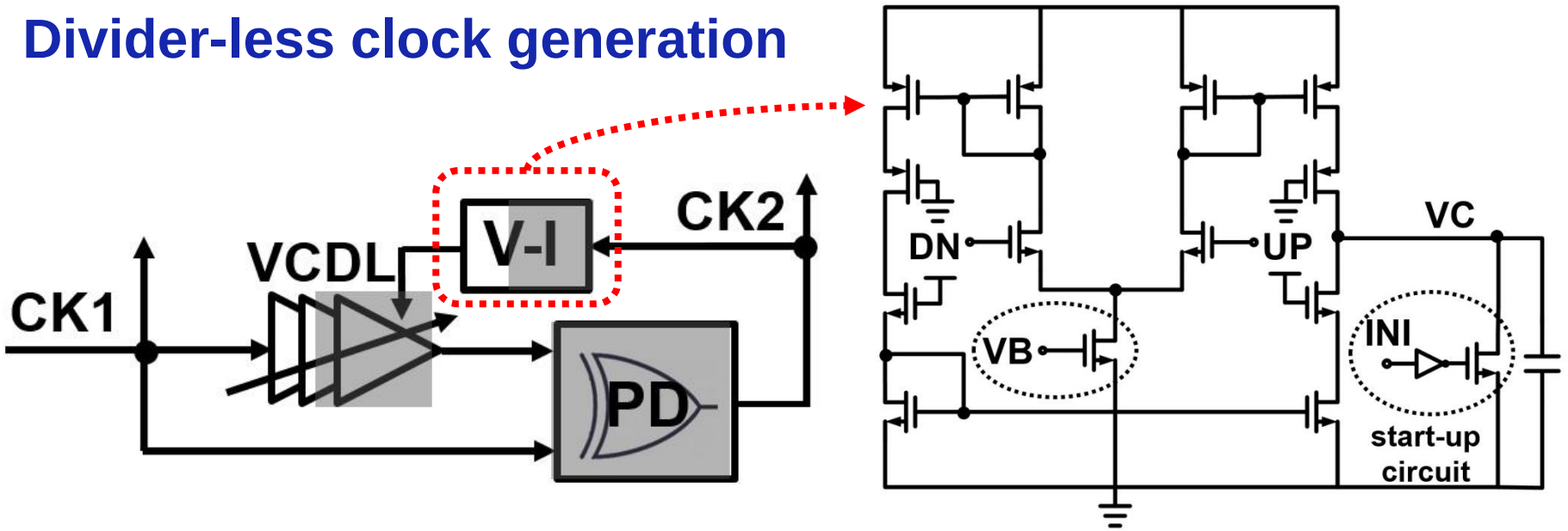
- **Cascading 3 delay cells**
- **Delay range: 28.6~77.2ps @5GHz (VC:0~1V)**
- **90° is the unique phase locked point**

Reference : [H. Y. Chang, TMTT 2014]

Divider-Less Clock Generation-V/I

Voltage-to-current converter

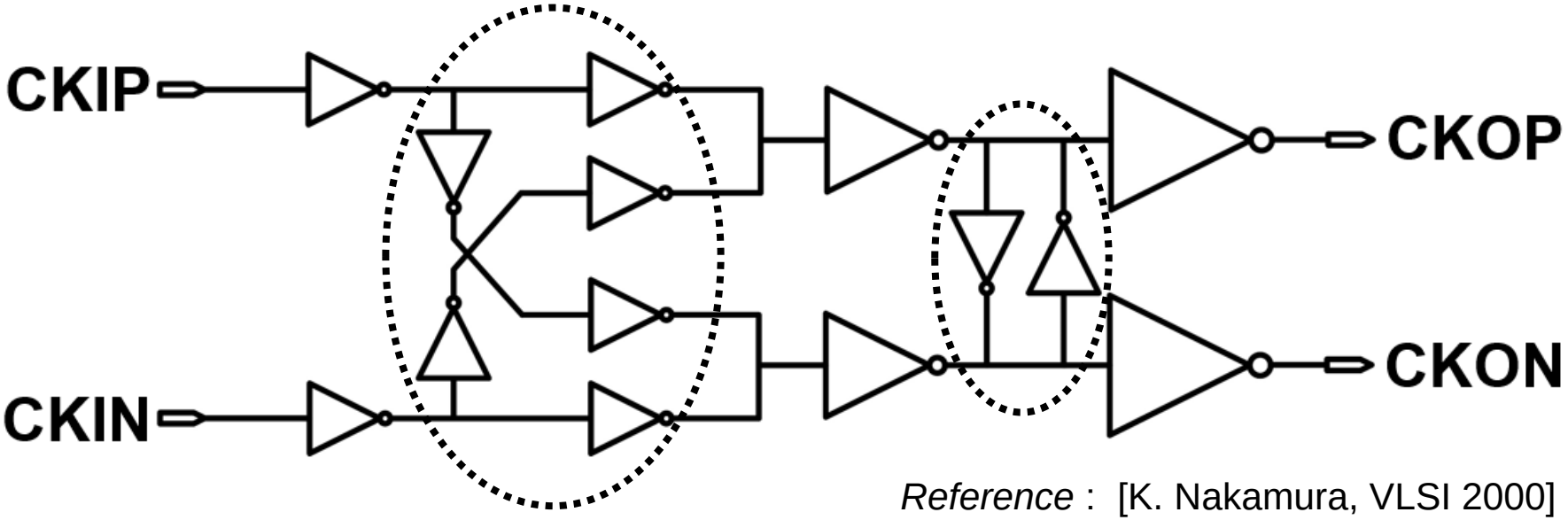
Divider-less clock generation



Reference : [Jri Lee, JSSC 2009]

- **The start-up circuit is used to set up the initial control voltage (VC) to 0V to avoid the false locking condition**
- **VB can be slightly calibrated through an off-chip DAC to solve the offset problem**

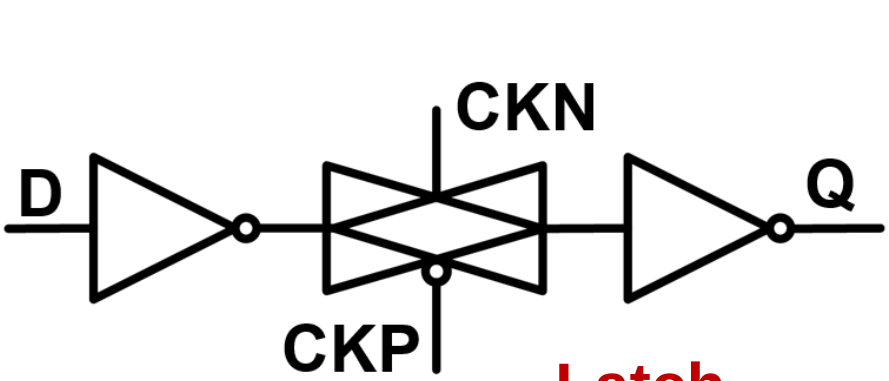
Duty-Cycle Corrector



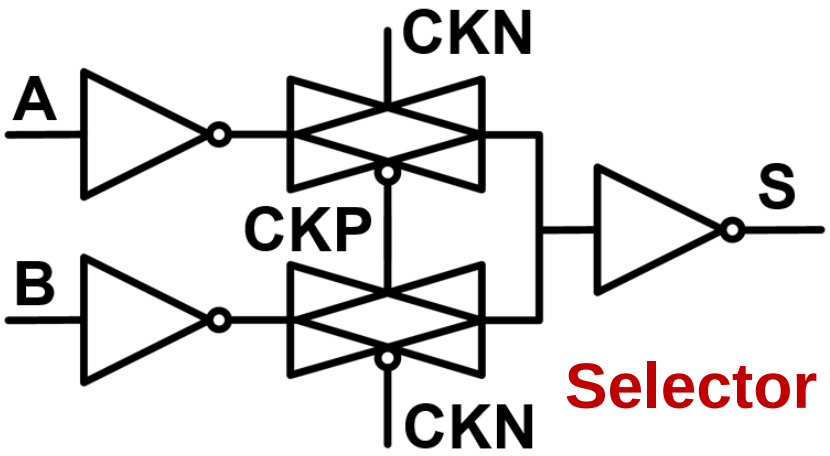
Reference : [K. Nakamura, VLSI 2000]

- **Complementary phase blending architecture to correct the clock signal's duty cycle**
- **4-stage CMOS inverter chain to guarantee the adequate drive capability**

CMOS Latch and Selector



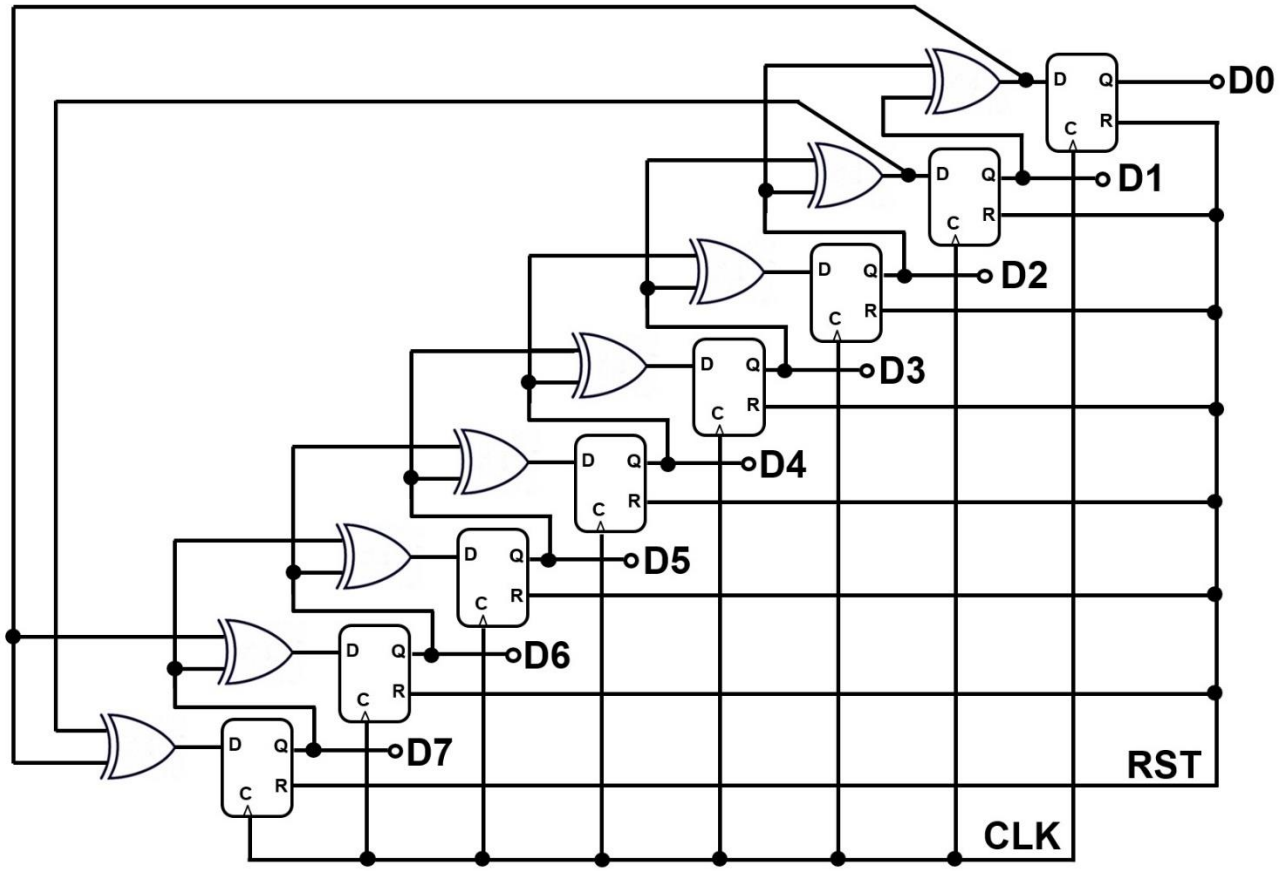
Latch



Selector

- Based on CMOS transmission-gate
- Dynamic structure is suitable for high data-rate
- No static power consumption

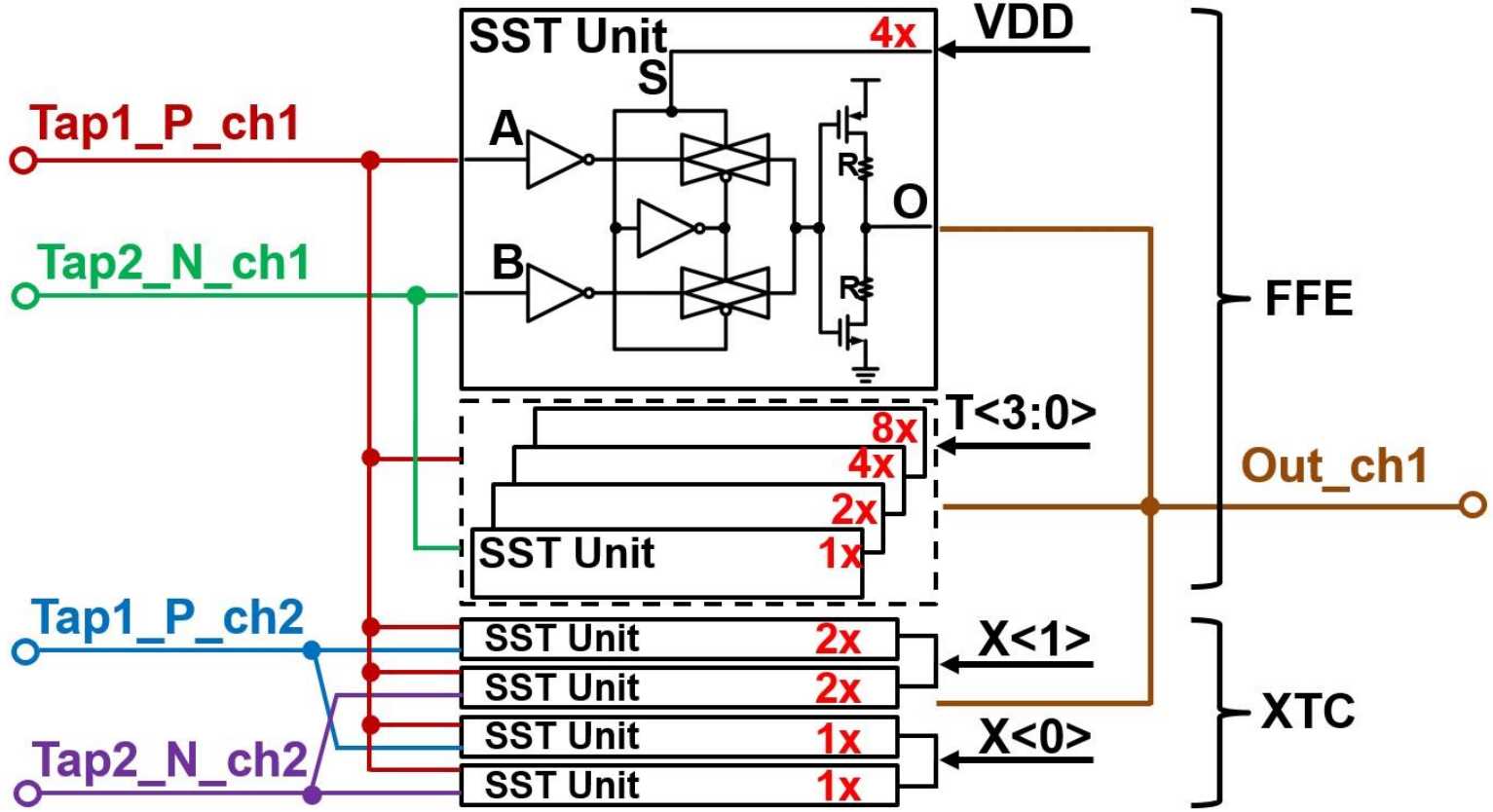
Parallel PRBS Generator



Reference : [E. Laskin, JSSC 2006]

- **CMOS XORs and CMOS transmission-gate DFFs**
- **8-lane PRBS-7 ⇨ TX output is still PRBS-7**

SST Driver with FFE and XTC

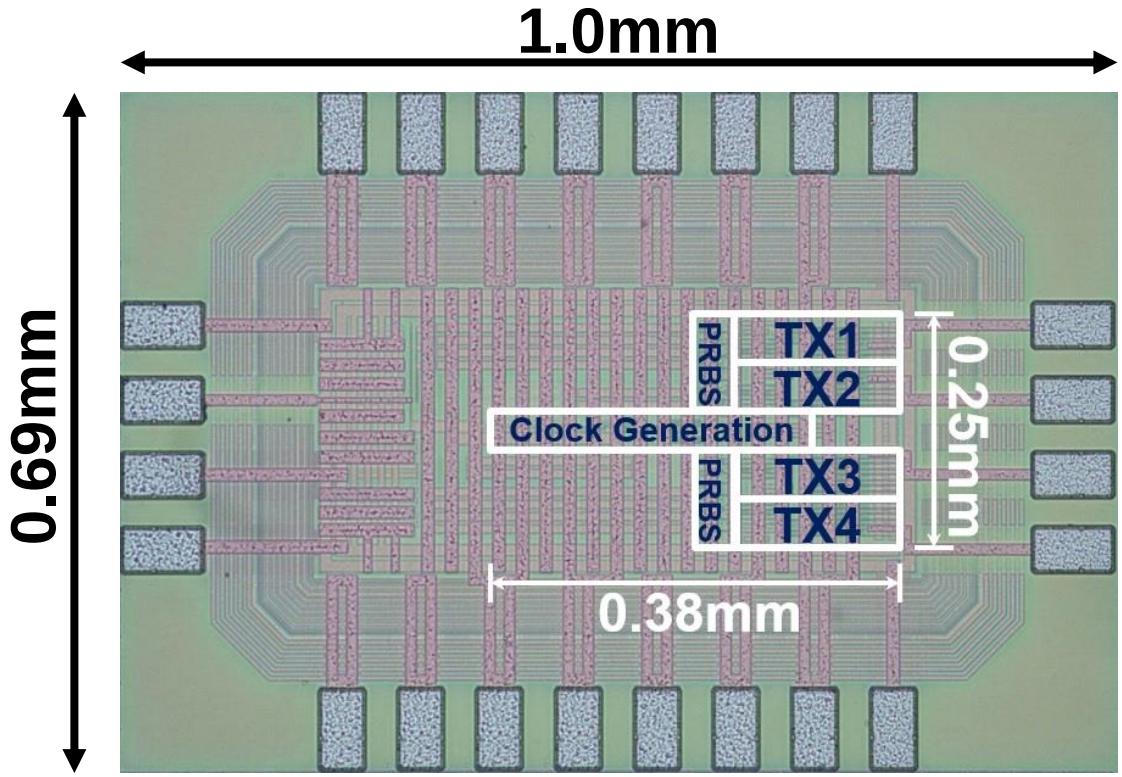


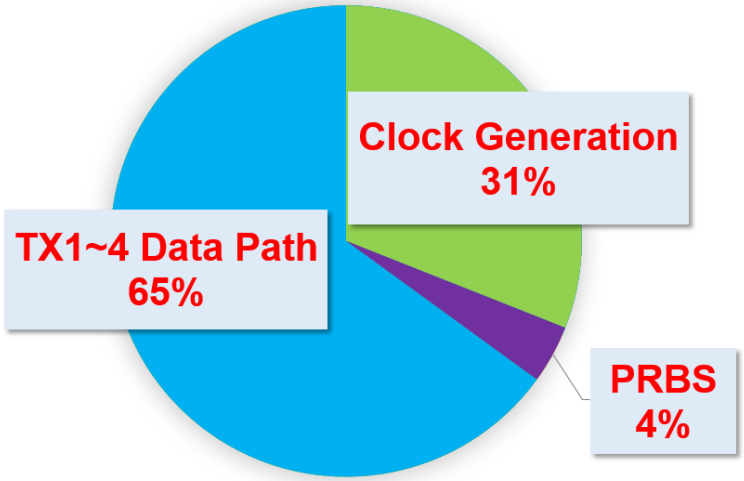
- 25 SST units in total to achieve the impedance of 50Ω
- T<3:0> for calibrating the FFE tap coefficient
- X<1:0> for calibrating the XTC coefficient

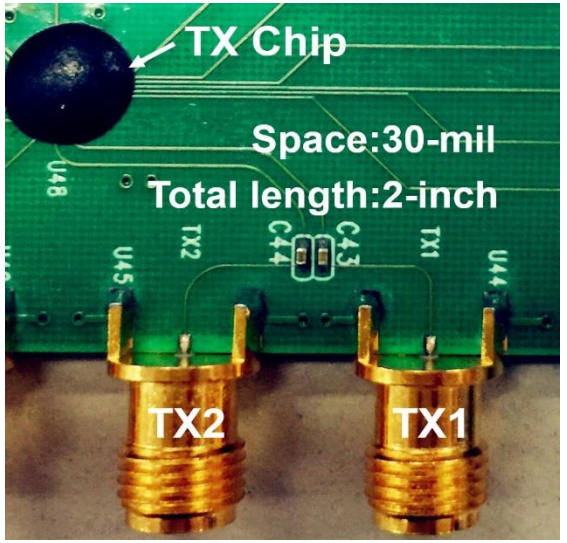
Outline

- Motivation
- Transmitter Architecture
- Circuit Implementation
- **Measurement Results**
- Conclusion

Die Photo, Power Breakdown and Testing Setup



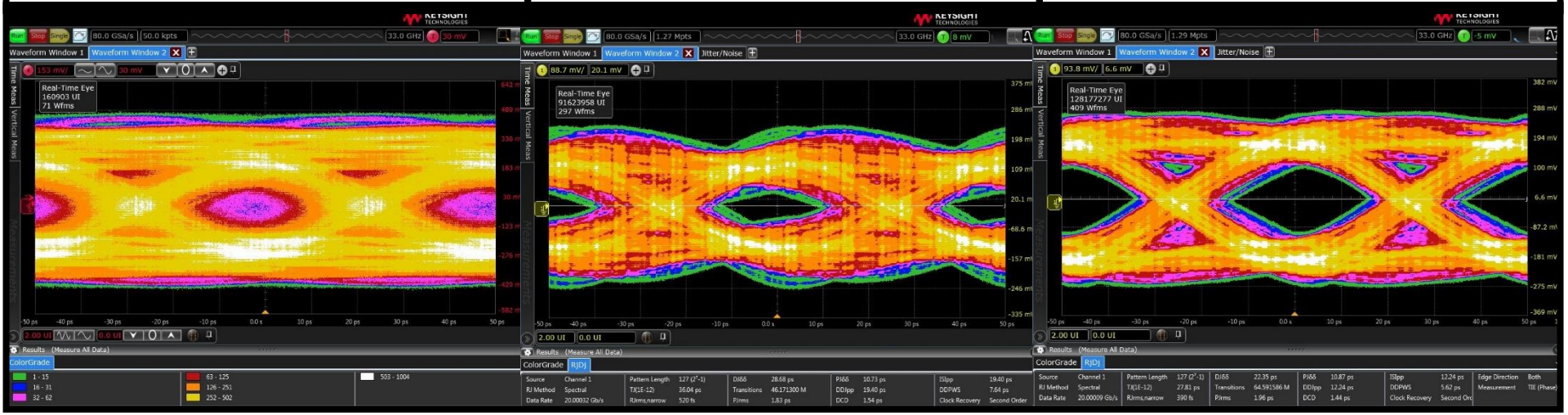




- TSMC 65nm CMOS technology
- Active area: 0.045mm^2
- Total power: 69mW

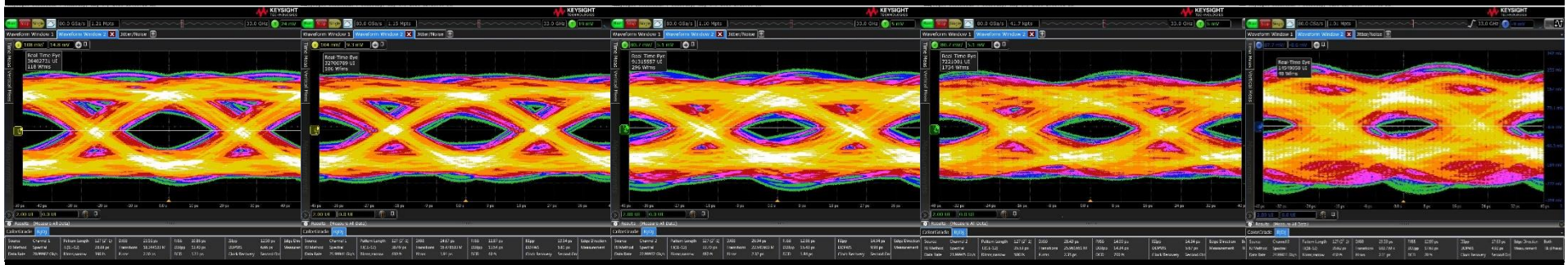
Measured Eye Diagrams

20Gb/s w/o FFE, w/o XTC	20Gb/s w/i FFE, w/o XTC	20Gb/s w/i FFE, w/i XTC



- PRBS 2^7-1 @20Gb/s
- Total jitter: 36ps ⇨27.8ps; DDJ: 19.4ps ⇨12.2ps
- Vertical eye opening (signle-ended): 180mV

Higher Data Rates ?

21Gb/s	22Gb/s	23Gb/s	24Gb/s	25Gb/s
				
TJ:29.0ps	TJ:30.5ps	TJ:33.7ps	TJ:35.5ps	TJ:35.6ps

- PRBS 2^7-1 @21~25Gb/s
- Higher data rates with smaller eye opening and worse jitter performance
- The proposed architecture is suitable for higher data-rate in advanced process nodes

Performance Comparison

Ref.	C. Menolfi ISSCC 2012	Y. H. Song ISSCC 2014	H. Wang JSSC 2010	This work
Data Rate (Gb/s)	28	16	20	20
Technology	32nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Equalization	FFE	FFE	FFE	FFE+XTC
Driver	SST	SST	CML	SST
Total Jitter (ps)	7.7	29	/	27.8
BER	/	/	10^{-12}	10^{-12}
TX Swing (mV)	160	55	100	180
Power Supply (V)	1.1	1	1.2	1.2
Power Efficiency (pJ/bit)	7.75	1.05	2.25	0.86

Outline

- Motivation
- Transmitter Architecture
- Circuit Implementation
- Measurement Results
- **Conclusion**

Conclusion

- A 4×20Gb/s serial link transmitter is presented in 65nm CMOS technology
- The proposed transmitter architecture with divider-less clock generation can save a lot of hardware cost and power compared with the conventional designs
- The FFE and XTC are merged together with SST driver
- The transmitter achieves a total power efficiency of 0.86pJ/b/lane at the data-rate of 20Gb/s
- The proposed architecture is suitable for higher data-rate applications in advanced process nodes

Acknowledgements

- This work is supported by the National Natural Science Foundation of China, No. 61371011 and Funding No. JCYJ20130401173716277.

- Special thanks to Keysight open lab in Beijing for testing assistance.