A 4.6mW, 22dBm IIP3 all MOSCAP Based 34-314MHz Tunable Continuous Time Filter in 65nm

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Outline

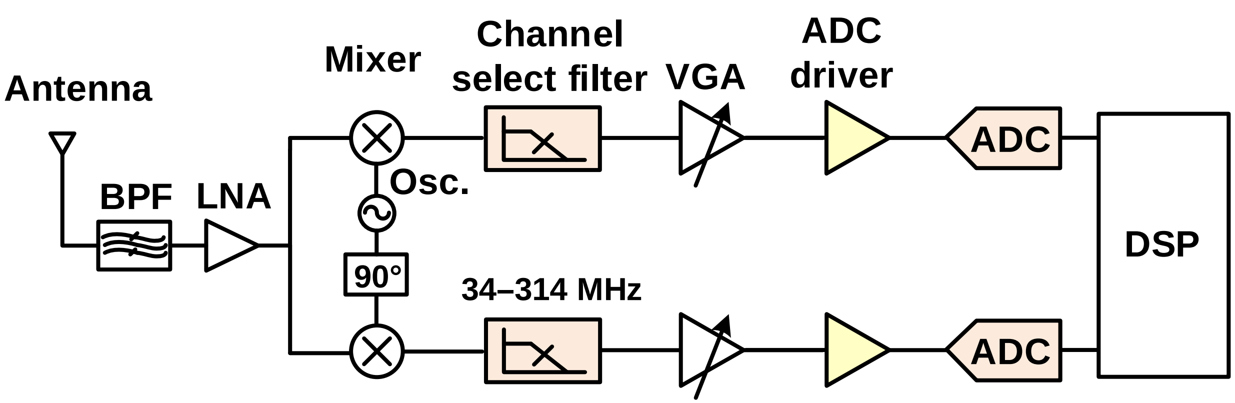
- Motivation
- Low Pass Filter Architectures
- Use of MOSCAP
- Non-Linearity Cancellation
- Self Compensation
- Use of Inverters
- Measurement Results
- Conclusion

Motivation

Portable devices

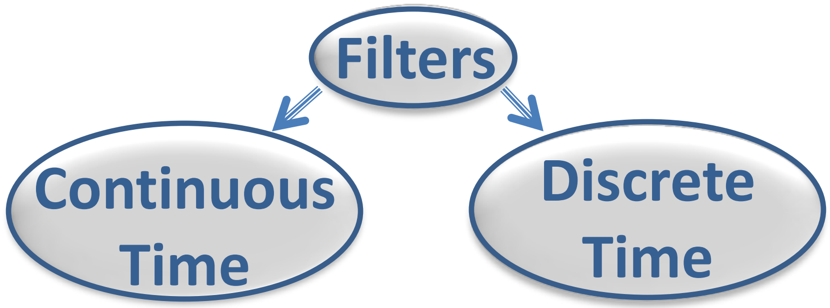
Multiple Radios

CDMA, GSM. UMTS, LTE
Wi-Fi (802.11), Bluetooth
HSPA (850,900,1700/2100)



- Each radio uses multiple channels
- Channel select filter is used to select channel of interest

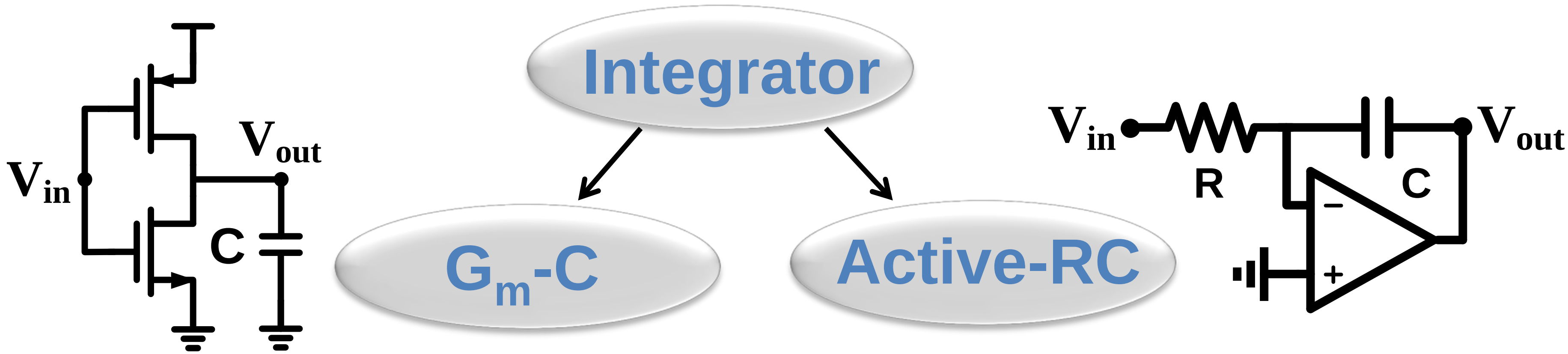
Motivation (II)



Difficult to tune	Easily tunable
Does not require additional filter	Requires CT anti-alias filter
Low power	Medium power
Fc varies with PVT	Fc is PVT tolerant

- **Need low-power, linear tunable continuous time filters**
- **Integrators are key part of filters**
  - Design of high swing integrators is difficult in lower tech.
- **Challenges**
  - Filter specs becoming more stringent

Motivation (III)

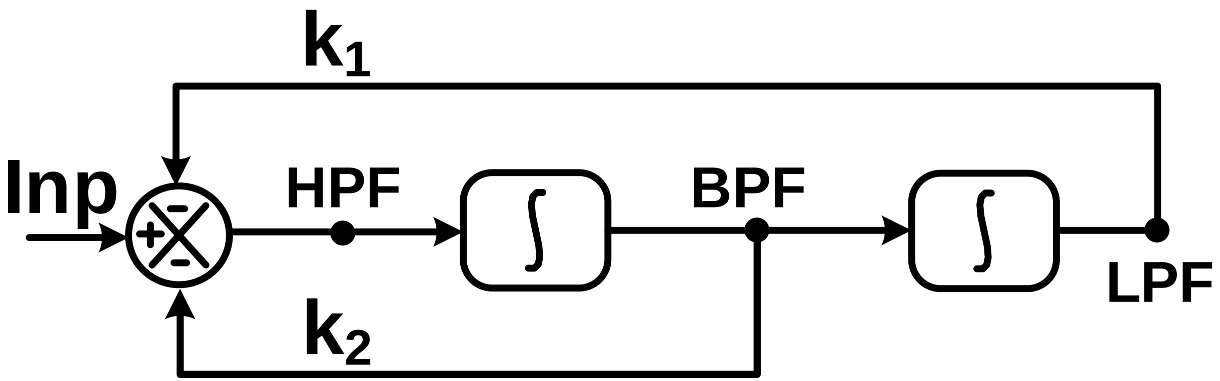


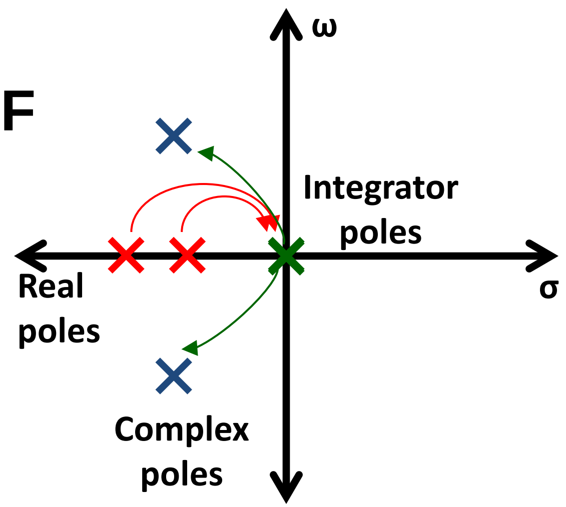
	G_m-C	Active-RC
Linearity	★★	★★★★
Input swing	★★	★★★★
Noise	★★	★★★
Speed	★★★★	★★
Tunability	★★★★	★★

Focus

Active Filter Design

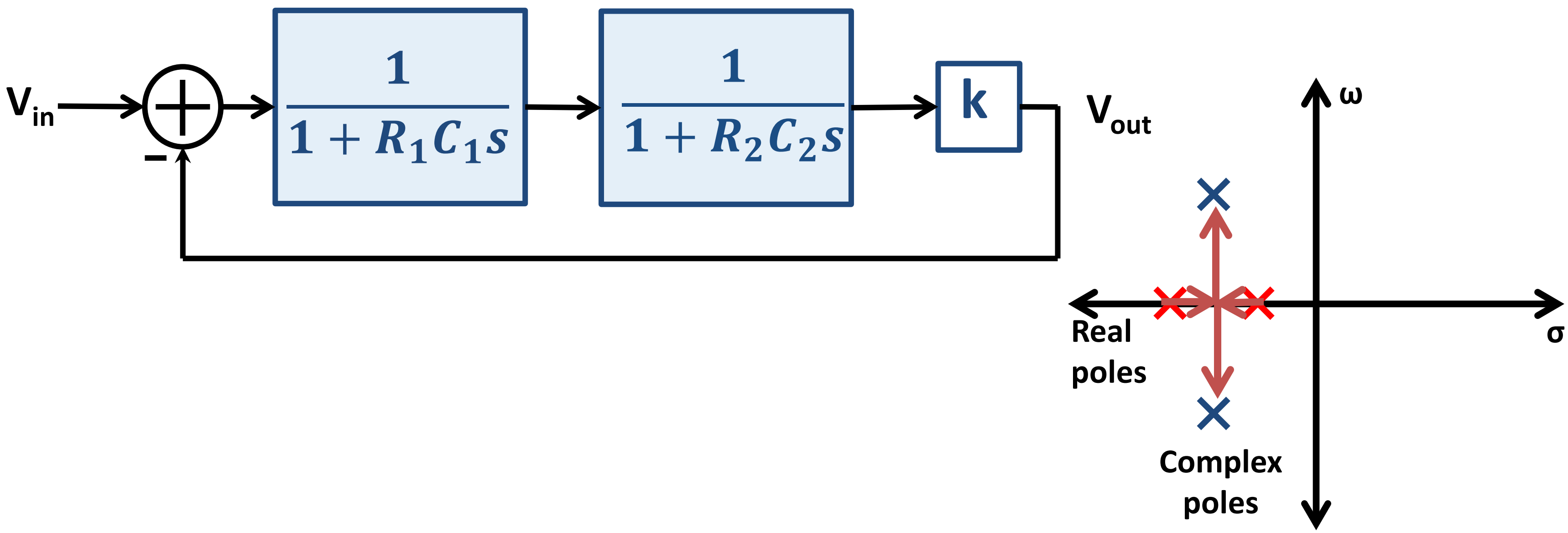
- **Traditional design (Integrator based approach)**
  - Poles are moved from origin to complex plane
  - Filtering is done in voltage mode
  - Integrators are realized using OTAs in neg. feedback



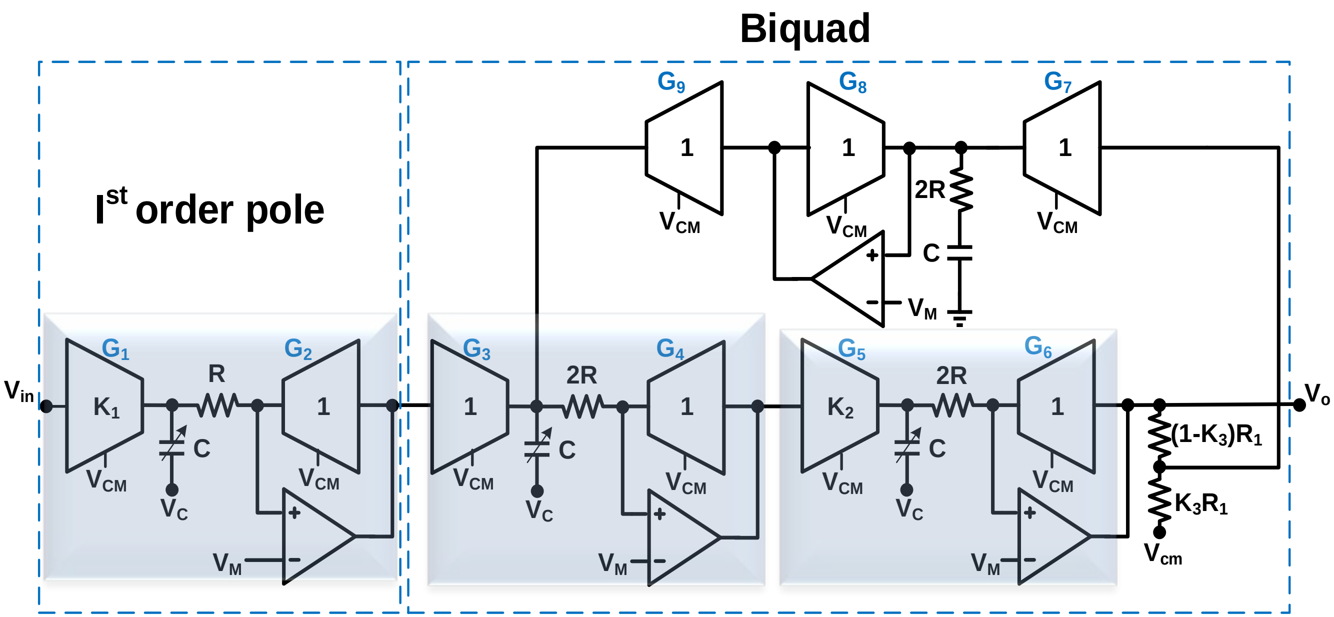


Active Filter Design

- **Real low pass filter approach**
  - Real poles are moved to complex plane using neg. fb
  - Filtering is done in current mode
  - Low pass filters are realized using passives
  - Lower number of low impedance nodes (Lower noise)



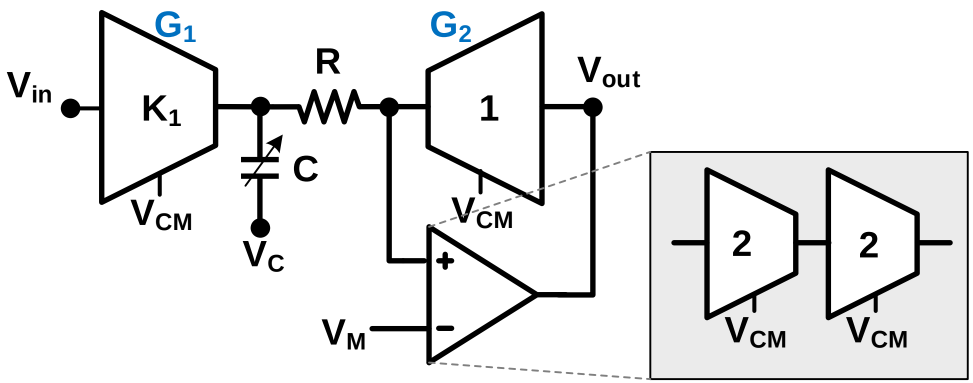
Channel Select Filter (Block diagram)



Single ended shown for simplicity
Actual implementation is **differential**

- **Cascade of first order pole and biquad**
- **First order pole**
  - Realized in current domain using gm cells and passives
  - Ratio of gm cells gives gain

Low Pass Filter Design

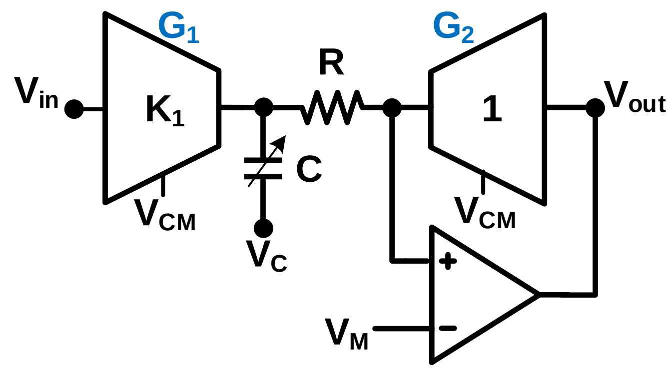


VM metastable voltage of SCCB inverters

- **Desired**
  - High input impedance and low output impedance
  - Tunable cut off frequency
- **G_1, G_2 are gm cells (Biased inverters)**
- **G_1 converts input voltage to current**
- **G_2 with neg. fb converts low pass current to voltage**
- **Ratio of Gm cells provides gain**

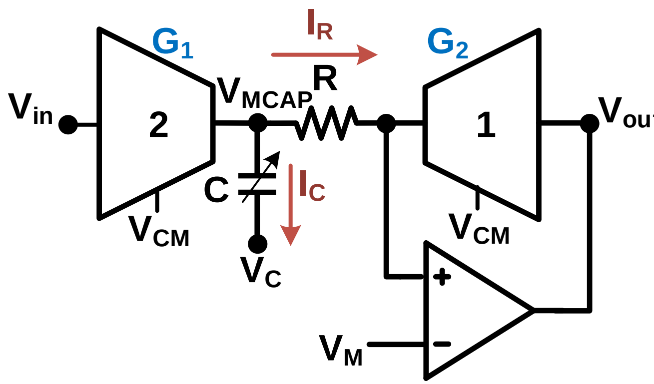
Gm Non Linearity Cancellation: Low freq

- **Assume Gm nonlinearity**
  - $G_m(x) = a_0 + a_1 x + a_2 x^2 + a_3 x^3$



- **All in band signal current is converted back to voltage**
- **$G_1(V_{in}) = G_2(V_{out})$**
- **In fully differential implementation**
  - $V_{out} = K_1 V_{in} + \frac{a_3}{a_1}(K_1 - K_1^3) V_{in}^3$
- $\mathbf{IIP3} = \sqrt{\frac{4}{3(1-K_1^2)} \frac{a_1}{a_3}}$

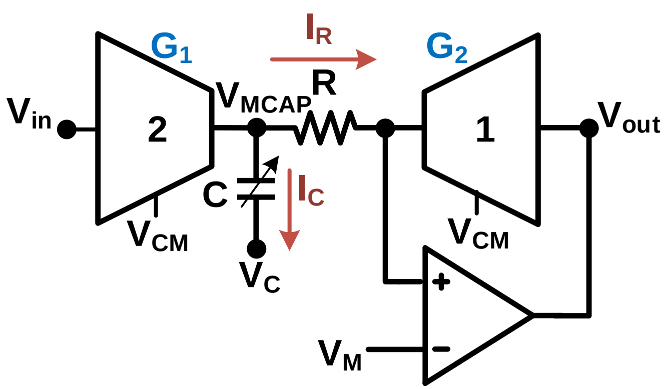
Non Linearity Cancellation: High freq

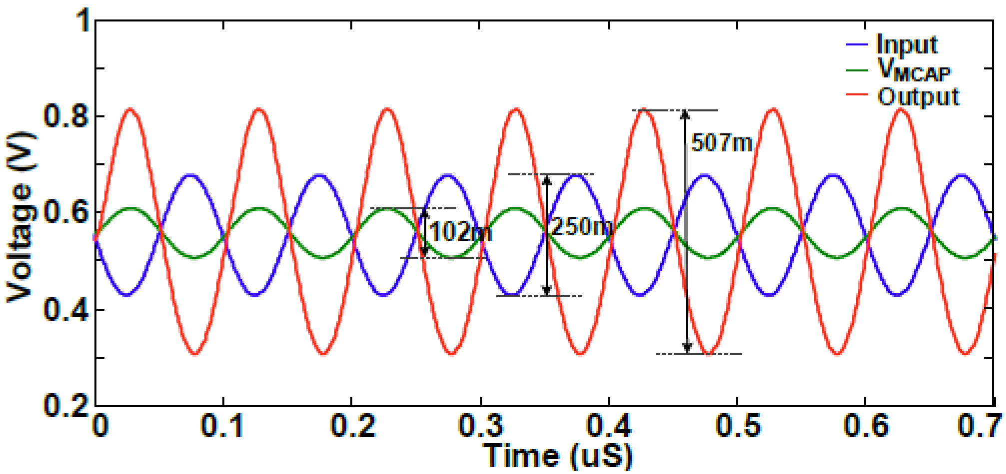


- **Assume Gm nonlinearity**
  - $G_m(x) = a_0 + a_1x + a_2x^2 + a_3x^3$
  - $G_1(V_{in}) = I_R + I_c$
- **Most of signal current is filtered**
- **$I_R = G_2(V_{out})$**
- **Unfiltered high frequency components**
  - Appear at the output
  - Filtered by subsequent stages

Use of MOSCAP

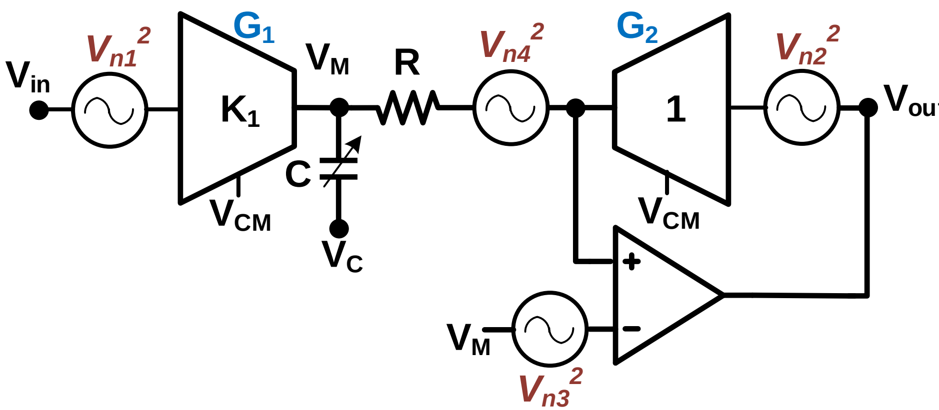
- **Lower resistor (R) and higher capacitor (C)**
  - Reduces swing at V_{MCAP}
  - Use of high density MOSCAPS as filter capacitors
  - Continuously tunable cut off frequency
  - Helps in compensation





Reduction of swing from 0.5V to 0.1V reduces IM_3 by 40dB

Noise Analysis

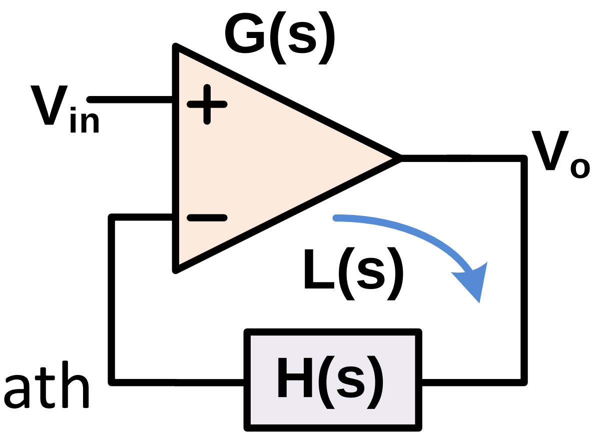


Dominant noise

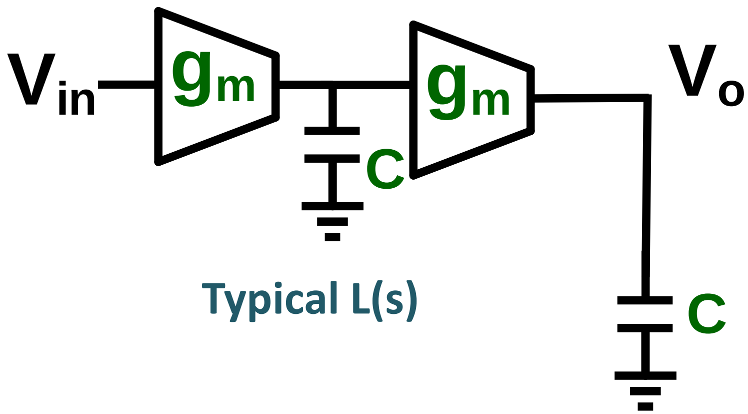
- $$V_{out}^2 = \boxed{\frac{K_1^2}{1+(RC\omega)^2} V_{n1}^2 + V_{n2}^2} + \frac{(\omega C)^2}{1+(RC\omega)^2}(V_{n3}^2 + V_{n4}^2)$$
- **Noise of OTA and resistor are high pass filtered**
- **Noise of the Gm cells appear at the output**
- **The resistor doesn't load negative feedback network**
  - Low R and higher C is used for low swing at V_M

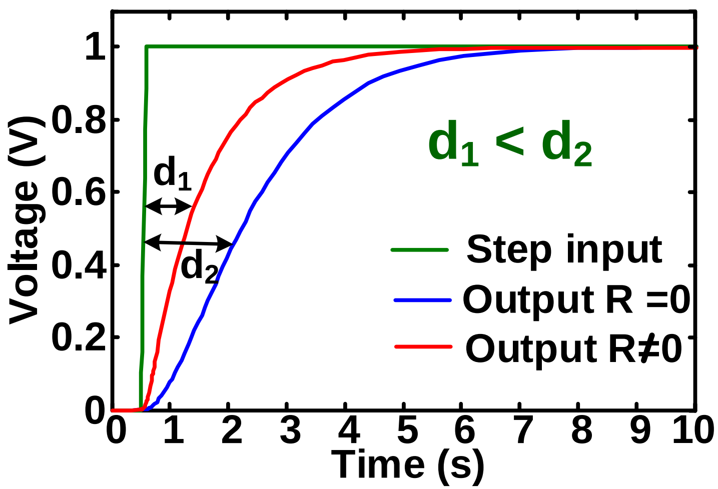
Self Compensation

- **Excess loop delay → Instability**



- **Compensation**
  - Reduce the delay, Provide the fast path
- **Resistor converts current to voltage indep. of freq**
  - Reduce the delay between Vin and Vout





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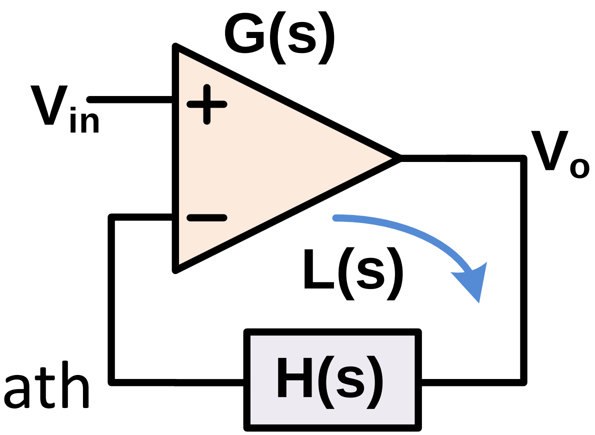
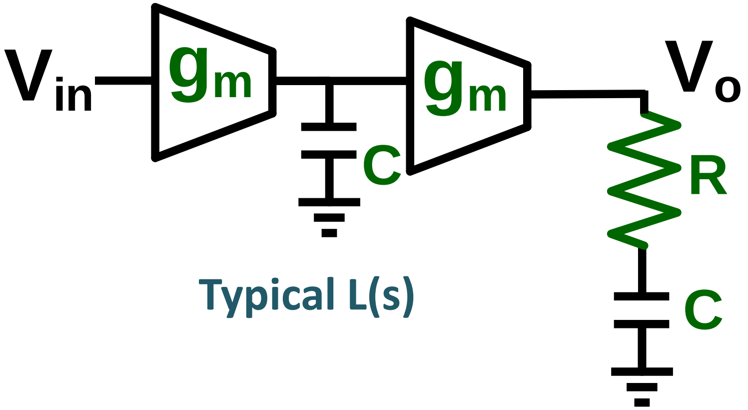
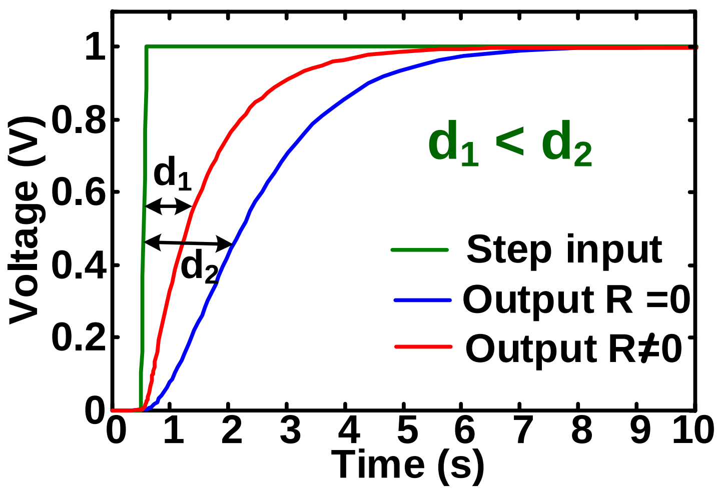
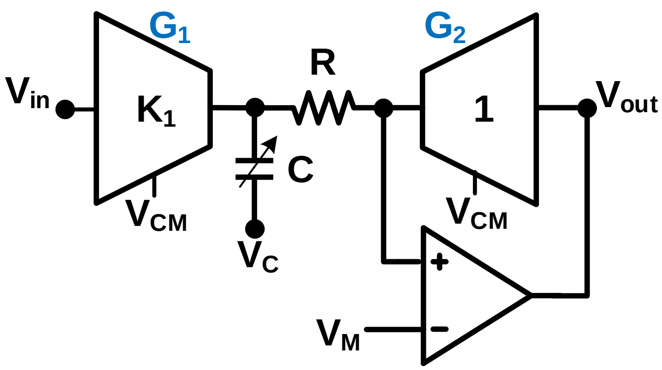




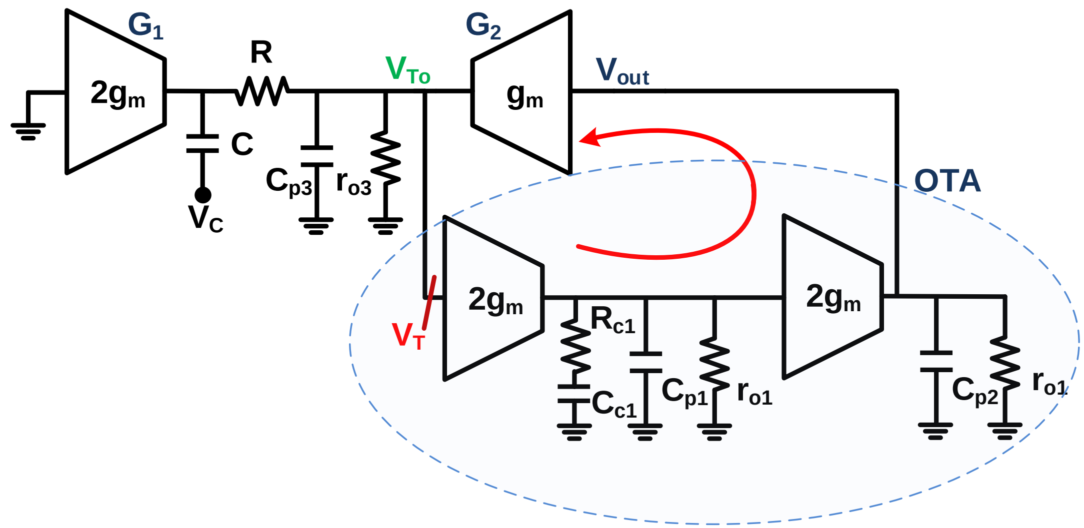
Typical L(s)



Self Compensation

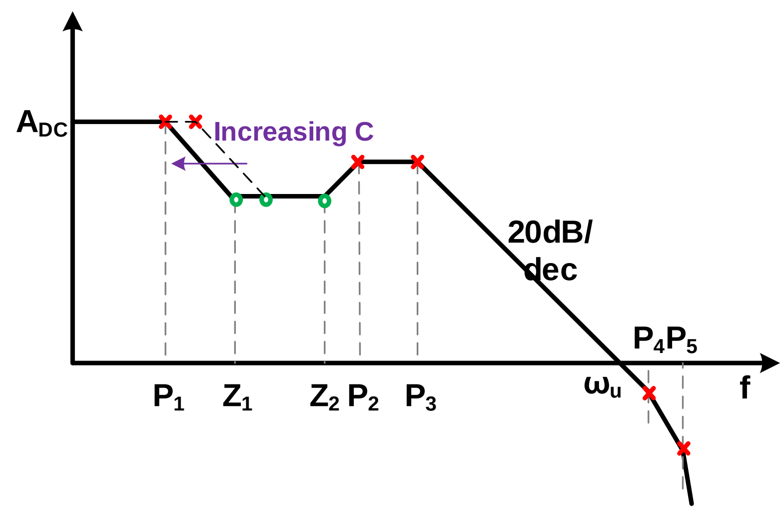


First order system



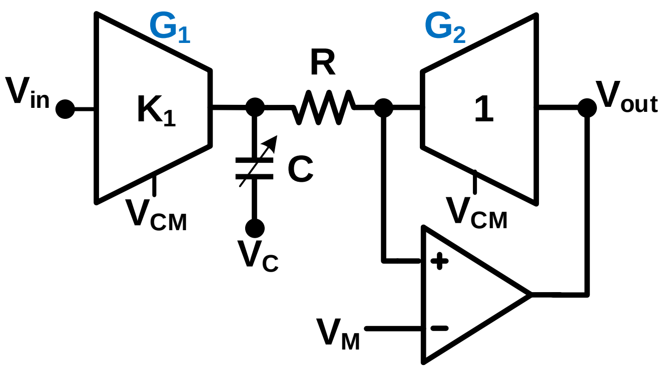
First order system with parasitics

- $Z_1 = -\dfrac{1}{RC}$, $\quad Z_2 = -\dfrac{1}{R_{C1}C_{C1}}$
- $P_1 = -\dfrac{1}{r_{03}C}$, $\quad P_2 = -\dfrac{1}{r_{o1}(C_{p1}+C_{C1})}$
- $P_3 = -\dfrac{1}{r_{01}C_{p2}}$, $\quad P_4 = -\dfrac{1}{R_{c1}C_{p1}}$
- $P_5 = -\dfrac{1}{RC_{p3}}$, $\quad \omega_u = -\dfrac{A_{DC}}{r_{o1}C_{p2}}$



(Independent of tuning capacitor)

Self Compensation



First order system

- **Compensation**
  - Load compensates the loop
  - Increases freq. response of loop
  - Tracks with tuning capacitor
  - ω_u independent of tuning

- $Z_1 = -\frac{1}{RC}$, $Z_2 = -\frac{1}{R_{C1}C_{C1}}$
- $P_1 = -\frac{1}{r_{03}C}$, $P_2 = -\frac{1}{r_{o1}(C_{p1}+C_{C1})}$
- $P_3 = -\frac{1}{r_{01}C_{p2}}$, $P_4 = -\frac{1}{R_{c1}C_{p1}}$
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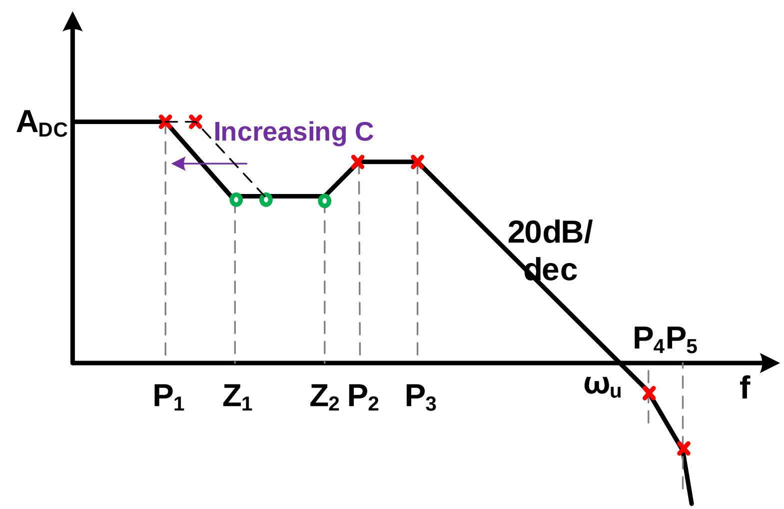
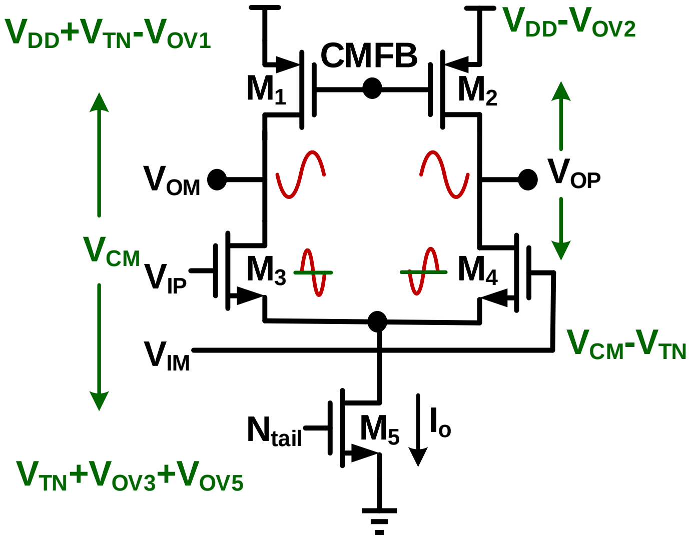
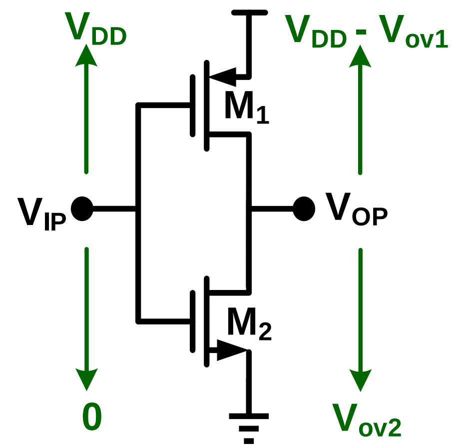
(Independent of tuning capacitor)



Design of Gm cells



Traditional differential pair



Inverters

Swing limited by input V_{CM}	Swing limited by output
Current biasing	Voltage biasing
Gm is less PVT tolerant	Gm is PVT tolerant
Excess noise factor >1	Excess noise factor = 1

Traditional OTA vs Inverter OTA (Swing)

- **Traditional OTA** → $Vo_{\max} = Vdd - \Delta V$
  - Vo_{max} limited by output
  - Vin_{min} limited by input

$$Vin_{\min} = 2\Delta V + V_{TN}'$$

$$Vpp_{OTA} = Vdd - 3\Delta V - V_{TN}'$$

- **Inverter** → $Vo_{\max} = Vdd - \Delta V_{INV}$
  - Vo_{max} limited by output
  - Vo_{min} limited by output

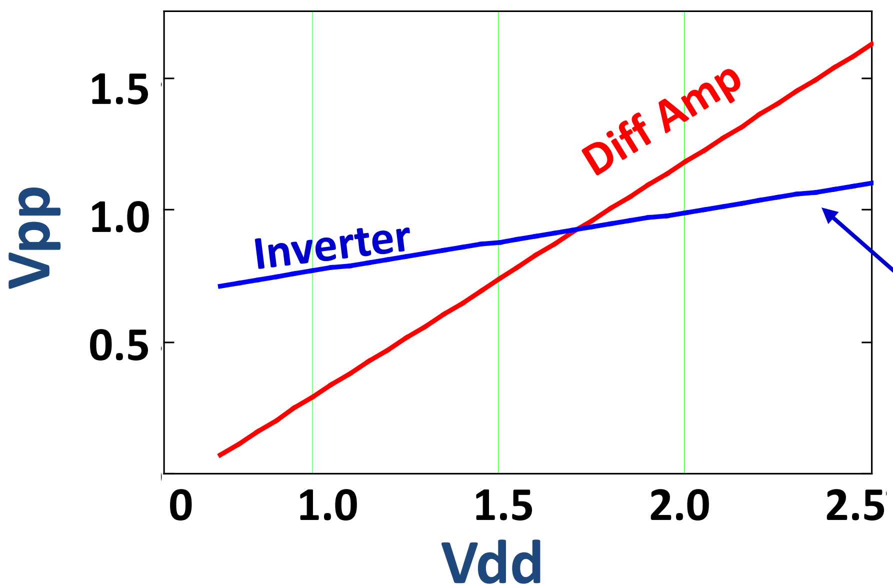
$$Vo_{\min} = \Delta V_{INV}$$

$$Vpp_{INV} = Vdd - 2\Delta V_{INV}$$

$$Vdd = V_{TN} + |V_{TP}| + 2\Delta V_{INV}$$

$$\Delta V_{INV} = \frac{Vdd - V_{TN} - |V_{TP}|}{2}$$

$$Vpp_{INV} = V_{TN} + |V_{TP}|$$

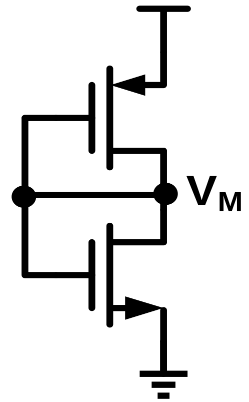


V_T scales slightly with VDD

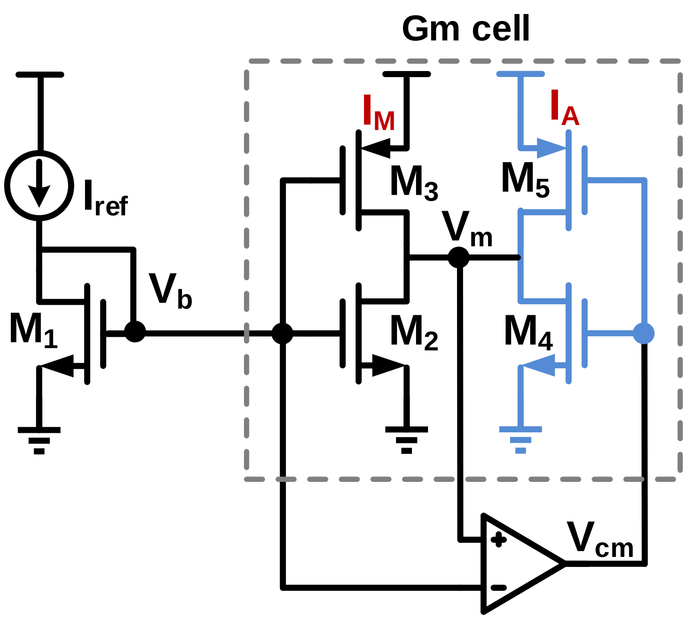
ΔV = 125mV, V_{TN} = 0.383V, V_{TP} = 0.55V

Semi Constant Current Biasing (SCCB)

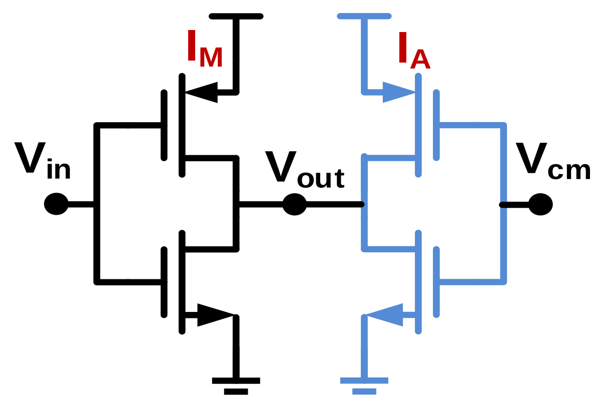
- **Bias voltage (V_b) is derived from NMOS current**
  - NMOS current is constant
- **Input and output voltages are made equal**
  - Auxiliary inverter with negative feedback
  - Overall variation in gm is small



Metastable biasing



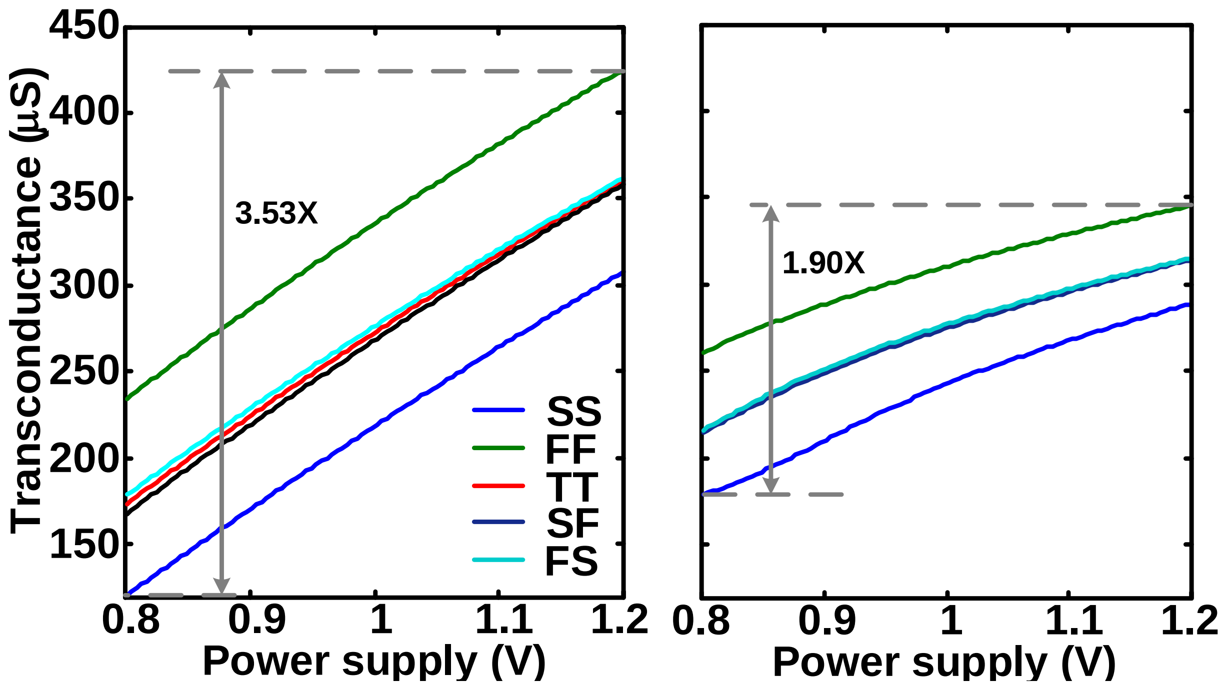
Replica bias network



Use of SCCB biased inverters

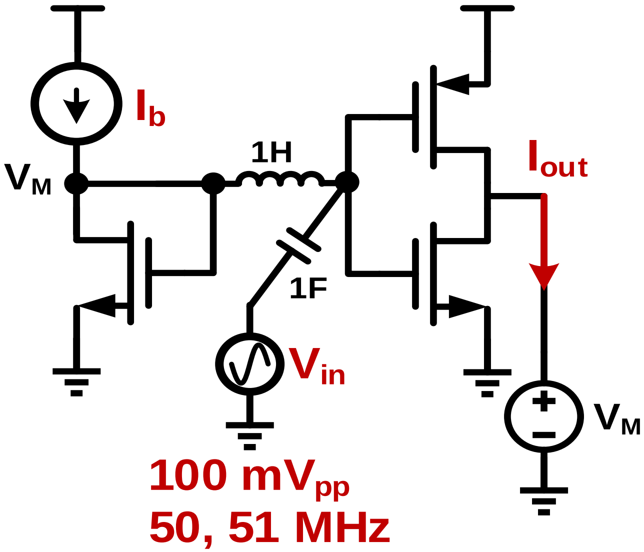
SCCB: Simulation Results

- **Variation in gm is reduced by 50%**
- **NMOS/PMOS current can be selected for best linearity**
- **Auxiliary inverter loads the main inverter**
  - Reduces the output impedance/ gain of amplifier

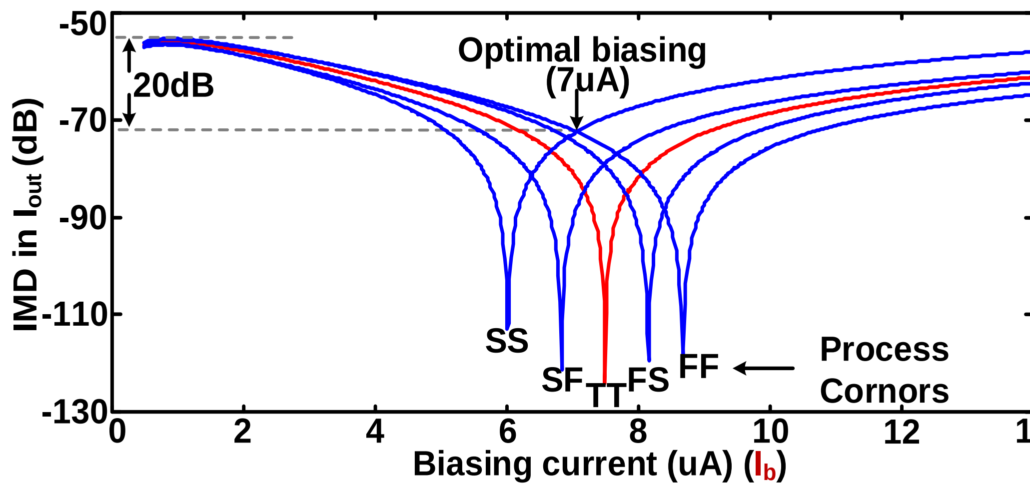


Traditional metastable biasing SCCB biasing

SCCB: Linearity



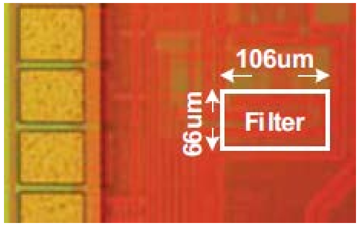
Simulation setup

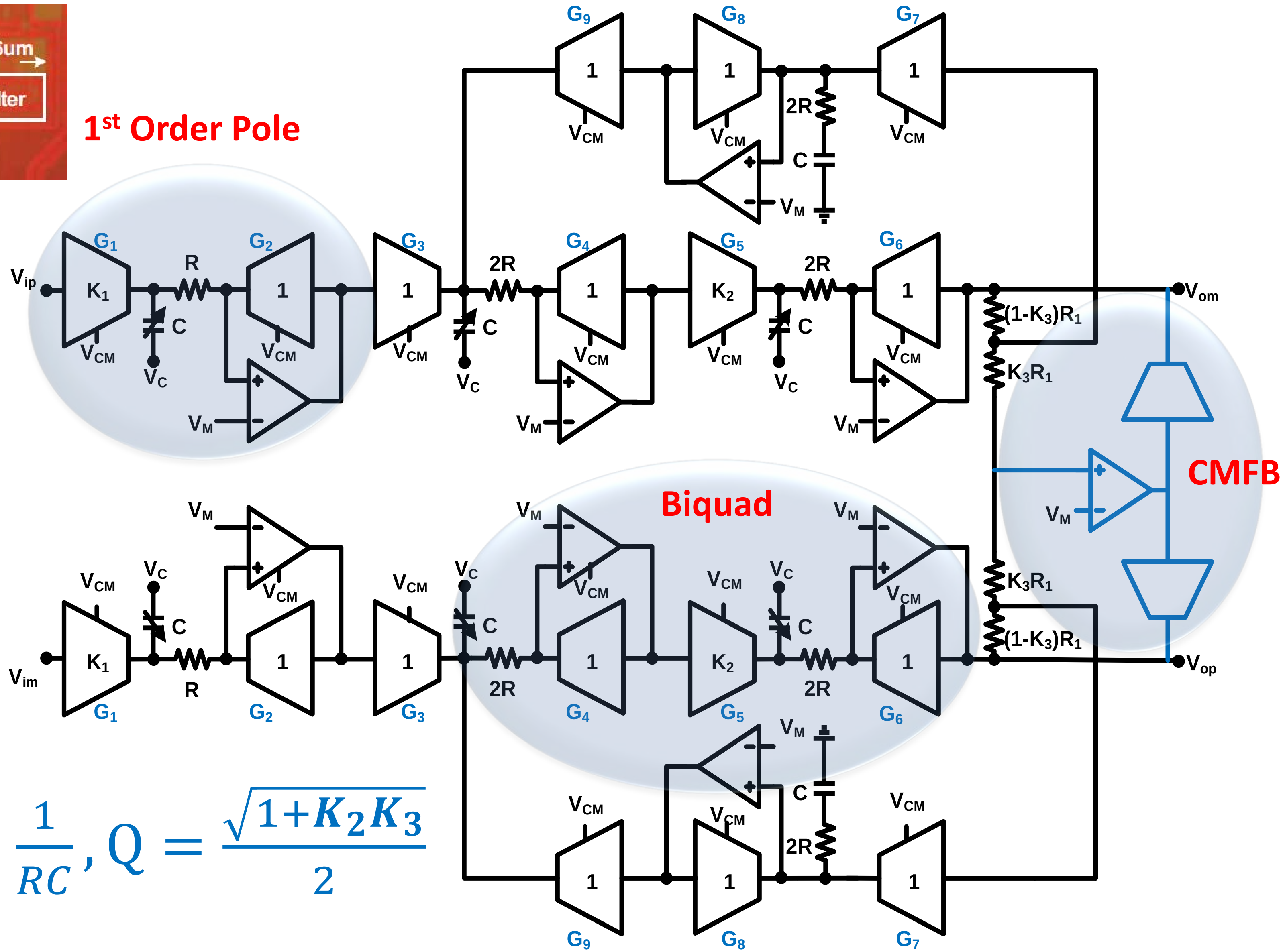


Simulation of IMD in I_{out}

- **NMOS/PMOS current can be selected**
  - To increase inherent linearity of inverter
  - Optimal biasing results in 20 dB improvement in IMD
  - NMOS and PMOS harmonic terms cancel out

Third Order Channel Select Filter

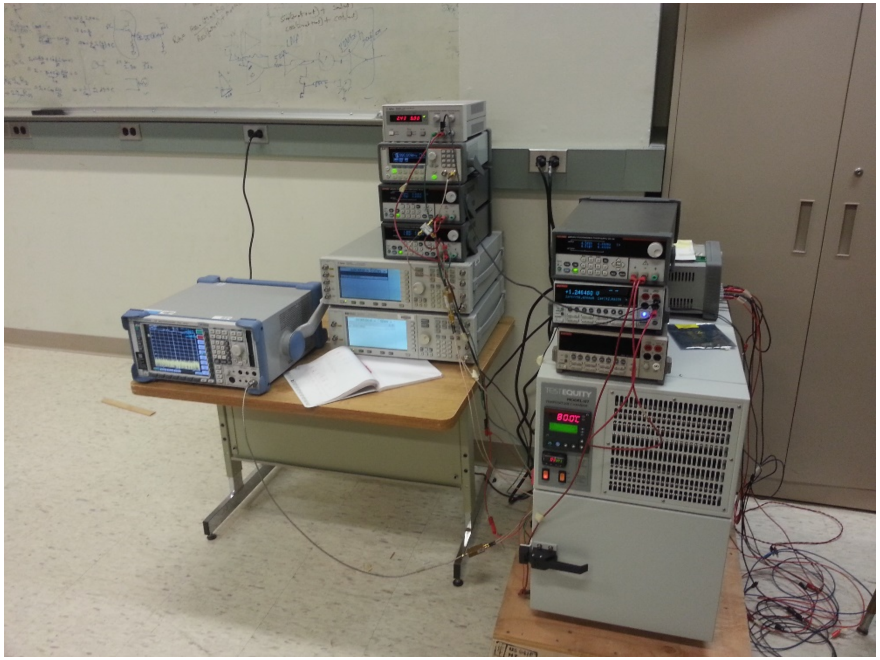


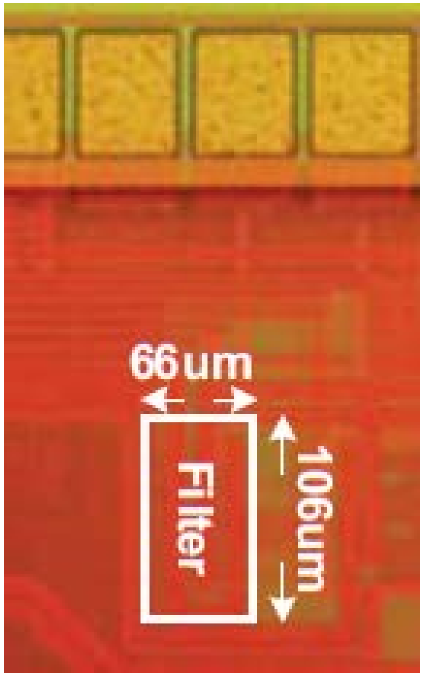


$$\omega_o = \frac{1}{RC}, \mathrm{Q} = \frac{\sqrt{1+K_2K_3}}{2}$$

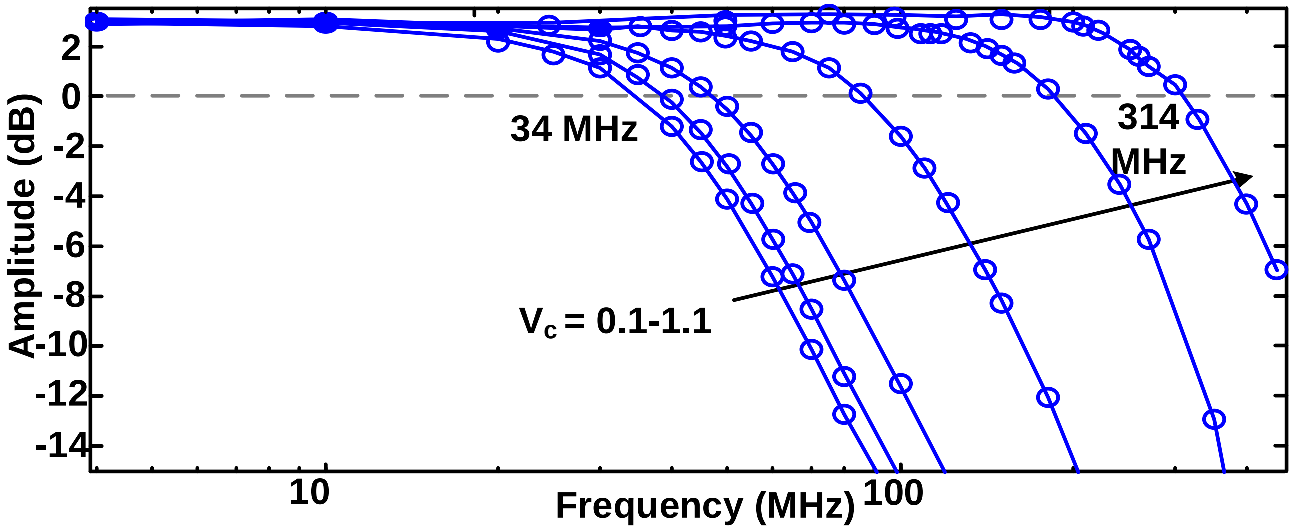
Measurement Results (I)

- **Prototype 3rd order filter**
  - Fabricated in TSMC 65nm GP process
  - Packaged in 5x5 QFN Package
  - Source follower is used to drive the 50 Ω interfaces
- **Area = 0.007mm^2**



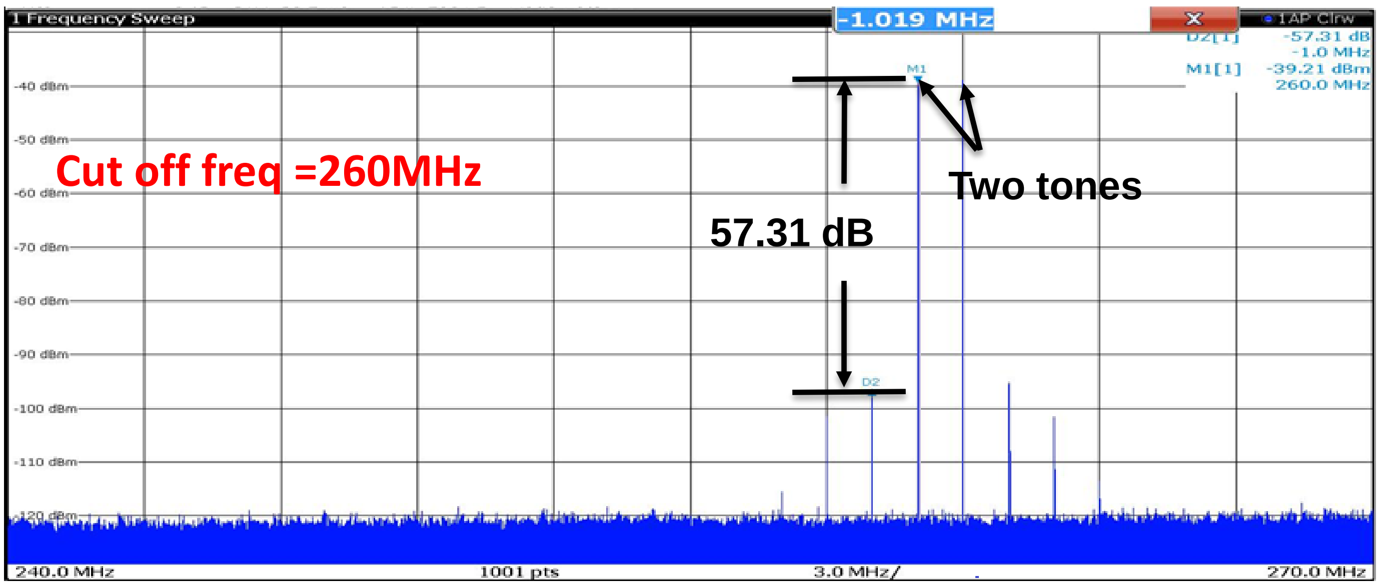


Measurement Results (II)



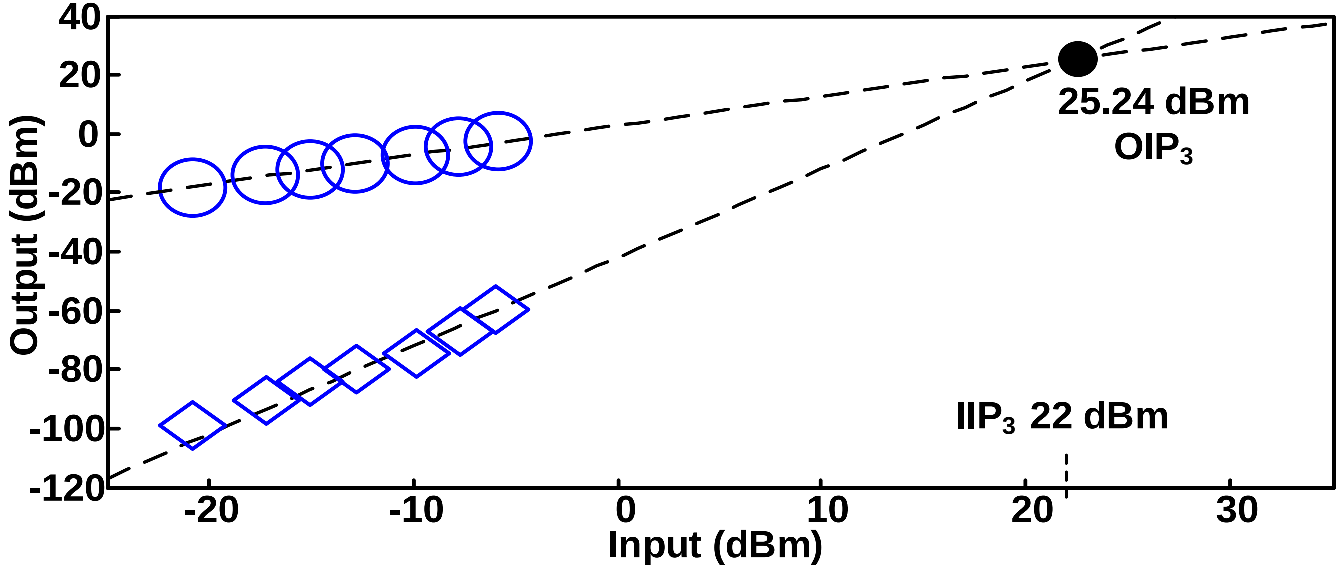
Output Swing 1Vpp

Measured magnitude response (cut off frequency tunable from 34 -314MHz)

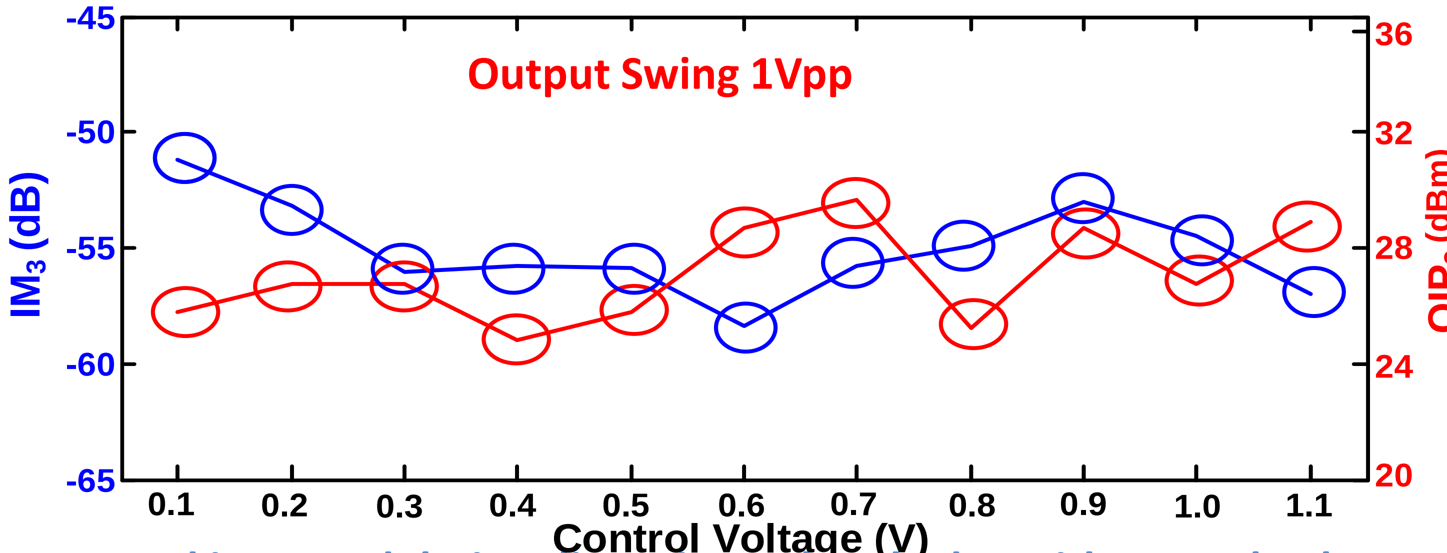


Measured IM_3 at 260MHz with Vc = 1.1V

Measurement Results (III)

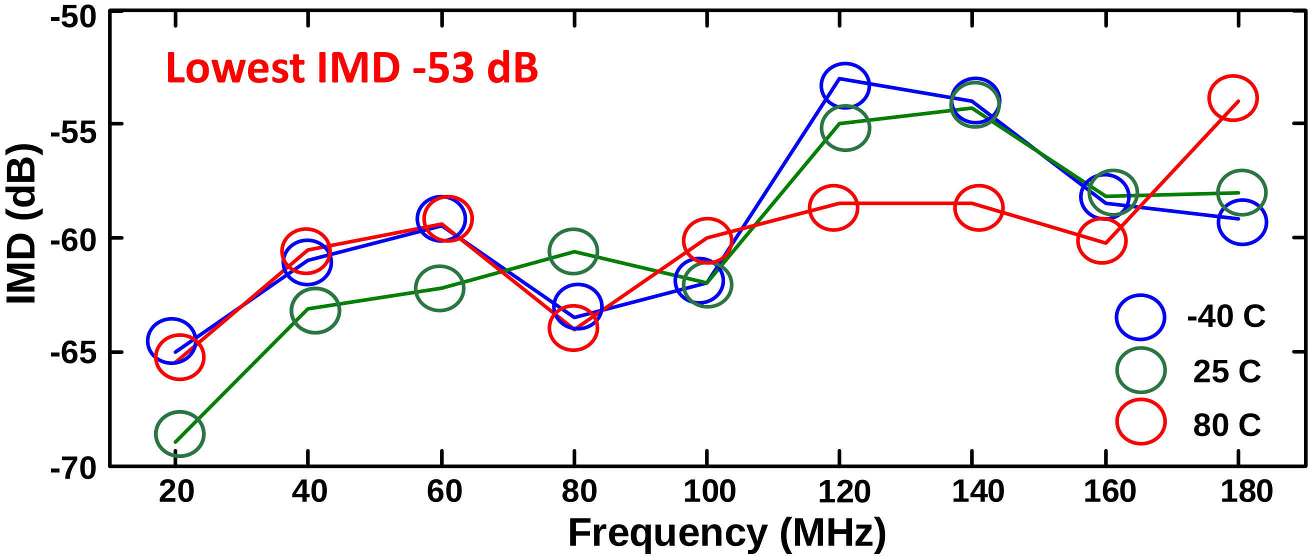


Measured IIP3 at 260MHz of the proposed filter



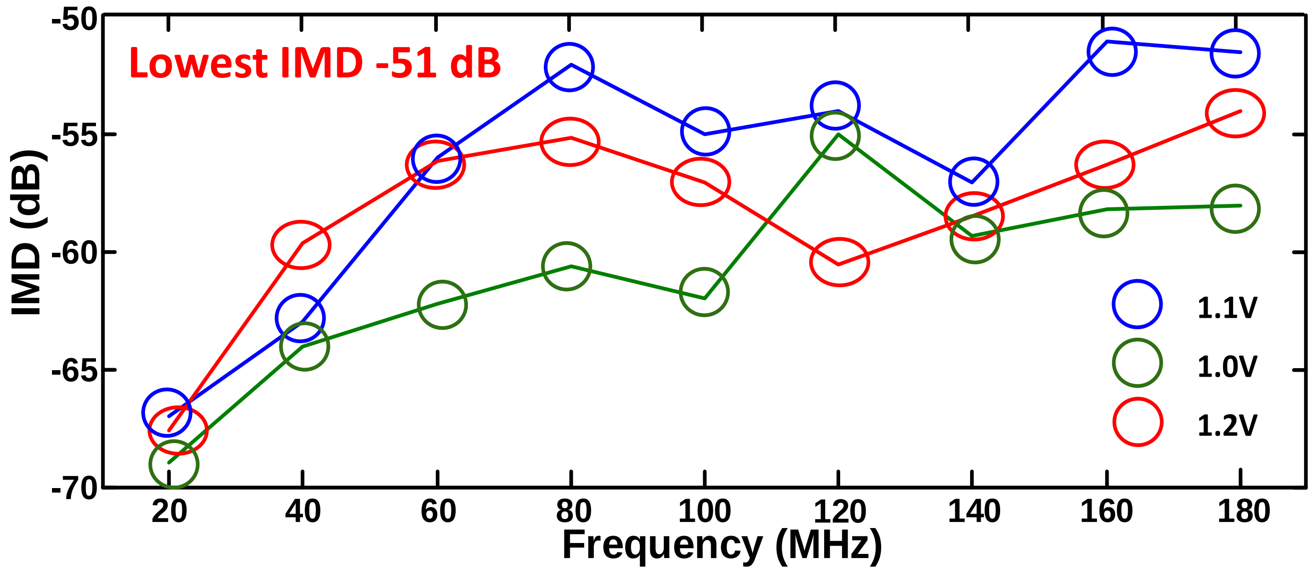
Measured intermodulation distortion at band edge with control voltage

Measurement Results (IV)



Output Swing 1Vpp

Measured intermodulation distortion at band edge across temperature

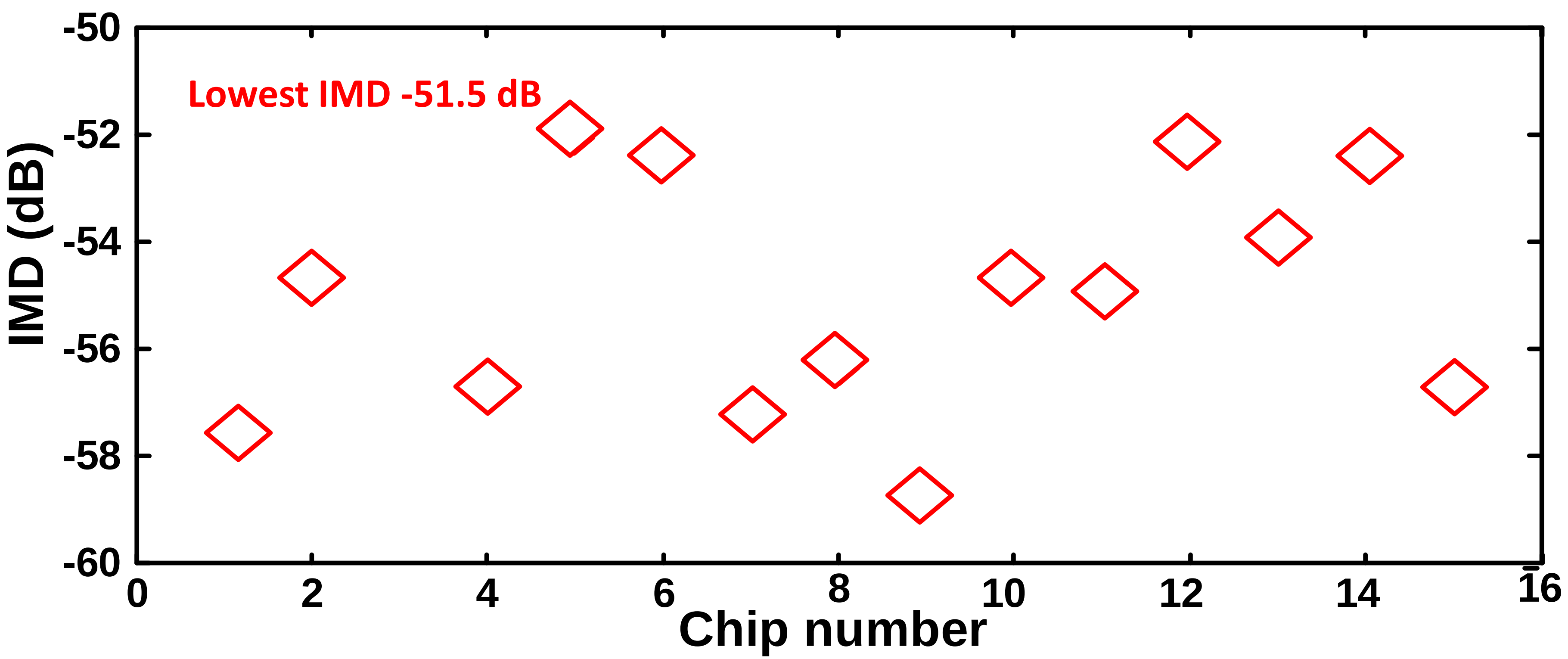


Output Swing 1Vpp

Measured intermodulation distortion at band edge across power supply

Measurement Results (V)

Output Swing 1Vpp



Measured intermodulation distortion at band edge @fc=314MHz across 15 chips

Performance Summary & Comparison

	[1]	[2]	[3]	This Work
Technology (nm)	65	90	90	**65**
Supply voltage (V)	0.6	0.55-0.9	1	**1.1**
Power (mW)	26.2	1.9	4.4	**4.6**
Area/N (mm^2)	0.095	0.073	0.039	**0.007**
Bandwidth (MHz)	70	7-30	8.1-13.5	**34-314**
Noise (nV/$\sqrt{Hz}$)	44	33	75	**25**
N	4	4	8	**3**
DC gain (dB)	0	0	0	**3**
IIP3 (dBm)	32.8	29.6	22.1	**22.4**
FOM (aJ)	117	126	238	**61**
FOM T	182	177	173	**186**

10x lower area

9x Continuous tunable

IIP3 @ 260 MHz

[1] ISSCC 2014, [2]ISSCC 2012, [3] JSSC 2009

Conclusions

- **Continuously tunable filter**
  - MOSCAPs are used as filter capacitors
  - SCCB inverters for improved PVT tolerance
  - Low pass filter architecture
  - Self compensation to improve power efficiency
- **Prototype design**
  - 34-314MHz tunable, 22.4 dBm IIP3 third order filter

Acknowledgement

Research supported by the DARPA CLASIC program

Back up slides

IIP3 (Out of Band: Simulation)

- **Fc = 34MHz**
- **Fin = 1GHz, 1.1GHz**