An Injection Locked PLL for Power Supply Variation Robustness Using Negative Phase Shift Phenomenon of Injection Locked Frequency Divider

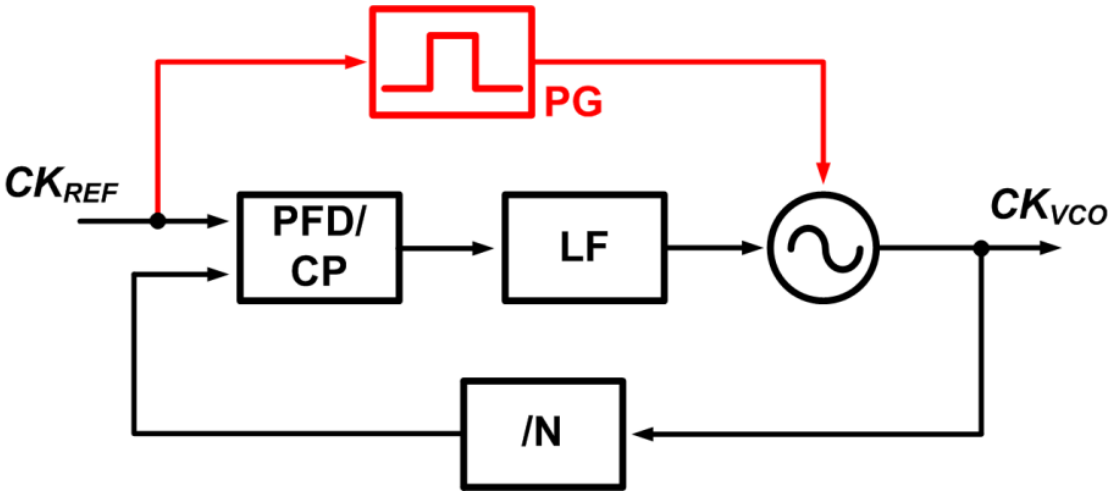
Dongil Lee, Taeho Lee, Yong-Hun Kim, Young-Ju Kim and Lee-Sup Kim

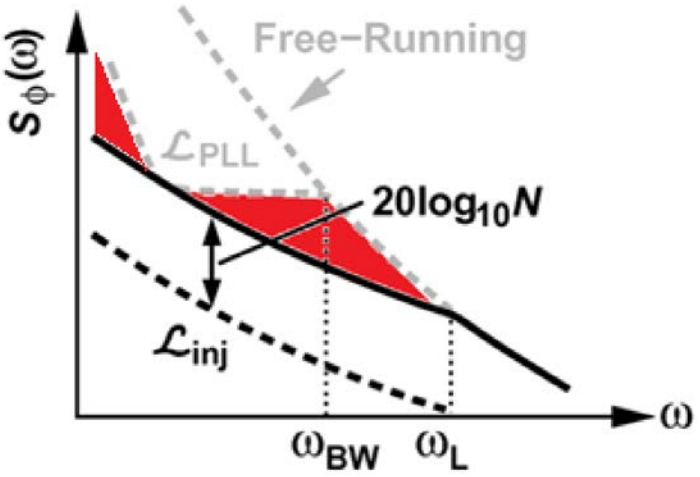
KAIST, Daejeon, Korea

Outline

- Introduction
- Negative phase shift phenomenon
- Background injection timing calibration
- Measurement Results
- Conclusions

Injection-locked PLL





[Jri Lee, JSSC, 2009]

- Frequency synthesizer

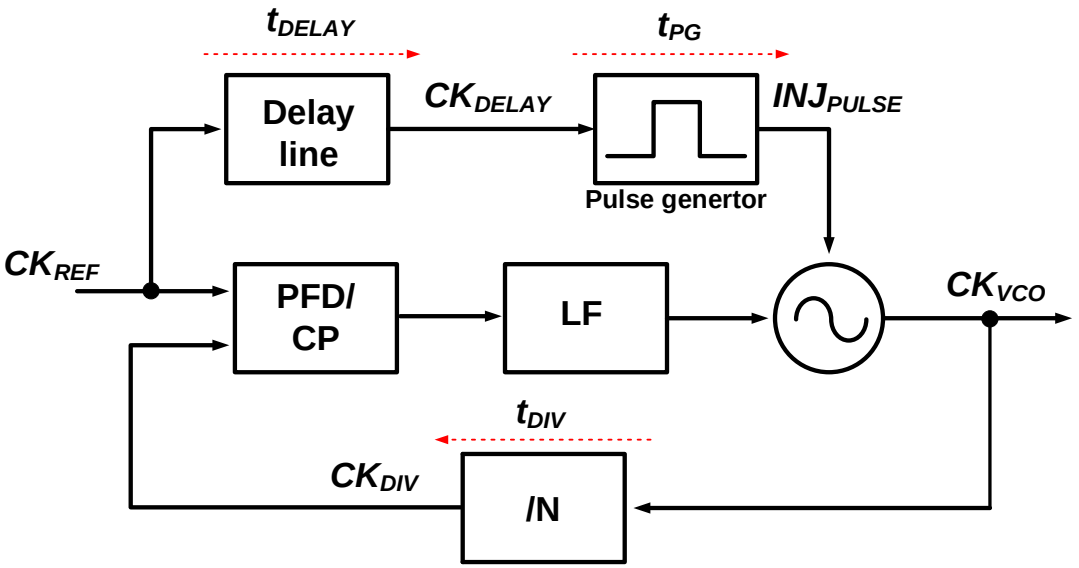
  → Widely used in various communication systems

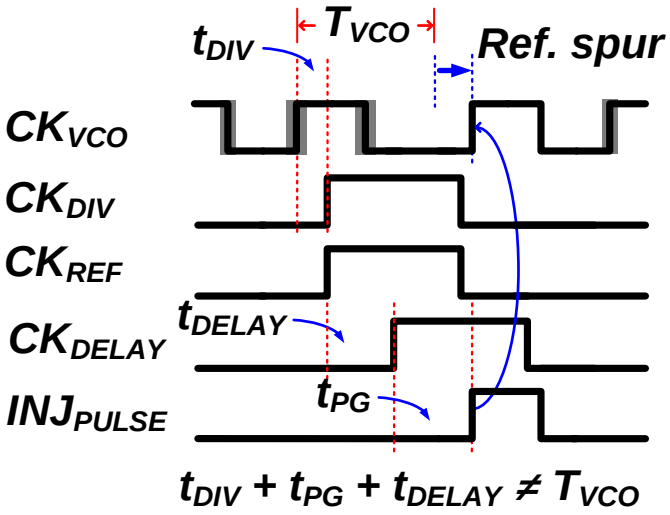
  → Low phase noise clock is essential

  for system performance

- Injection-locked PLL(ILPLL) is well suited

Injection timing mismatch



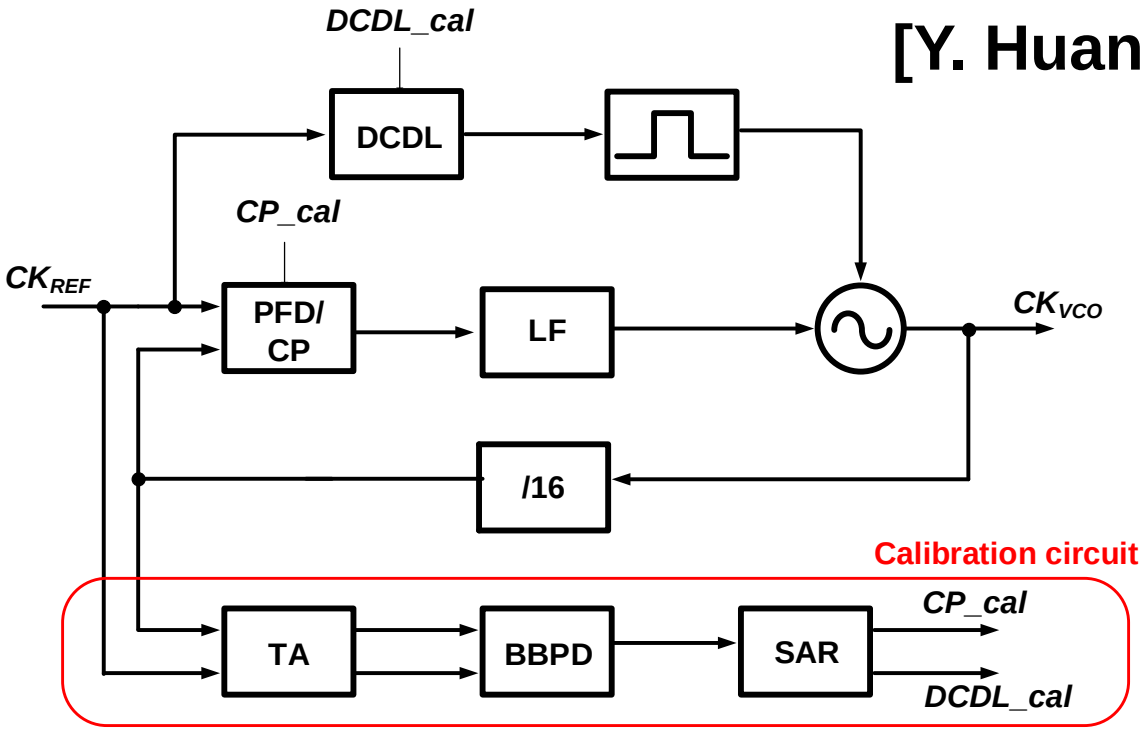


- **Jitter reset by clean reference injection**
- **However, large reference spur is generated due to injection timing mismatch**
- **Optimum injection timing**

$$t_{DIV} + t_{PG} + t_{DELAY} = T_{VCO}$$

Injection timing calibration [2]

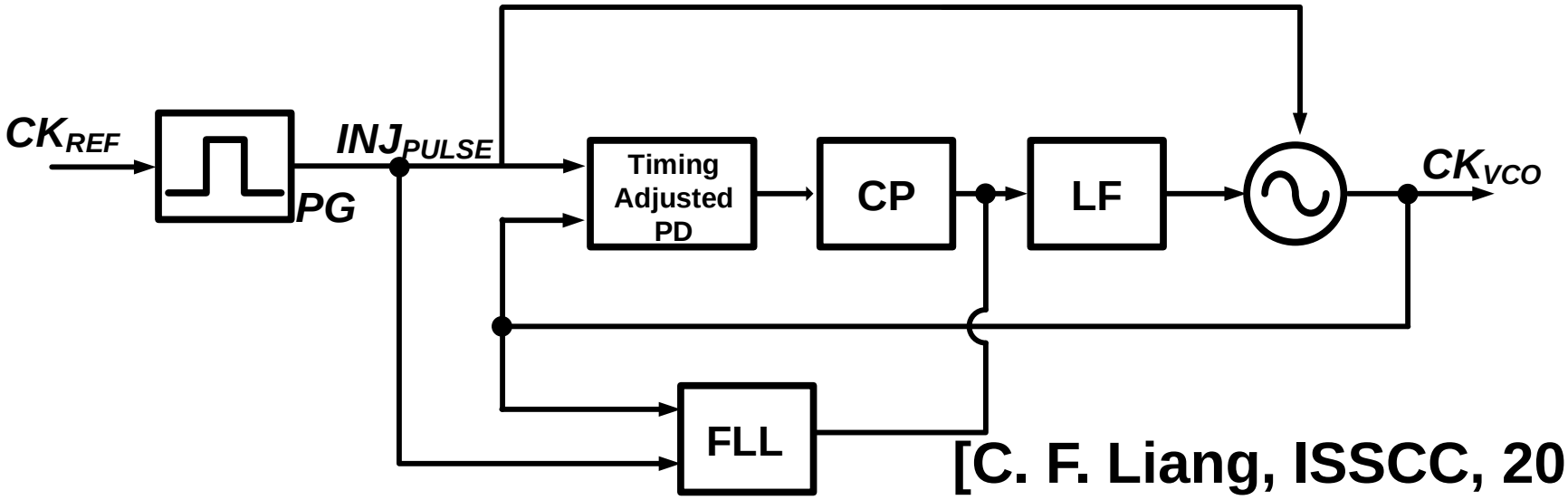
[Y. Huang, JSSC, 2013]



- Using time amplifier, injection timing is calibrated
- Limited to the foreground calibration due to complexity
- Delay line is sensitive to supply noise

➔ Vulnerable to voltage and temperature variation

Divider-less ILPLL[3, 4]



[C. F. Liang, ISSCC, 2011]
[I. Lee, ISSCC, 2013]

- Divider-less ILPLL
  - ➔ Achieve low phase noise
  - ➔ No injection timing mismatch
- Sensitive to voltage and temperature variation due to the limited frequency tracking range

Injection timing calibration

- **Optimum injection timing**

$$t_{DIV} + t_{PG} + t_{DELAY} = T_{VCO}$$

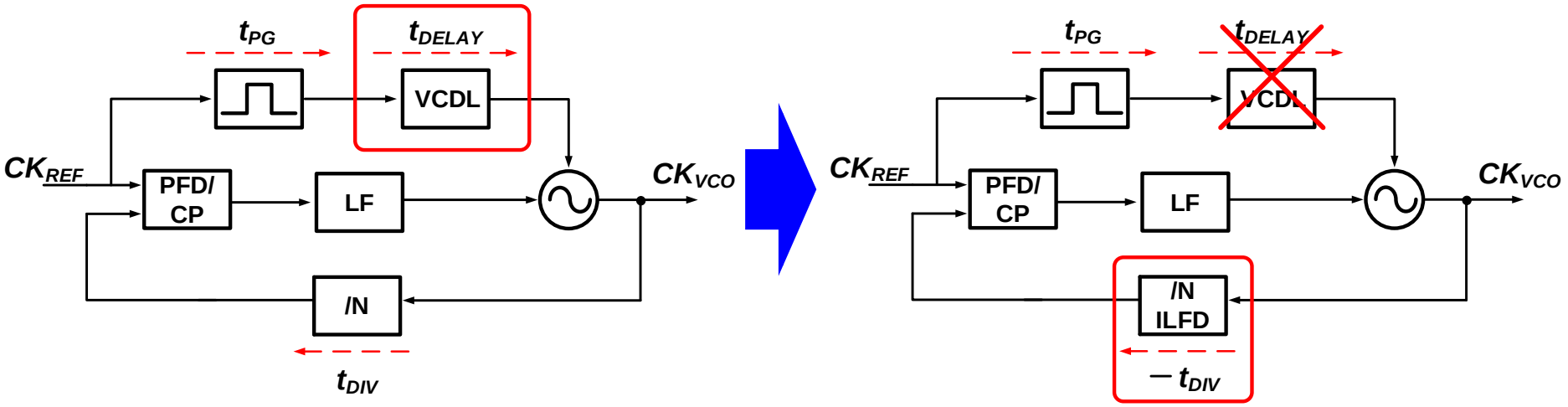
- **Difficult to find the exact amount of t_{DELAY}**
  - **Complex timing calibration method**

    (limited to the foreground calibration)
  - **Divider-less ILPLL**

Problems

⇨ ***Vulnerable to voltage and temperature variations***

Motivation

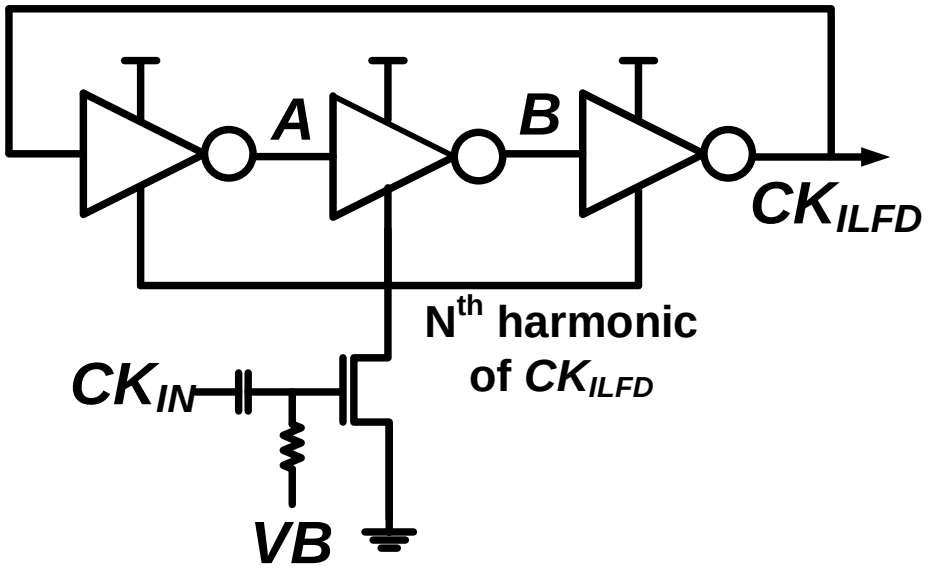


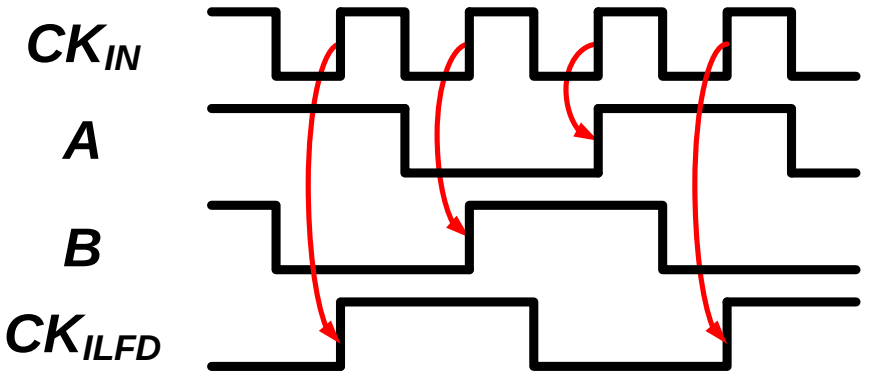
- **Simple structure for easy calibration**
  - ➢ **Delay line is removed**
- **Negative phase shift of divider**

$$t_{DIV} + t_{PG} + t_{DELAY} = T_{VCO} \quad \Rightarrow \quad (-t_{DIV}) + t_{PG} = 0$$

How to achieve negative phase shift?

Injection locked frequency divider



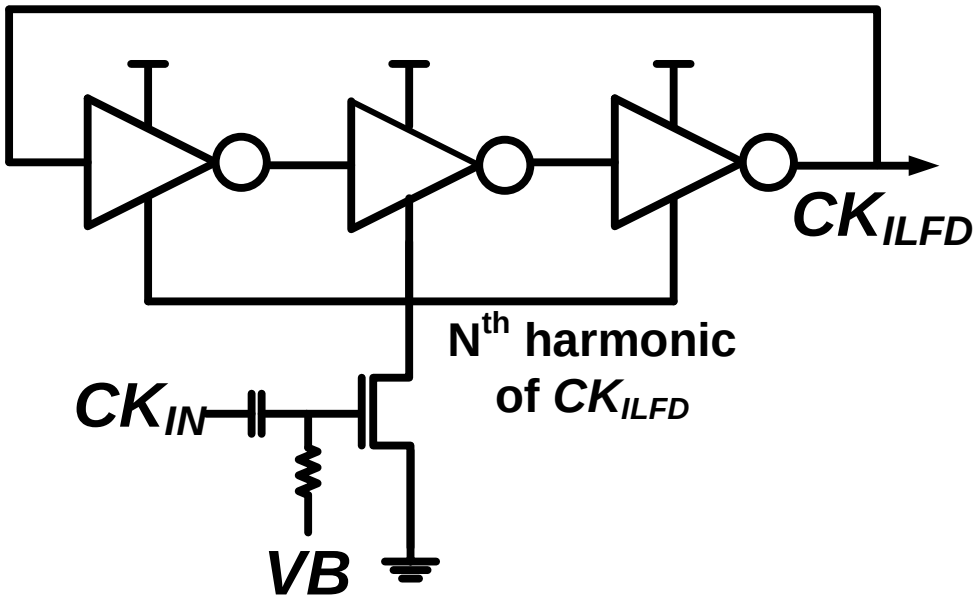


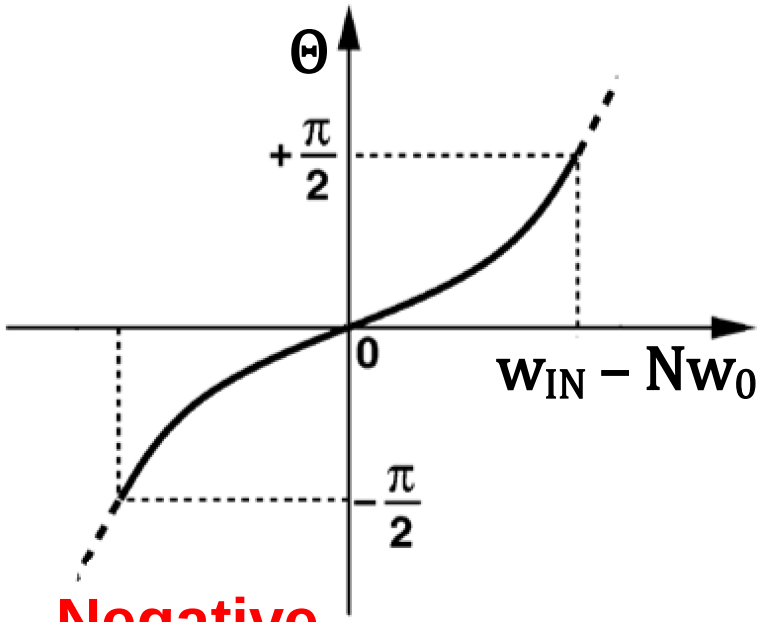
- **Injection locked frequency divider (ILFD)**
  - **Frequency locking**

    → CK_{IN} and N^{th} harmonic of CK_{ILFD}

    ($w_{IN} = Nw_{ILFD}$)

Negative phase shift phenomenon





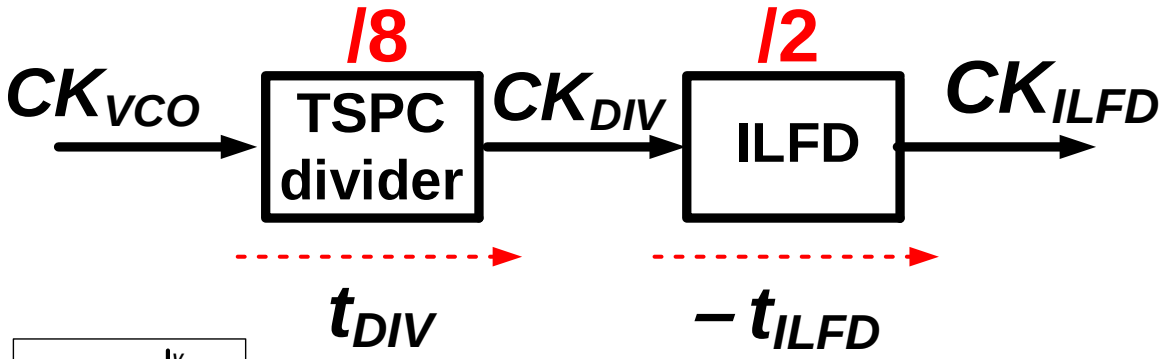
Negative Phase shift

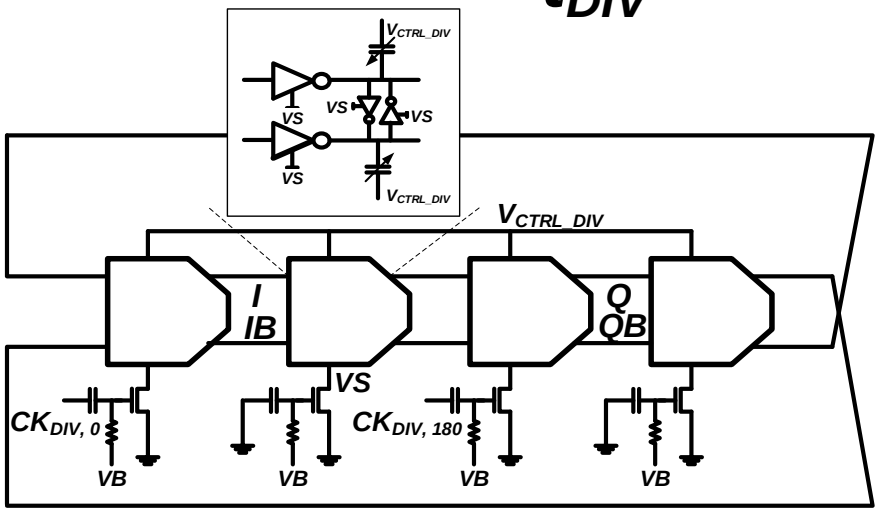
$$\Theta \propto \sin^{-1}[(w_{IN} - Nw_0)/K]$$

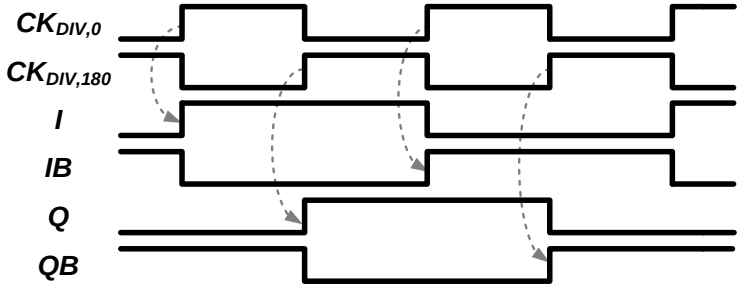
- When $w_{IN} - Nw_0 < 0$, (w_0 : free-running frequency)

  ILFD can have **negative phase shift**

Proposed ILFD

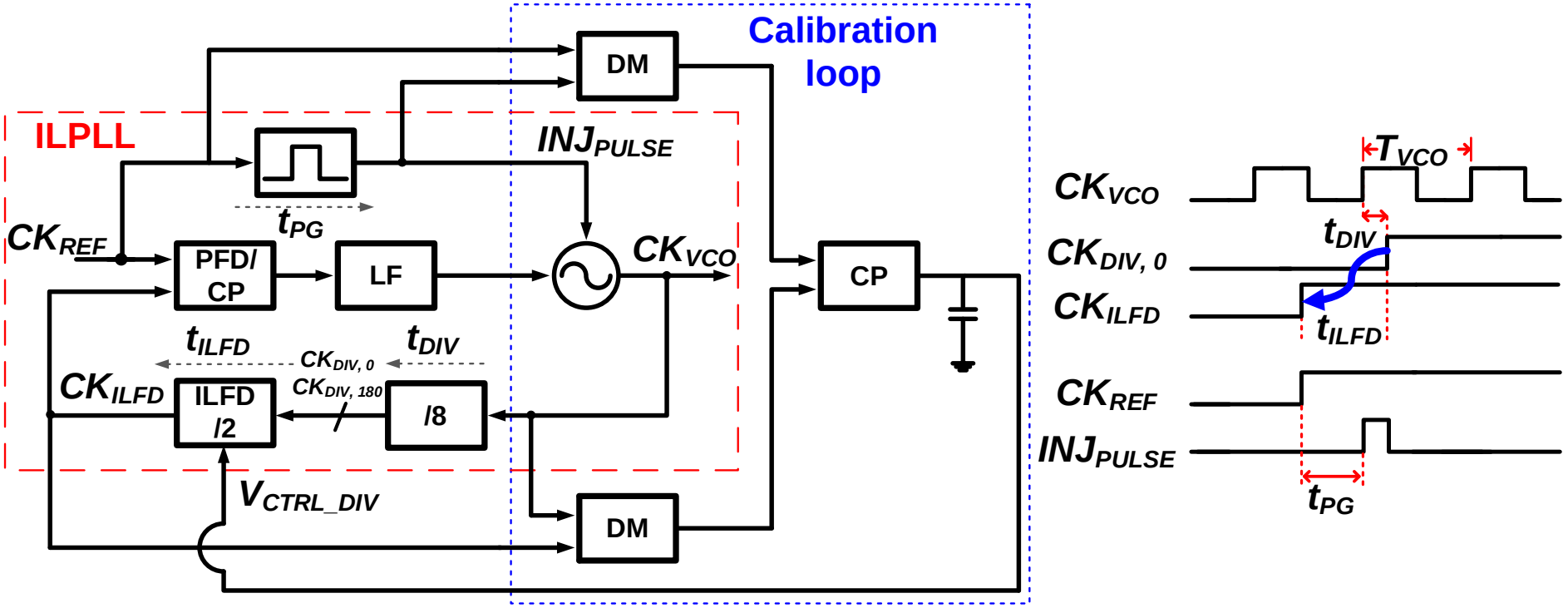






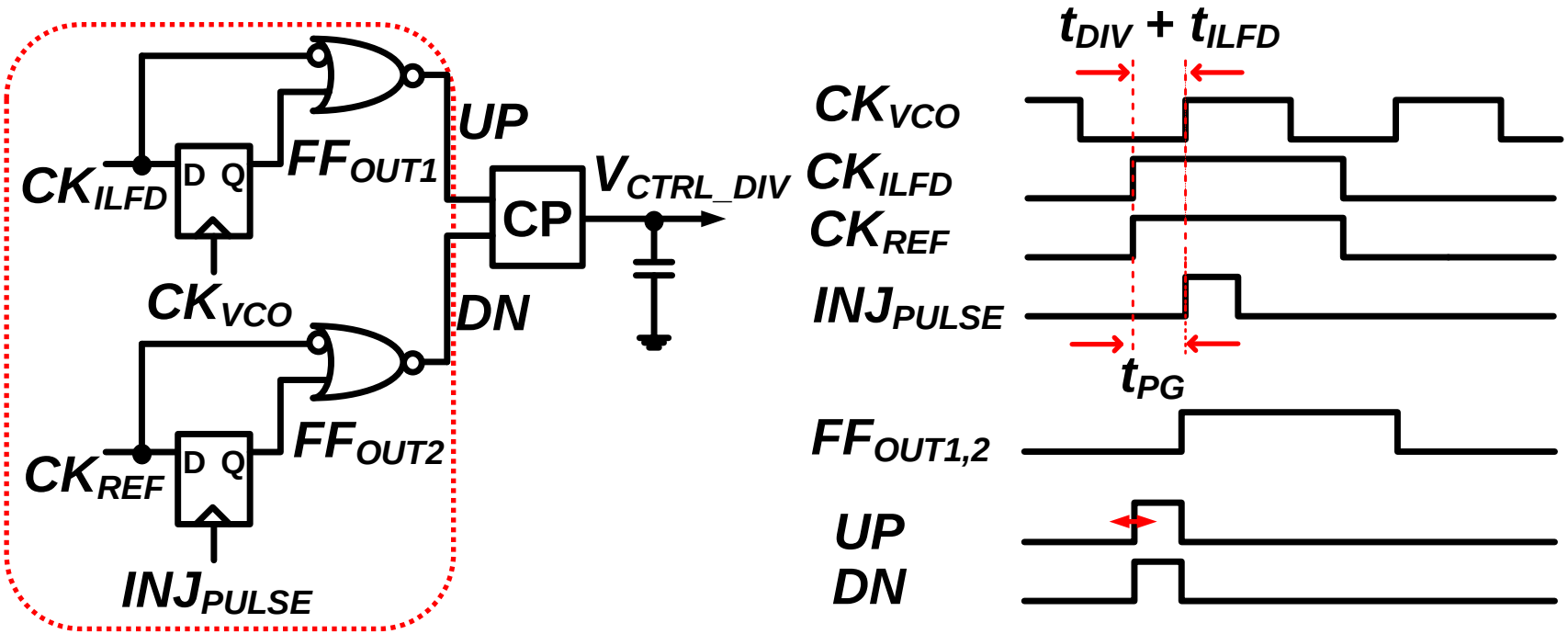
- **Two-stage divider (TSPC divider + ILFD)**
  - **to achieve wide lock range and phase control range**

Overall Architecture



- **Negative phase shift : ILFD**
- **Background calibration loop**
  - **Simply matching $t_{DIV} + t_{ILFD}$ to t_{PG}**

Background calibration loop



Delay measurement blocks (DMs)

- **Two DMs measure the delays (t_{PG} and $t_{DIV} + t_{ILFD}$)**
- **V_{CTRL_DIV} controls ILFD's free-running frequency and finds optimum delay ($t_{PG} = t_{DIV} + t_{ILFD}$)**
- **Background calibration**

Injection timing calibration

- **Proposed optimum injection timing**

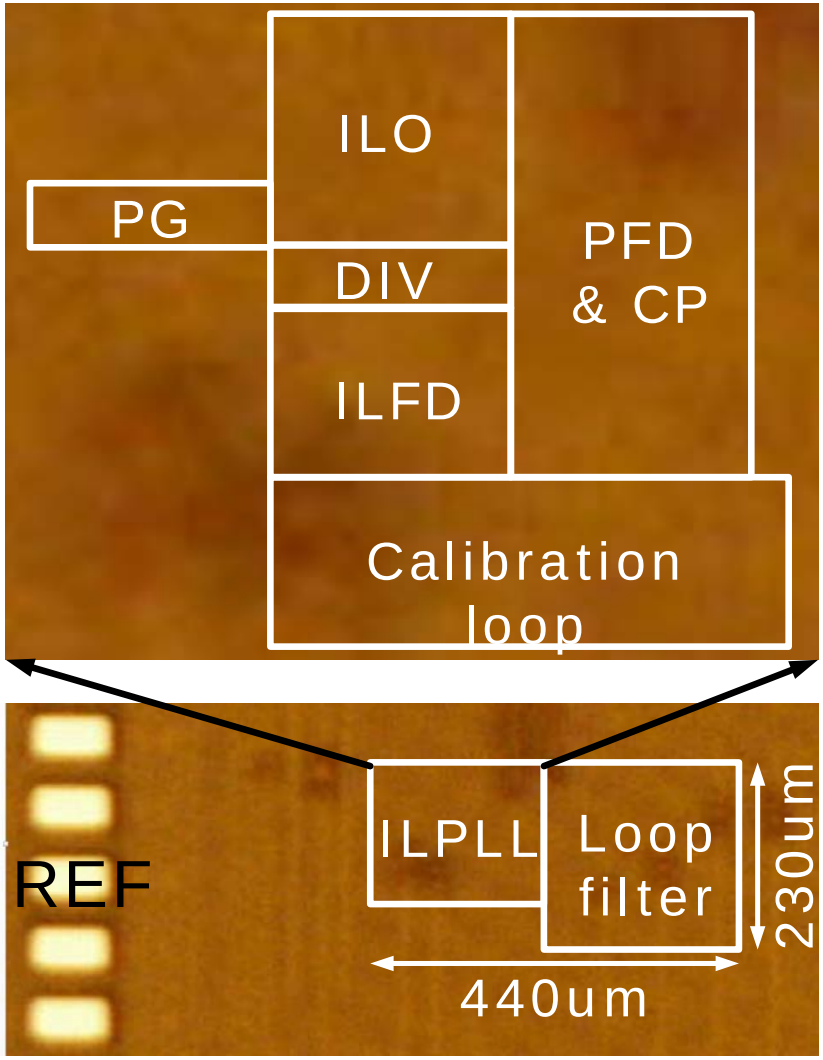
$$(-t_{DIV}) + t_{PG} = 0$$

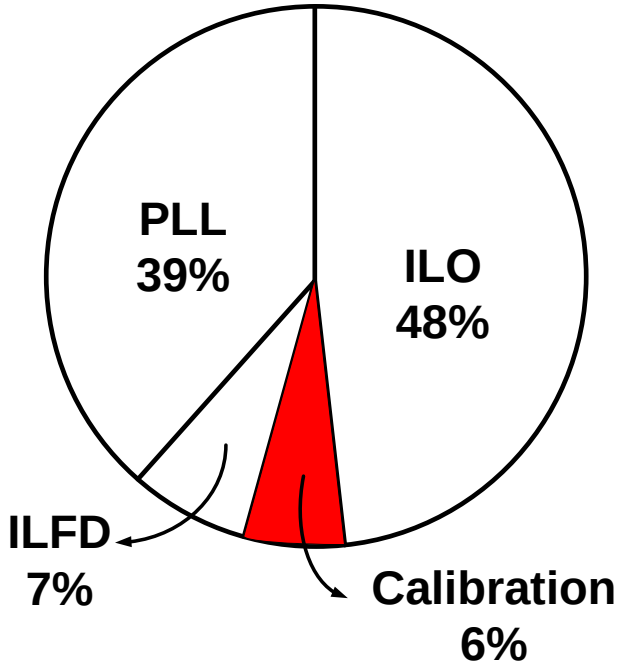
- **Easy to find the $t_{DIV} = tP_G$**
  - **Simple structure**
  - **Background calibration with low power**

Achievement

⇨ ***Robust to voltage and temperature variations***

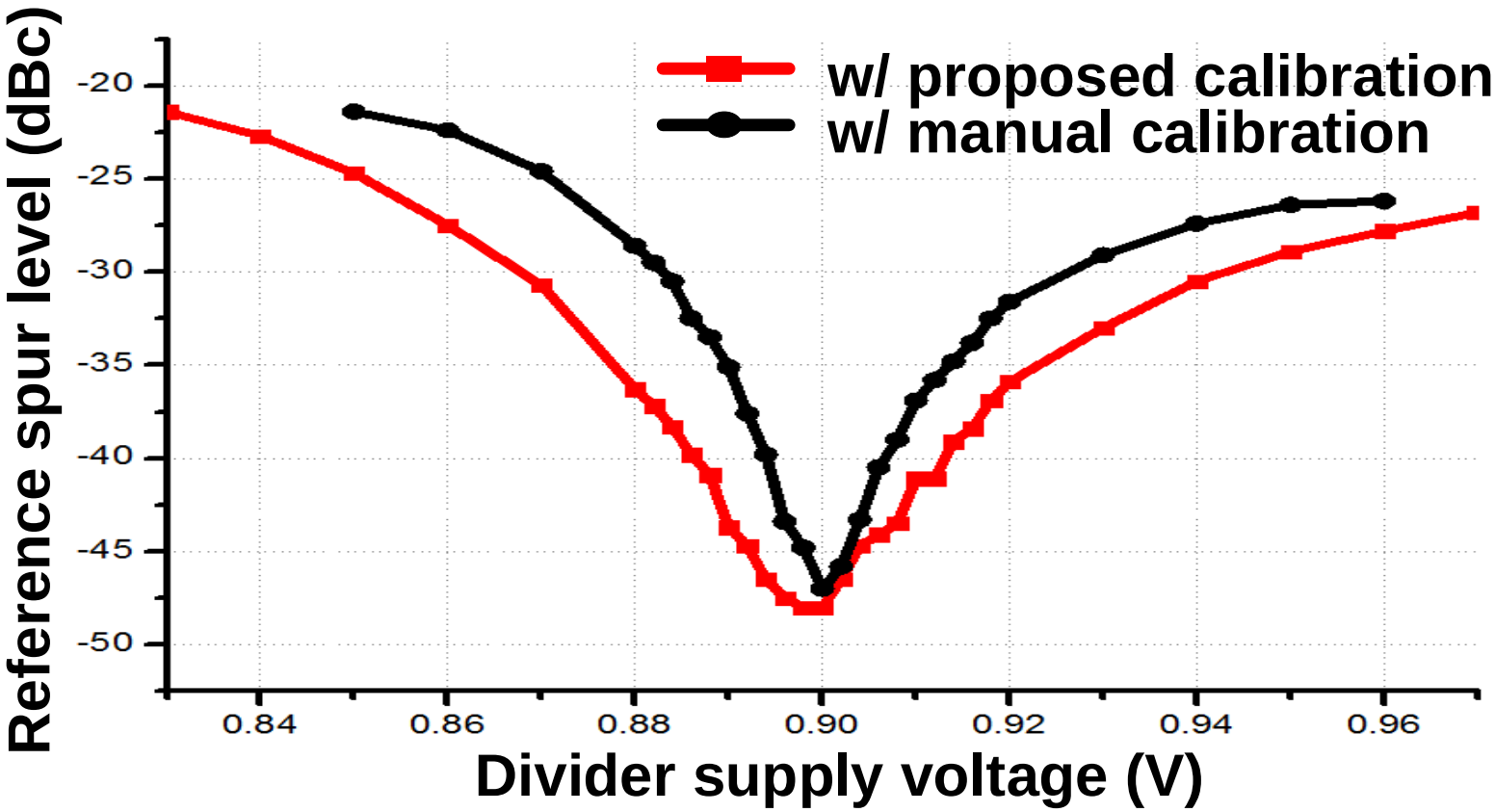
Chip Micrograph





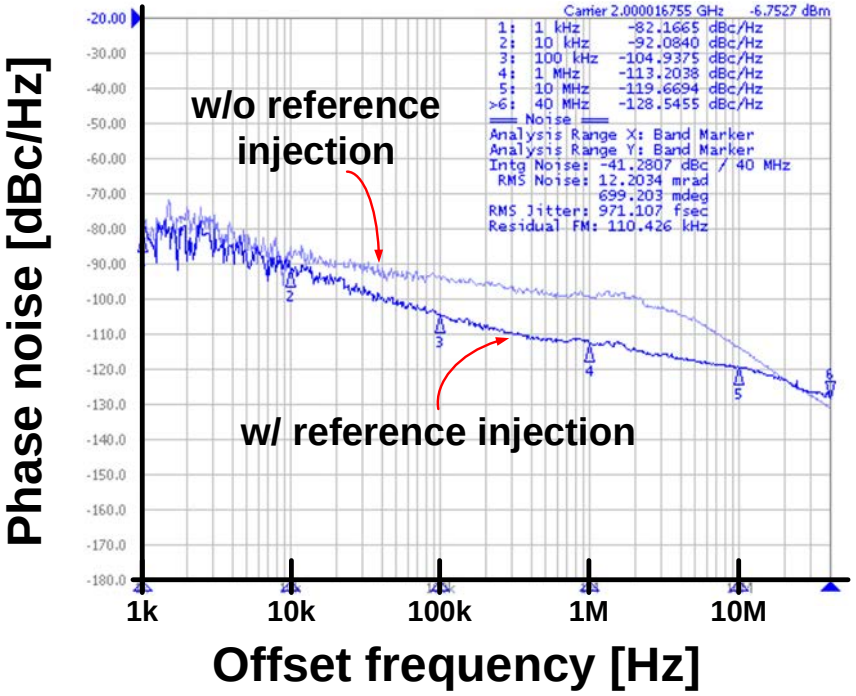
Technology	65nm CMOS
Frequency	2GHz
Power consumption	3.74mW

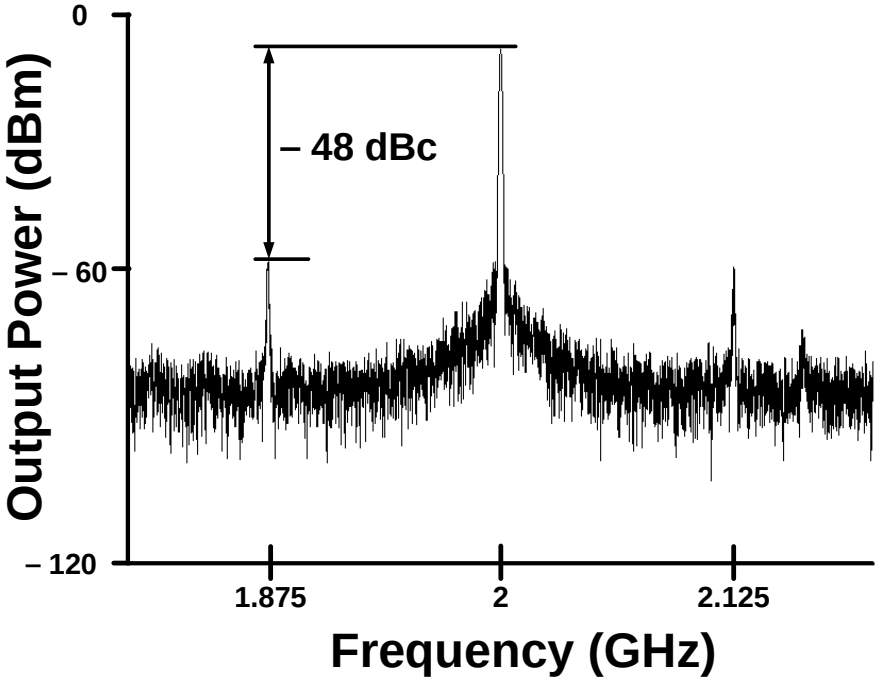
Supply voltage variation



- With calibration, about 27% operating range improvement and maximum 8dB reference spur improvement at 0.89V supply

Phase noise performance





- **Phase noise : -113dB @ 1MHz offset**
- **Integrated RMS jitter : 971fs**
- **Reference spur : -48dBc @ 125MHz offset**

Comparison Table

	[2]	[3]	[4]	[5]	This work
Method	Analog ILPLL	Analog ILPLL	Analog ILPLL	Digital ILPLL	Analog ILPLL
VCO Type	LC	Ring	LC	Ring	Ring
Frequency (GHz)	2.4	0.432	2.4	0.5~1.6	2
Reference (MHz)	150	27	150	40~300	125
Phase Noise (dBc/Hz) @ 1MHz	–129	–123	–126	–128	–113
Integrated Jitter (σ_t)	145fs	2.4ps	188fs	700fs	971fs
Reference Spur(dBc)	–40	–70.7	–48.8	–57	–48
Power(mW)	12.6	6.9	5.2	0.97	3.74
Area(mm^2)	0.64	0.03	0.25	0.022	0.1
Process(nm)	180	55	65	65	65
FOM	–246	–224	–247	–243	–234.5
Timing Method	Foreground	Divider-less	Divider-less	Dual-loop	Background

Conclusions

- **A 2 GHz ILPLL with ILFD is proposed**
- **Negative phase shift phenomenon of ILFD enables simple injection timing calibration**
- **Background calibration achieves power supply variation robustness**