# 2-4 GHz Q-Tunable LC Bandpass Filter with 172-dB·Hz Peak Dynamic Range, Resilient to +15-dBm Out-of-Band Blocker


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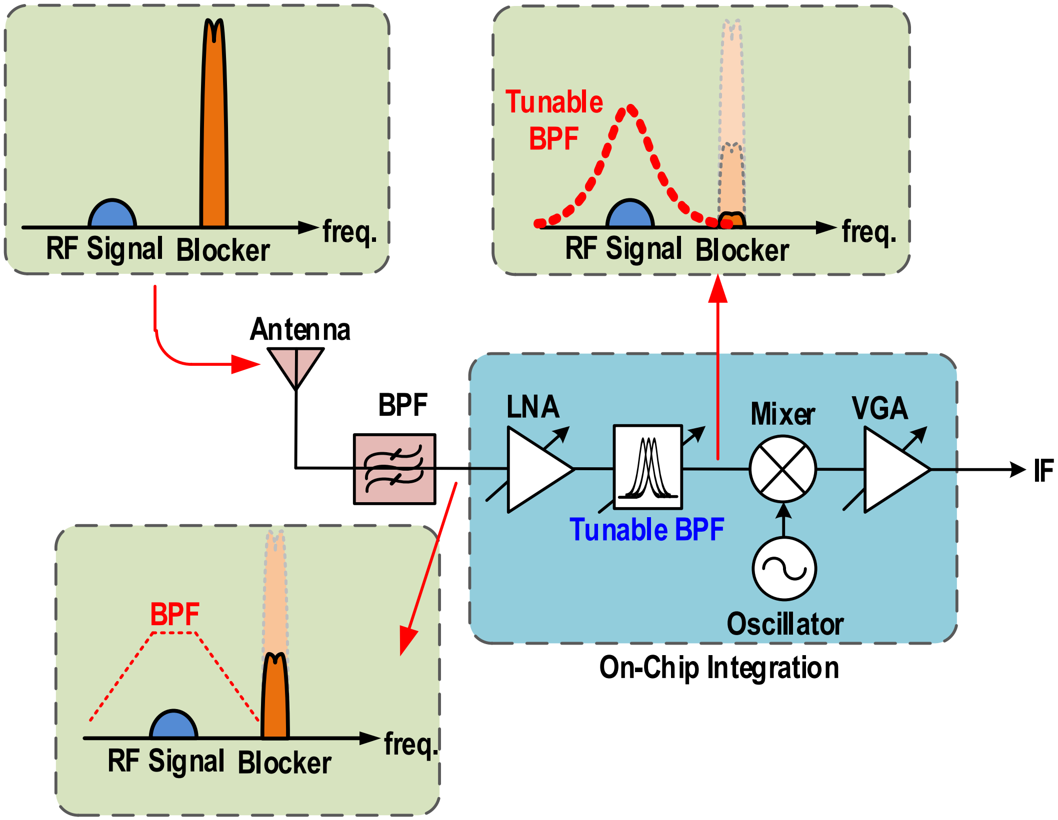
# Outline

- Background / Motivation
- Current-Driven BPF vs Voltage-Driven BPF
- Band-Pass Filter Circuit Design
  - Dual Varactor Inverse (DVI) Control
  - LC-Resonator with Dynamic Negative Resistance
- Measurement Results
- Conclusion

# Introduction

## ❑ <u>On-Chip Tunable Band-pass Filter:</u>




- Frequency selectivity at the earliest possible stage in the receiver chain.
- Band pass filtering after LNA will increase the rejection of the strong blocker, relieving interference issue in the receiver chain.

# Q-Enhanced LC BPFs

## ❑ Q-enhanced LC filters suffer from:

- Tradeoff between selectivity and dynamic range.
- Linearity and NF degrade as Q increases.

# Design Objectives

- **Q-enhanced LC filters suffer from:**
  - Tradeoff between selectivity and dynamic range.
  - Linearity and NF degrade as Q increases.

- **On-chip Compact Q-Enhanced LC BPF that has:**
  - 2:1 wideband frequency tuning range (2-4 GHz).
  - Bandwidth tuning independent from frequency tuning.
  - Variable gain (>12 dB).
  - High dynamic range.
  - Robust to large Interferer (blocker power>0 dBm).

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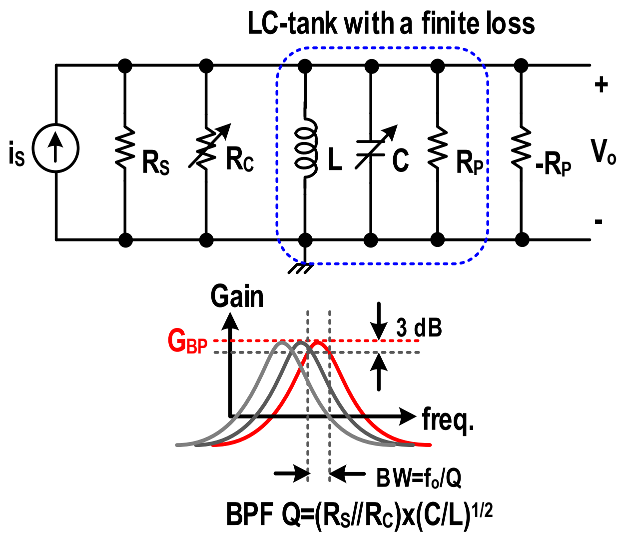
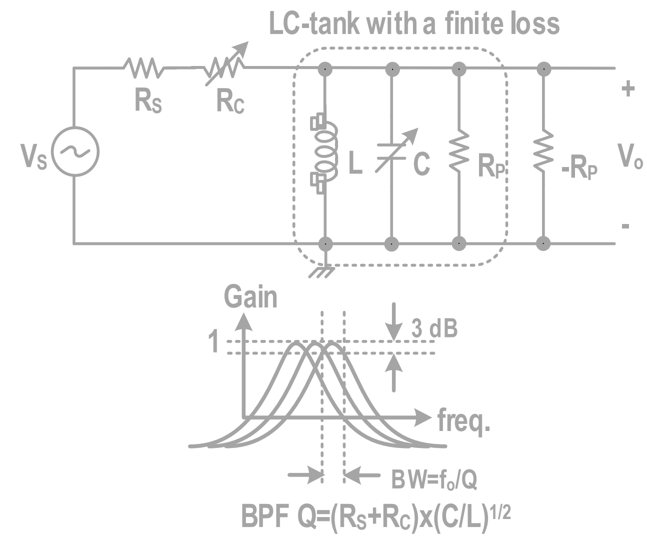
# Current-Driven BPF vs Voltage-Driven BPF

## ❑ Current-Driven BPF




$$V_o = i_s(R_s||R_c) = i_s \cdot Q_F \cdot \sqrt{L/C} = i_s \cdot Q_F \cdot Z_0$$

## ❑ Voltage-Driven BPF




$$V_o = V_s$$

### Current-driven BPF

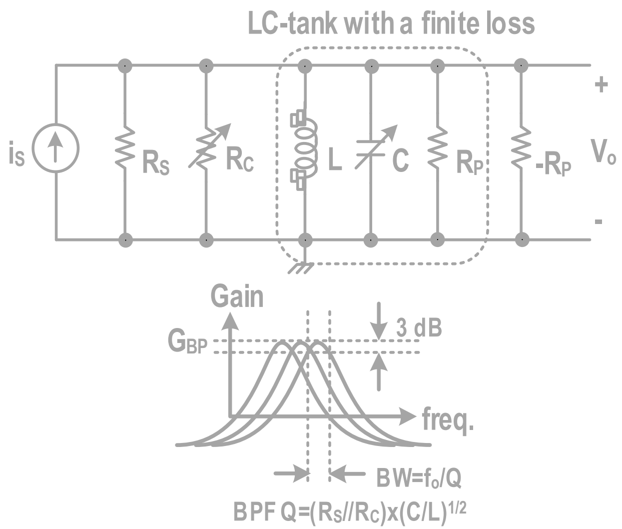
- Gain amplifier topology.
- $V_o$ is proportional to filter Q.
- \+ Larger signal gain with lower NF.
- \- Nonlinearity becomes severe as filter Q increases.

### Voltage-driven BPF

- Gain is limited to unity regardless of the filter Q.
- \+ Linearity will be less sensitive the increase of Q.
- \- Higher NF.

# Current-Driven BPF vs Voltage-Driven BPF

## ❑ Current-Driven BPF




$$V_o = i_s(R_s||R_c) = i_s \cdot Q_F \cdot \sqrt{L/C} = i_s \cdot Q_F \cdot Z_0$$

## Current-driven BPF

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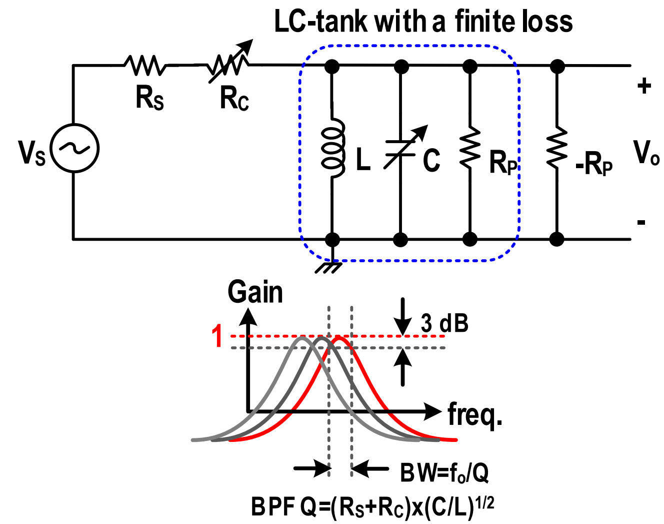
## ❑ Voltage-Driven BPF

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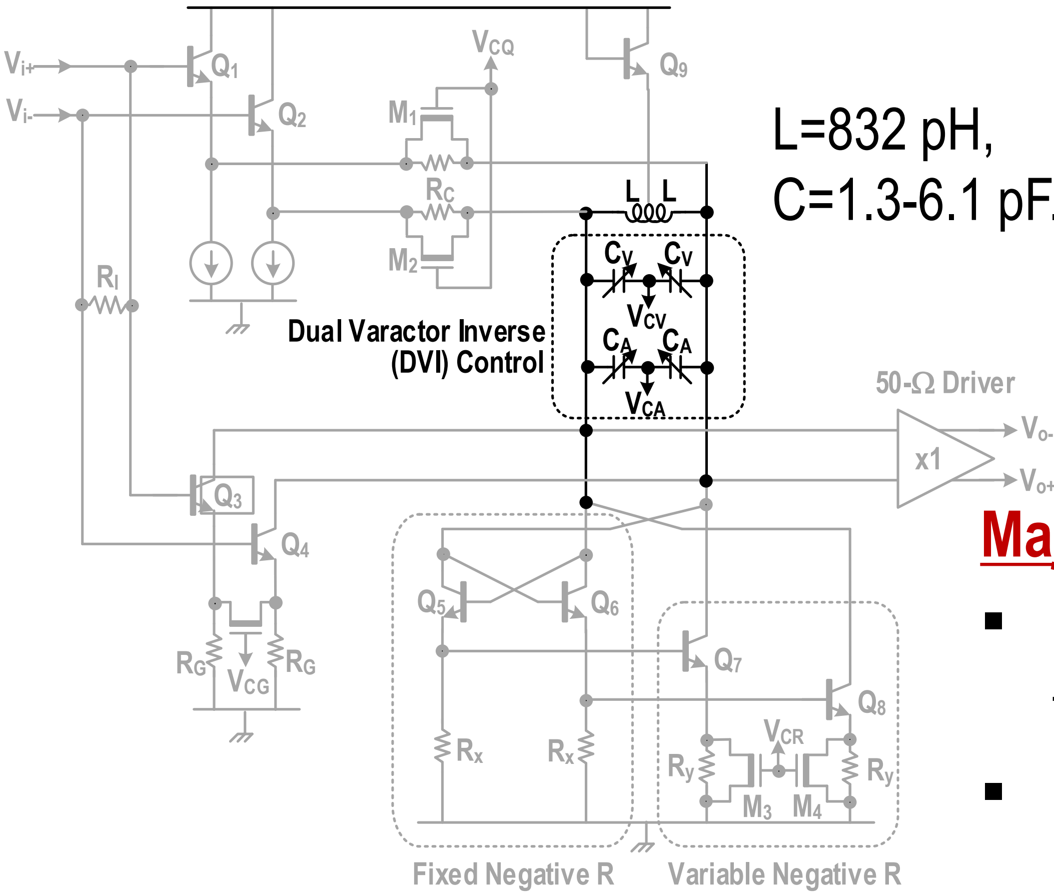
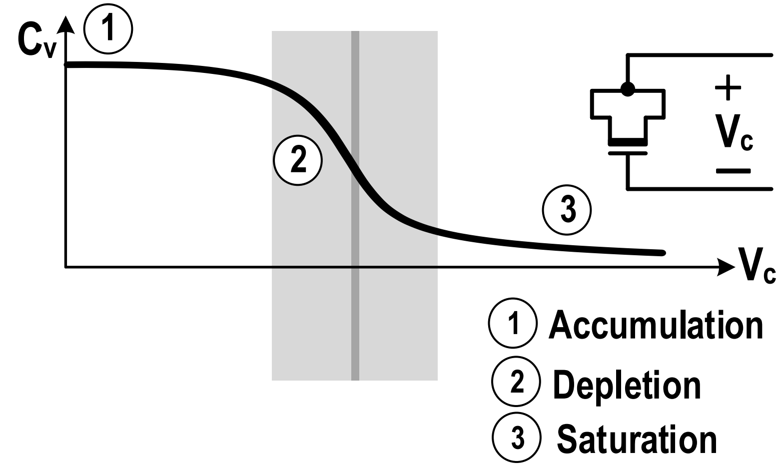
# BPF Circuit Design

## ❑ Varactor Nonlinearity




L=832 pH,
C=1.3-6.1 pF.

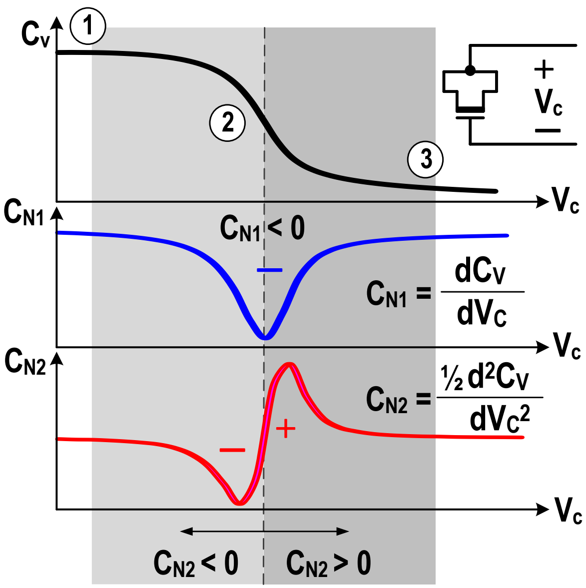



## Major nonlinearity source in tank

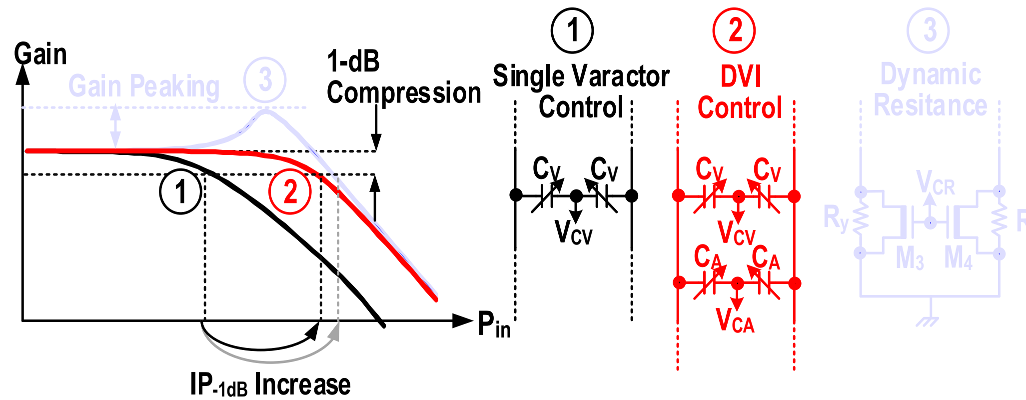
- Need 4:1 varactor tuning to cover 2:1 frequency range.
- Large varactor tuning range introduces sharp nonlinear transition.
- This introduces severe nonlinearity

# BPF Circuit Design

## ❑ Dual Varactor Inverse (DVI) Control




① Accumulation
② Depletion
③ Saturation




Nonlinear C: $C_V(V_c) = C_o + C_{N1} \cdot V_c + C_{N2} \cdot V_c^2$

Nonlinear Q: $dQ_V = C_V(V_c) \cdot dV_c$

Nonlinear Current:

$$i_V = \frac{dQ_V}{dt} = C_V(V_c) \cdot \frac{dV_c}{dt}$$

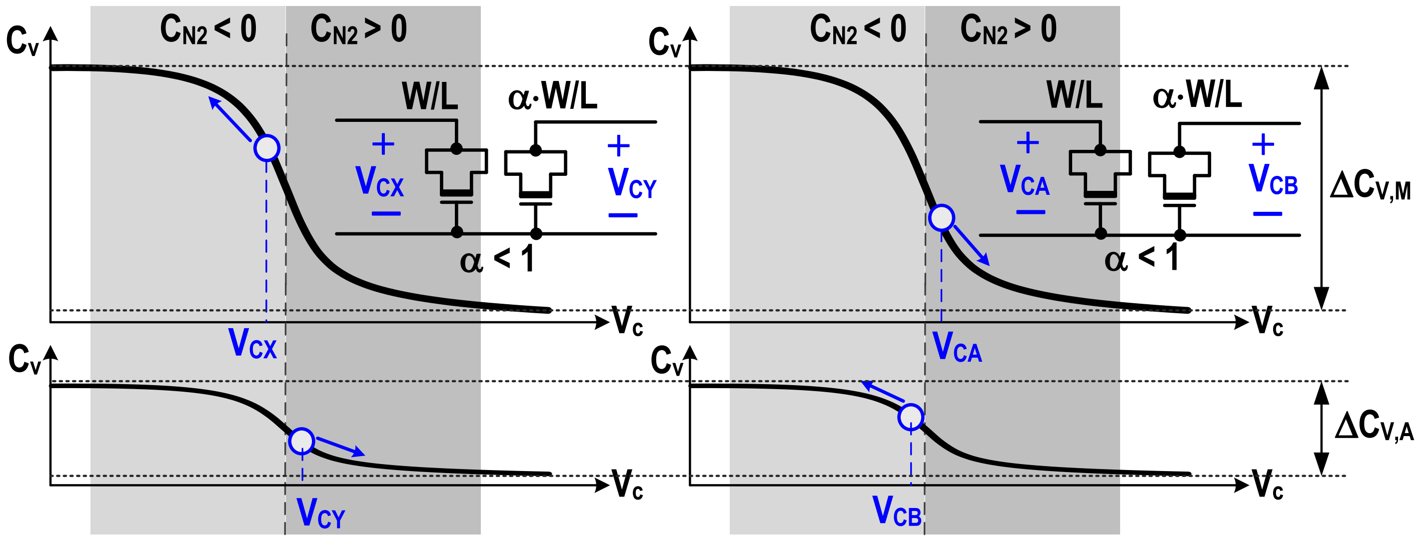
$$= C_o \cdot \frac{dV_c}{dt} + \frac{1}{2} C_{N1} \cdot \frac{dV_c^2}{dt} + \frac{1}{3} C_{N2} \cdot \frac{dV_c^3}{dt}$$

## DVI Control

- The polarity of $C_{N2}$ changes in the middle.
- $C_V$ and $C_A$ move in the opposite direction.
- Substantial cancellation of varactor nonlinear coefficients.
- Increasing $IP_{-1dB}$ by~10 dB.

# BPF Circuit Design

## ❑ Dual Varactor Inverse (DVI) Control




## DVI Control

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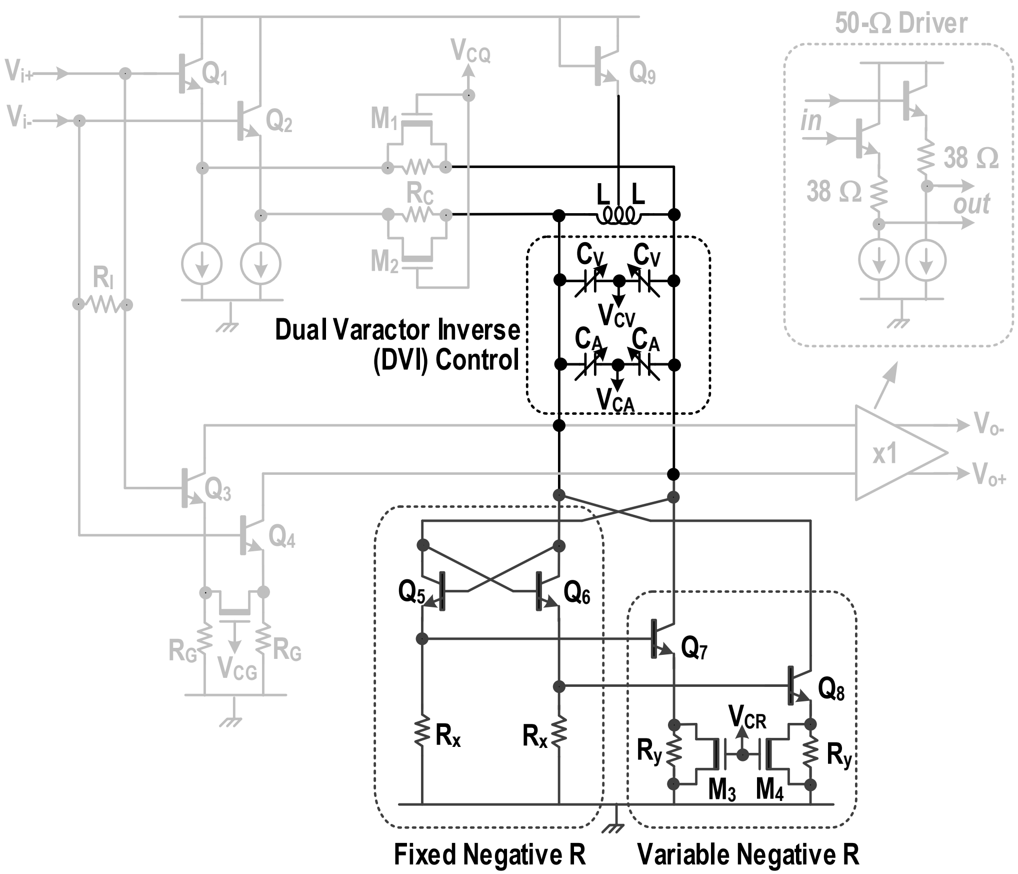
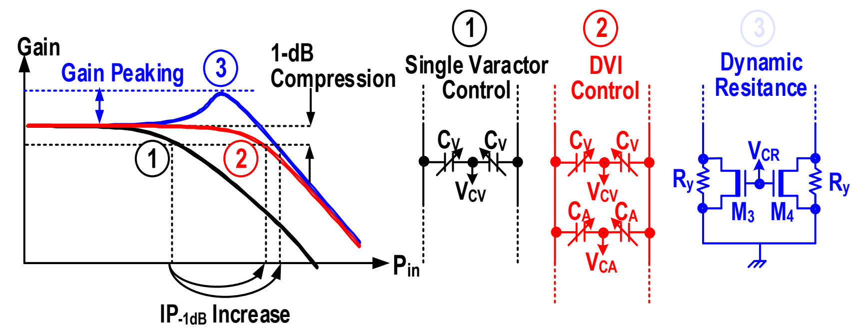
# BPF Circuit Design

## ❑ LC-Resonator with Dynamic Negative Resistance



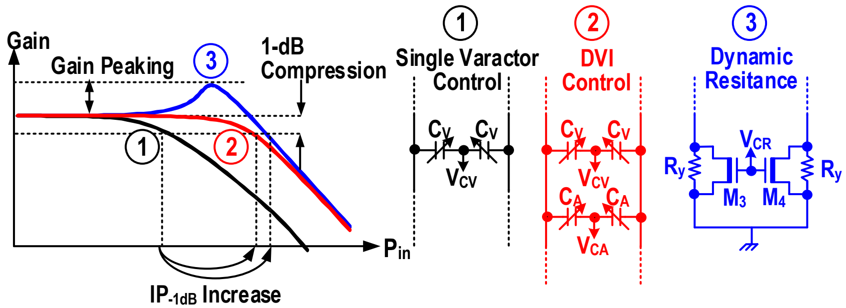

### Dynamic Negative Resistance

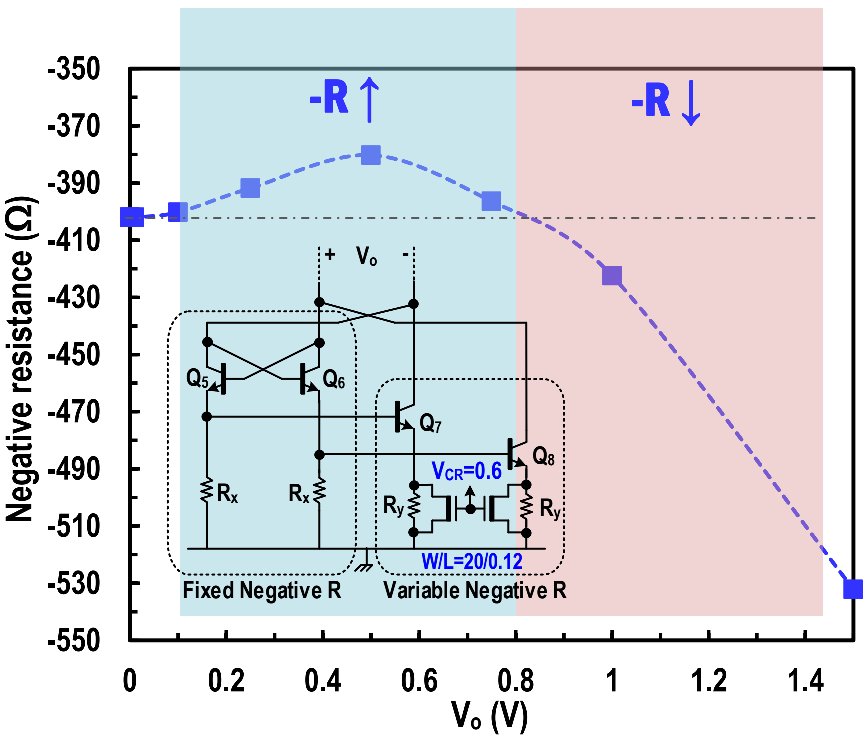
Compensating LC tank limited Q.

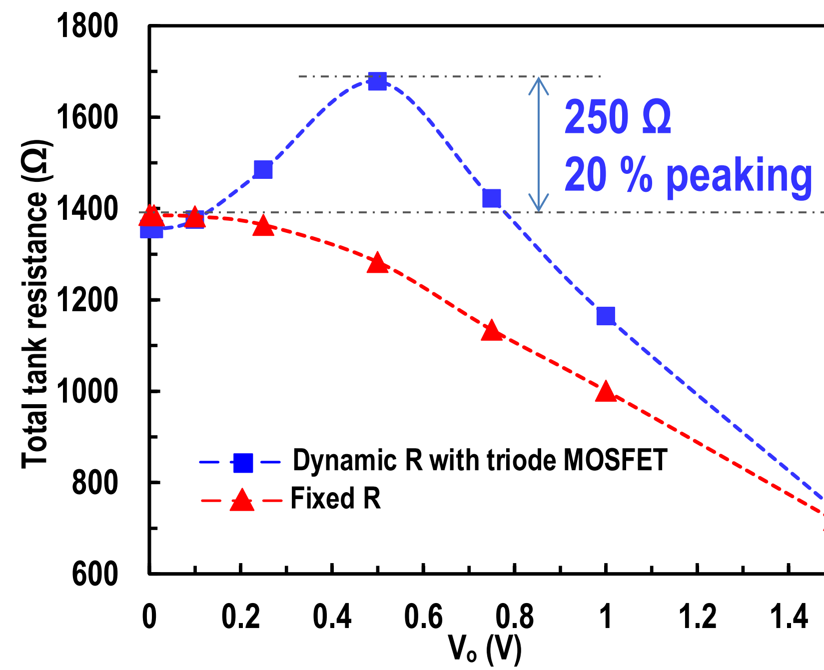
- Further $IP_{-1dB}$ improvement by gain peaking.
- Increases $IP_{-1dB}$ by 2~3 dB.

# BPF Circuit Design

## ❑ LC-Resonator with Dynamic Negative Resistance



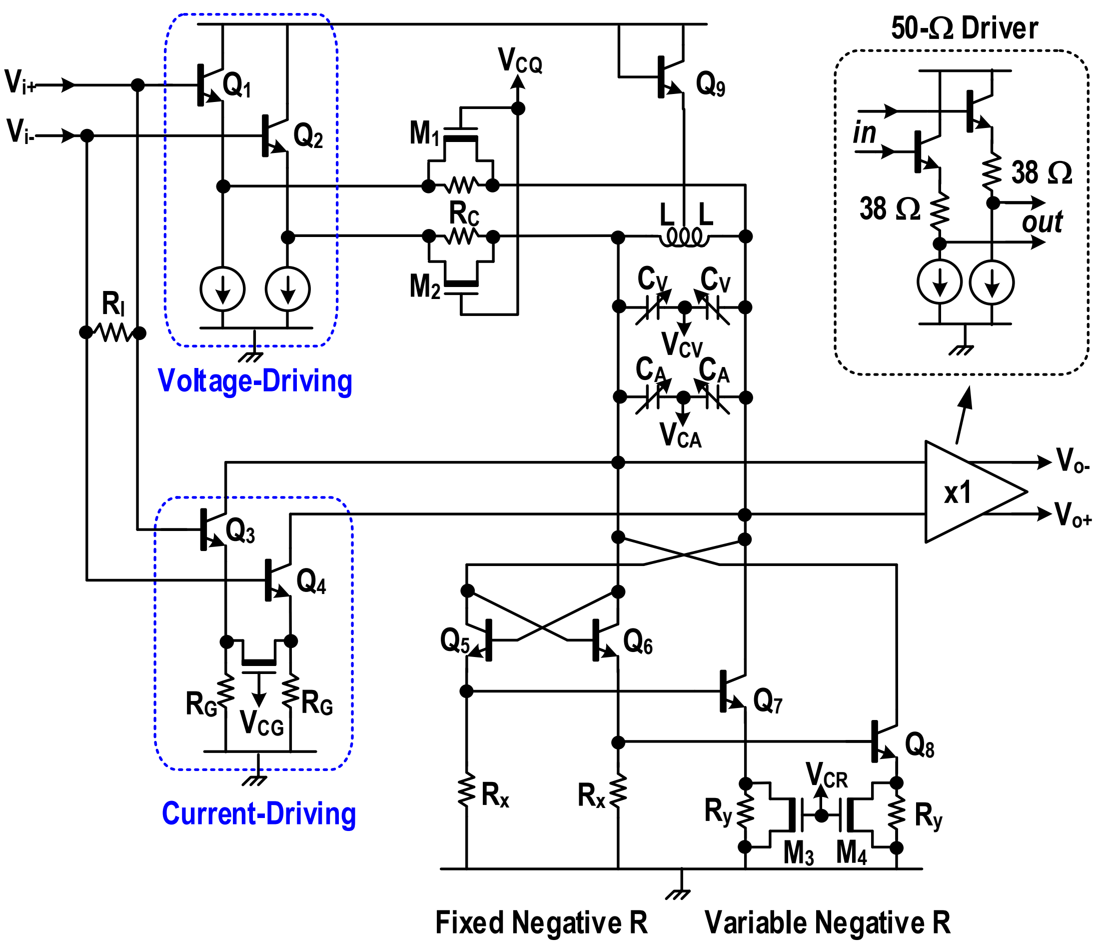




## Negative Resistance @ 3.25 GHz

- More Negative R @ 0.1 to 0.82 V.
- Overall tank resistance increases.

# BPF Circuit Design

## ❑ LC-Resonator Drivers




### Voltage and Current Drivers

- $Q_{1,2}$ voltage mode driving.
- $Q_{3,4}$ current mode driving.
- $R_I$ for input matching.

### Voltage Mode driving

- Lower gain and better linearity.

### Current Mode driving

- Higher gain and better NF.

### Dynamic Range

- Increases by using dual-mode driving.

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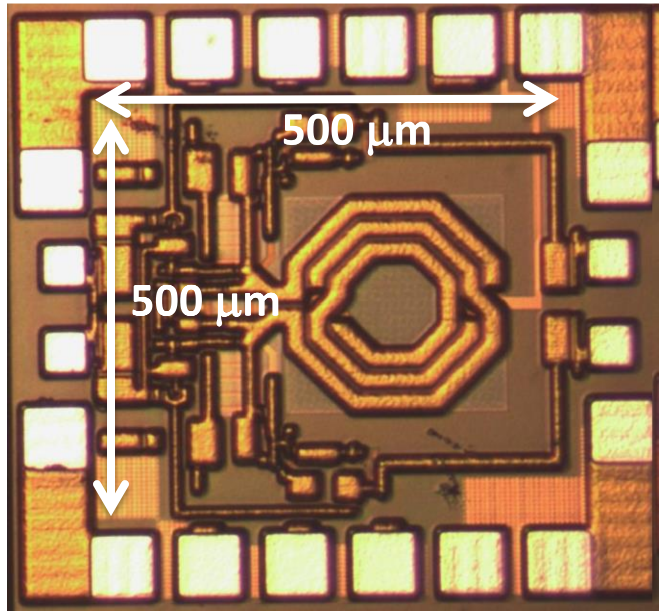
# Measurement Results

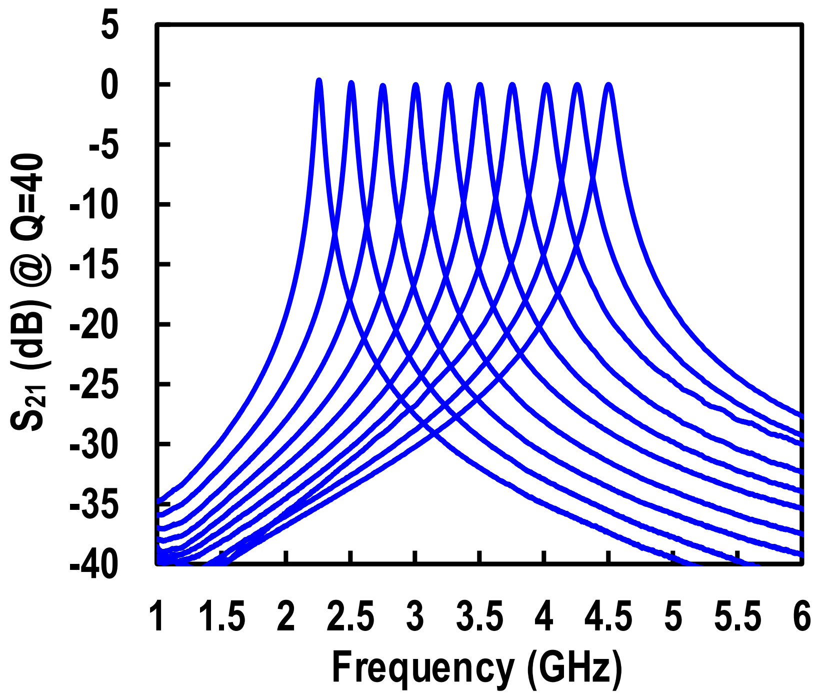
## ❑ Chip Photo

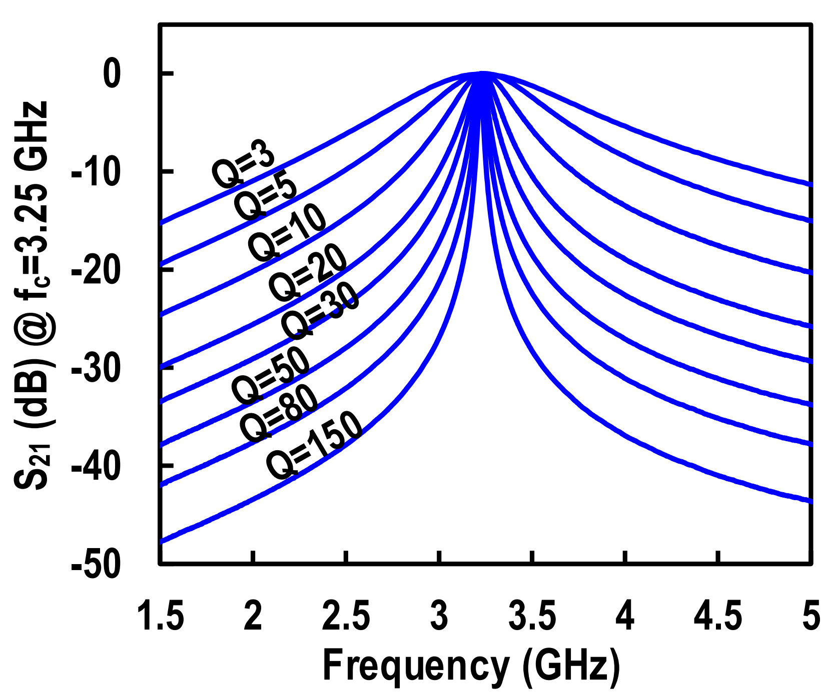



- 0.13 µm SiGe BiCMOS (IBM 8HP 1P7M process, fT/fmax=180/220 GHz).
- Chip size for BPF : 0.7 x 0.68 $mm^2$ (including pads).
- The silicon chip is measured after differential SOLT calibration with GSSG probes (calibration step: ~2 MHz).

# Measurement Results

## ❑ BPF Bandwidth & Q Tuning

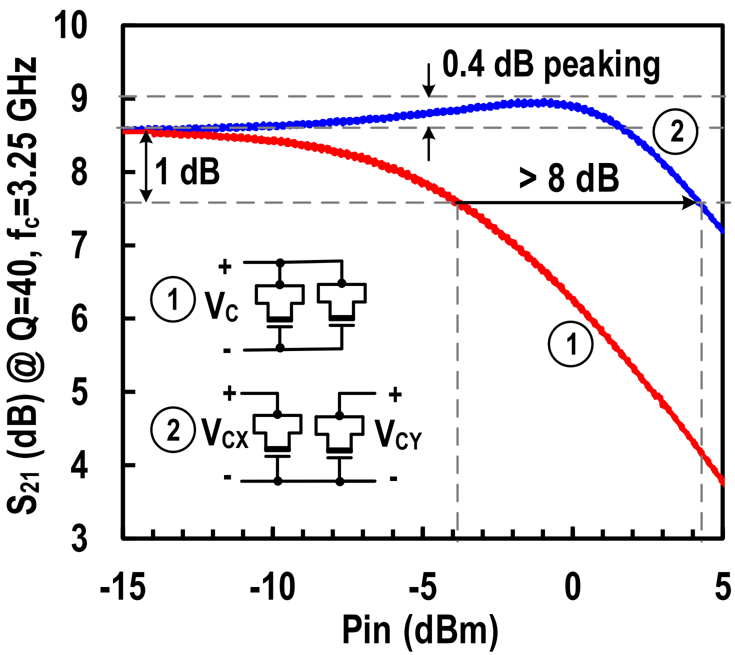


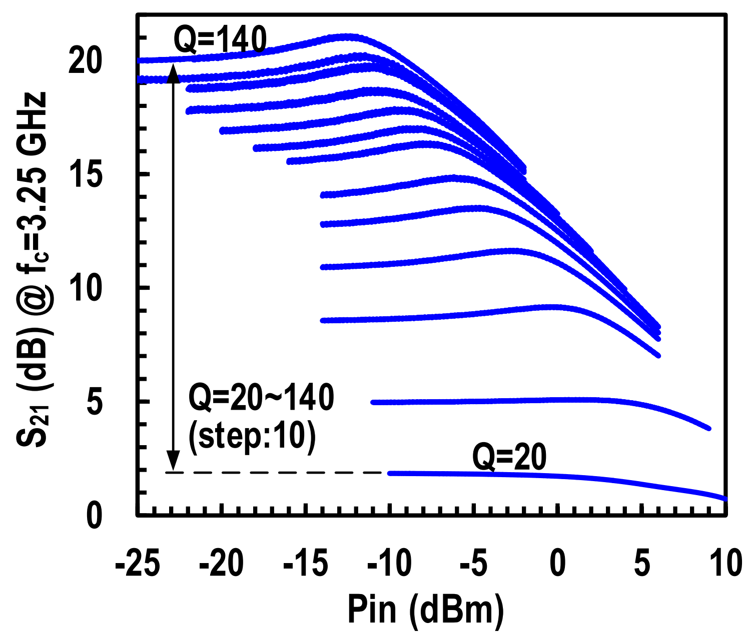




- Continuous frequency tuning over 2.25-4.5 GHz range.
- By controlling the negative resistance, the BPF Q increases up to 150.
- BPF bandwidth can be adjustable independent from frequency tuning.

# Measurement Results

## ❑ $IP_{-1dB}$ Improvement Using DVI Control and Negative Dynamic Resistance

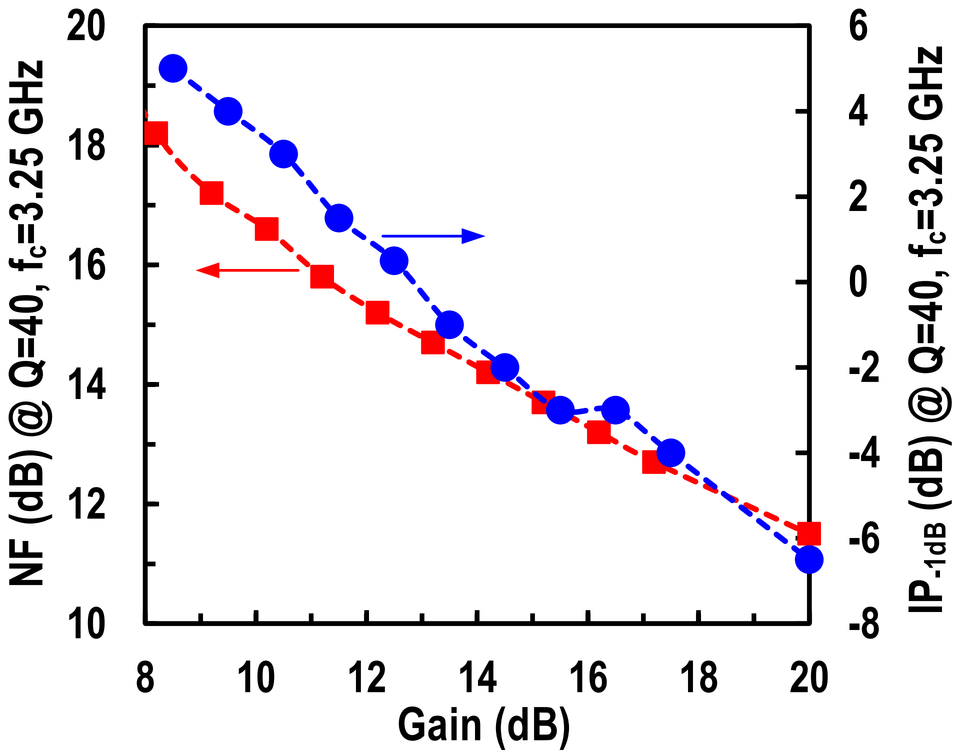


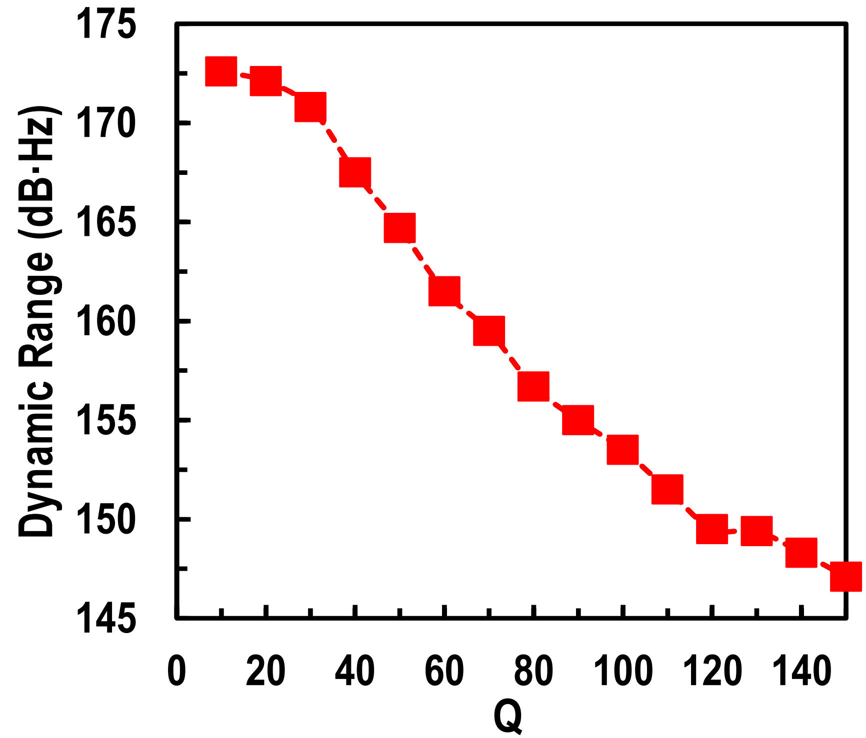

- $IP_{-1dB}$ improves with DVI control.
- Dynamic negative resistance introduces 0.5-1 dB gain peaking.
- Both DVI control & dynamic negative resistance improve $IP_{-1dB}$ >8 dB.
- A consistent 0.5-1 dB gain peaking for all Q ≥40.

# Measurement Results

## ❑ BPF NF & IP-1dB Versus Gain

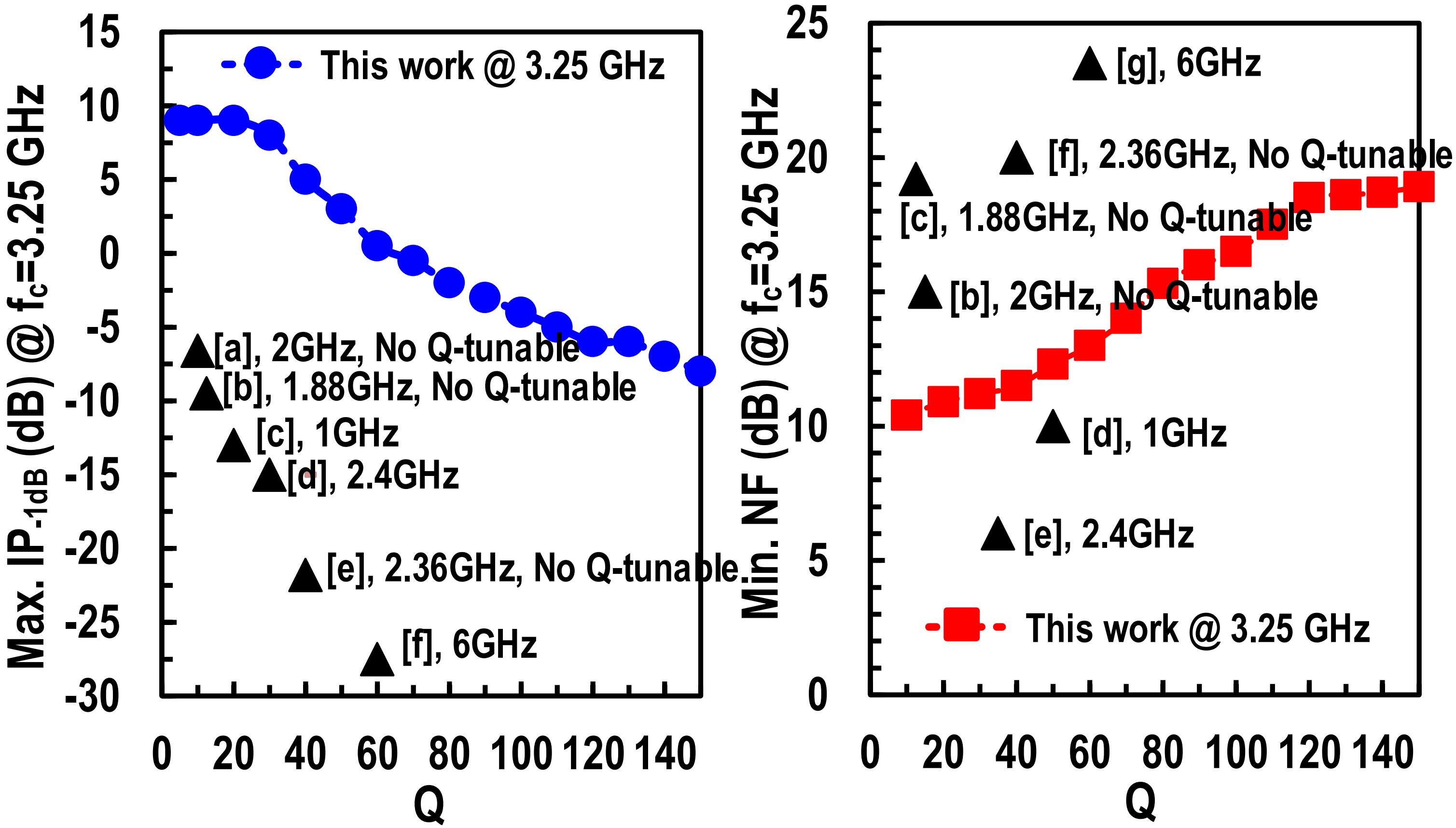



## ❑ Dynamic Range Versus Q




- BPF can work in either **low NF** or **high linearity** mode.
- NF ranges from 18~11 dB when gain increases by ~10 dB.
- $IP_{-1dB}$ +5 to -6 when gain increases from 8 to 20 dB.

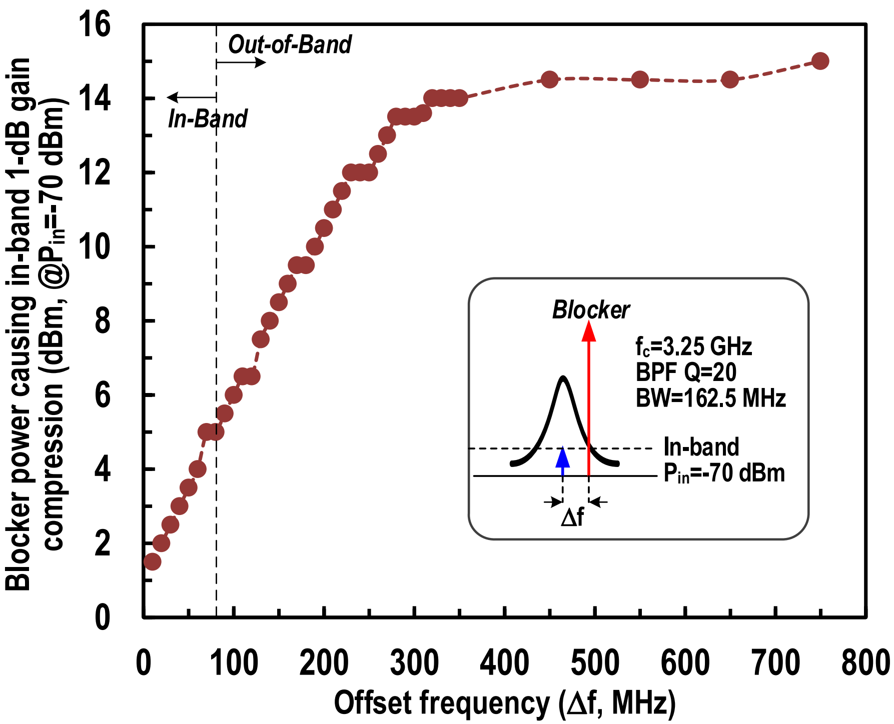
# Comparison with state of the arts

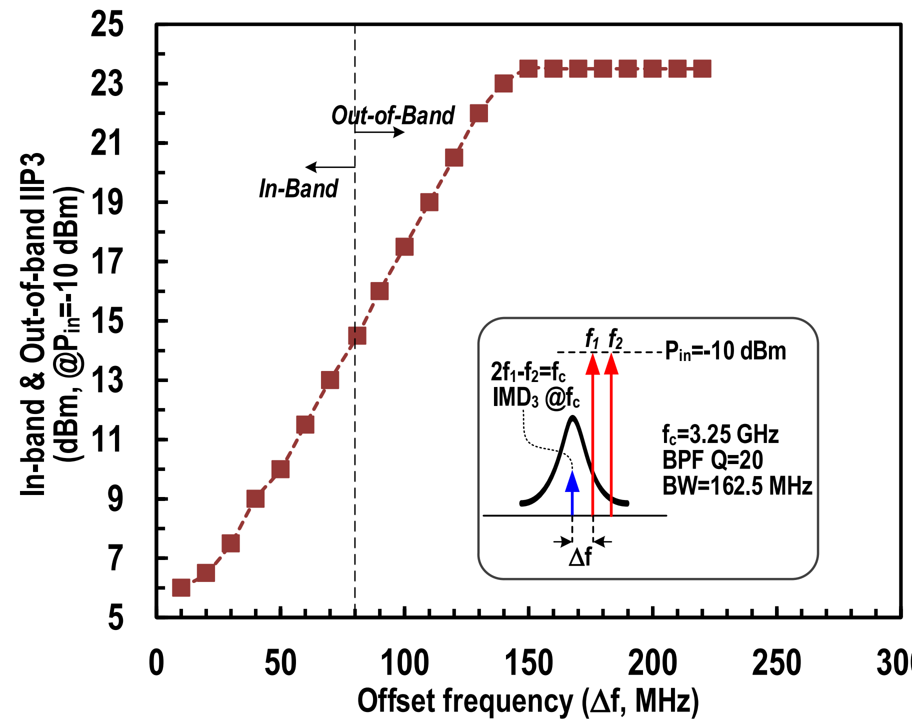



[a] B. Georgescu *et al.*, JSSC 2006; [b] D. Li *et al.*, JSSC 2002;
[c] S. Bantas *et al.*, TCAS-II 2004; [d] Xin He *et al.*, JSSC 2005;
[e] J. Kulyk *et al.*, JSSC 2006; [f] S. Li *et al.*, RFIC 2005

# Measurement Results

## ❑ BPF Out of Band Linearity Test



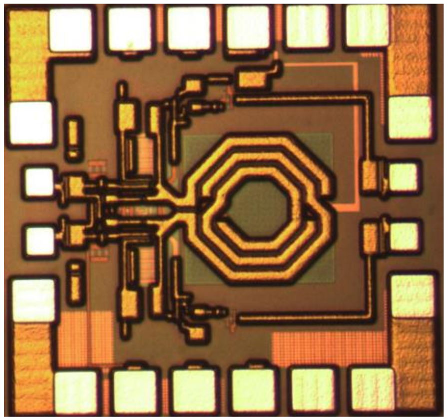

- When Q=20, typical in-band blocker $P_{-1dB}$ power ranges 1~5 dBm.
- OOB blocker $P_{-1dB}$ power at Δf=100 MHz is ~6 dBm and increases linearly as Δf increases until it reaches to ~15 dBm @ Δf=300 MHz.
- For the two-tone test, the in-band IIP3 is 6-15 dBm and it saturates to 23.5 dBm.

# Performance Summary

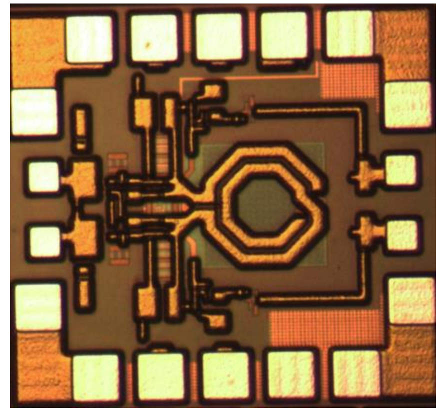
## Measured performance summary

| | | | | |
|---|---|---|---|---|
| Process | 0.13-$\mu$m SiGe BiCMOS ($f_t$=180 GHz) | | | |
| Filter type | 2nd – order Q-enhancement LC filter | | | |
| Frequency tuning | 2.25 ~ 4.5 GHz (2:1 tuning range) | | | |
| Q tuning | 3 ~ 150 | | | |
| Min. Gain (dB) @ $f_c$=3.25 GHz | 0 @Q=10 | 11 @Q=50 | 17 @Q=100 | 20.5 @Q=150 |
| NF (dB) @ $f_c$=3.25 GHz & 20 dB Gain | 10.4 @Q=10 | 12.5 @Q=50 | 16.5 @Q=100 | 18.5 @Q=150 |
| $IP_{-1dB}$ (dBm) @$f_c$=3.25 GHz & Min. Gain | 9 @Q=10 | 3 @Q=50 | -4 @Q=100 | -8 @Q=150 |
| Normalized dynamic range (dB· Hz) | 172.6 @Q=10 | 164.5 @Q=50 | 153.5 @Q=100 | 147.5 @Q=150 |
| OOB $P_{-1dB}$ blocker power (dBm) @Q=20 | 6 @$\Delta$f=100 MHz | 10.5 @$\Delta$f=200 MHz | 13.5 @$\Delta$f=300 MHz | 15 @$\Delta$f=400 MHz |
| OOB $IIP_3$ (dBm) @Q=20 | 17.5 @$\Delta$f=100 MHz | | 23.5 @$\Delta$f=200 MHz | |
| DC current (mA) (Vcc=3.3 V) | 13 ~ 20 (without output 50-$\Omega$ driver), 22 ~ 29 (with output 50-$\Omega$ driver) | | | |
| Die area | 0.7 x 0.68 $mm^2$ | | | |

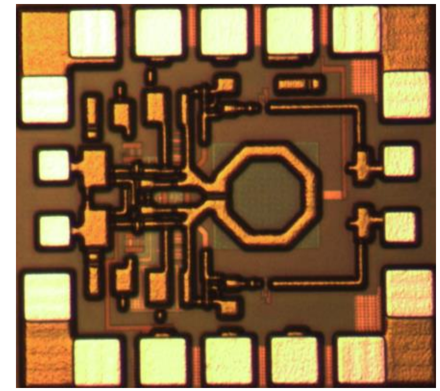
# Implementation @ Higher Frequencies



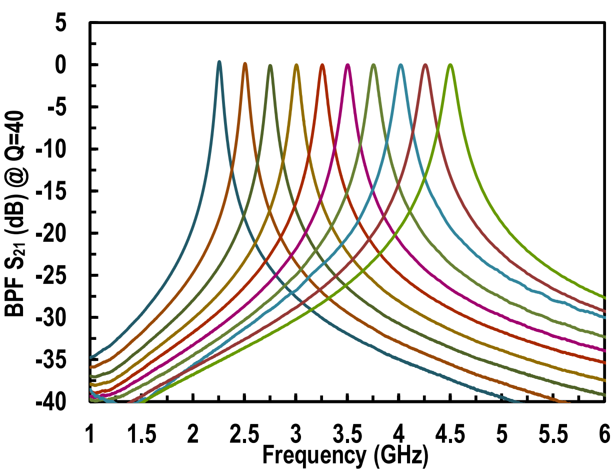
2.25-4.5 GHz

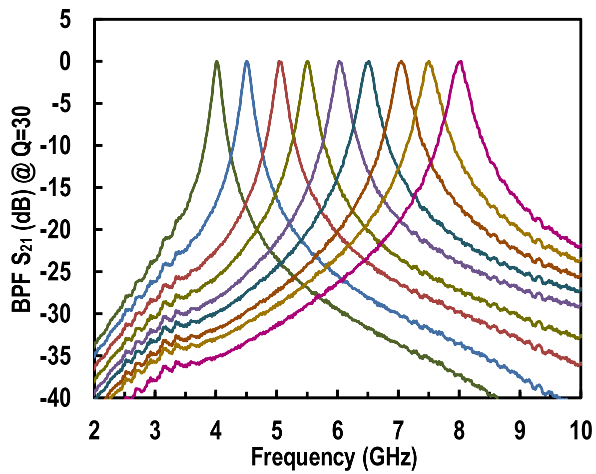


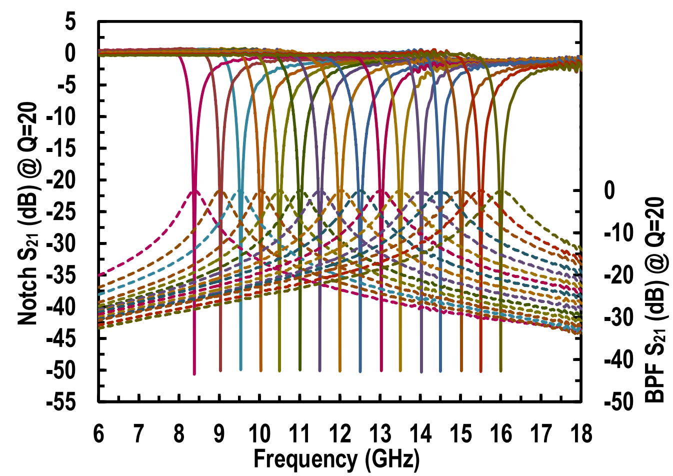
4-8 GHz



8-16 GHz



# Conclusion & Performance Summary

- Q-enhancement LC bandpass filter in 0.13 μm SiGe BiCMOS.
- Achieved wide continous turning range of **2.25~4.5** GHz with independent **Q control up to 150** over the overall frequency range.
- Dual-mode driving **voltage-mode** (low-gain) and **current-mode** (high-gain) drivers allows more flexible operation in the noise and linearity tradeoff space.
- The proposed **dual varactor inverse (DVI)** control can suppress varactor nonlinearity substantially.
- The **gain peaking technique** enabled by a dynamic negative resistance circuit effectively increase the filter's power handling capability further.
- DVI control and gain peaking result in exceptional level of **170~150 dB·Hz** of normalized filter dynamic range when **Q varies from 10 to 100**.

# Acknowledgement

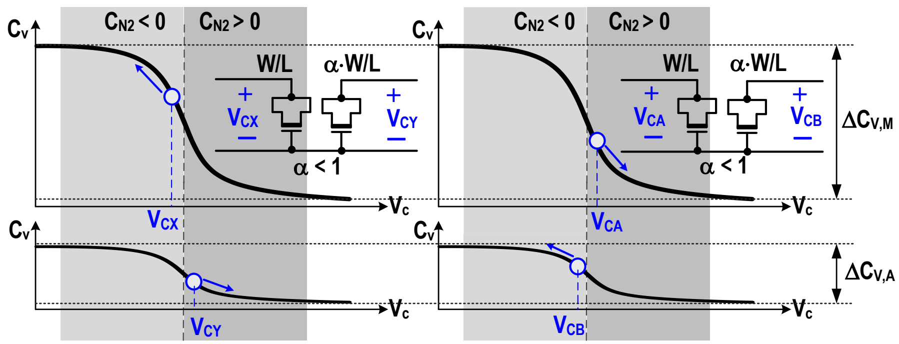

- The authors would like to thank RFIC Design Center (Director: Mr. Kenneth Schulz), Lockheed Martin, for the silicon chip fabrication.

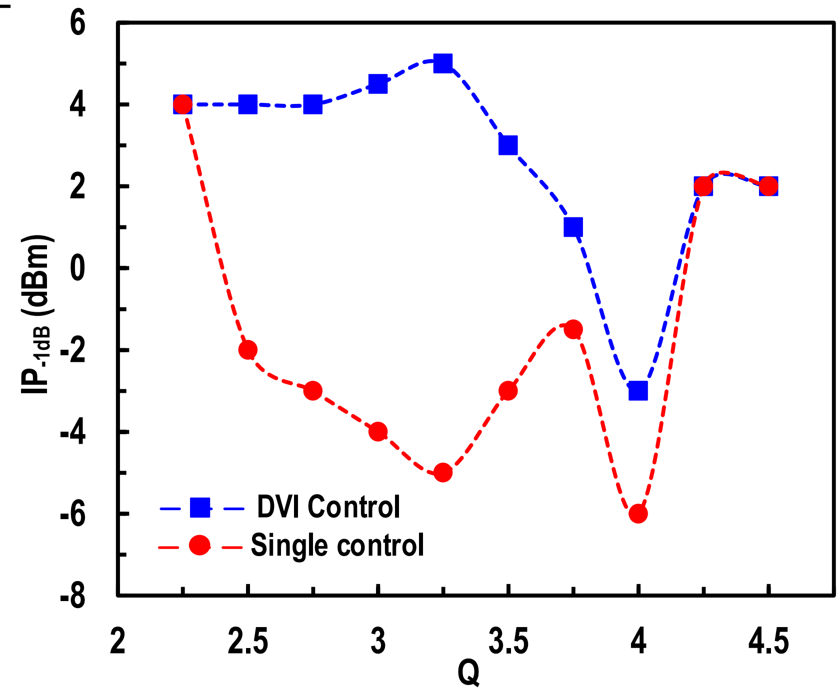
- The authors also thankfully acknowledge the help in the measurement equipment from the Electrical and Computer Engineering (ECE) Instructional Lab, Virginia Tech (Director: Dr. Dennis Sweeney).

# Back-up

# BPF Circuit Design

## ❑ Dual Varactor Inverse (DVI) Control



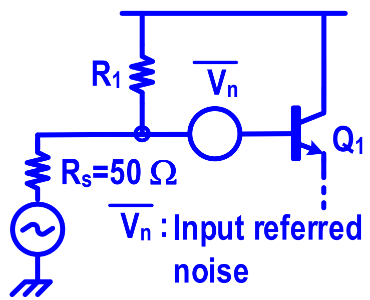




## DVI Control

- The polarity of $C_{N2}$ changes in the middle.
- $C_V$ and $C_A$ move in the opposite direction.
- Substantial cancellation of varactor nonlinear coefficients.
- Increasing $IP_{-1dB}$ by~10 dB.

# Input Matching Effect

## ❑ Input 50 Ω Matching

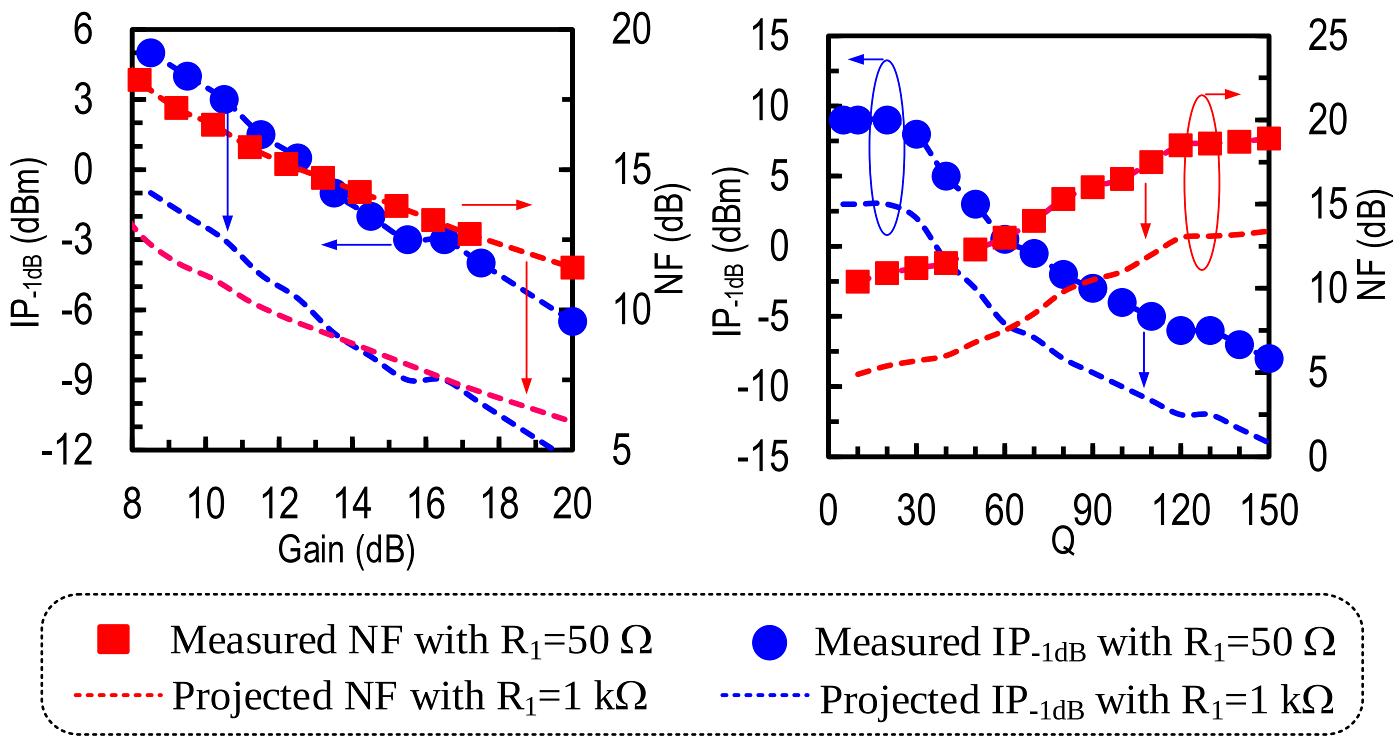



**With $R_1$=50 Ω (Z-matching)**

① $F = 2 + \frac{\overline{V_n^2}}{4KTR_s} \times 4$

**With $R_1$=1 kΩ**

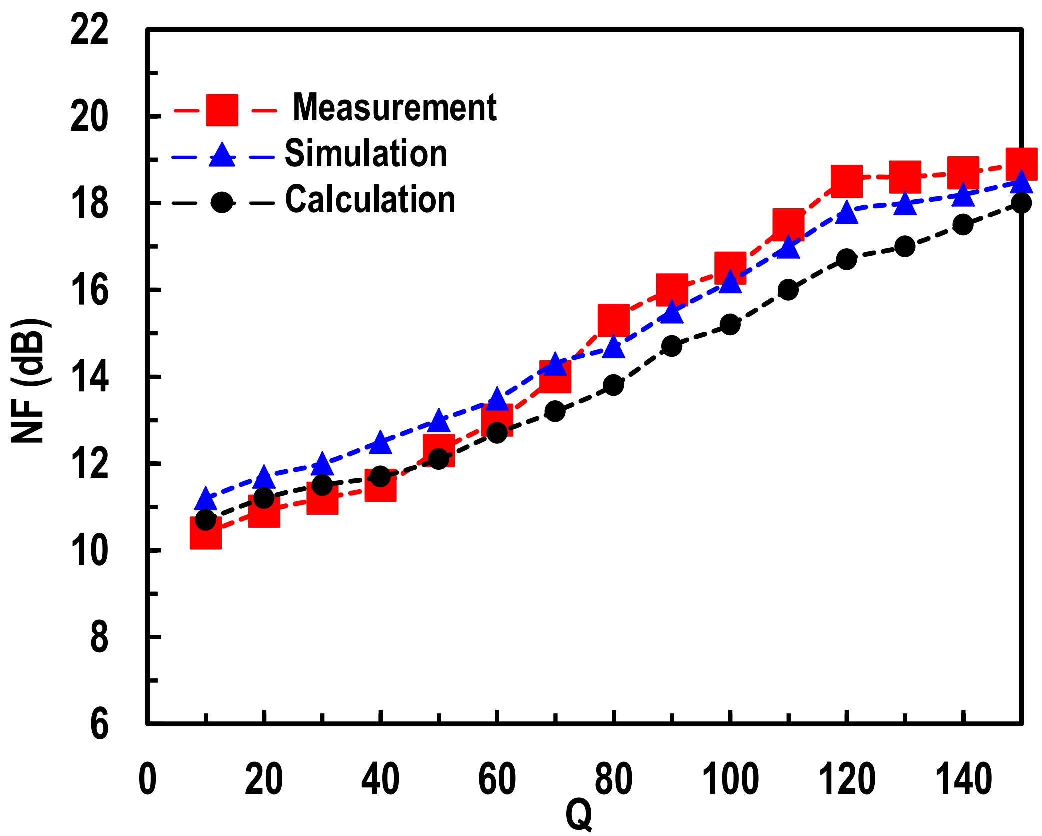
② $F = 1 + \frac{\overline{V_n^2}}{4KTR_s}$




## DVI Control

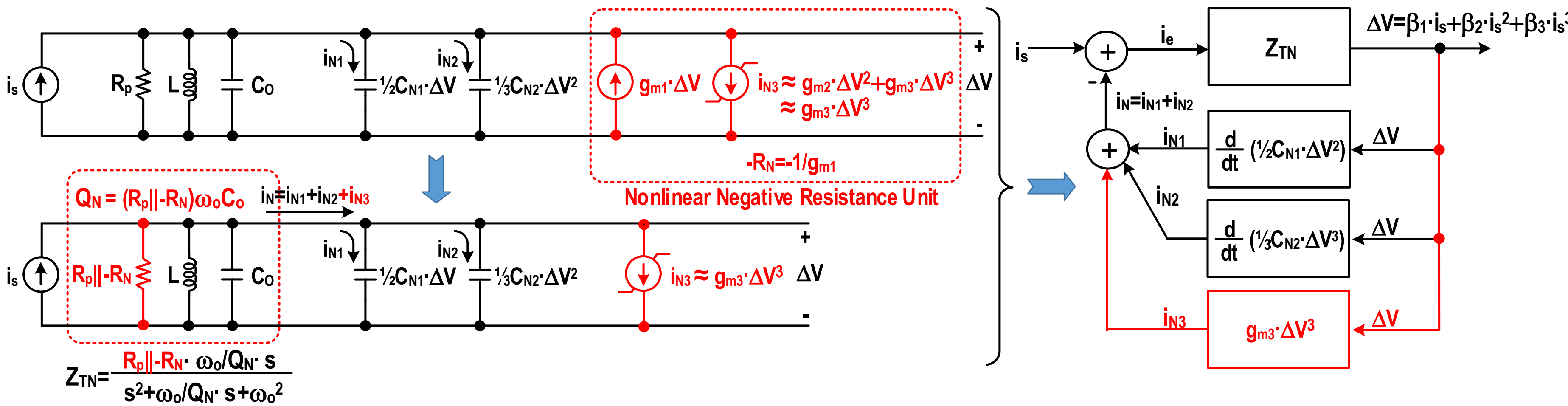
- Q=40 for all cases.
- With high impedance matching ($R_l$=1k) NF would be 5-6 dB lower.
- Linearity would degrade by 5-6 dB.

# Design Trend




$$NF \approx 1 + 1 + (0.08) \cdot \left( \underbrace{r_b + \frac{Q\sqrt{L/C}}{2A_v}}_{\text{Current Driver}} + \underbrace{\frac{\gamma(g_{m3} + g_{ds3})}{4{A_v}^2} \cdot Q^2 \cdot \frac{L}{C}}_{\text{Negative Resistance}} \right)$$

# Design Trend



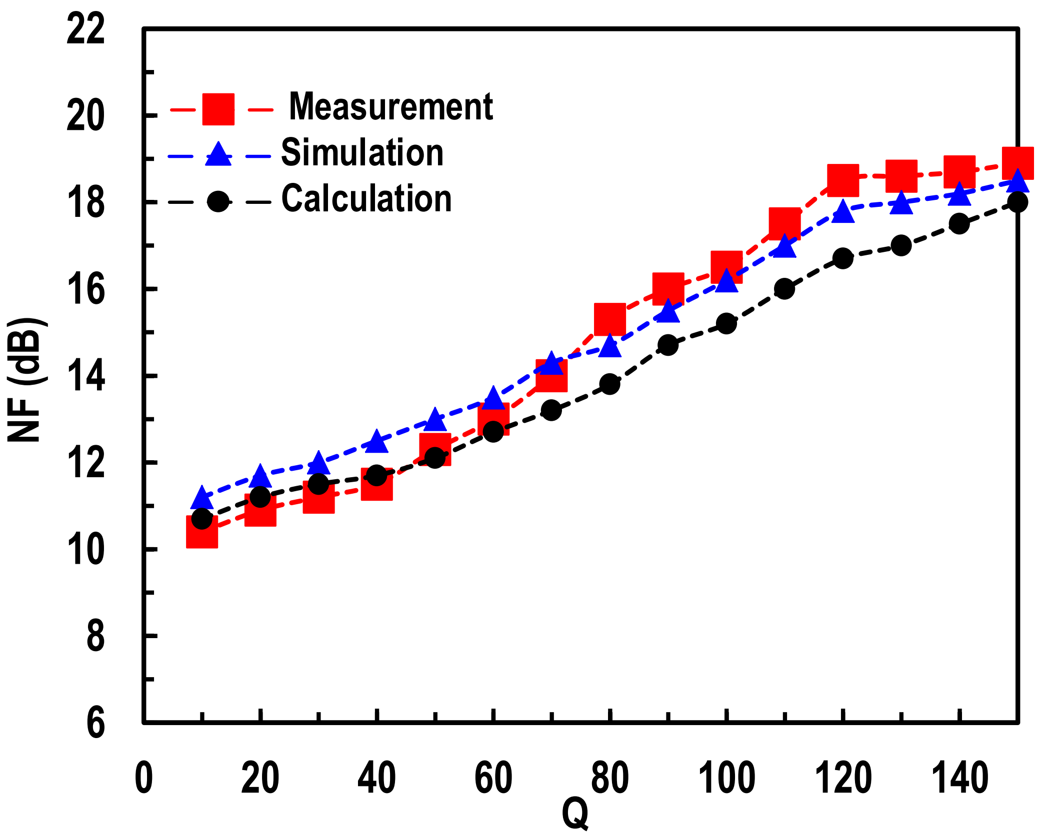

- Major nonlinearity comes fro **varactor** and negative resistance.
- We can intuitively model the nonlinearity as a feedback.

# Design Trend

$$A_v = \frac{G_{m2}}{2} \cdot Q\sqrt{L/_C}$$

$$\frac{1}{G_{m2}} = \frac{Q\sqrt{L/_C}}{2A_v}$$

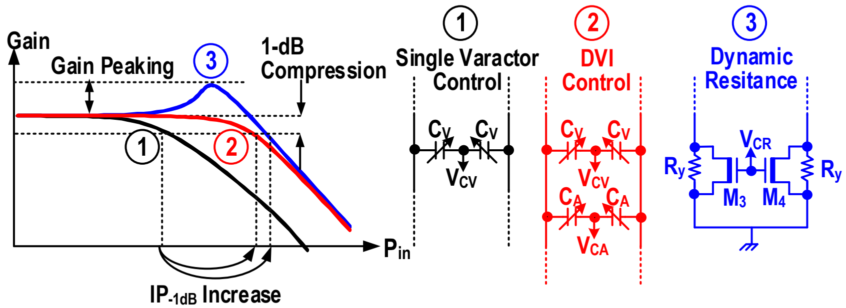
$$G_{m2} = \frac{g_{m2}}{1 + \ g_{m2}R_E} = \frac{1}{r_{m2} + \ R_E}$$

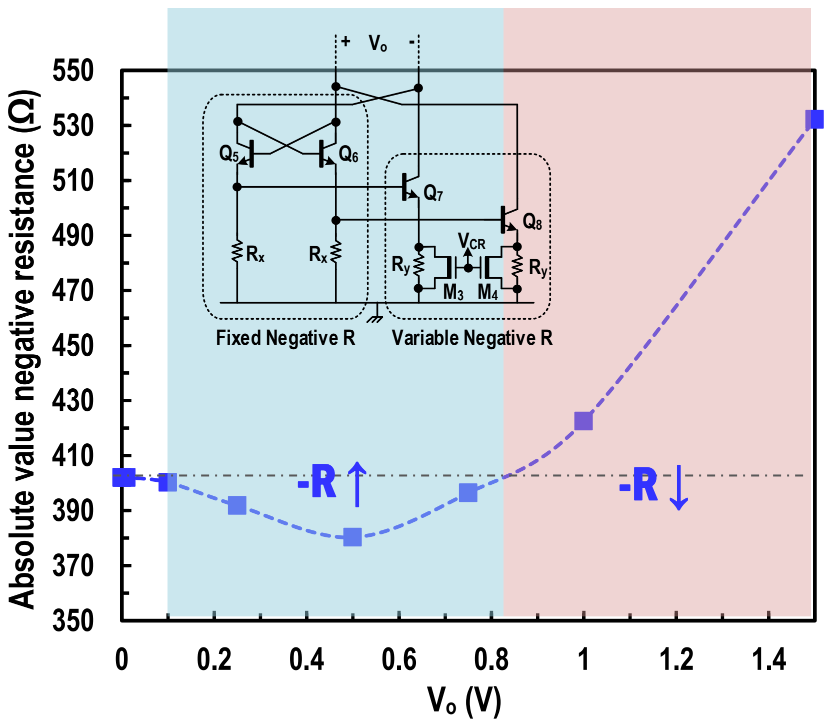


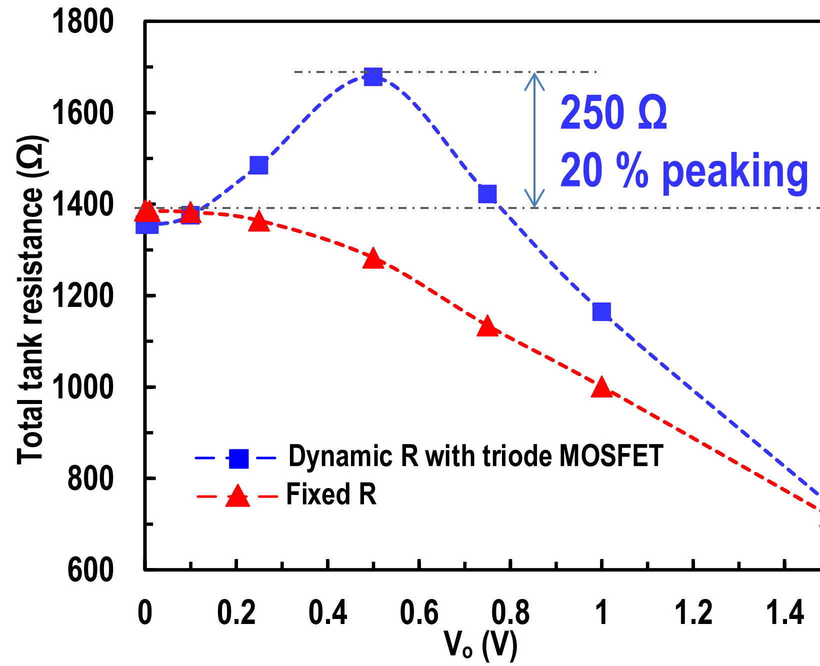

$$NF \approx 1 + 1 + (0.08) \cdot \left( r_b + \frac{Q\sqrt{L/_C}}{2A_v} + \frac{\gamma(g_{m3} + \ g_{ds3})}{4{A_v}^2} \cdot Q^2 \cdot \frac{L}{C} \right)$$

# BPF Circuit Design

## ❑ LC-Resonator with Dynamic Negative Resistance




## Negative Resistance @ 3.25 GHz

- More Negative R @ 0.1 to 0.82 V.
- Overall tank resistance increases.