A 200 MS/s 98-dB SNR Track-and-Hold in 0.25-um GaN HEMT

SungWon Chung[1,2] and Hae-Seung Lee[1]

[1]Massachusetts Institute of Technology

[2]University of Southern California

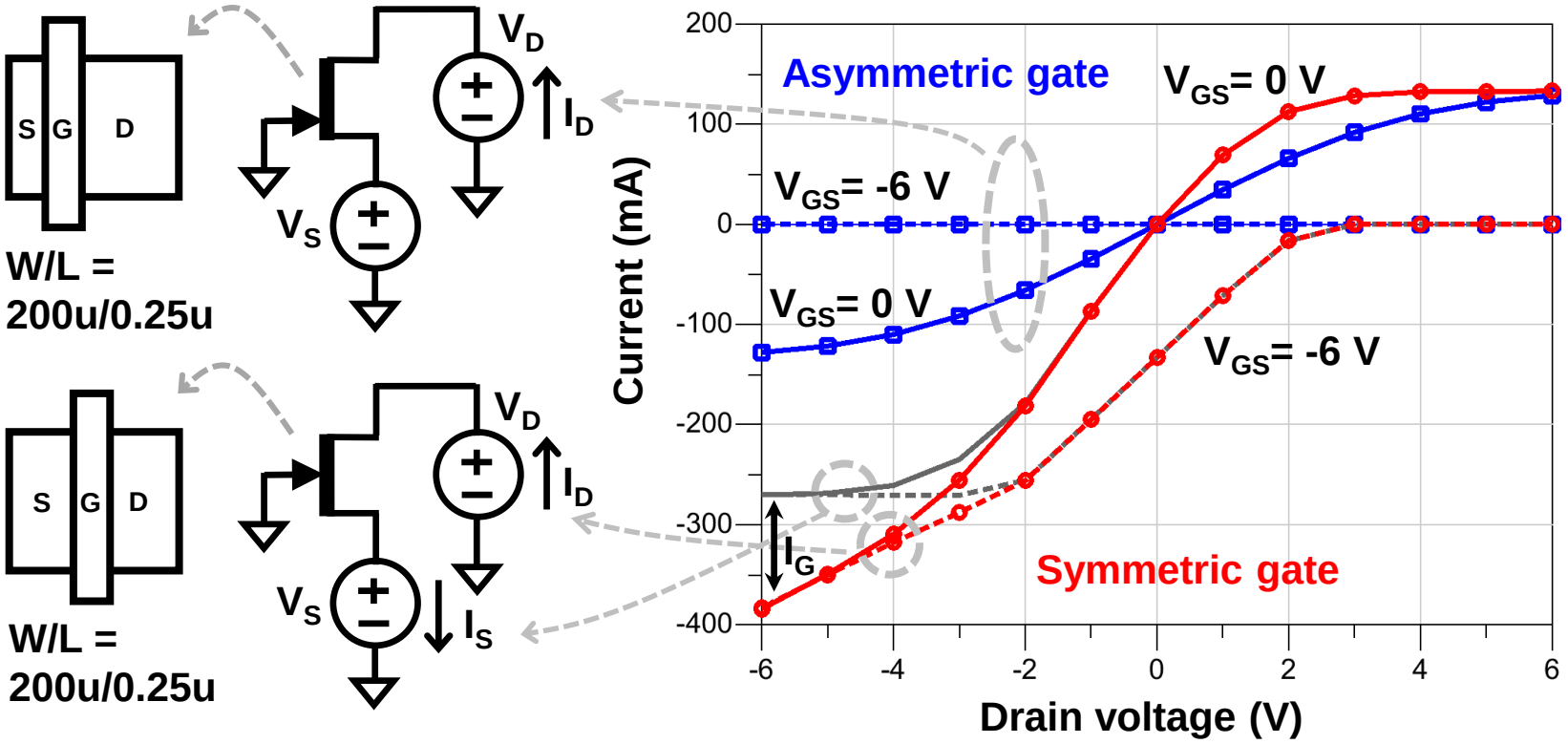
Outline

- **Motivation: Ultra High SNR**
- **GaN HEMT T/H Design Challenge**
- **Proposed Two-Stage GaN HEMT T/H**
- **Measurement Results**

Motivations

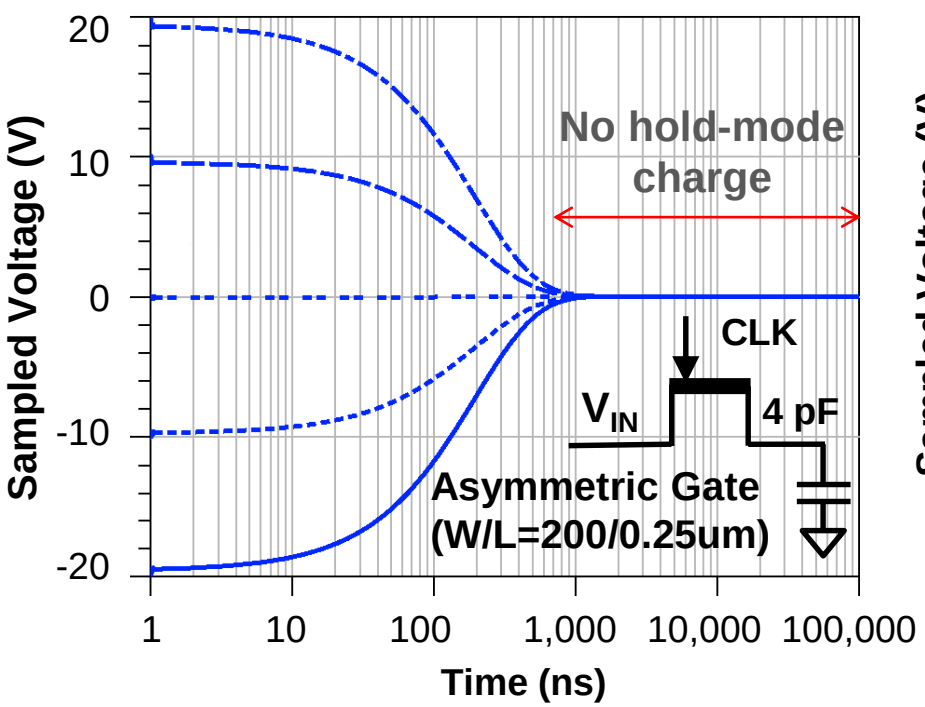
- **Track-and-Hold (T/H) for future GaN ADCs with *large signal* range**
- **High supply voltage capability of GaN provides *ultra high SNR***
- **High speed capability of GaN provides *high bandwidth***
- **Digital post-processing can significantly suppress *distortion***

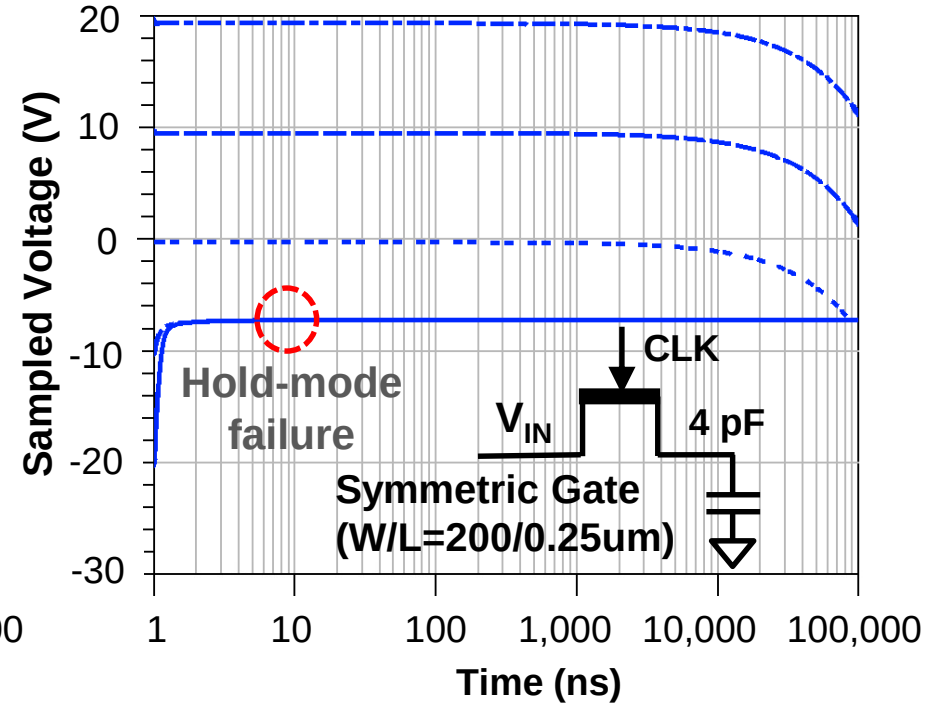
Schottky Junction in GaN HEMT



- **Gate-source junction has a built-in Schottky diode**
- **Large gate current introduces permanent damage**

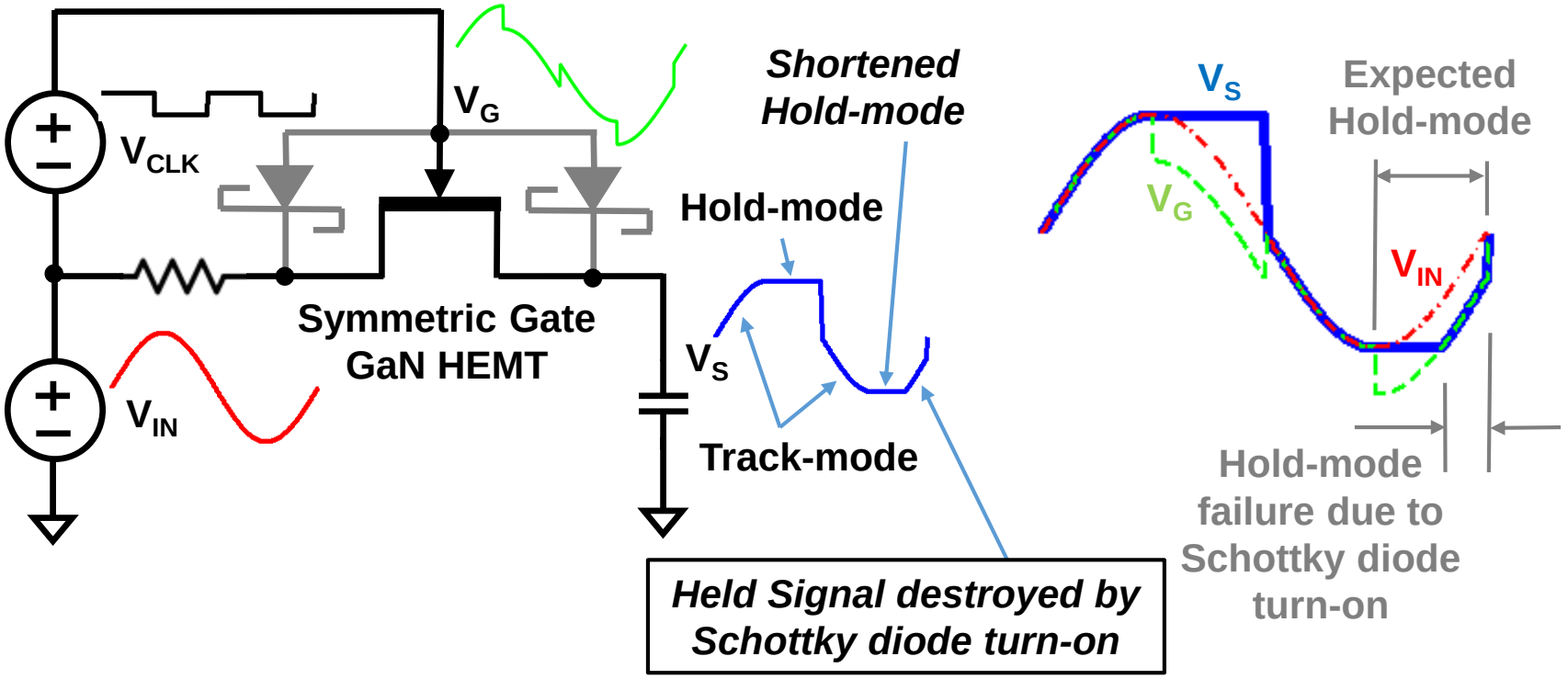
Leakage Current in GaN HEMT





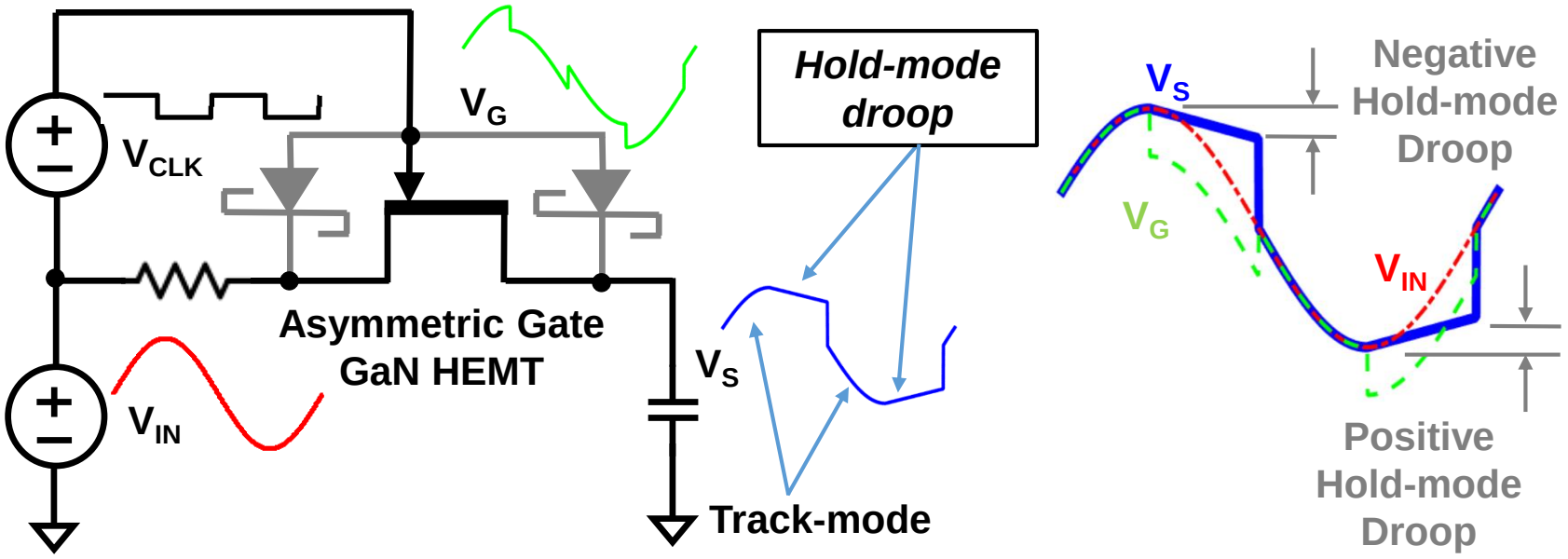
- **1000x smaller leakage current with symmetric gate**
- **Symmetric devices require a larger clock swing**

Gate-Bootstrapping in GaN HEMT with a *Symmetric* Gate



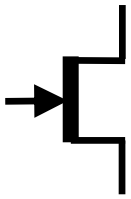
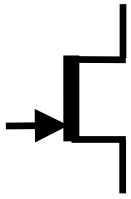
- **Very large clock signal swing is required to avoid Schottky diode turn-on**

Gate-Bootstrapping in GaN HEMT with an *Asymmetric* Gate



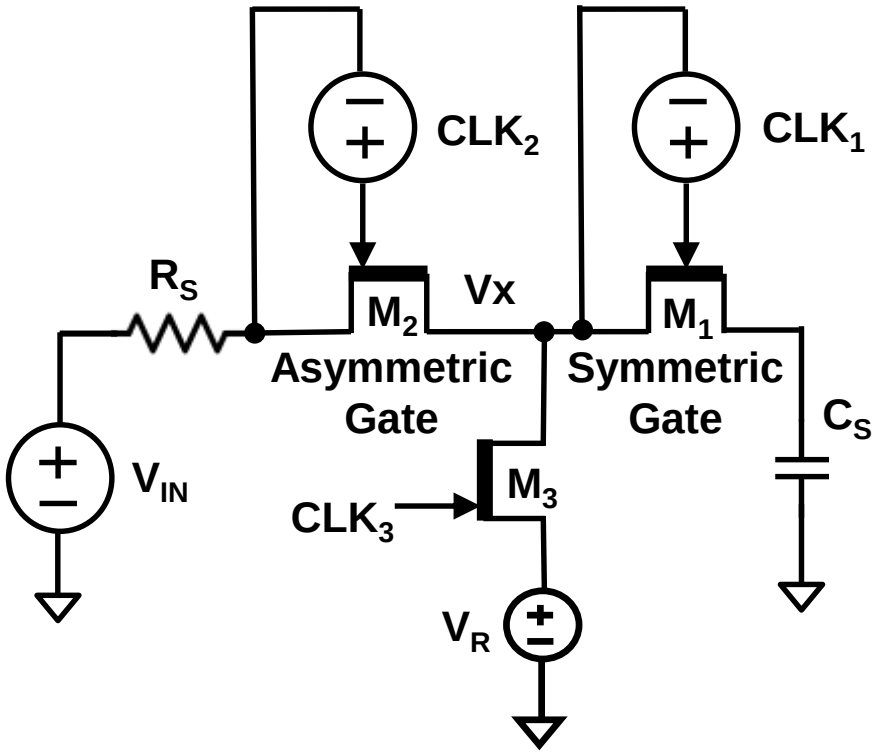
- **Hold-mode droop is significant due to the large leakage current**

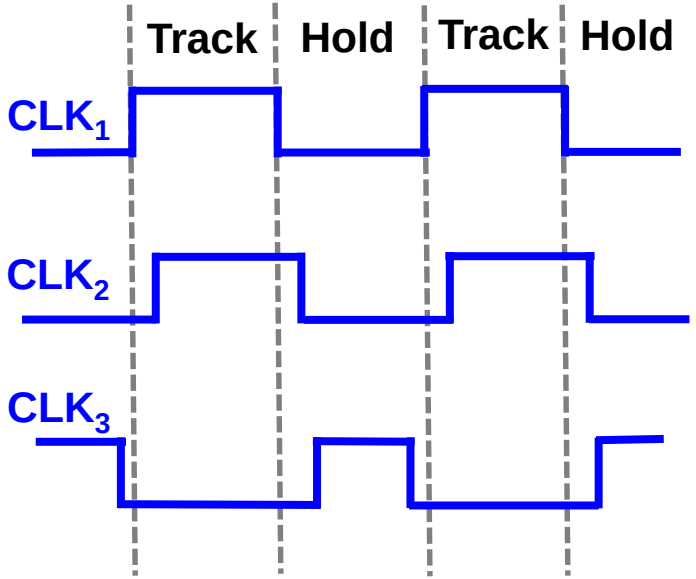
Gate-Bootstrapping GaN HEMT T/H Design Challenges

GaN HEMT Sampling Switch Type	**Leakage Current**	**Schottky Turn-on Voltage** (gate-drain)
Symmetric 	Small → **Small Droop**	Small → High Swing CLK
Asymmetric 	Large → Large Droop	Large → **Low Swing CLK**

- **Challenging to allow "*small hold-mode droop*" and "*low swing sampling clock*" at the same time**

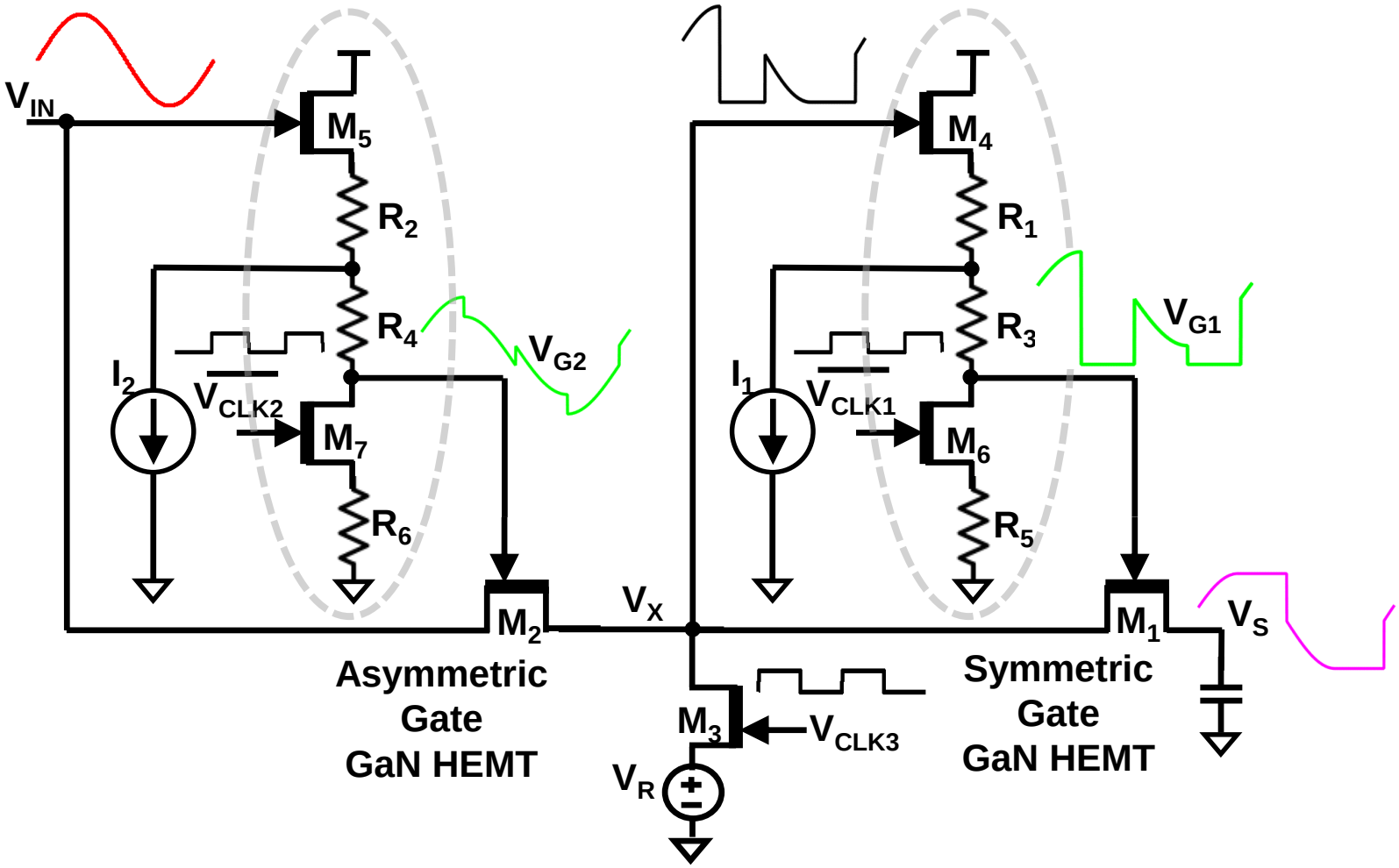
Proposed 2-Stage GaN HEMT T/H





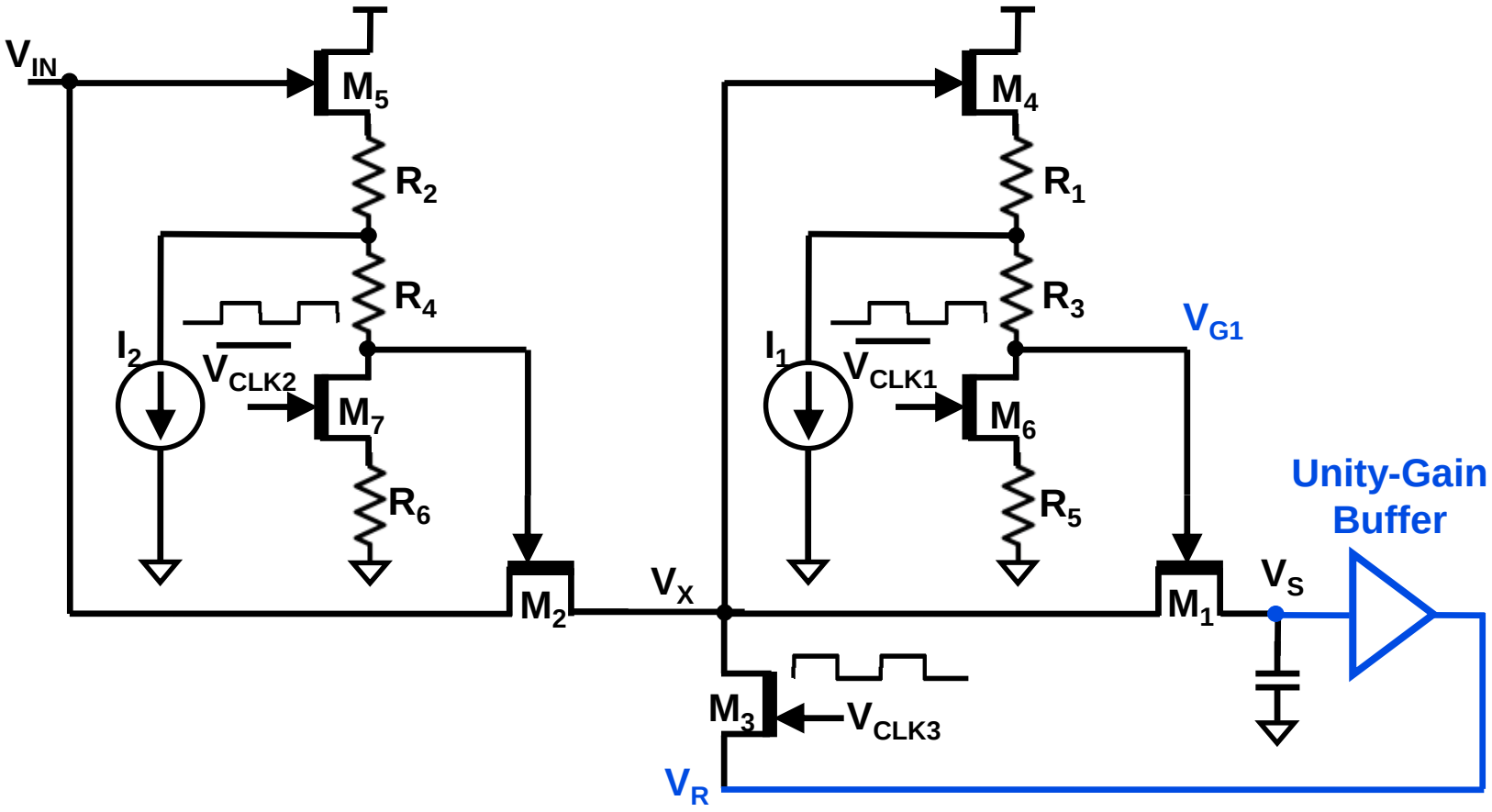
- **Takes the advantage of symmetric & asymmetric devices → Allows Small droop & Low swing clock**

N-type GaN HEMT Implementation



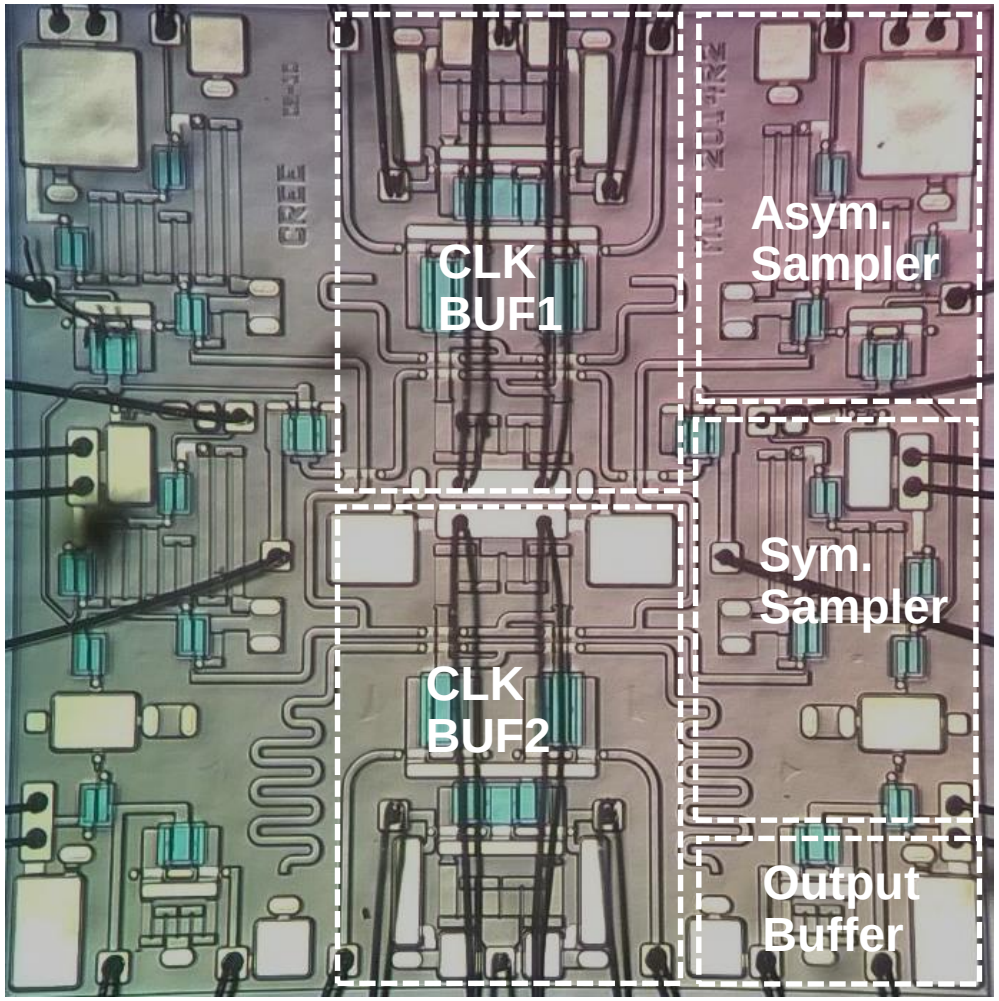
- Switched source follower for gate-bootstrapping
- Most current consumption during hold-mode

Low-Power Operation



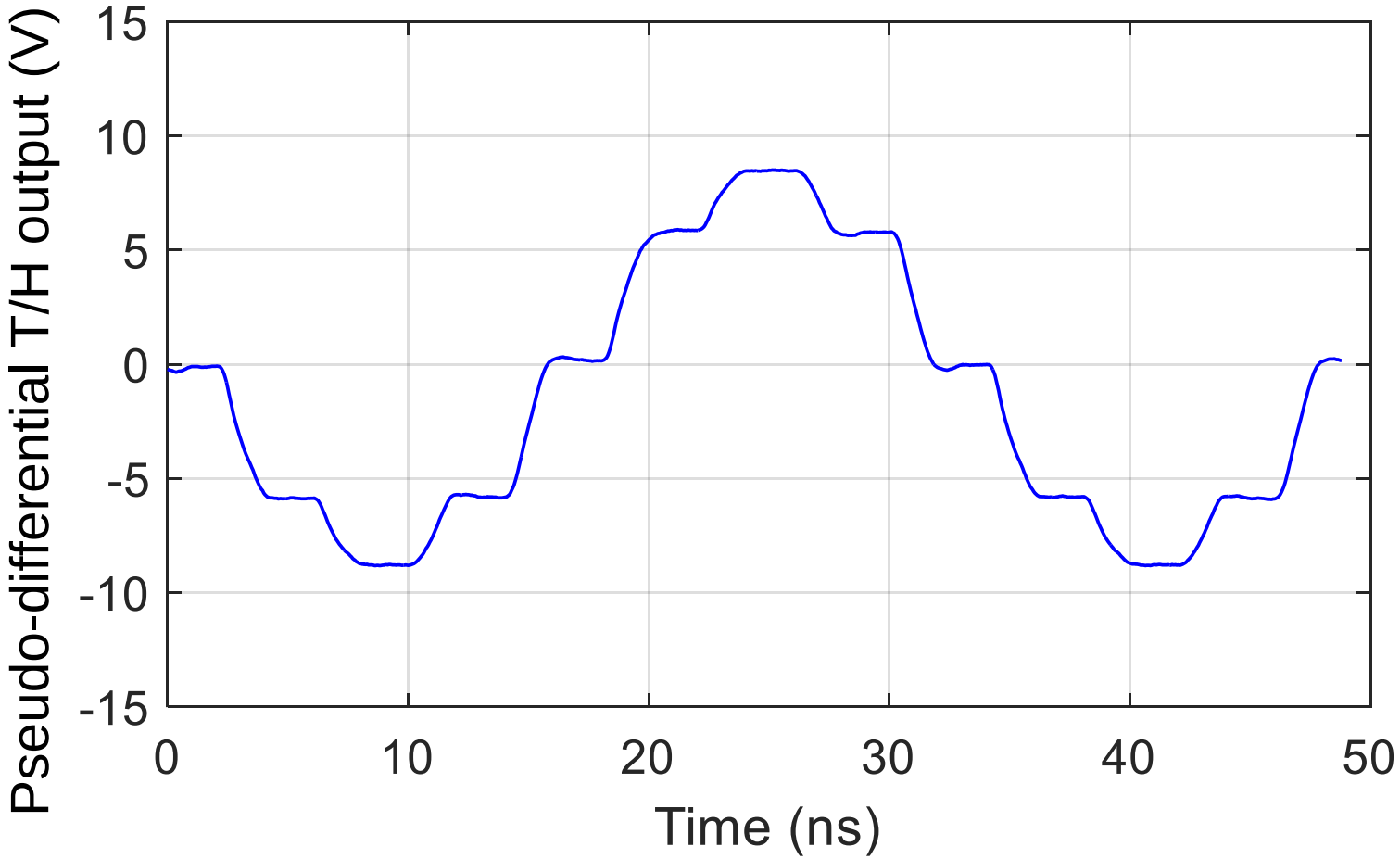
- **Feedback generation of V_R in order to reduce the voltage swing of the gate-bootstrapping clock V_{G1}**

2-Stage GaN HEMT T/H Test Chip



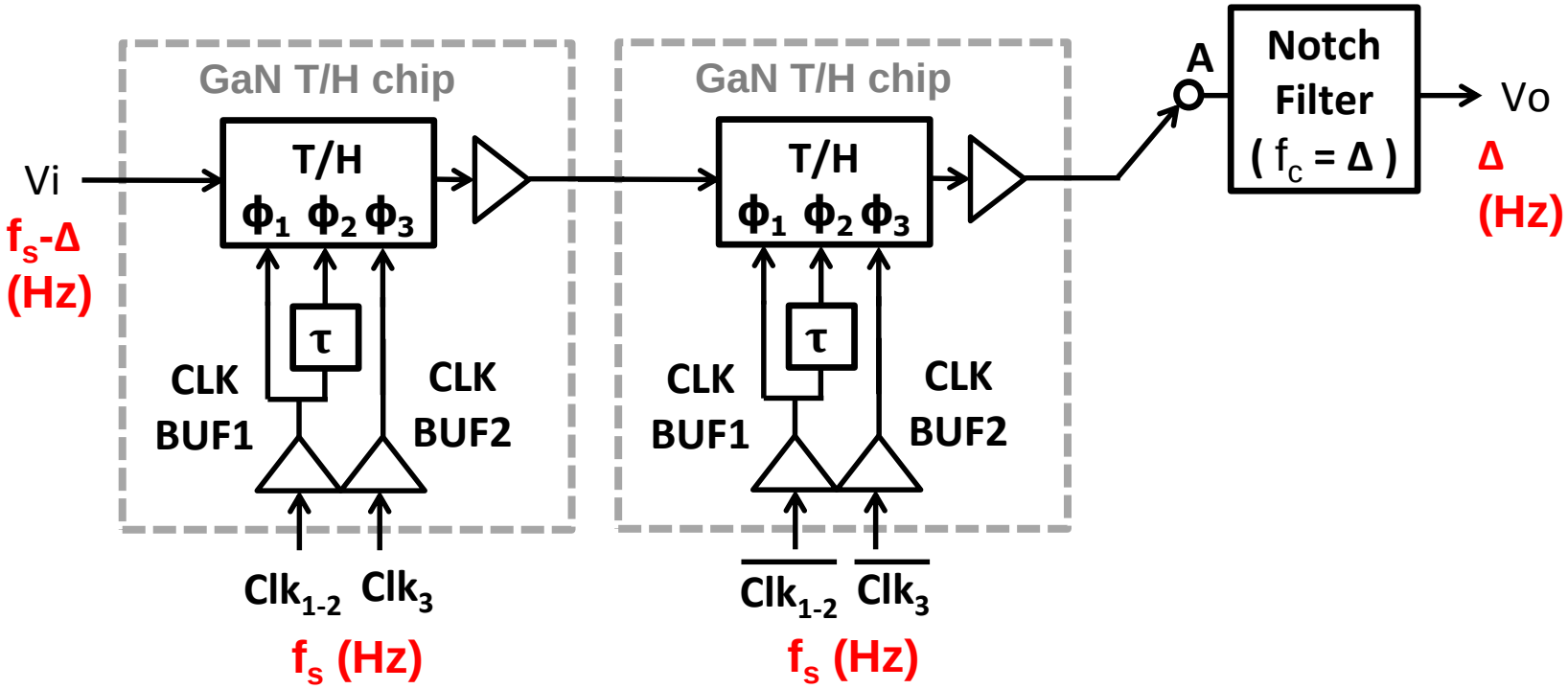
Process	250nm GaN-on-SiC
f_t	10 GHz
Supply	28 V
Size	3 mm x 3 mm
Input	24 V_{pp} p-differential
C_{sample}	6 pF
$f_{sample,\ max}$	250 MHz
BW	240 MHz (track-mode)
Current	55 mA (T/H core)

Measured T/H Transient Output



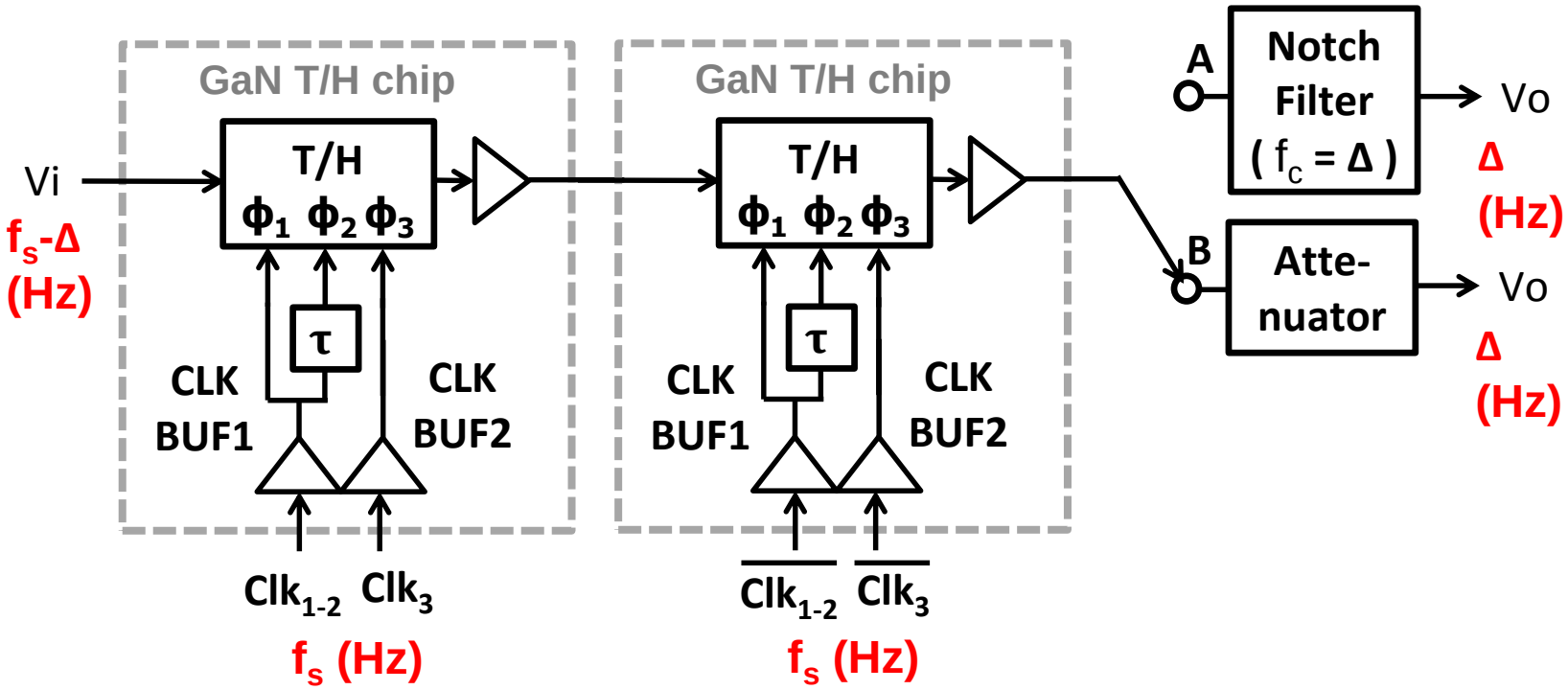
- **250 MS/s with 22-V_{pp} pseudo-differential input**

Over 100-dB SNR Measurement on 24-V_{pp} Differential Signal



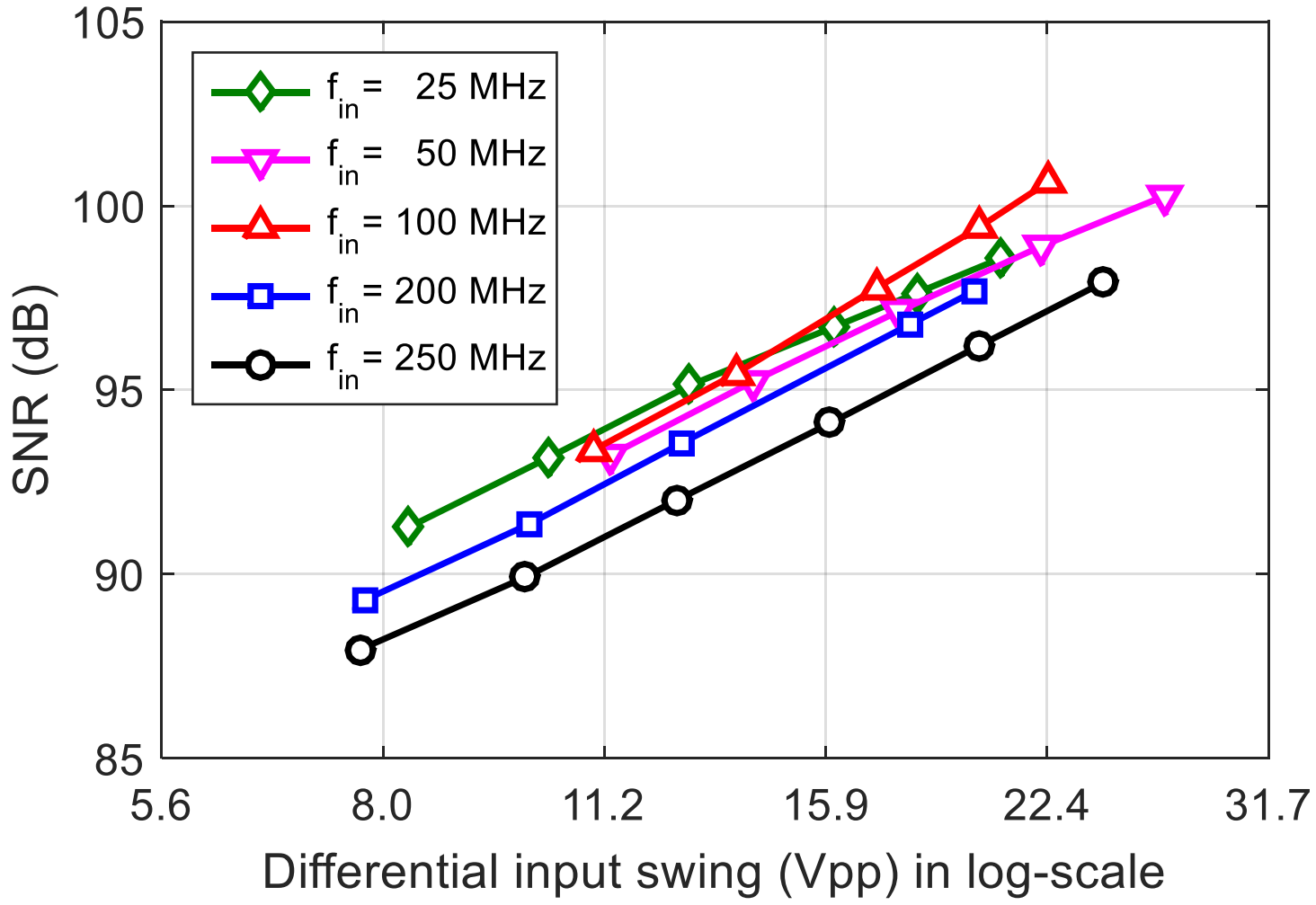
- **Step 1 : Noise floor measurement with notch filter**

Over 100-dB SNR Measurement on 24-V_{pp} Differential Signal



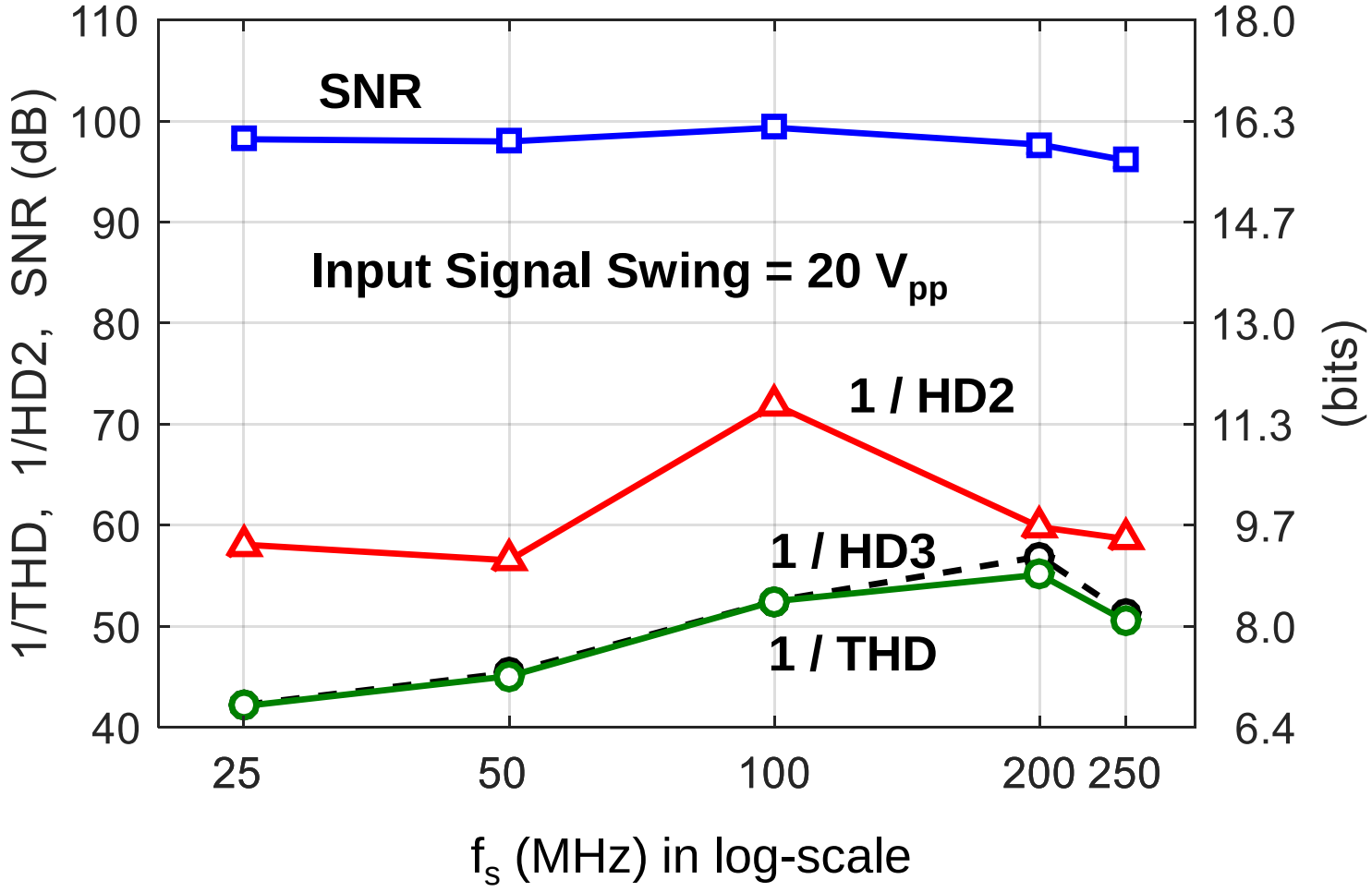
- Step 1 : Noise floor measurement with notch filter
- **Step 2 : Dynamic range measurement with attenuator**

Measured Signal-to-Noise Ratio



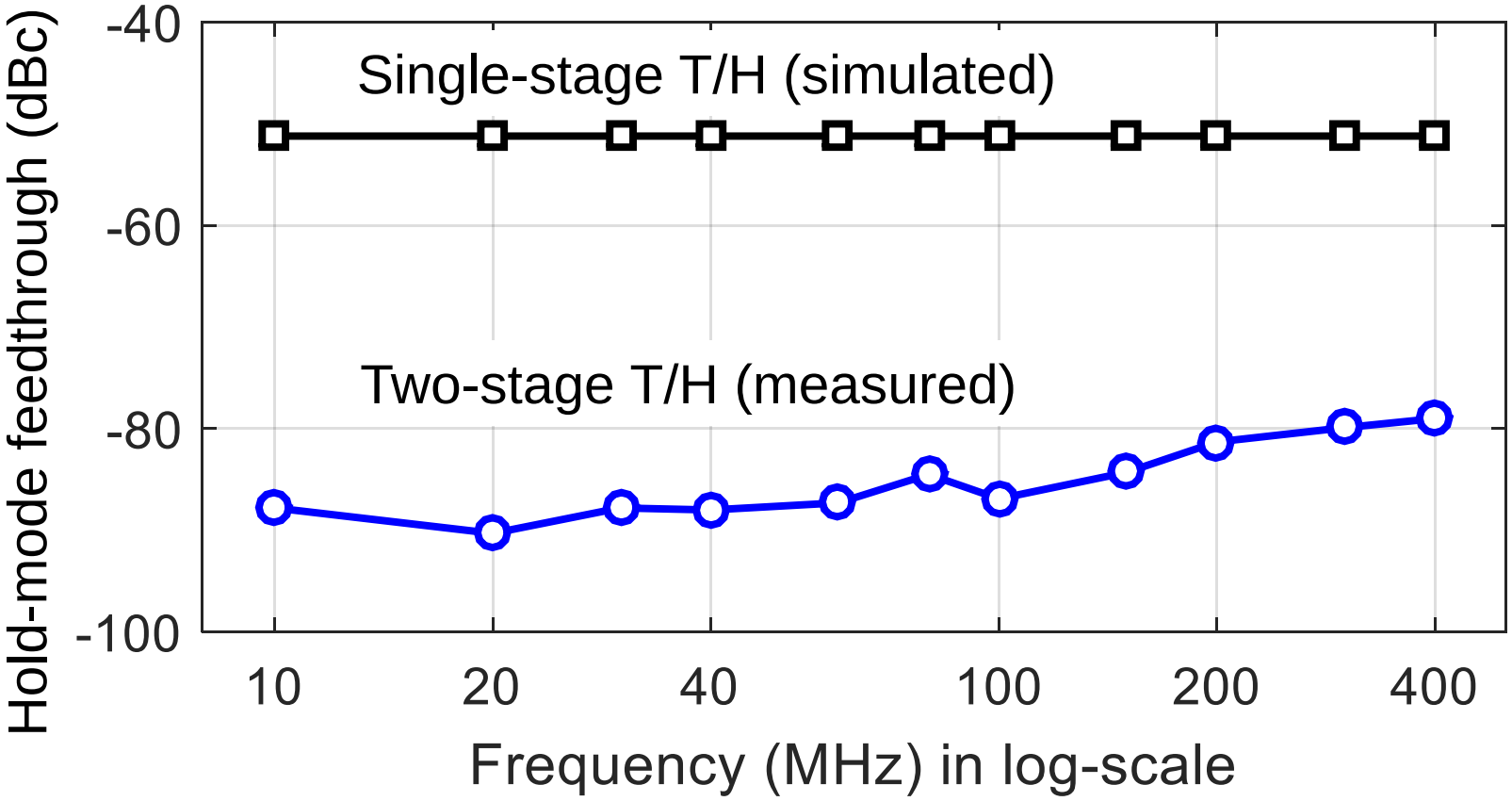
- **101.7-dB peak SNR at 100.1 MS/s with 100-MHz input**

Measured Linearity



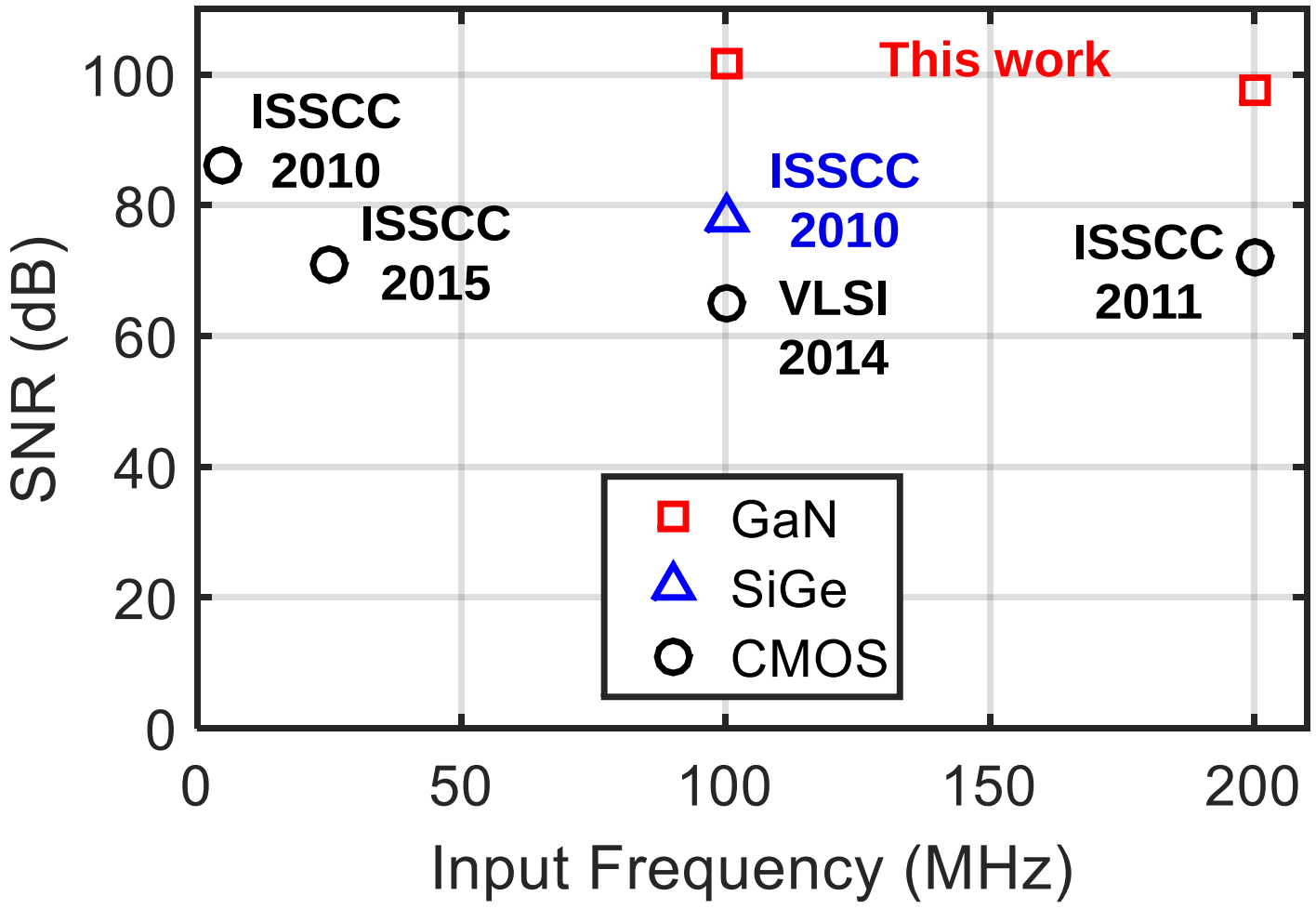
- **Linearity can be improved by digital post-processing**

Measured Feedthrough



- **More than 30-dB improvement with 2-stage design**

Comparison of High-SNR T/H



Summary

- **Implemented a 2-stage GaN HEMT T/H sampler for low-power and low-leakage operation**
  - **Asymmetric gate transistor in the 1st stage for the low power operation of the 2nd stage**
  - **Symmetric gate transistor in the 2nd stage for low leakage operation**
- **Demonstrated the highest reported bandwidth-SNR product enabled by a large signal swing**
  - **101.7-dB SNR with 100-MHz 24-V_{pp} pseudo-differential input signal sampled at 100.1 MS/s**