# Materials Challenges for III-V/Si Co-integrated CMOS

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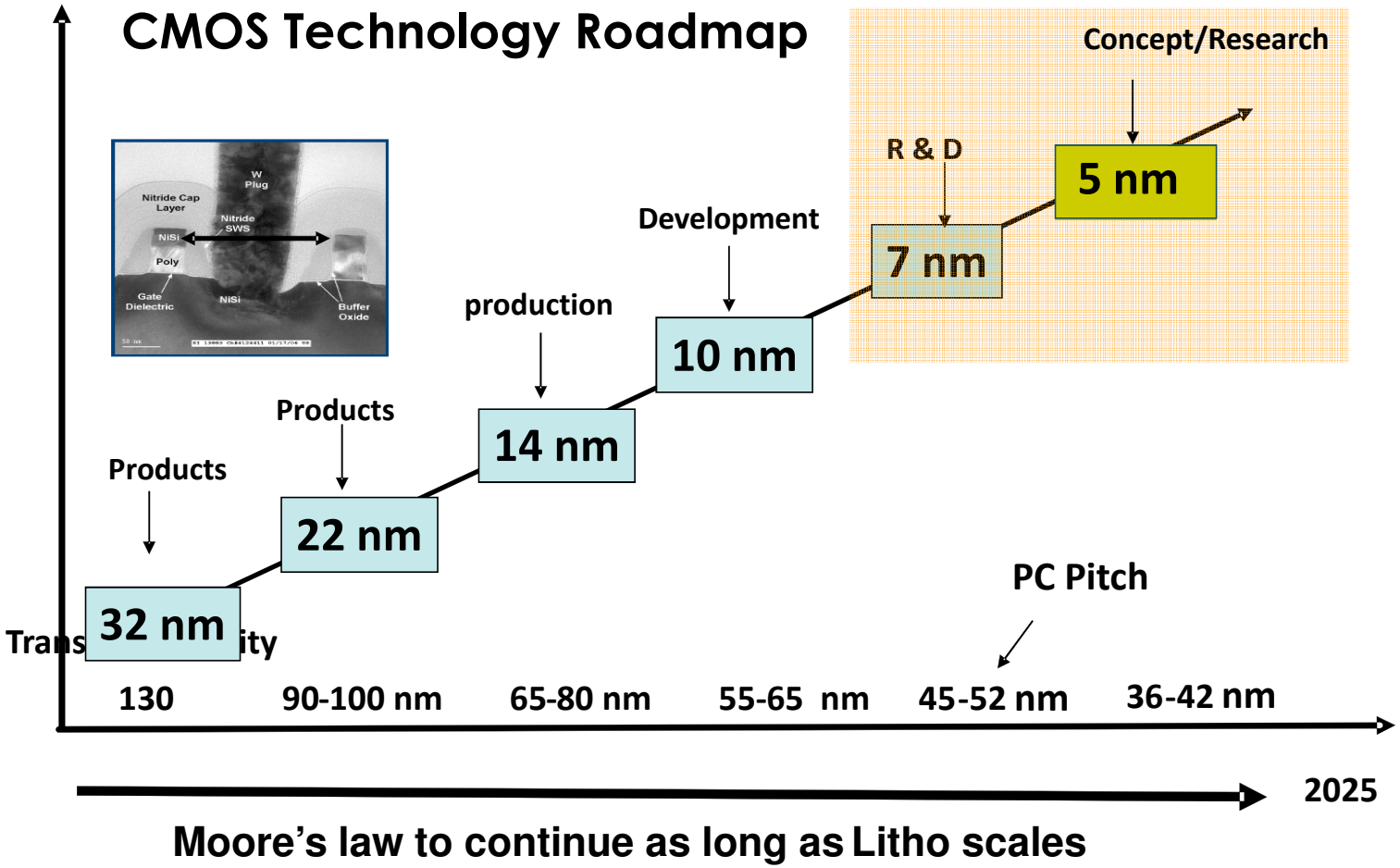
- A Majumdar
- Rajiv Joshi

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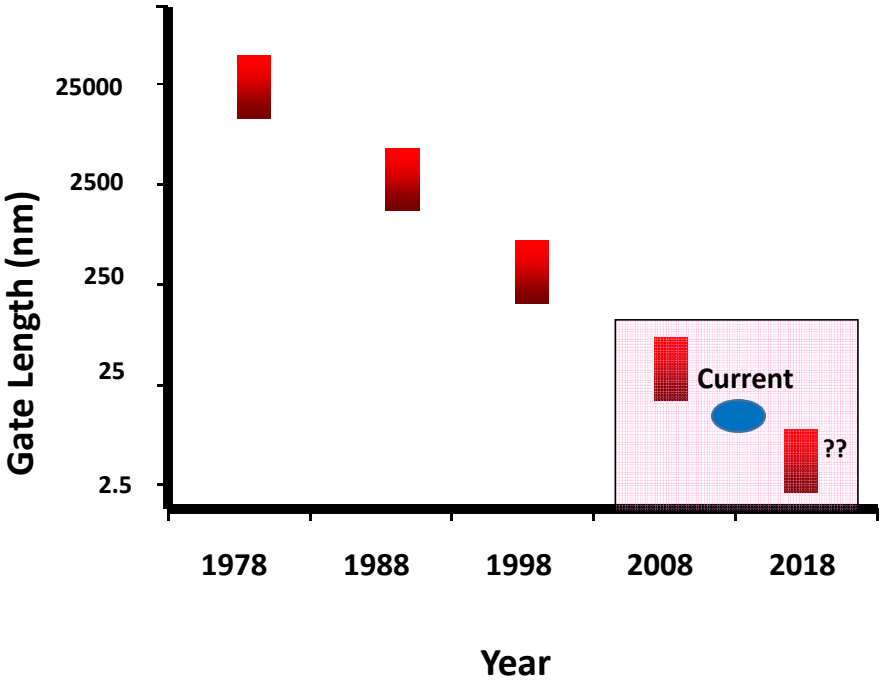
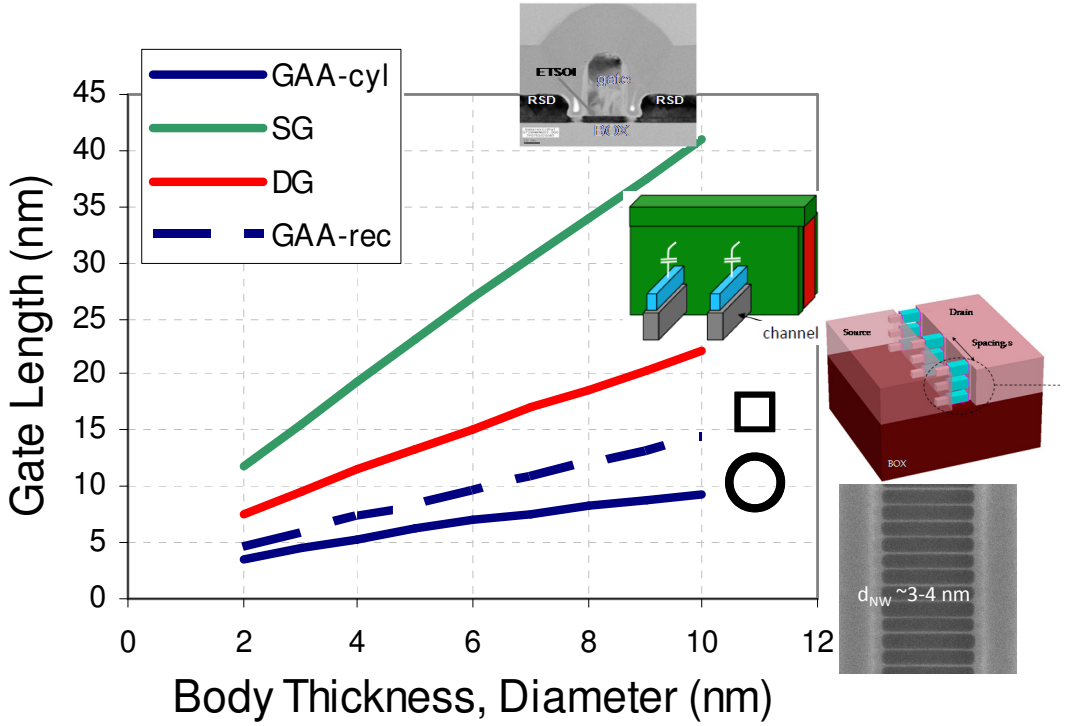
# Moore's Law to Continue….




- Gate Length Scaling path to 5 nm & beyond

- Options to control device electrostatics in scaled transistors

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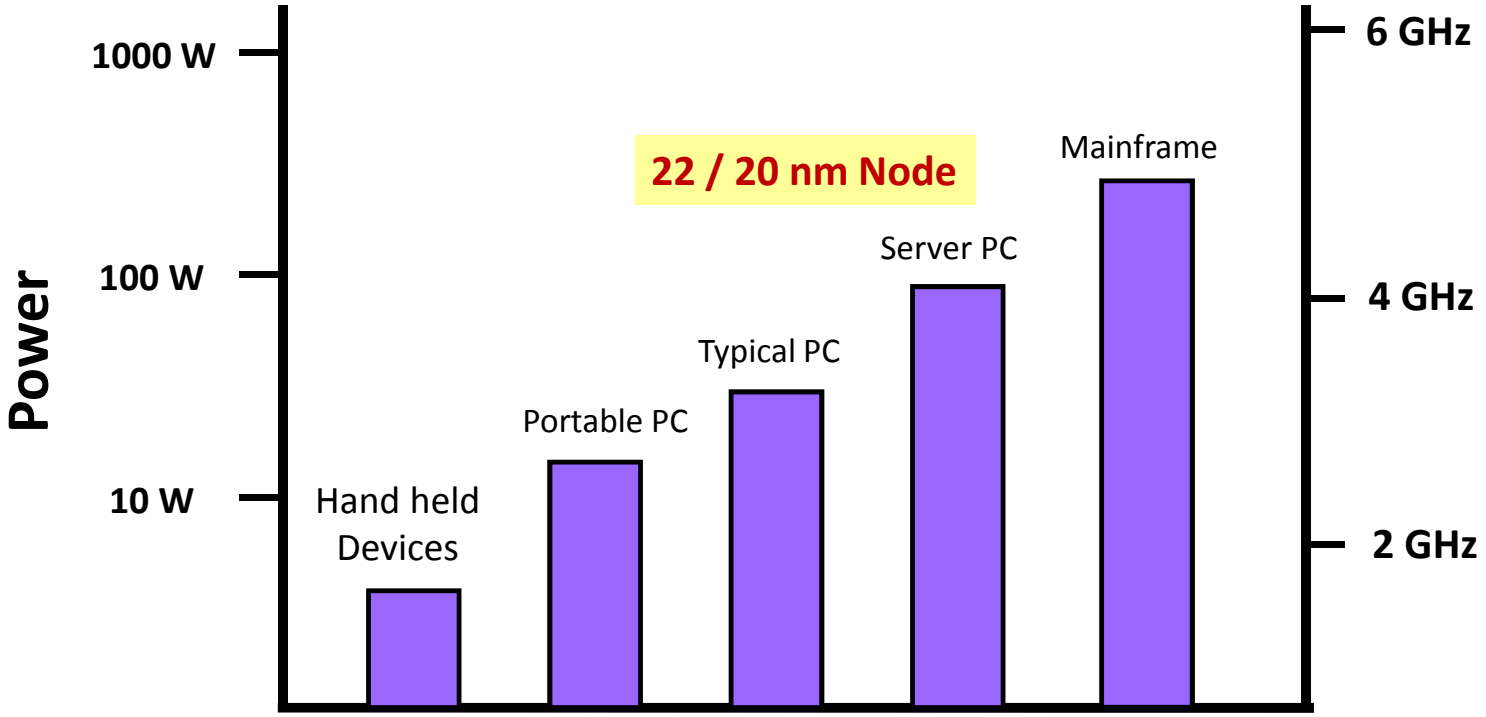
# Scaling Motivation: Processor Device Count

| Node | Transistors / $cm^2$ *(20% GR hit per node)* | Transistors in 500 $mm^2$ (Billions) | 3D Stack: 1-3 Layers (Billions) | Chips/MCM 1-8 (Billions) |
|---|---|---|---|---|
| 65 | 0.2 | 1 | | |
| 45 | 0.32 | 1.6 | | |
| 32 | 0.512 | 2.6 | | |
| 22 | 0.82 | 4.1 | 4 – 12 | 4 - 96 |
| 14 | 1.3 | 6.5 | 6 – 18 | 6 – 144 |
| 10 | 2.1 | 11 | 11 – 33 | 11 – 264 |
| 8 | 3.4 | 17 | 17 – 51 | 17 – 410 |
| 6 | 5.5 | 28 | 26 - 78 | 26 – 624 |

- 100s of billions of transistors on a multi-core processor

# Power-Performance by Product




- Most applications operate ***within a power-constrained environment***
- Future technologies require high performance operation with reduced power
- High mobility materials ideal for reduced power CMOS technology

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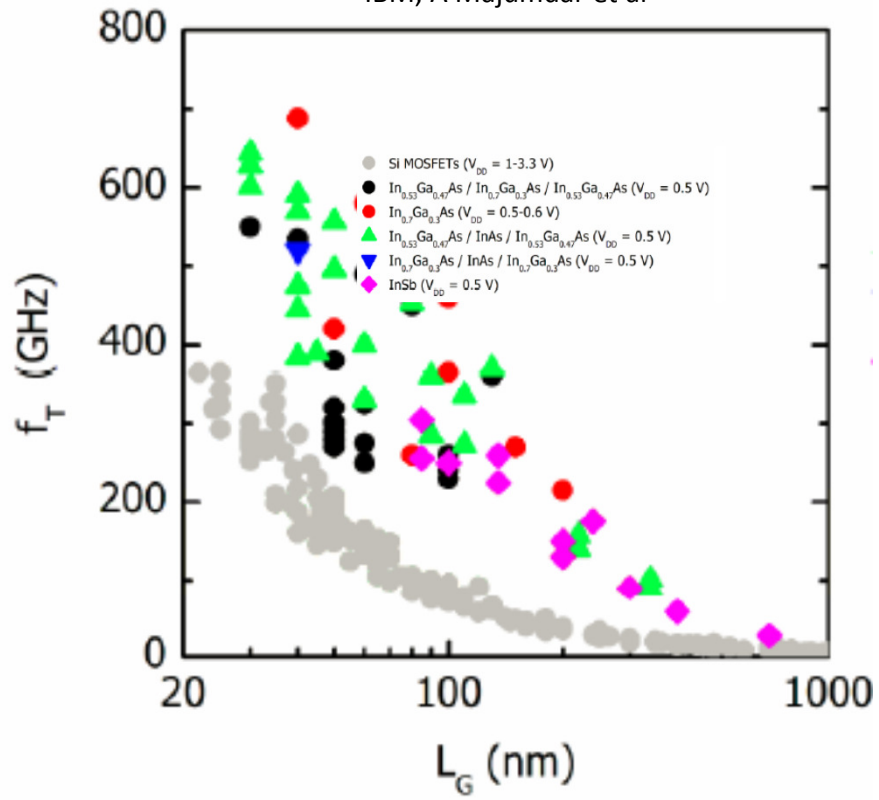
# Why III-V Channels?

- **Power density** is increasing with each successive CMOS node
- Device operation at ever **reducing supply voltage** required for both the total power and power density reduction $P_A \sim f\,CV_{DD}^2N \Rightarrow N\uparrow \rightarrow V_{DD}\downarrow$
- **Si CMOS performance suffers at reduced supply voltage**
- **High mobility channel** may be a possible path to address the performance issue at low voltages

IBM, A Majumdar et al




- **Intrinsic $f_T$ of III-V HEMTs ~ x2.0 higher @ $V_{dd}$ of 0.5-0.6V compared to Si @$V_{dd}$ of 1.33 V**

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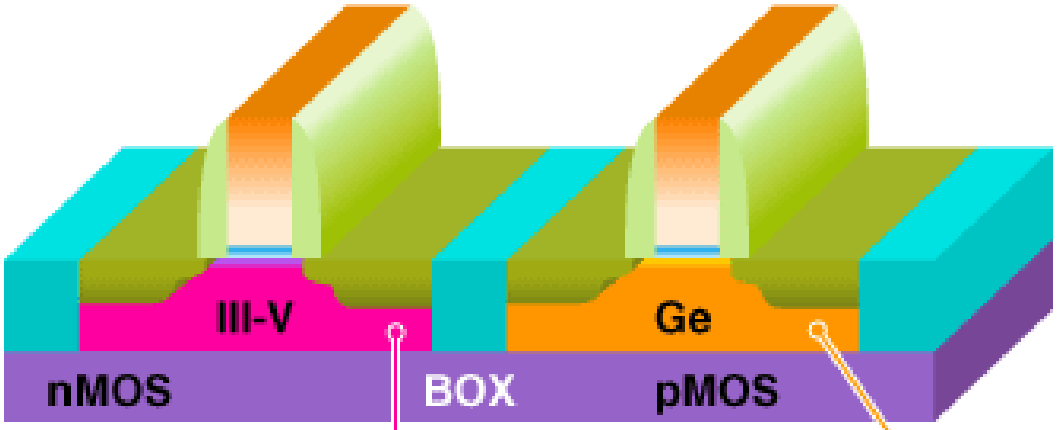
# Ideal CMOS for Highest Performance with High Mobility Channels




| Material | Si | InAs | Ge |
|---|---|---|---|
| Electron mobility (cm²/Vs) | 1,600 | 40,000 | 3,900 |
| Hole mobility (cm²/Vs) | 430 | 500 | 1,900 |

Existing channel material

**Key Fundamental Challenges**

- Band to band tunneling
- High density of defects in channel

| Material | $\mu_e$ ($cm^2/Vs$) | $\mu_h$ ($cm^2/Vs$) | $E_g$ (eV) |
|---|---|---|---|
| Si | 1350 | 480 | 1.12 |
| Ge | 3900 | 1900 | 0.66 |
| InP | 5400 | 200 | 1.34 |
| GaAs | 8500 | 400 | 1.42 |
| InGaAs(53%) | 12000 | 300 | 0.74 |
| InAs | 40000 | 500 | 0.35 |
| GaSb | 3000 | 1000 | 0.73 |
| InSb | 77000 | 850 | 0.17 |

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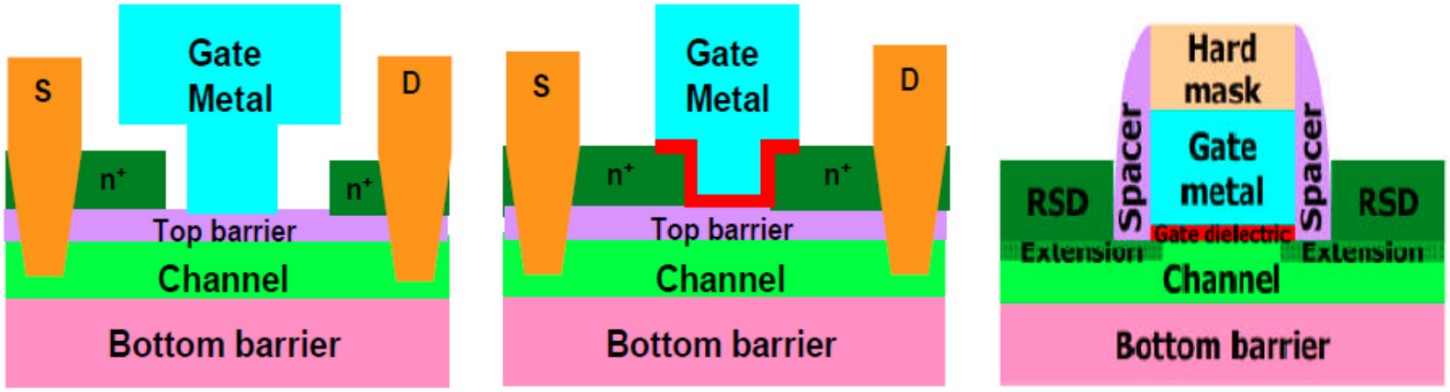
# Schematics of Planar Device Architectures of III-V Devices: Pros & Cons



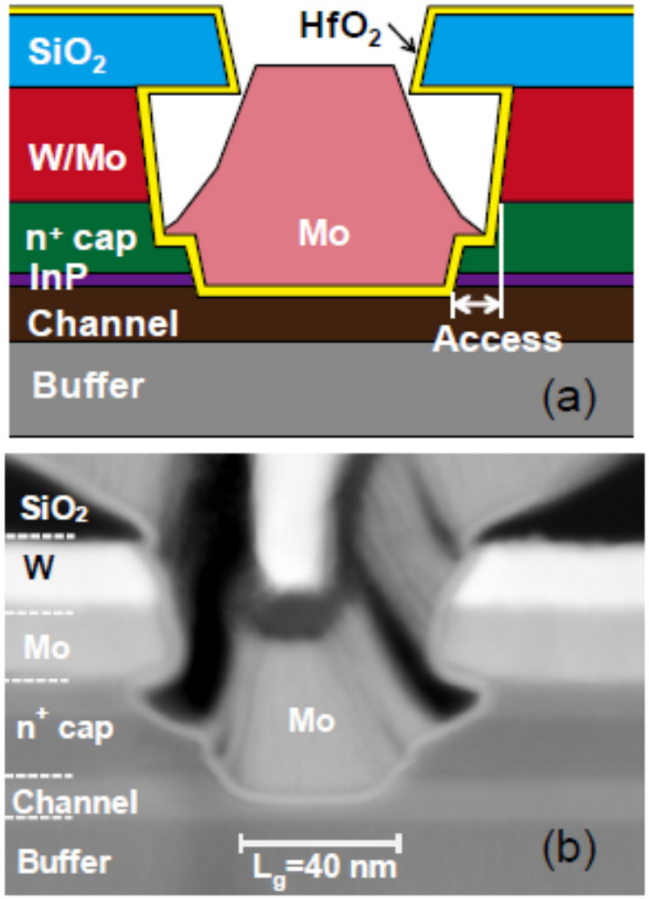

**HEMT** **MOS-HEMT** **MOSFET**

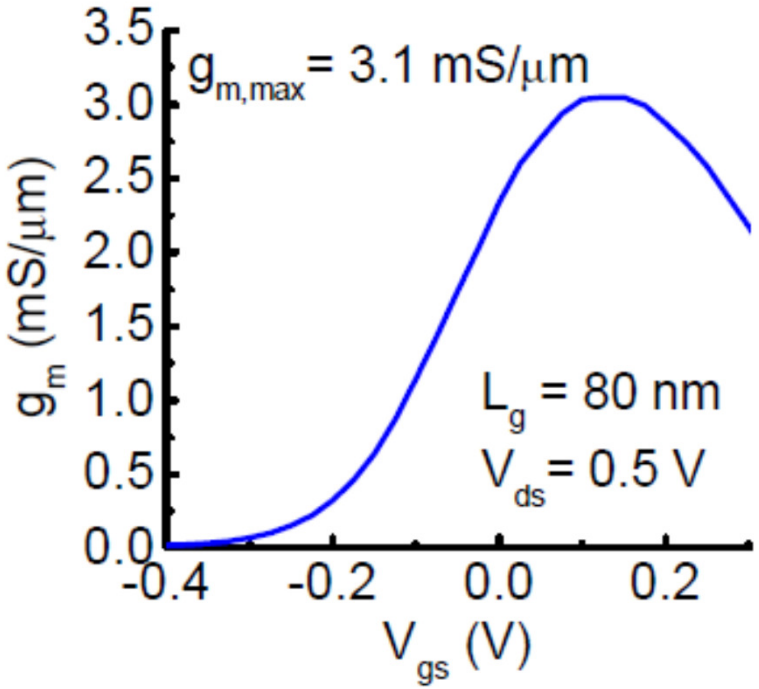
| | HEMT | MOS-HEMT | MOSFET |
|---|---|---|---|
| Gate leakage ($I_G$) | High | Low | Low |
| Self aligned | No | No | Yes |
| Overlap ($C_{OV}$) | Low | High | Low |

IBM, Y Sun

D K Sadana, IBM, CICC 2015

# Record Performance via High Mobility ($In_{0.53}Ga_{0.47}As$) MOSFET Channel

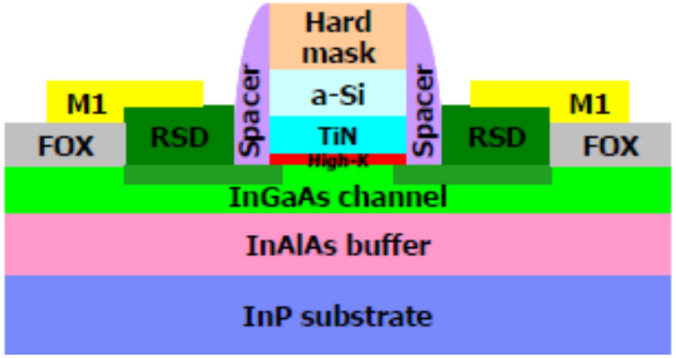


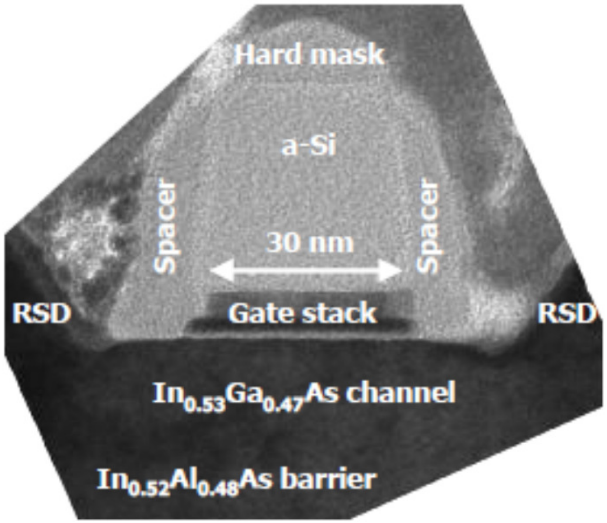



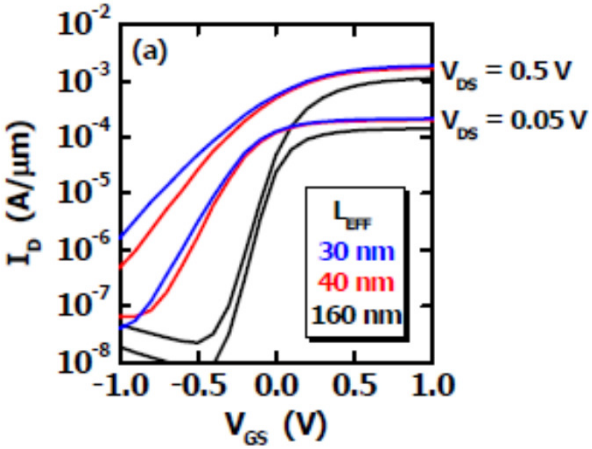

MIT, Lin et al, IEDM Proc, pp 575-578, 2014

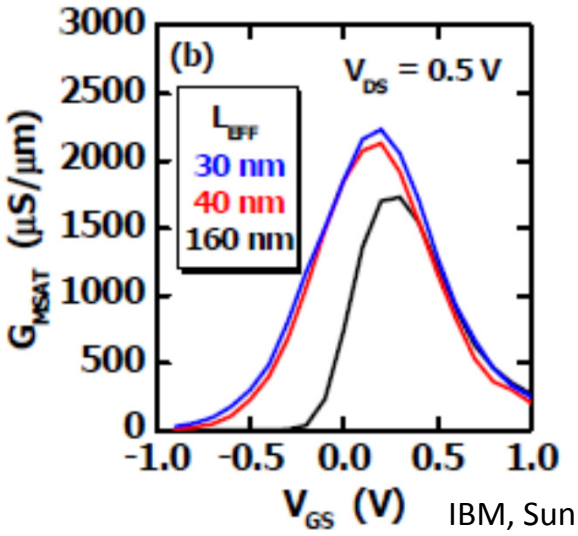
D K Sadana, IBM, CICC 2015

# Record Performance Self-aligned InGaAs Planar MOSFET on an InP Substrate



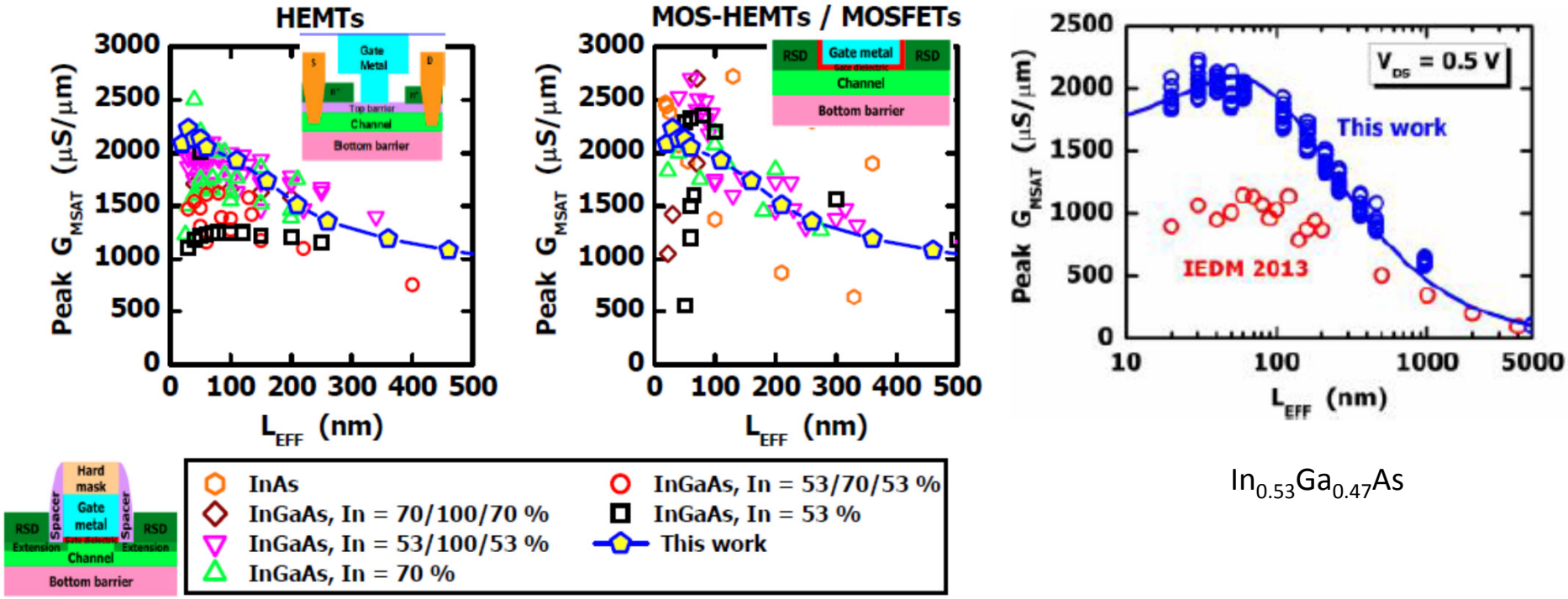

- Experimental data from planar devices demonstrates power of III-V channel for future CMOS

IBM, Sun et al IEDM 2014

D K Sadana, IBM, CICC 2015

# Benchmarking of InGaAs Based HEMTs, MOS-HEMTs, and Self-Aligned MOSFETs

IBM, Y Sun et al, IEDM 2014




$In_{0.53}Ga_{0.47}As$

- Performance ($G_{MSAT}$ ) of self –aligned $In_{0.53}Ga_{0.47}As$ MOSFETs has been improved to be at par with HEMTs and MOS-HEMTs
- This is a significant development from the point of view of co-integrating III-Vs into mainstream Si CMOS technology

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# Gaps Between Si and Co-Integrated Si/III-V NFET Technologies

| Basic Properties | Silicon | III-V ($In_{0.53}Ga_{0.47}As$) |
|---|---|---|
| Band gap (eV) | 1.1 | 0.74 |
| Electron Mobility ($cm^2$/V-s) | 1400 | 12000 |
| **Crystallogrphic defect density ($cm^{-2}$ )** | **Undetectable** | **> $10^9$** |
| Dieletric/Si interface charge ($cm^{-2}$ $eV^{-1}$) | X $10^{10}$ | X $10^{12}$ |
| Shortest channel length (nm) | < 20 | > 30 |
| Subthreshold slope (mV/dec), SC | < 70 | > 90 |
| $I_{off}$ @ < 30 nm channel (A/μm) | pA range | nA range |
| Contact resistance (Ω $cm^2$) | $10^{-9}$ range | $10^{-8}$ range |
| Self-aligned contacts | Yes | No |
| Process temperature (° C) | > 1200 LSA | < 650 |

- There is a formidable gap between Si and III-V materials, processes, and device properties
- Innovative solutions required to integrate III-V materials into Si technology

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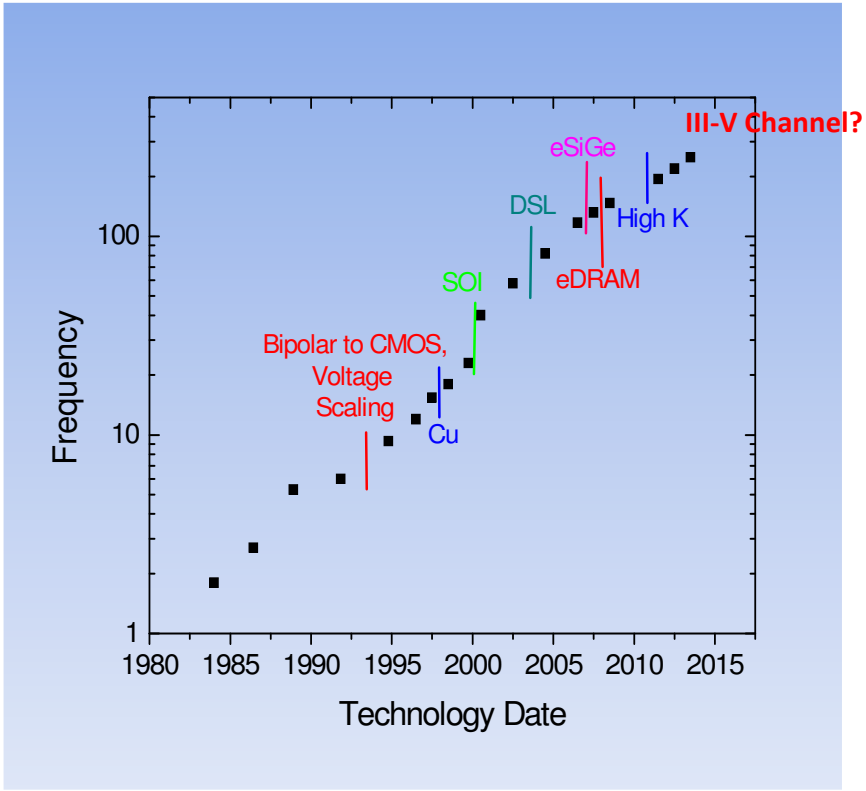
# Outline

- **Heterogeneous Si/III-V integration**
- **Key Challenges**
  - **Substrate → defects**
  - **Integration → temperature**
  - **Devices → SS, DIBL, $D_{it}$**
- **Conclusions**

**Technological Innovations to Maintain High Performance**



# Si/III-V Growth Questions

## What's the end substrate product ?

**$In_{0.53}Ga_{0.47}As$ (< 20 nm) / Si**

## Why don't we bond III-V channel directly onto Si ?

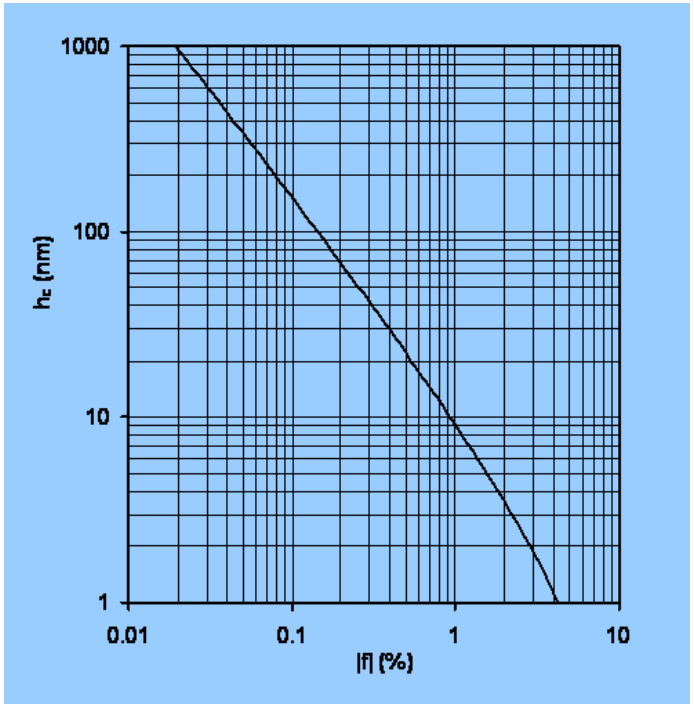
**Si (300 mm) and III-V wafer (100 – 150 mm) diameter incompatibility**

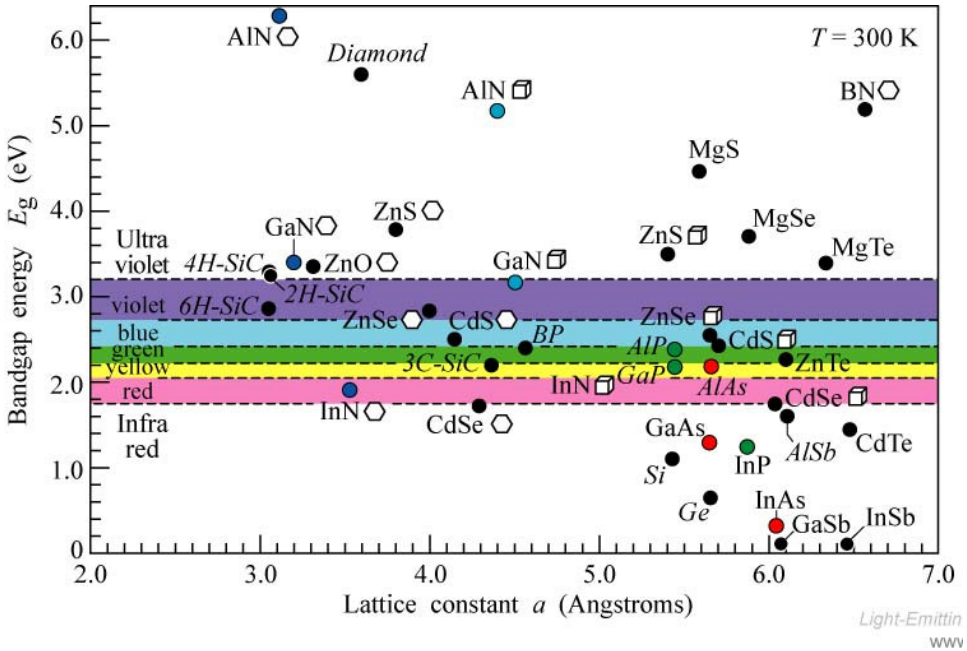
## What happens when we grow III-V channel directly onto Si ?

**Highly lattice mismatched (> 8%) system is thermodynamically unstable and balls up during the growth (this is how QDs are created!!)**

**High defect density (> $10^{10}$ $cm^{-2}$) at the III-V/Si interface: unsuitable for product**

# Issue: Growth of III-Vs on Si Causes Defect Generation due to Large Lattice Mismatch




- InGaAs or InP mismatch with Si: > 8%
- Ge or GaAs mismatch with Si: ~ 4%
- Critical thickness for lattice mismatch of > 4% : < 0.5 nm
- Instantaneous defect formation in $In_{0.53}Ga_{0.47}As$ growth on Si

## Lattice Mismatch & Growth Induced Defect Types

- Planar: Stacking faults, Micro-twins, & Anti-phase boundaries
- Threading dislocations

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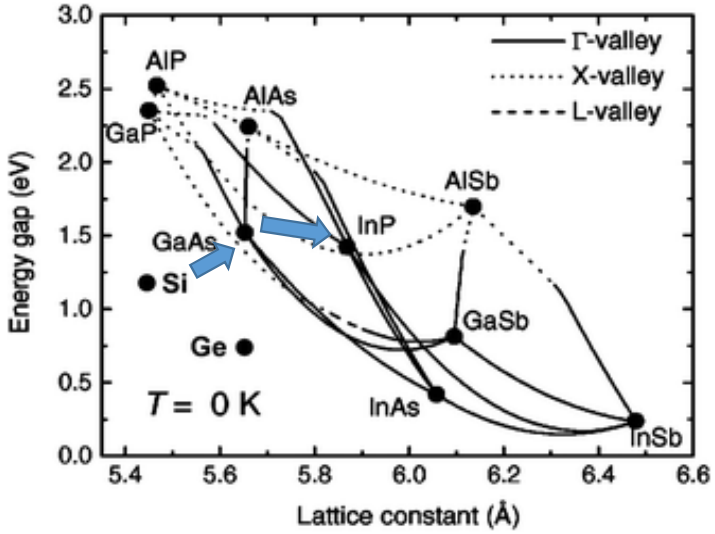
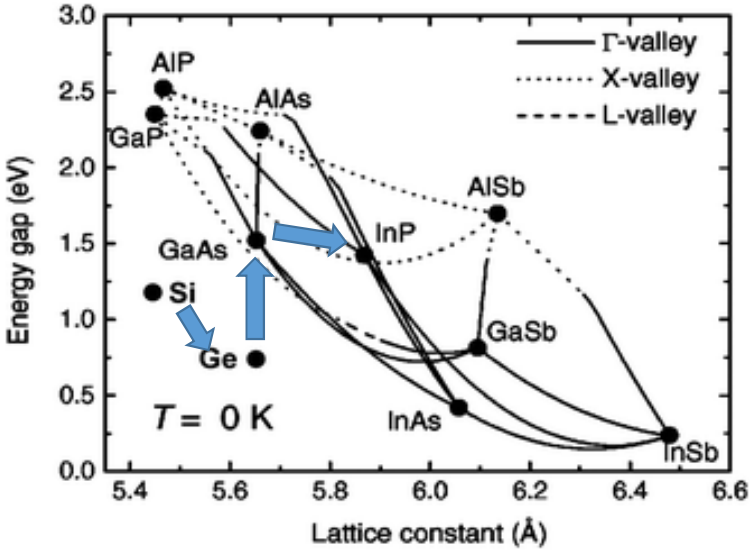
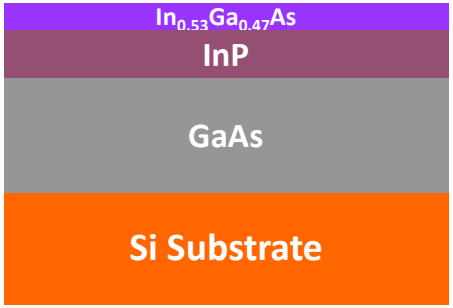
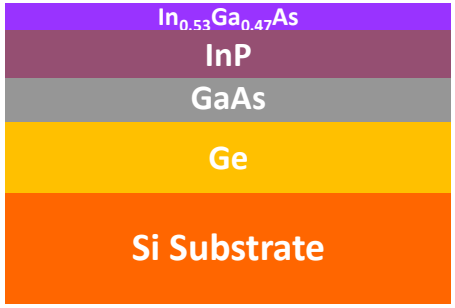
# Multiple Paths to III-V Growth on Si




D K Sadana, IBM, CICC 2015

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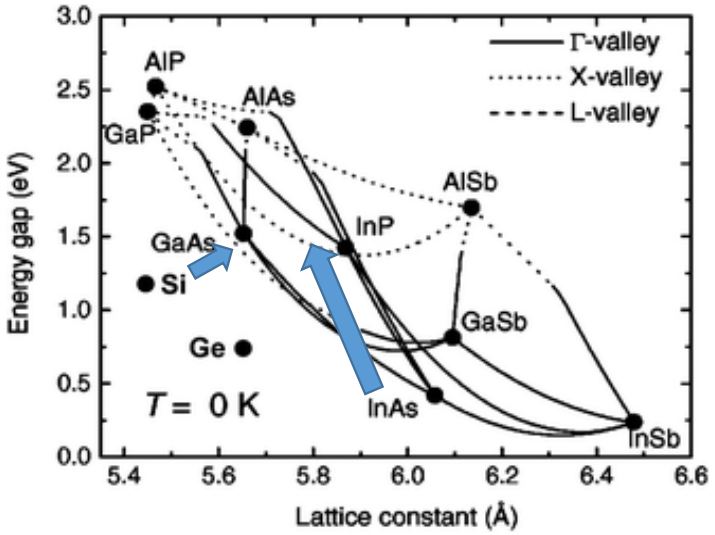


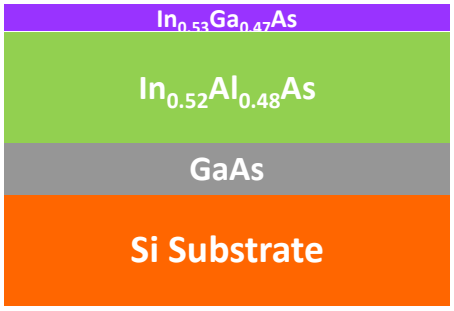


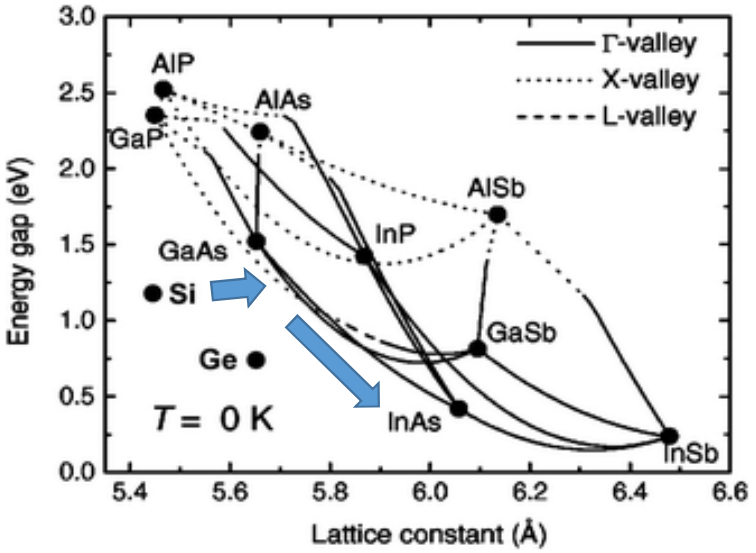


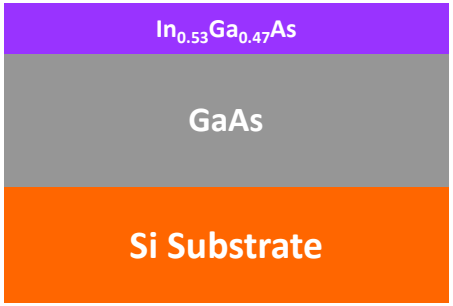


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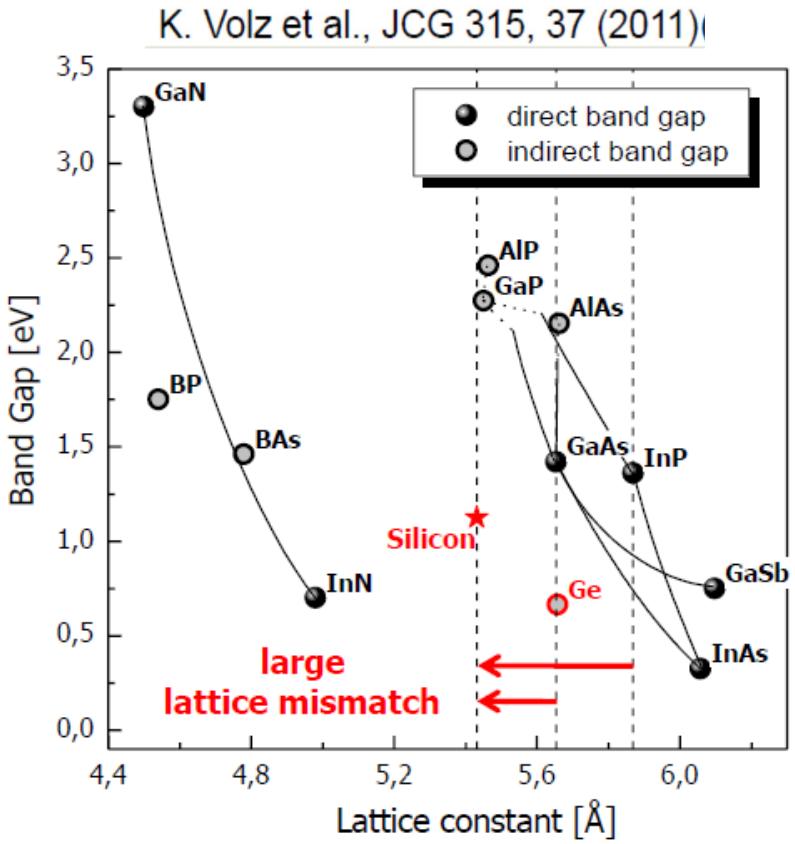
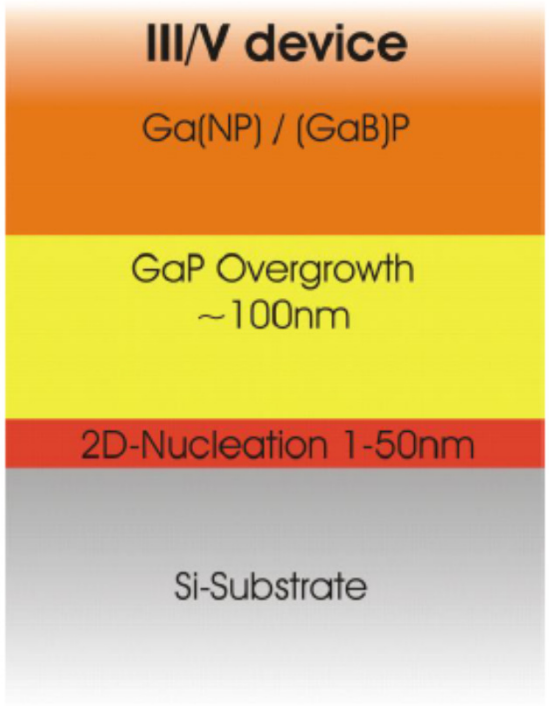
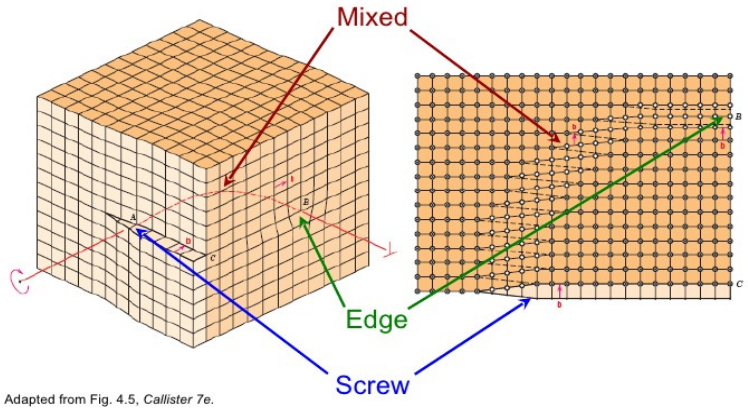


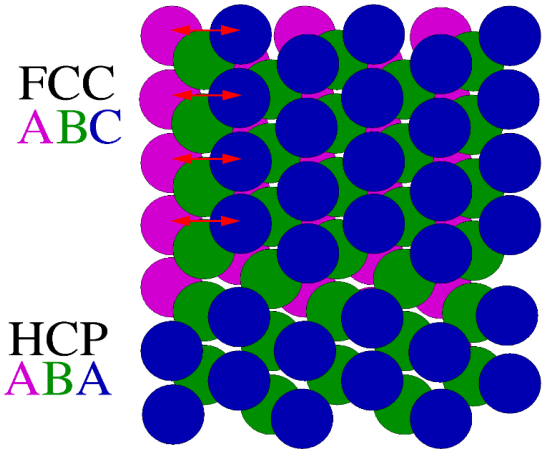
# Types of Crystallographic Defect in III-V Grown on Si

Edge, Screw, and Mixed Dislocations

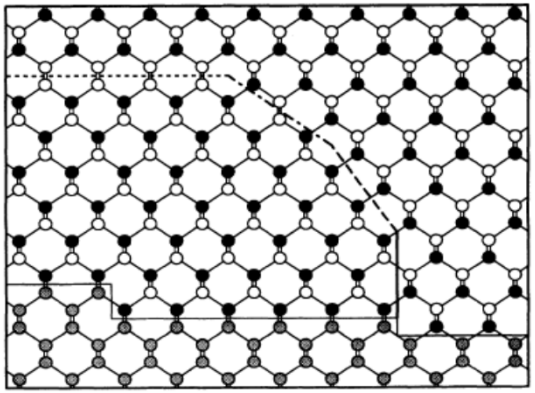



Adapted from Fig. 4.5, *Callister 7e.*

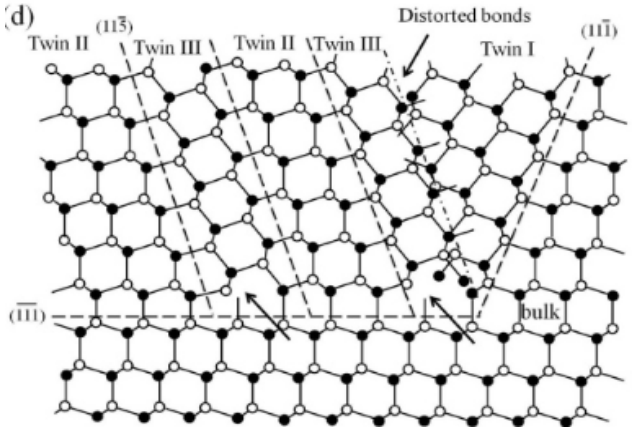
Stacking Faults




Anti-phase Boundry

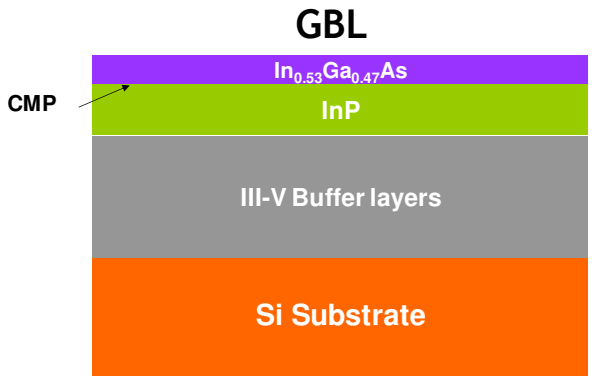


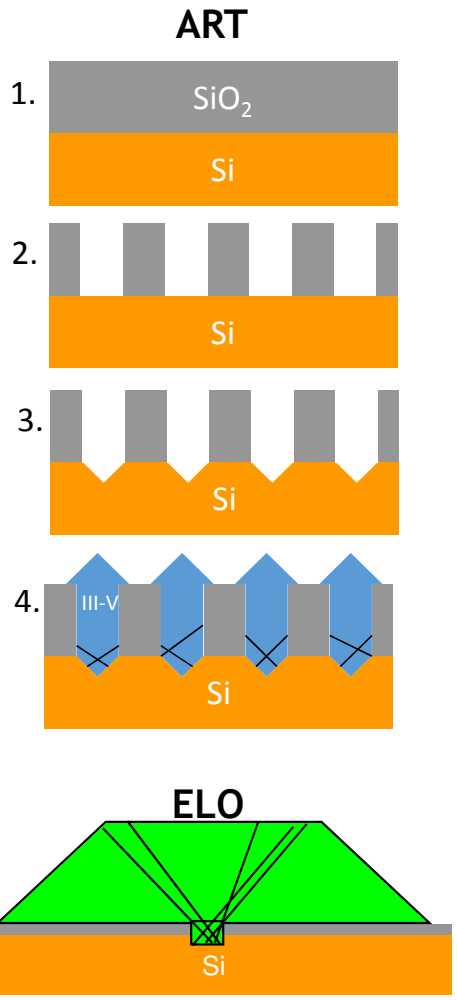
Micro-twins

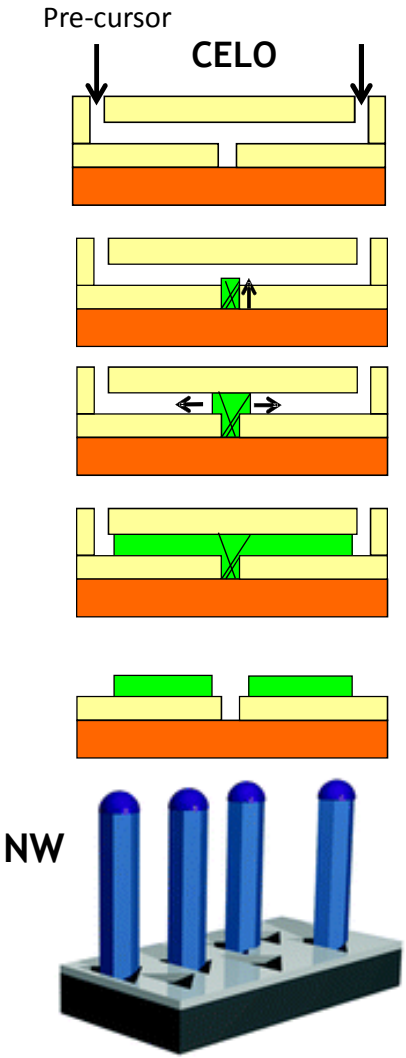


# Various Growth Approaches for Defect Reduction

1. **Graded buffer layer (GBL)**
   - Multiple options for buffer materials
   - Ge, GaAs, InP, InGaAs, InAlAs etc
2. **Aspect Ration Trapping (ART)**
3. **Confined Epitaxial Lateral Overgrowth (CELO)**
4. **Cyclic annealing**
5. **Layer transfer on Oxide (SOI-like)**
6. **Epitaxial Lateral Overgrowth (ELO)**
7. **Nanowires (NW)**



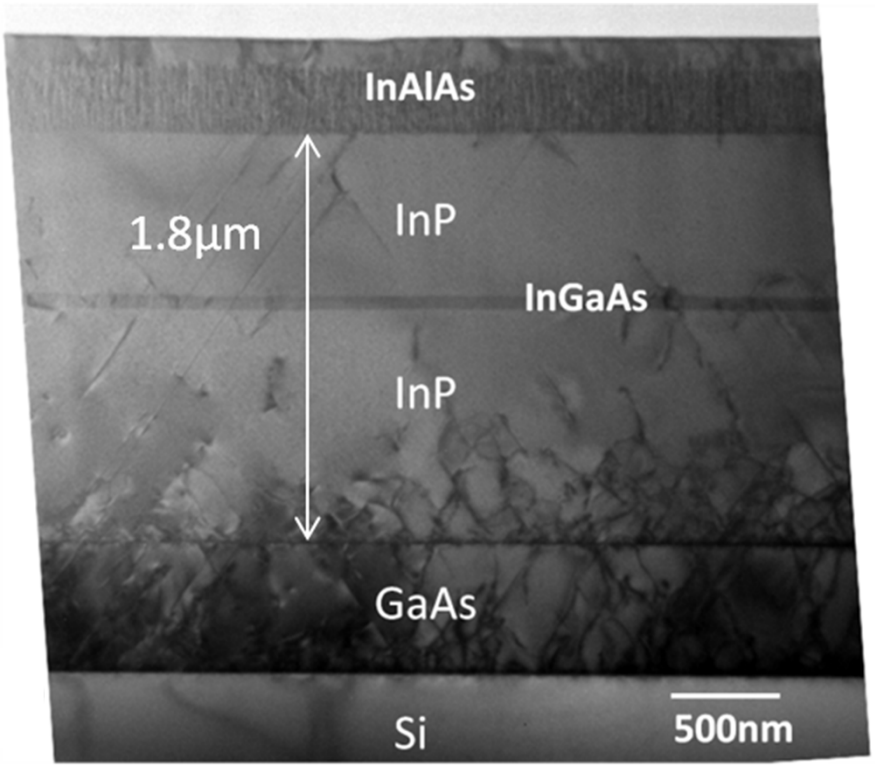



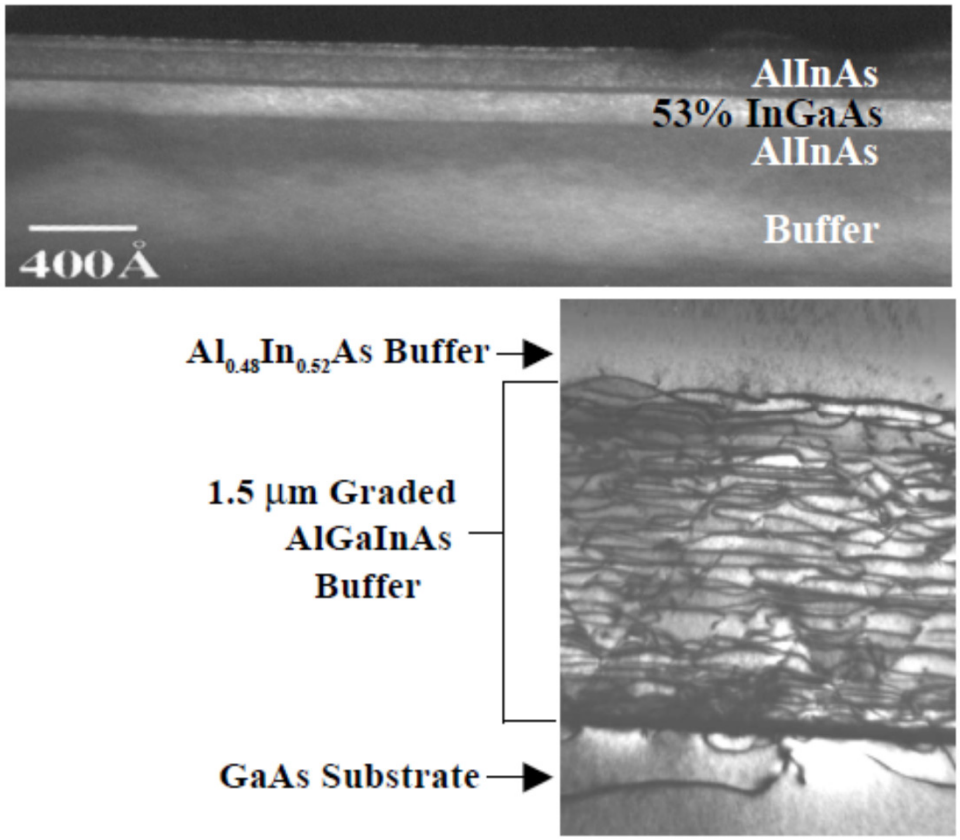

D K Sadana, IBM, CICC 2015

# Approach 1: Defect Reduction in III-V on Si Through a Thick Buffer Layer

**Q. Li**, et al, **IEEE Trans. Electron Devices**, 60(12), pp.4112-4118, Dec.2013



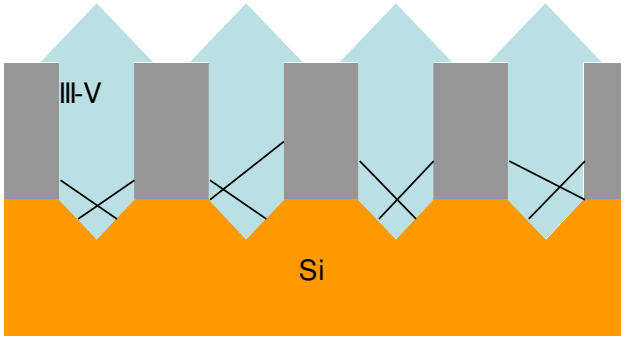

Hoke et al, GaAs Mantech, 2001



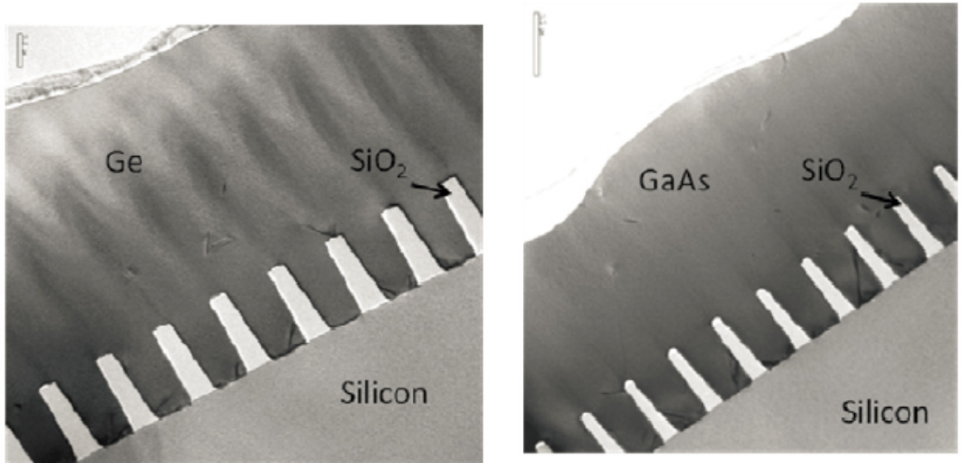

- Defect reduction can be achieved in a multiple way: (i) by growing a thick InP layer on GaAs/Si, and (ii) by grading AlGaInAs on GaAs/Si
- Best defect density is still > $10^8$ $cm^{-2}$

D K Sadana, IBM, CICC 2015

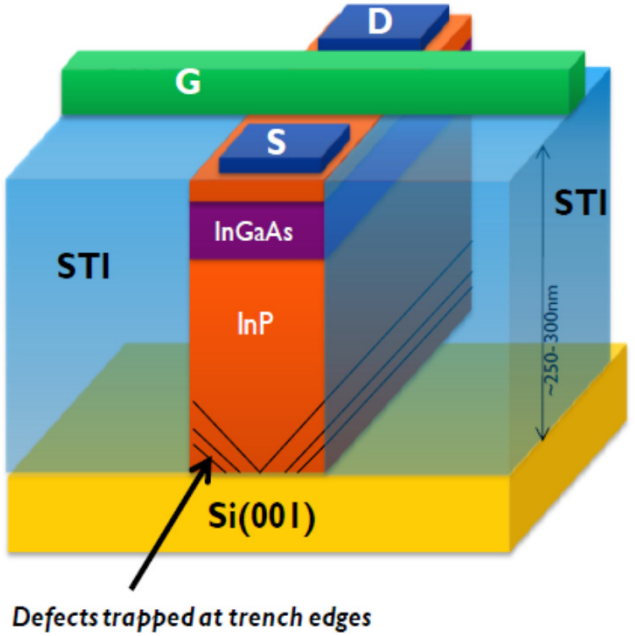
# Approach 2: Aspect Ratio Trapping (ART)




Fiorenza et al, ECS Trans, 33, 963-976 (2010)



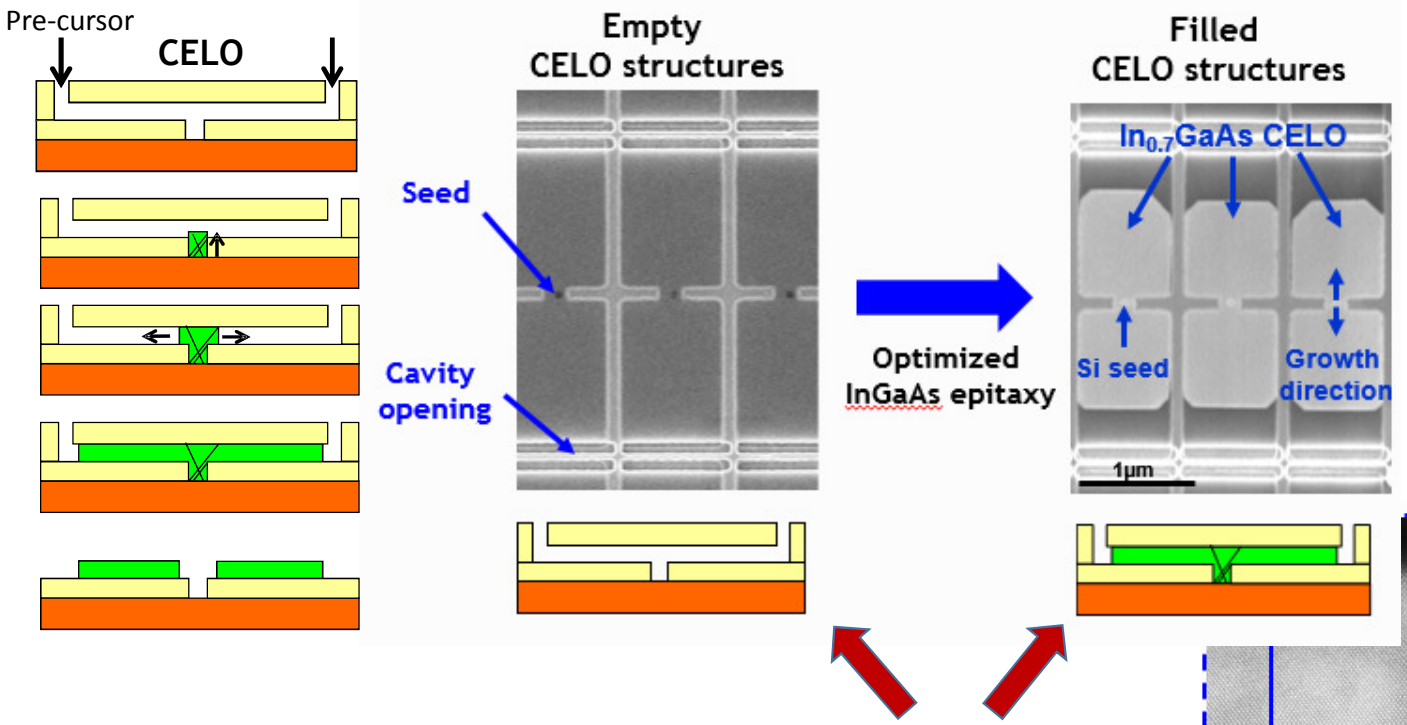

Initial Concept & its Verification




Current Implementation into III-V/Si co-integrated technology

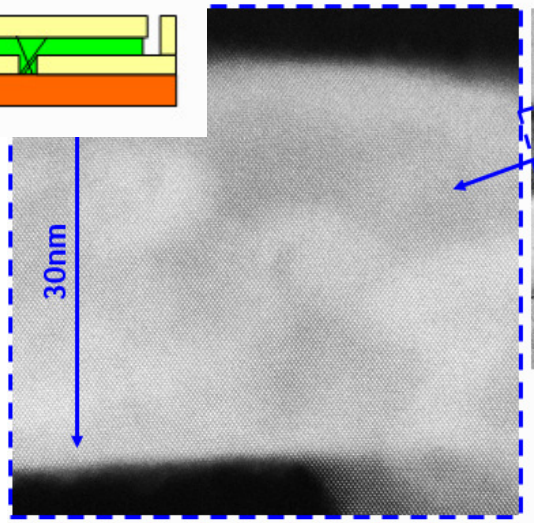
D K Sadana, IBM, CICC 2015

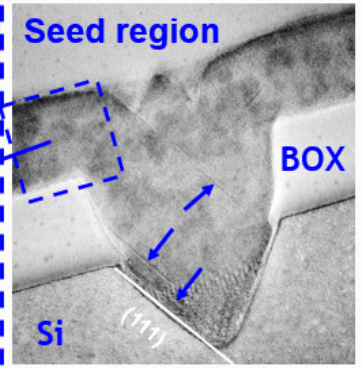
# Approach 3: Confined Epitaxial Lateral Overgrowth (CELO)




IBM, Czornomaz et al, IEEE VLSI Symp 2015

- Uniform InGaAs growth in active device region achieved
- Effective reduction of defects away from the seed region evident

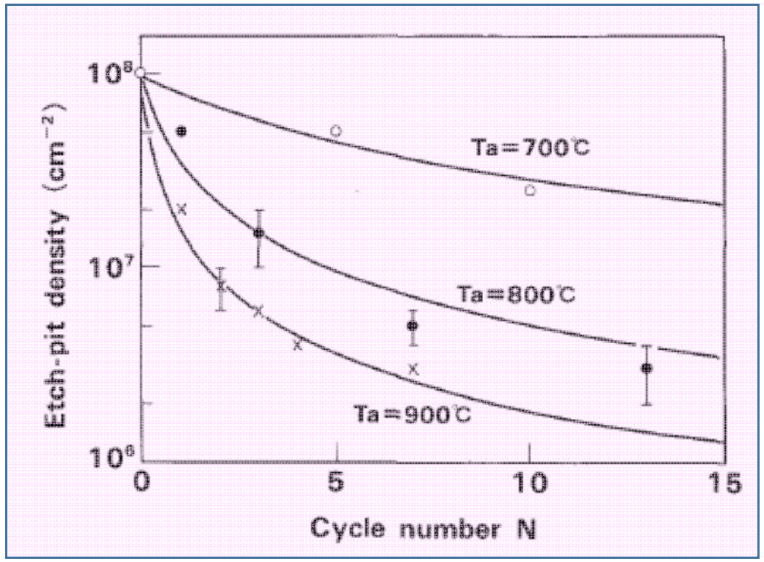



No defects observed right after the change of growth direction

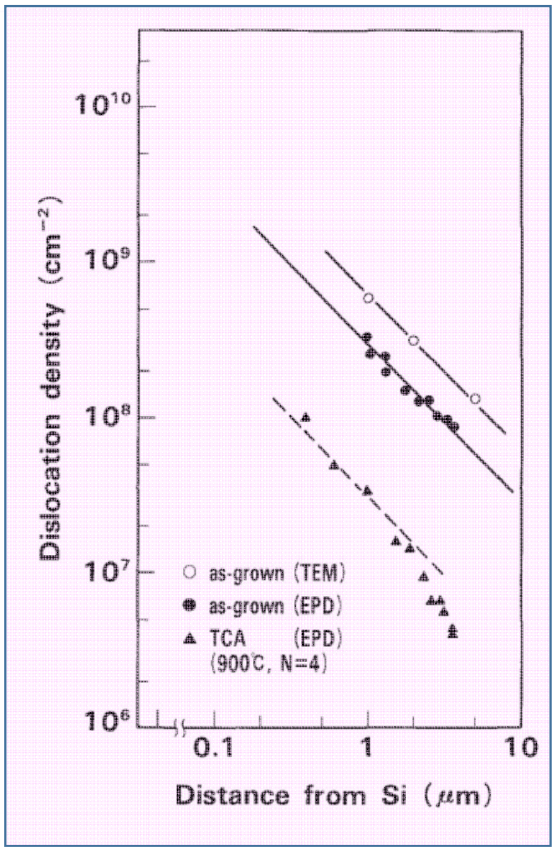
D K Sadana, IBM, CICC 2015

# Approach 4: Defect Reduction by Post Epi Cyclic Anneal



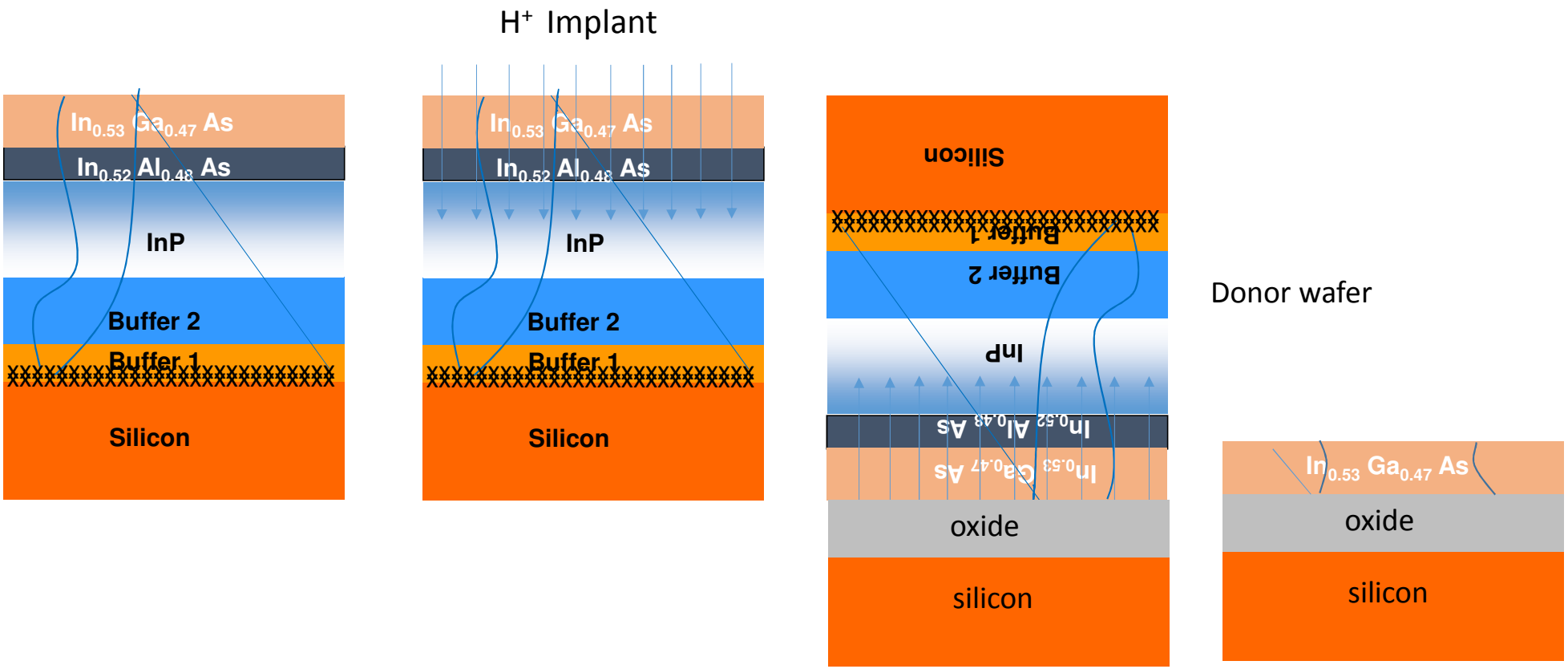

GaAs/Si

- Defect reduction by two orders of magnitude possible by high T cyclic anneal




Yamaguchi, JMR, 1991, pp 376-384

# Approach 5: Layer Transfer on an Insulator by wafer bonding

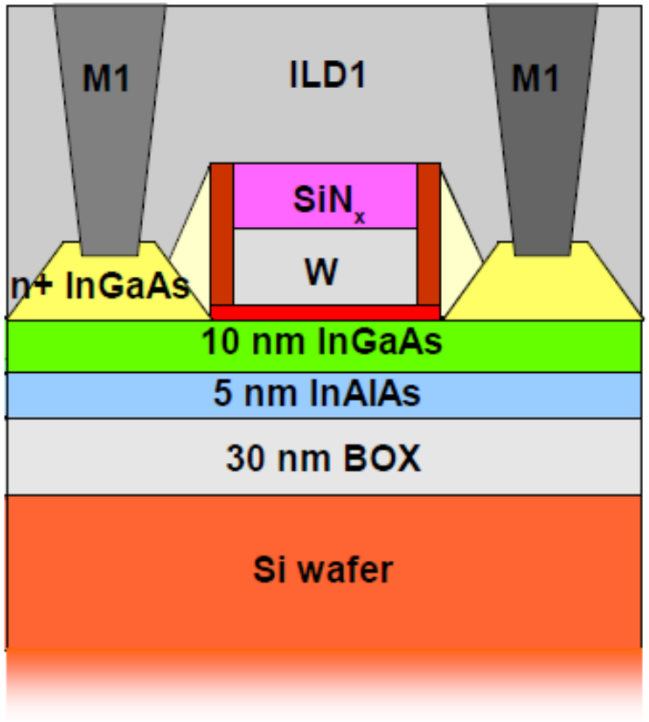


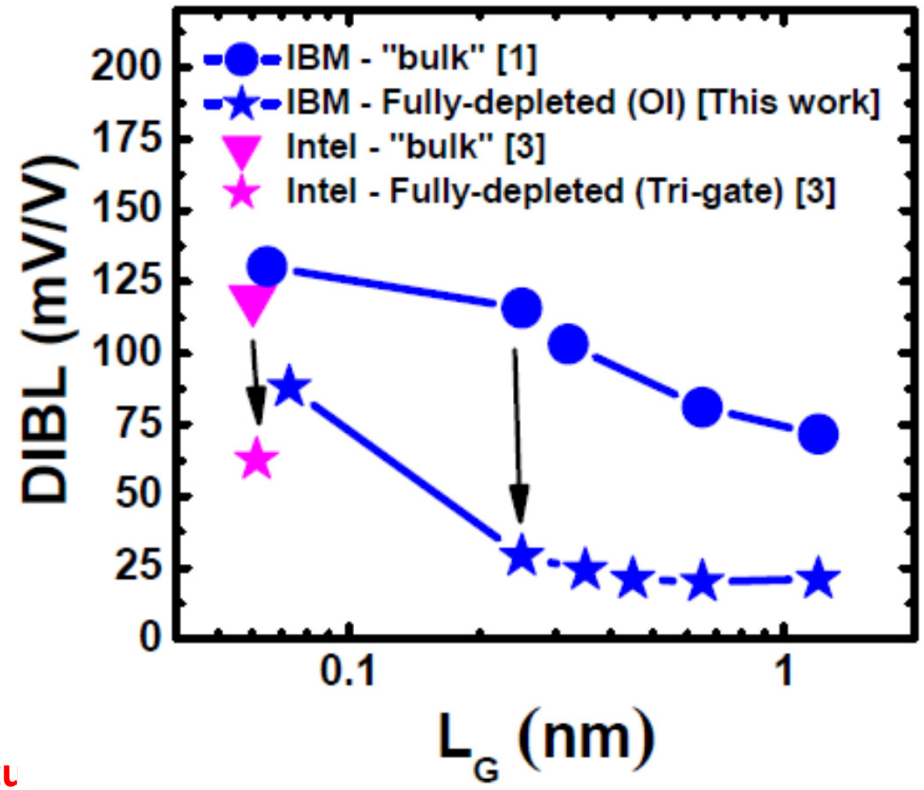

- Elimination of heavily defective region by layer transfer
- Defects only in the surface region are transferred
- Carrier recombination is minimized at defects because thin channel layer is fully depleted

D K Sadana, IBM, CICC 2015

# Defect-Electrical Correlation

# Improved Device Electrostatics in III-Vs on Insulator (Approach 5)

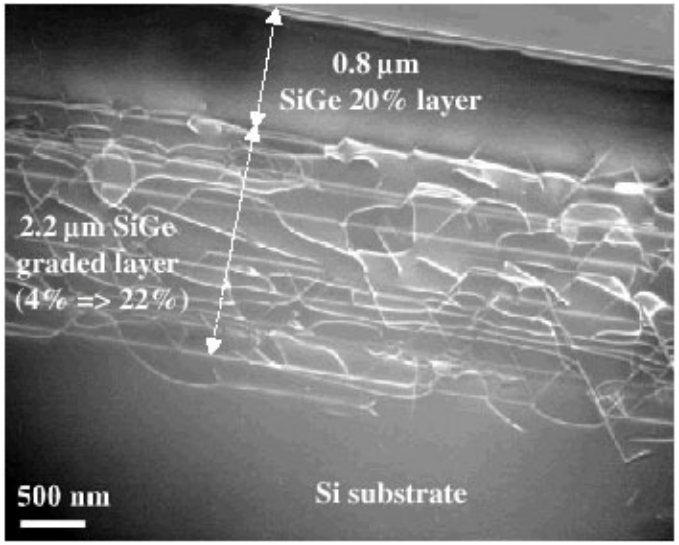


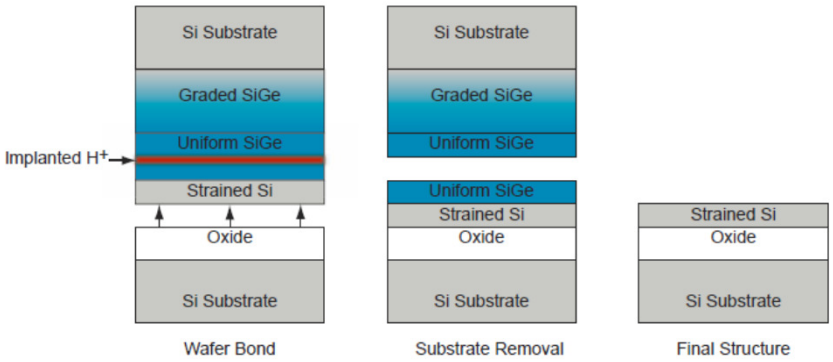

- **Layer transfer in conjunction with III-VOI structu near-ideal for Si/III-V device eletrostatics**

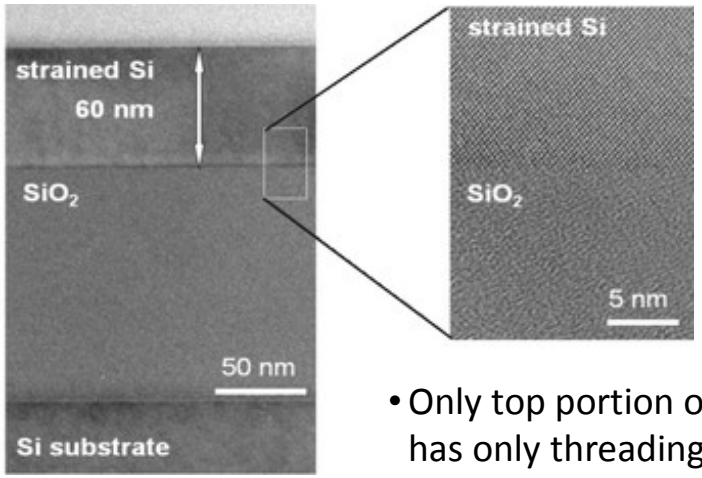
IBM, Czornomaz et al, 43rd, IEEE ESSDERC Conf, Bucharest, 2013

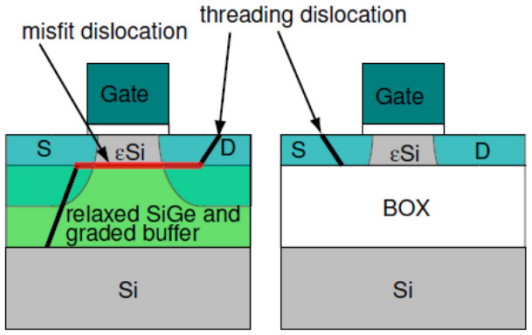
# Approach 5: Layer Transfer on an Insulator by wafer bonding

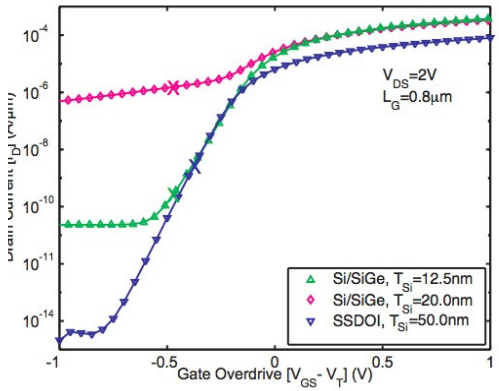



Lauer et al, IEEE EDL, Vol.25, 83-85, 2004
Lee et al, J App Phys, Vol. 97, 011101, 2005



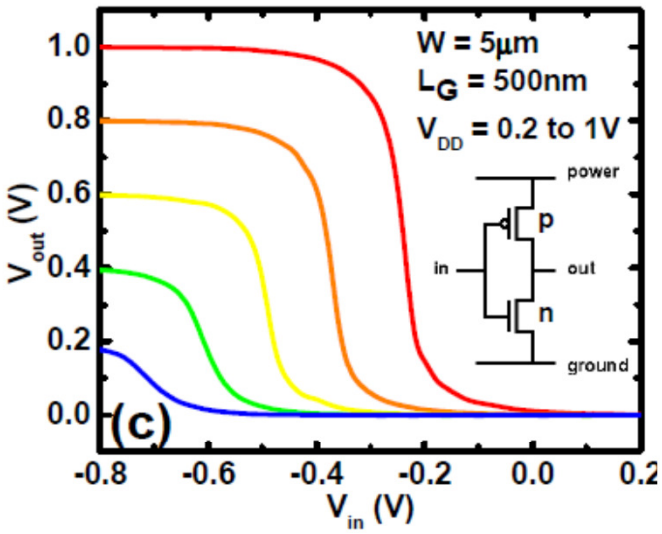



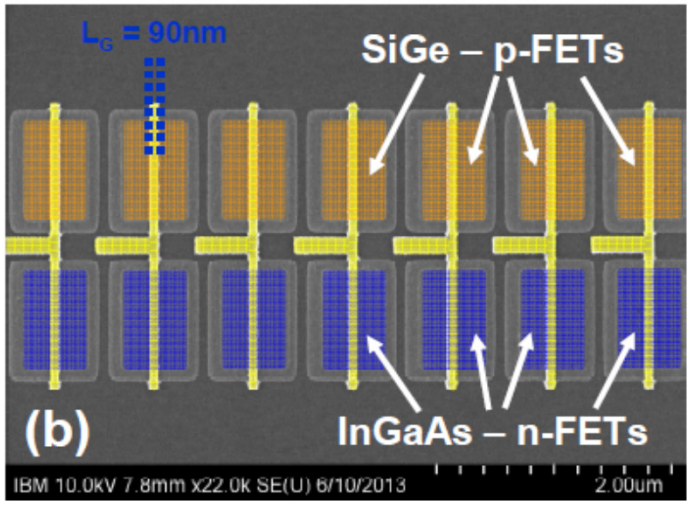

- Only top portion of the layer is transferred leaving behind misfit dislocations. The SOI layer has only threading dislocation arms which do not significant impact device leakage.

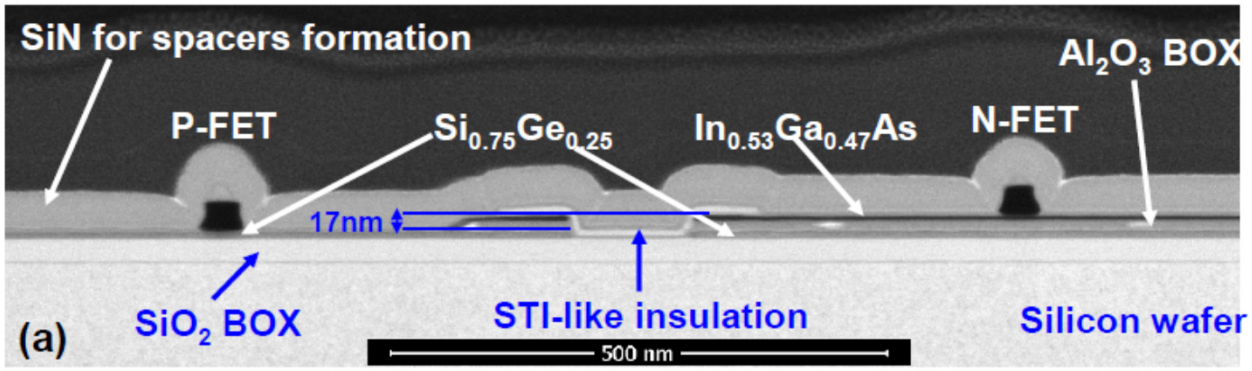
D K Sadana, IBM, CICC 2015

# Inverters with SiGe pFETs and InGaAs nFETs on Insulator (Approach 5)

IBM, Czornomaz et al, IEDM 2013



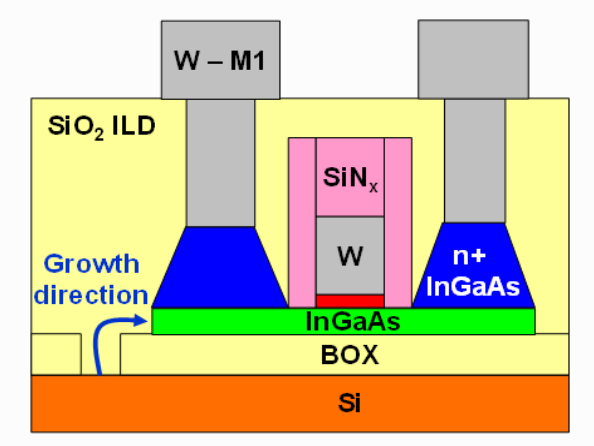



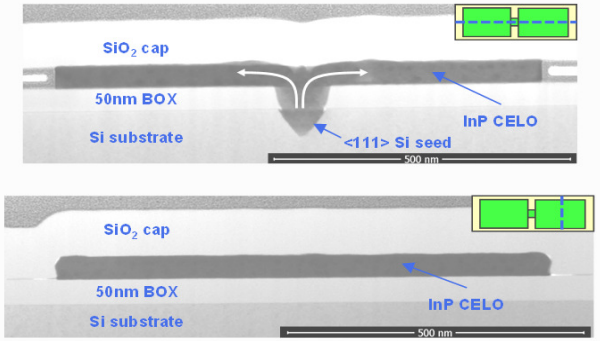

- Transfer characteristics of the CMOS inverter measured at different $V_{DD}$. Well-behaved operation occurs down to 0.2V.

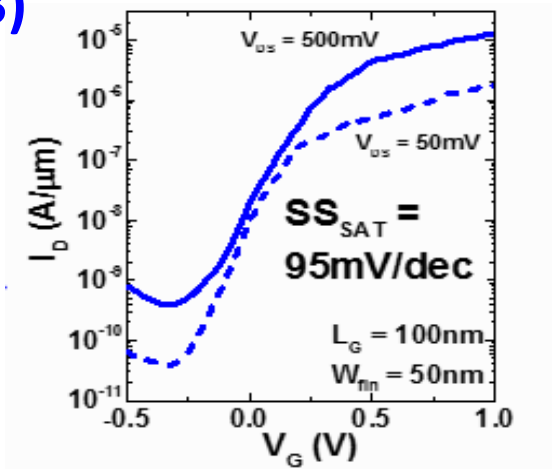
D K Sadana, IBM, CICC 2015

# InGaAs FinFET on Si (Approach 3)

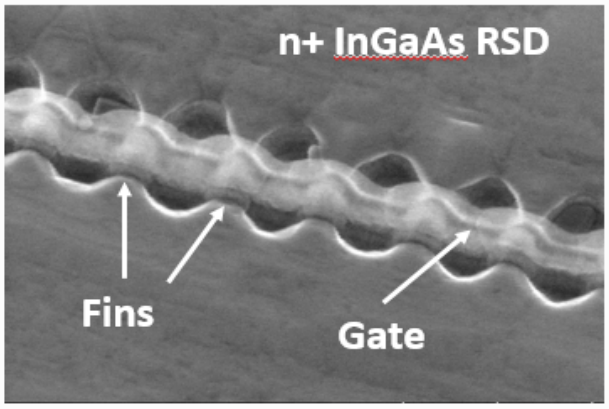



Cross-section of 30nm-thick InP CELO (8% mismatch)

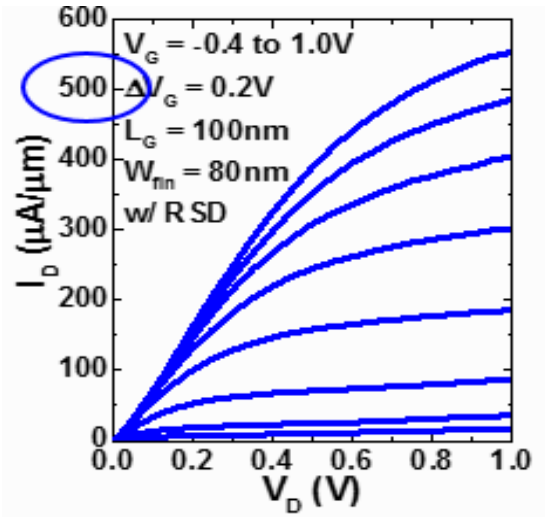



- CELO structure fabrication
- InGaAs selective epitaxy
- CELO cap removal
- InGaAs fins etch
- HKMG deposition
- Gate patterning
- $SiN_x$ Spacers formation
- Raised Source/Drain epitaxy
- $SiO_2$ ILD deposition
- Metal contacts (M1)



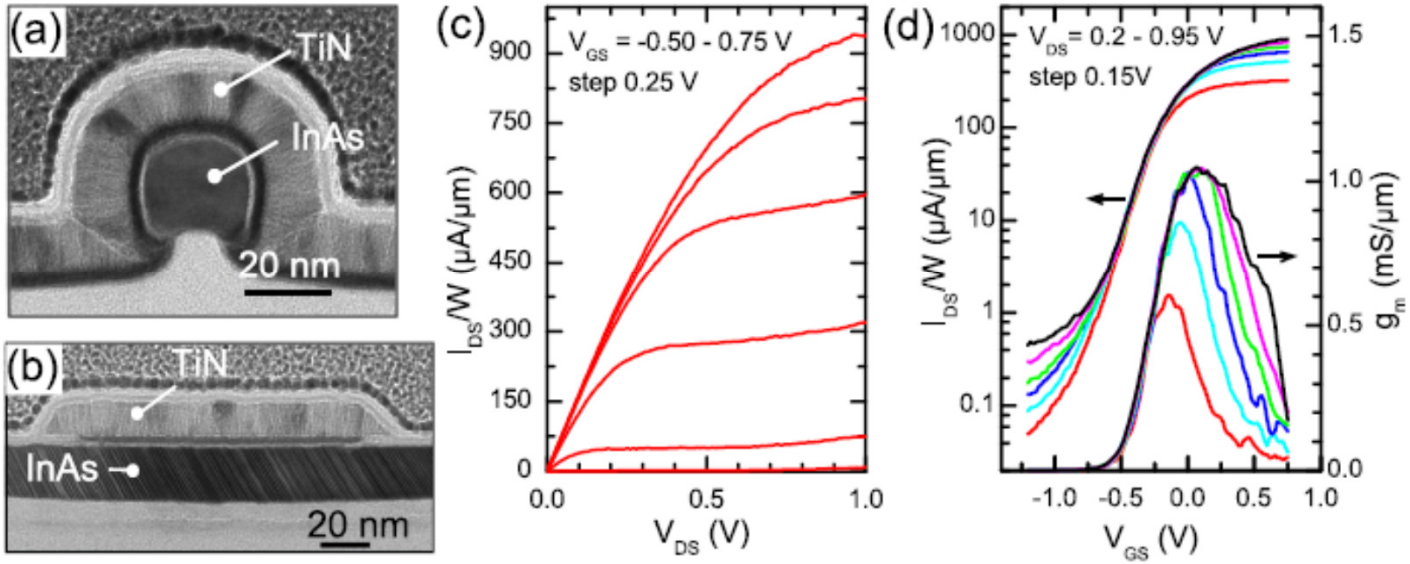

IBM, Czornomaz et al, IEEE VLSI Symp 2015




- First successful demonstration of co-integrated Si/III-V SRAMs with 150 nm gate length

# Defect – Electrical Correlation in III-V Nanowire MOSFETs on Si

IBM, Schmid et al, APL, 222101, 2015




- High $I_{on}$ / $I_{off}$ ratio (~ $10^4$) despite an extremely high density of planar defects (> $10^{10}$ $cm^{-2}$) in InAs nanowires

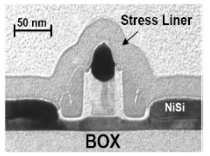
D K Sadana, IBM, CICC 2015

# Concluding Remarks

- Ground breaking progress in co-integrating high mobility non-Si channels in CMOS
- Various innovative III-V growth schemes on Si under investigation for defect reduction
- High performance self-aligned III-V MOSFETs operating at 0.5 V have been demonstrated using Si compatible processing
- Defects in co-integrated III-V may not be a show stopper for III-V technology development
- Demonstration of scaled device for 5 nm node is in progress
- Many challenges have yet to be overcome

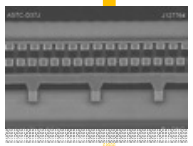
# Technology Innovations to Continue ….

Extending Si CMOS



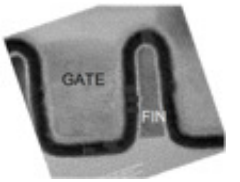

Strain Layers

High-k / Metal Gate



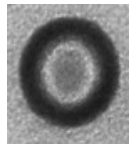
Interconnects / ULK Dielectric

SMO



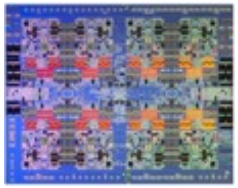

FINFETs

Si Nano-wires

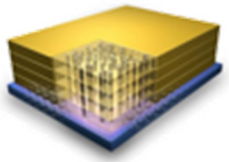


Subsystem Integration

eDRAM

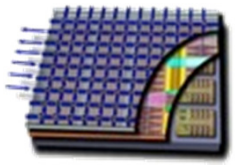


3Di

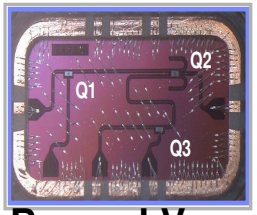


MRAM, PCM for SCM

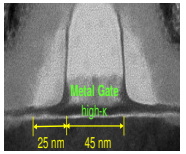

Silicon Photonics



Non-Si FET




Beyond Von-Neumann Architectures




III/V

Carbon Electronics

Beyond FET

D K Sadana, IBM, CICC 2015