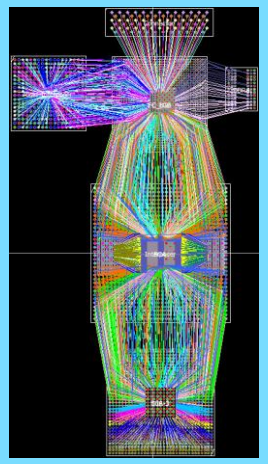
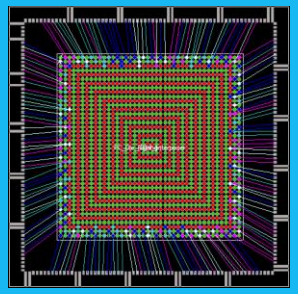
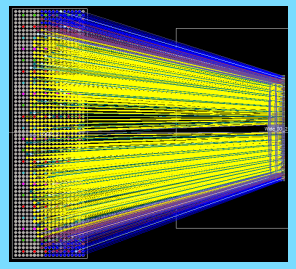


BroadPak

2.5D/3D Technologies



A Novel Low Cost, High Performance and Reliable Silicon Interposer



CONFIDENTIAL

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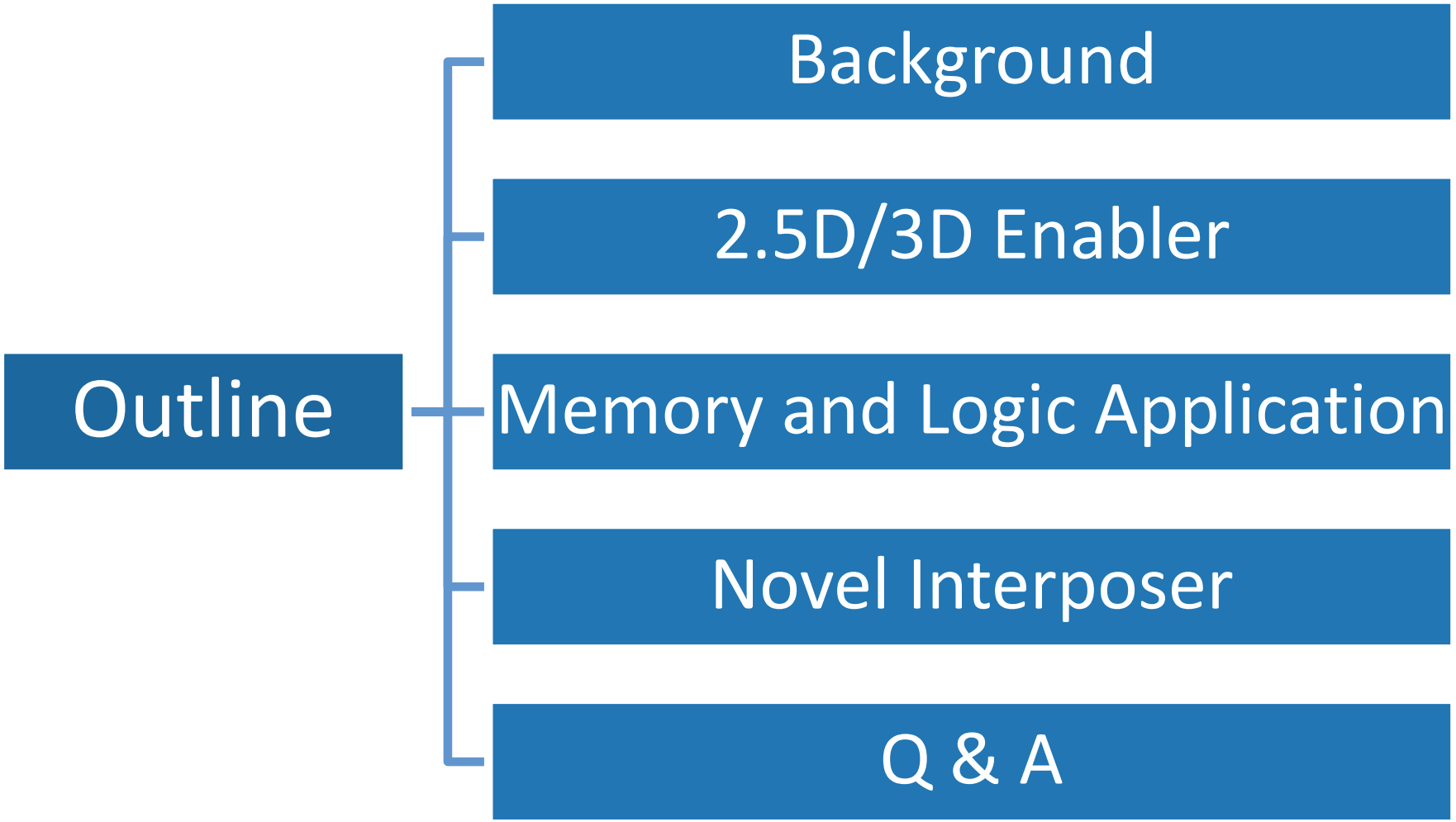
1735 N 1ST ST STE 301A
San Jose, California 95112
www.broadpak.com

Farhang Yazdani
President & CEO
farhang.yazdani@broadpak.com
Tel: (408) 922-9006

Agenda



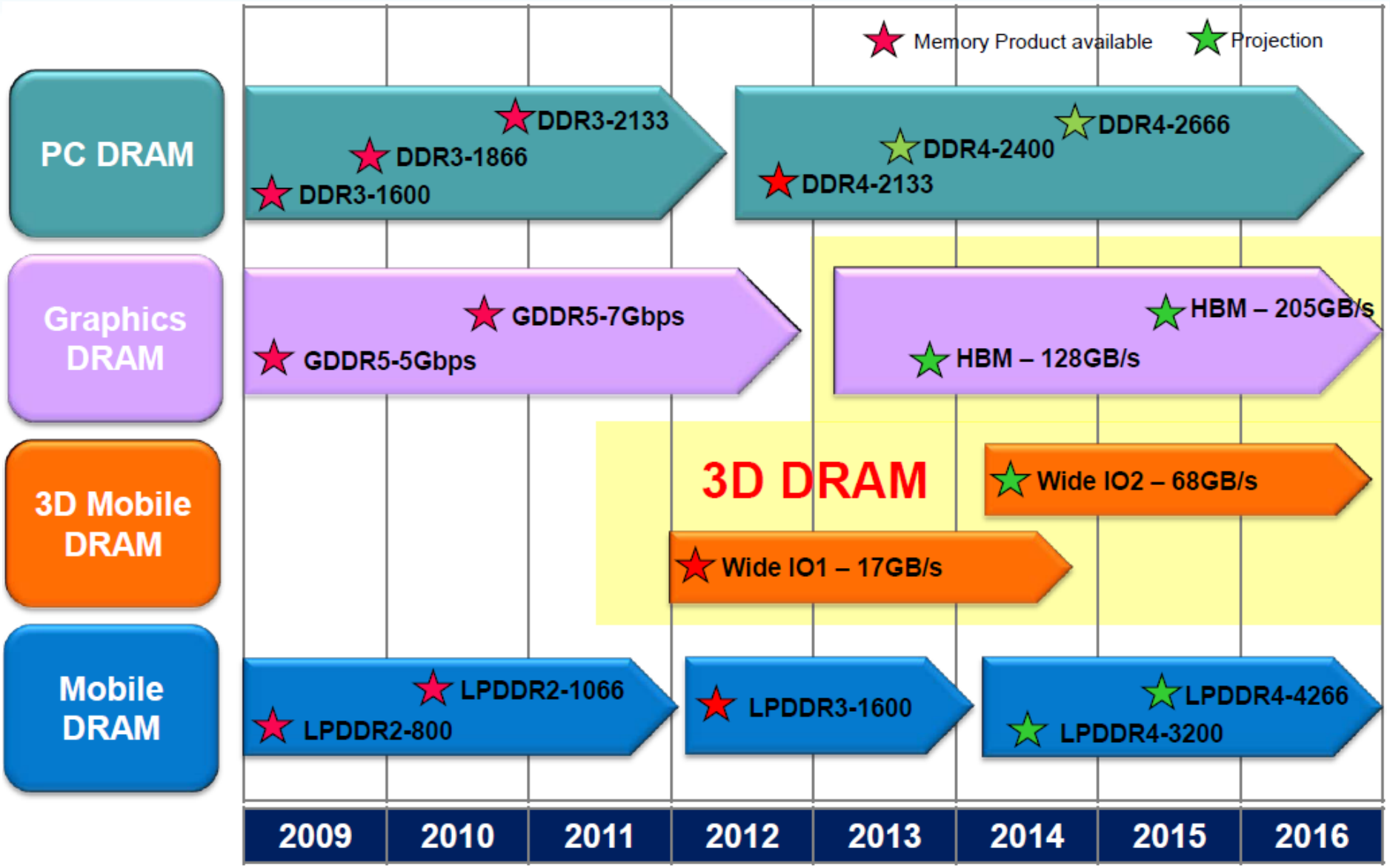
BroadPak Background

- **Founded: 2007**
- **Location: San Jose, California**
- **Services: Provider of total solution and technologies to develop and launch 2.5D/3D products.**
- **Customers: Major semiconductor players**

2.5D/3D Enabler

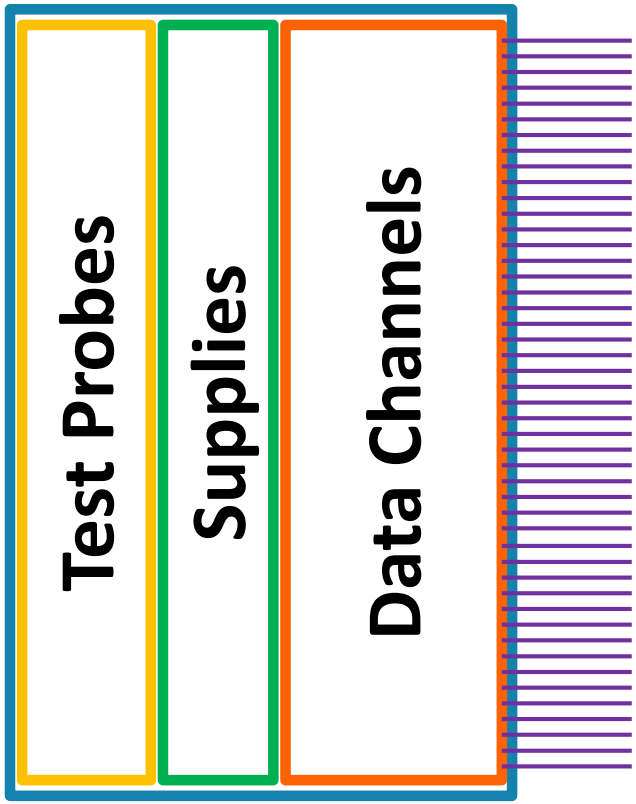
Memory Trends (Biggest Driver)

Source: http://www.jedec.org/sites/default/files/files/H_Vuong_Mobile_Forum_May_2013.pdf



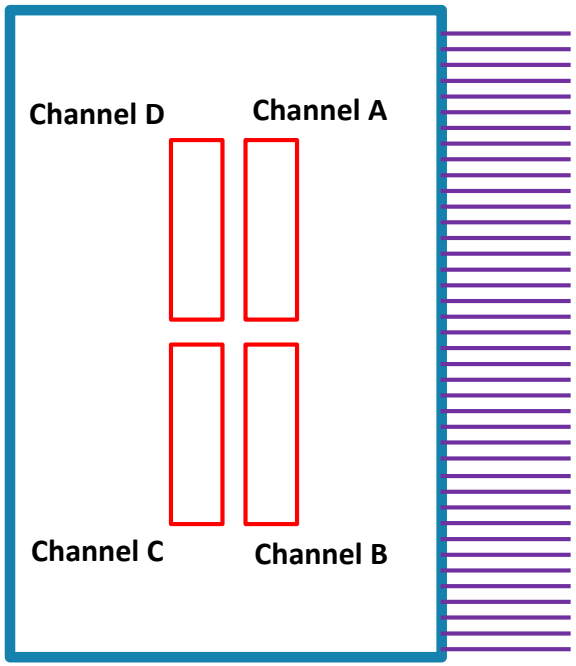
HBM (GEN2) VS. WIDE I/O (GEN2)

HBM



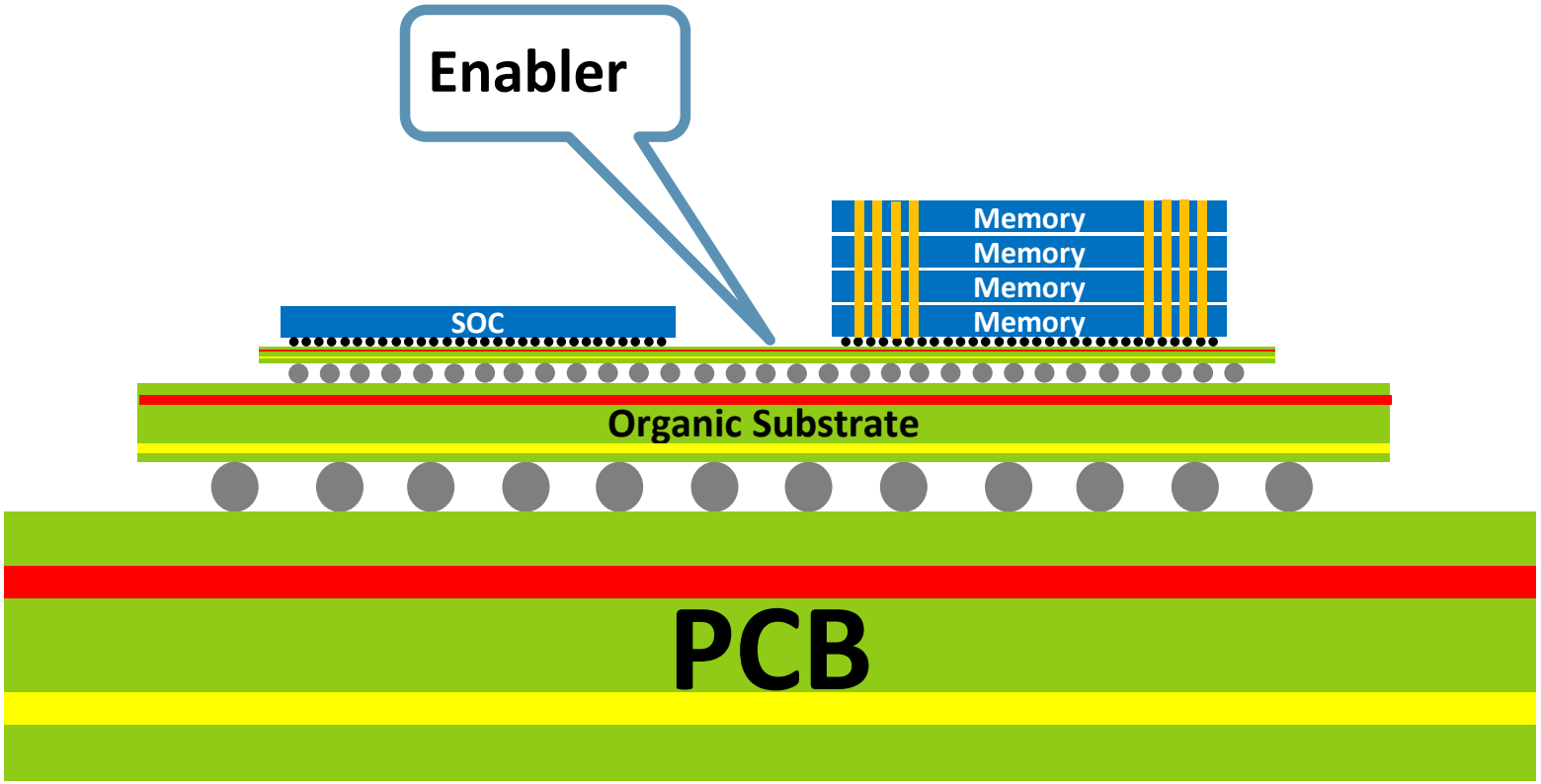
55um staggered bump pitch
Max BW: 256 GB/s
# of IO: ~1600 incl. supplies
1024 wide

Wide I/O



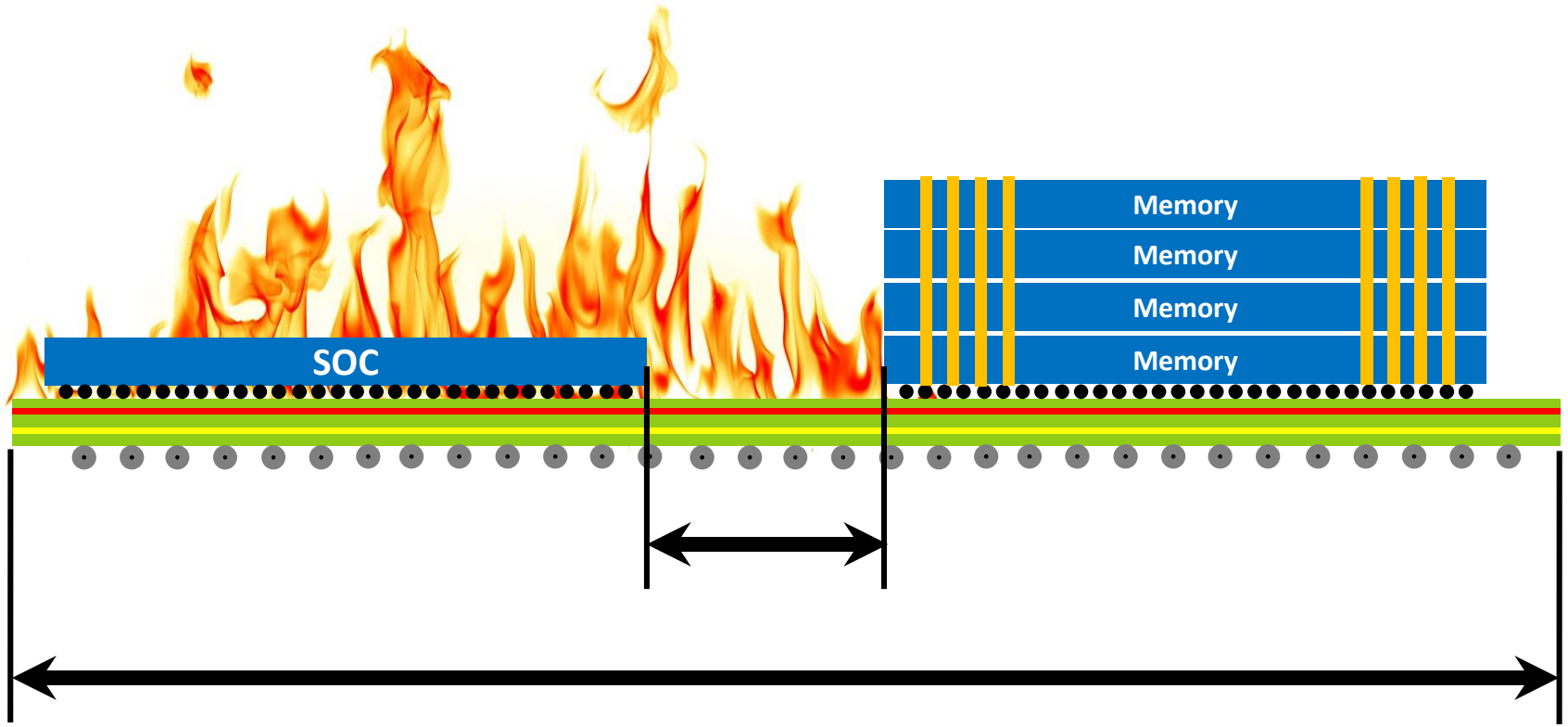
40um in-line bump pitch
Max BW: 68 GB/s
# of IO: ~1200 incl. supplies
512 wide

2.5D Memory & Logic (Big Picture)



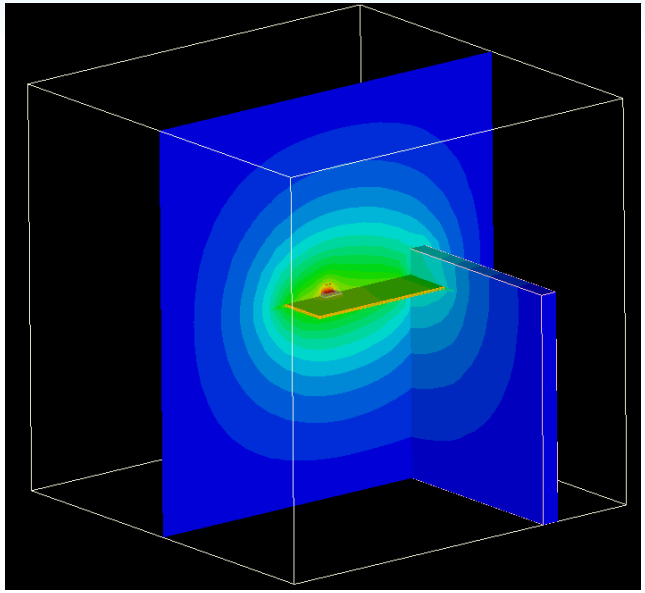
Thermal Impact

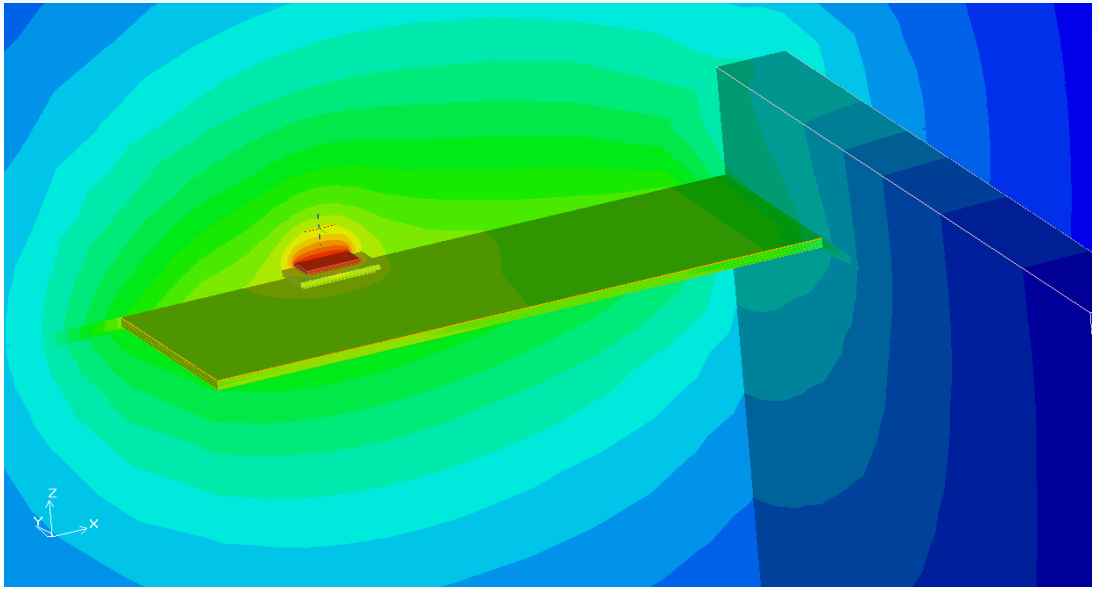
1) Thermal Impact (thermal coupling)
2) Thermal Stress Impact

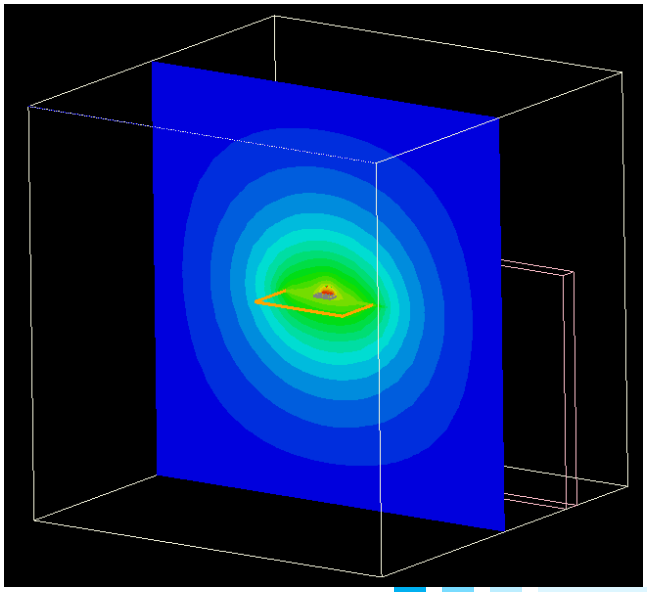


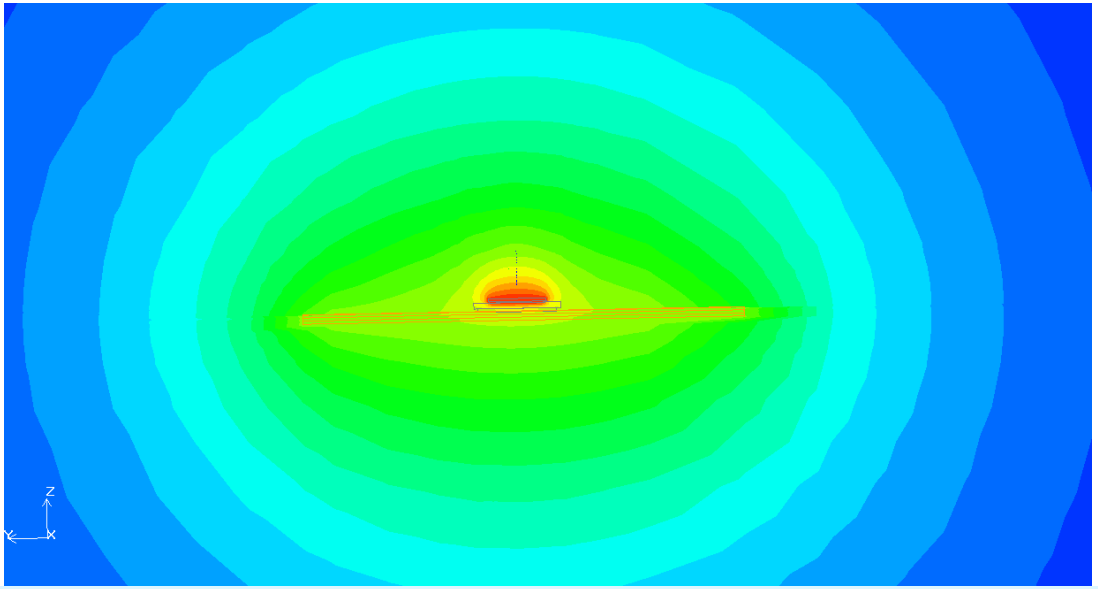
Fire image source: http://bisericaimpact.ro/blog/apropiere

Thermal Coupling

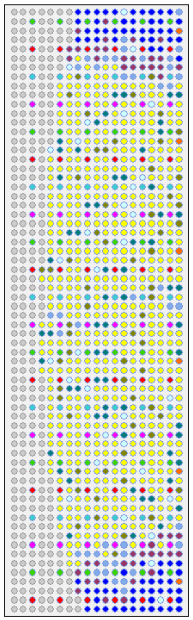


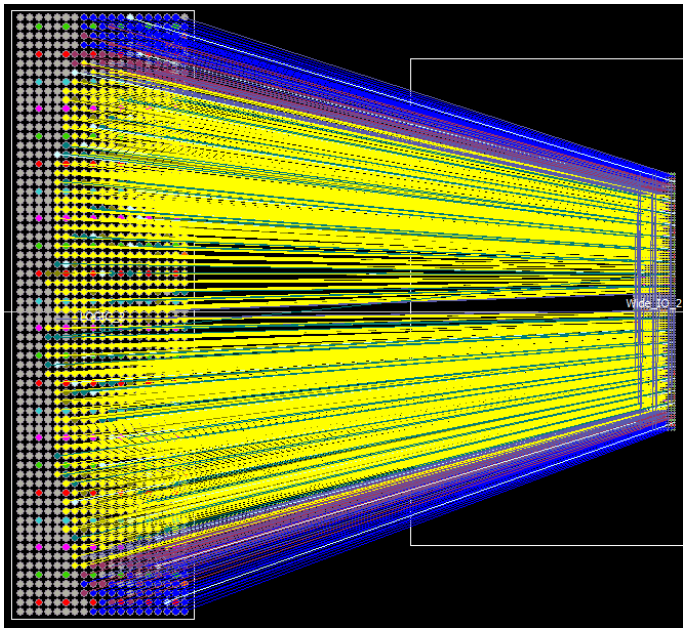


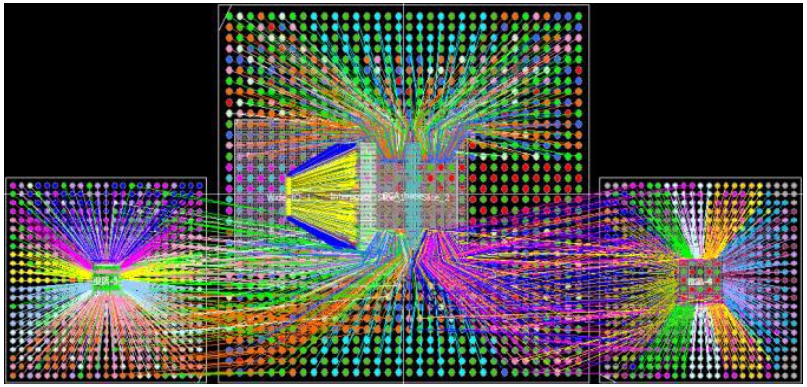




EXAMPLE: WIDE I/O TO SOC OPTIMIZATION







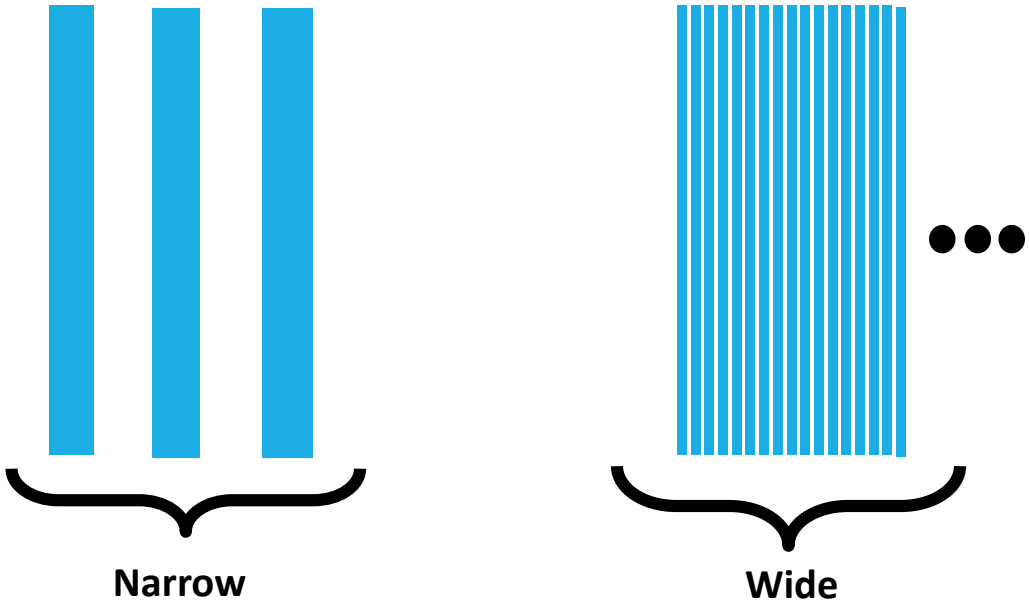
Interposers

Why Silicon?

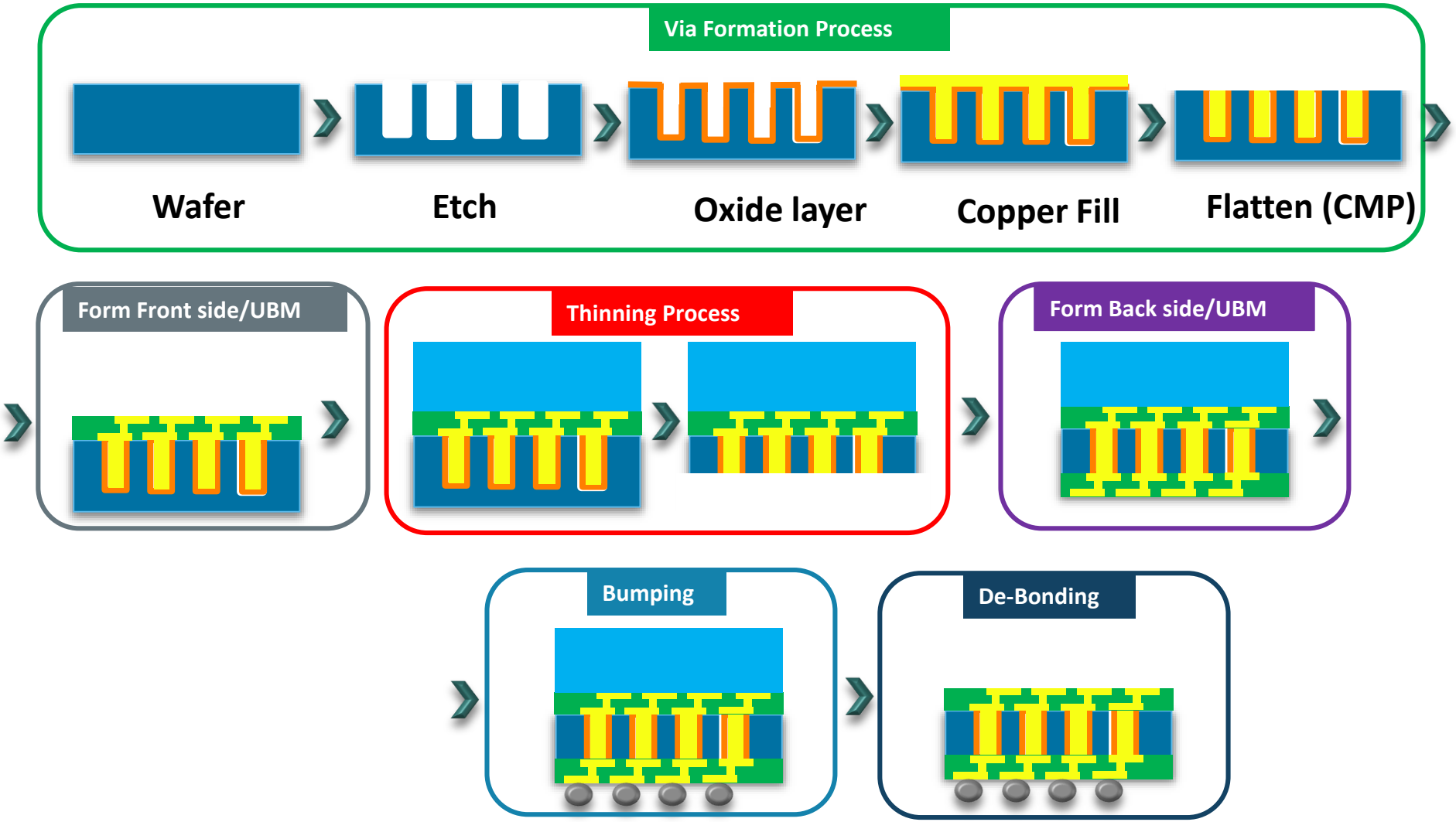
- Mature process
- Know how's
- High volume production
- Same CTE as chip
- Other options at R&D stage

INTERPOSER AS ENABLER!

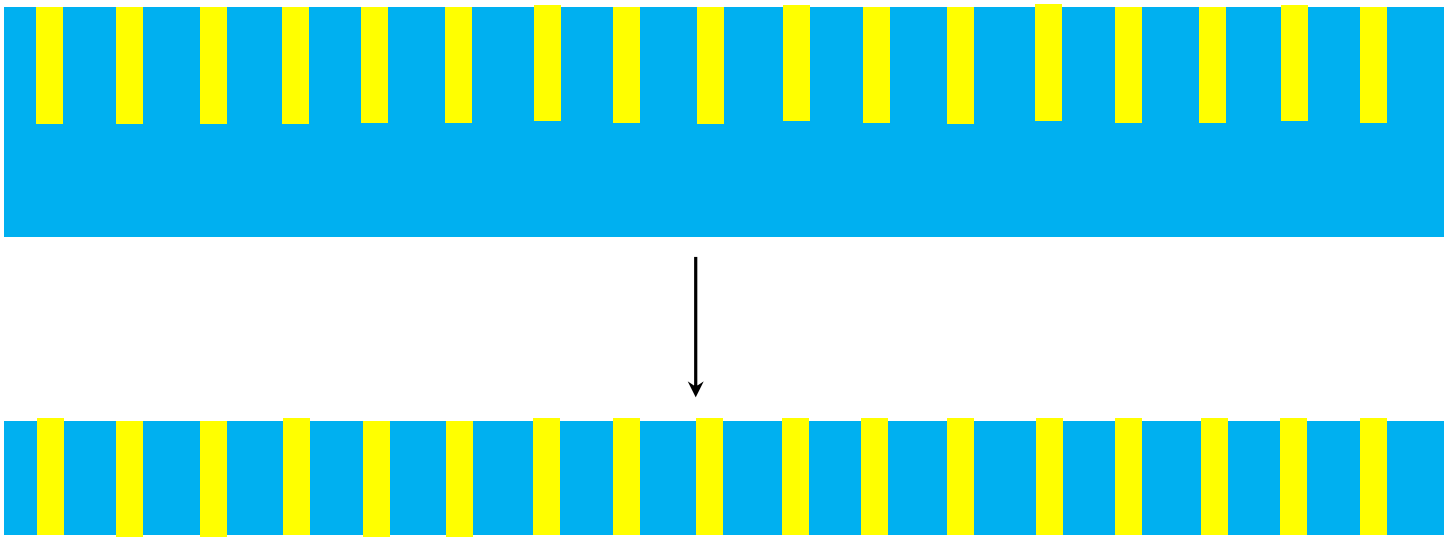
A super-wide bus compared to today's narrow channel



How Silicon Interposer is Made?



Thinning Process (TSV Reveal)!



KEY TECHNOLOGIES

- RDL (provides bandwidth)
  - Trace width and spacing
- TSV formation (impacts aspect ratio, i.e 10:100)
  - Diameter, depth, pitch
- Bonding and Debonding (impact yield)
- Back-grind (TSV reveal) (impact yield)
- Thin wafer handling (impact yield)
- Bumping (Cu pillar) (impact yield)

Path to Low Cost Silicon Interposer?

What do we hear about 2.5D/3D?

Pros

- Improves overall die yield
- lowers the power
- Allows mixed node
- Allows IP reuse
- Smaller footprint

Cons

- Expensive
- Limited in size
- Integration & Design
- Reliability
- KGD, Yield
- Test
- Supply Chain

Is it Doable?

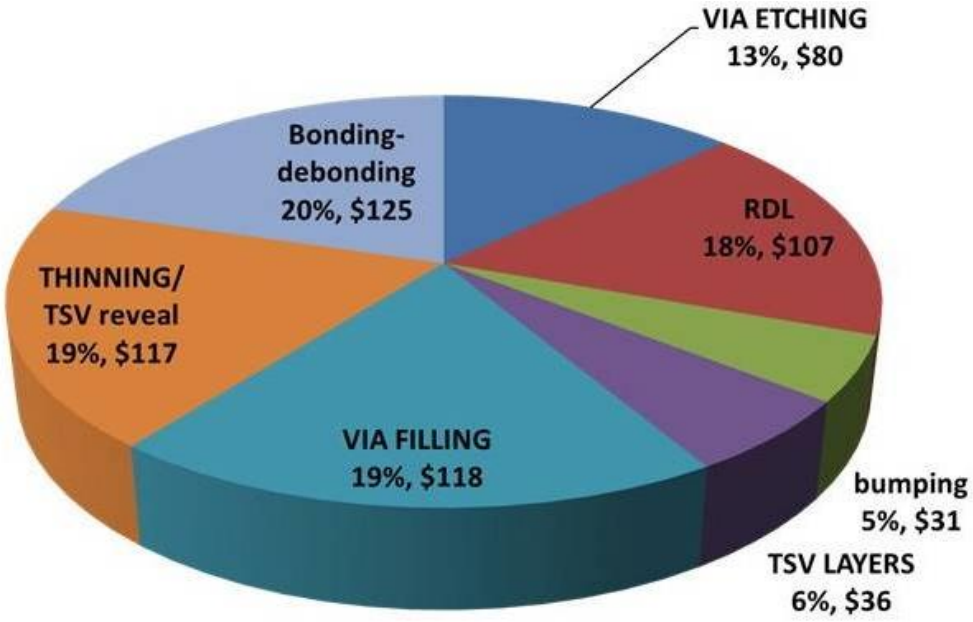
How to substantially reduce the cost while:

Improving reliability

Improving performance

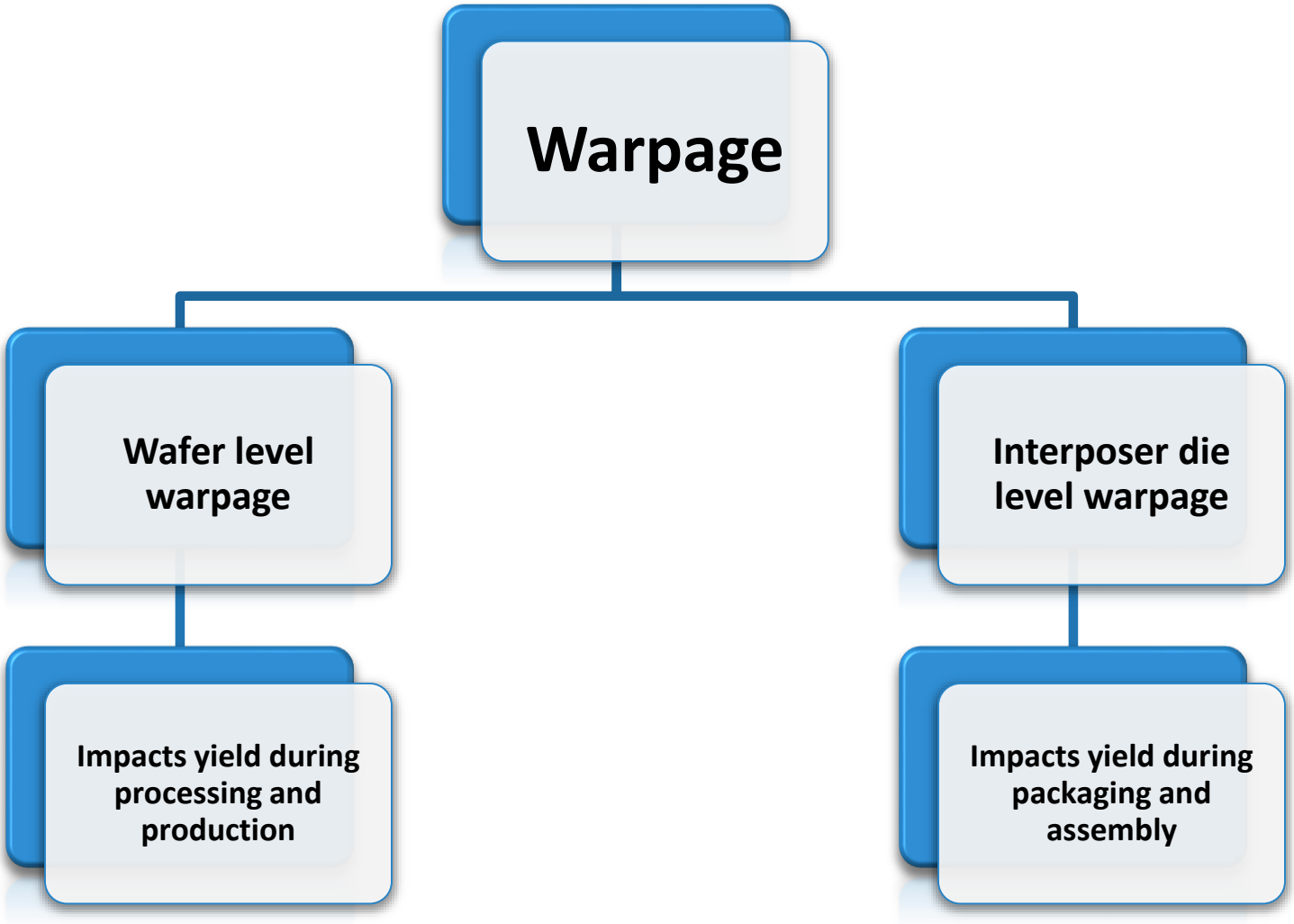
Study on Interposer Manufacturing Cost

Size: 31X31mm²
Thickness: 100um
Via Size: 12um
RDL: 3 copper damascene layers
Process Node: 65nm design rule for routing on top layer



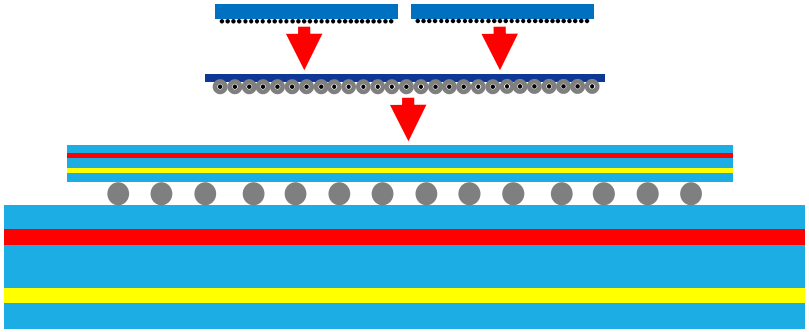
Source:
12/24/2012
By Dr. Phil Garrou
Lifting the veil on silicon interposer pricing - ElectroIQ
http://www.electroiq.com/articles/ap/2012/12/lifting-the-veil-on-silicon-interposer-pricing.html

Warpage, a Challenge!

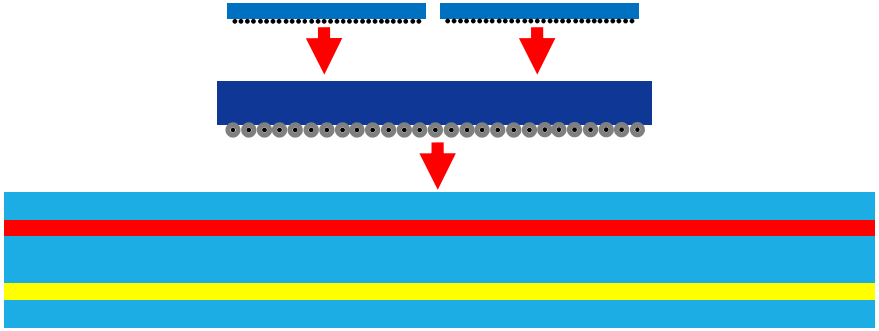


Thin VS Rigid Interposer Approach

Thin



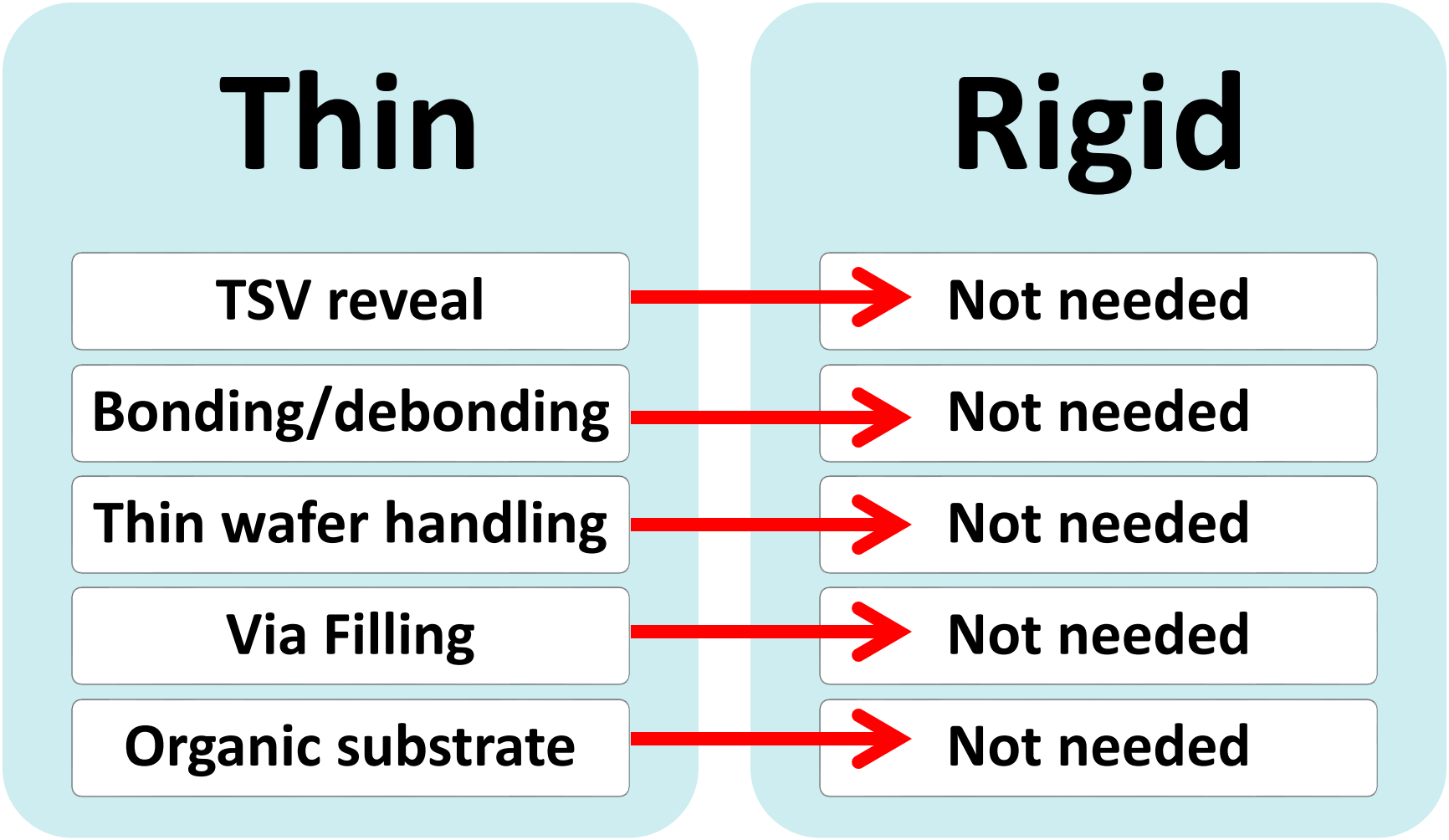
Rigid



An Integration that mitigates warpage

A simpler approach

Thin vs. Rigid Interposer

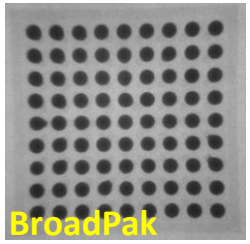


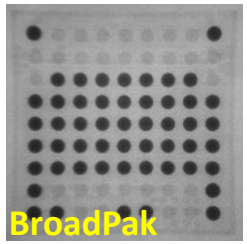
Test Vehicle

Farhang Yazdani, "Design and Direct Assembly of 2.5D/3D Rigid Silicon Interposer on PCB" Proceedings of *IMAPS 47th International Symposium on Microelectronics*, October 13-16, 2014, San Diego, CA, USA, pp. 783-786.

Test Vehicle Specification

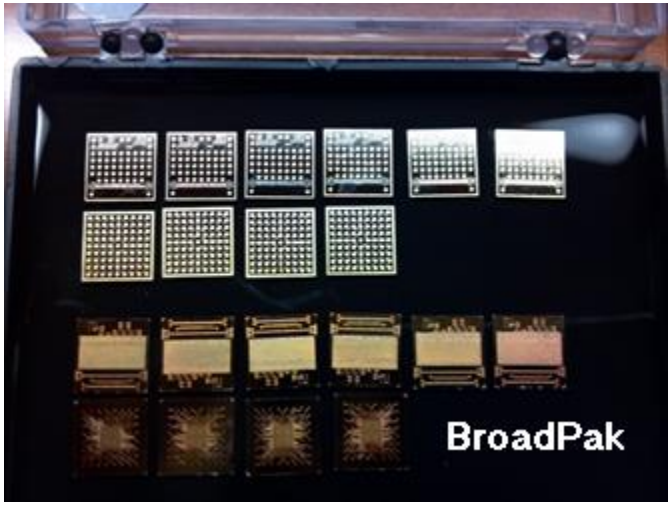
- 10mm X 10mm silicon interposer
- 1mm Ball pitch on the back side
- 50um pitch on the front side
- Two BGA ball patterns
  - Even BGA pattern
  - Odd BGA pattern



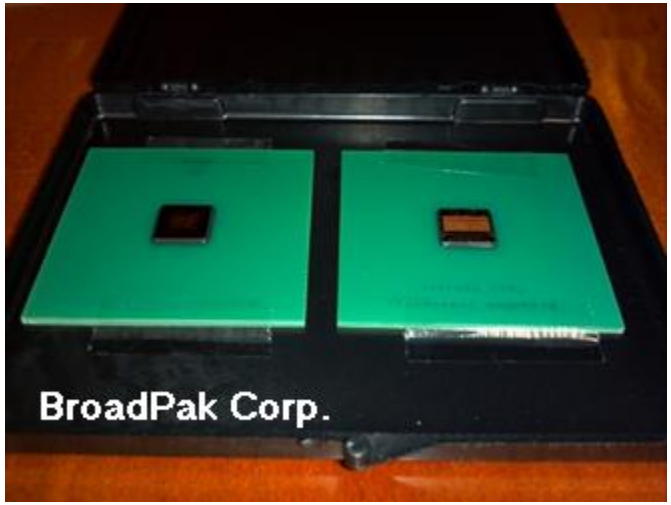


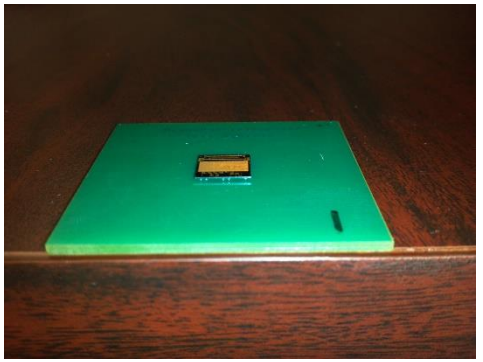
Manufacturing and Assembly

Manufactured



Assembled

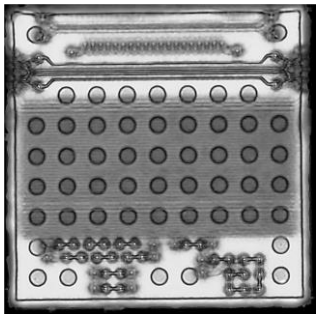




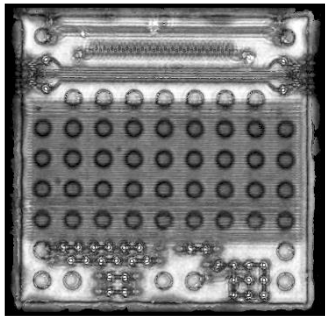
JEDEC Spec	JESD22-A104
Condition B	Temperature -55C to 125C
Temperature Cycle	2 times / hour
Duration	1000 Cycles
CSAM Inspections at	250, 500, 750 and 1000 cycles

Successfully Passed 1000 Temp Cycles

250 cycles

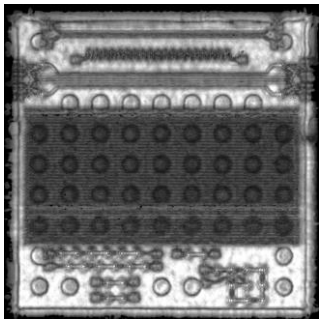


Without Underfill

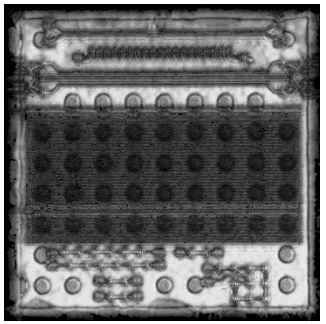


With Underfill

500 cycles

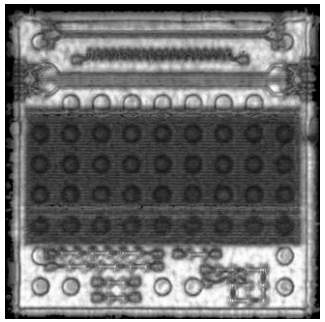


Without Underfill



With Underfill

750 cycles



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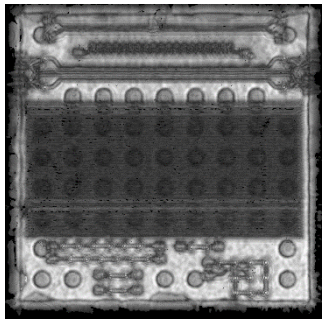
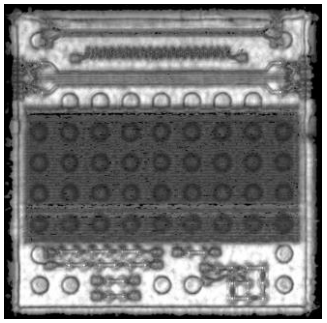


With Underfill

1000 cycles



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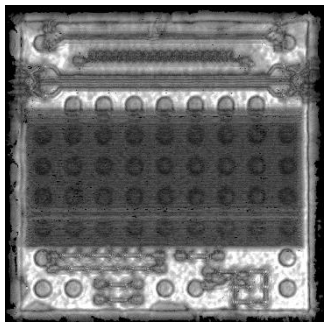

With Underfill

Summary

- Silicon interposer as enabler for 2.5D/3D memory and logic integration
- Structure and making of silicon interposer
- Path to low cost silicon interposer
- Thin verses rigid interposer
- Rigid interposer test vehicle manufacturing, assembly and reliability data.

THANK YOU