COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

Scaling Analog Circuits into Deep Nanoscale CMOS:

Obstacles & Ways to Overcome Them

Peter Kinget

Analog & RF IC Design Research

Columbia Integrated Systems Laboratory

http://www.cisl.columbia.edu

Outline

- Why ...
  - We have no choice
  - We can enable novel applications
- What are the obstacles

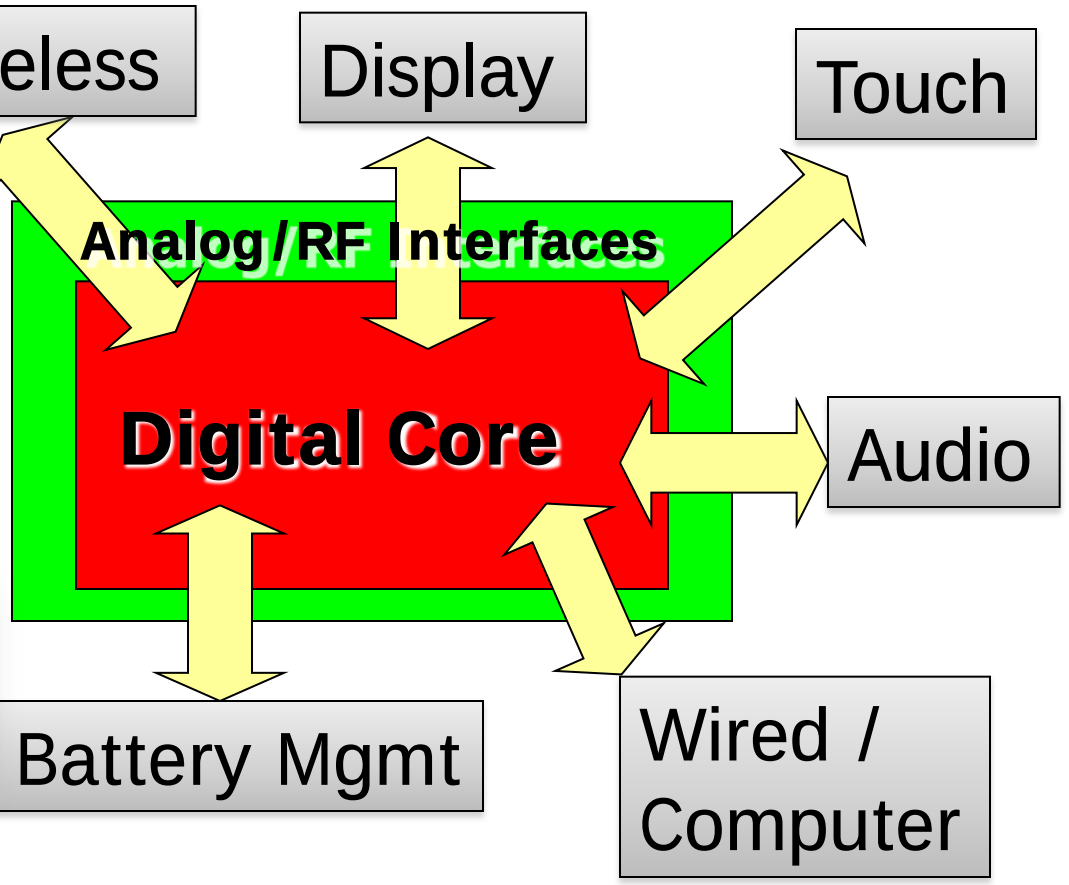
  when scaling analog circuits
- How ...
  - Solutions for analog circuits in nanoscale CMOS:
    - Scale V_{DD}, new architectures, use digital gates
  - Leveraging nanoscale CMOS in different ways
    - Novel circuits and analog information representation
- Outlook & Conclusions

Why?

What drives the need for scaling analog & RF circuits?

It's All About The Interfaces…

World is Analog * ^ % !! & * $

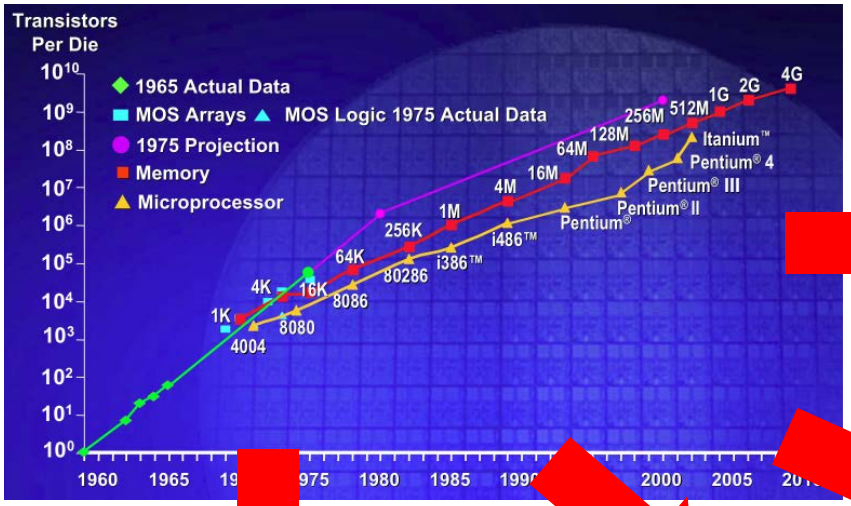


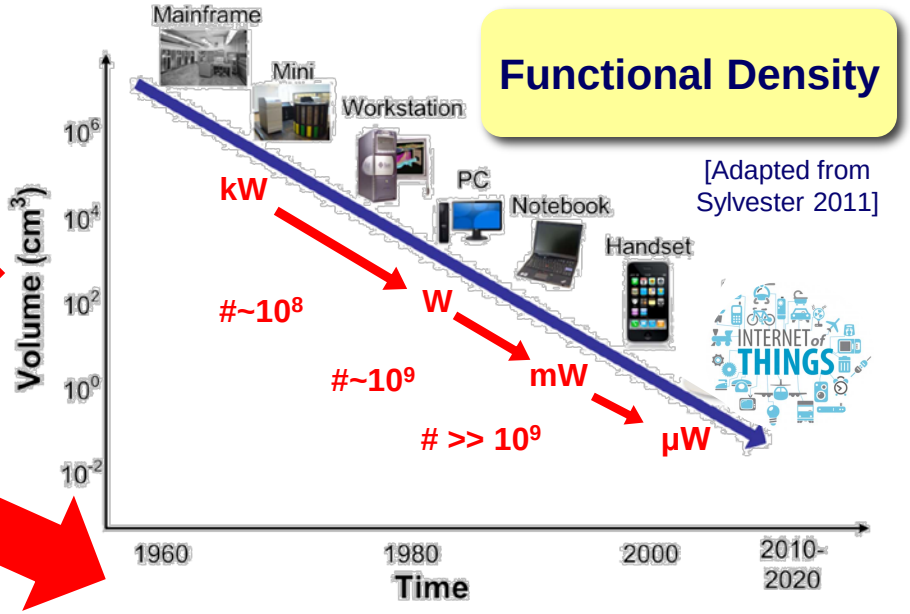
'Analog & RF connect the bits to life'

Why?

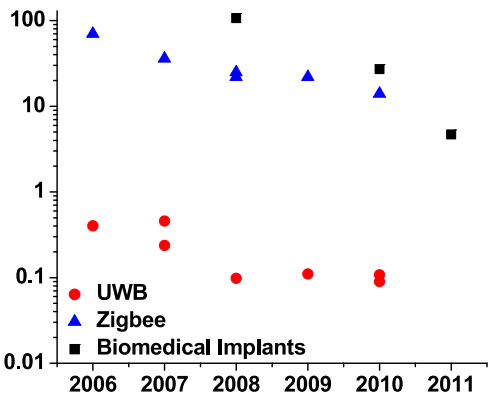
Scaled CMOS enables the creation of new classes of devices and applications

50 Years of Moore's Law: A Different Look



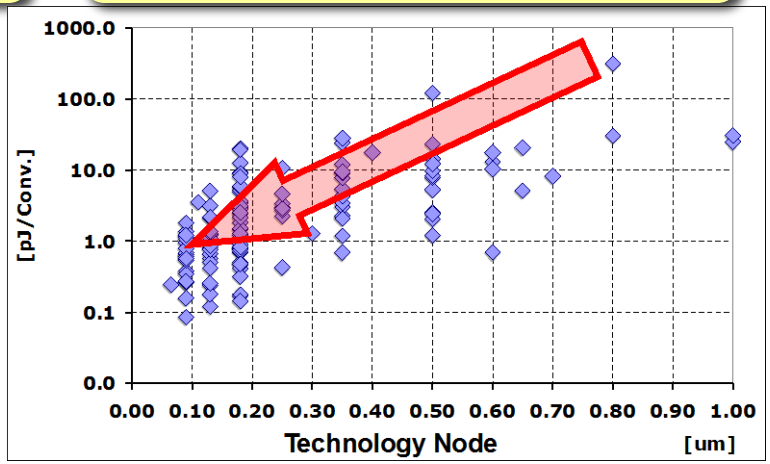


Short Range Wireless: Energy per bit

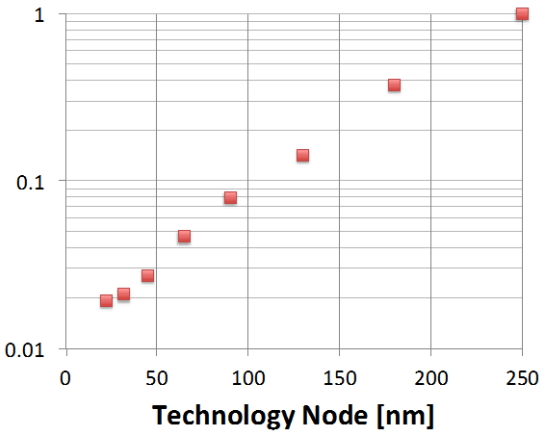


[Sylvester 2011]

Analog-to-Digital Conversion: Energy per Conv.

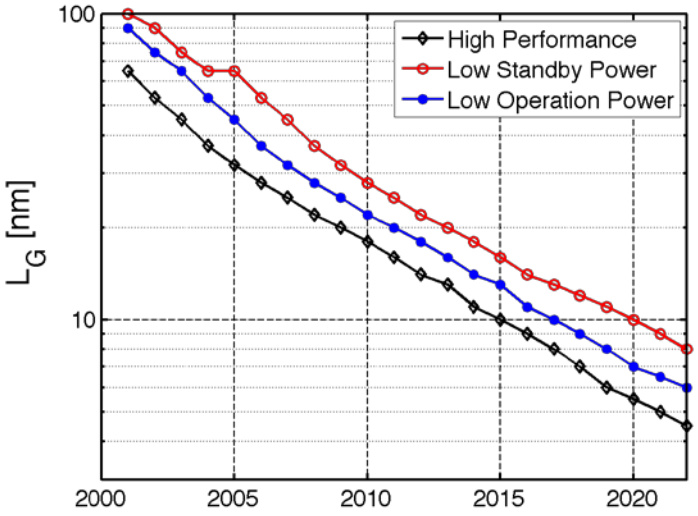


Computation: Energy per Operation

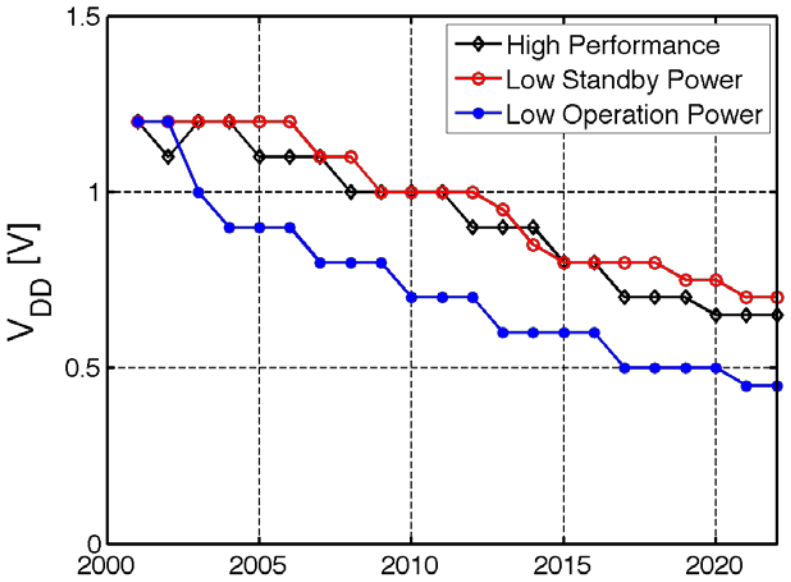


Scaling & Circuits

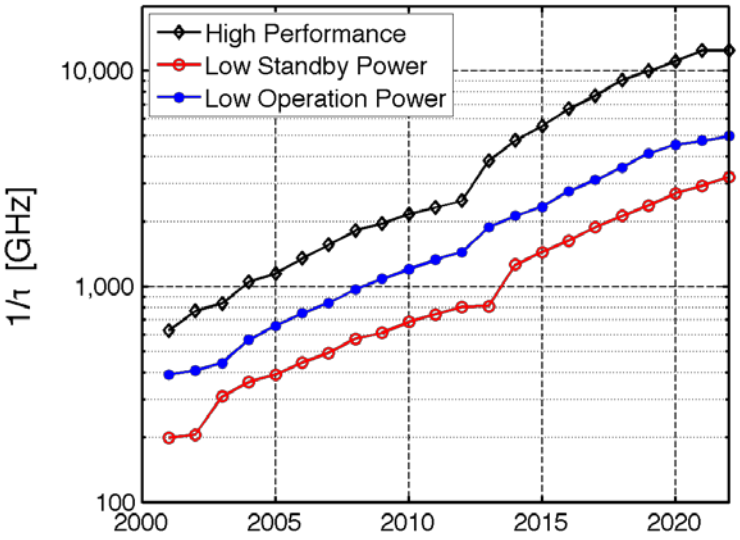
CMOS Scaling



Device speed & density ↑



Supply Voltage ↓



CMOS scaling is targeted at improving *digital performance*

[ITRS CMOS Roadmap]

Performance & Scaling

- **Digital** Performance Metrics

$$Power \propto f_{CLK} C_{gates} V_{DD}^2$$

$$Area \propto L_{min}^2$$

Device size scaling helps directly!

- **Analog** Performance Metrics

$$SNR \propto \left(\frac{V_{RMS}^2}{4 \cdot kT \cdot \Gamma \cdot 1/g_m \cdot BW} \right)$$

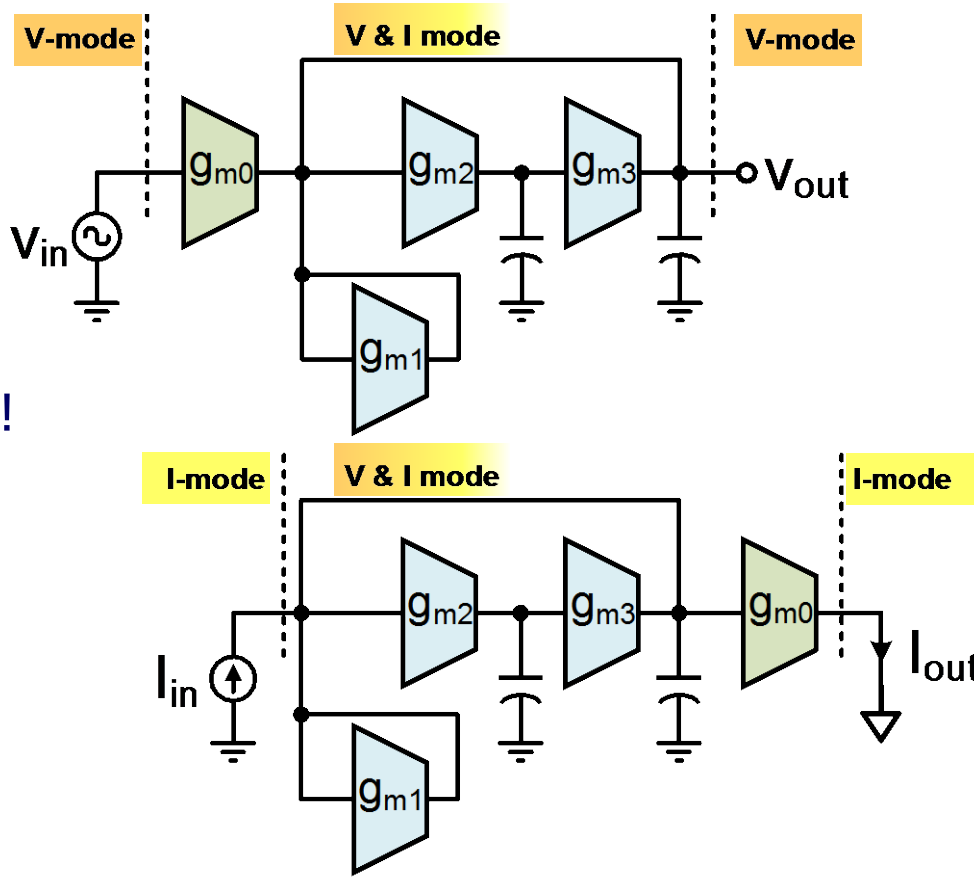
$$Power \propto kT \cdot BW \cdot SNR \cdot \left(\frac{1}{V_{DD}} \right) \cdot \frac{\Gamma}{\left(g_m / I \right)}$$

Device size scaling does not help directly!

Scaling means supply reduction, gain reduction, more leakage, more substrate & supply interference, more mismatch, more 1/f noise …

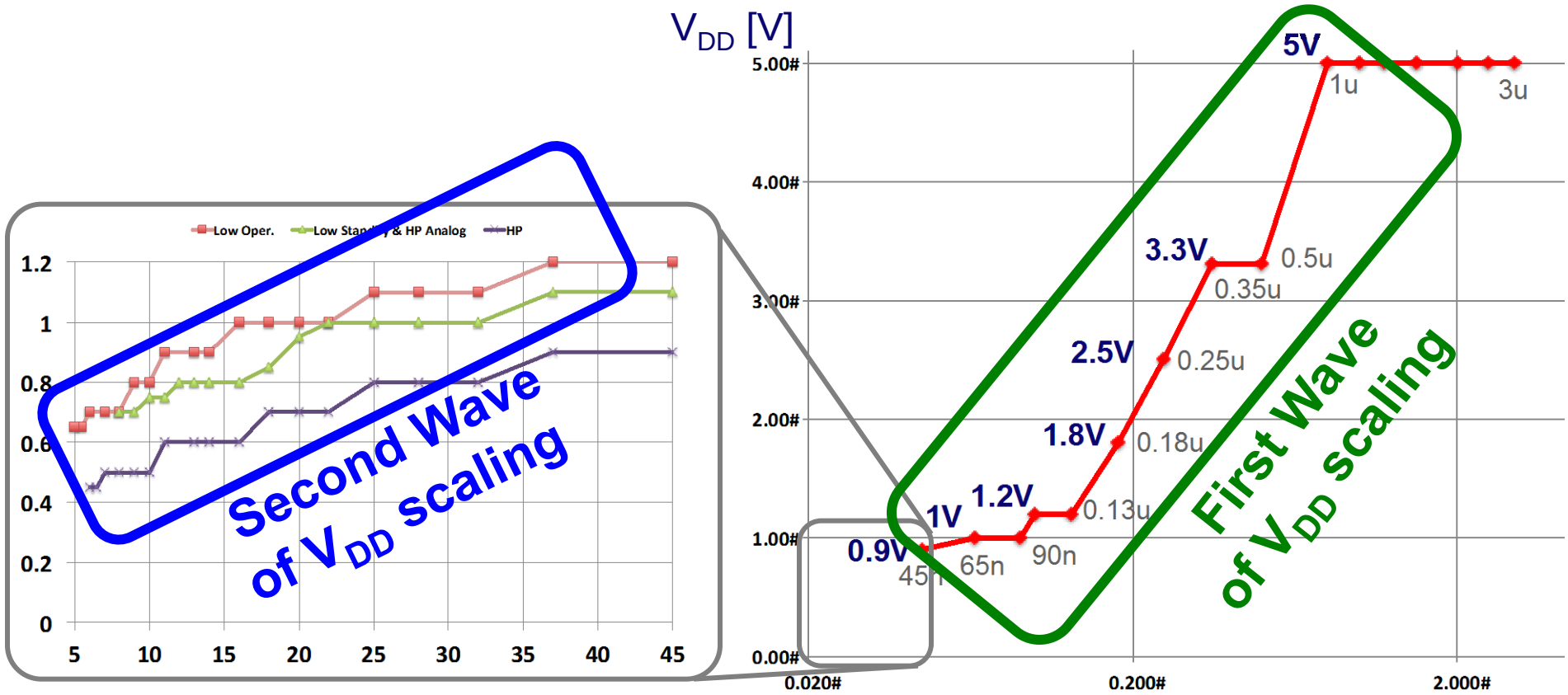
We Are Stuck With Voltages

- MOS transistor is V-I converter
  - Only a square i-v relationship (at best ...)
  - Always current & voltage mode!
  - Sub-threshold
    - Exponential i-v
    - But, low f_T
- Power supplies are voltage ...
- Most sensors, signal sources are voltage ...



- But, there are some new interesting opportunities

V_{DD} Scaling

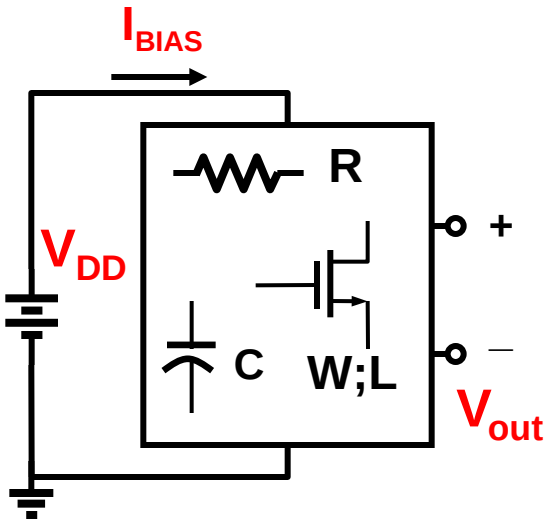


[Kinget ESSCIRC13]

Scaling the Analog V_{DD}

What to expect

A-V_{DD} Scaling: Constant g_m / I_D

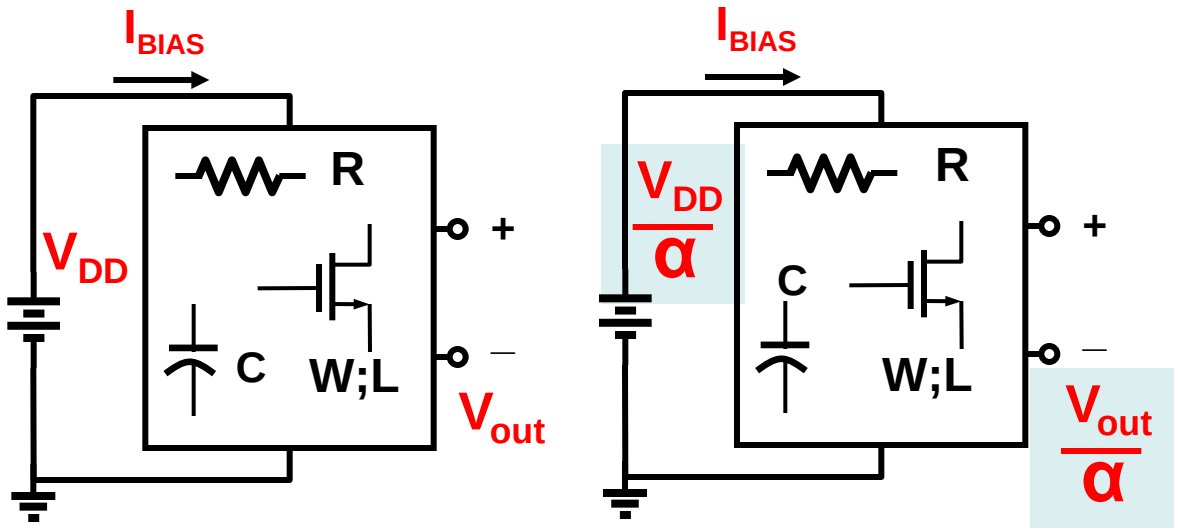


Constant BW scaling

$\sigma^2(V_n) \approx kT/C$
$\sigma^2(V_{OS}) \approx A^2_{VT}/(WL)$
$SNR \approx V^2_{out}/\sigma^2(V_n)$
$Acc. \approx V^2_{out}/\sigma^2(V_{OS})$
$P = I_{BIAS} V_{DD}$
Area

Caution: only first order approximations!!

A-V_{DD} Scaling: Constant g_m / I_D

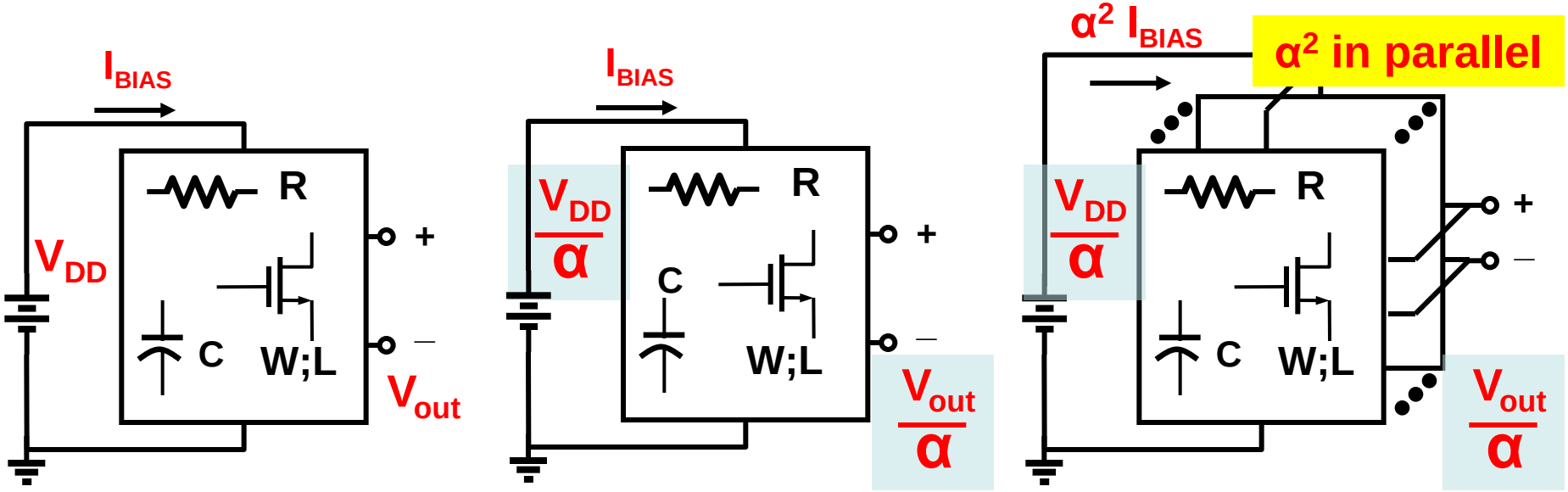


Constant BW scaling

$\sigma^2(V_n) \approx kT/C$	$\sigma^2(V_n)$
$\sigma^2(V_{OS}) \approx A^2_{VT}/(WL)$	$\sigma^2(V_{OS})$
$SNR \approx V^2_{out}/\sigma^2(V_n)$	SNR / α^2
$Acc. \approx V^2_{out}/\sigma^2(V_{OS})$	Accuracy / α^2
$P = I_{BIAS} V_{DD}$	P / α
Area	Area

Caution: only first order approximations!!

A-V_{DD} Scaling: Constant g_m / I_D

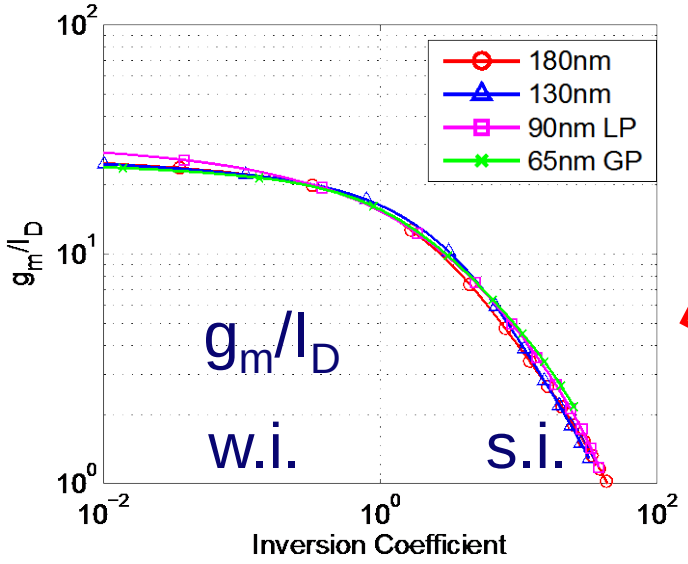


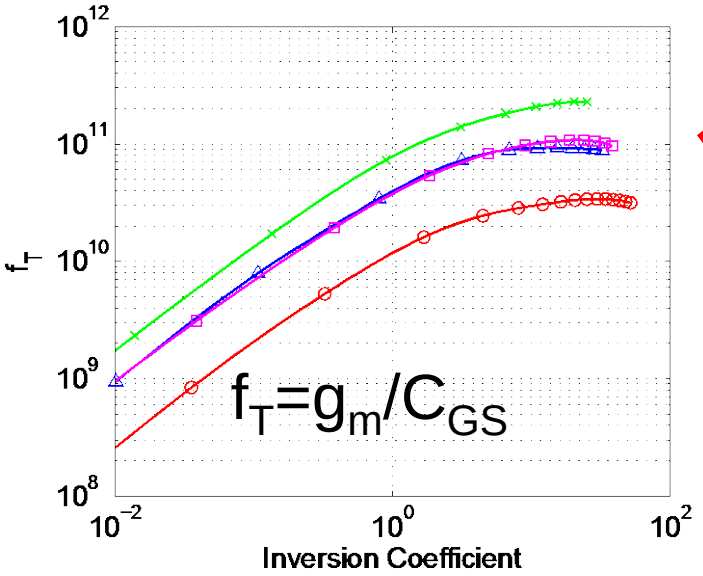
Constant BW scaling

$\sigma^2(V_n) \approx kT/C$	$\sigma^2(V_n)$	$\sigma^2(V_n) / \alpha^2$
$\sigma^2(V_{OS}) \approx A^2_{VT}/(WL)$	$\sigma^2(V_{OS})$	$\sigma^2(V_{OS}) / \alpha^2$
$SNR \approx V^2_{out}/\sigma^2(V_n)$	SNR / α^2	SNR
$Acc. \approx V^2_{out}/\sigma^2(V_{OS})$	Accuracy / α^2	Accuracy
$P = I_{BIAS} V_{DD}$	P / α	P α
Area	Area	Area α^2

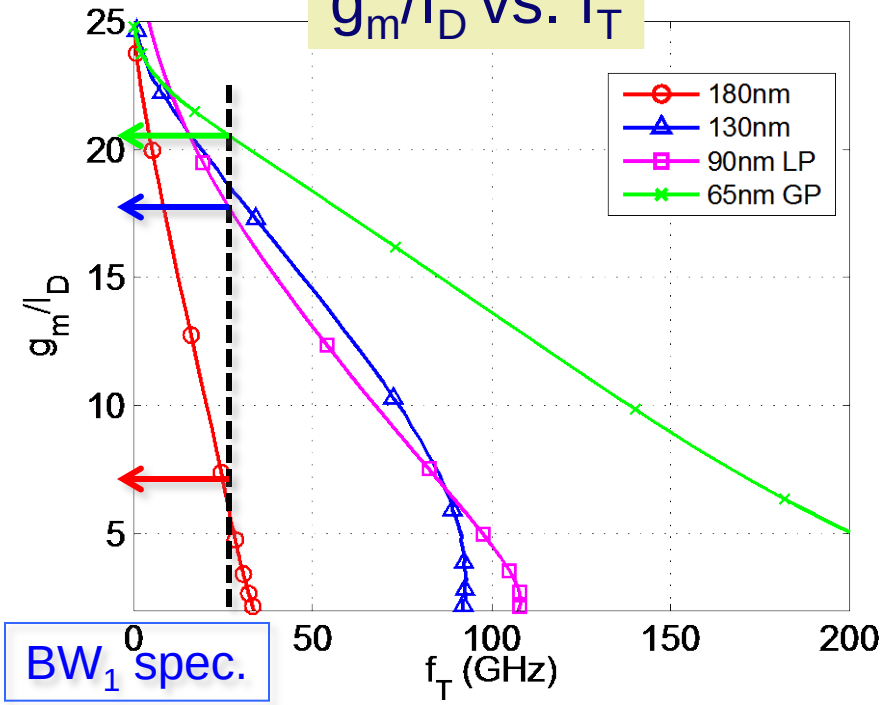
Caution: only first order approximations!!

Analog Perspective on Technology Scaling



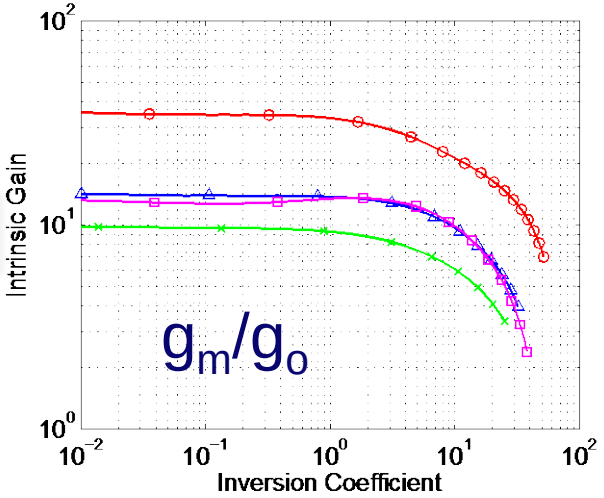


g_m/I_D vs. f_T



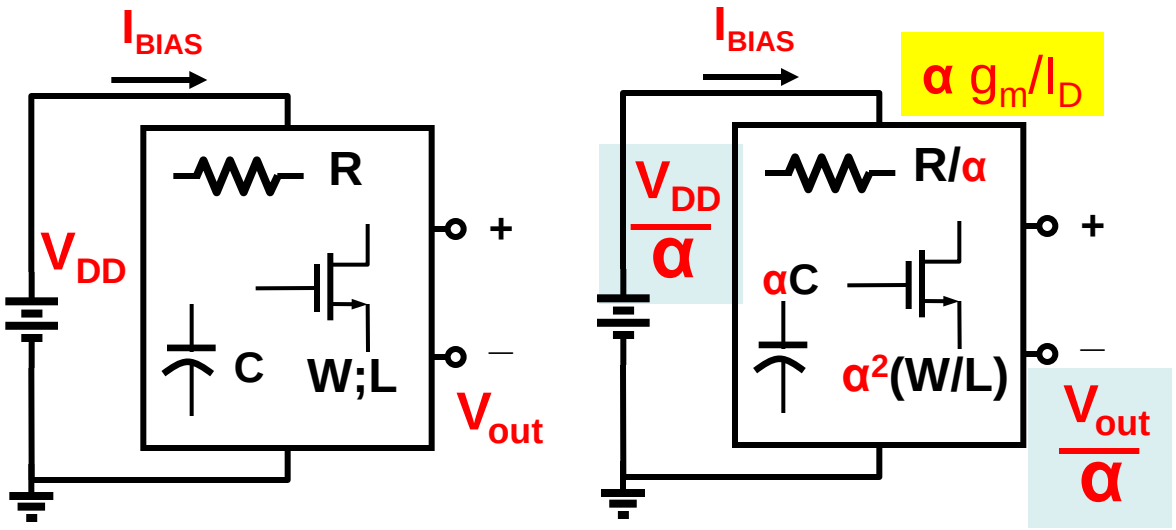
BW_1 spec.

Gain



[Kinget ESSCIRC13]

A-V_{DD} Scaling: Scaling g_m / I_D

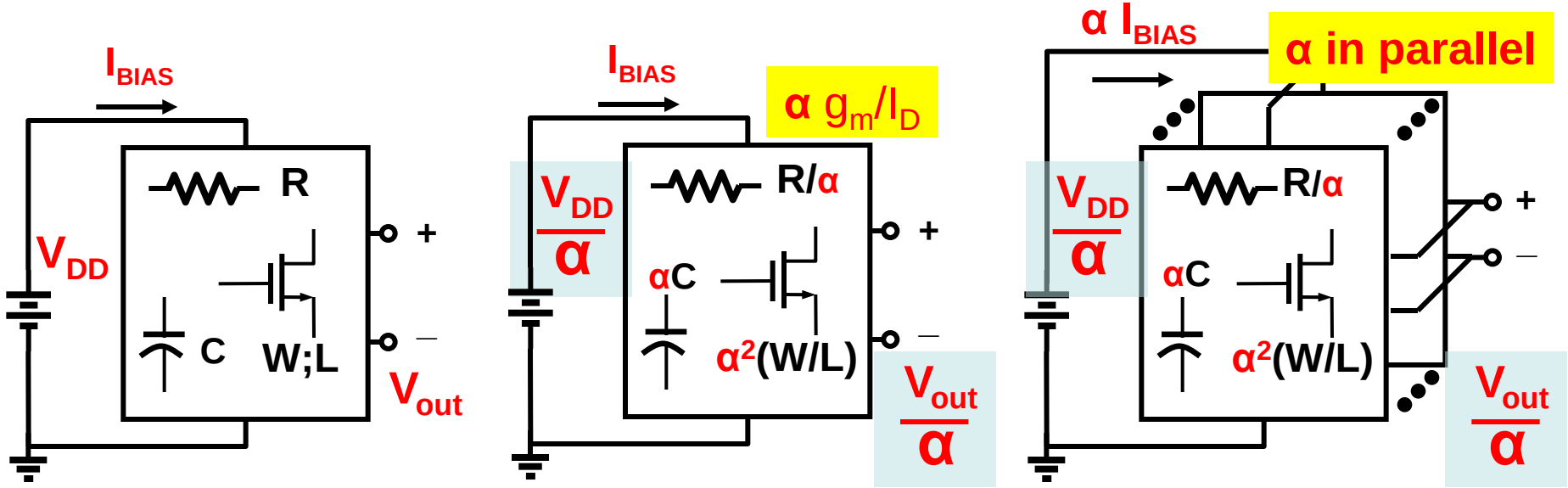


Constant BW scaling

$\sigma^2(V_n) \approx kT/C$	$\sigma^2(V_n)/\ \alpha$
$\sigma^2(V_{OS}) \approx A^2_{VT}/(WL)$	$\sigma^2(V_{OS})$?
$SNR \approx V^2_{out}/\sigma^2(V_n)$	SNR / α
$Acc. \approx V^2_{out}/\sigma^2(V_{OS})$	Accuracy ?
$P = I_{BIAS}\, V_{DD}$	P / α
Area	Area α

Caution: only first order approximations!!

A-V_{DD} Scaling: Scaling g_m / I_D

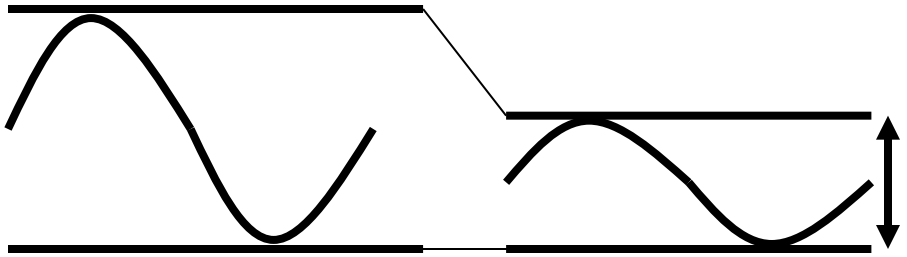


Constant BW scaling

$\sigma^2(V_n) \approx kT/C$	$\sigma^2(V_n)/\ \alpha$	$\sigma^2(V_n)\ /\ \alpha^2$
$\sigma^2(V_{OS}) \approx A^2_{VT}/(WL)$	$\sigma^2(V_{OS})$?	$\sigma^2(V_{OS})$?
$SNR \approx V^2_{out}/\sigma^2(V_n)$	SNR / α	SNR
$Acc. \approx V^2_{out}/\sigma^2(V_{OS})$	Accuracy ?	Accuracy ?
$P = I_{BIAS}\ V_{DD}$	P / α	P
Area	Area α	Area α^2

Caution: only first order approximations!!

Theoretical Power Limits for Analog



$$V_{DD} = 2\sqrt{2}\,V_{RMS}$$

- Noise limited circuits [Vittoz90]:

Independent of V_{DD}

$$SNR = \frac{V_{RMS}^2}{v_{n,RMS}^2} \qquad \overline{v_{n,RMS}^2} = \frac{kT}{C} \qquad I_{DC} = 2 f C \sqrt{2} V_{RMS}$$

$$P \geq 8\, kT\, f\, SNR$$

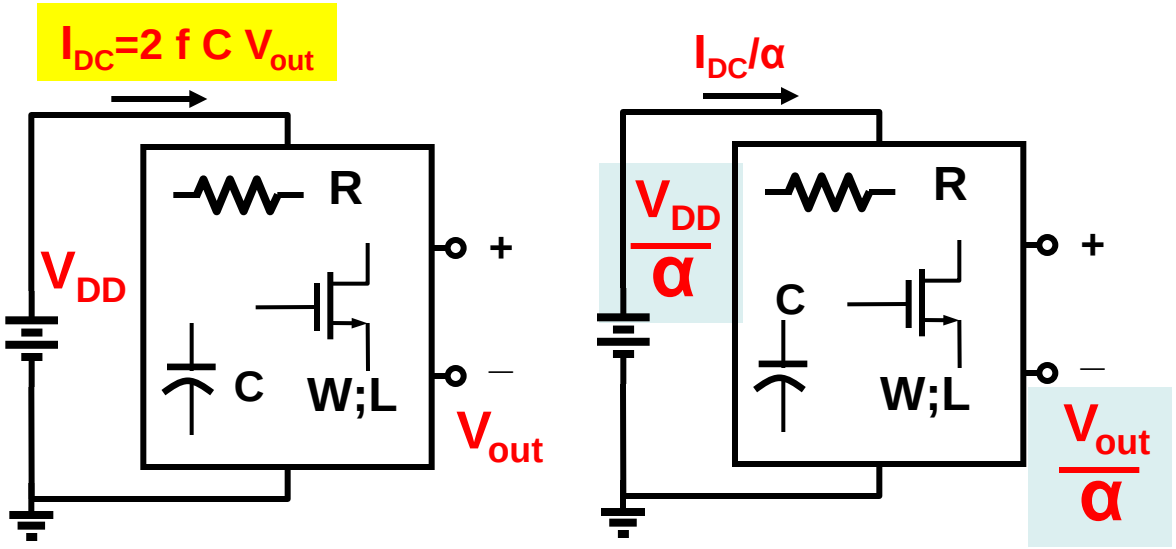
ideal class B & Load Dominated

- Mismatch limited circuits [Kinget96,05]:

$$Acc = \frac{V_{RMS}^2}{3\sigma^2(V_{os})} \qquad \sigma^2(V_{os}) = \frac{C_{ox} A_{VT}^2}{C} \qquad I_{DC} = 2 f C \sqrt{2} V_{RMS}$$

$$P \geq 24\, C_{ox}\, A_{VT}^2\, f\, Acc$$

A-V_{DD} Scaling: Load Dom. Scaling

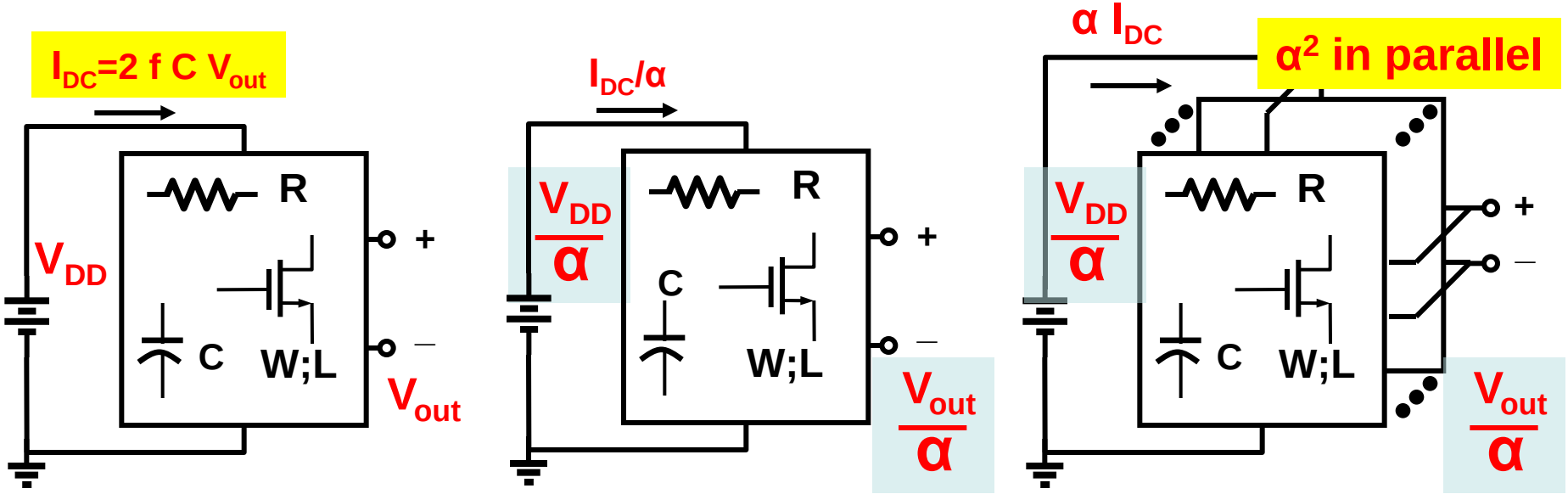


Constant BW scaling

$\sigma^2(V_n) \approx kT/C$	$\sigma^2(V_n)$
$\sigma^2(V_{OS}) \approx A^2_{VT}/(WL)$	$\sigma^2(V_{OS})$?
$SNR \approx V^2_{out}/\sigma^2(V_n)$	SNR / α^2
Acc. $\approx V^2_{out}/\sigma^2(V_{OS})$	Accuracy / α^2
$P = I_{DC} V_{DD}$	P / α^2
Area	Area

Caution: only first order approximations!!

A-V_{DD} Scaling: Load Dom. Scaling



Constant BW scaling

$\sigma^2(V_n) \approx kT/C$	$\sigma^2(V_n)$	$\sigma^2(V_n)$ / α^2
$\sigma^2(V_{OS}) \approx A^2_{VT}/(WL)$	$\sigma^2(V_{OS})$?	$\sigma^2(V_{OS})$ / α^2
$SNR \approx V^2_{out}/\sigma^2(V_n)$	SNR / α^2	SNR
$Acc. \approx V^2_{out}/\sigma^2(V_{OS})$	Accuracy / α^2	Accuracy
$P = I_{DC} V_{DD}$	P / α^2	P
Area	Area	Area α^2

Caution: only first order approximations!!

Analog V_{DD} Downscaling Strategies

Fixed BW & SNR performance target

1. Fixed g_m/I_D
   - "W-scaling" ➔ Power ⇑ & Area ⇑⇑
2. Scaling g_m/I_D
   - "W/L & W-scaling" ➔ Power ⇔ & Area ⇑⇑ (?)
3. Load dominated scaling
   - "Ideal Scaling" ➔ Power ⇔ & Area ⇑⇑

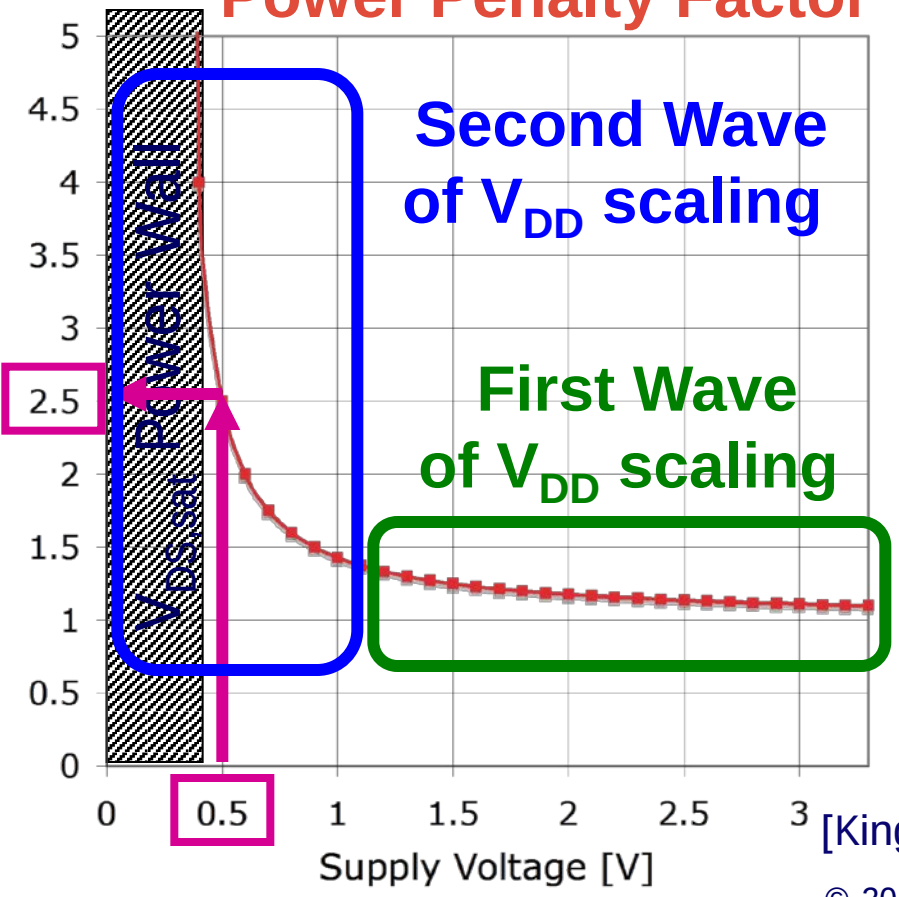
Caveat: for area, we assumed constant fF/μm^2

$V_{DS,sat}$ Power Wall

$$P \geq 8\,kT\,f\,SNR\left(1+\frac{2V_{DS,sat}}{V_{DD}-2V_{DS,sat}}\right)$$

Power Penalty Factor

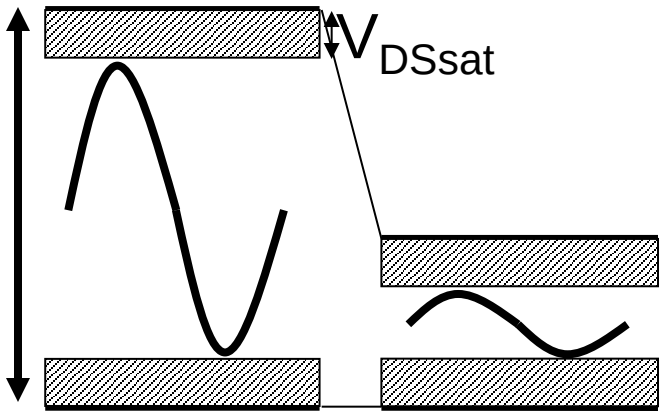
Power Penalty Factor



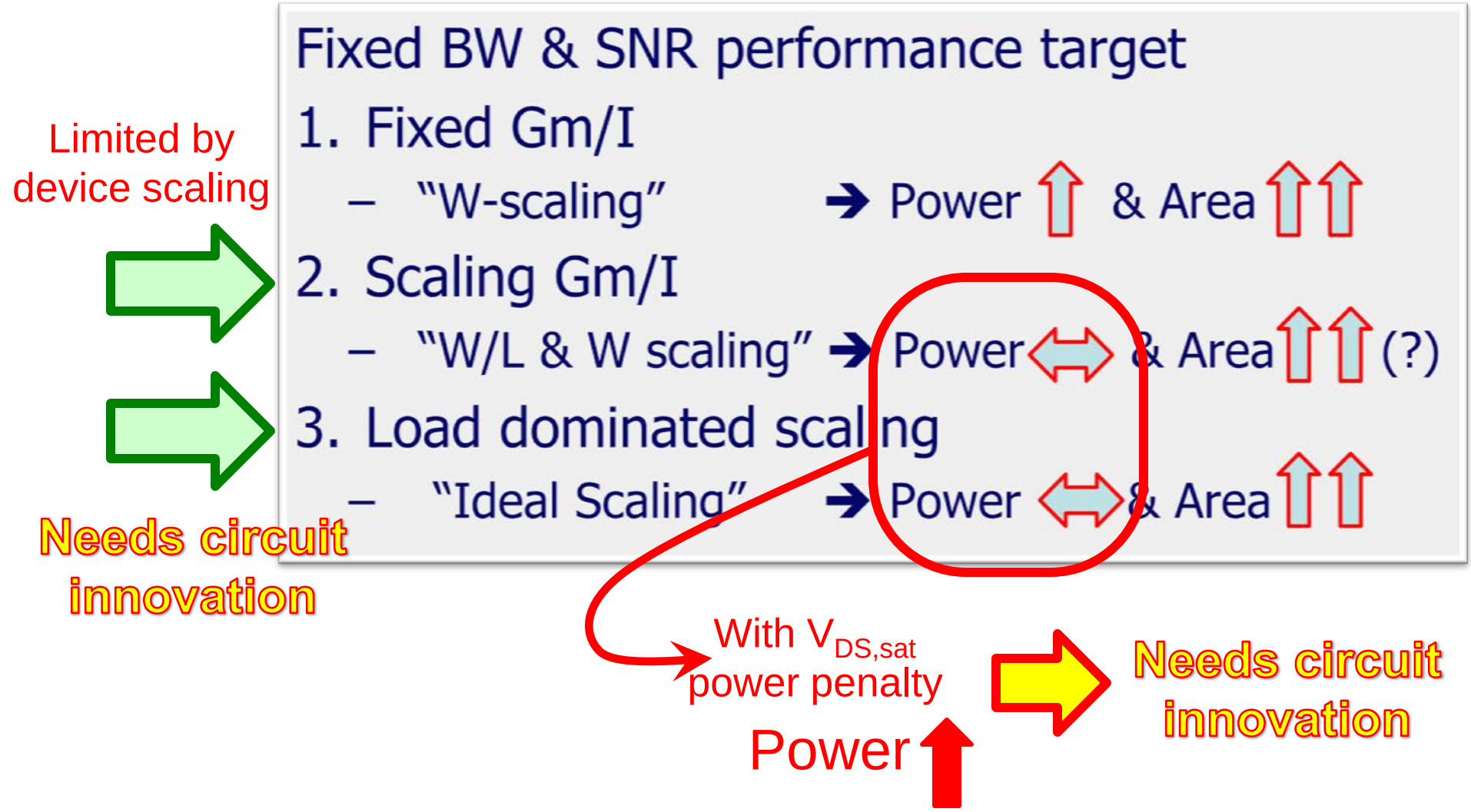
[Kinget ESSCIRC13]

Signal swing REDUCES MORE than proportionally to V_{DD}

$$V_{DD} = 2\sqrt{2}\,V_{RMS} + 2V_{DSsat}$$



Analog V_{DD} Scaling Design Strategies



Scaling the Analog V_{DD}

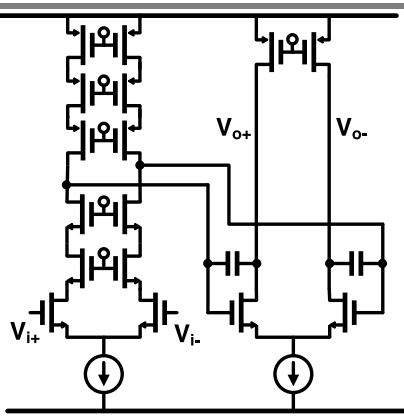
How it can be done

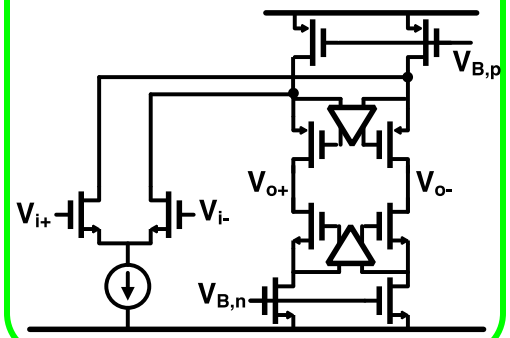
3.3V | 1.8V | 1.0V | 0.5V

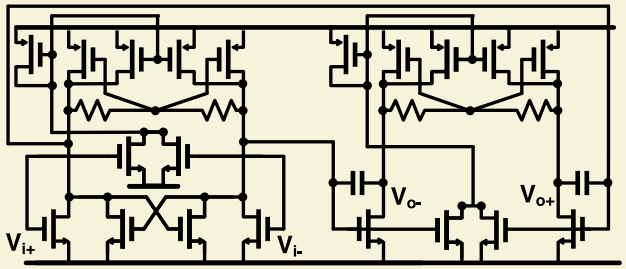
Telescopic Cascode

Folded Cascode
Gain Boosting

Pseudo-Diff. & CMFF
Neg. Resistance
Body Bias



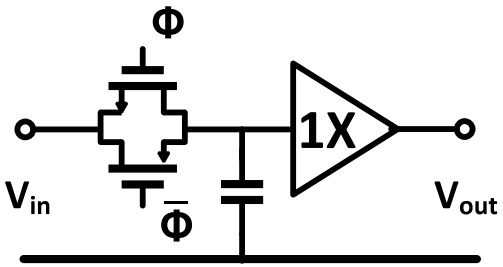


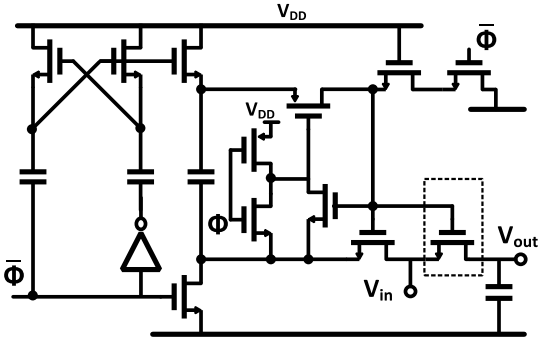


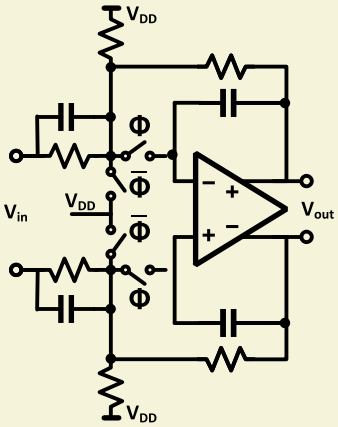
Transmission Gate THA

Bootstrapped THA

Feedback THA
with Level Shift

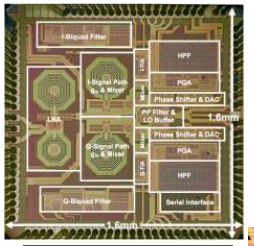




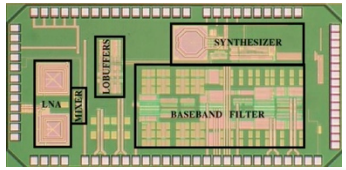


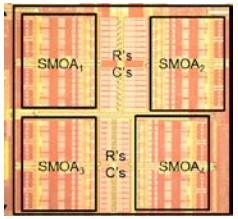
Columbia's 0.5-0.6V Analog & RF Roadmap

Complexity & Performance



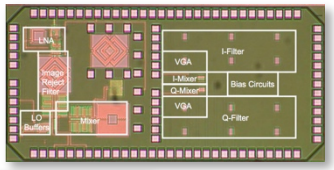
900MHz RCV Cell.



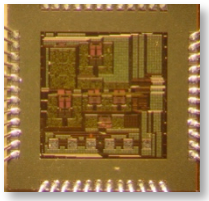


70MHz SMOA LPF

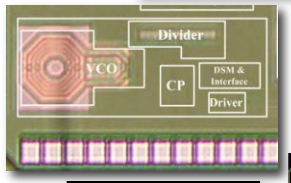
2.4GHz RCV+Synth WPAN



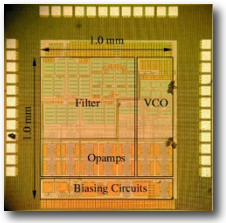
2.4GHz RCV



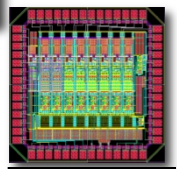
CT 74dB 25kHz ΣΔ A/D



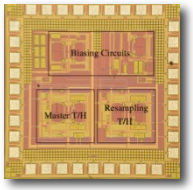
2.4GHz LO Synth.



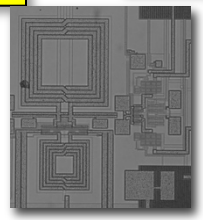
135kHz LPF + Tuning



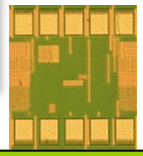
8b 10Ms A/D



10b 1Ms THA



900MHz RF Front-end



0.6V V_{DD} V-Reference

Body- & Gate-input OTAs

65nm
90nm
180nm
250nm

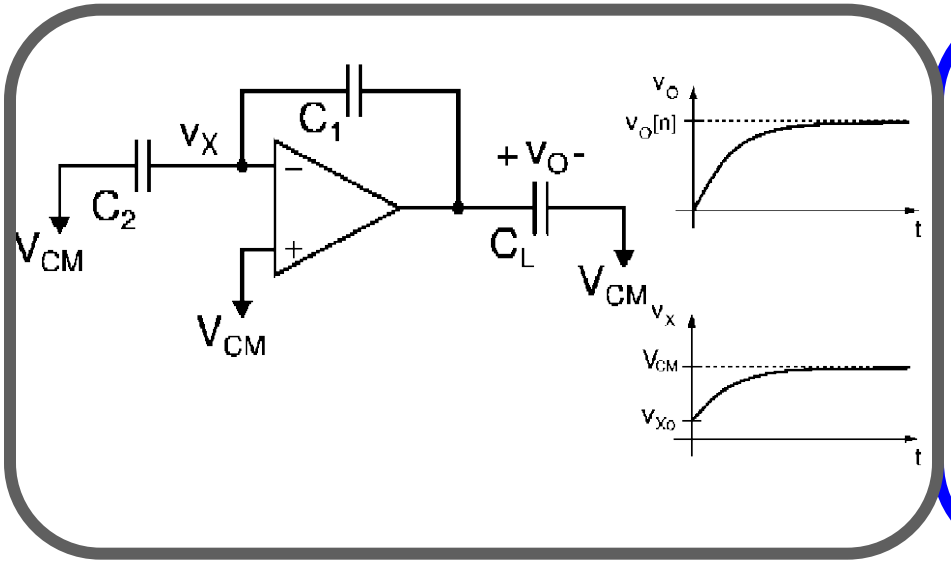
2004 2005 2006 2007 2008 2009 2010 2014

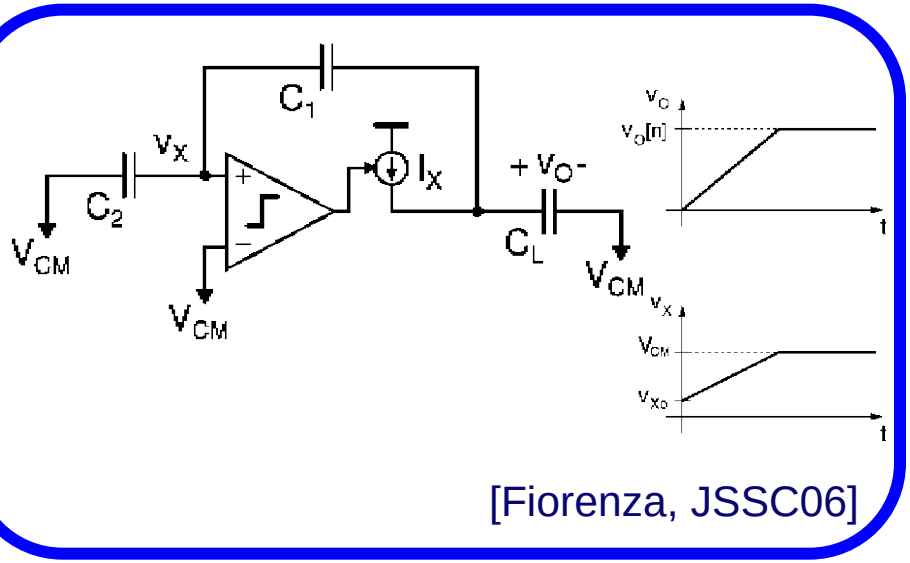
Leveraging Nanoscale CMOS

Different Architectures for Analog

Zero-Crossing-Based Sampled Circuits

OTA Based Circuits | Comparator Based Circuits

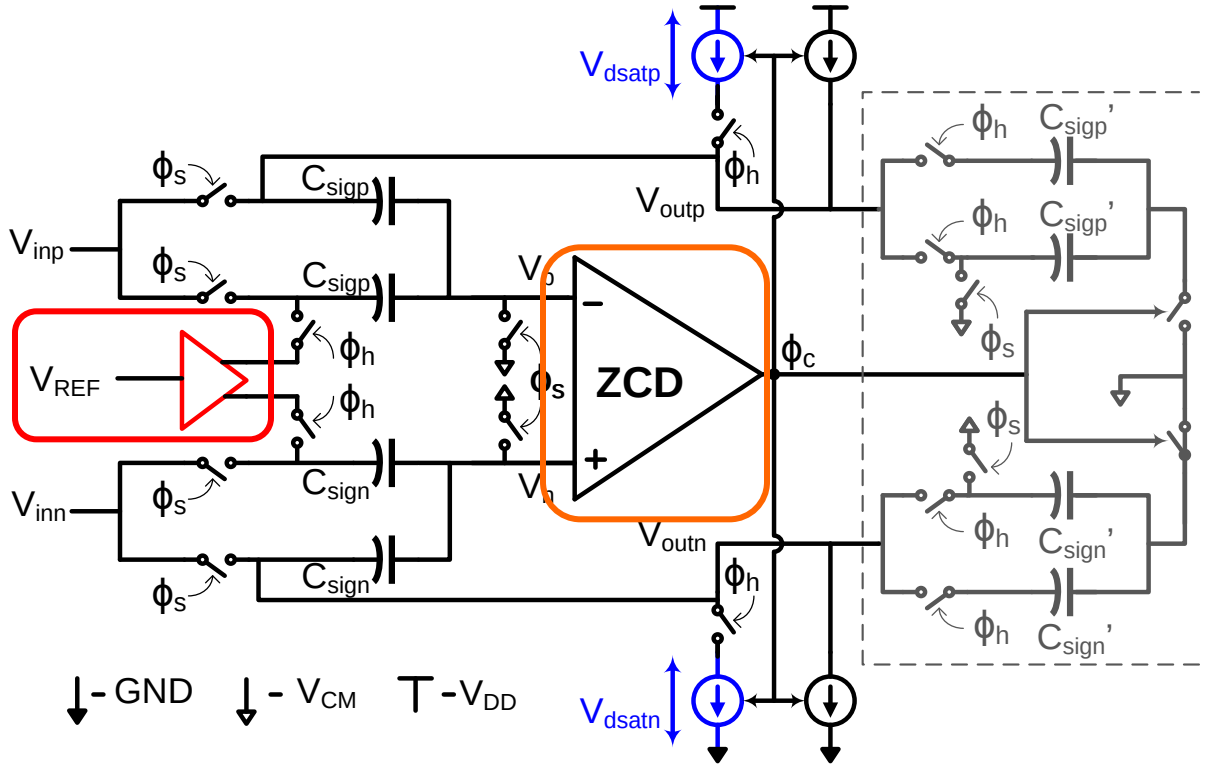




[Fiorenza, JSSC06]

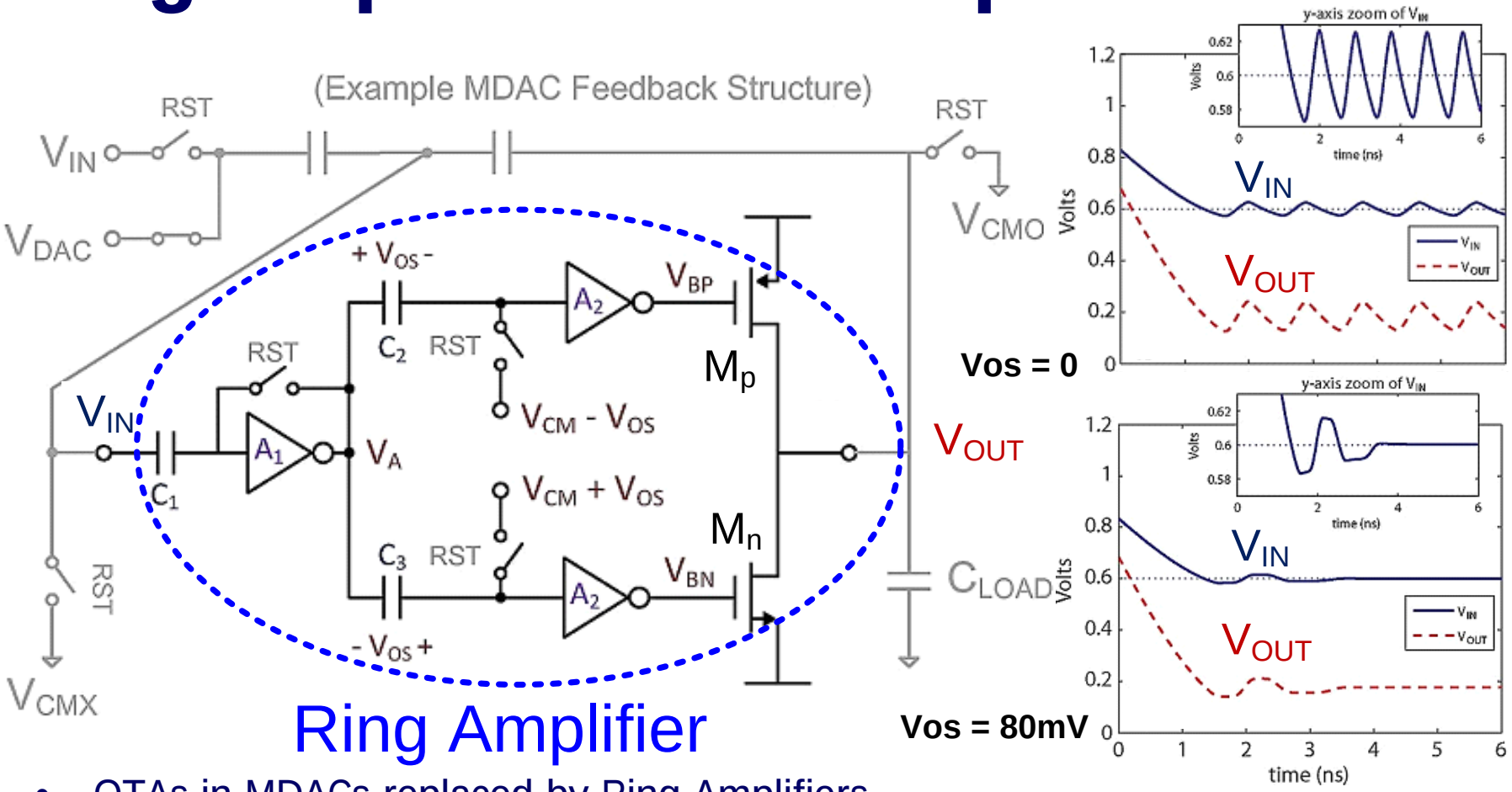
- High gain OTA replaced by zero-crossing-detecting CT comparator + current sources
- 'Linear' exp. settling replaced by slew-based charging
- Closed loop stability constraints issues avoided

ZCB Circuits: In Detail



- MDAC linearity determined by linearity of **output current sources**
  - Voltage headroom: limited voltage swing
- MDAC noise performance determined by **ZCD noise-performance**
  - Conventional analog noise-scaling
- **Reference buffer design** is more complicated than OTA-based MDACs
- Accurate settling requires overshoot cancellation

Ring Amplifiers for Sampled Circuits

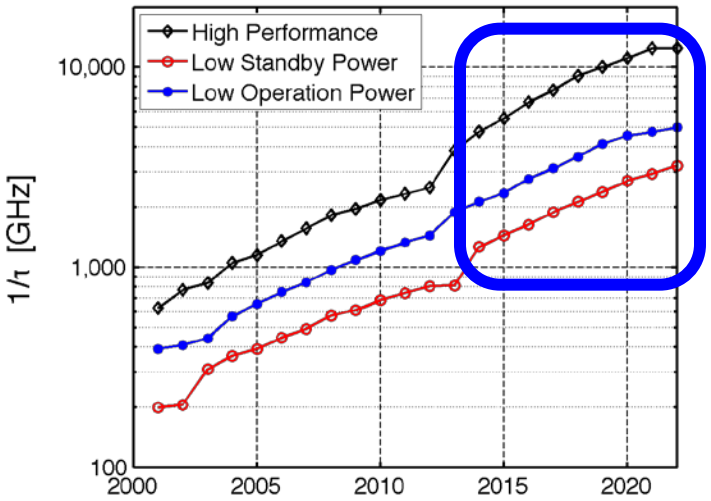


- OTAs in MDACs replaced by Ring Amplifiers
  - Ring Oscillators with embedded offset
- Potential low-voltage operation
  - M_p and M_n operate as switched current sources
  - Slew rate need not be constant (no headroom required)

[Hershberg, JSSC12]

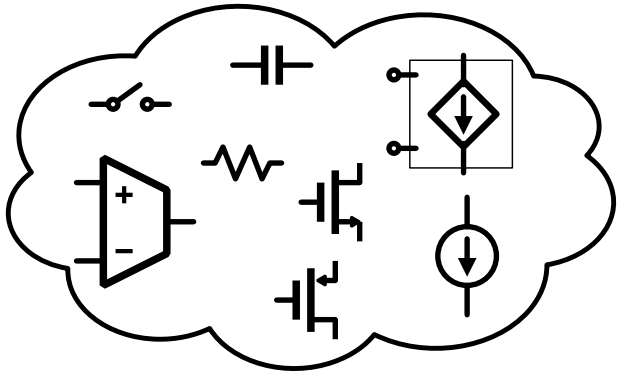
Leveraging Nanoscale CMOS

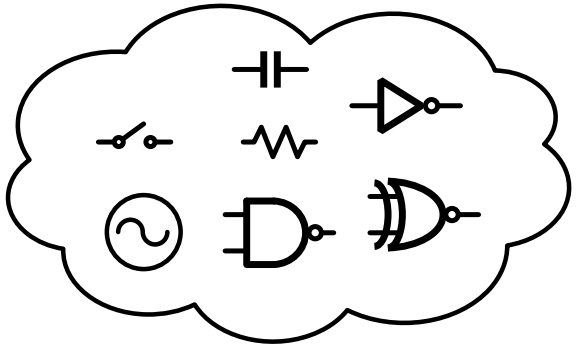
Different Approaches to Analog Signal Representation



Exploiting Device Speed

Circuit Primitives





Signal Representation

Voltage and Current

Delay or Phase

Topologies

OTA & Feedback

Telescopic Cascode

Folded Cascode
Gain Boosting

Pseudo-Diff. & CMFF
Neg. Resistance
Body Bias

Switched Mode
OpAmps

Non-OTA & Feedback

Comparator
Based Circuits

Ring Amplifiers

VCO Based Circuits

Non-OTA &
No Feedback

VCO Based Circuits

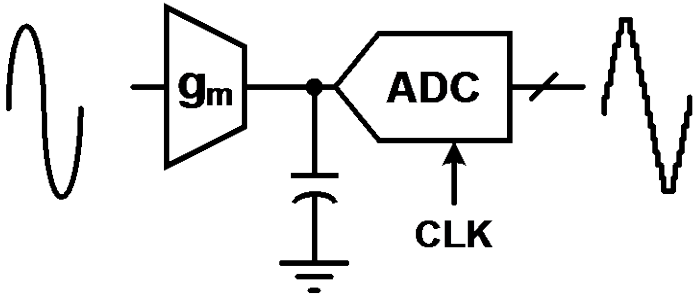
[Kinget13]

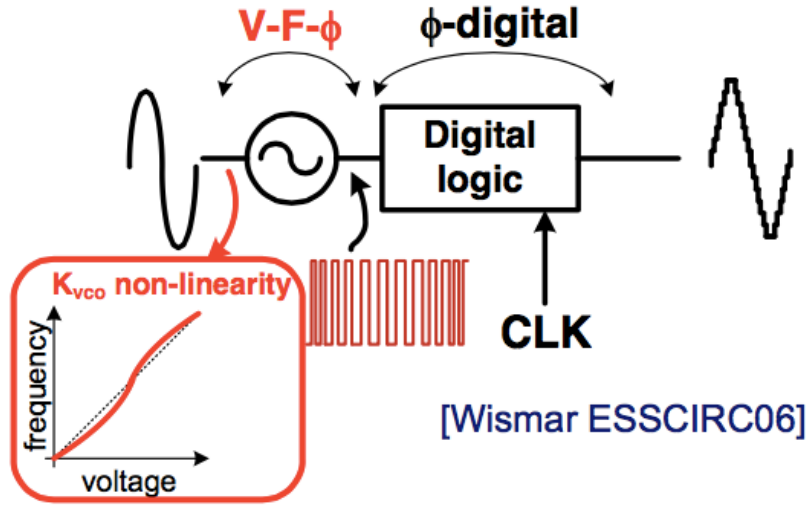
V & I → Delay or Phase

	V / I	Delay (or Phase)
Signal Swing	V_{SS}+x → V_{DD}-x	T_{min} → T_{max}
Noise	1/f & Thermal	Jitter & Phase noise
Distortion	Active V→I is non-linear but feedback with *linear passives* helps	V→T & T→V non linear !?
Integration	Active RC, G_m-C	VCO or CCO (V→Φ or I→Φ)
Amplification	Intrinsic gain, cascode, multi-stage	??
Analog SHA	store Q on C	Recirculating DLL

VCO-Based Quantizers

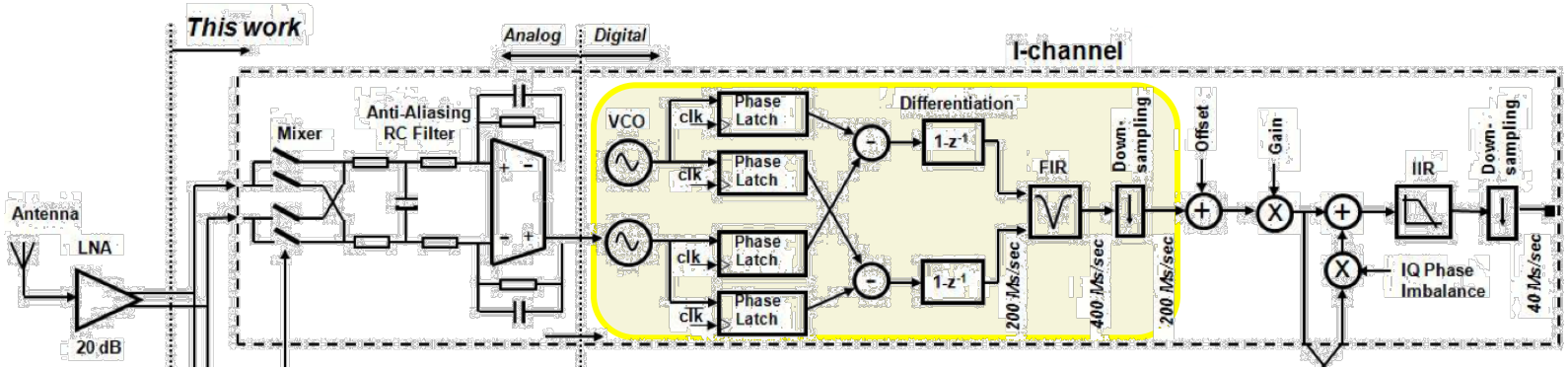
V or I based Quantizer | VCO Based Quantizer





[Wismar ESSCIRC06]

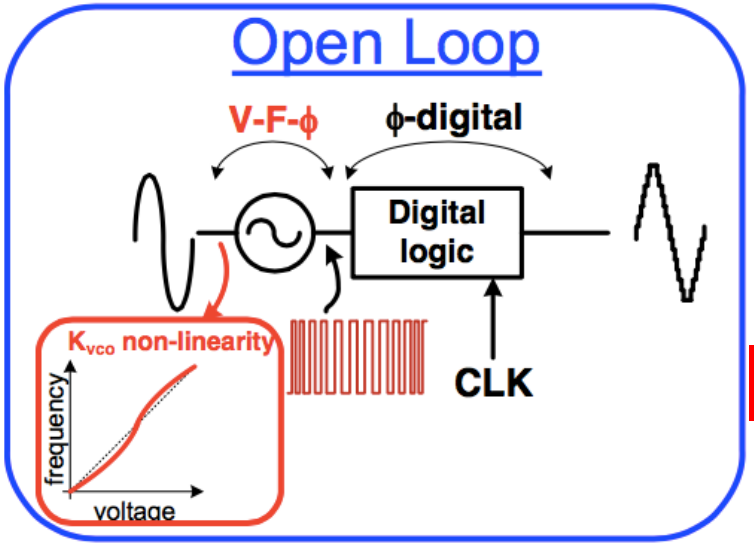
- Diff. Open Loop Example

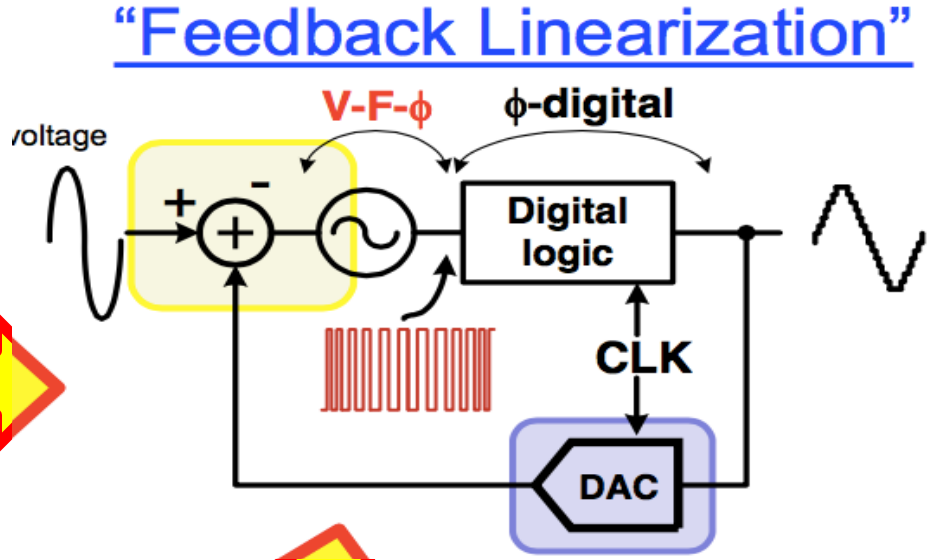


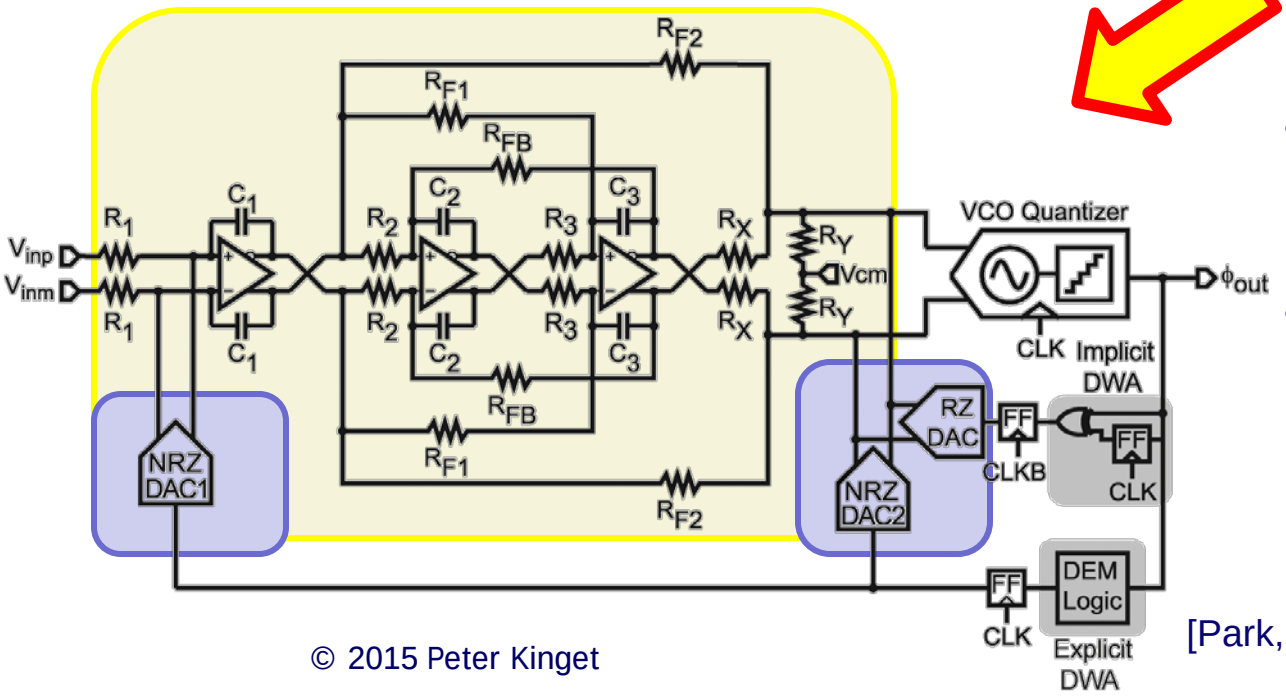
[Op 't Eynde, ISSCC10]

- Still requires analog AAF

VCO-Based Quantizers







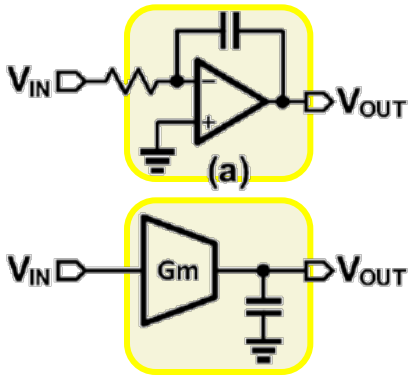
- Quantizer exploits phase domain processing
- Linearization still relies on OTA-RC based voltage/current domain circuits

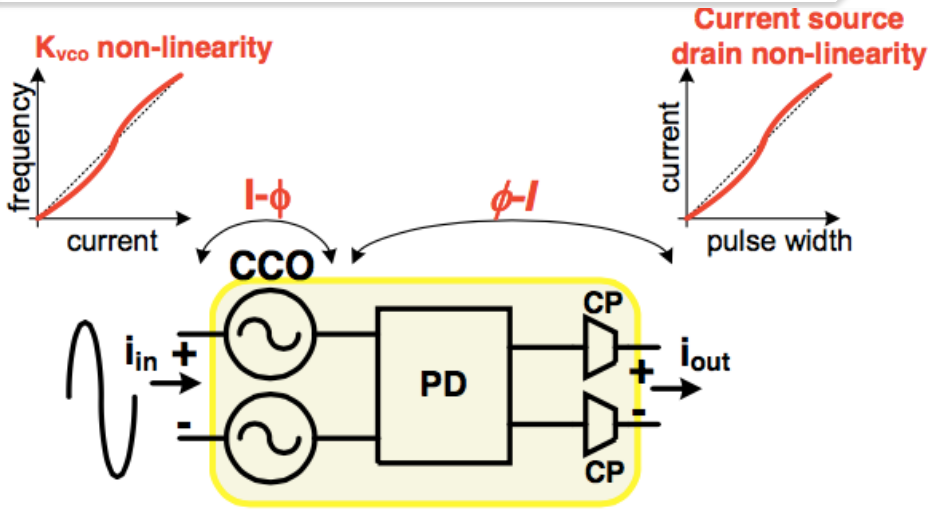
[Park, ISSCC09]

VCO-Based CT Filters

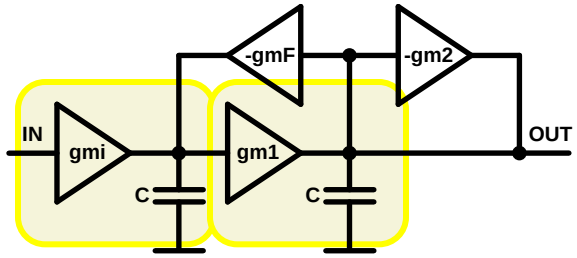
Active RC or Gm-C Integrator

VCO Based Integrator

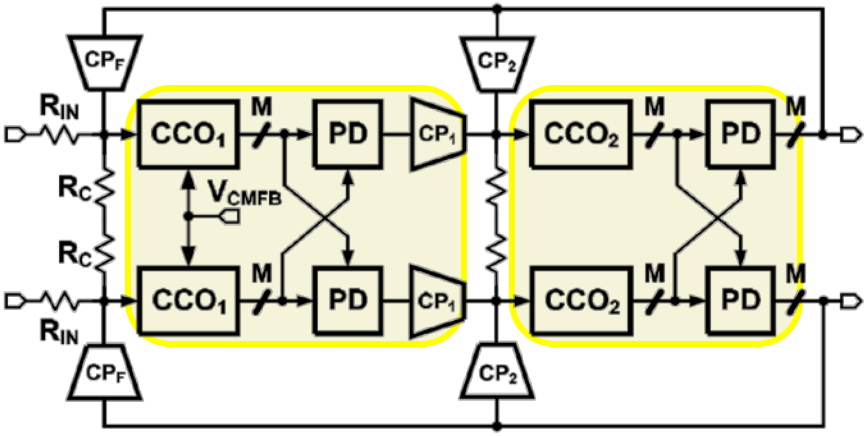




- Biquad Gm-C Filter



'Perfect' integration, but o/p swing limited by CS



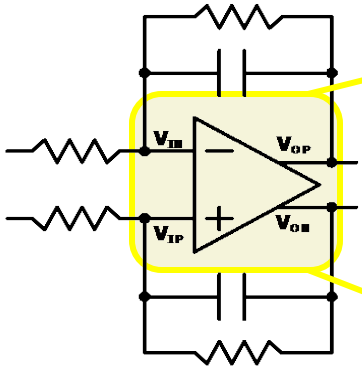
0.55V

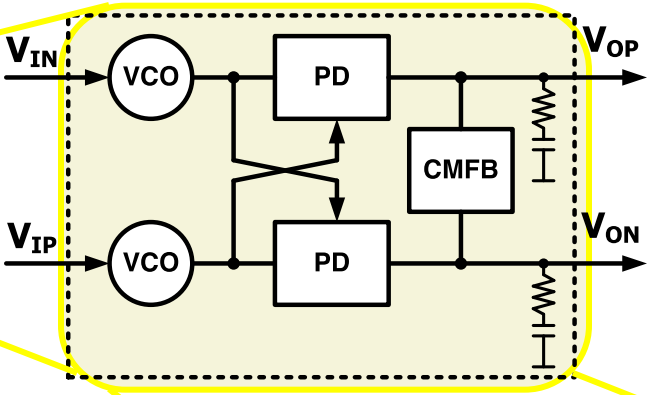
[Drost, ISSCC12]

VCO-Based OTA & Filter

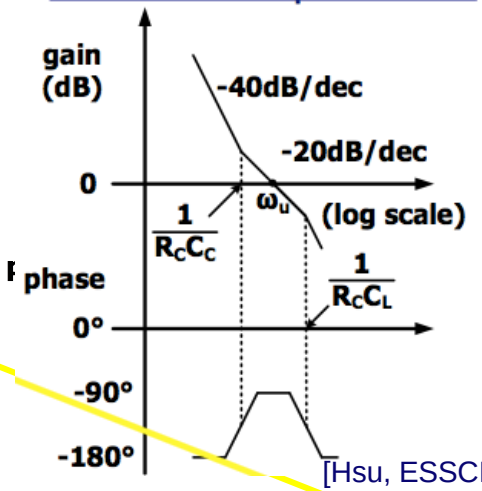
Active RC Integrator with OTA

VCO Based OTA with zero for freq. compensation



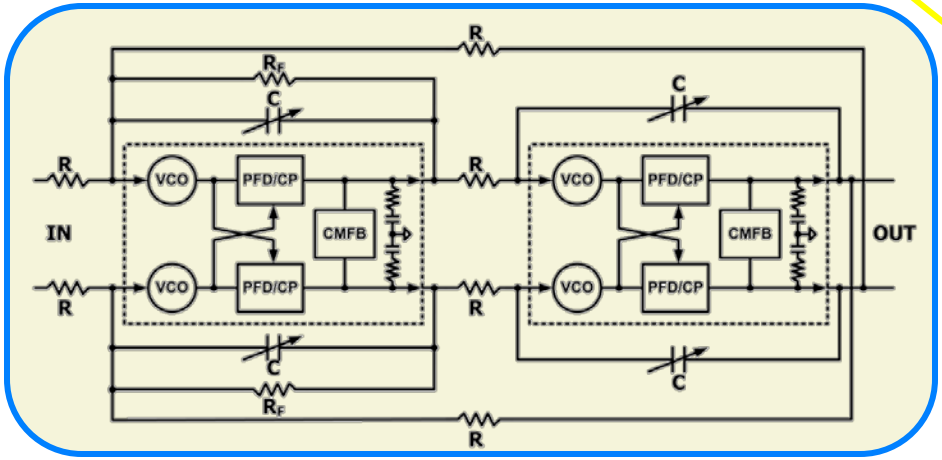


Zero for compensation

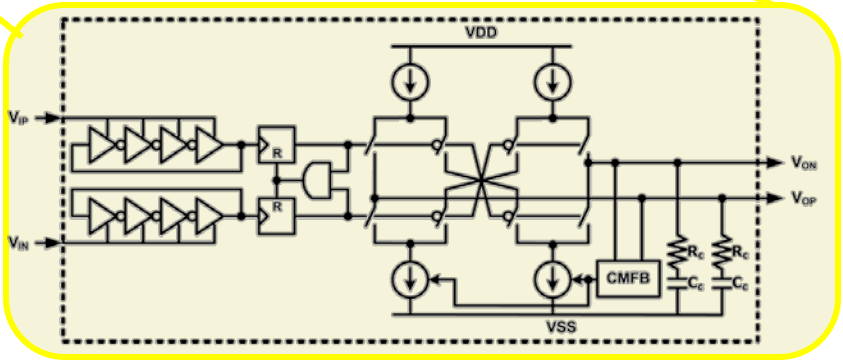


[Hsu, ESSCIRC14]

Complete Active Filter



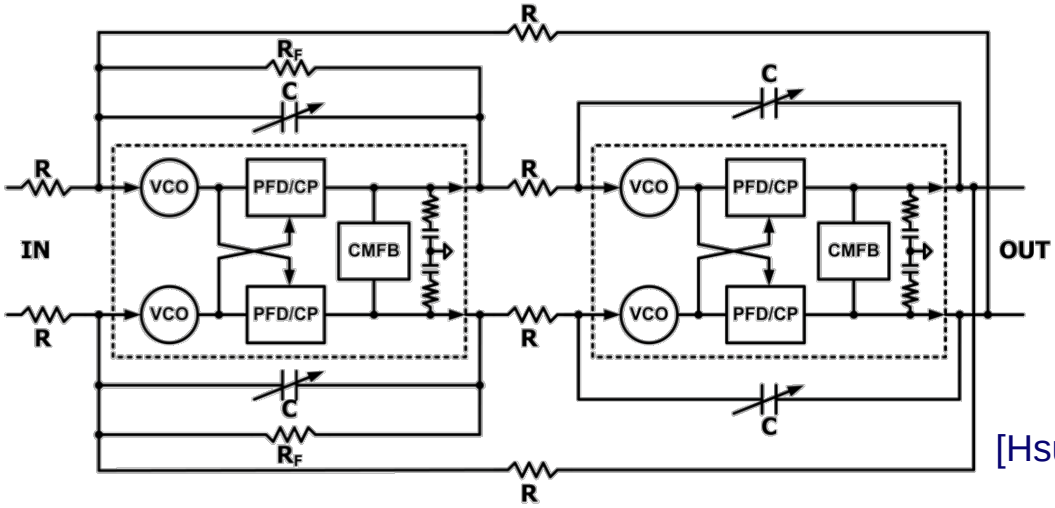
VCO Based OTA



- Very high DC gain

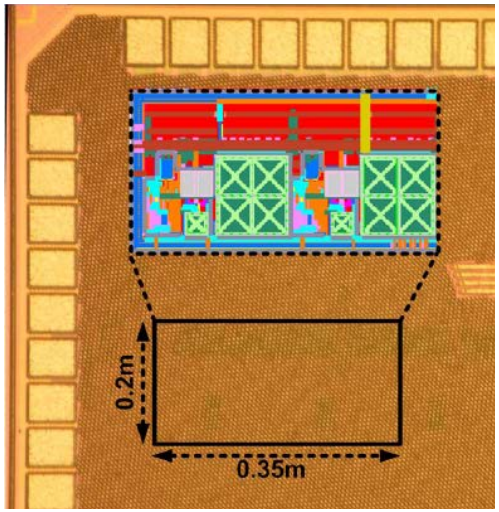
VCO-Based OTA & Filter

A 40MHz 4th-order Active-UGB-RC Filter

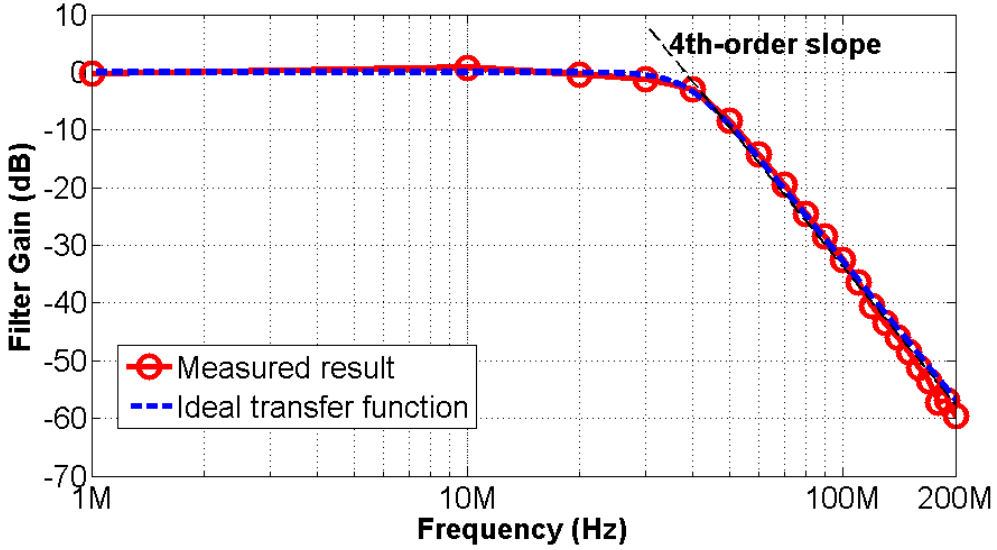


[Hsu ESSCIRC14]

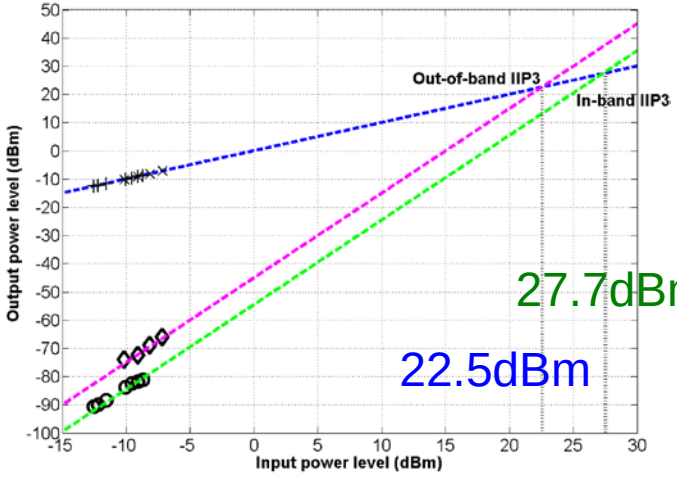
1.2V
7.8mW
0.07mm^2



55nm CMOS



In-Band & OOB IIP3

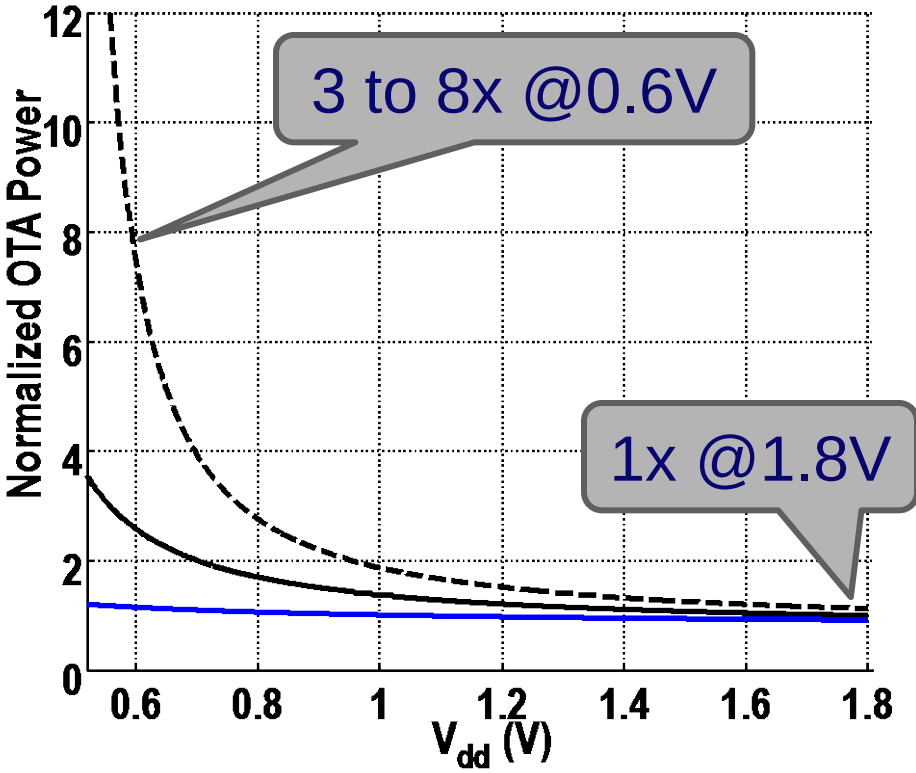


27.7dBm

22.5dBm

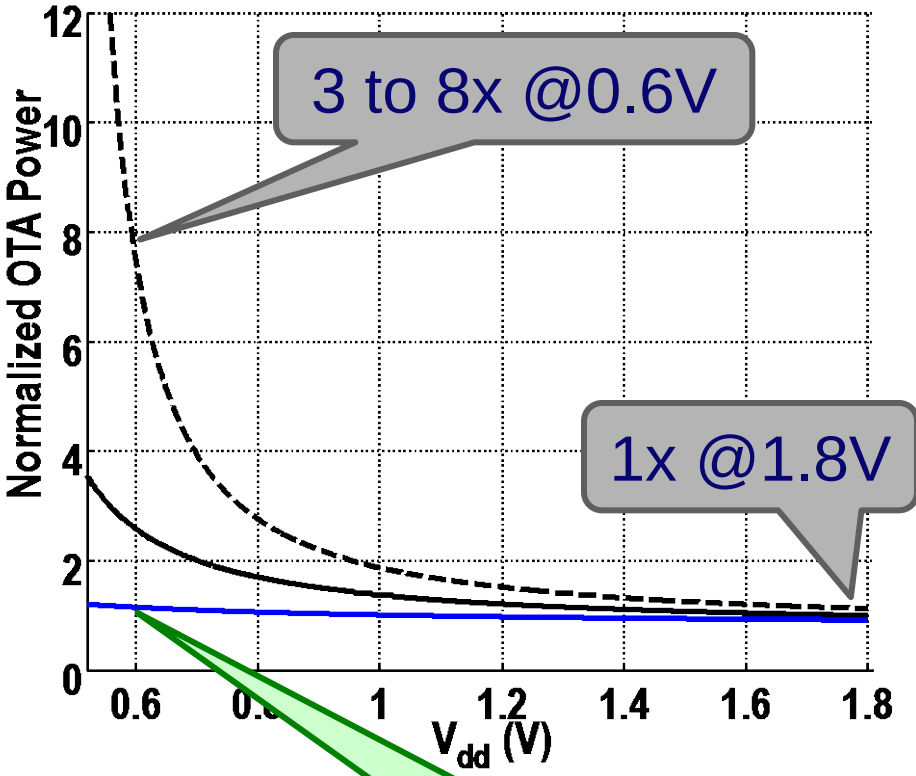
Switched Mode OpAmps

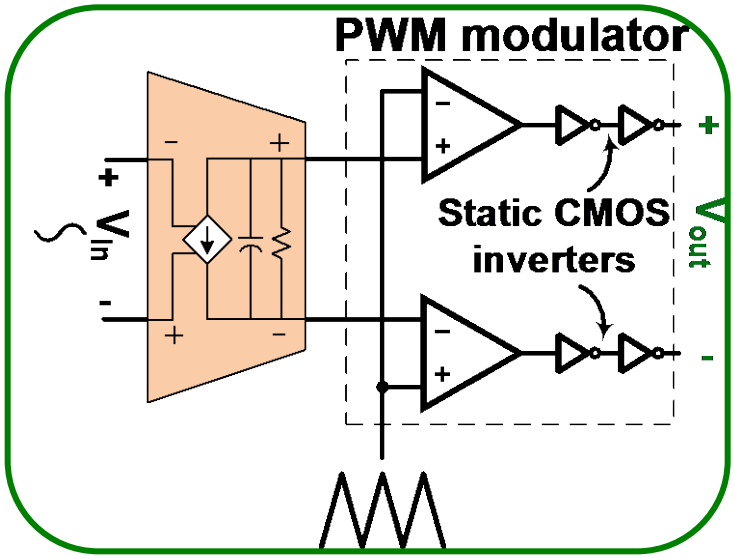
- 'Standard' analog V_{DD} scaling
  - Strong $V_{DS,sat}$ penalty for V_{DD} << 1V
  - Small o/p swing
    ➔ more power in *noise-limited* first stage
  - High o/p stage efficiency is also difficult

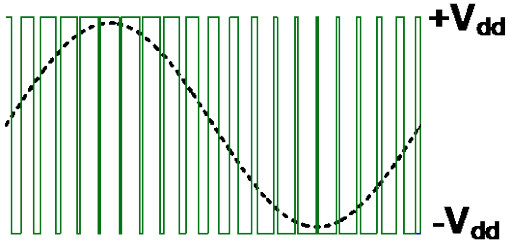


Switched Mode OpAmps

- 'Standard' analog V_{DD} scaling
  - Strong $V_{DS,sat}$ penalty for V_{DD} << 1V
  - Small o/p swing
    ➔ more power in *noise-limited* first stage
  - High o/p stage efficiency is also difficult
- Switched Mode Operational Amplifier
  - Rail-to-rail output swing
  - Low Zout
  - Large BW
  - **Performance gets BETTER with SCALING!!**



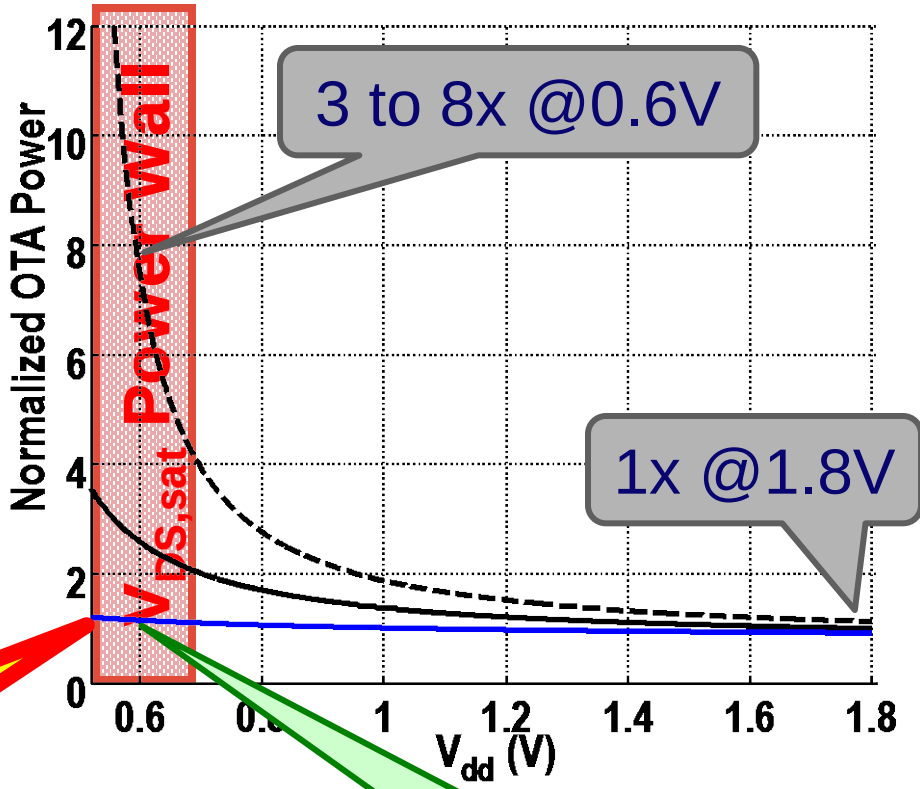


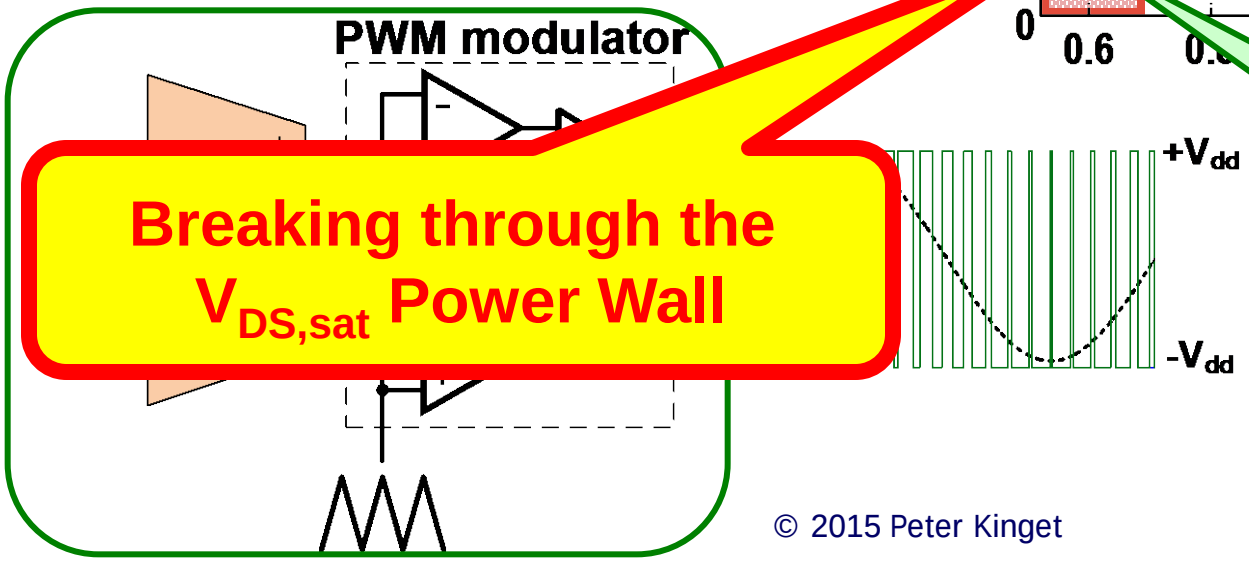


[Vigraham JSSC14]

Switched Mode OpAmps

- 'Standard' analog V_{DD} scaling
  - Strong $V_{DS,sat}$ penalty for V_{DD} << 1V
  - Small o/p swing
    ➔ more power in *noise-limited* first stage
  - High o/p stage efficiency is also difficult
- Switched Mode Operational Amplifier
  - Rail-to-rail output swing
  - Low Zout
  - Large BW
  - **Performance gets BETTER with SCALING!!**

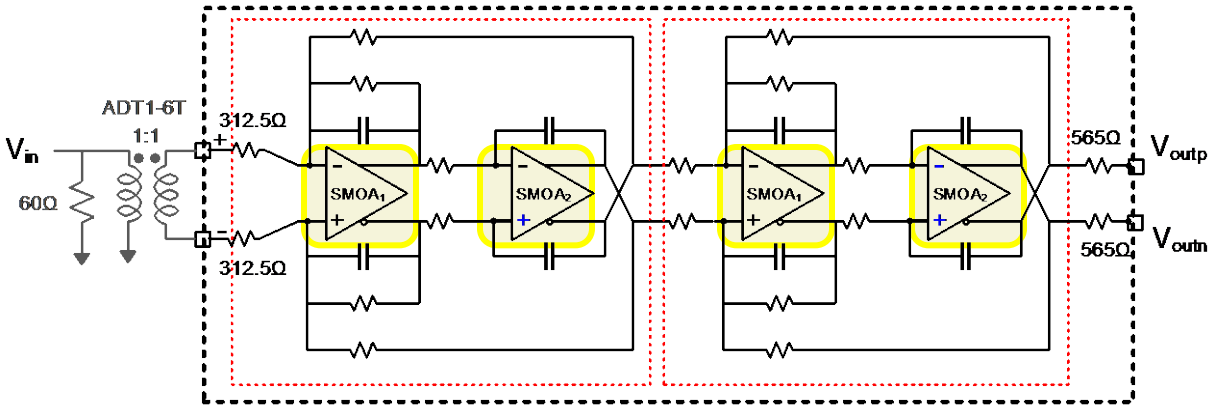


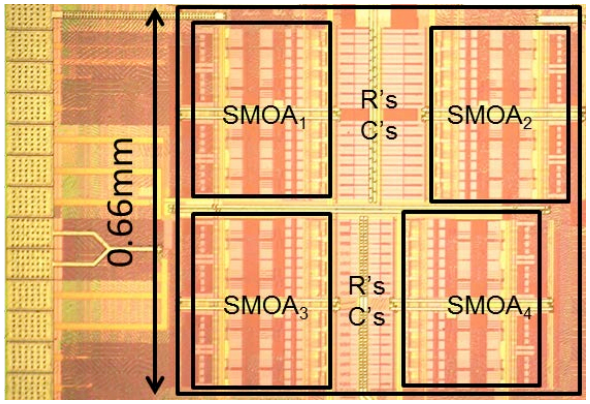


[Vigraham JSSC14]

A 0.6V 70MHz 4th Order CT Butterworth Filter

Active RC Biquads with SMOAs

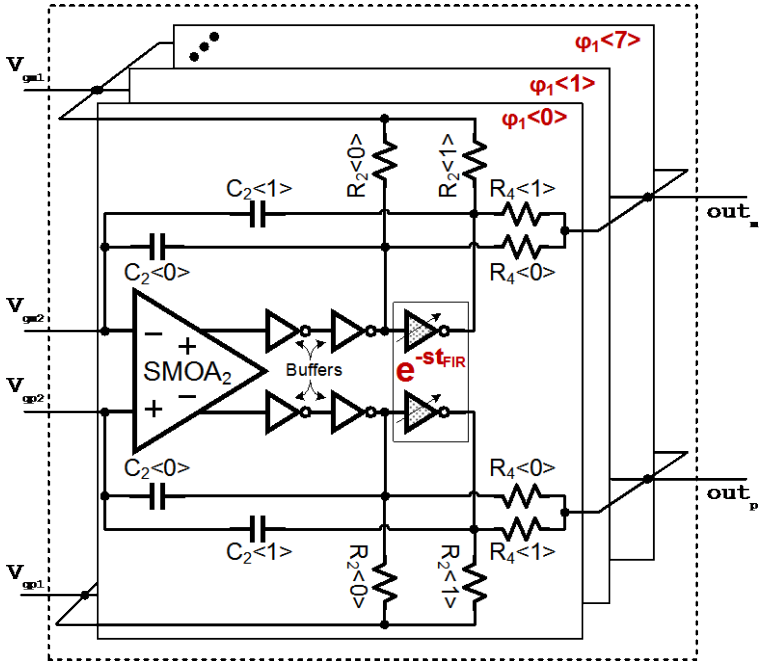




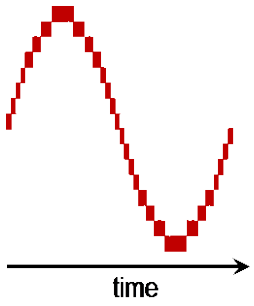
65nm

[Vigraham JSSC14]

Multi-Phase SMOA

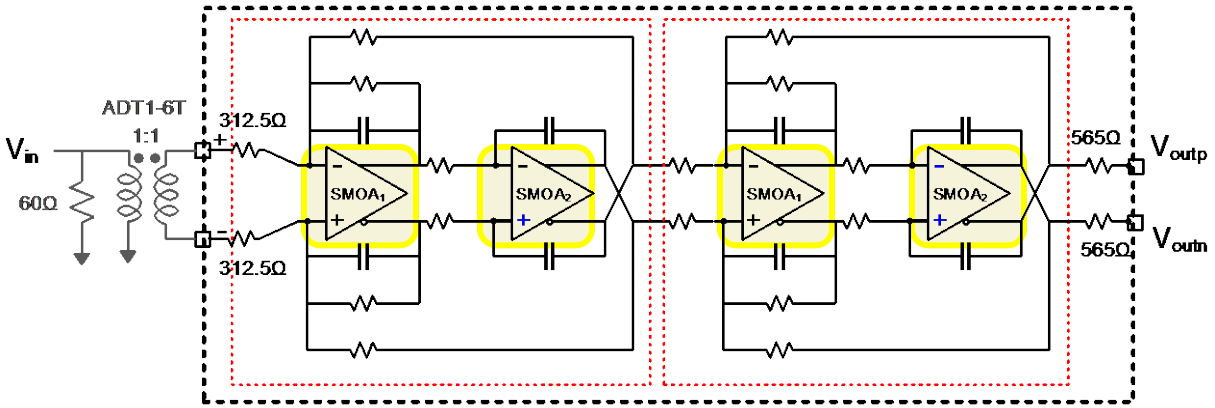


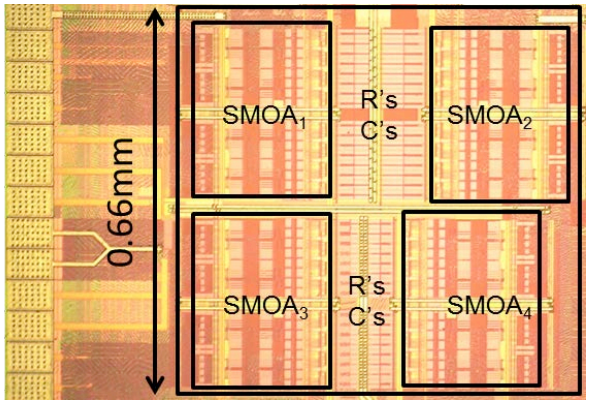
17-level signal



A 0.6V 70MHz 4th Order CT Butterworth Filter

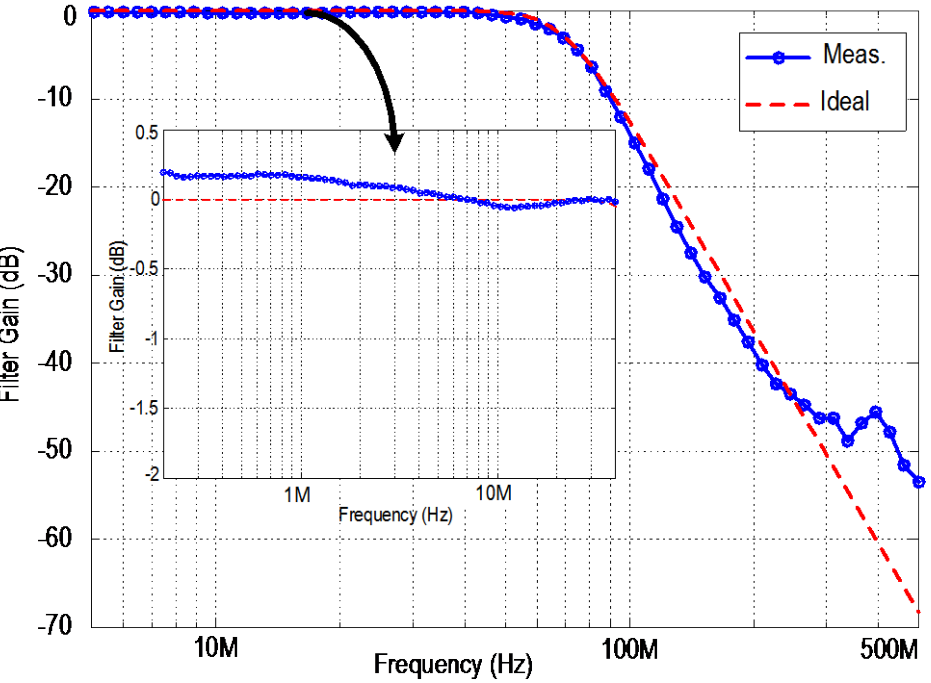
Active RC Biquads with SMOAs

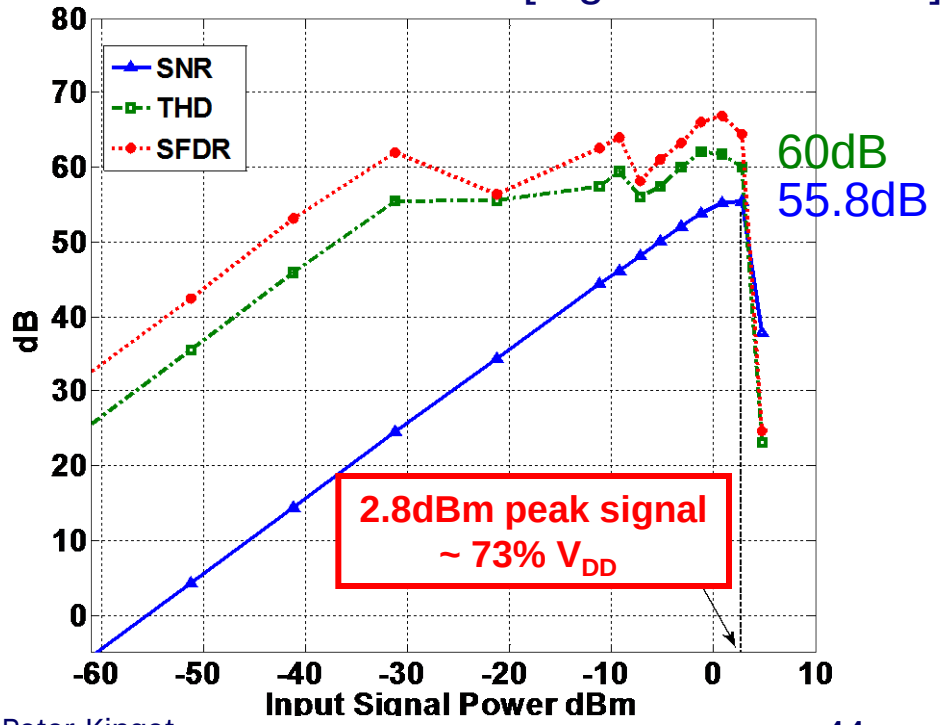




65nm

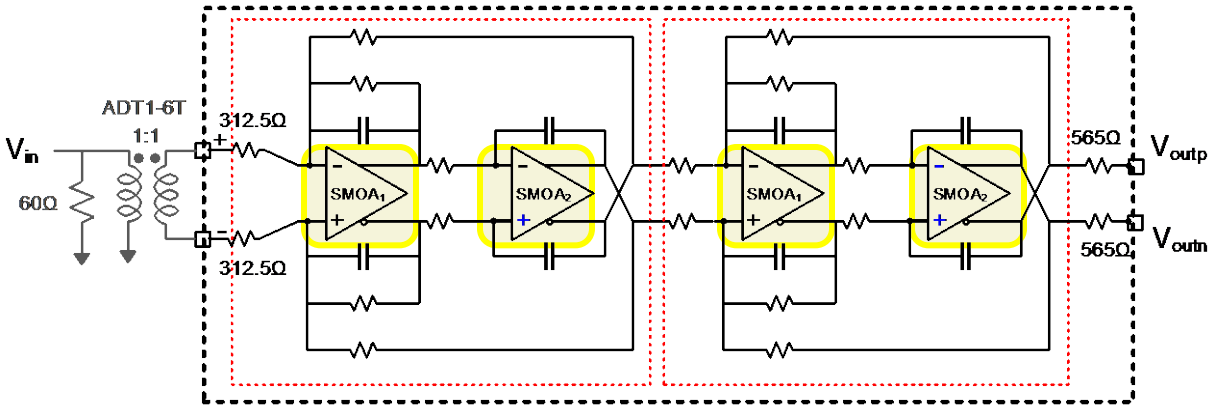
[Vigraham JSSC14]

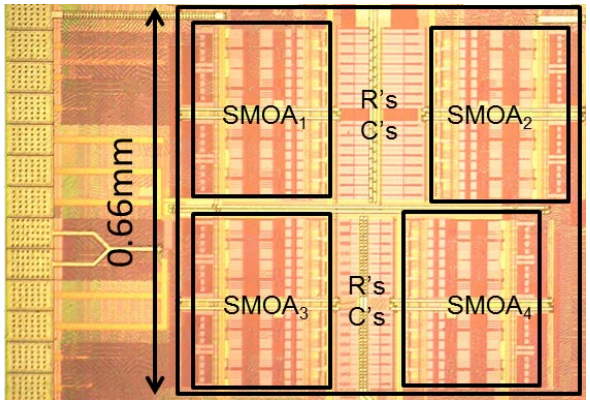




A 0.6V 70MHz 4th Order CT Butterworth Filter

Active RC Biquads with SMOAs

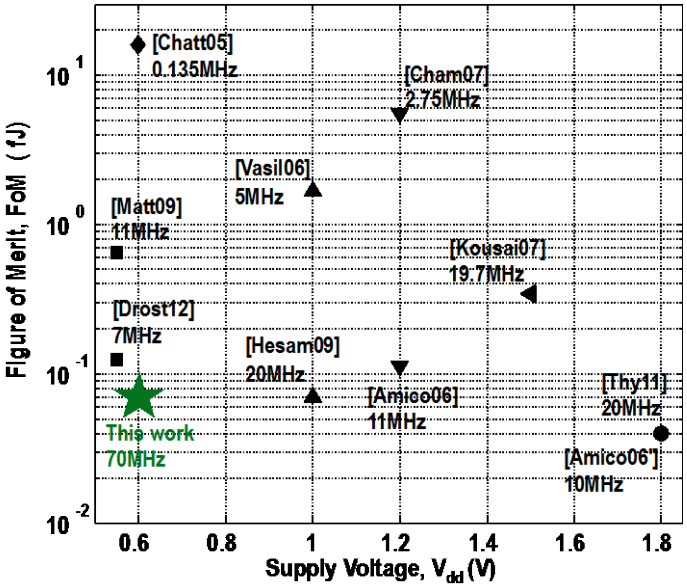




65nm

[Vigraham JSSC14]

Figure of Merit

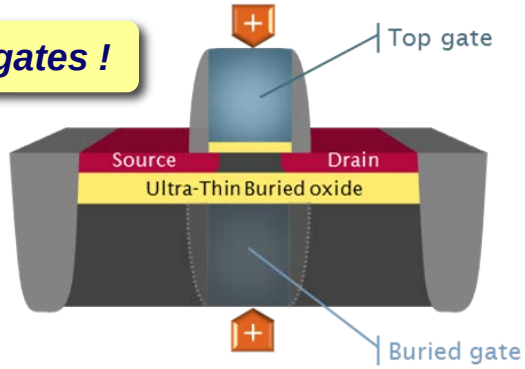


Outlook

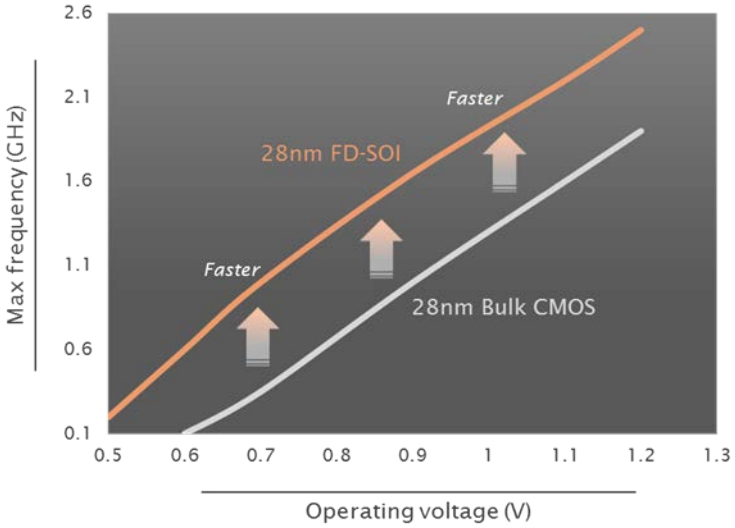
New Devices

28nm FD-SOI CMOS

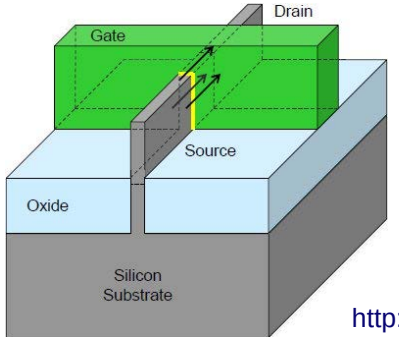
TWO gates !

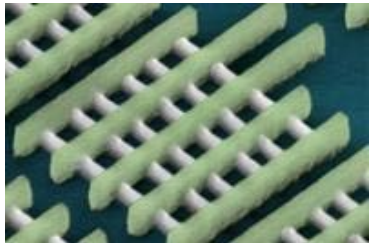


http://www.stericsson.com/technologies/FD-SOI.jsp

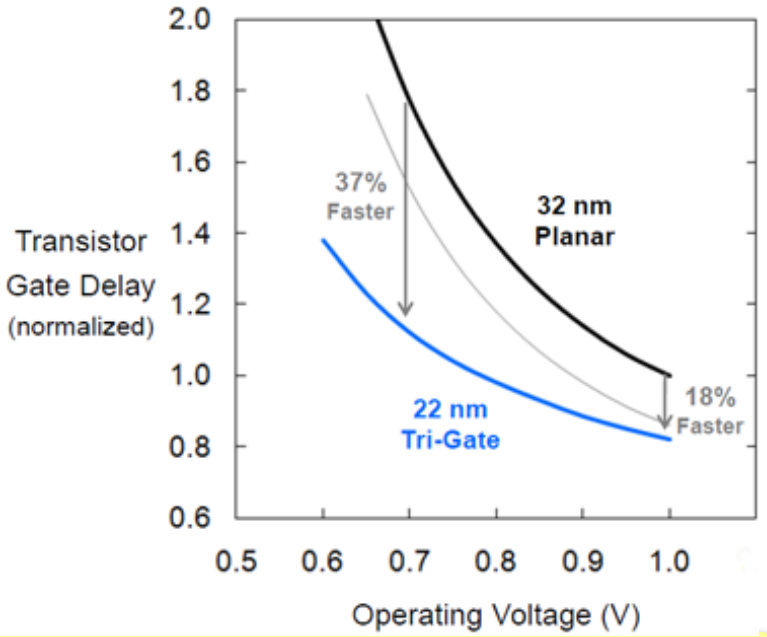


22nm FinFET



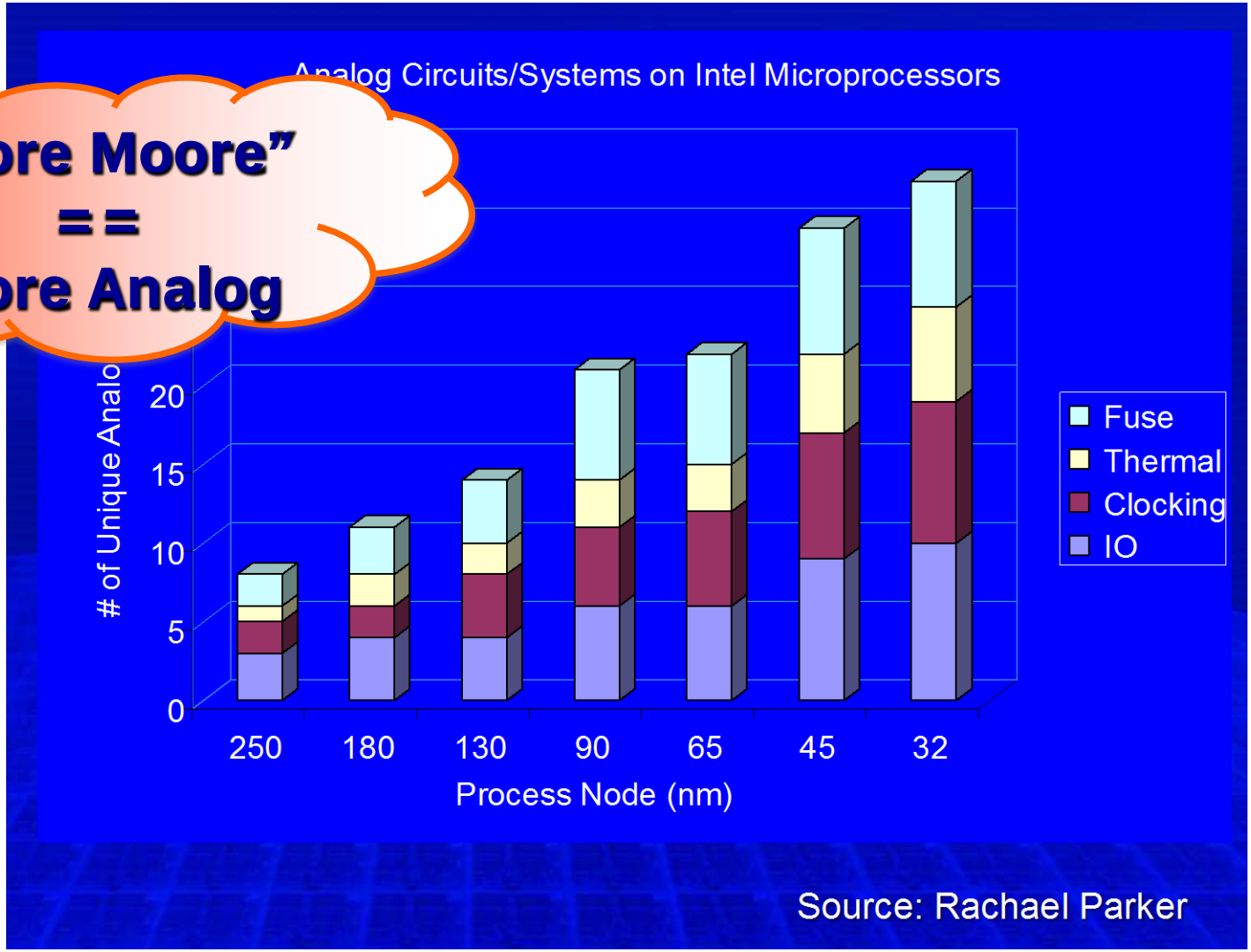


http://www.realworldtech.com/intel-22nm-finfet/



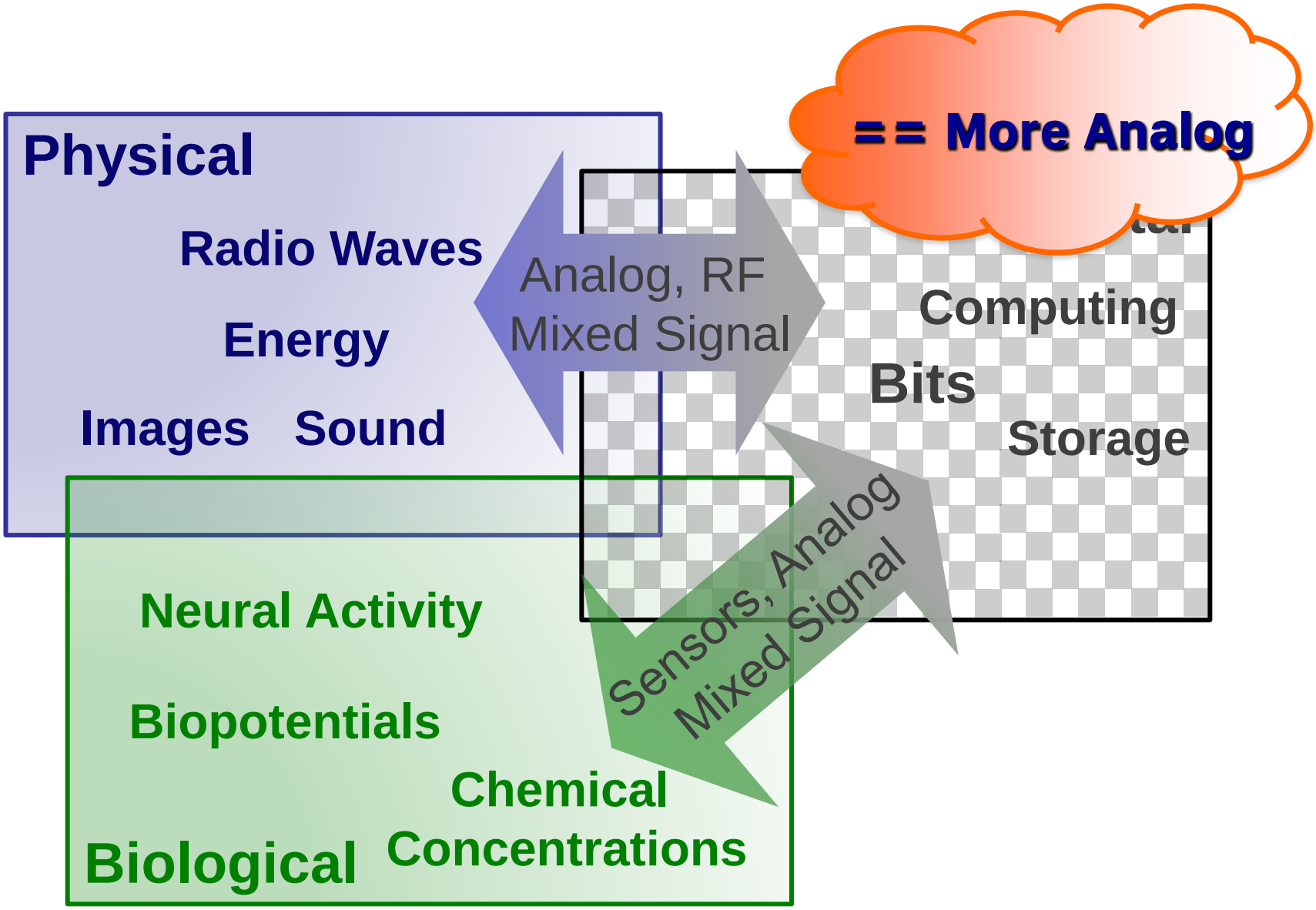
Faster @ lower V_{DD} ➔ lower Power!
Better short channel control ➔ better analog performance?

Analog Circuits in Microprocessors

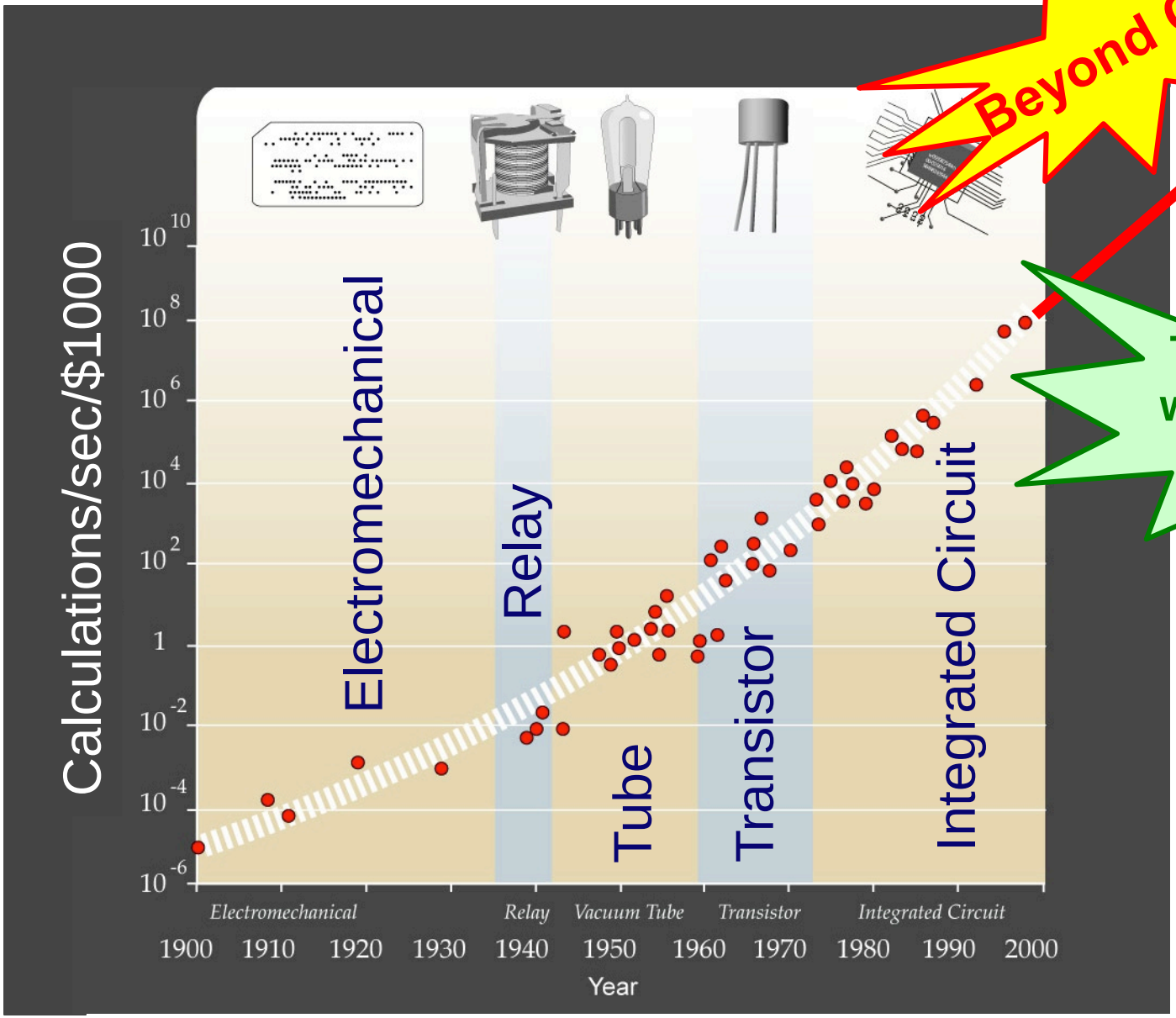


[Greg Taylor, Intel, "Analog/Mixed Signal Design: The Technology Scaling Rate Limiter?"]

“More than Moore”



CMOS: Just a Step ..



Beyond CMOS

The physical world remains ANALOG…

[Wikipedia: Kurzweil's extension of Moore's law]

Scaling Analog Circuits

Exciting Opportunities Ahead

- Device scaling introduces challenges to ‘traditional’ analog design
  - Supply scaling arguably being the most severe challenge, but it can be overcome

- Device scaling offers new opportunities for analog design
  - Novel circuit approaches
  - Different representation for analog information
  - New device architectures hold interesting promises

“Digital scaling” makes analog design actually more interesting & important

Acknowledgments

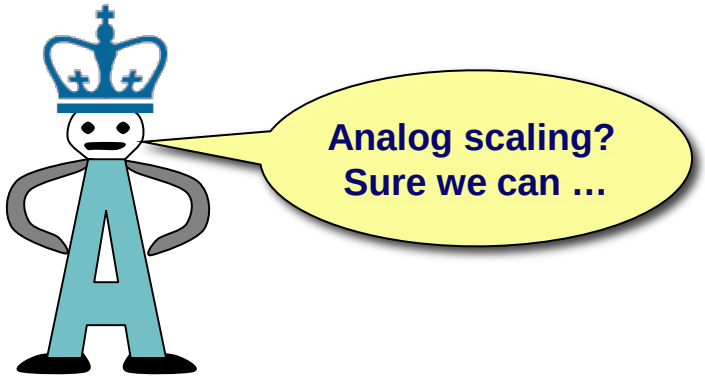
- Collaborators: Y. Tsividis, K.P. Pun (Chinese Univ. Hong Kong), S. Chatterjee (now IIT Delhi), A. Balankutty (now Intel), J. Shen (now ADI), N. Stanic (now SiLabs), S. Yu (now VIA), B. Vigraham (now Maxlinear), J. Kuppambatti (now Seamless Devices), C. Hsu (now ADI).

- Funding Support: Analog Devices, Intel, SRC, Silicon Labs, Texas Instruments, DARPA, National Science Foundation.

- Fabrication Support & Donation: CMP, ST Microelectronics, UMC and VIA Telecom.

- Tools: Integrand Software for EMX software and Berkeley Design Automation (Mentor) for BDAsim

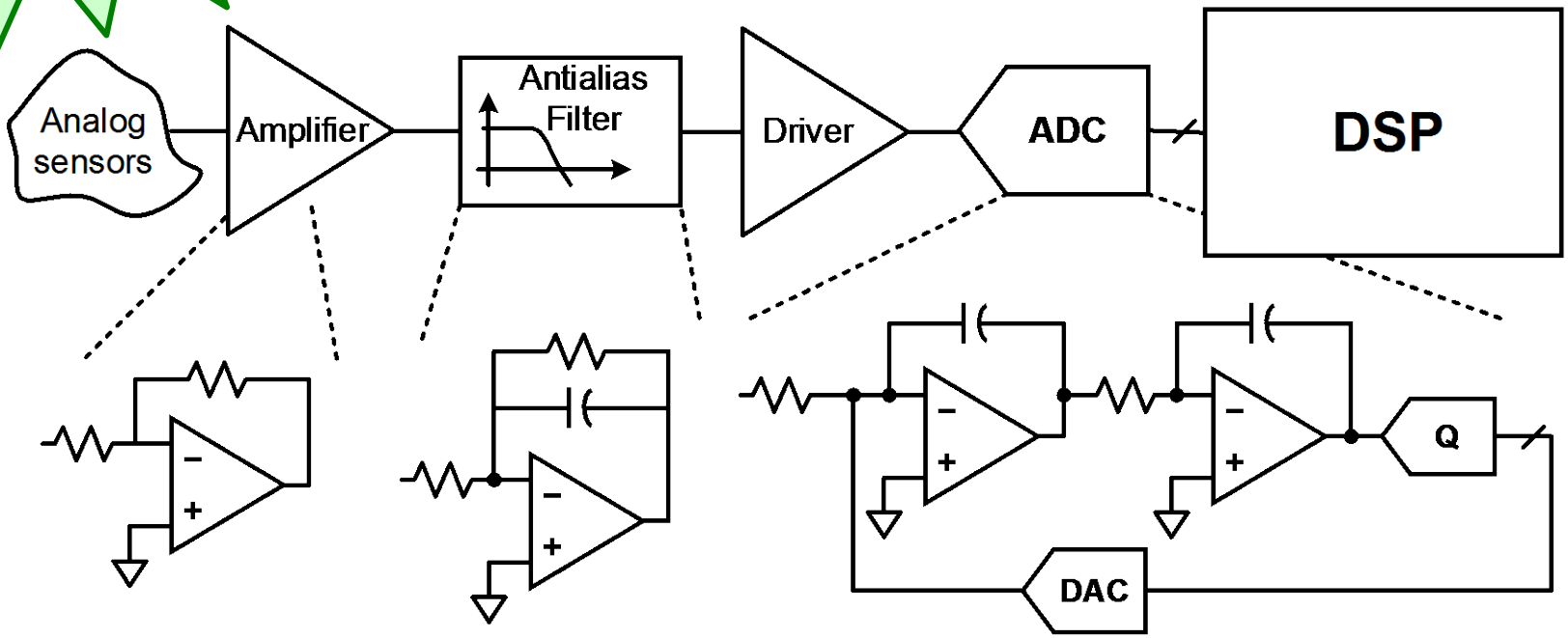
Thank You
for your attention



We Are Stuck With Analog

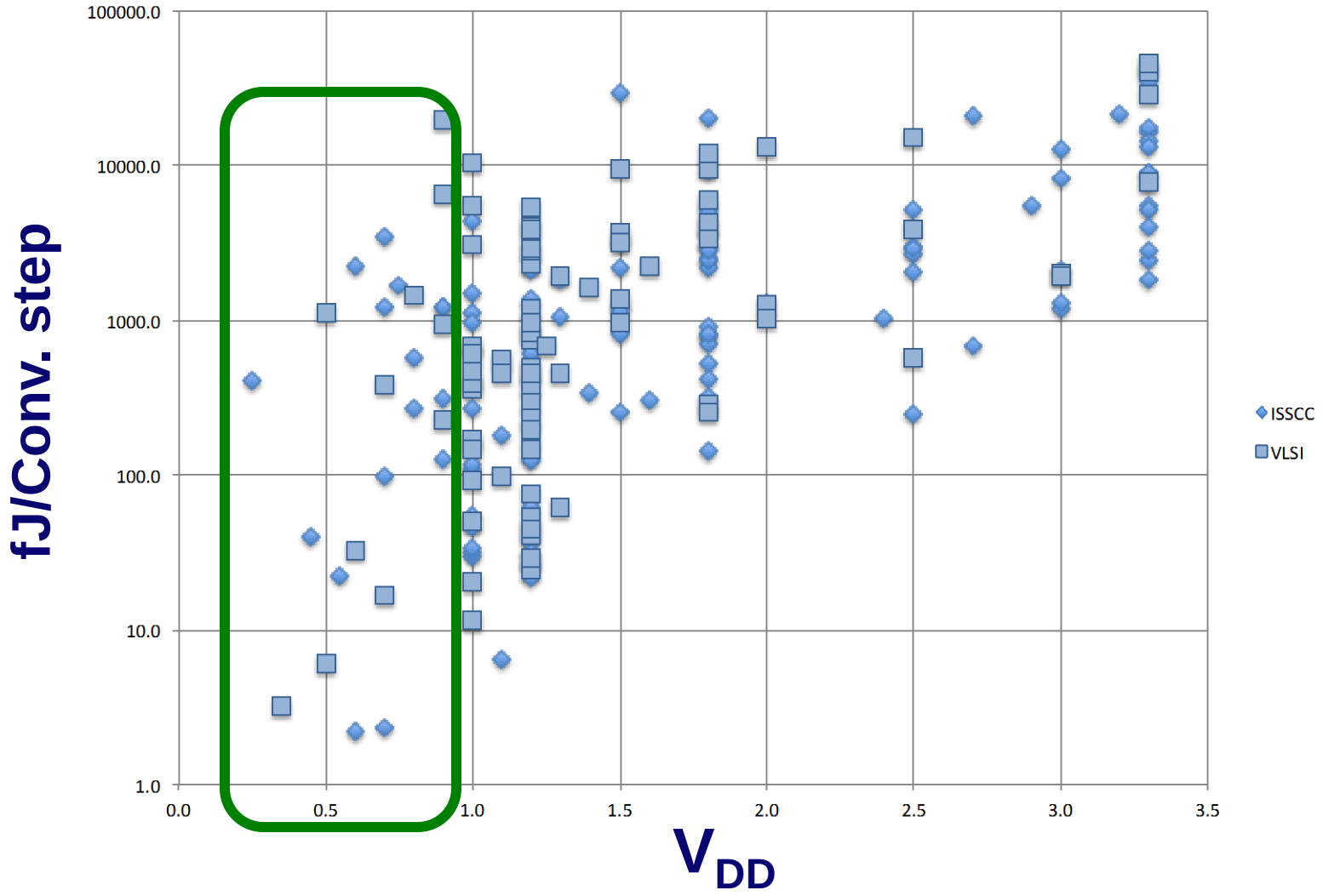
The Physical World is ANALOG…

Physical World to Digital



Also, CLK generation, I/O, RF, D/A, Power Mgmt, …

ADC FOM vs V_{DD}



Data adapted from B. Murmann, "A/D Converter ISSCC Performance Data," 2013