ANALOG DEVICES

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A 110nA Quiescent Current Buck Converter with Zero-power Supply Monitor and Near-constant Output Ripple

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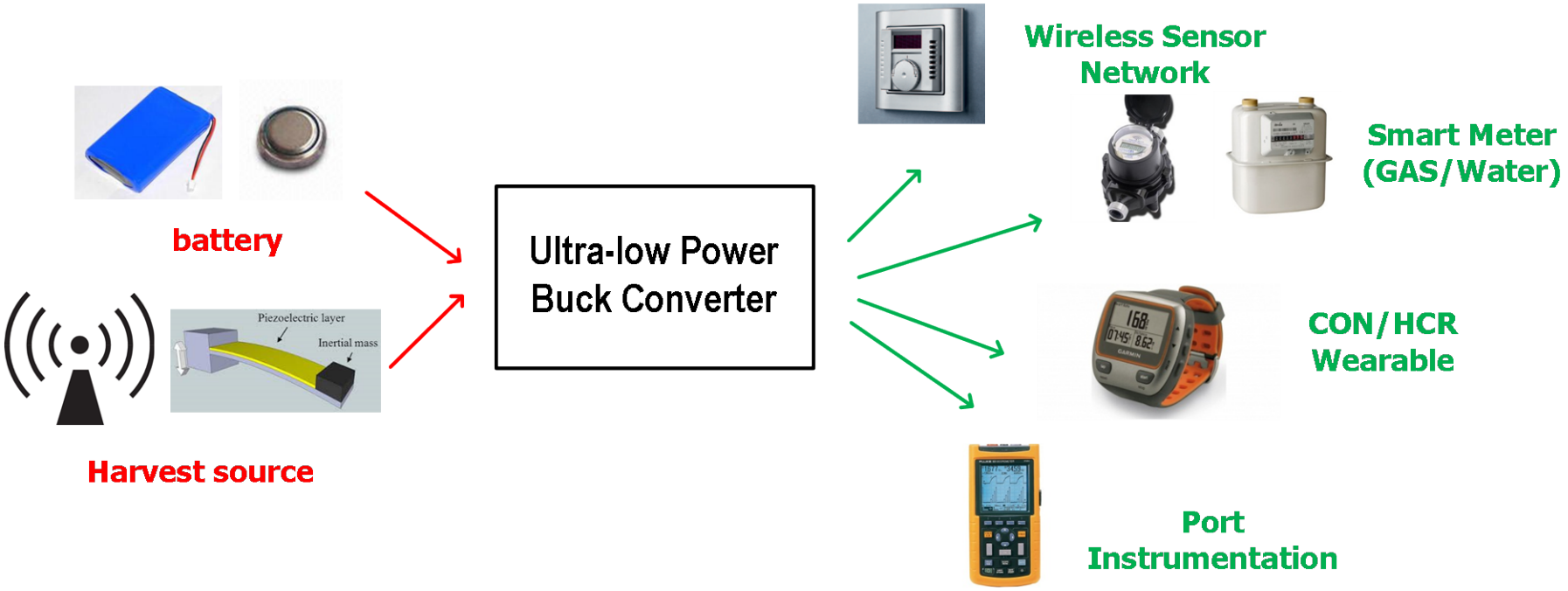
- Analog Devices
- Shanghai, China

Outline

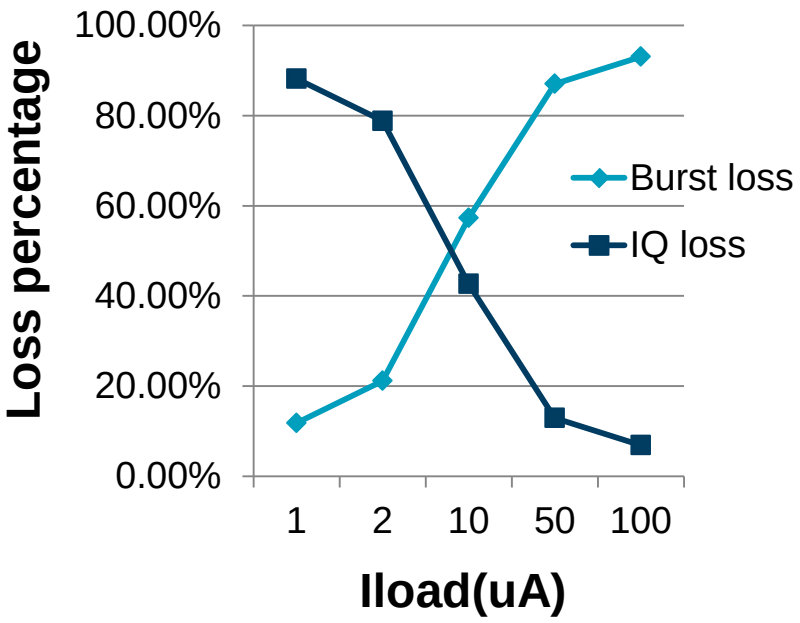
- Motivation & previous research
- System structure
- Ultra low power circuit design
  - Zero IQ pull-down structure
  - Adaptive-bias comparator
- Measured results

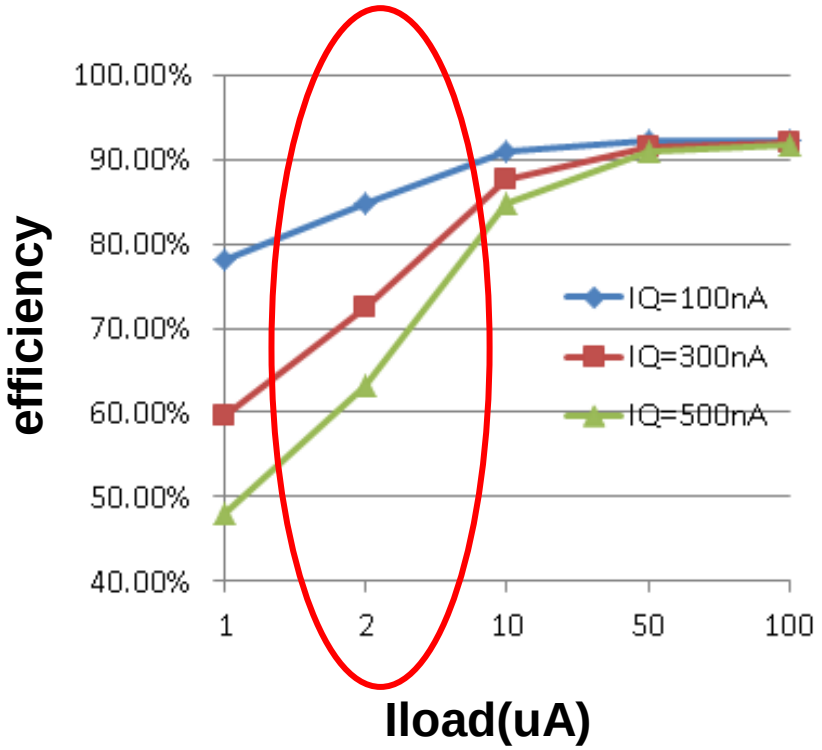
Motivation



- Ultra low IQ DC-DC convertor could extends battery life to achieve the longest operation lifespan
- If the IQ is low enough, it could also be used in energy harvest application with high open voltage, such as Piezo-harvest or RF power

Efficiency analysis

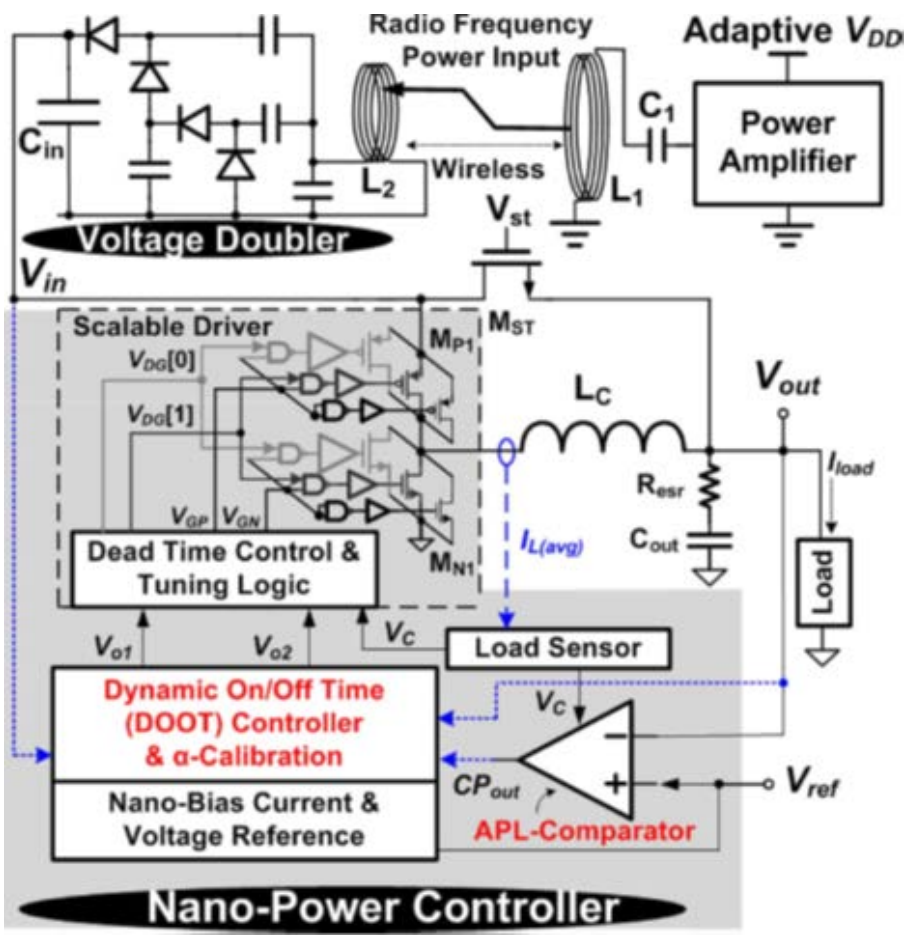




- IQ breakdown could improve the efficiency below 10uA load
- Further IQ reduction might be not so necessary since the best battery self-leakage is about 1uA currently

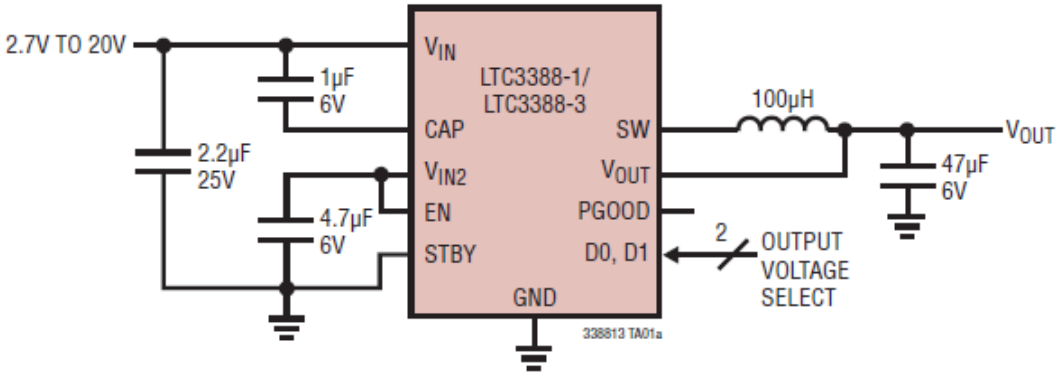
Previous research

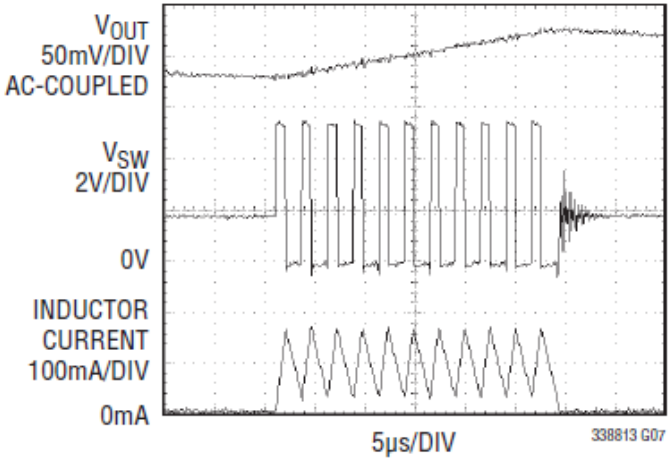
- Using dynamic on/off time control to realize low IQ control
- Total IQ is about 180nA with bias and reference circuit
- The IQ of supply monitor (like power-on reset or under voltage lockout) is not included.
- Supply monitor is necessary for every DC-DC converter chip



JSSC 2012 [1]

Previous research





LTC 3388 [3]

- **Using Hysteresis control to realize low IQ**
- **Total IQ is about 720nA with reference and supply monitor circuit**
- **Output ripple is large (~50mV) for the delay of the hysteresis comparator when bias current is reducing**

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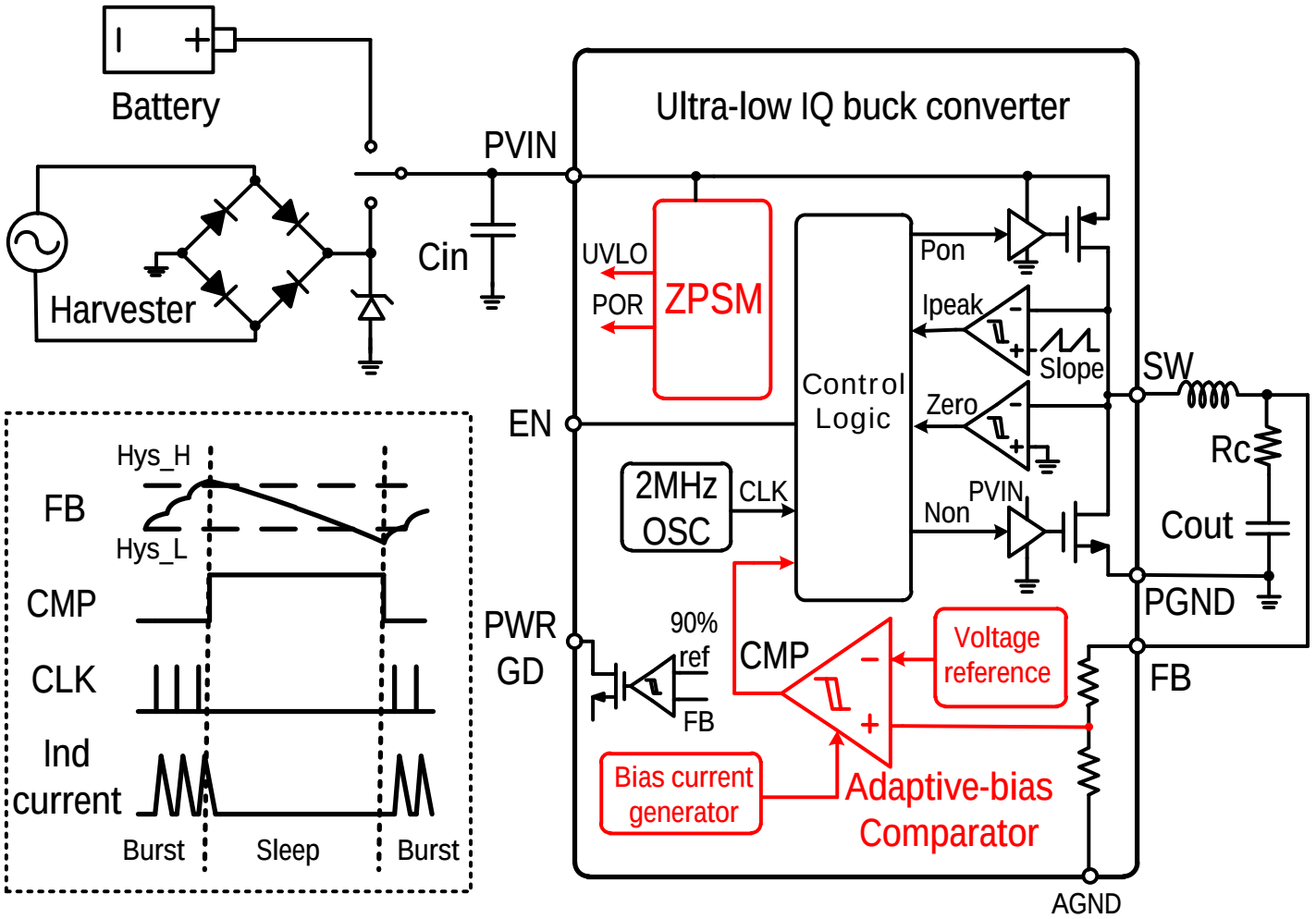
System Block Diagram



Sleep Mode IQ Breakdown

Function Block	IQ (nA)
1nA bias	15
Bandgap reference	65
Adaptive-bias comparator	30
POR	0
UVLO	0
Total IQ	110

- **Voltage reference and bias current cost about 70% of IQ budget to achieve high accuracy**
- **30nA is consumed on adaptive-bias comparator, which could perfectly limit output ripple in different load condition**
- **Zero IQ pull-down structure is applied to realize zero power POR and UVLO**

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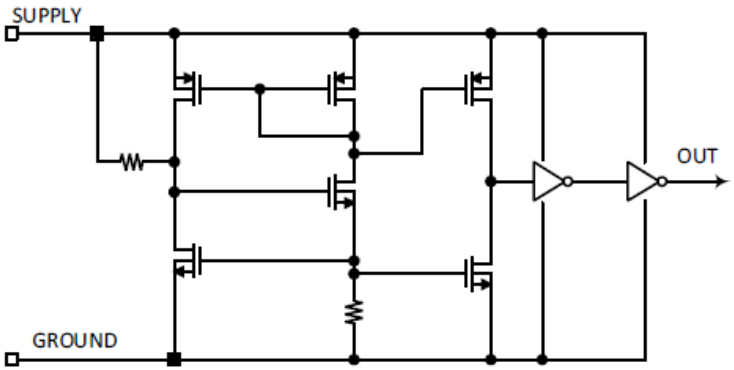
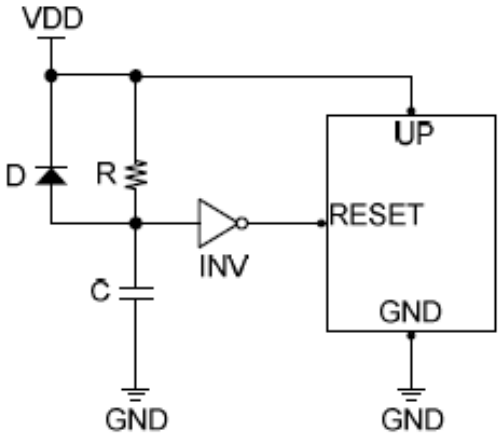
Previous research



IQ required

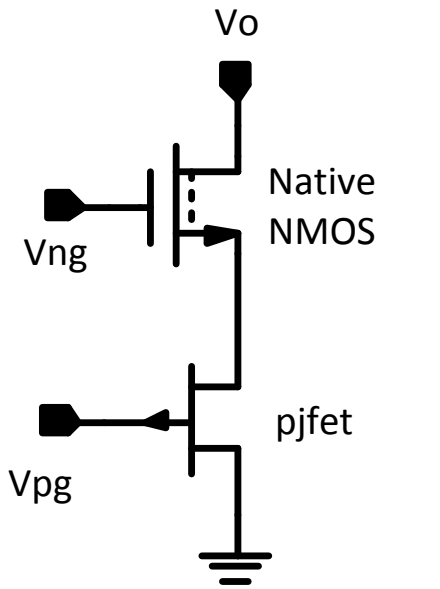


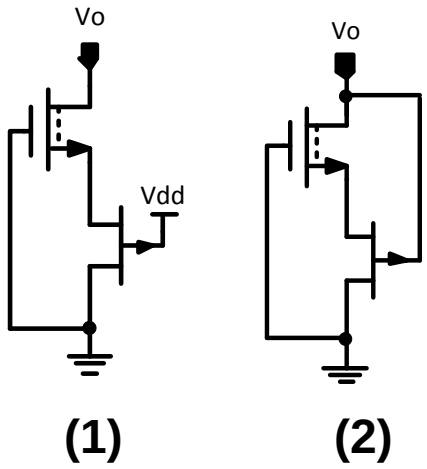
Zero IQ based on capacitor

DCAS 2014 [6]

- **traditional supply monitor circuit requires several uA IQ**
- **Previous zero IQ POR structure based on charging capacitor, so it could not monitor the falling edge of supply**
- **UVLO should monitor both rising and falling of supply voltage**

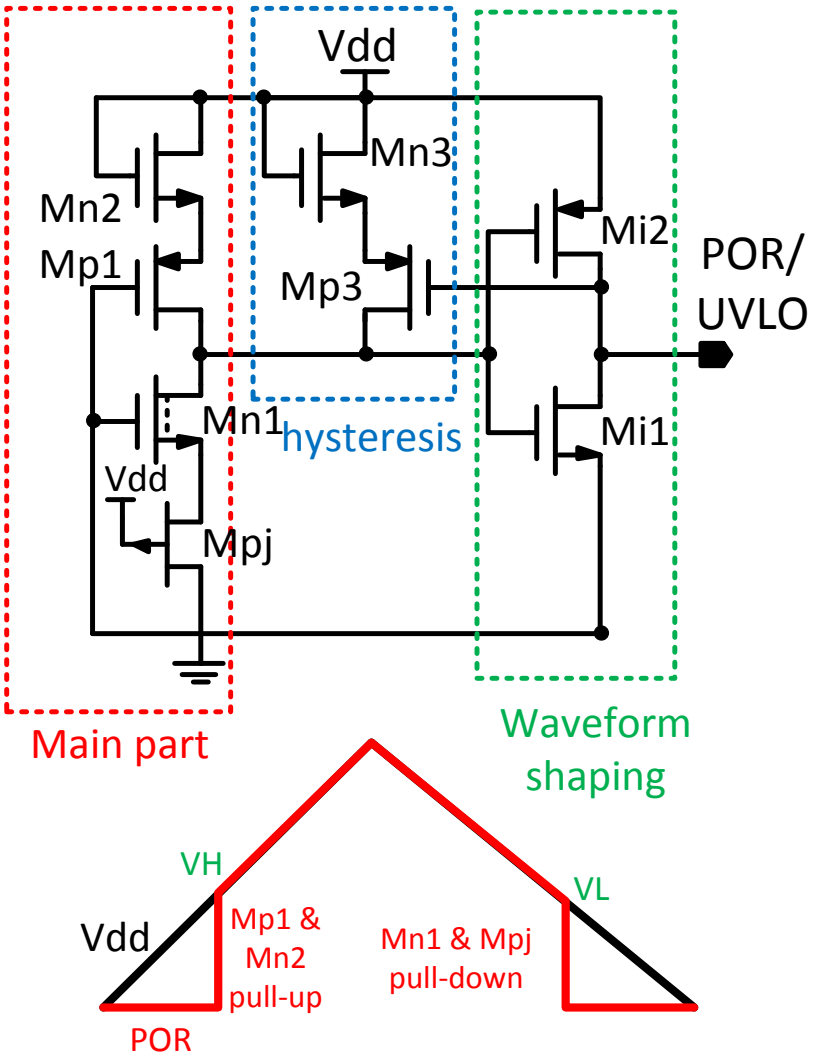
Zero IQ Pull-Down Structure





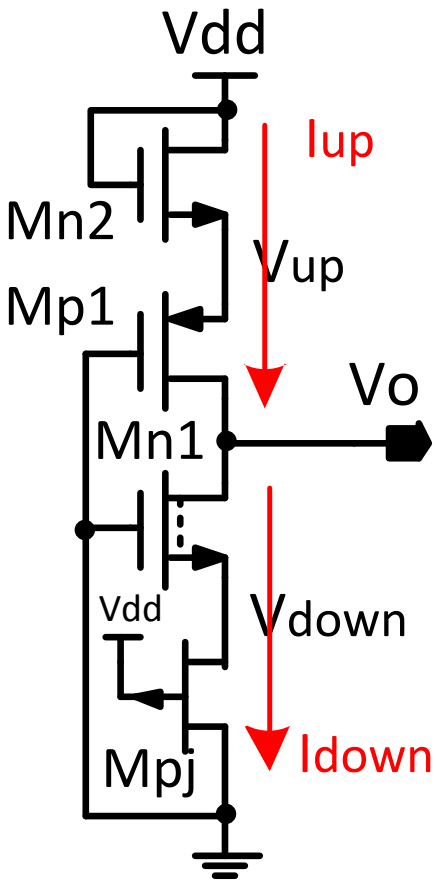
- **Consist of Native NMOS and p-jfet**
- **It have pull-down ability on Vo even Vng and Vpg is near 0**
- **It could be used with different connection to achieve zero IQ**
  - when Vdd/Vo is larger than Vp-Vthnt, the pull-down current is decreasing to zero

Zero IQ POR & UVLO



- When Vdd < VL, pull-down pass (Mn1+Mpj) will set output to 1
- When Vdd > VH, pull-up pass (Mp1+Mn2) will set output to 0
- Mp3 and Mn3 generate the hysteretic window
- Ipull-down is reduced when Vdd increasing, so Iq ≈ 0

Threshold voltage calculation



$$I_{down} = I_{pj0}\frac{W_{pj}}{L_{pj}}\exp(\frac{q(-(V_{dd}-V_{down})+V_p)}{n_{pj}kT})\exp(\frac{qK_1V_{down}}{kT}) = I_{n0}\frac{W_{n1}}{L_{n1}}\exp(\frac{q(-V_{down}-V_{thnt})}{n_nkT})$$

$$I_{up} = I_{p0}\frac{W_{p1}}{L_{p1}}\exp(\frac{q(V_{up}-V_{thp})}{nkT}) = I_{p0}\frac{W_{n2}}{L_{n2}}\exp(\frac{q(V_{dd}-V_{up}-V_{thn})}{nkT})$$

$$\Longrightarrow V_{down} = \frac{\frac{V_{dd}-V_p}{n_{pj}} - \frac{V_{thnt}}{n_n} + V_T\ln\frac{W_nL_pI_n}{W_pL_nI_{pj}}}{\frac{1}{n_{pj}}+\frac{1}{n_n}+K_1} \qquad V_{up} = \frac{V_{dd}+V_{thp}-V_{thn}}{2} + \frac{1}{2}n_pV_T\ln\frac{W_{n2}L_{p1}}{W_{n1}L_{p2}}$$

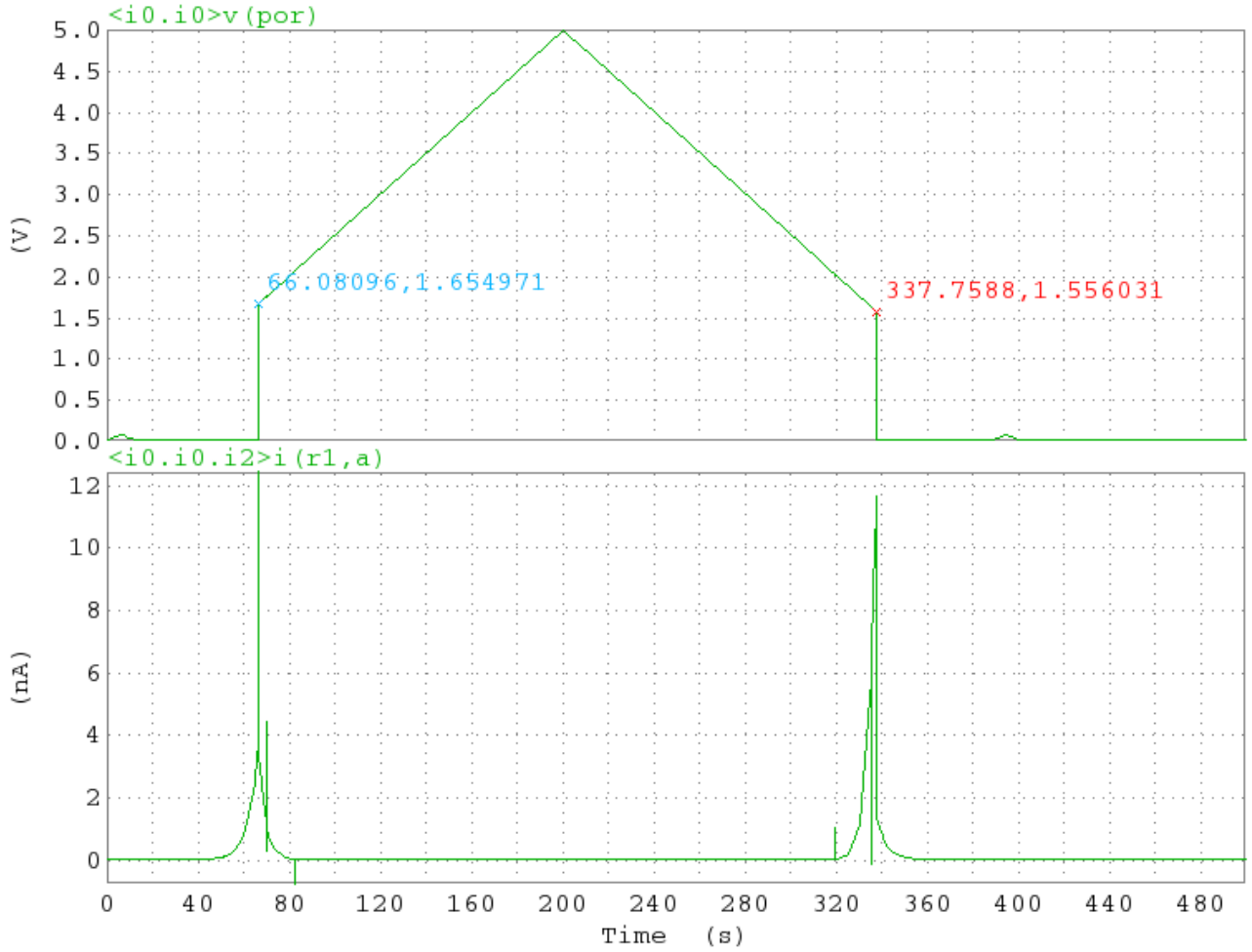
$$I_{up} = I_{down}$$

To simplify the result, assuming npj=nn=np=1, K1=0, Ip0=Ipj0=Ino and the size of all transistors are equal, then

$$V_{th\_ZPSM} = \frac{V_{thp}+V_{thn}}{2} + \frac{V_p-V_{thnt}}{2}$$

Temperature variation of Vth and Vp could be cancelled to some extent

IQ simulation



Zero IQ in the working region and several nA near the threshold voltage

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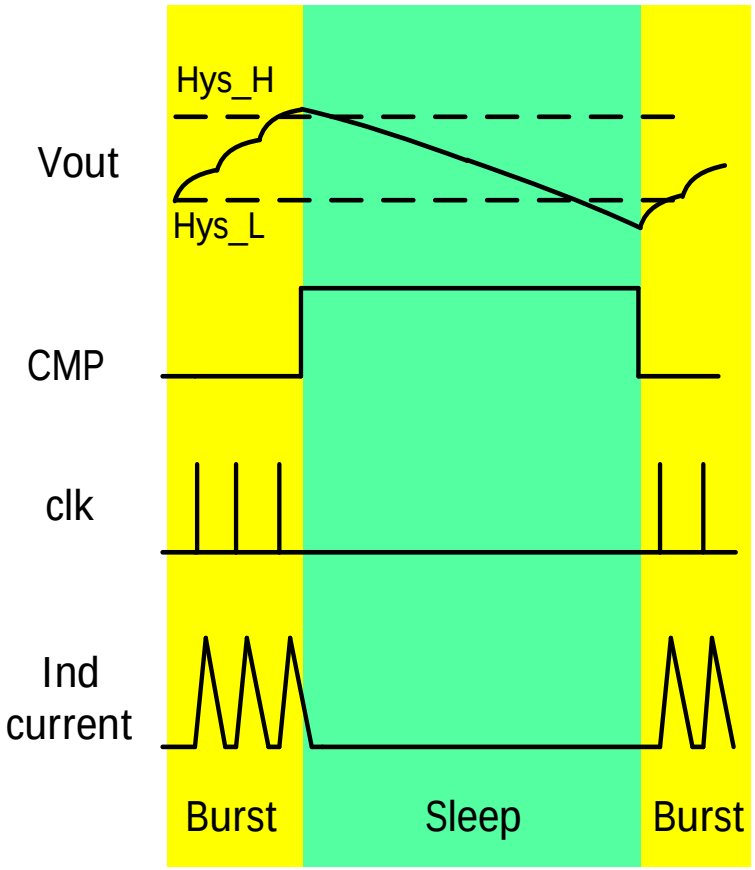
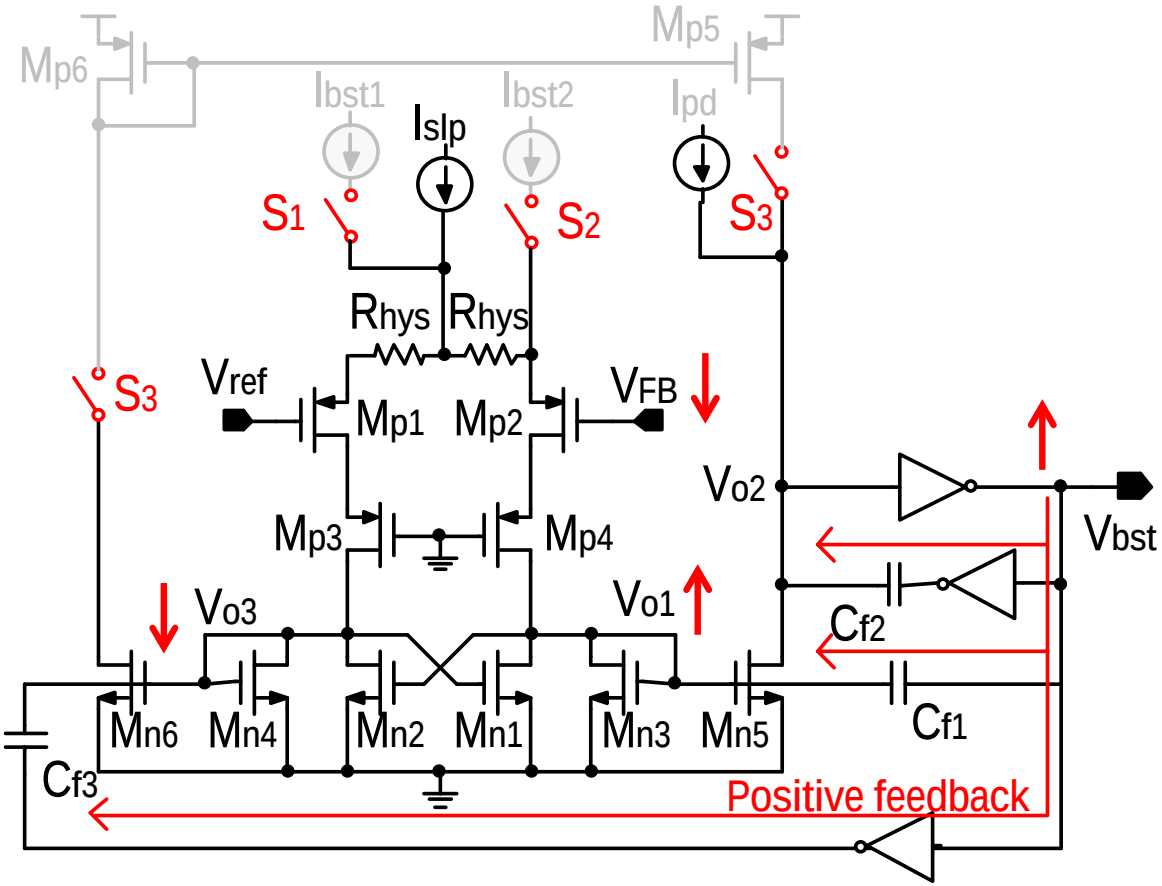
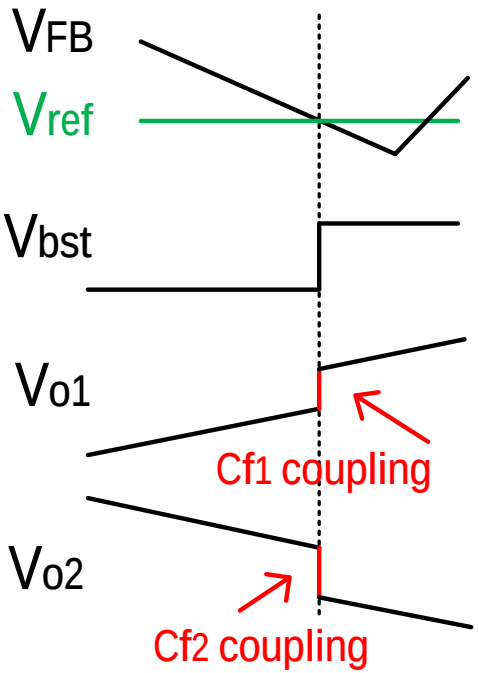
Adaptive-bias comparator



- In sleep, hysteresis comparator should keep alive to monitor Vout, so its IQ is critical for total IQ budget
- In burst, hysteresis comparator should fast detect whether Vout is higher than high threshold to control the ripple
- In heavy load, the discharge of output capacitor in sleep mode is fast and it will enlarge the ripple
- Therefore, we use adaptive-bias structure in circuit design

Adaptive-bias comparator in sleep

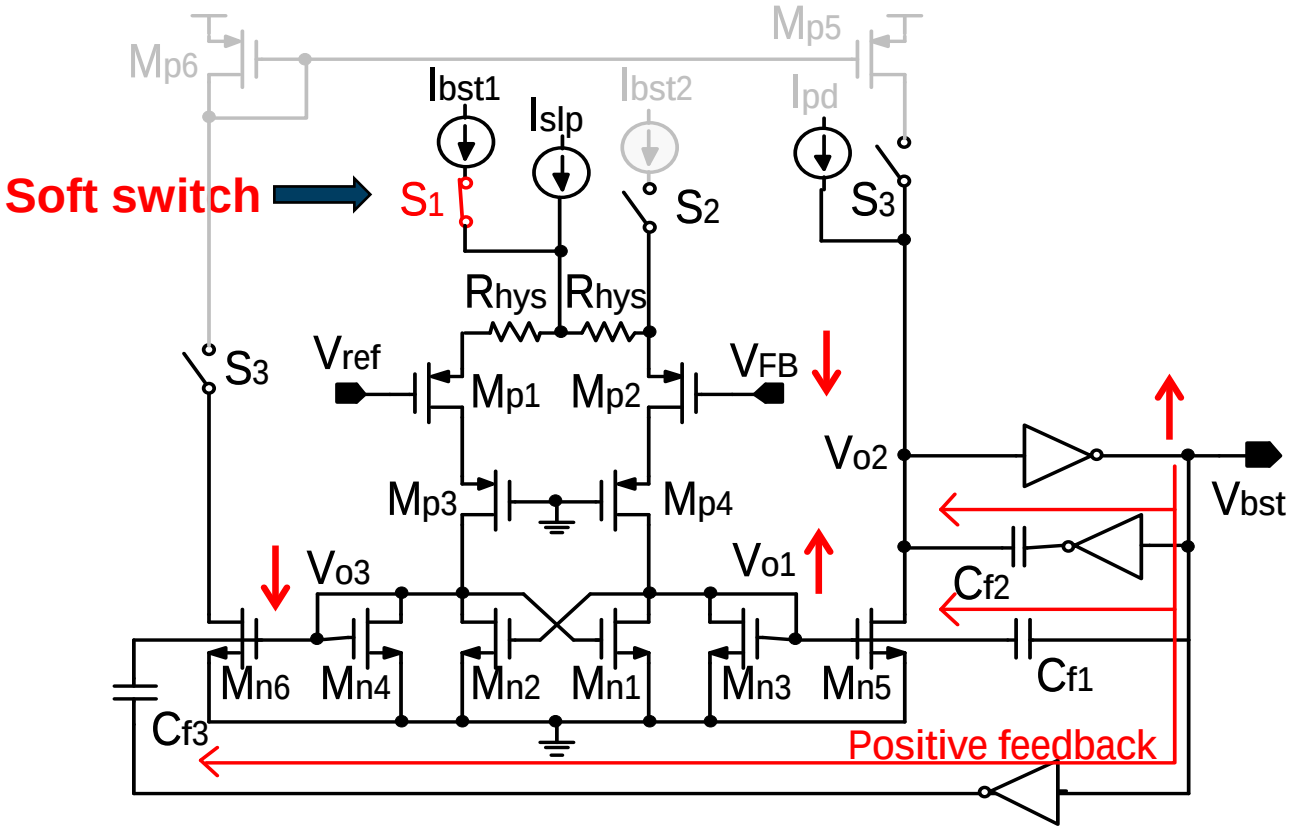




positive feedback

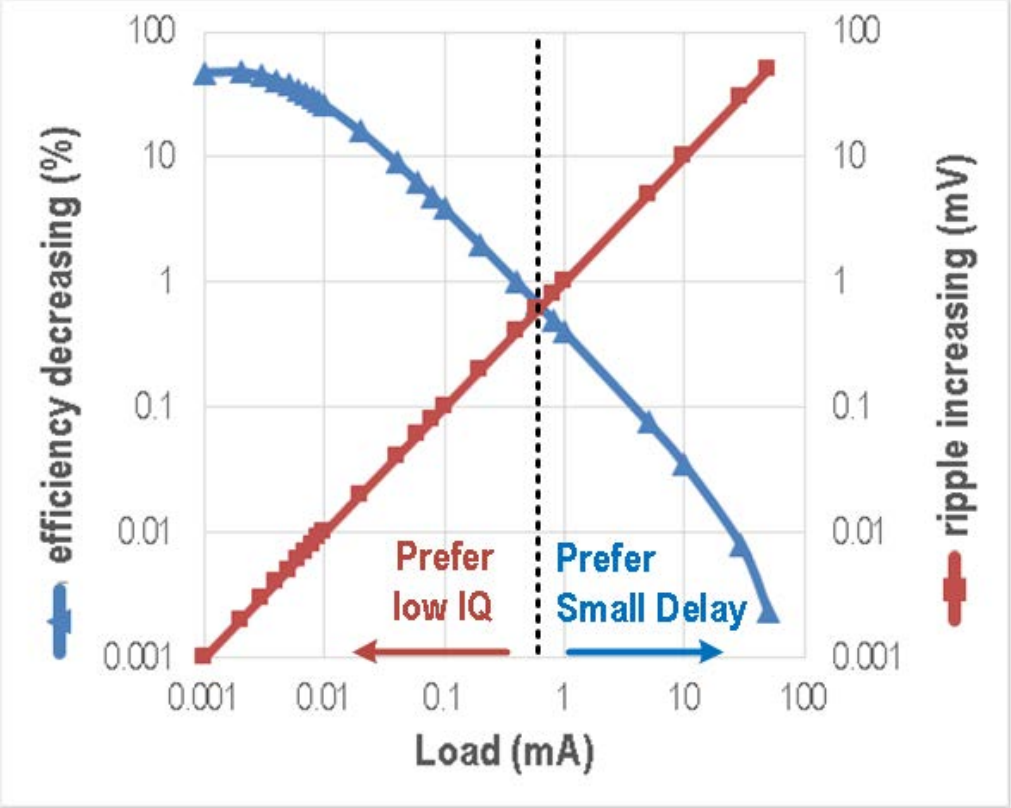
- **The comparator is only biased by Islp , so IQ is 30nA**
- **Two positive feedback passes are added to avoid glitch**

Large load current in sleep



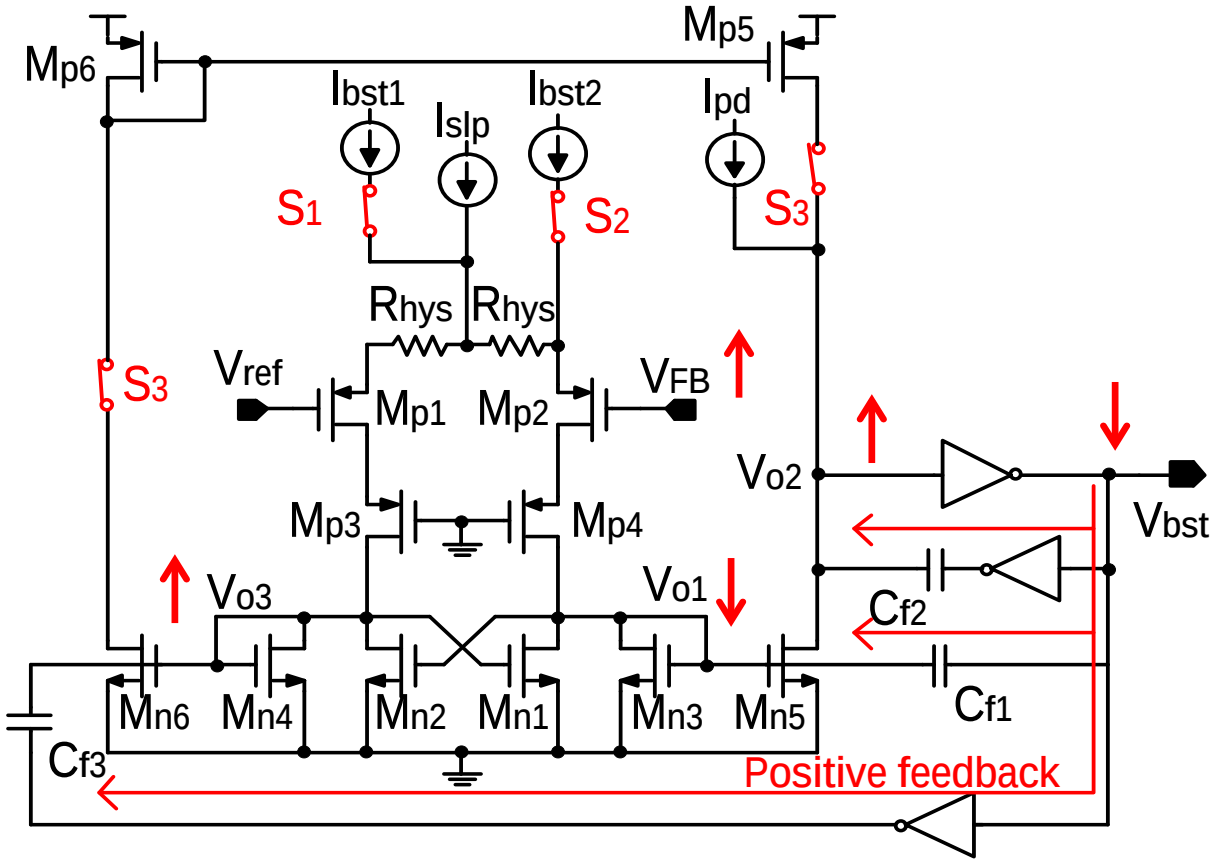
- In heavy load sleep mode, S1 are turned on and the bias current is increased to Ibst1+Islp, so IQ is about 1.5uA
- The current switch will open slowly to avoid glitch

Efficiency vs output ripple



- If load > 0.5mA, efficiency degeneration is less than 1% when the large bias current of comparator is used.
- output ripple will not increase more than 1mV with 30nA biased comparator unless the load is larger than 1mA
- Large bias current will be used at load>1mA and exit at load<0.5mA

Adaptive-bias comparator in burst



- All switches are turned on, so the bias current rises to Ibst1+ Ibst2+Islp and IQ is about 3uA
- Positive feedback passes are function through Cf1~3 in reverse direction of sleep during mode transition

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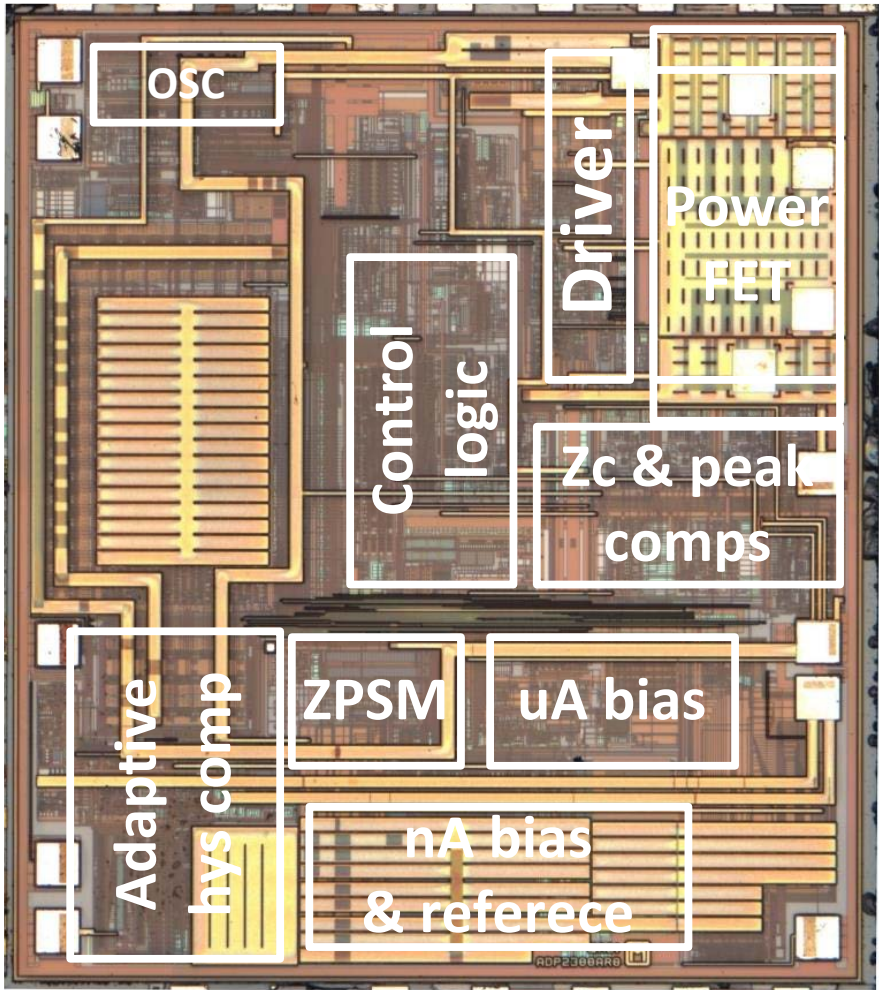
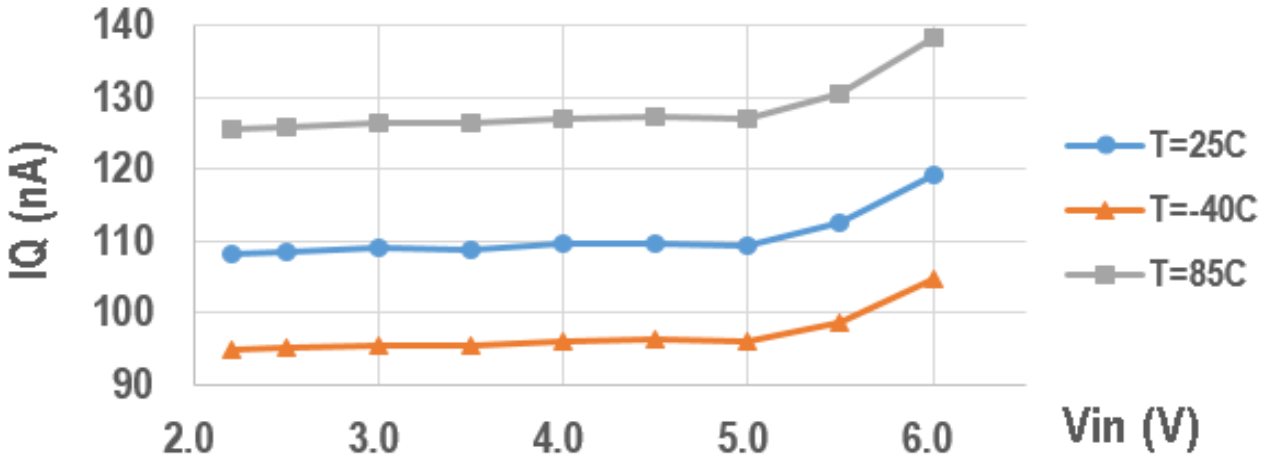
Chip Diagram



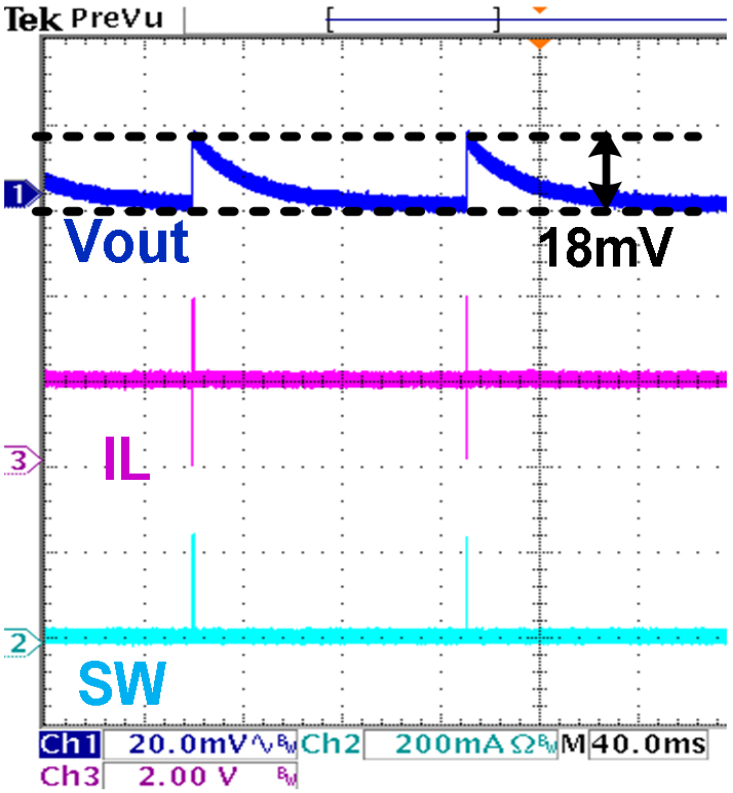
- Process
  - 2P4M 0.35um CMOS
- Core size
  - 1610um x 1830um

Quiescent Current

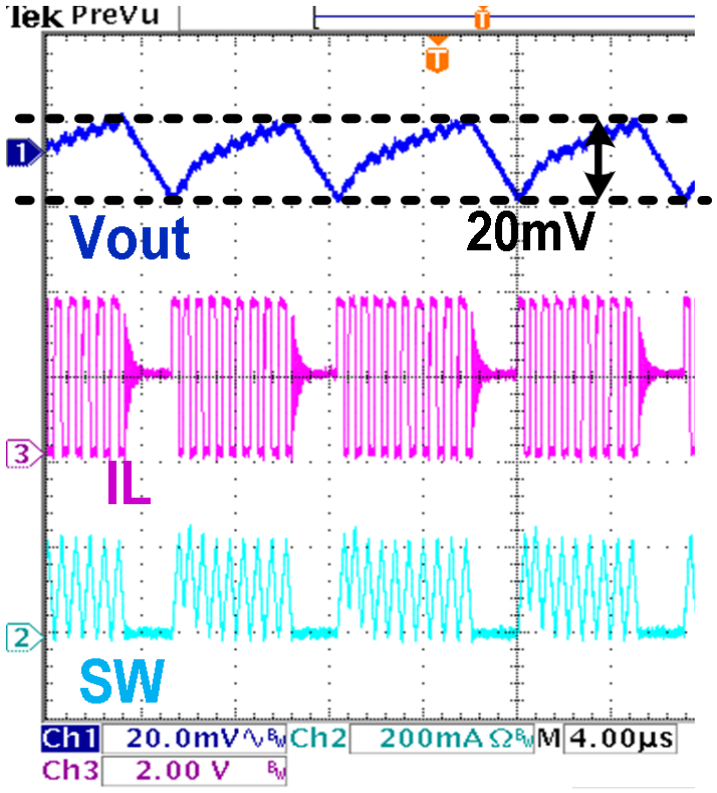


- the total IQ is about 110nA when Vin=3.6V in normal temp
- IQ variation with temperature is small, even in 85C it will not be larger than 140nA

Output ripple in PSM mode



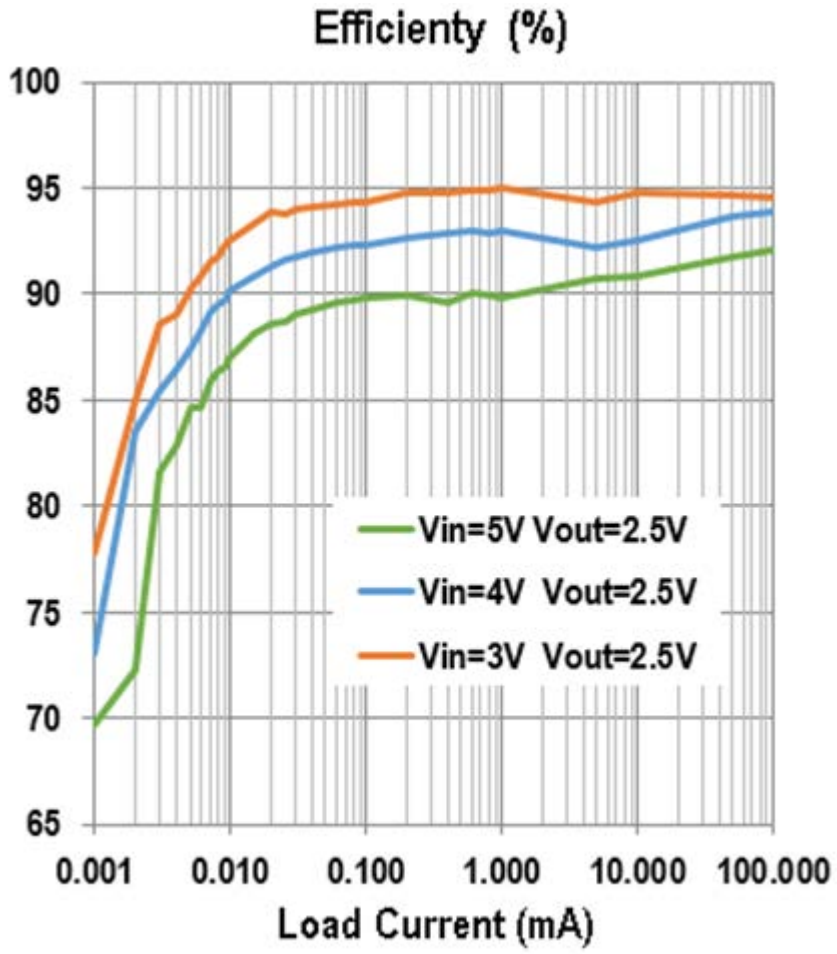
18mV@1uA



20mV@100mA

- With adaptive-bias PSM comparator, only 2mV output ripple increment is realized when load current increases one hundred thousand times

Efficiency



- The peak efficiency reaches 95% with 3V Vin, 2.5V Vout and 1mA
- Over 90% efficiency is achieved for above 5uA load when Vin=3V

Summary and Comparison

	JSSC 2012 [1]	ISCAS 2009 [2]	LTC3388 [3]	ISSCC 2015 [4]	This work
Process	0.25µm	0.18µm	-	0.18um	0.35 µm
Supply voltage (V)	1.2 ~ 2.5	1.6 ~3.6	2.7 ~ 20	0.55 ~ 1	2.2 ~ 6
Inductor & capacitor	3.3 µH & 4.7 µF	-	100 µH & 47 µF	4.7 µH -	2.2 µH & 10uF
Load capability (mA)	10	50	50	20	100
IQ (nA)	181	960	720	-	110
Supply monitor	No	No	No	No	Yes
Output ripple (mV)	30	20	50	10	20
Ripple variation (mV)	-	18	15	-	2
Efficiency @ 1uA load	61%	42%	45%	75%	78%
Peak efficiency	95%	95%	90%	92%	95%

Reference

[1] T. Huang, C. Hsieh, Y. Yang, et al., “A Battery-Free 217 nW Static Control Power Buck Converter for Wireless RF Energy Harvesting With -Calibrated Dynamic On/Off Time and Adaptive Phase Lead Control,” *IEEE J. of Solid-State Circuits.*, vol. 47, no. 4, pp. 852-862, Apr. 2012.

[2] N. Schemm, et al. “The design of an ultra-low power buck regulator supporting dynamic voltage scaling for wireless sensor networks,” *IEEE ISCAS*, pp. 828-831, 2009.

[3] Linear Technology, “LTC3388 Datasheet,” http://cds.linear.com/docs/en/datasheet/338813f.pdf, Aug. 2010

[4] P. Chen, C. Wu, K. Lin, “A 50nW-to-10mW output power tri-mode digital buck converter with self-tracking zero current detection for photovoltaic energy harvesting,” *IEEE ISSCC*, pp. 376-378, Feb. 2015.

[5] R. Prakash, “Zero Quiescent Current, Delay Adjustable, Power-on-Reset Circuit,” *IEEE DCAS*, pp. 1-4, 2014.

Q & A

Thanks you !