Fast-Transient Asynchronous Digital LDO with Load Regulation Enhancement by Soft Multi-Step Switching and Adaptive Timing Techniques in 65-nm CMOS

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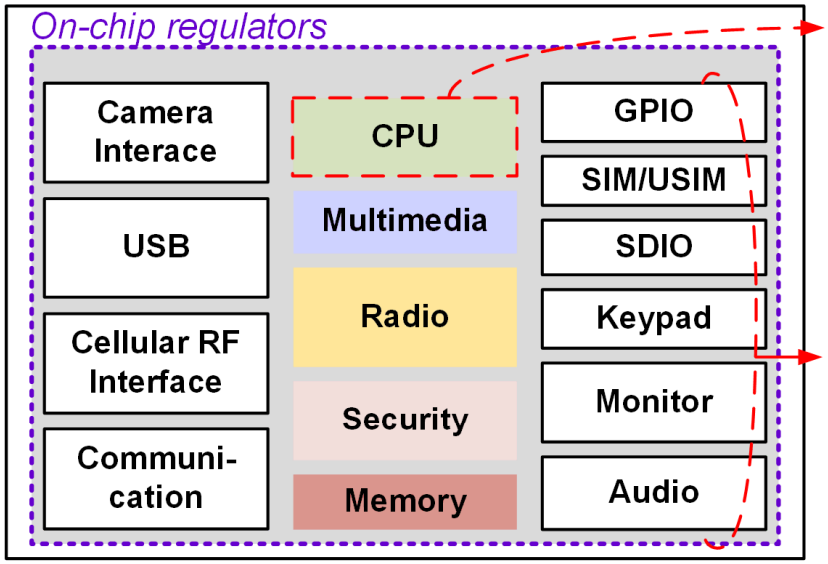
Outline

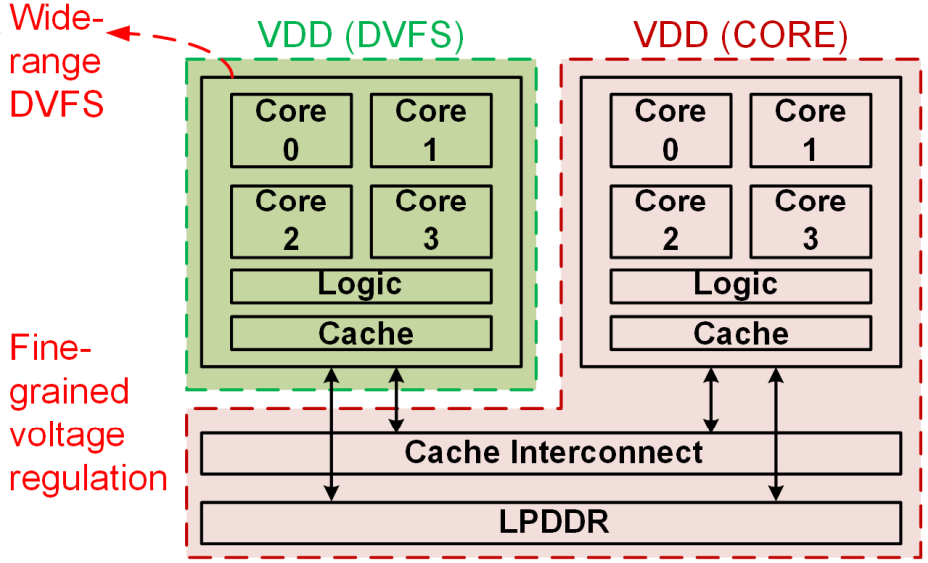
- **Background and Motivations**
  - Mixed-signal on-chip power management
- **Review of Fine-grained Digital LDO**
- **Proposed Asynchronous Digital LDO**
  - Analysis of voltage regulation
  - Soft multi-step switching and adaptive timing
- **Measurement Results**
- **Comparison & Conclusions**

Mixed-signal on-chip power management

- Wide-range: Dynamic voltage and frequency scaling (DVFS)
- Fine-grained on-chip voltage regulation
- CPU as the power management supervisor



Eg. 1: A Cellular SoC



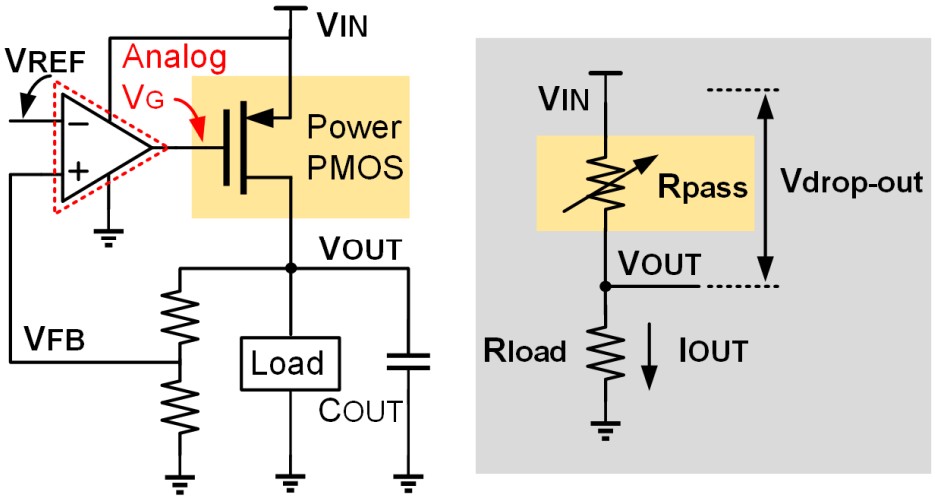
Eg. 2: An Octa-core mobile AP

[X. Jiang, ESSCIRC 2014] [M. Igarashi, ISSCC 2014]

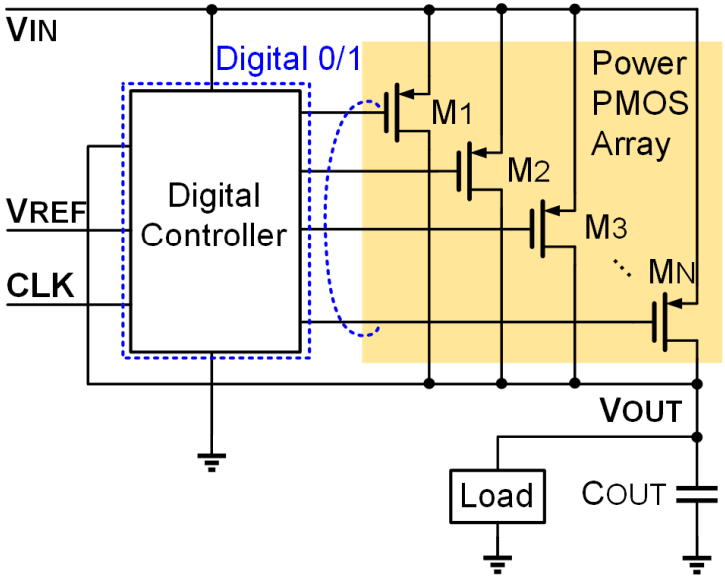
Fine-grained voltage regulation

- Low-dropout regulator (LDO)
  - "Resistor-divider"
  - Fine-grained voltage regulation
  - Controller: analog (high-gain) or digital (wide range)

Analog LDO

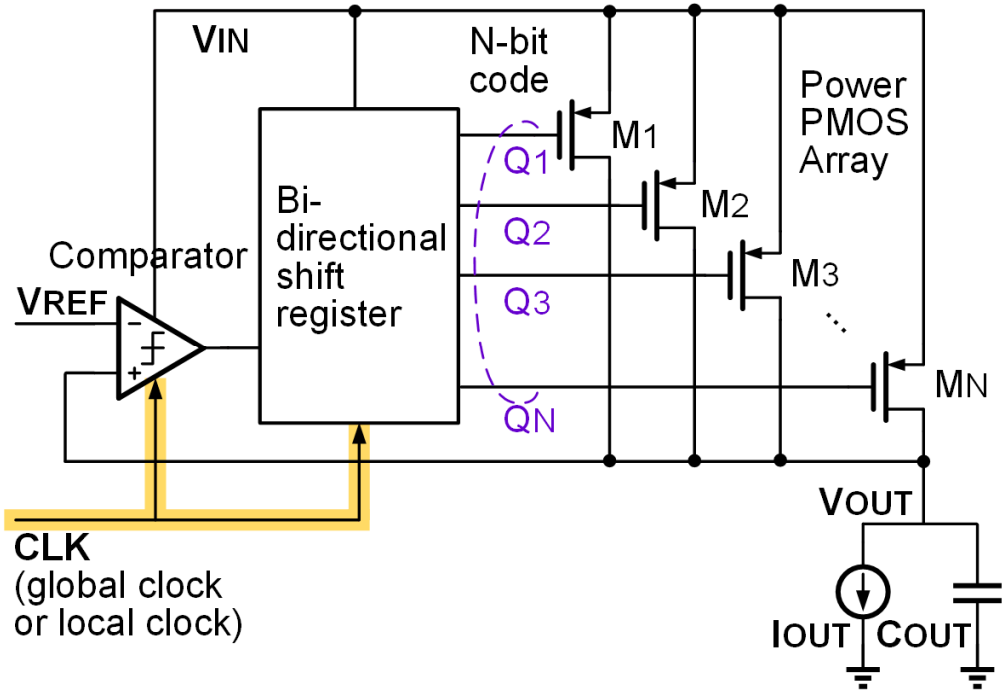


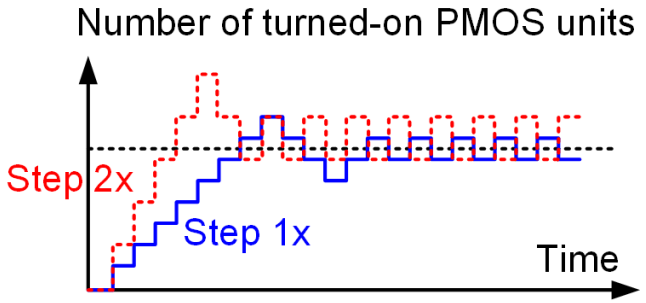
Digital LDO



DAC-ADC-based Digital LDO

- Successive comparison: Vout ~ Vref
- ✓ **Pros:** Fully synthesizable; Flexibility; PVT robust; Low power
- × **Cons:** Coarse voltage regulation





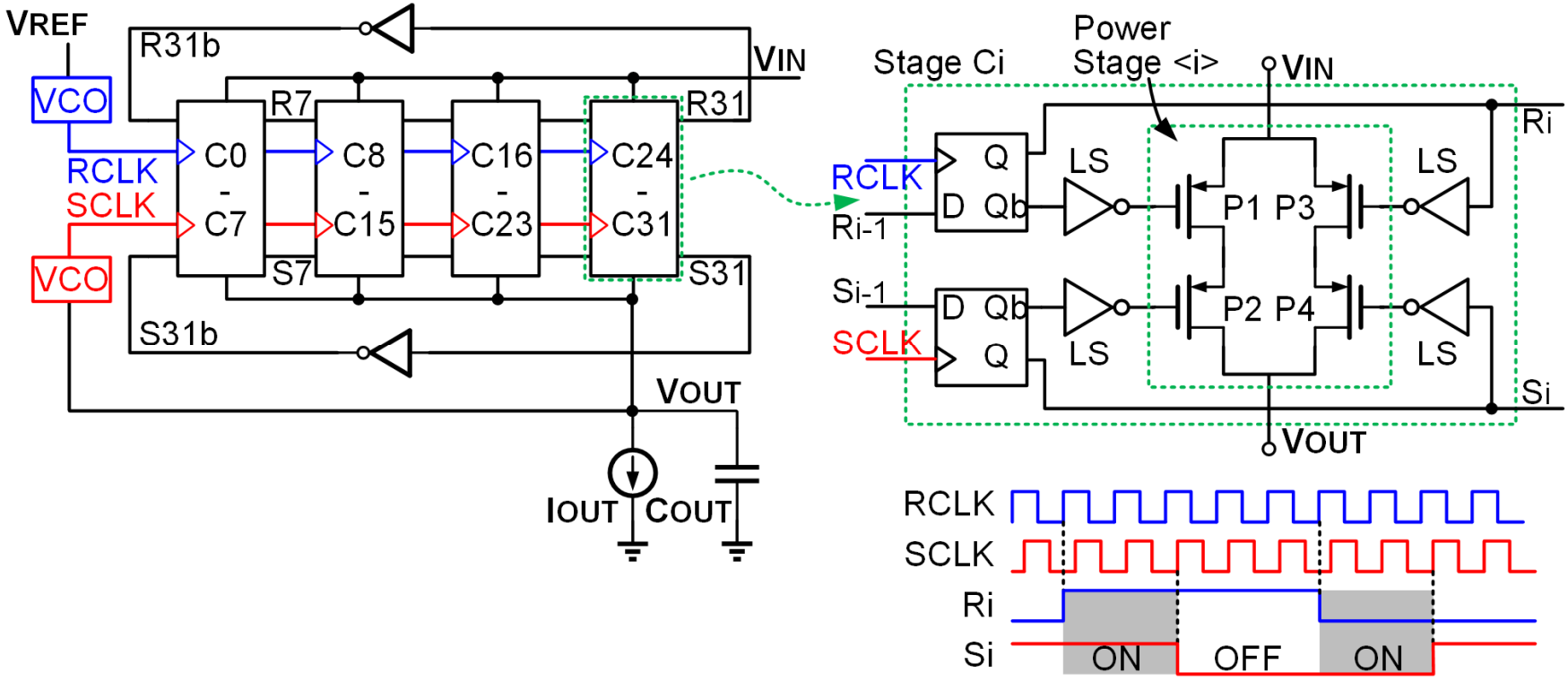
Step Size ↑ Speed ↑ Resolution ↓

Basic Metrics
- **Speed:** Transient response
- **Resolution:**
  Equivalent number of binary bits:
  $\log_2 N$ (N: # of minimum units)

[Y. Okuma, CICC 2010] [Onouchi, ASSCC 2011] [Y.-H. Lee, VLSIC 2012]

VTC-TDC-based Digital LDO

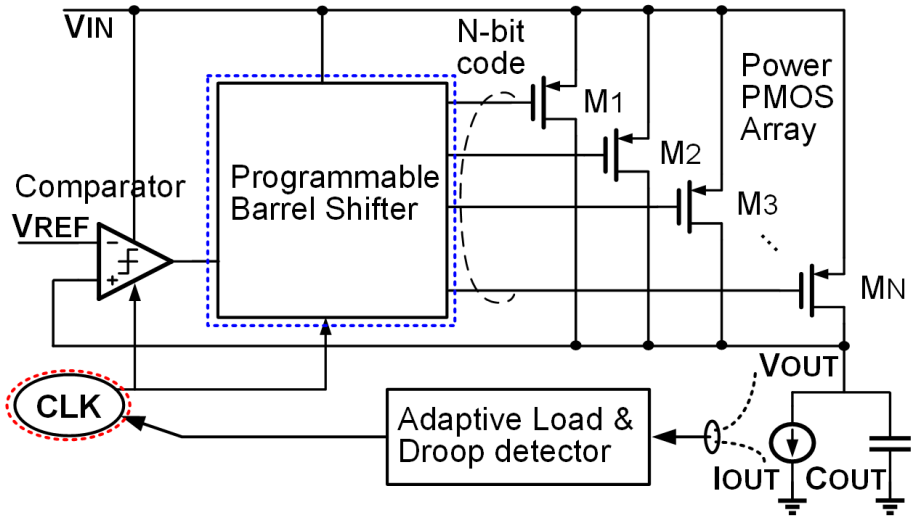
- Phase locked loop (PLL) locks the phase difference
- ✓ **Pros:** Fine voltage regulation
- ✗ **Cons:** PVT dependency; Less flexibility; High power

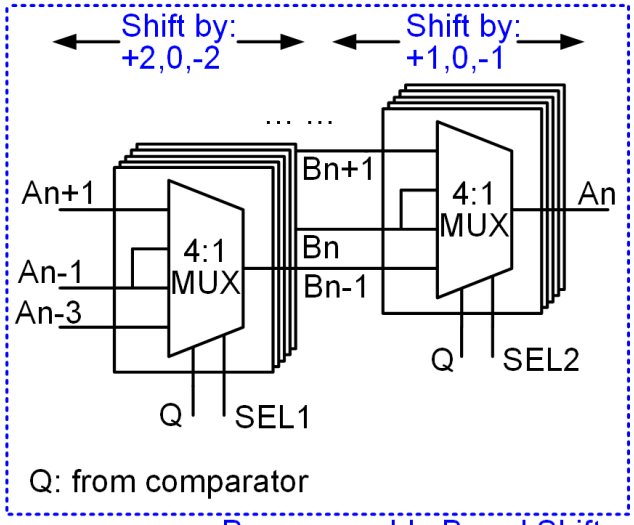


[A. Raychowdhury, VLSIC 2012]

Fine/Coarse Regulation: Multiple step size

- Multiple shift step sizes:
  - Loop gain 1x - 3x
- Adaptive frequency:
  - Large load or step
- Pros & Cons:
  - ✓ Fine/coarse adaptation
  - ✗ Analog droop detection
  - ✗ Linear improvement
  - ✗ Power hungry

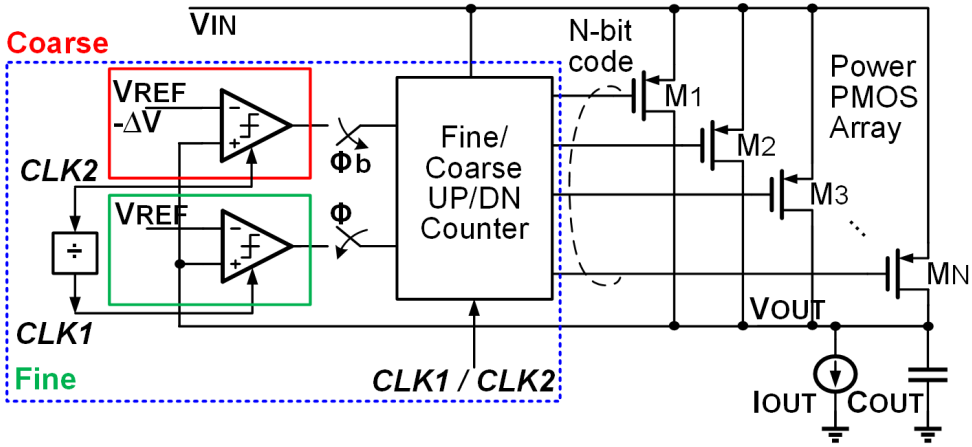


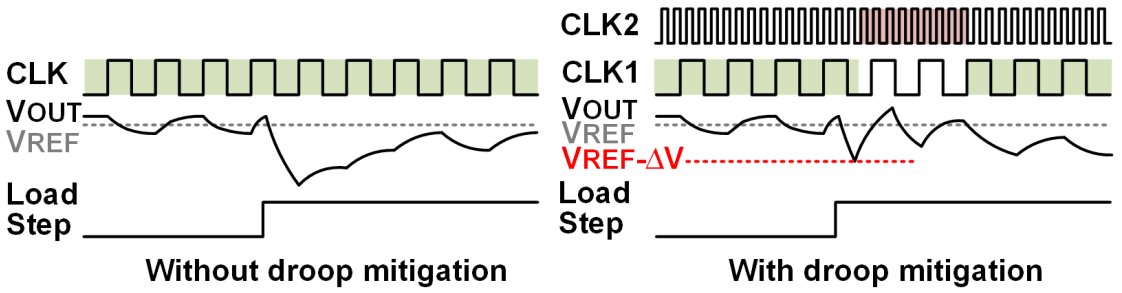


[S. B. Nasir, ISSCC 2015]

Fine/Coarse Regulation: Turbo frequency

- Dual coarse/fine counting mode:
  - Slow fine clocking for steady state
  - Fast coarse clocking for droop mitigation
- Droop detection
- Pros & Cons:
  - ✓ Fine/coarse adaptation
  - ✓ Various droop detection
  - ✗ Droop not scales with supply
  - ✗ Power hungry





[S. T. Kim, ISSCC 2015]

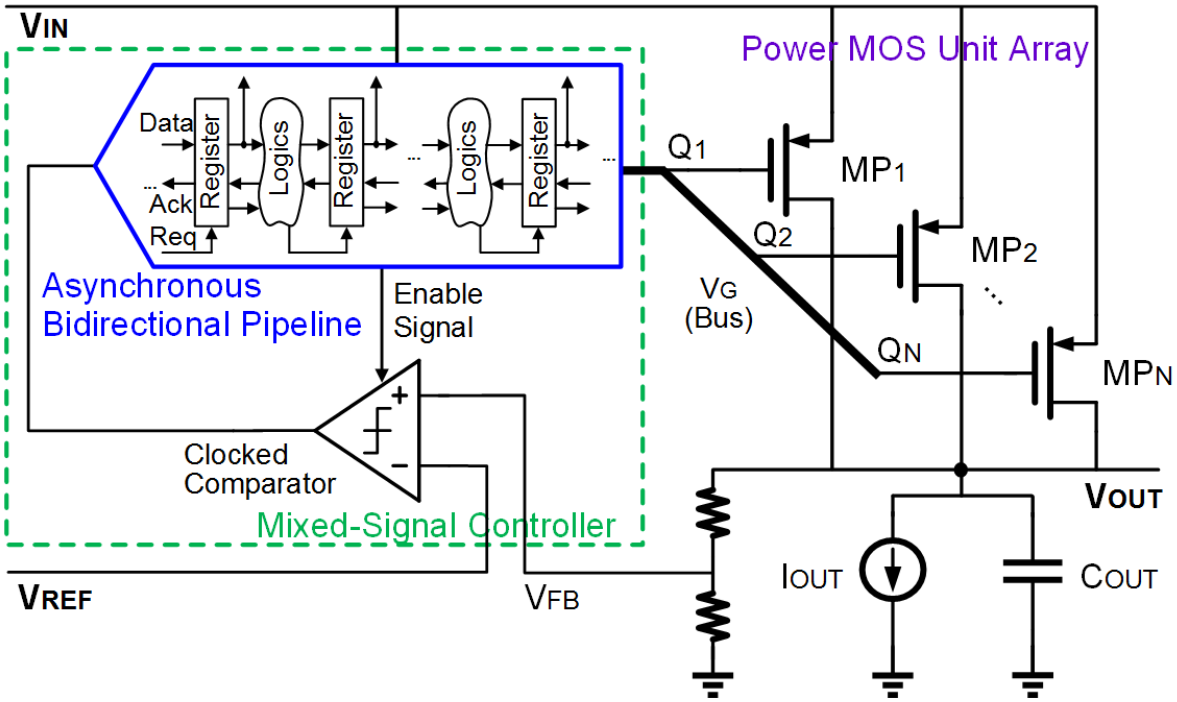
Any room for improvement?

- Limited topological innovation
  - ✗ Limited enhancement: linear multiple step size
- Clock frequency affected by PVT variation
  - ✗ Instability: turbo frequency at large load step
- Coarse/fine regulation has potential switching problem
  - ✗ Caused by size change or turbo clocking

- The need is:
  - ✓ Topology balances speed and resolution
  - ✓ Asynchronous “clocking”
  - ✓ Soft coarse/fine mode switching

Architecture of proposed digital LDO

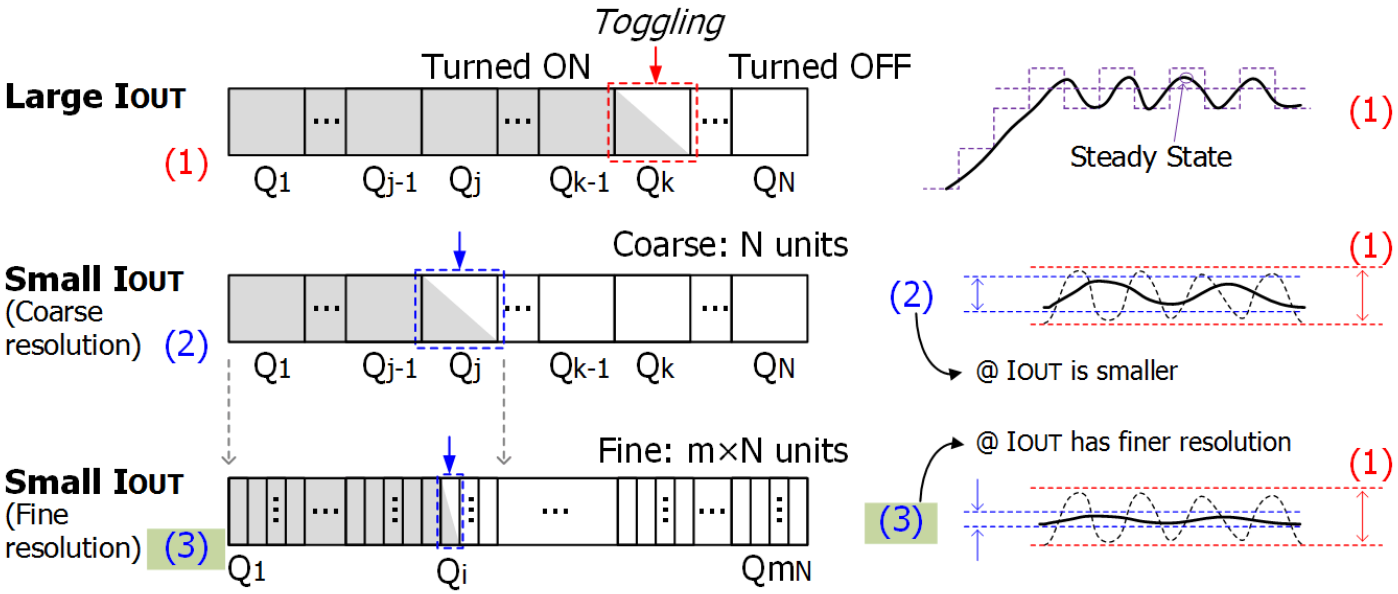
- Multiple-step-size power stage *
- Power-efficient speed and regulation enhancement
  - Regulation++: soft multi-step switching
  - Speed ++: adaptive & Power--: asynchronous clock



* [F. Yang, ESSCIRC 2015]

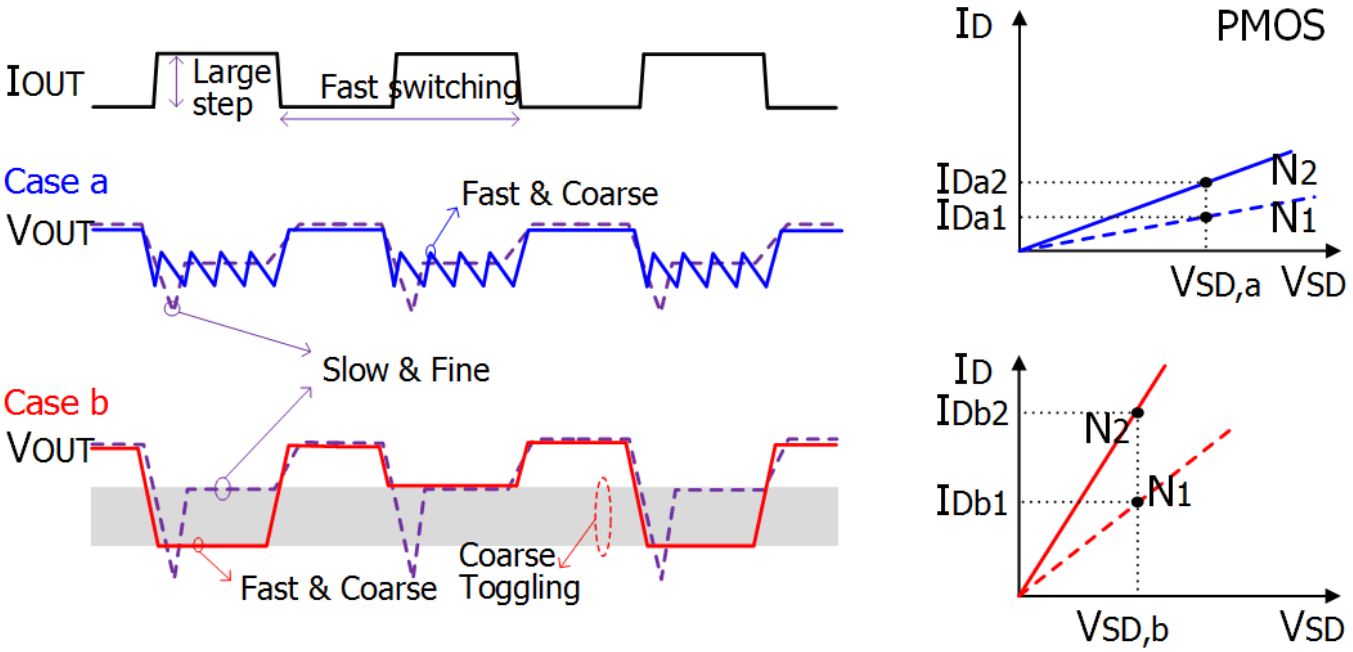
Analysis of steady state voltage regulation

- Steady state digital codes: On, Off, Toggling
- Ripple reduction by multi-step size:
  - Light load: small I_{OUT}
  - Fine resolution: m fine bit per coarse bit (N)
  - Large output capacitor



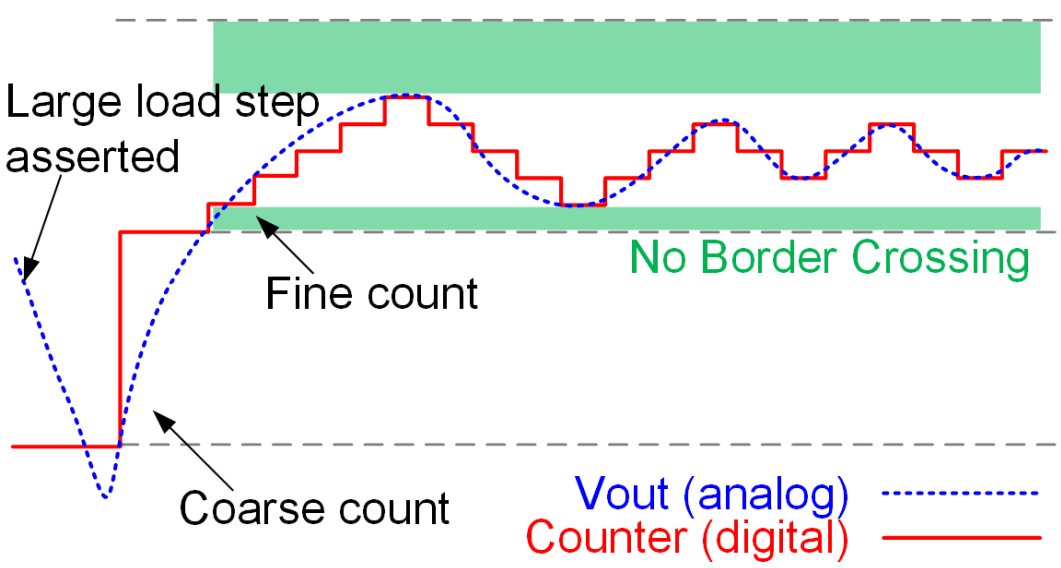
Analysis of in-transient voltage regulation

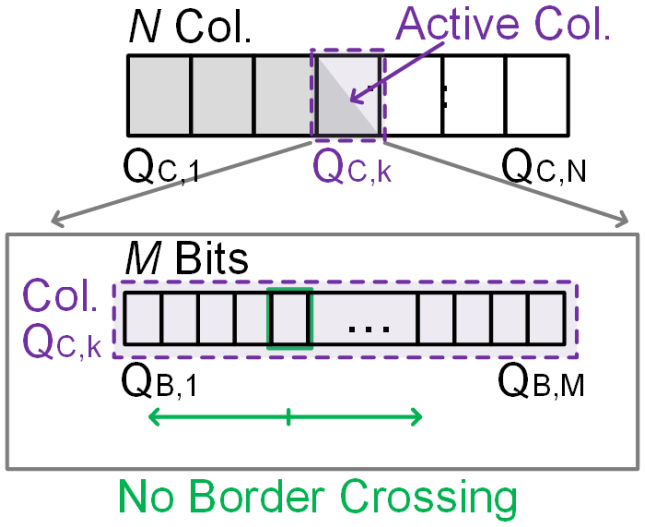
- Digitally controlled power MOS unit (PMOS)
  - Linear region (when ON), cut-off region (when OFF)
- Case a: small ripple → regulated in dc
- Case b: large ripple → regulation error (consecutive toggling)



Multi-step switching: No border crossing

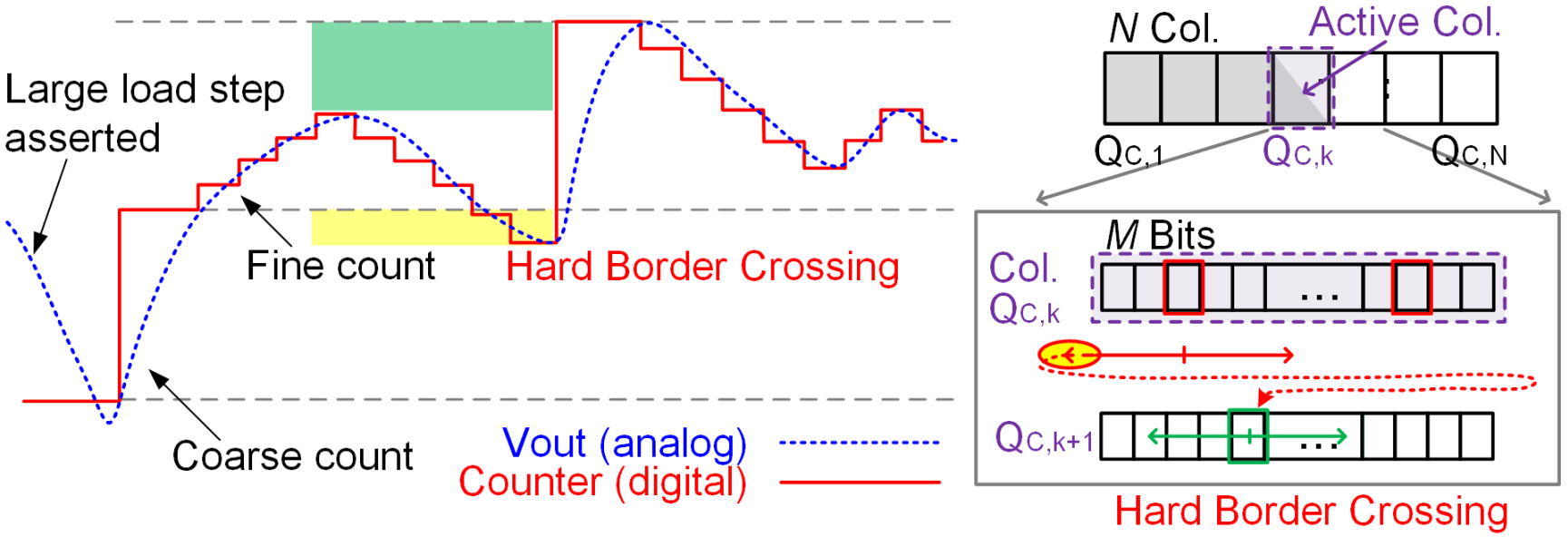
- Scenario: Two-step coarse/fine voltage regulation
  - *N* columns: each column with *M* bits
- Recovery from voltage droop @ large load step
  - Case 1: No border crossing
    - Voltage droop -> Coarse count -> Fine count … ☺





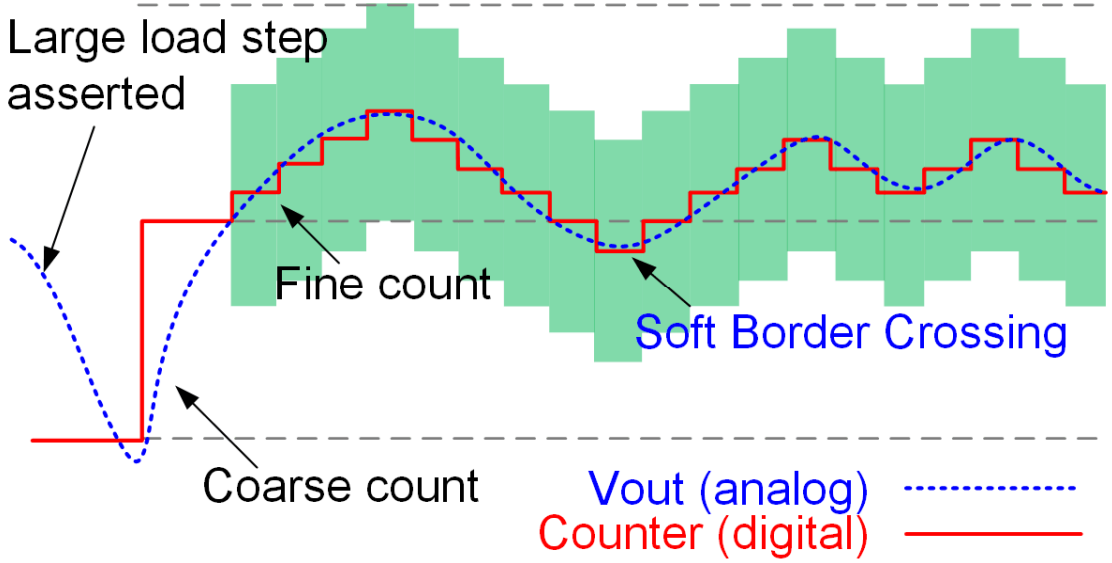
Multi-step switching: Hard border crossing

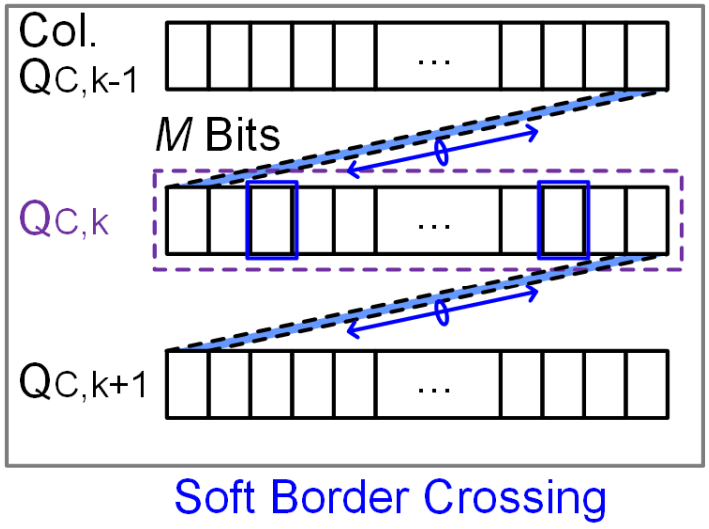
- Scenario: Two-step coarse/fine voltage regulation
  - *N* columns: each column with *M* bits
- Recovery from voltage droop @ large load step
  - Case 2A: Hard border crossing
    - Voltage droop -> Coarse -> Fine -> Coarse count -> … ☹



Multi-step switching: Soft border crossing

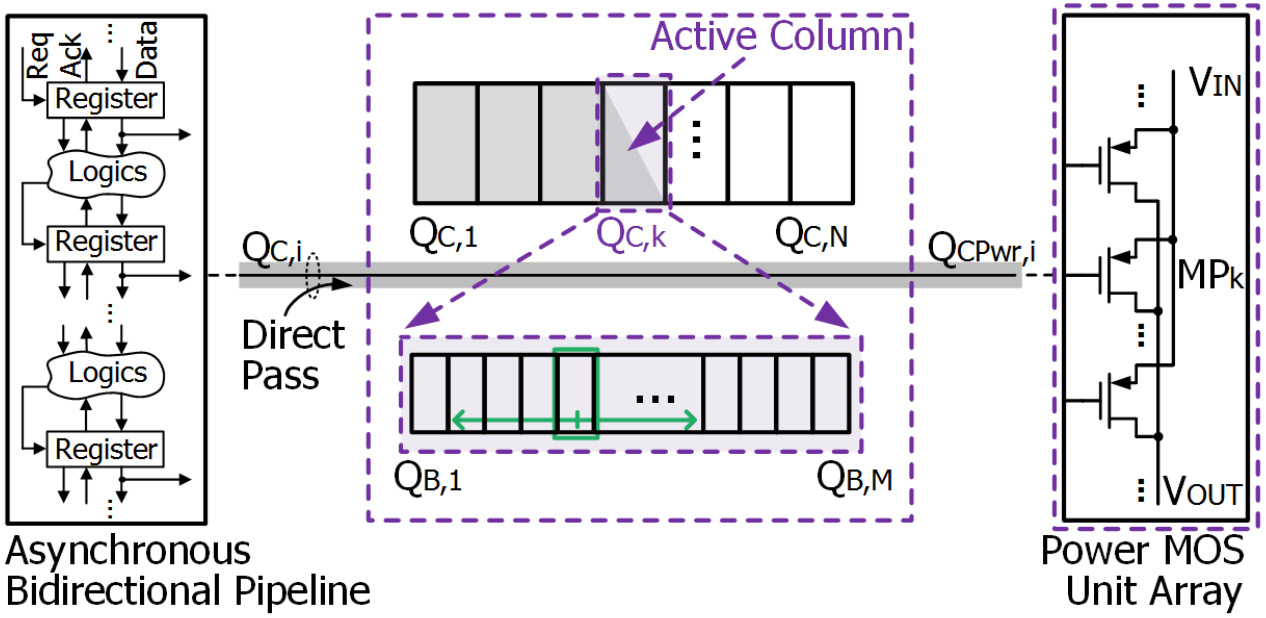
- Scenario: Two-step coarse/fine voltage regulation
  - *N* columns: each column with *M* bits
- Recovery from voltage droop @ large load step
  - Case 2B: Soft border crossing
    - Voltage droop -> Coarse count -> Fine count … ☺





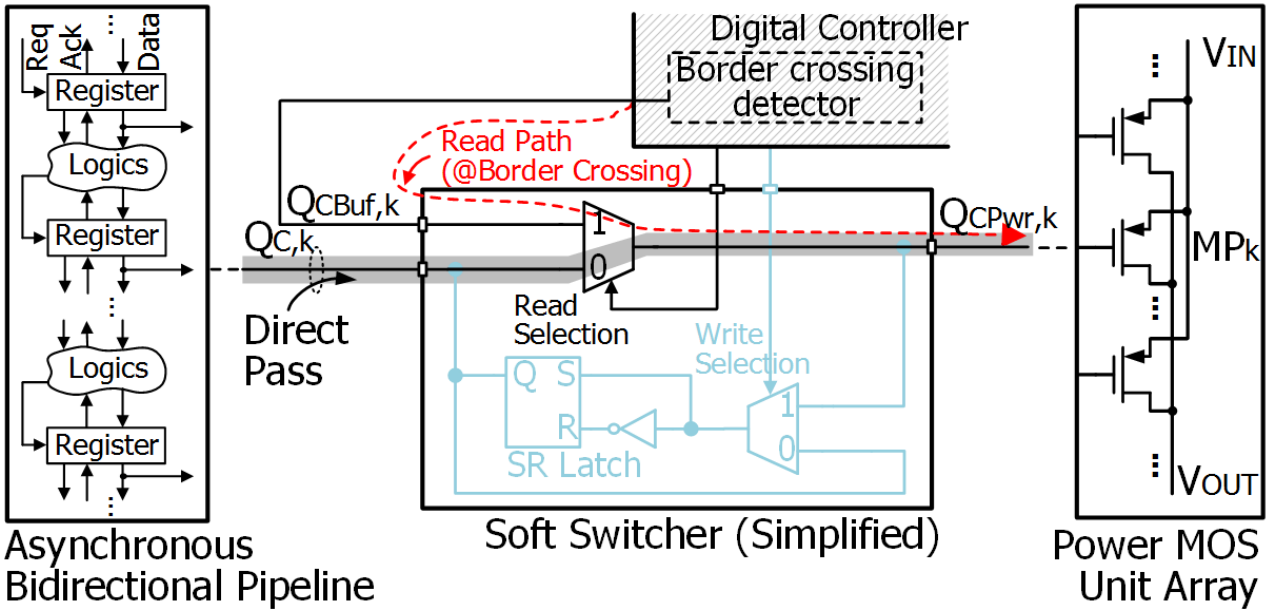
Direct multi-step switching

- Scenario: Two-step coarse/fine voltage regulation
  - *N* columns: each column with *M* bits
  - **Coarse mode:** locate active column
  - **Fine mode:** last toggling bits
- Direct pass comparator output $Q_{c,i}$ to power MOS gate $Q_{CPwr,i}$



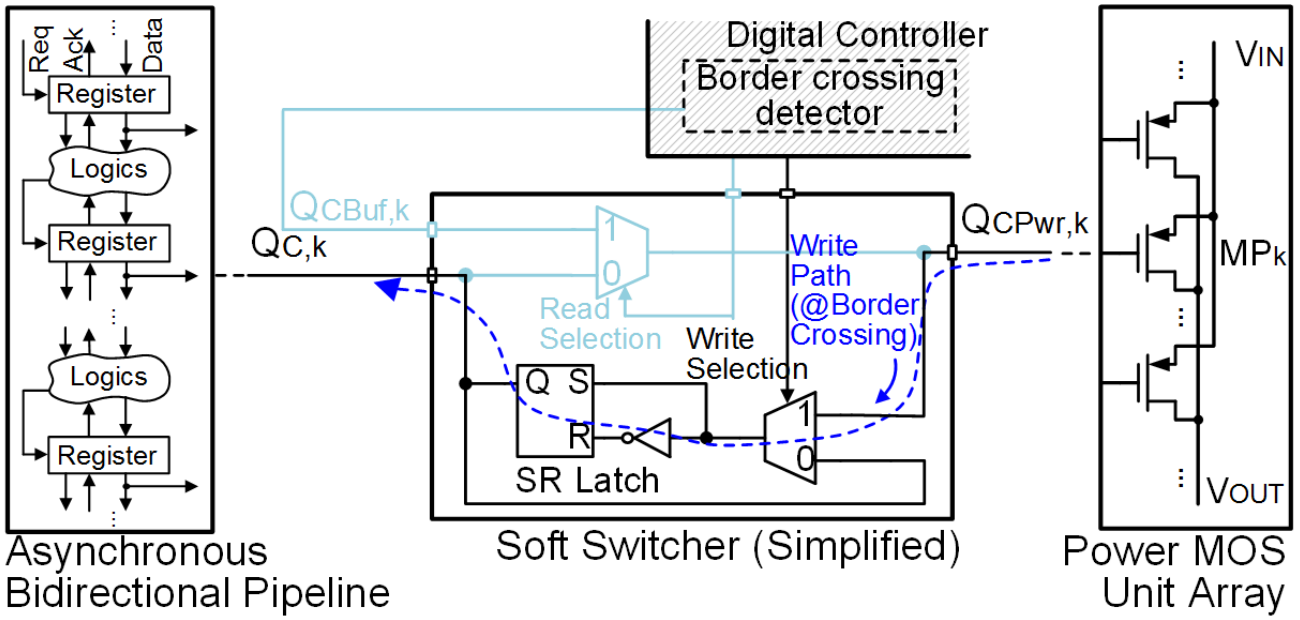
Soft multi-step switching: Read path

- Scenario: Two-step coarse/fine voltage regulation
  - *N* columns: each column with *M* bits
- Bi-directional multi-step switching
  - **Read path @ border crossing detected**
  - Adaptively change $Q_{CPwr,k}$ w/o coarse-mode comparison



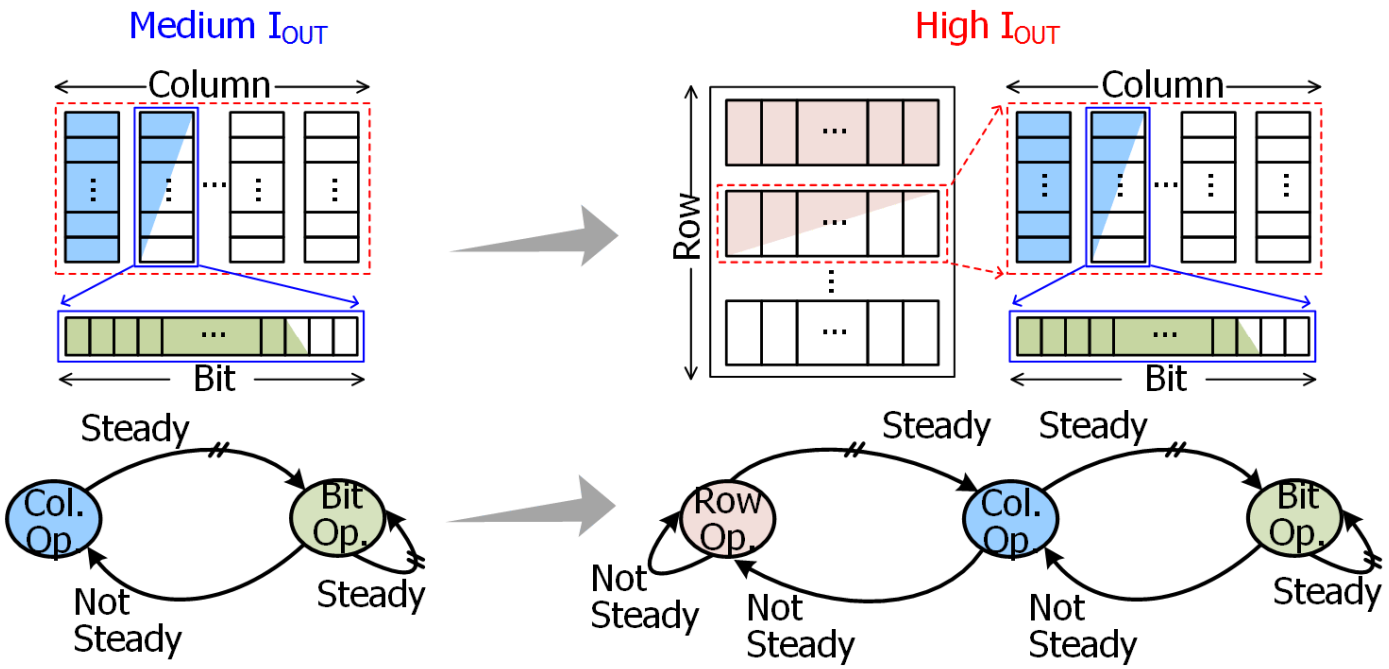
Soft multi-step switching: Write path

- Scenario: Two-step coarse/fine voltage regulation
  - *N* columns: each column with *M* bits
- Bi-directional multi-step switching
  - **Write path @ border crossing detected**
  - Update $Q_{CPwr,k}$ back to register before coarse-mode starts



Stronger power strength: to Row-Column-Bit

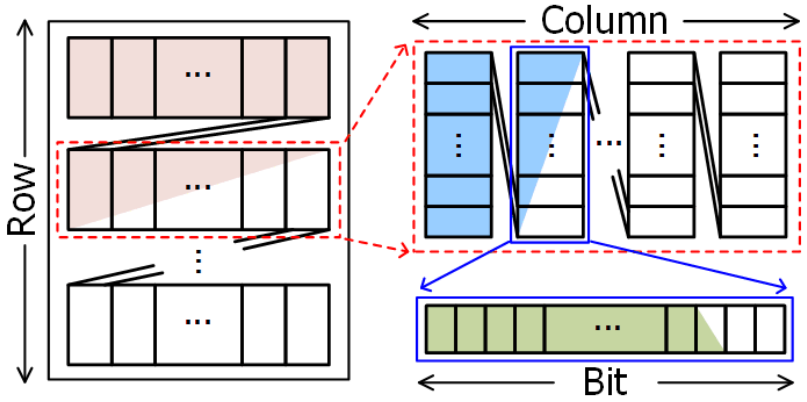
- Larger output current delivery
  - *Row* virtually defined as grouped *Columns*
- Coarse/fine mode conducted by Finite State Machine (FSM)
  - Transient enhancer path + Resolution enhancer path

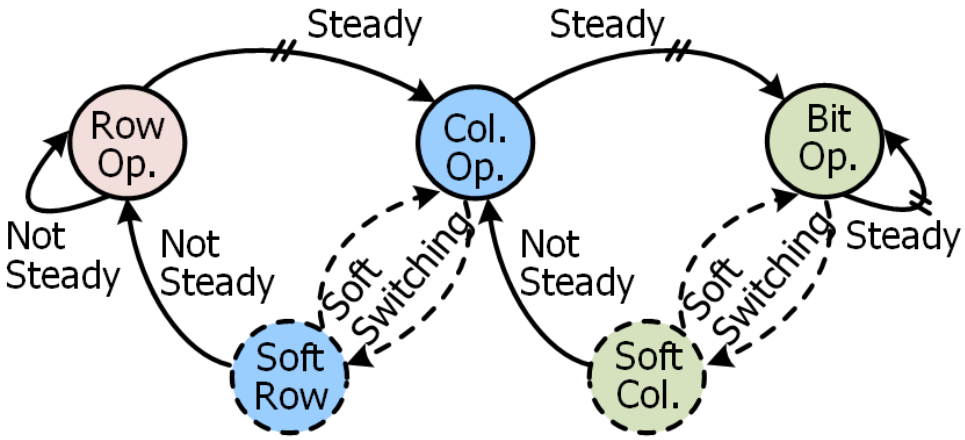


[F. Yang, ESSCIRC 2015]

Finite state machine (FSM) with adaptive timing

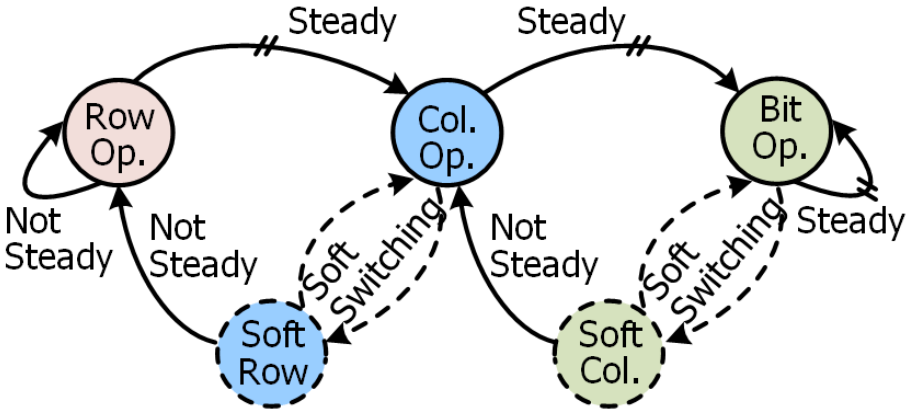
- Multi-step switching with richer FSM
  - Column operation <- Soft Column <- -> Bit operation
  - Row operation <- Soft Row <- -> Column operation
- FSM state transition: internal counter

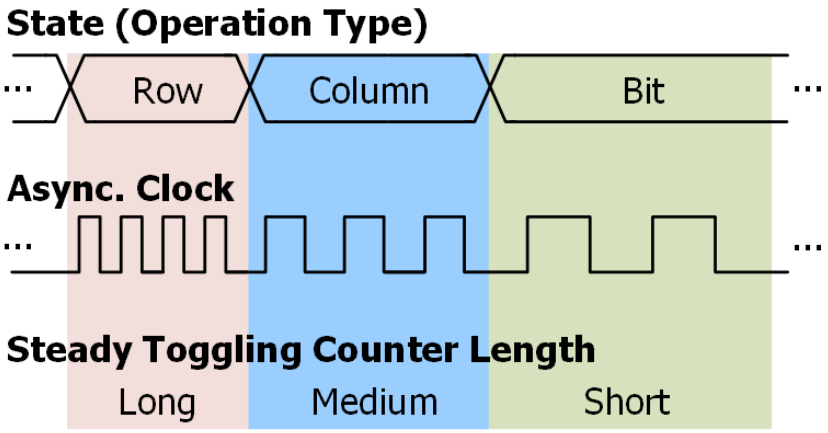




Finite state machine (FSM) with adaptive timing

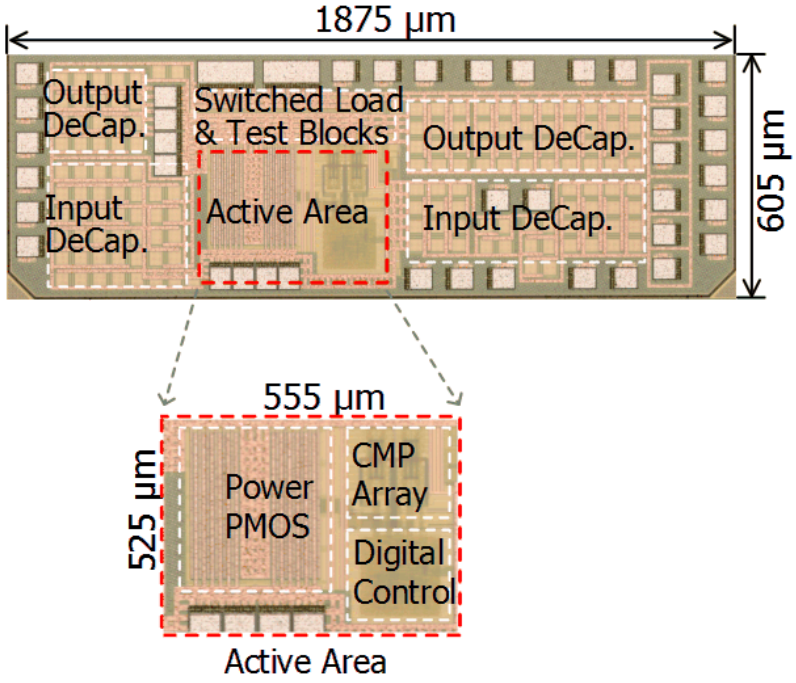
- FSM state transition: internal counter
- **Adaptive timing in FSM**
  - Power strength consideration
  - Long (Row) /Medium (Column) /Short (Bit)





The chip and Specification

Chip micrograph



CMP: comparator
DeCap: decoupling capacitor

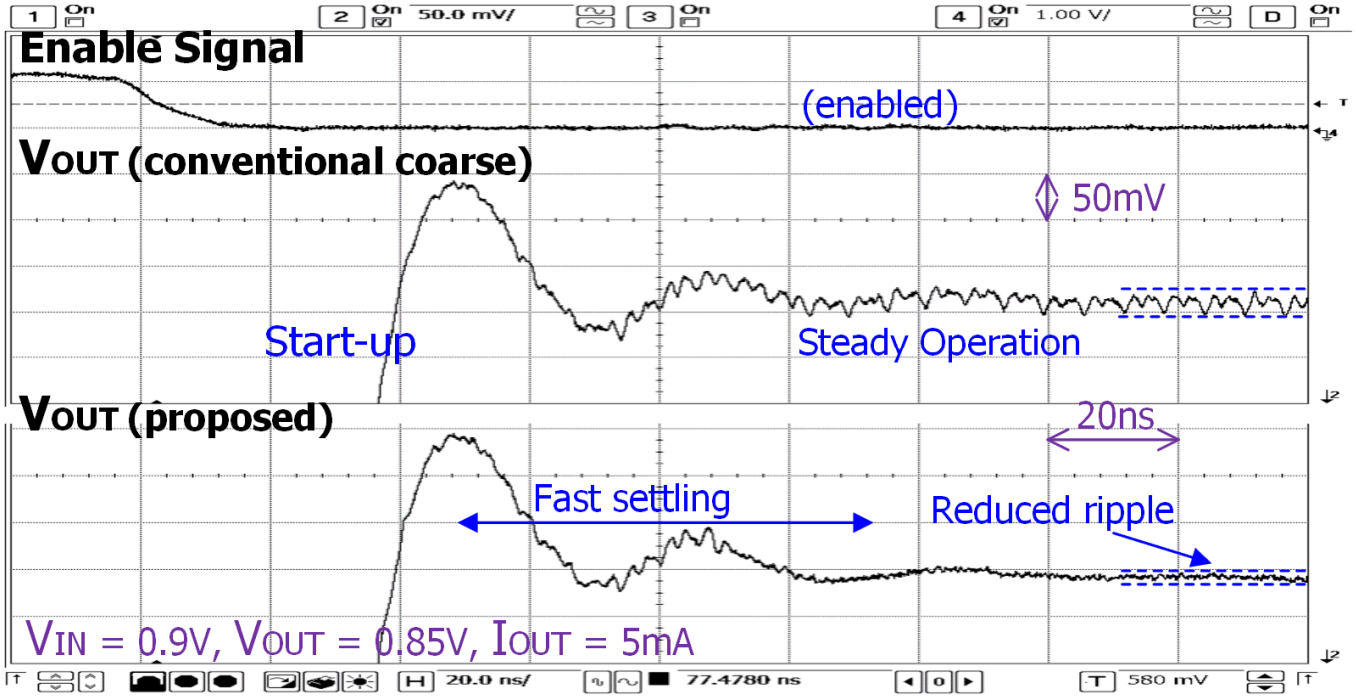
Specification

Technology	65nm LL
Input voltage	0.6 – 1.0V
Output voltage	0.55 – 0.95V
Maximum output current	500mA
Load capacitor	2nF
Control method	Asynchronous digital control
Equiv. binary bits	9.5 *
Quiescent current	350µA
Transient edge	2ns

* 9.5 is calculated from: ~ $\log_2(6\times8\times16)$

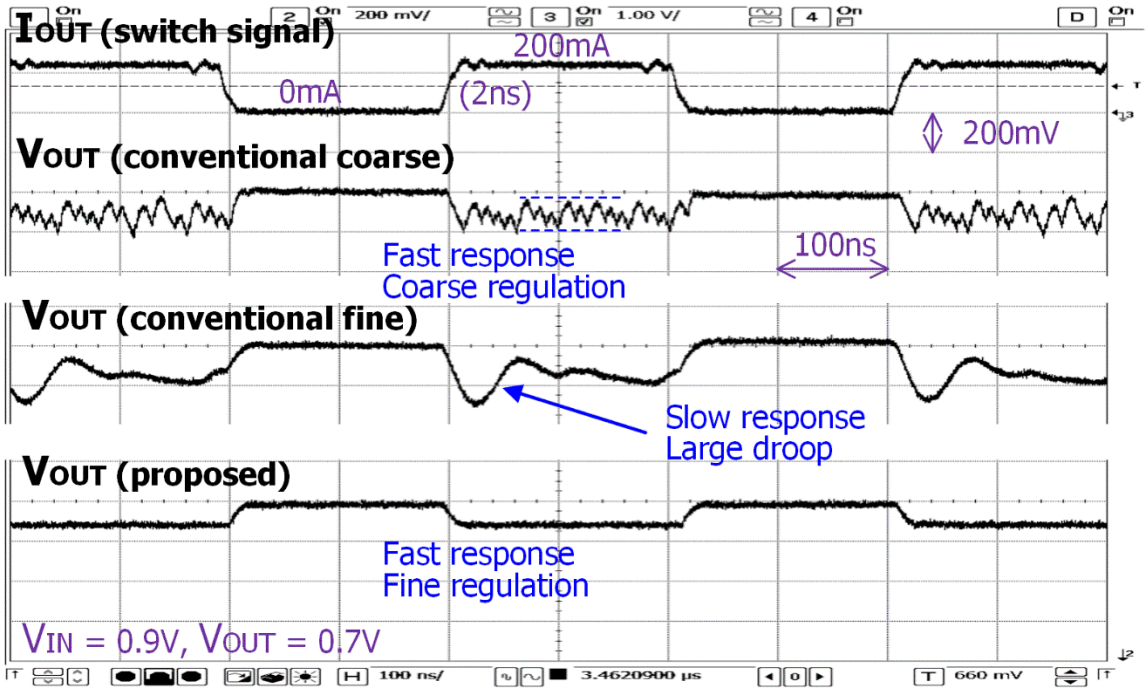
Measured start-up and steady operation

- Comparison with:
  - Conventional design with coarse-grained regulation
- Comparable fast settling time



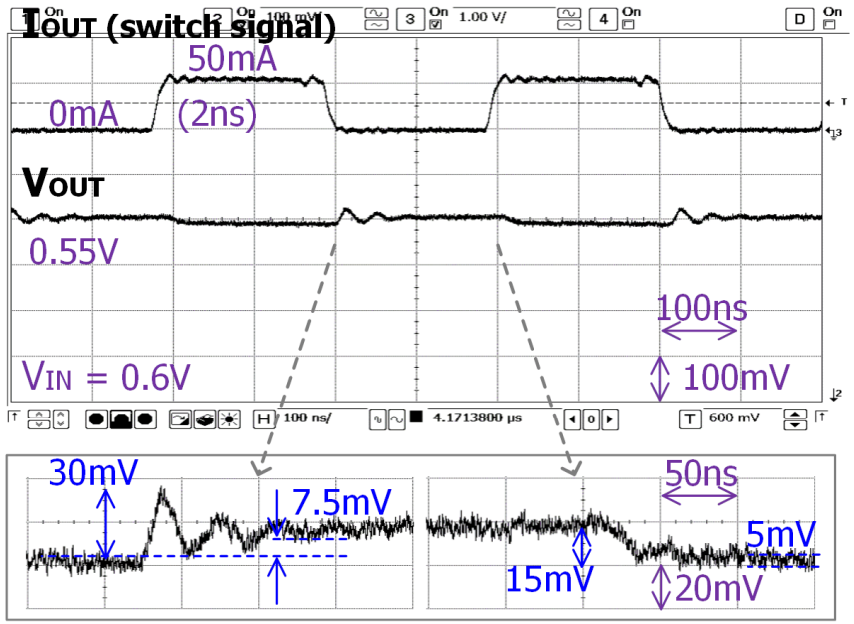
Measured load transient response (for comparison)

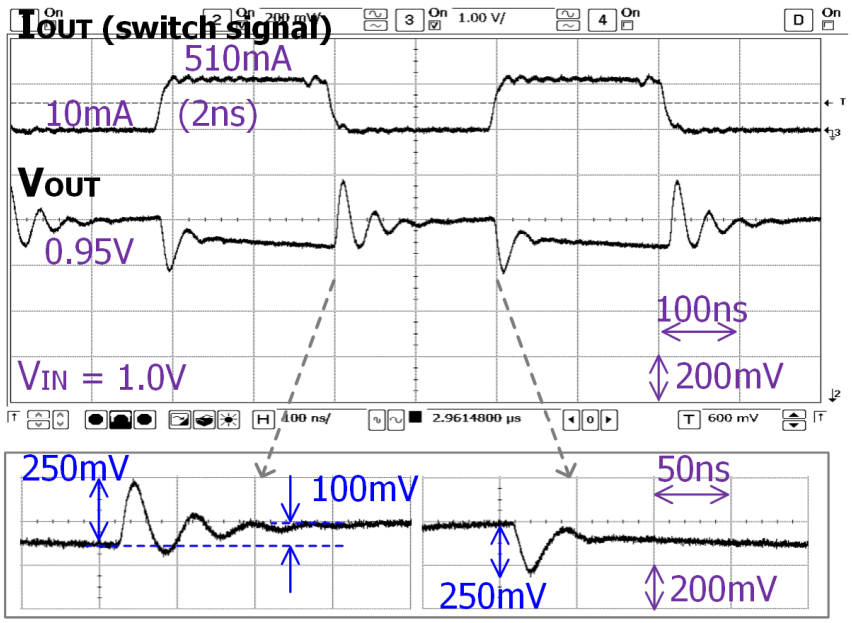
- Comparison with:
  - Conventional design: coarse-grained or fine-grained only
- Faster transient response and smaller droop
- Finely regulated output voltage



Measured Transient Response

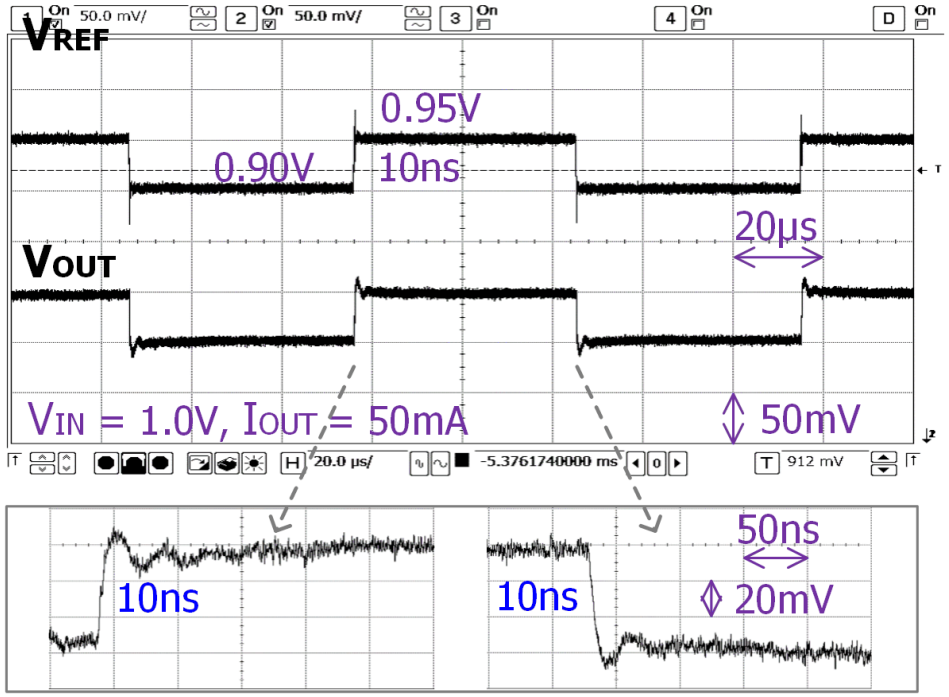
- Measured load transient response
  - 50mA on-chip current step
  - 500mA on-chip current step





Measured Transient Response

- Measured reference tracking
  - 0.9 - 0.95V (50mV) reference voltage step at V_{IN} = 1.0V, I_{OUT} = 50mA



Comparison of Performance

Publication	Hazucha JSSC'07	Okuma CICC'10	Onouchi ASSCC'11	Oh TVLSI'14	Gangopadhyay JSSC'14	Nasir ISSCC'15	This Work
Technology	90nm	65nm	40nm	110nm	32nm	130nm	65nm
V_{IN} (V)	2.4	0.5	1.34	0.6-1.2	0.7-1.0	0.5-1.2	0.6-1.0
V_{OUT} (V)	1.2	0.45	1.20	0.5-0.9	0.5-0.9	0.45-1.14	0.55-0.95
$I_{OUT,MAX}$ (mA)	1000	0.2	250	80	5	4.6	500
Equiv. bin-bits	4	8	5.8(2)	9	N/A	7	9.5
C_{OUT} (nF)	2.4	100	N/A	1	0.1	1	2
Edge Δt (ns)	0.288	N/A	5	25000(2)	10(2)	N/A	2(1)
ΔI_{MAX} (mA)	1000	0.2	114	80	0.8	1.4(2)	500
ΔV_{OUT} (mV)	120	40	50	53	150	90(2)	250
Load reg. (mV/mA)	N/A	0.65	N/A	0.30	N/A	10	0.15-0.2
Quiescent I_Q (μA)	25700	2.7 (1MHz)	10000 (1GHz)	32	92	24-221	350
FOM_T (ps)(3)	7.4	270000	6140.4	0.27	1150	8571(2)	0.7
FOM_V (V)(4)	0.0031	N/A	0.076	1.840	0.599(2)	N/A	0.0012

(1) Simulated data (2) Estimated from figure or content

(3) $FOM_T = (C_{OUT} \times \Delta V_{OUT} \times I_Q)/\Delta I^2_{MAX}$ or $T_R \times I_Q/\Delta I_{MAX}$ (if T_R given)

(4) $FOM_V = K(\Delta V_{OUT} \times I_Q)/\Delta I_{MAX}$

Conclusions

- **Proposed a 65-nm asynchronous digital LDO**
  - Nanoseconds' transient response over 500 milli-amperes
  - 9.5b fine resolution, 0.6V to 1V input voltage range
  - improved load regulation
- **Featured soft coarse/fine multi-step switching**
  - Adaptive to wide load: multiple-step-size power stage
  - Asynchronous pipeline with adaptive size and timing
  - Soft switching between coarse/fine modes
- **State-of-the-art Figure of Merits (FOM_T and FOM_V)**

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