# A Near-Optimum 13.56 MHz Active Rectifier with Circuit-Delay Real-Time Calibrations for High-Current Biomedical Implants

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# Outline

- **Background Introduction**
  - Wireless Power Transfer (WPT) System and Rectifier
  - Circuit-delay issues and impacts
  - Literature Review
- **Proposed Active Rectifier**
  - Design Overview
  - Real-Time Calibrations
- **Simulation and Measurement Results**
- **Conclusions**

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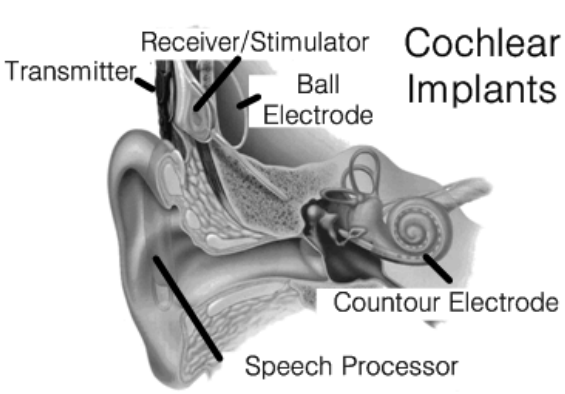
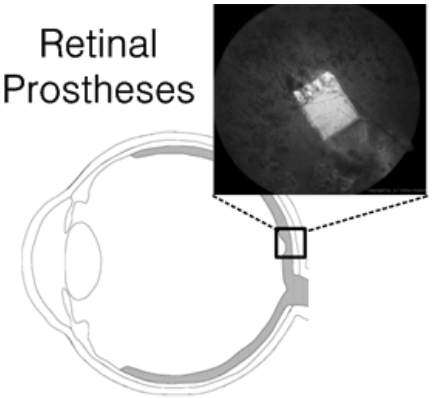
# Background Introduction



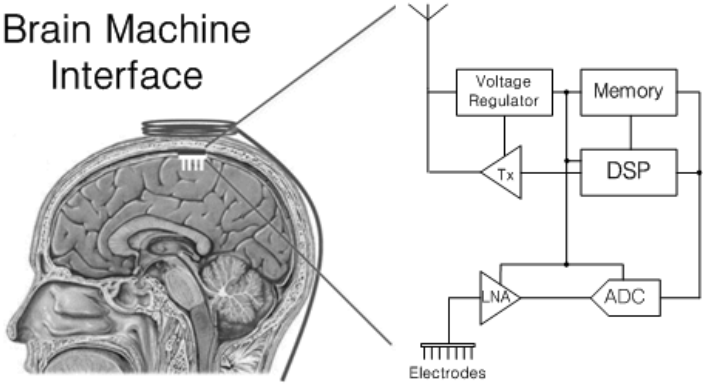

Cochlear Implants

Bhatti JSSC'06



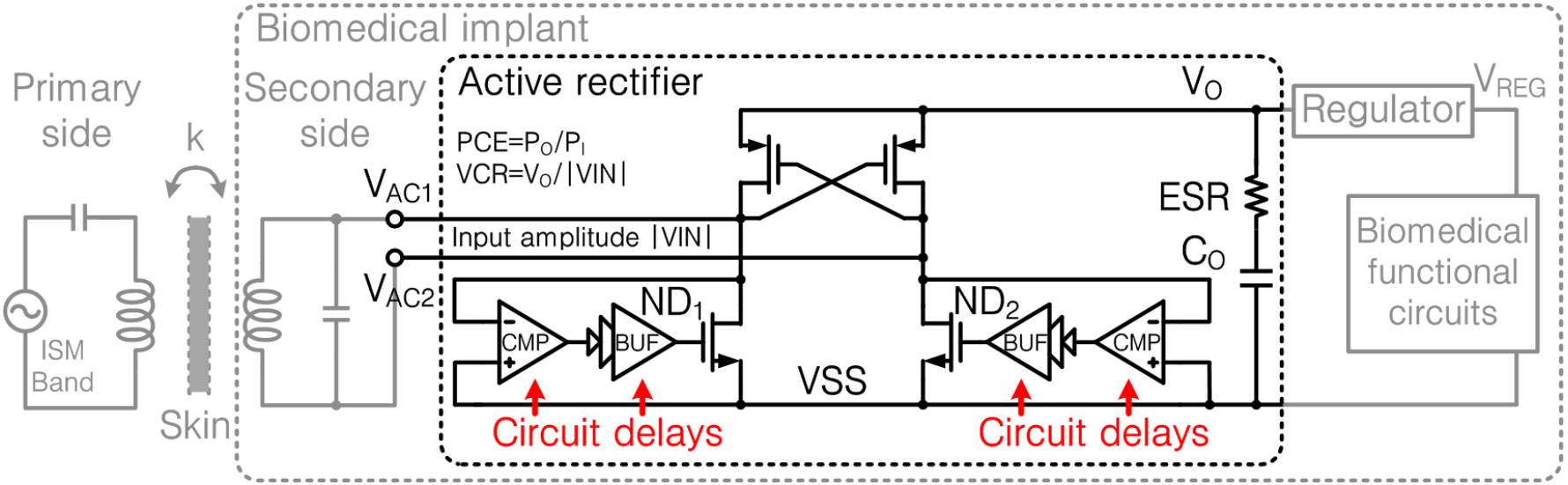
Retinal Prostheses

Graf JSSC'06



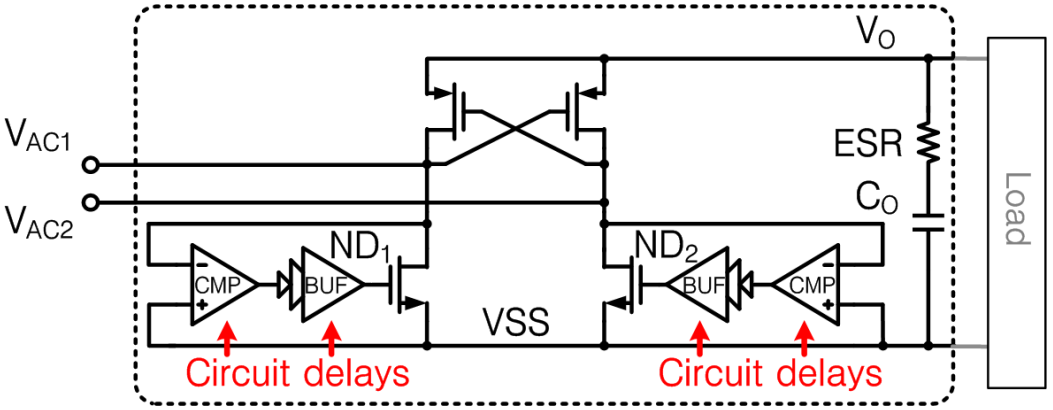

Chen and Rabaey, UC Berkely

WPT systems for biomedical applications



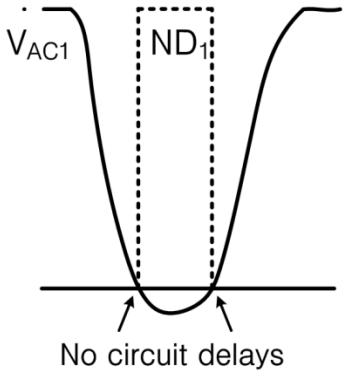

A typical WPT system for biomedical implatns

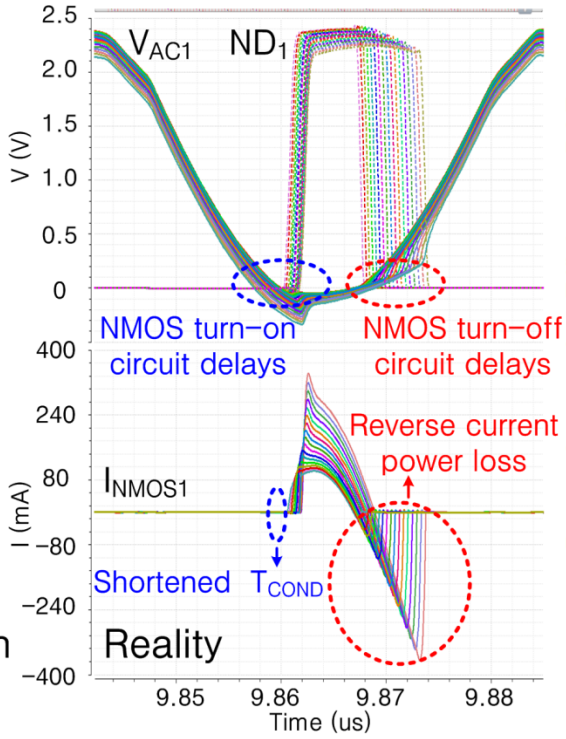
# Circuit Delays and the Impacts

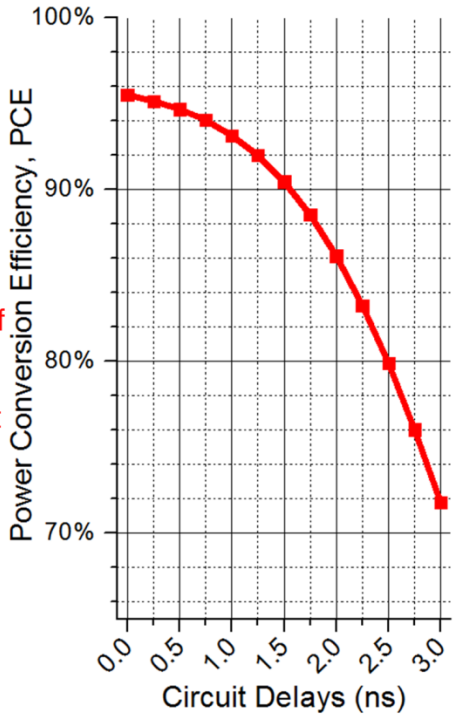



**Delay Occurs in the control path**

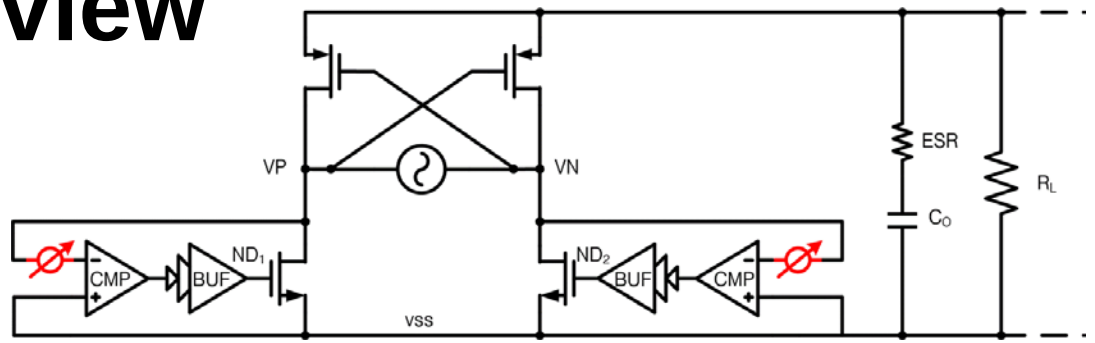
- NMOS turn-on delay
  - Conduction time shortened
- NMOS turn-off delay
  - Reverse current appears



# Literature Review




- **[Guo JSSC'09] and [Cha TCAS-II'12]**
  - fixed offset voltage, delay compensation is open-loop
  - Not accurate under different process/volt./temp. (PVT) corners
  - Only considering NMOS turn-off side
- **[Lu VLSI'11] and [Lu TBioCAS'14]**
  - prediction offsets on supply voltage, delay compensation is open-loop
  - Not accurate any more under process and temp. corners
  - Only considering NMOS turn-off side
- **[Lee TCAS-I'11]**
  - off-chip trimming (human in the delay compensation feedback loop)
  - Only considering NMOS turn-off side
- **Still no universal solution with close-loop delay compensation considering PVT variations for both NMOS on and off time.**

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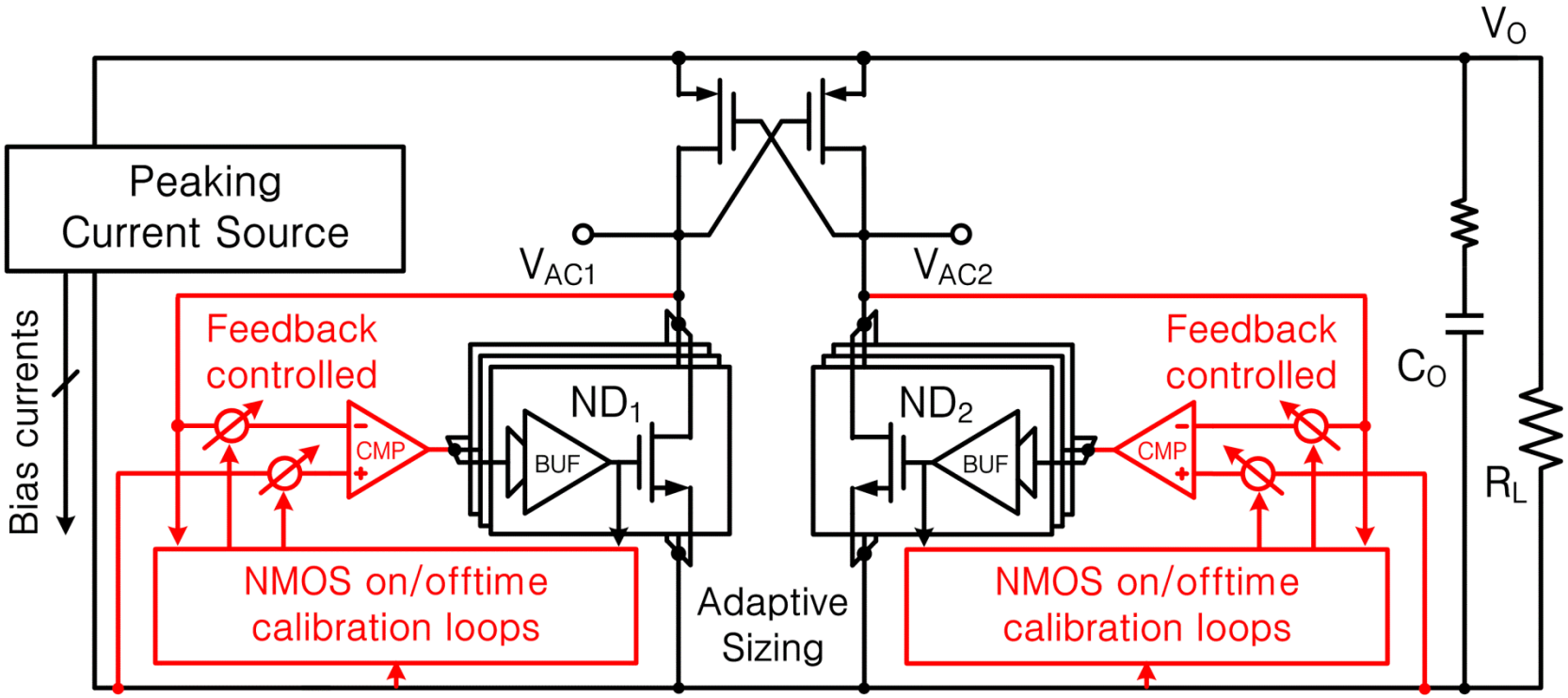
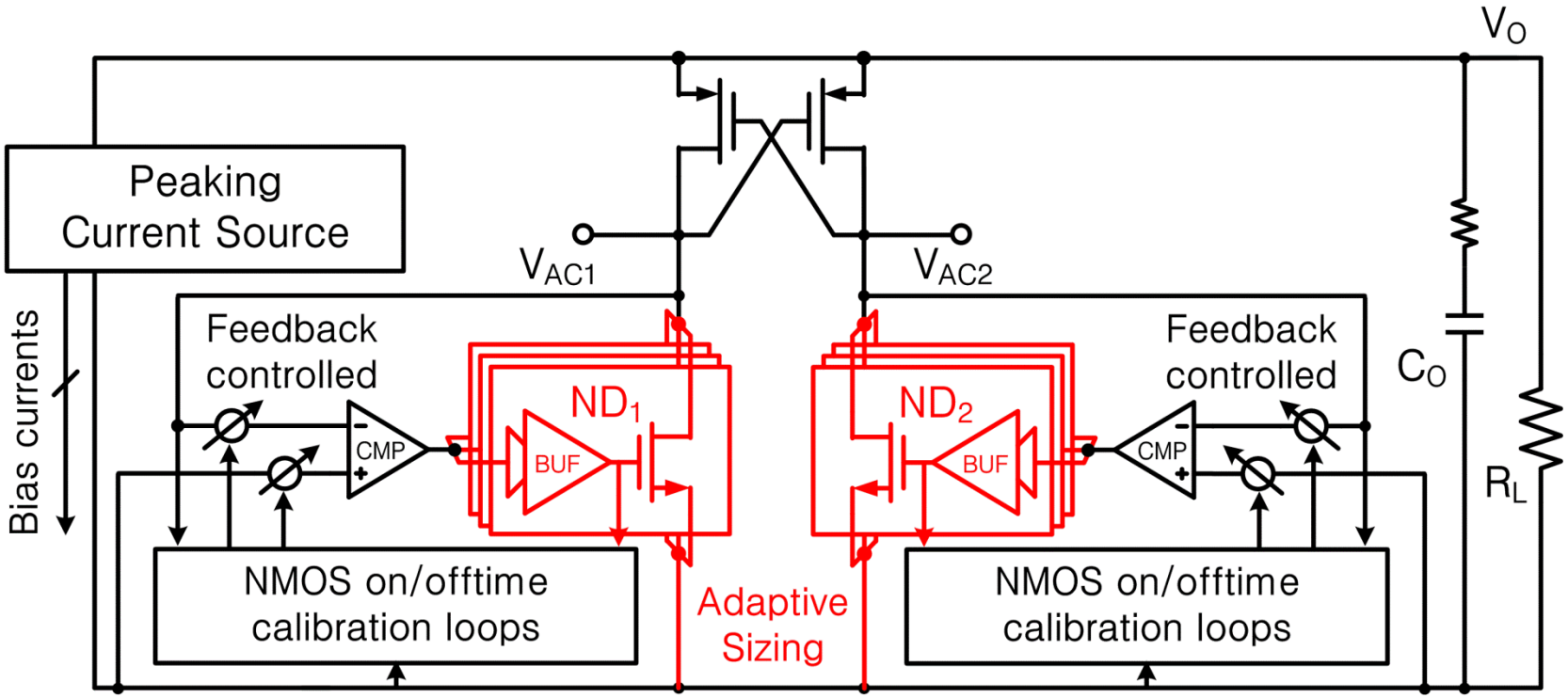
# Proposed Active Rectifier




- System block diagram
  - Real-time calibrations for NMOS on/off delays, both sides
  - Adaptive sizing according to different loading conditions

# Proposed Active Rectifier

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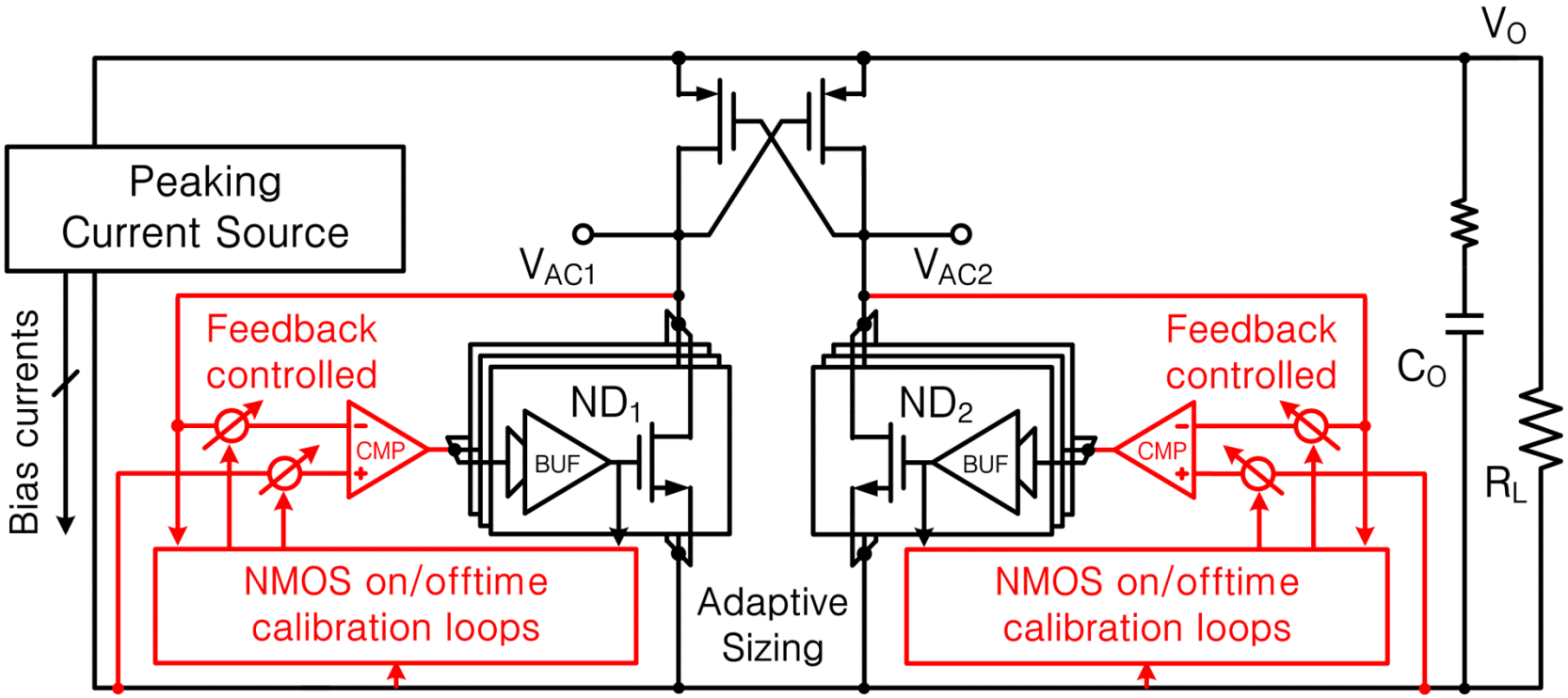
# Proposed Active Rectifier

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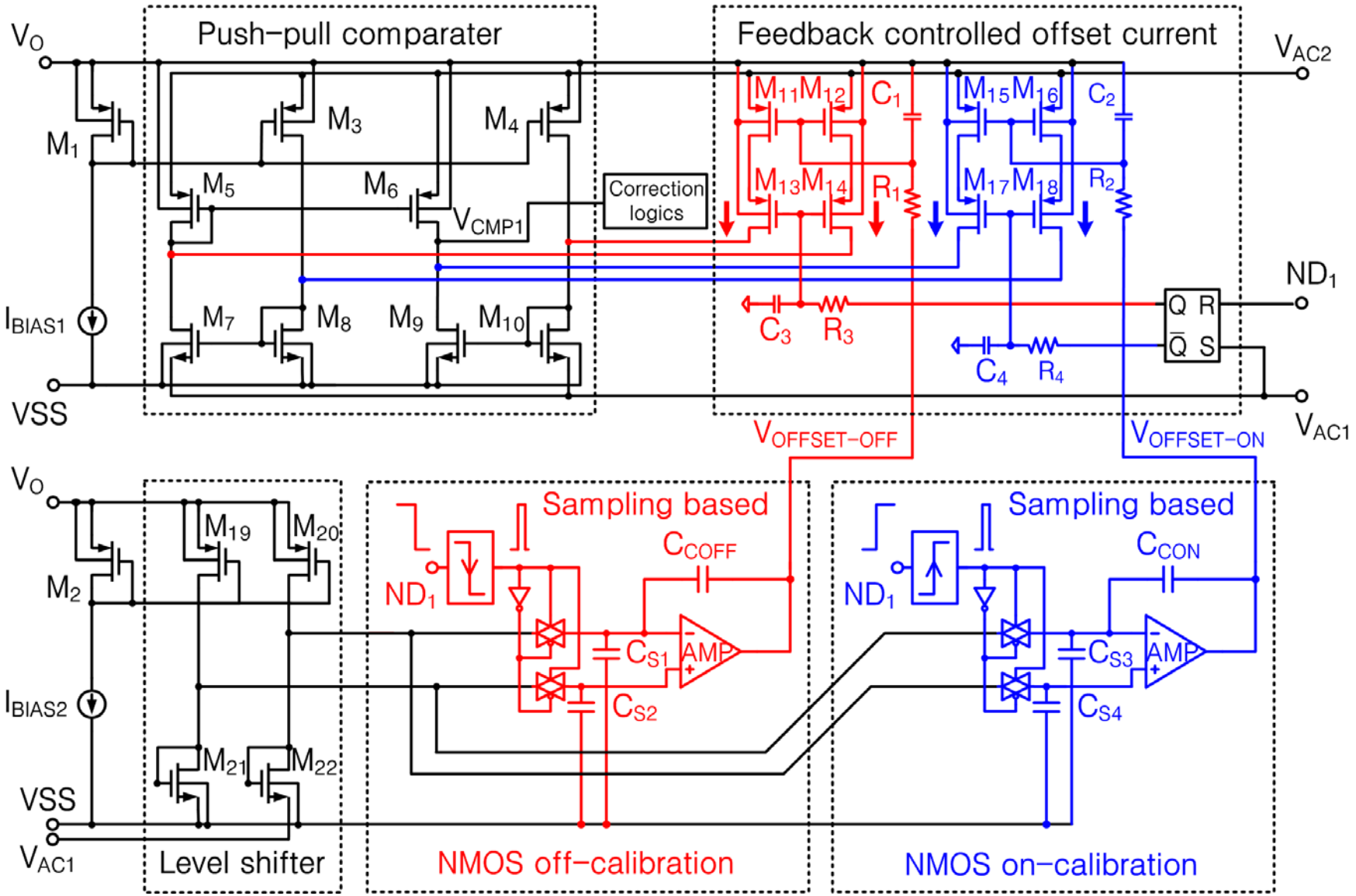
# Proposed Real-Time Calibrations



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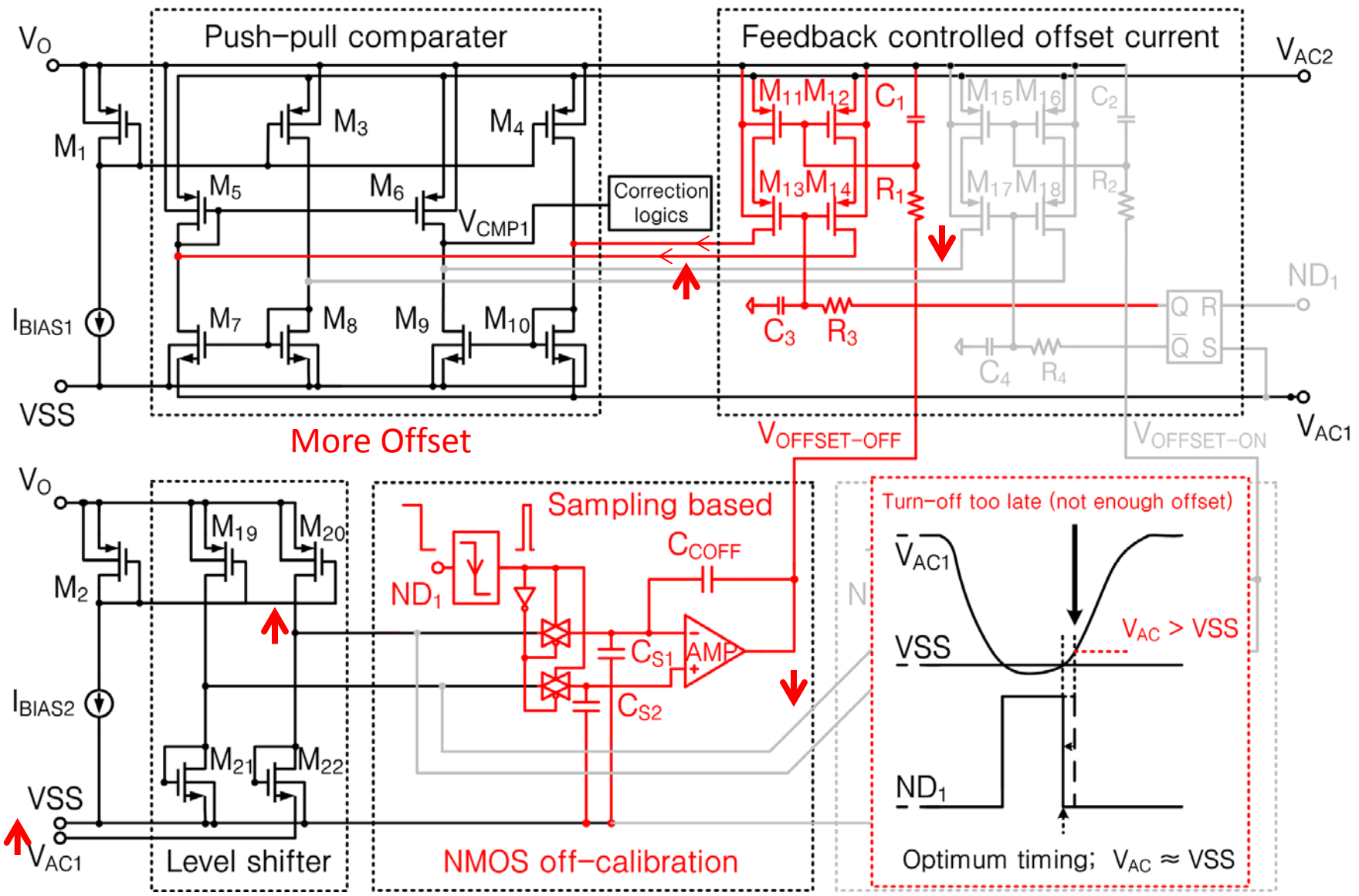

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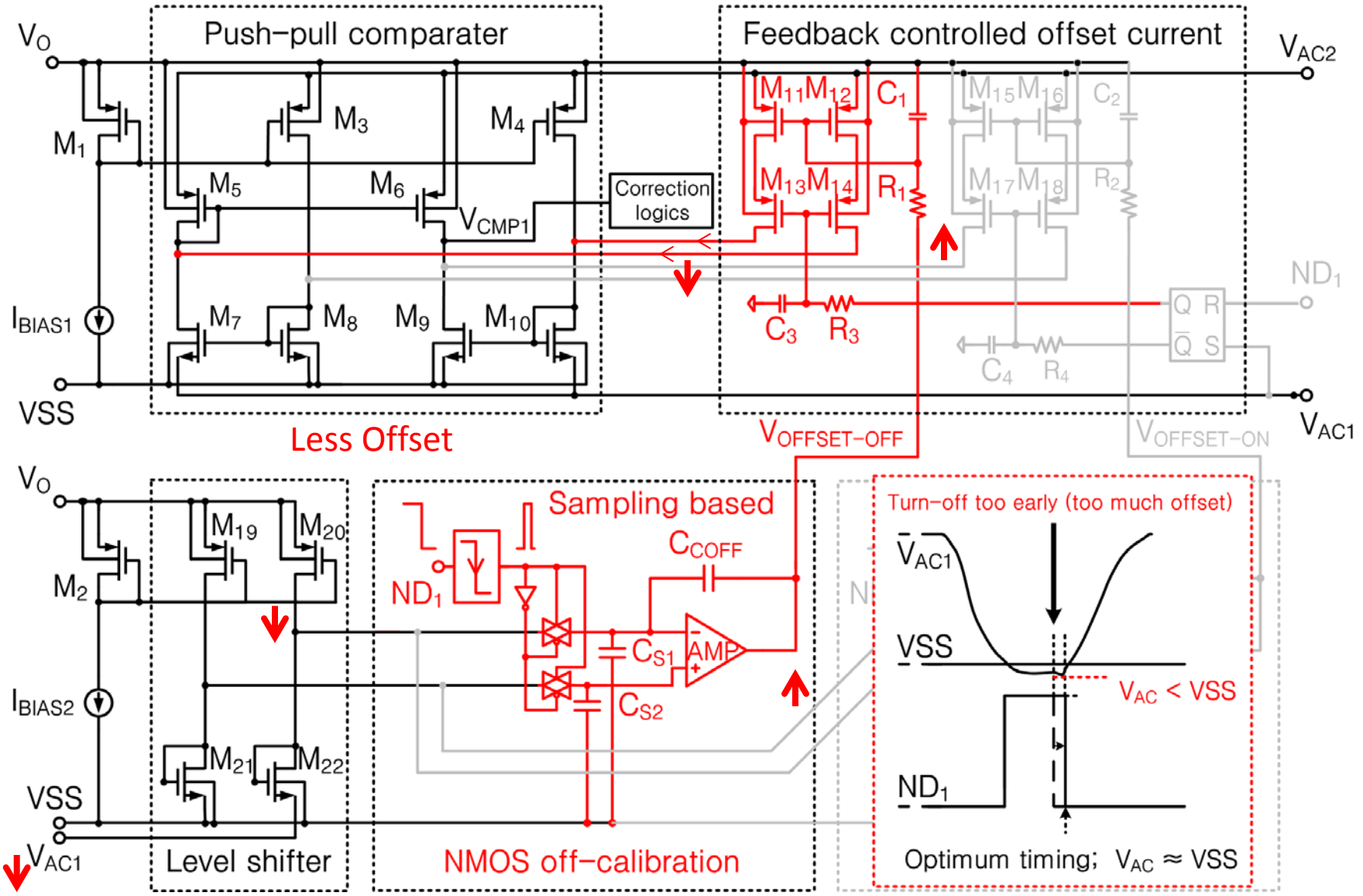
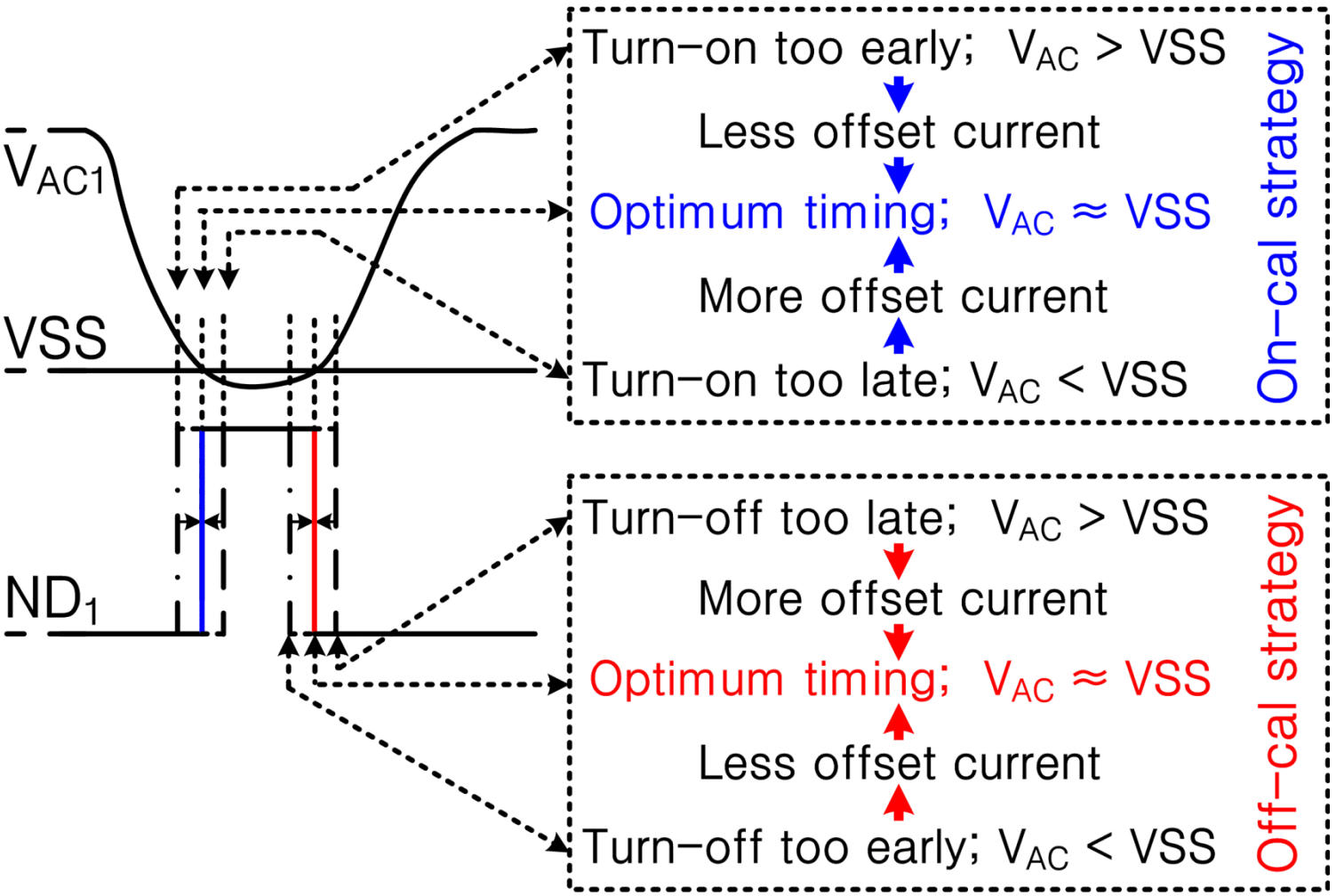


# Proposed Real-Time Calibrations




Both NMOS turn on/off time are well calibrated

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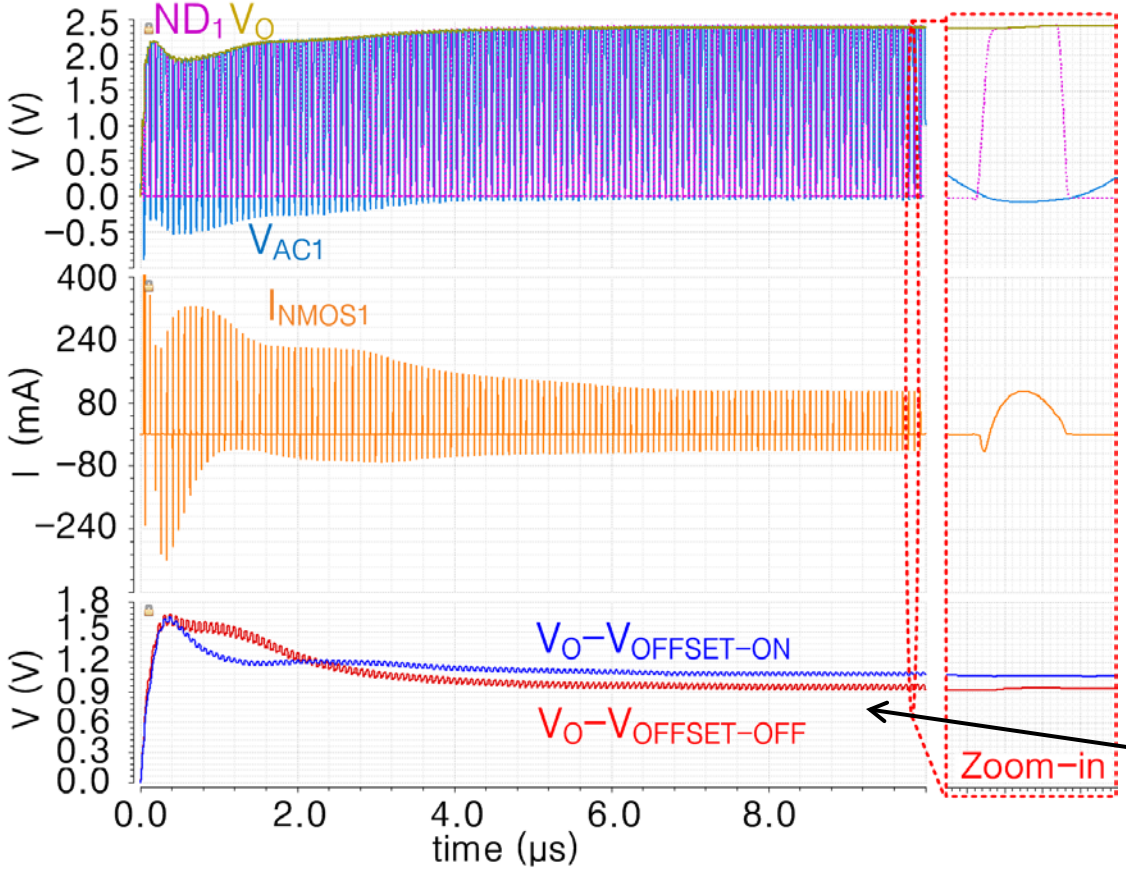
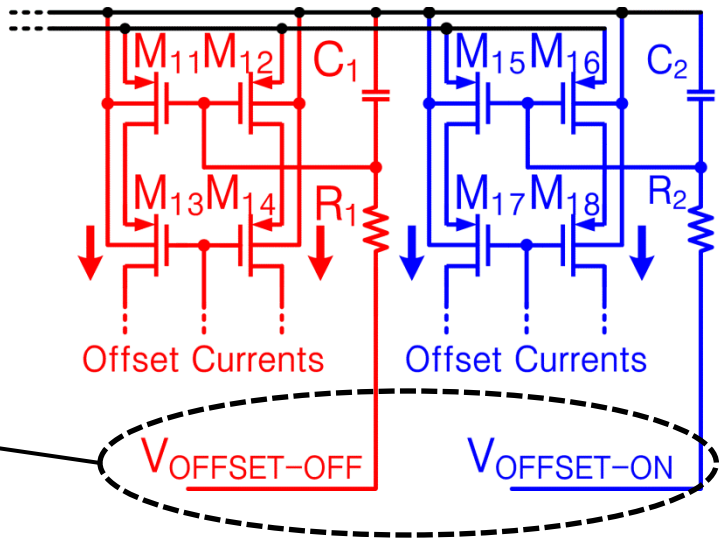
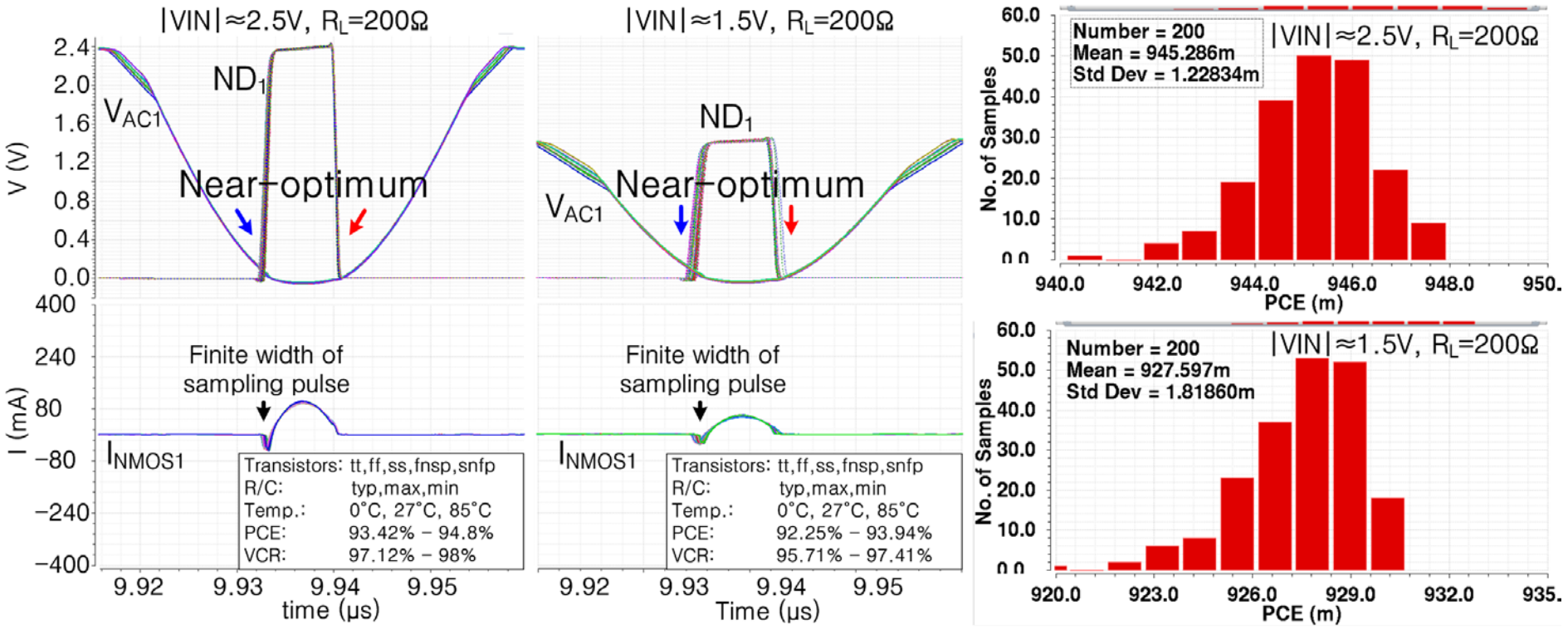
# Simulation Results




- $V_O$-$V_{OFFSET-ON}$ and $V_O$-$V_{OFFSET-OFF}$, representing the NMOS on and off offset calibration current, respectively, will be stable after a few micro-seconds.

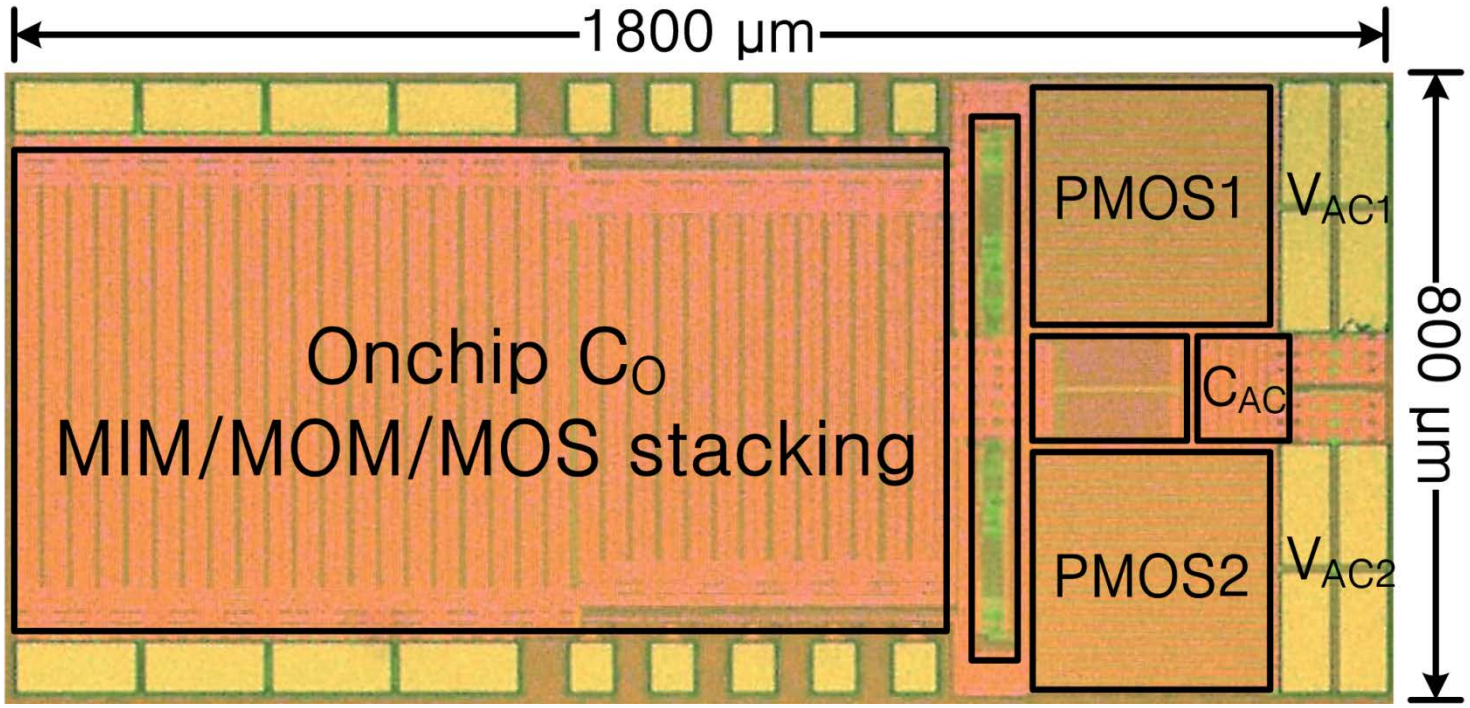
# Simulation Results




Simulations with PVT variations and Monte Carlo mismatches

Near-optimum operation achieved under various PVT conditions
Minor errors due to the finite width of sampling windows

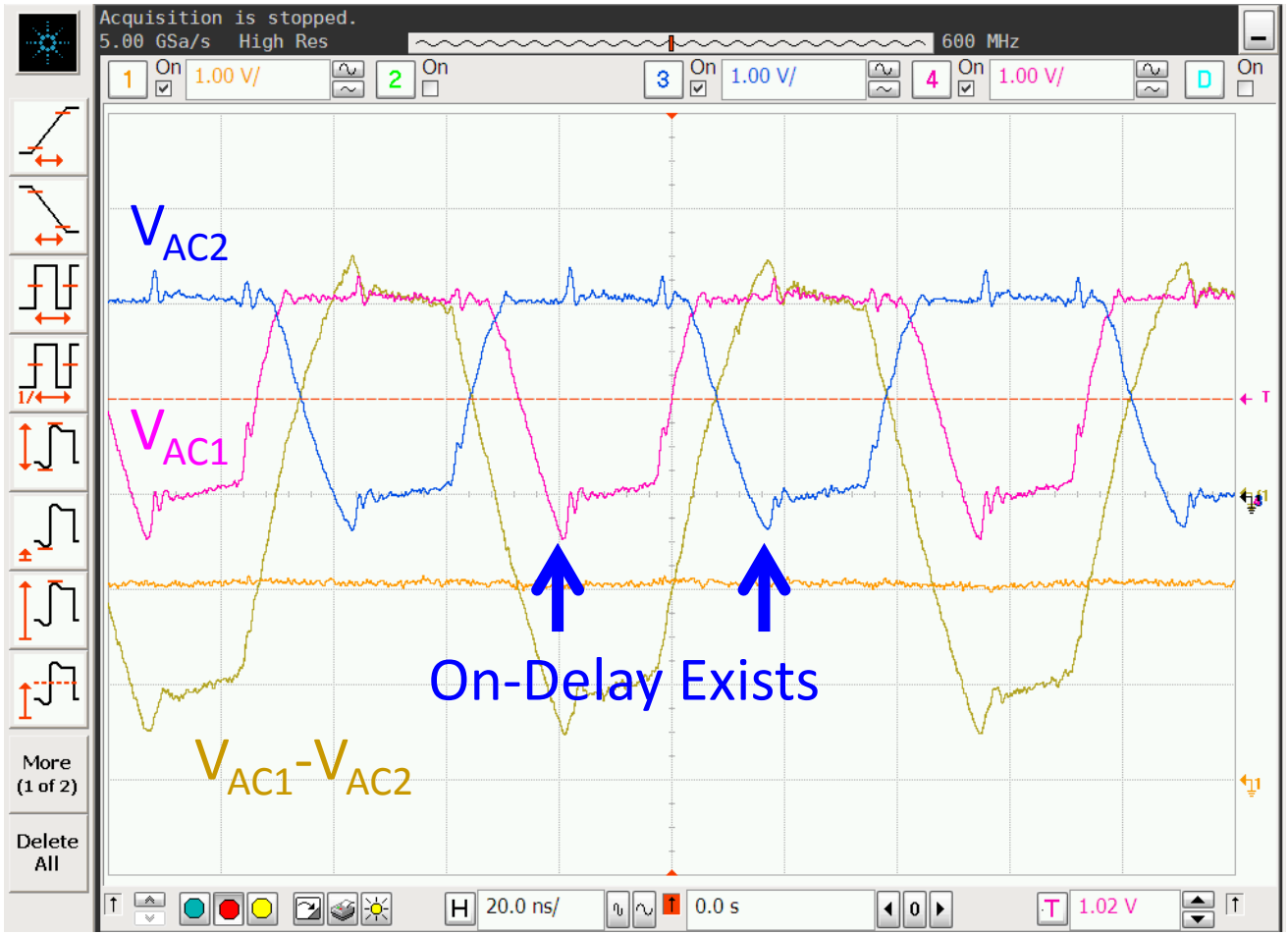
# Chip Photo




- The chip is fabricated in TSMC 65nm process, using I/O devices
- 1.44 $mm^2$ chip-area, dominated by the integrated output capacitors
- PMOS much larger than NMOS for better efficiency

  (PMOS gate-capacitances do not contribute to switching loss, BUT NMOS gate-capacitances DO [Lu TBioCAS'14])

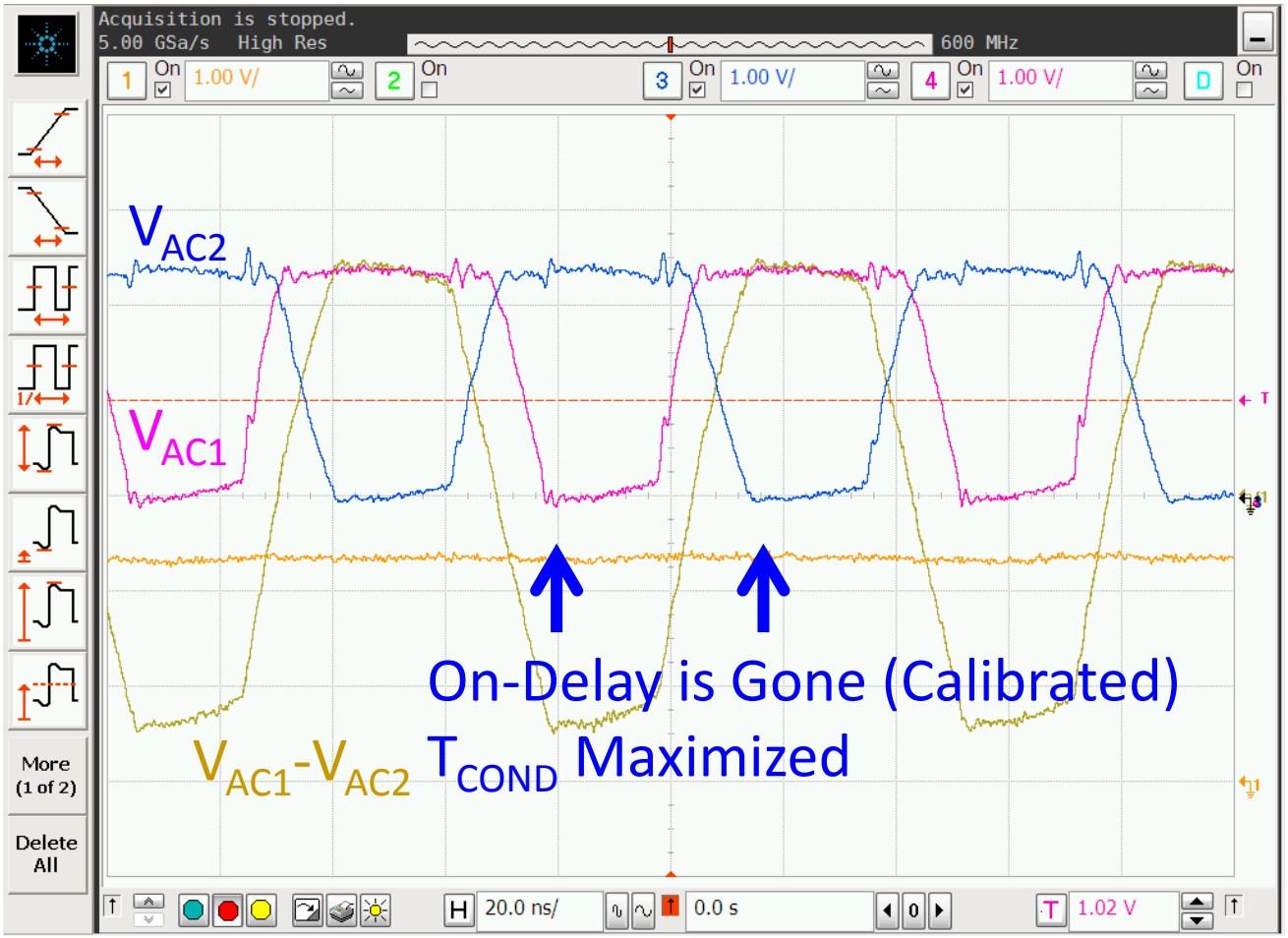
# Measured Waveforms




Measured waveforms of $V_{AC1}$, $V_{AC2}$, $V_{AC1}$-$V_{AC2}$ and $V_O$

**BEFORE** enabling ON-CAL

# Measured Waveforms

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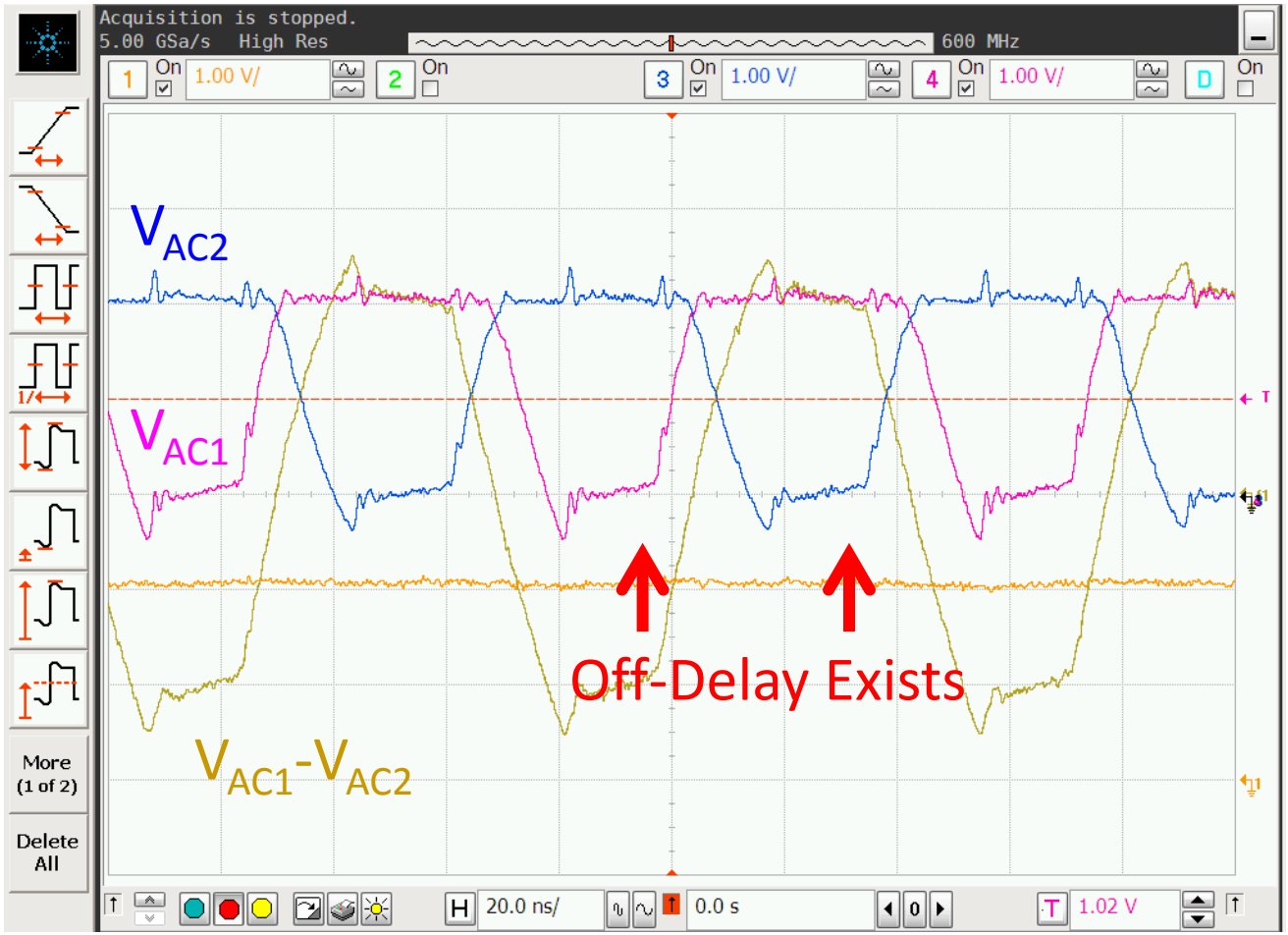


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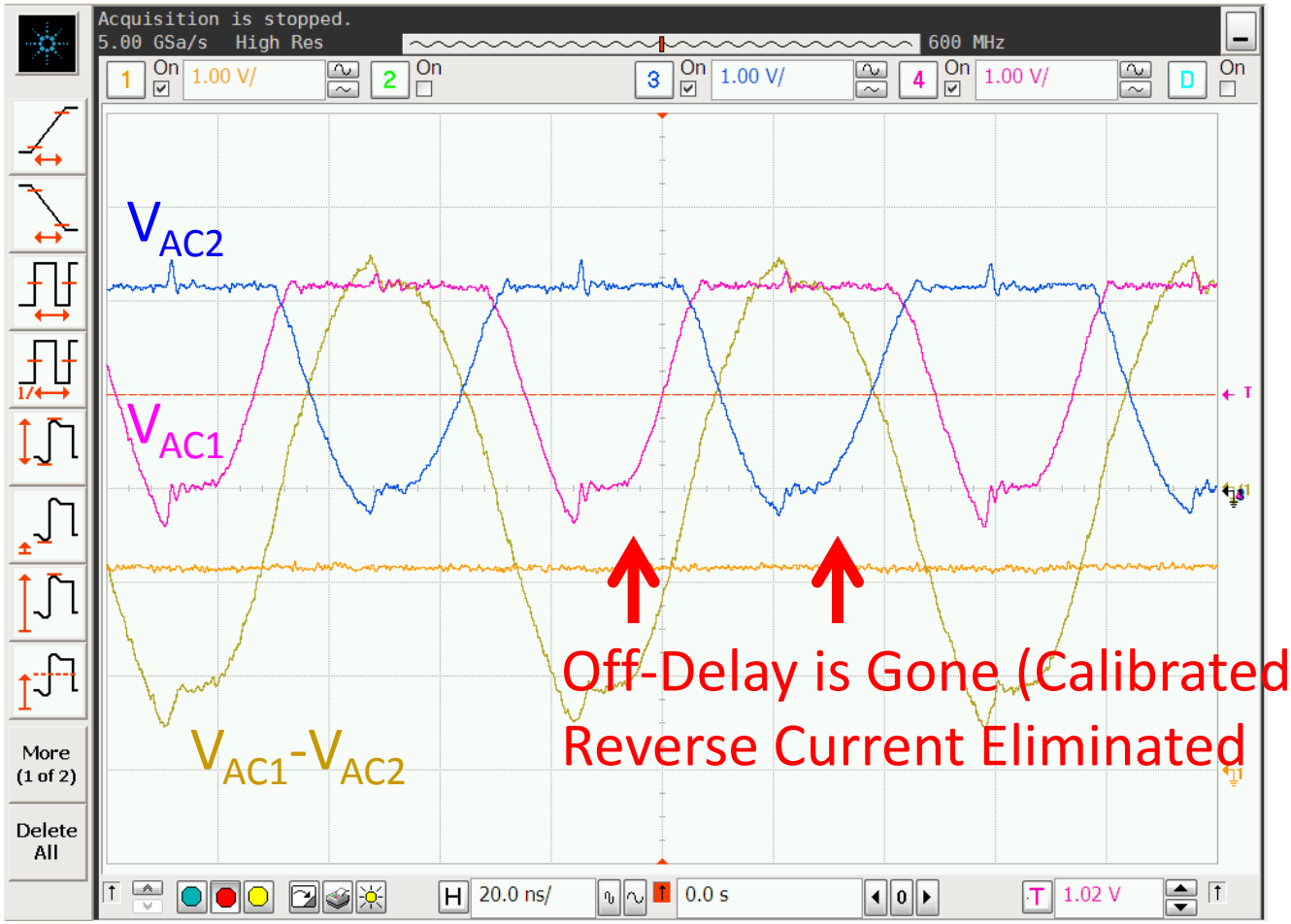


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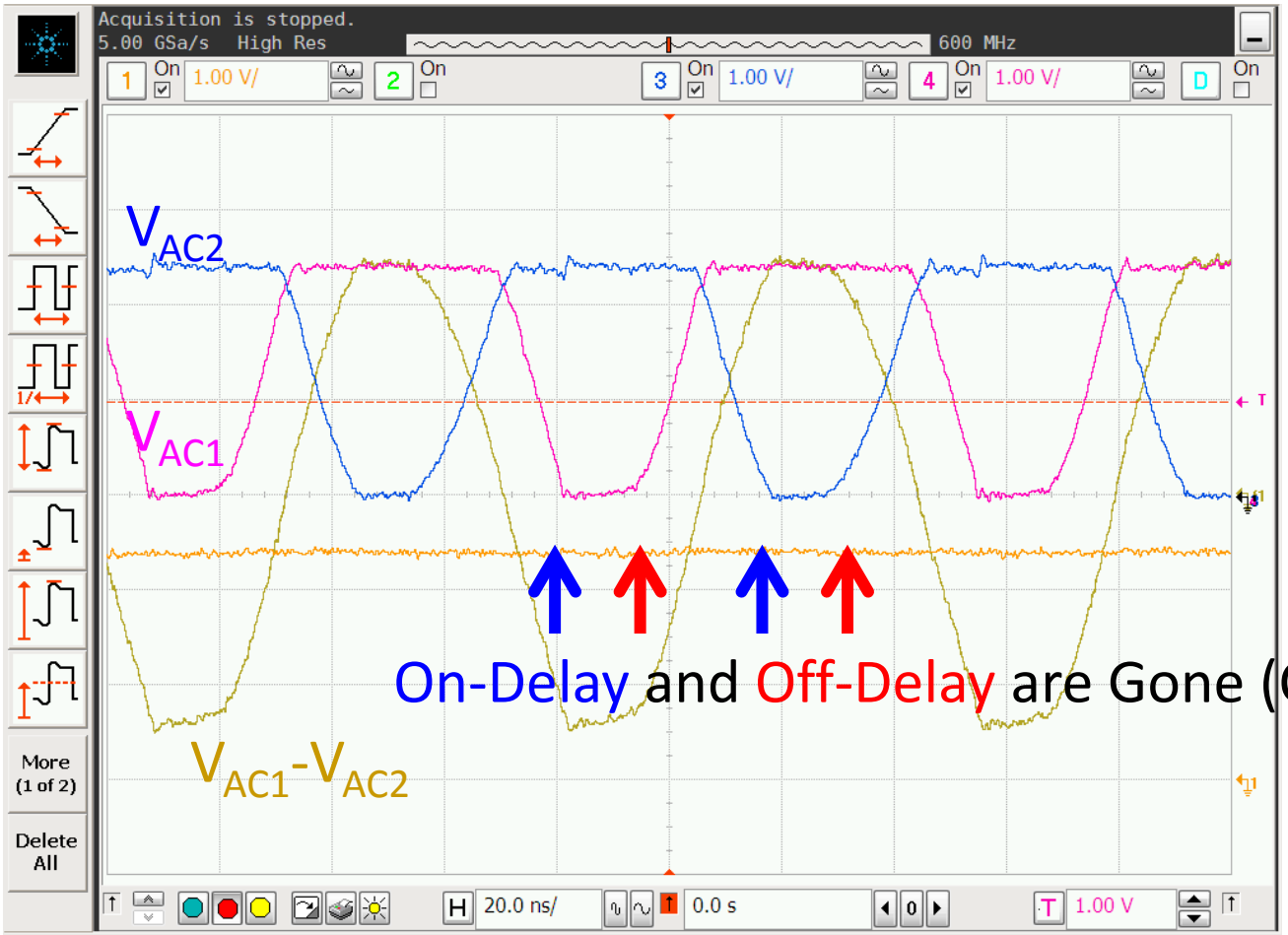
**AFTER** enabling OFF-CAL

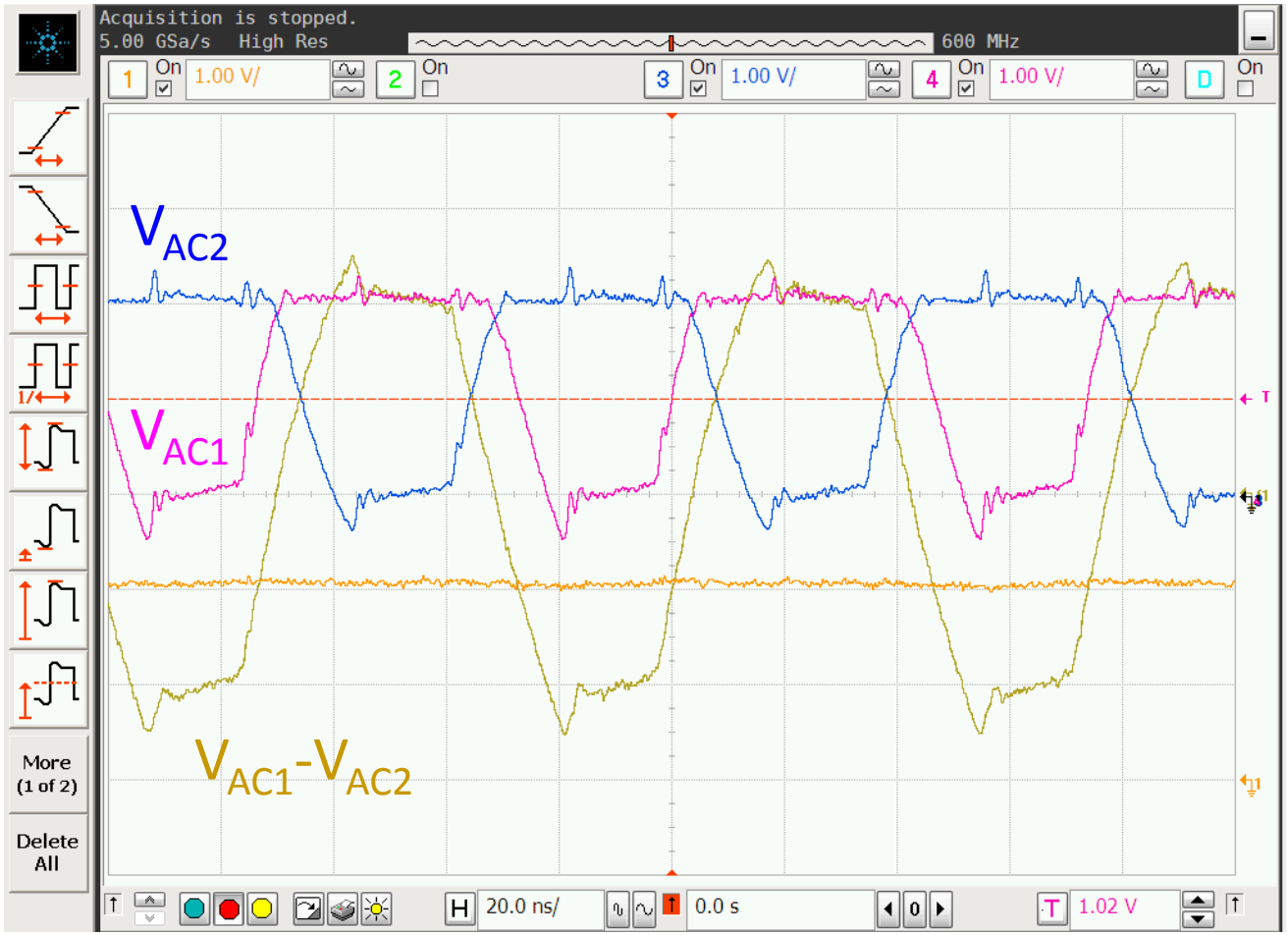
# Measured Waveforms




Measured waveforms of $V_{AC1}$, $V_{AC2}$, $V_{AC1}$-$V_{AC2}$ and $V_O$

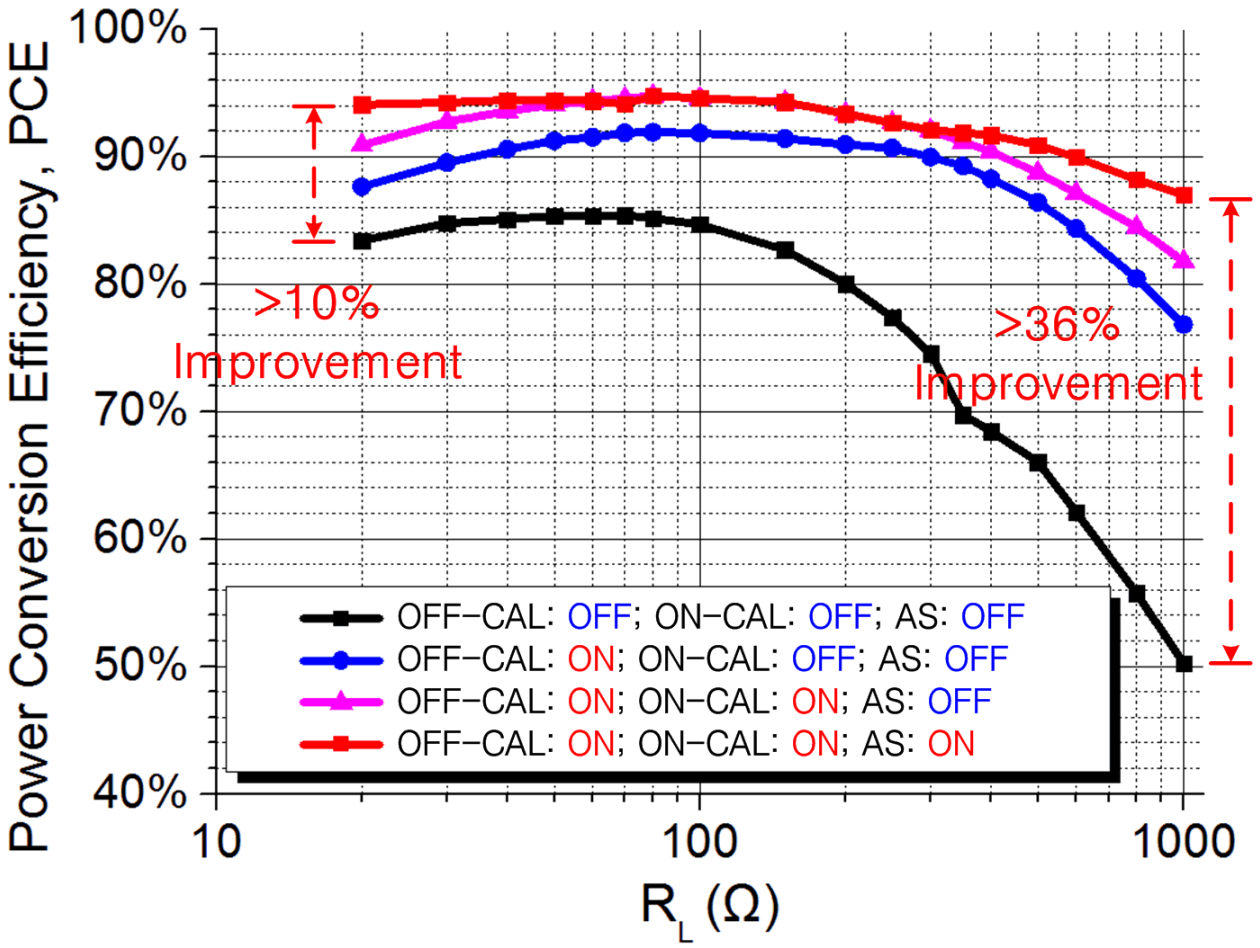
**AFTER** enabling both ON-CAL and OFF-CAL

# Measured Waveforms



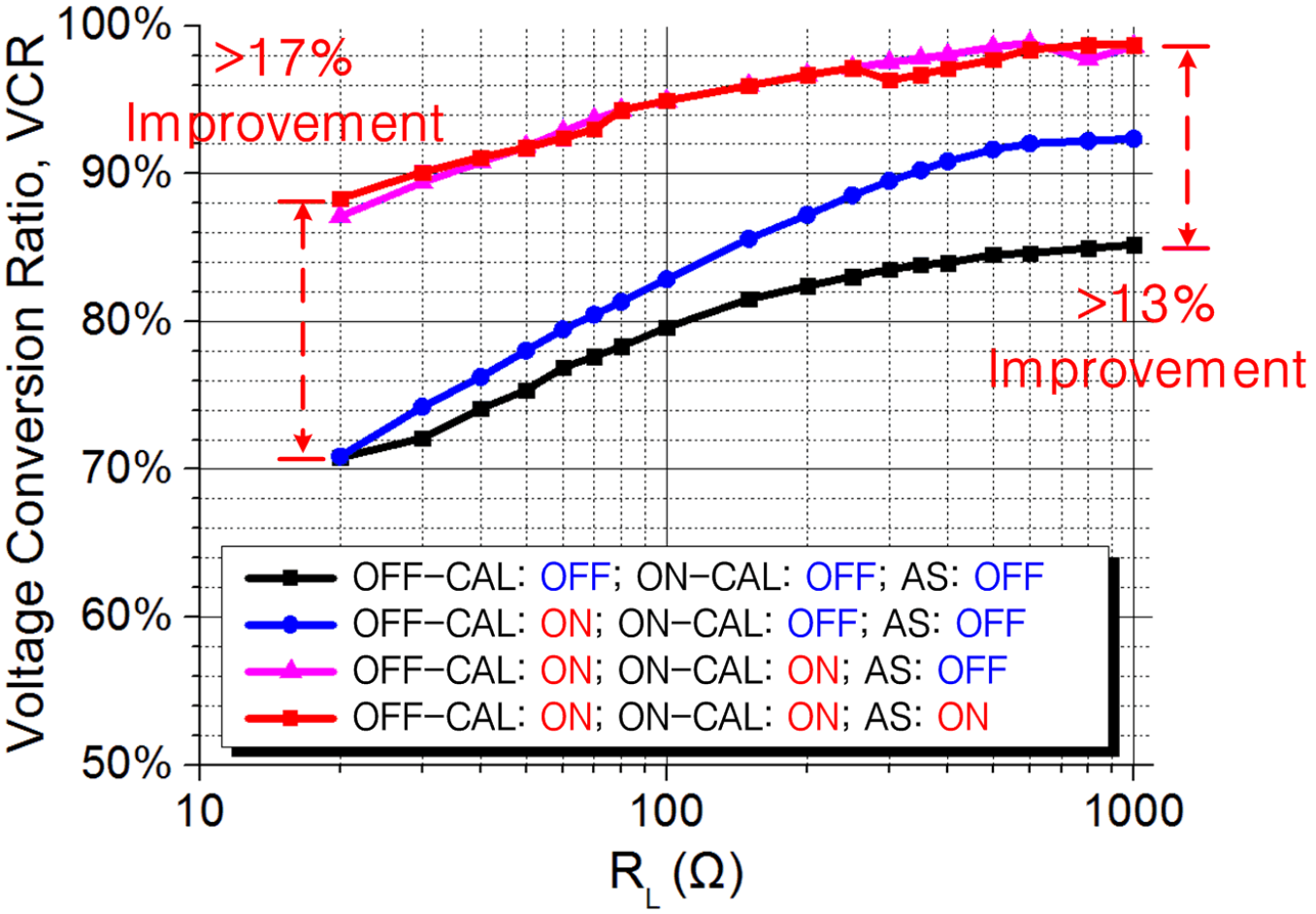

Measured waveforms of $V_{AC1}$, $V_{AC2}$, $V_{AC1}$-$V_{AC2}$ and $V_O$ **BEFORE** enabling ON-CAL or OFF-CAL

# Measured Power Conversion Efficiency



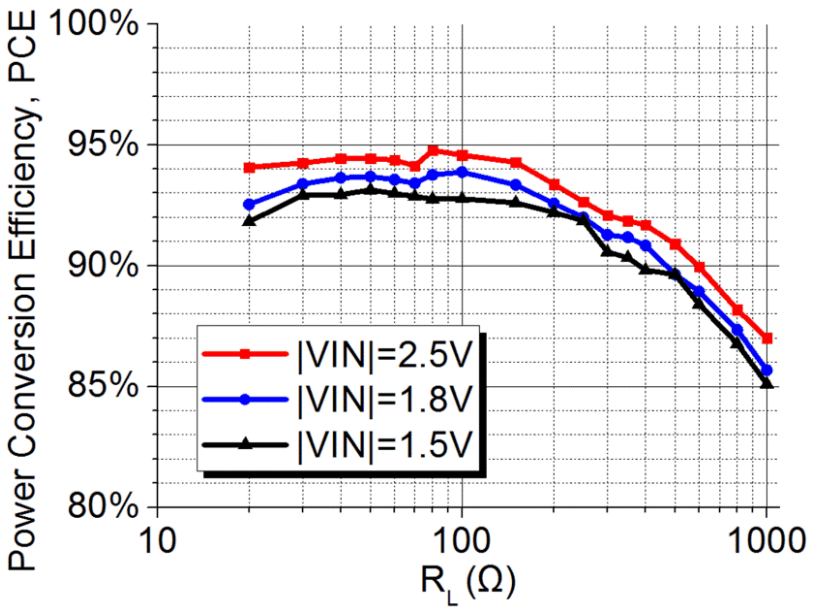

With all the functions: OFF-CAL, ON-CAL and Adaptive Sizing ON:
PCE improved >10% at heavy load and >36% at light load.
PCE >90% for a wide range, Peak approaching ~95%.

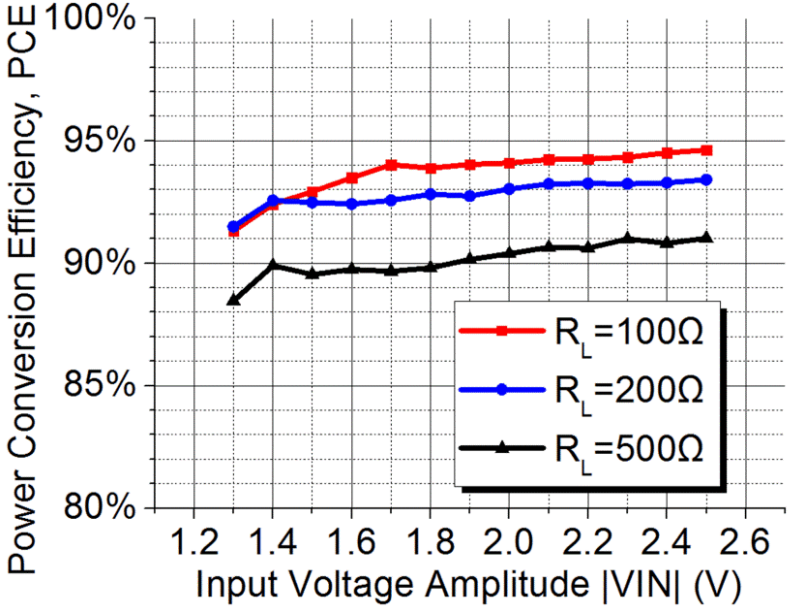
# Measured Voltage Conversion Ratio

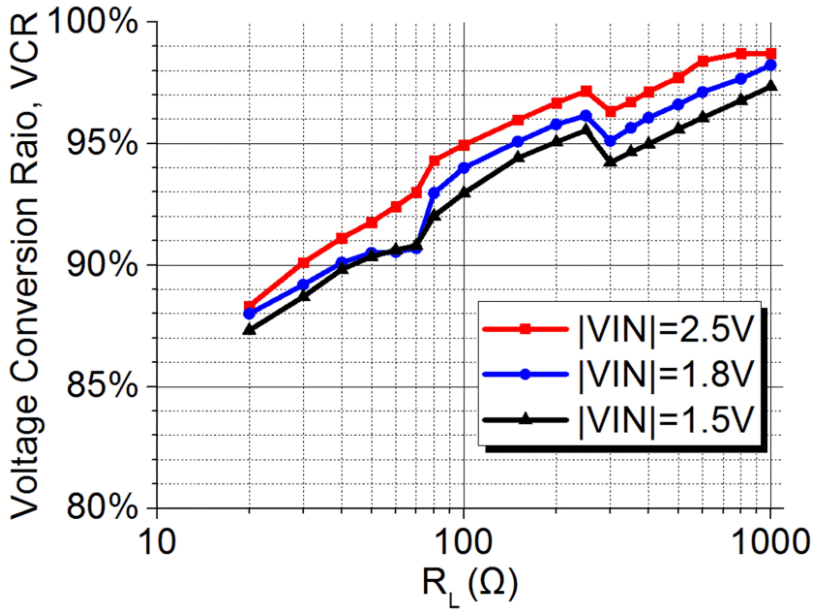


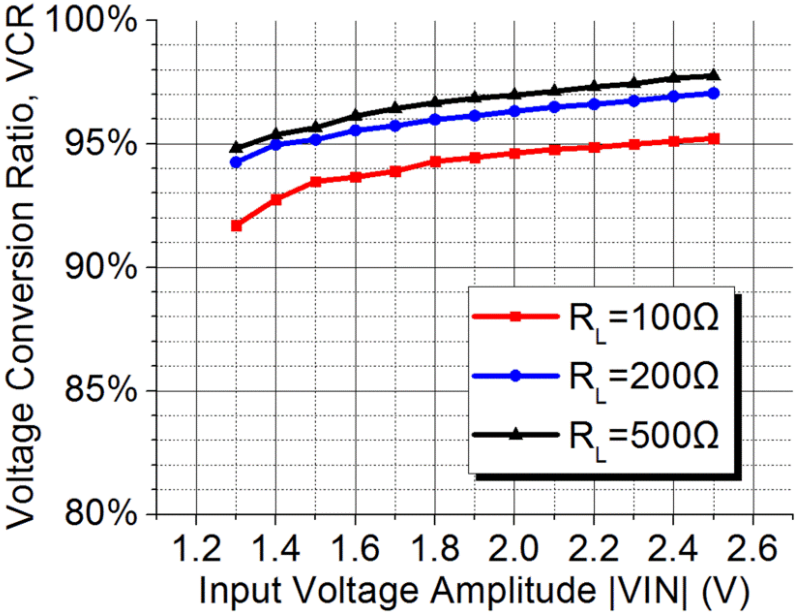

With all the functions: OFF-CAL, ON-CAL and Adaptive Sizing ON:
VCR improved >13% at heavy load and >17% at light load.
VCR >90% for a wide range, Peak approaching ~99%.

# Measured PCE and VCR



| | Lam TCAS-II 06 | Guo JSSC 09 | Lee TCAS-I 11 | Cha TCAS-II 12 | Hashemi TBCAS 12 | Chung JSSC 12 | Lu ISSCC 13† | Lu TBCAS 14 | This Work |
|---|---|---|---|---|---|---|---|---|---|
| **Tech.** | 0.35μm | 0.35μm | 0.5μm | 0.18μm | 0.18μm | 0.18μm | 0.35μm | 0.35μm | 65nm I/O Devices |
| **Area** | 0.107mm$^2$ | 1.03mm$^2$ | 0.263mm$^2$ | 0.009mm$^2$ | 0.608mm$^2$ | 0.34mm$^2$ | 1.42mm$^{2\#}$ | 0.186mm$^2$ | 1.44mm$^{2\#}$ |
| **Freq.** | 13.56MHz | 1.5MHz | 13.56MHz | 13.56MHz | 10MHz | 13.56MHz | 13.56MHz | 13.56MHz | 13.56MHz |
| **Input Amp.** | 1.5-3.5V | 1.2-2.4V | 3.3-5V | 0.9-2V | 0.8-2.7V | N/A | 1.5-4V | 1.5-4V | 1.3-2.5V |
| **Output Volt.** | 1.2-3.22V ($R_L$=1.8kΩ) | 1.13-2.28V ($R_L$=2kΩ) 0.98-2.08V ($R_L$=100Ω) | 2.5-3.9V ($R_L$=500Ω) | 0.45-1.78V ($R_L$=1kΩ) | 0.3-2.0V ($R_L$=2kΩ) | 1.2V (load chip) | 1.27-3.6V ($R_L$=500Ω) | 1.28V-3.56V ($R_L$=1.8kΩ) 1.19V-3.52V ($R_L$=500Ω) | 1.24-2.44V ($R_L$=500Ω) 1.2-2.39V ($R_L$=100Ω) |
| **$P_{OUT}$ (Max.)** | 5.76mW | 43.3mW | 30.42mW | 3.2mW | 2mW | 112.5mW | 32mW | 24.8mW | 248.1mW |
| **VCR** | 78%-92% ($R_L$=1.8kΩ) | 94%-95% ($R_L$=2kΩ) 82%-84% ($R_L$=100Ω) | 76%-81% ($R_L$=500Ω) | 82%-89% ($R_L$=1kΩ) | 60%-89% ($R_L$=2kΩ) | N/A | 85%-90% ($R_L$=500Ω) | 87.3%-93% ($R_L$=1.8kΩ) 79%-89% ($R_L$=500Ω) | 94.8%-97.7% ($R_L$=500Ω) 91.7%-95.2% ($R_L$=100Ω) |
| **PCE** | 65%-89%* ($R_L$=1.8kΩ) | 82%-87%* ($R_L$=100Ω) | 68%-80.2% ($R_L$=500Ω) | 60%-81.9% ($R_L$=1kΩ) | 37%-80% ($R_L$=2kΩ) | 93%* (load chip) | 81%-84.2% ($R_L$=500Ω) | 82.2%-90.1% ($R_L$=500Ω) | 91.3%-94.6% ($R_L$=100Ω) |

* Simulation results.

† Compared with 1X structure.

# Integrated output capacitor $C_O$ included.

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# Conclusions

**The proposed real-time calibration techniques guaranteed that:**

- The active rectifier works at near-optimum operations under PVT variations that:
  - The NMOS on-delays are calibrated, conduction time is maximized;
  - The NMOS off-delays are calibrated, reverse current is minimized;
  - The VCR and PCE are always well optimized
  - Significant improvements are achieved

- The adaptive sizing further improves the VCR and PCE

# Thank You !



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Ishikuro Laboratory