A 1A, 20MHz/100MHz Dual-Inductor 4-Output Buck Converter with Fully-Integrated Bond-Wire-Based Output Filters for Ripple Reduction

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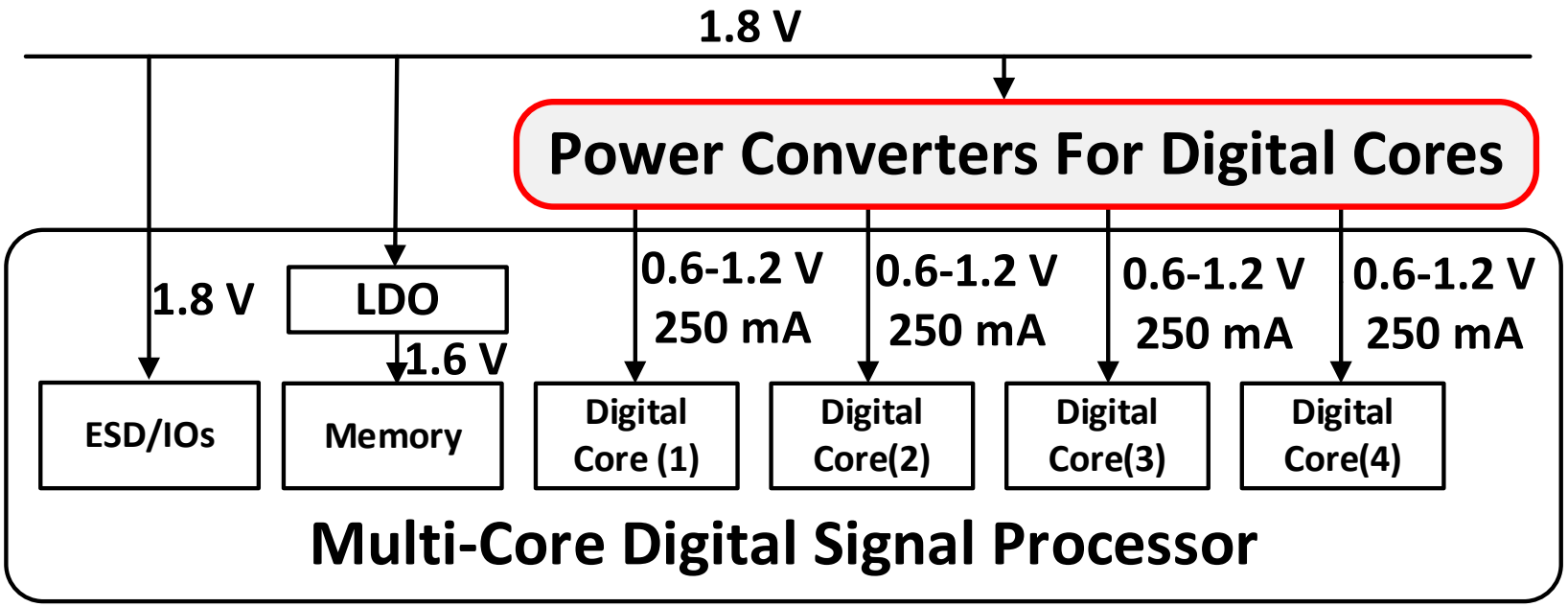
Outline

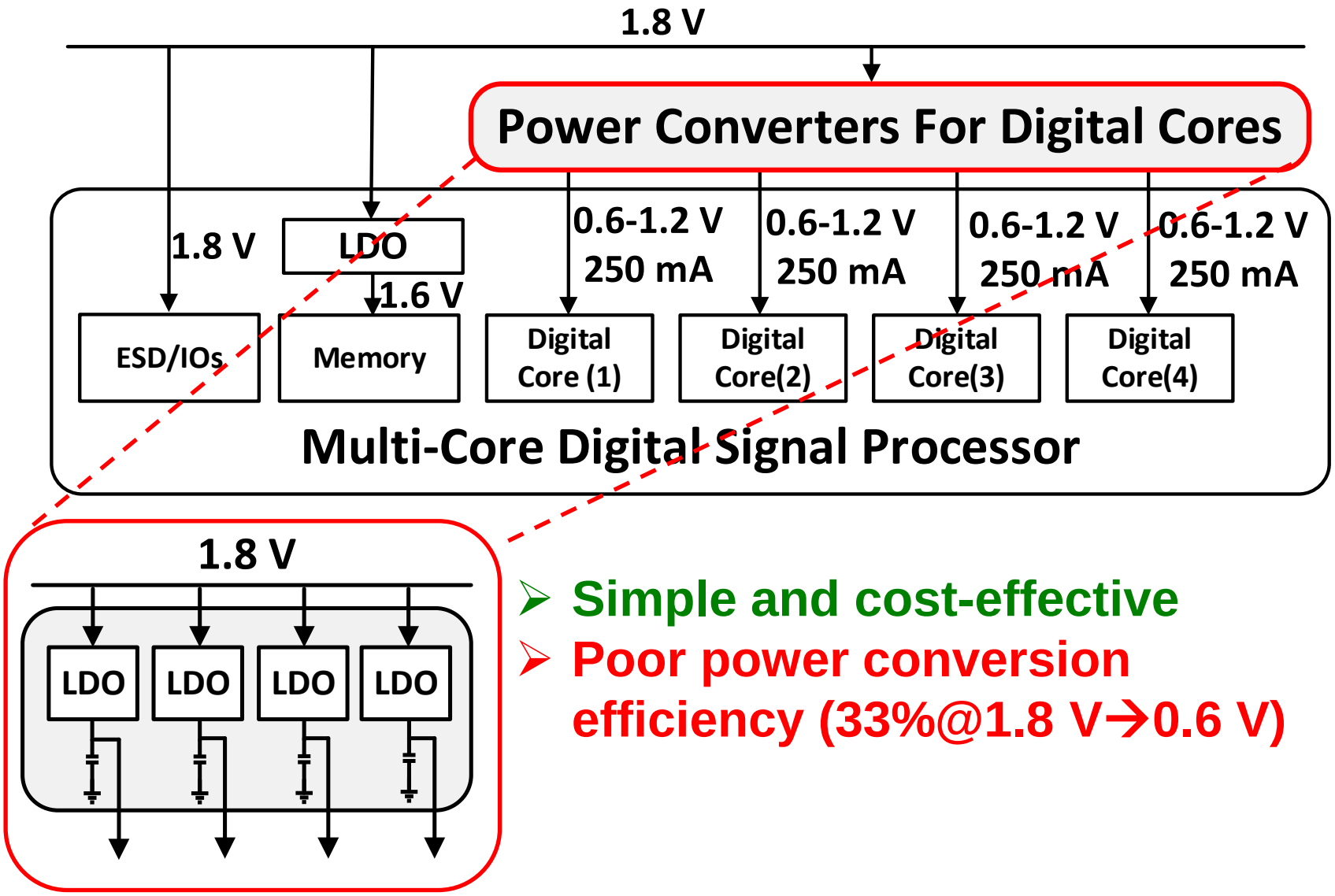
- Motivation
- Limitations of Existing Topologies
- The Proposed DF-DIMO Topology
- Measurement Results
- Comparison and Summary

Motivation



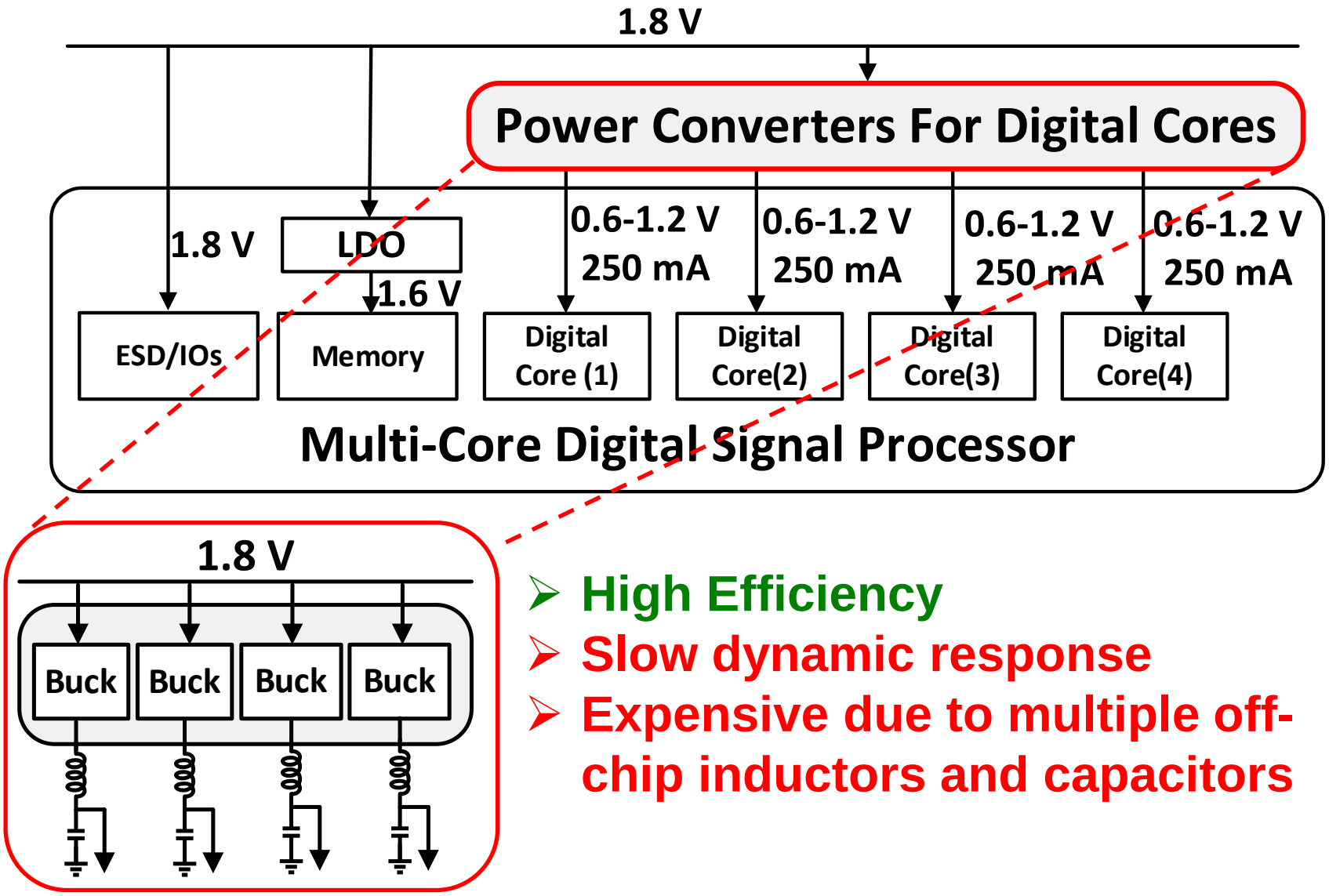
- Multiple dynamic power supplies with fast transient response
- 250-mA/core loads
- Wide range output voltages (0.6-1.2 V)

Linear Regulators



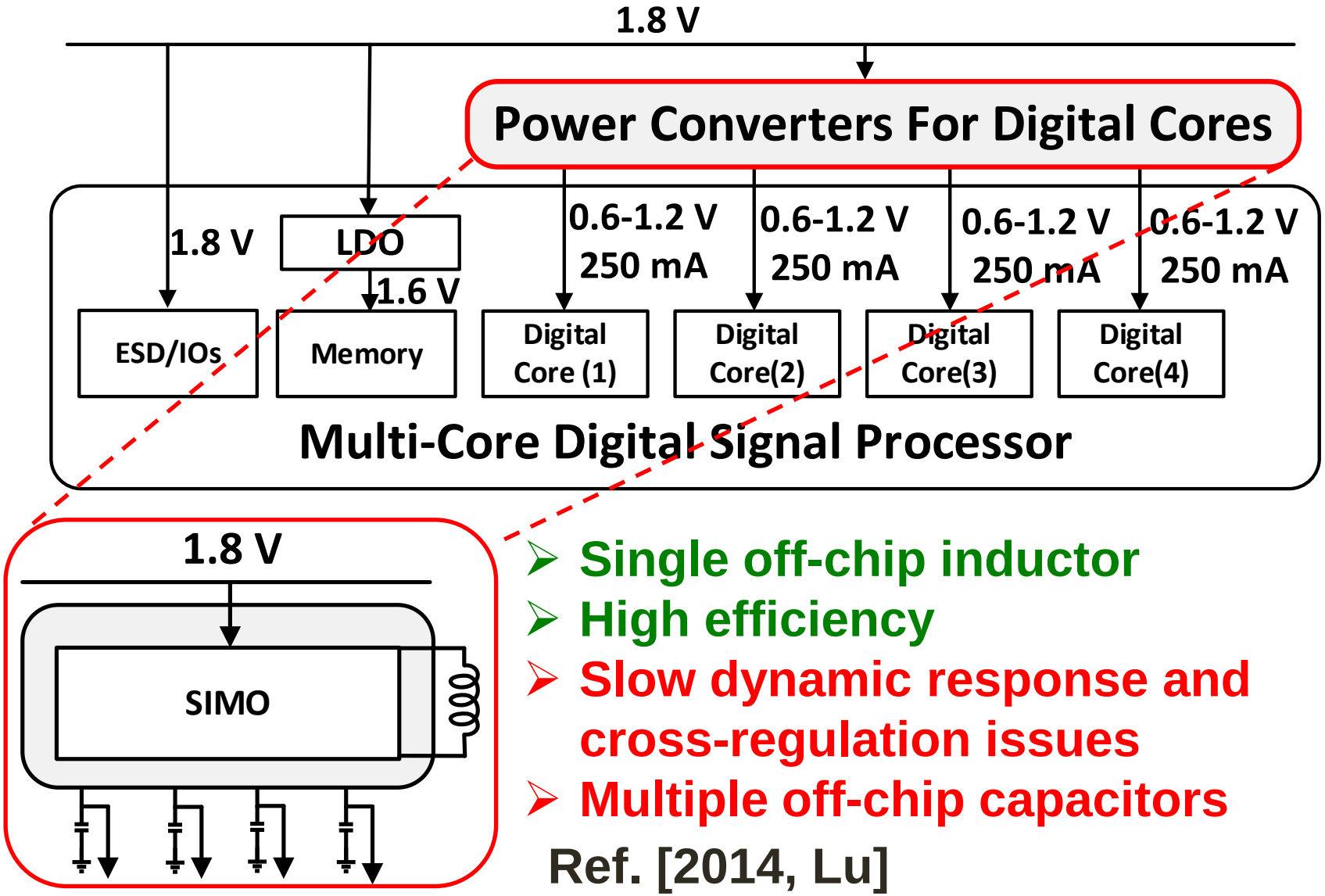
- Simple and cost-effective
- Poor power conversion efficiency (33%@1.8 V→0.6 V)

Conventional Buck



- High Efficiency
- Slow dynamic response
- Expensive due to multiple off-chip inductors and capacitors

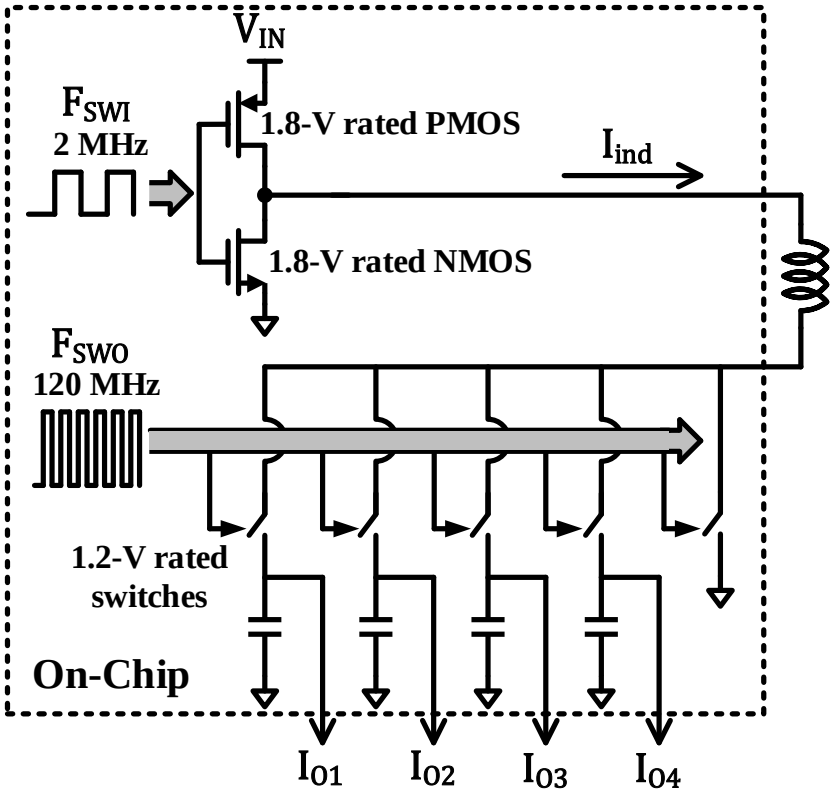
Conventional SIMO Buck

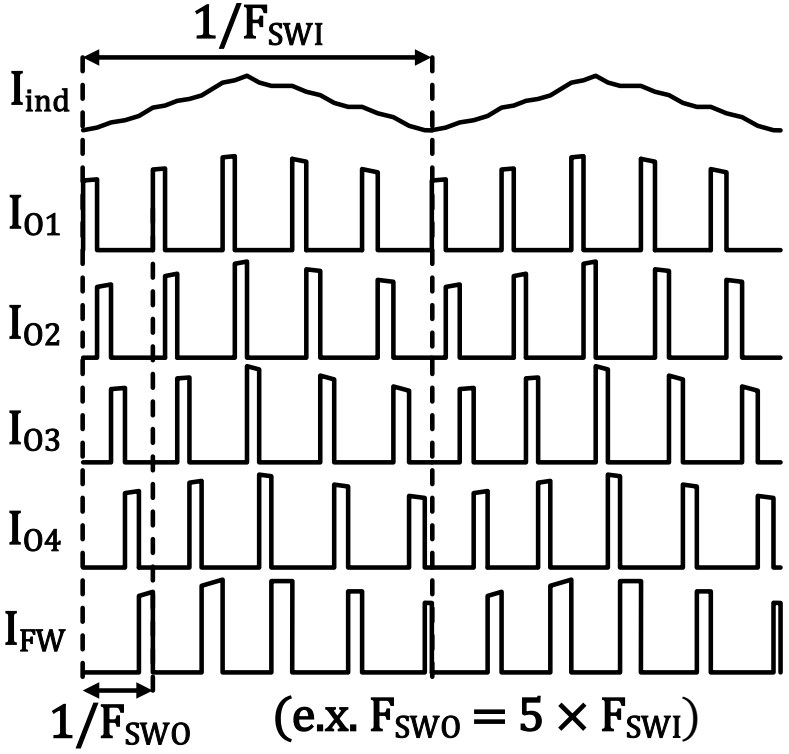


- Single off-chip inductor
- High efficiency
- Slow dynamic response and cross-regulation issues
- Multiple off-chip capacitors

Ref. [2014, Lu]

Dual-Frequency SIMO Buck

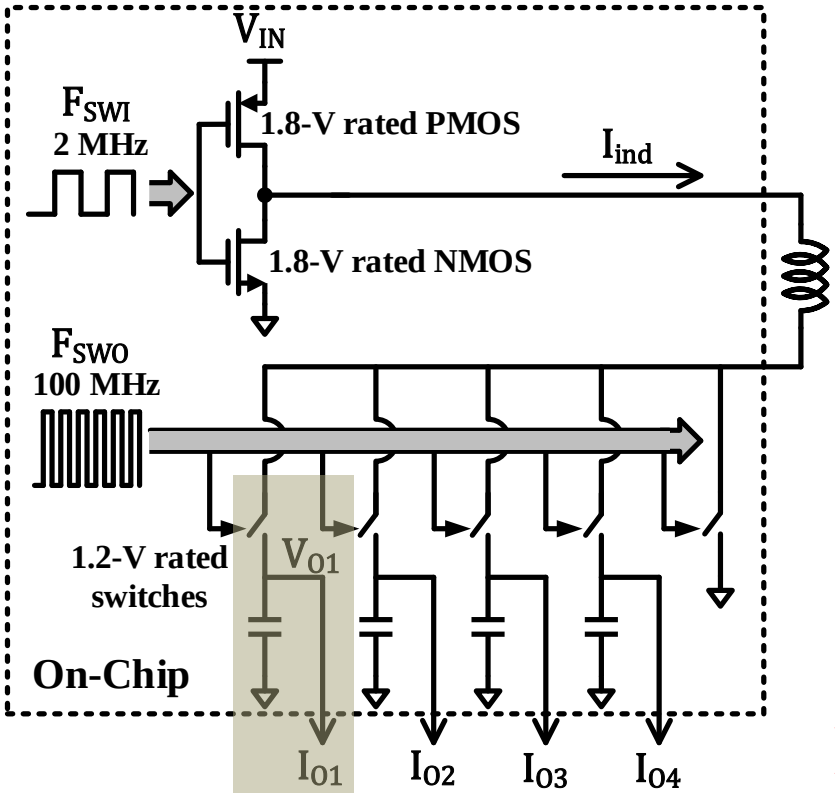




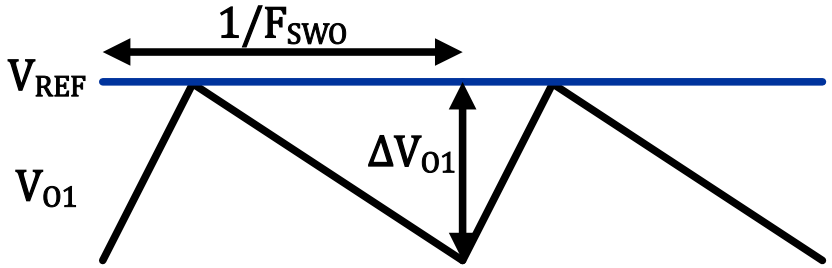
Ref. [2015, Chen]

- **High efficiency**
- **Much improved dynamic response**
- **No cross-regulation issues**
- **Fully-integrated output capacitors**

Dual-Frequency SIMO Buck



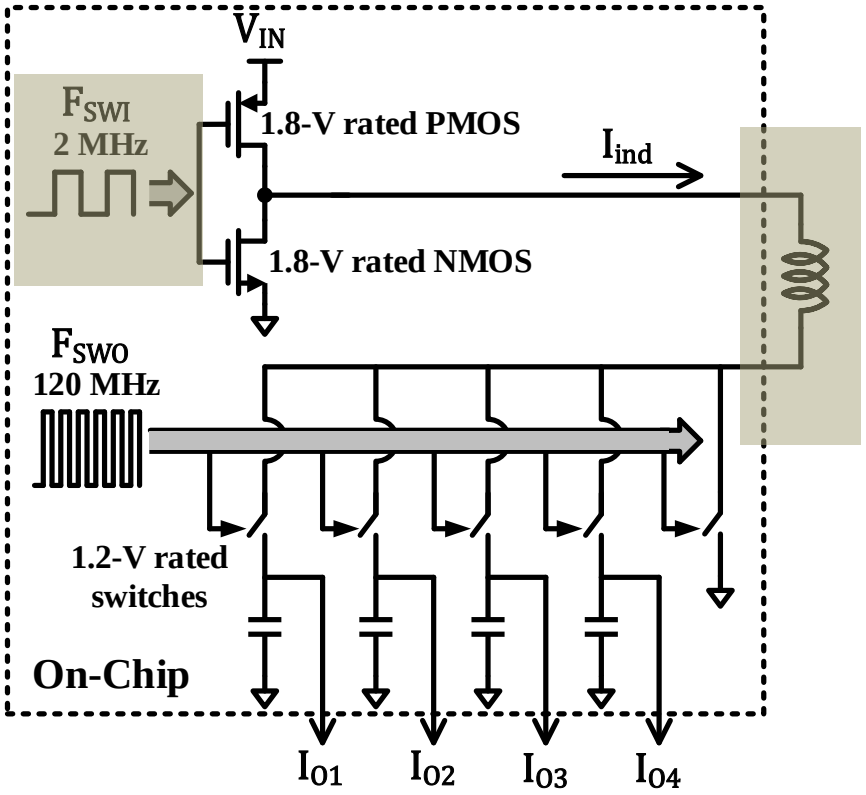
Ref. [2015, Chen]



$$\Delta V_{O1} \approx \frac{I_{O1}}{C_{O1} \cdot F_{SWO}} \left(1 - \frac{I_{O1}}{I_{ind}}\right)$$

- Excessive output voltage ripple (>80 mV) for loads beyond 50 mA
- Poor DC load regulation

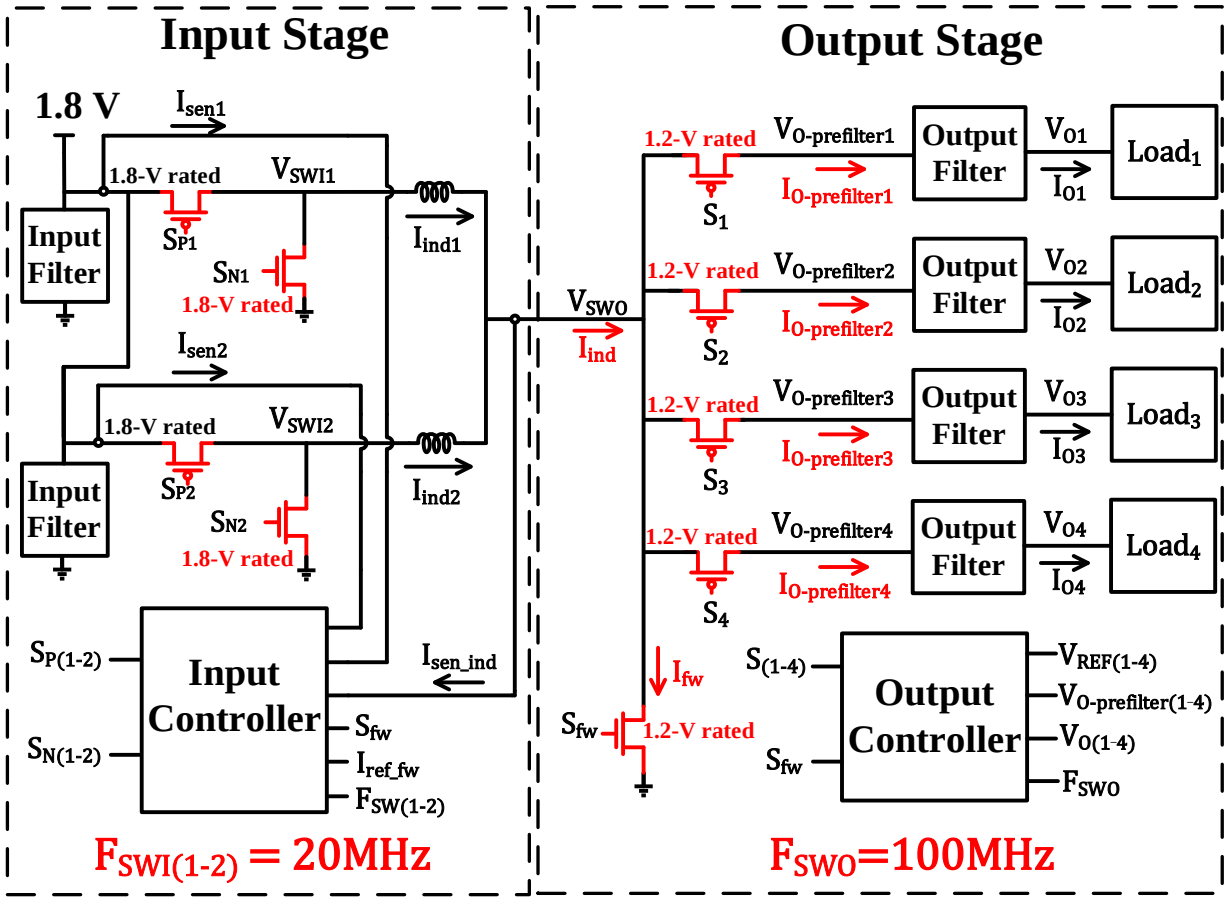
Dual-Frequency SIMO Buck



Ref. [2015, Chen]

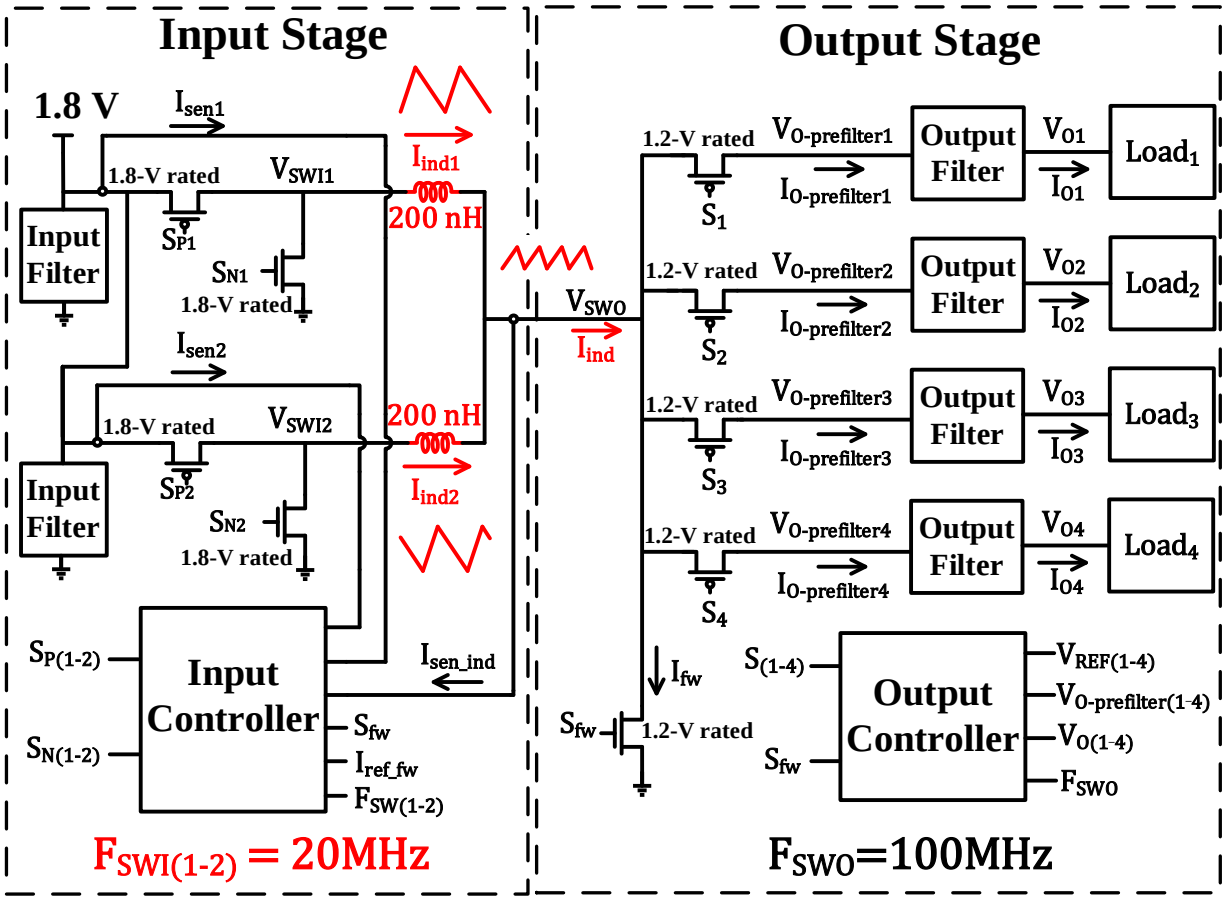
- Off-chip inductor
- Low input switching frequency still limits the dynamic response

Proposed DF-DIMO Buck



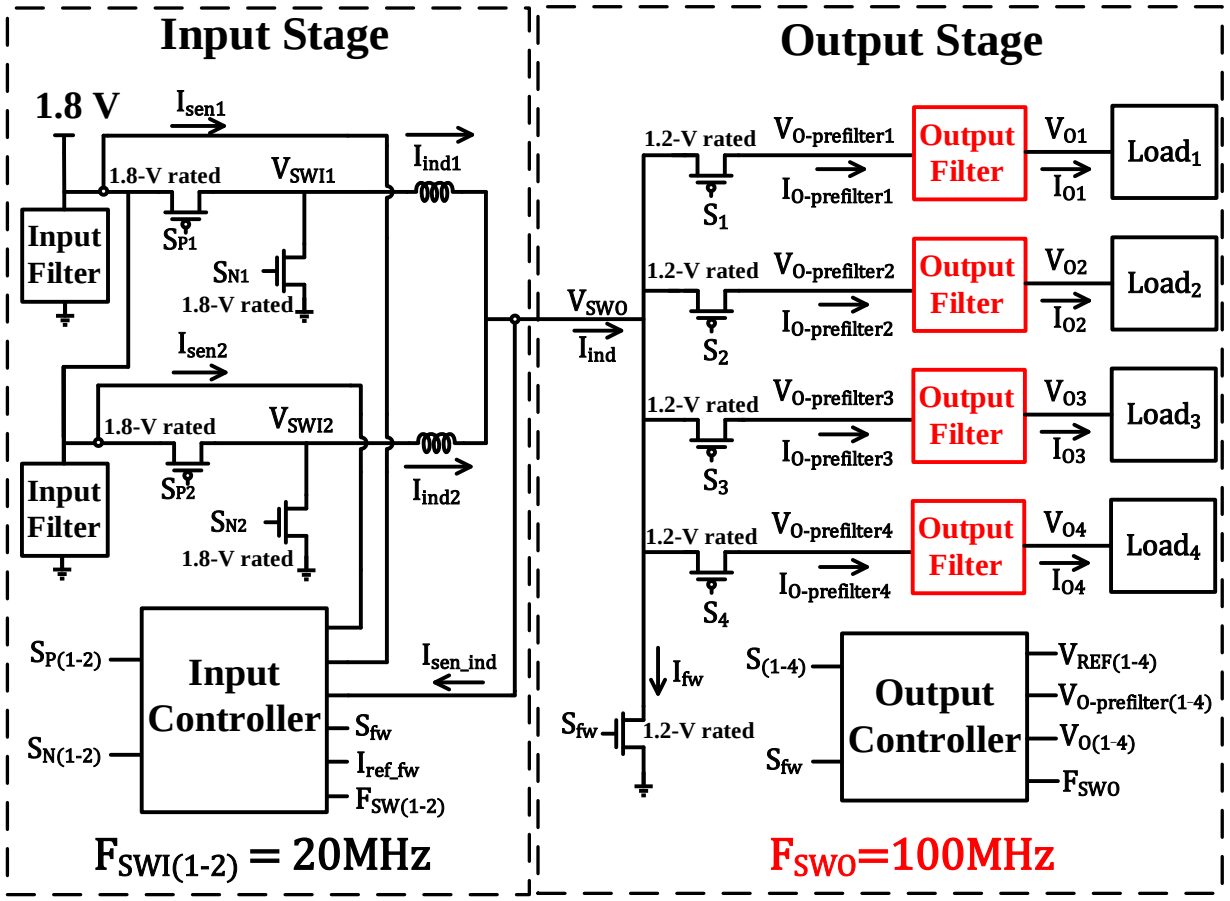
- Input stage : 1.8-V rated devices, F_{SWI} = 20 MHz
- Output stage: 1.2-V rated device, F_{SWO} = 100 MHz

Proposed DF-DIMO Buck



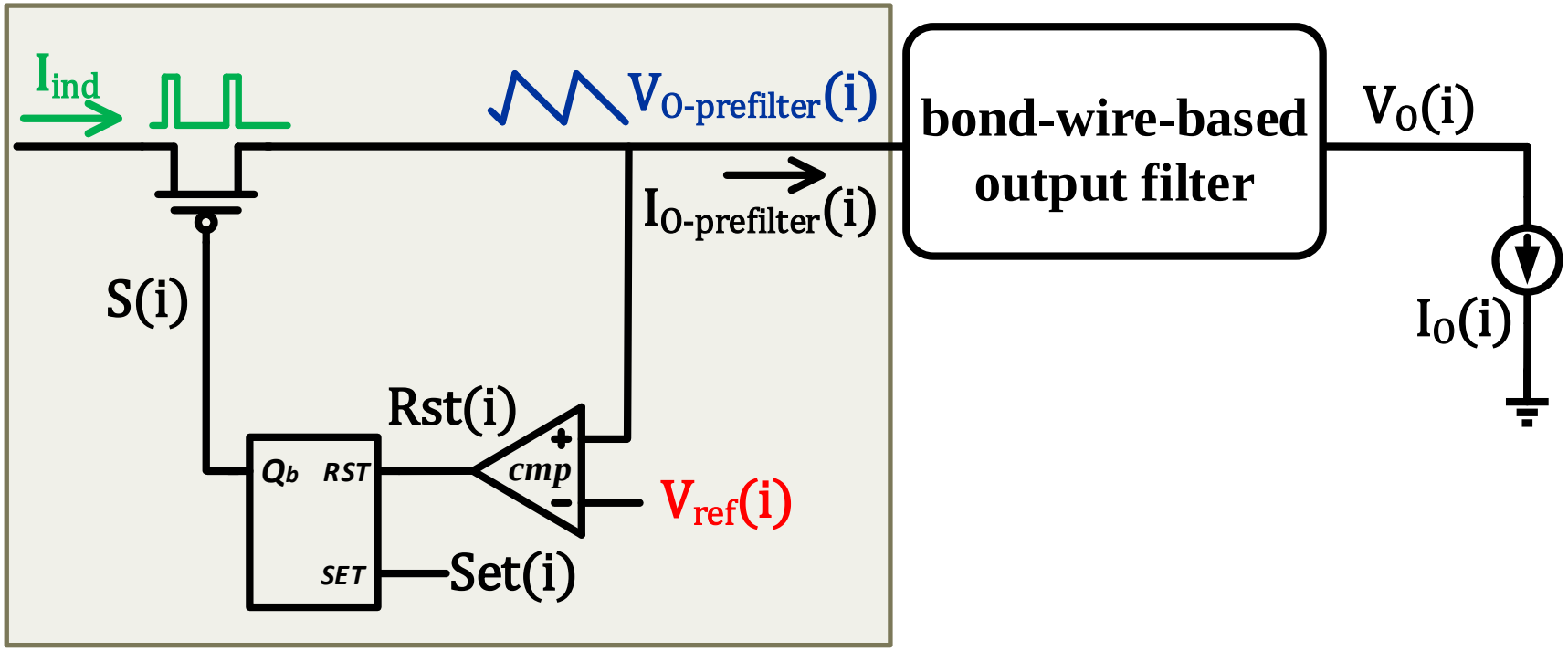
- F_{SWI} = 20 MHz → reduce off-chip inductance to 400 nH
- 2-phase input → reduce inductor conduction loss
- Both aspects further improve dynamic response

Proposed DF-DIMO Buck

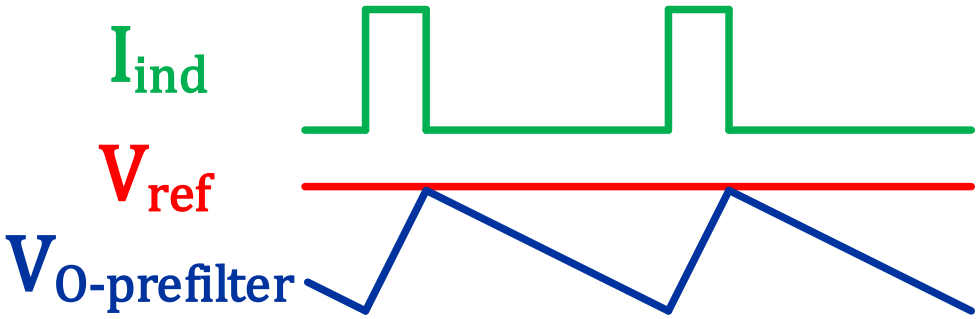


- Output filter → reduce output voltage ripple while allowing loads higher than 50 mA
- F_{SWO} = 100 MHz → reduce area, fast dynamic response

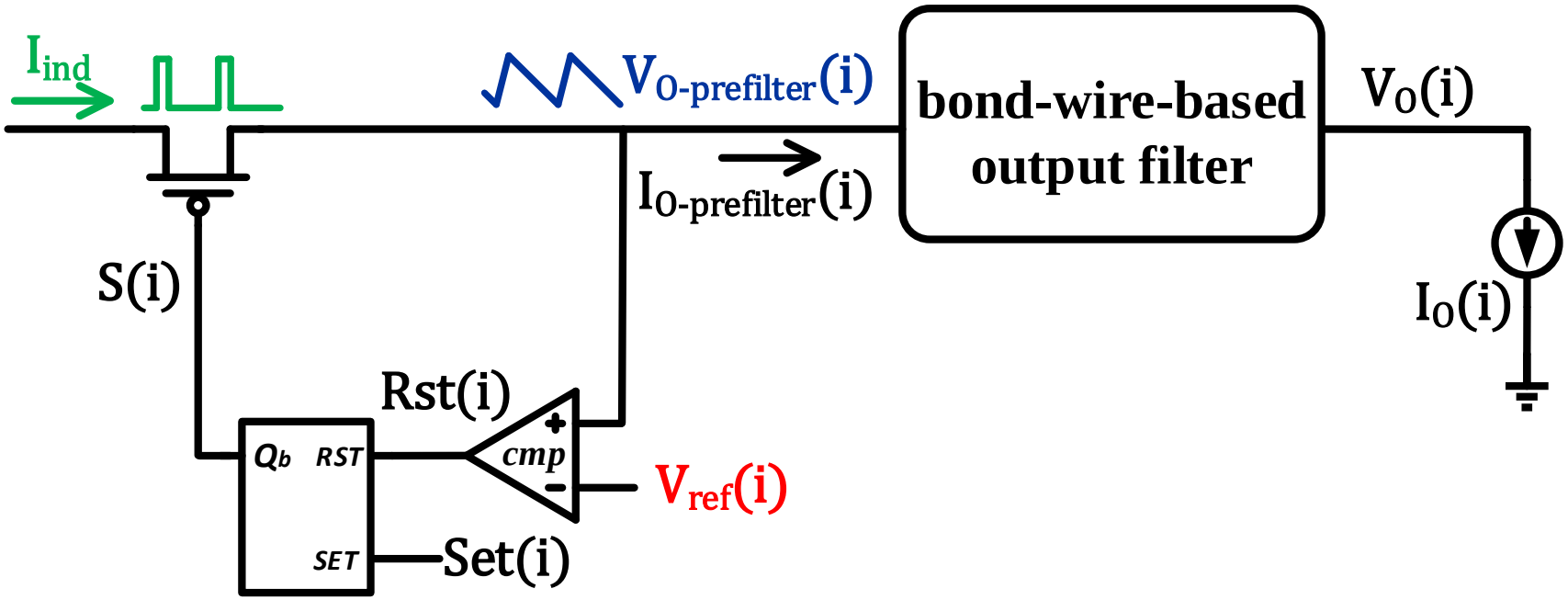
Output Voltage Regulation

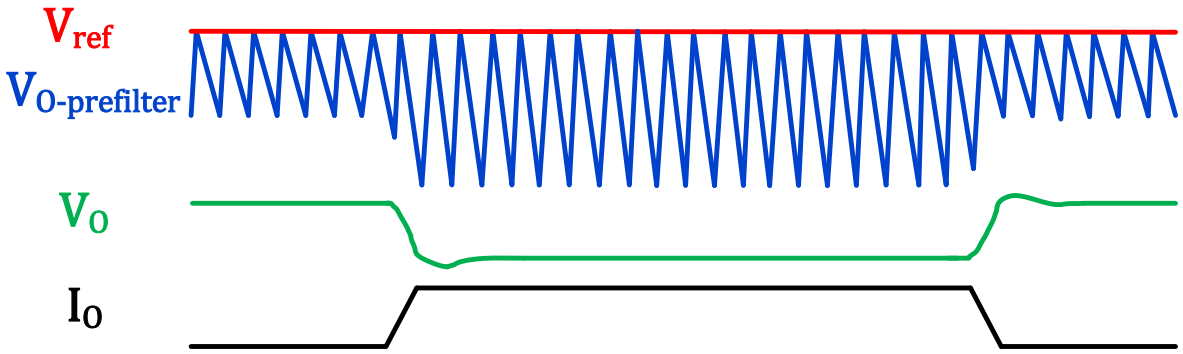


Comparator Based Control



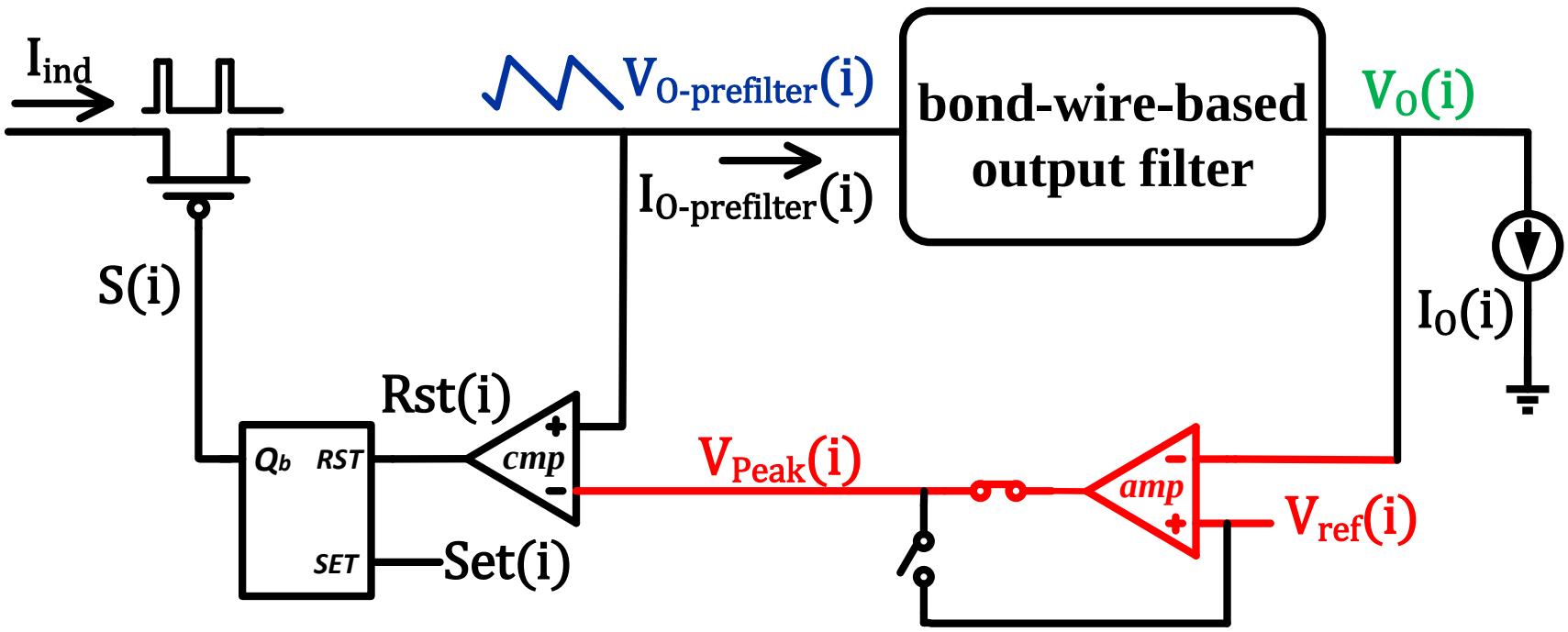
Output Voltage Regulation

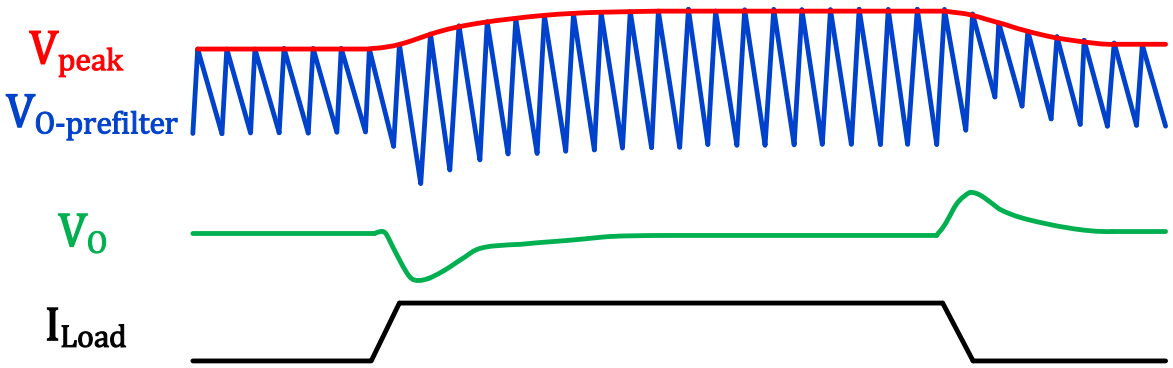




Poor DC load regulation

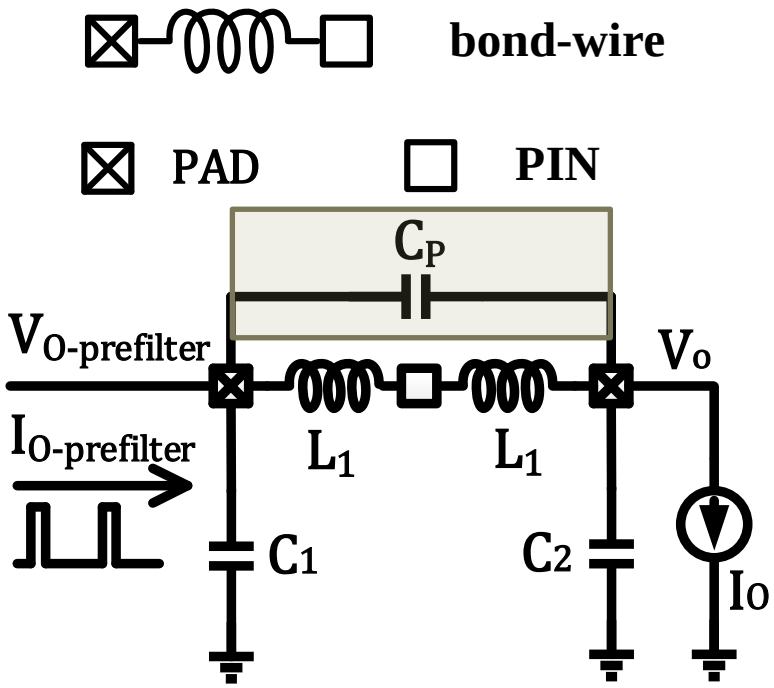
Output Voltage Regulation

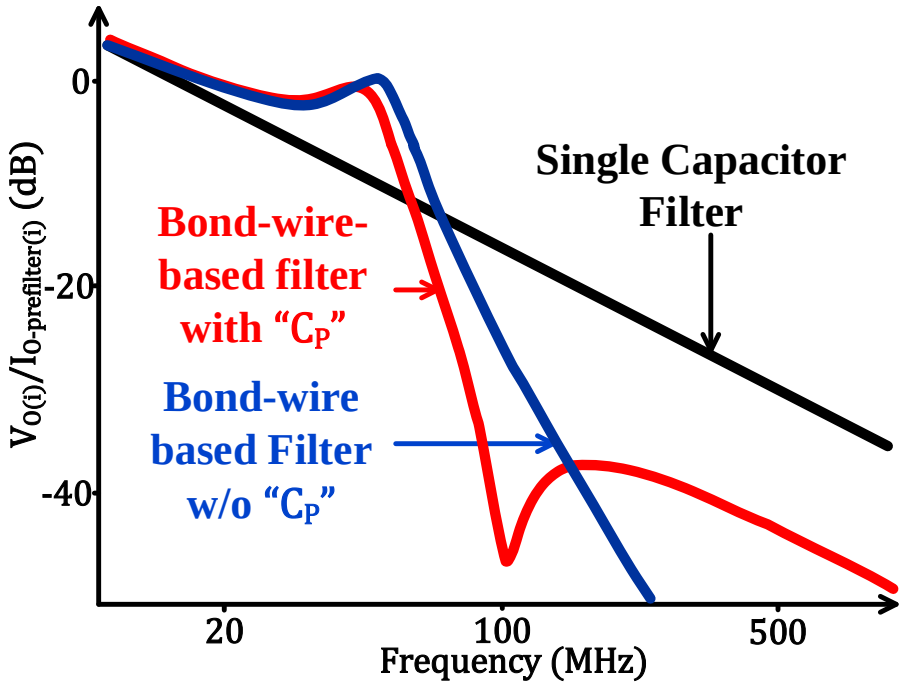




Improved DC load regulation

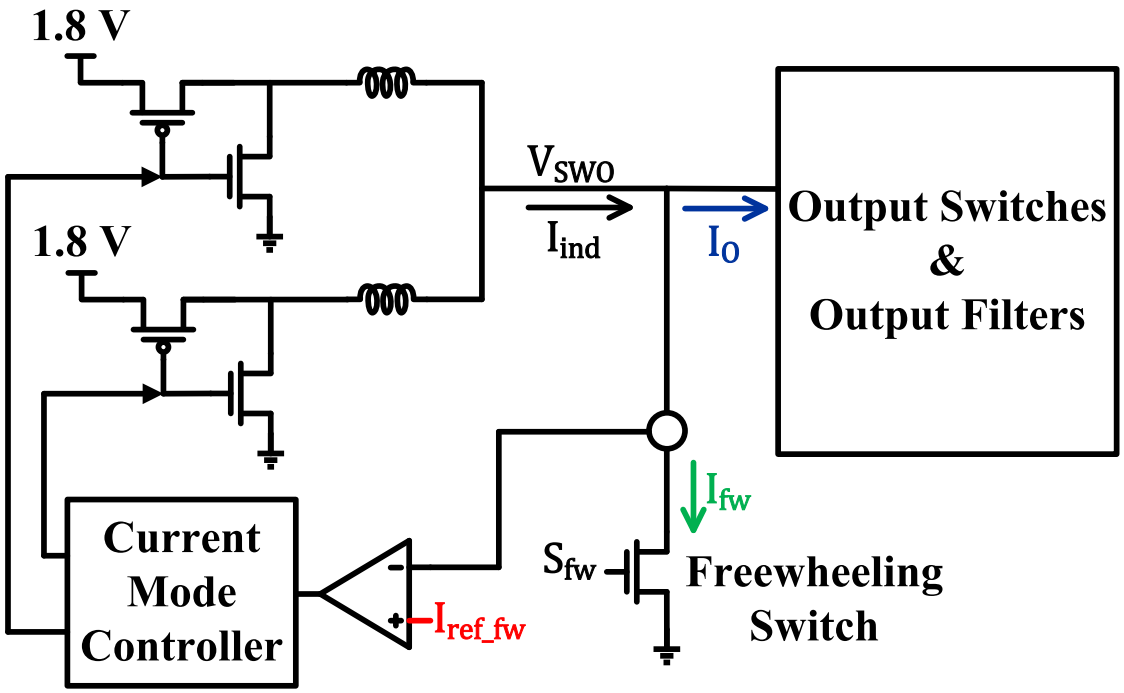
Proposed Output Filter



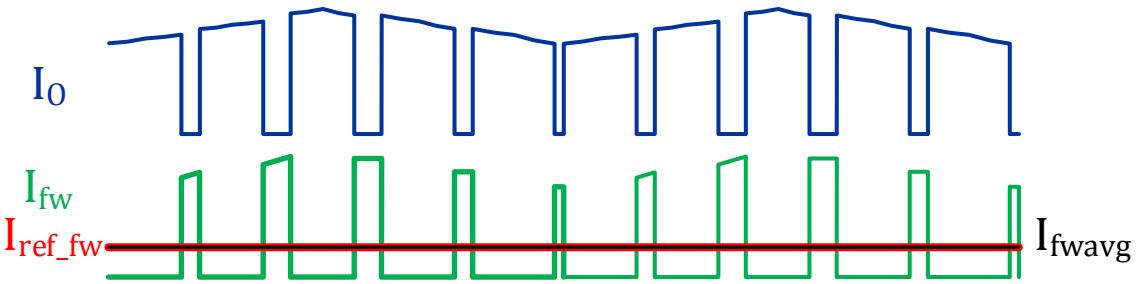


Bond-wire-based Filter

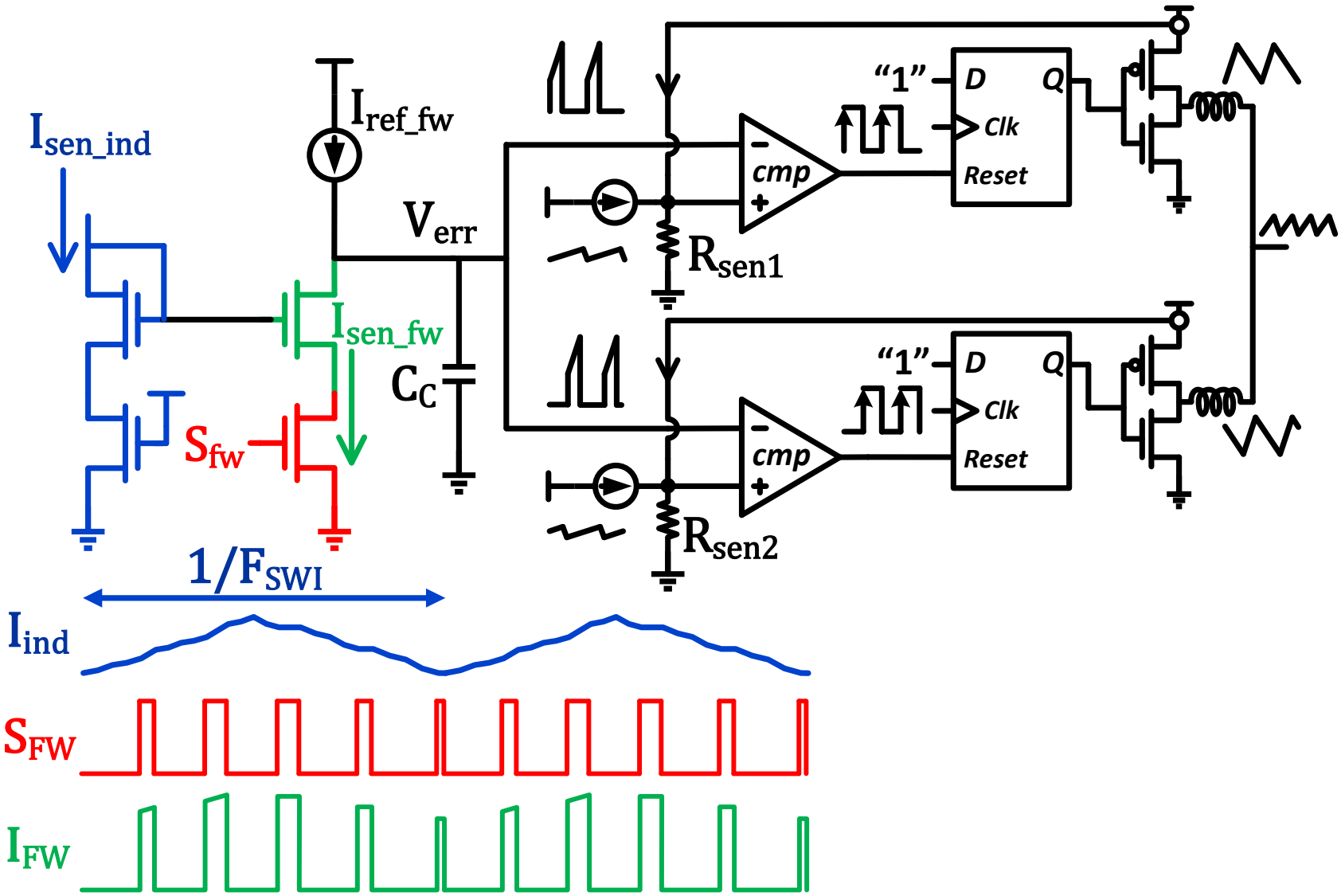
Input Stage Regulation



Freewheeling Current-Mode Control

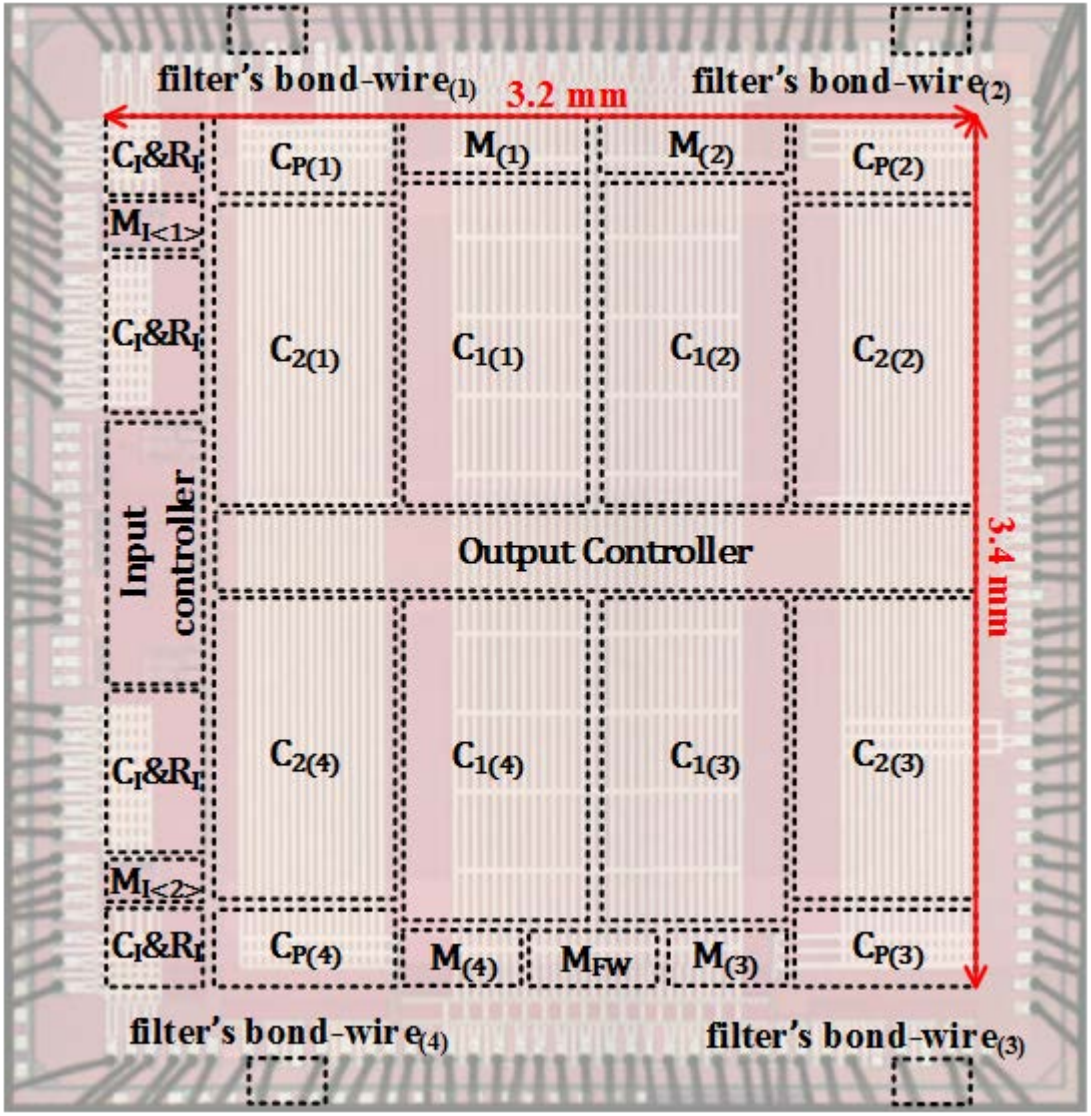


Input Stage Regulation



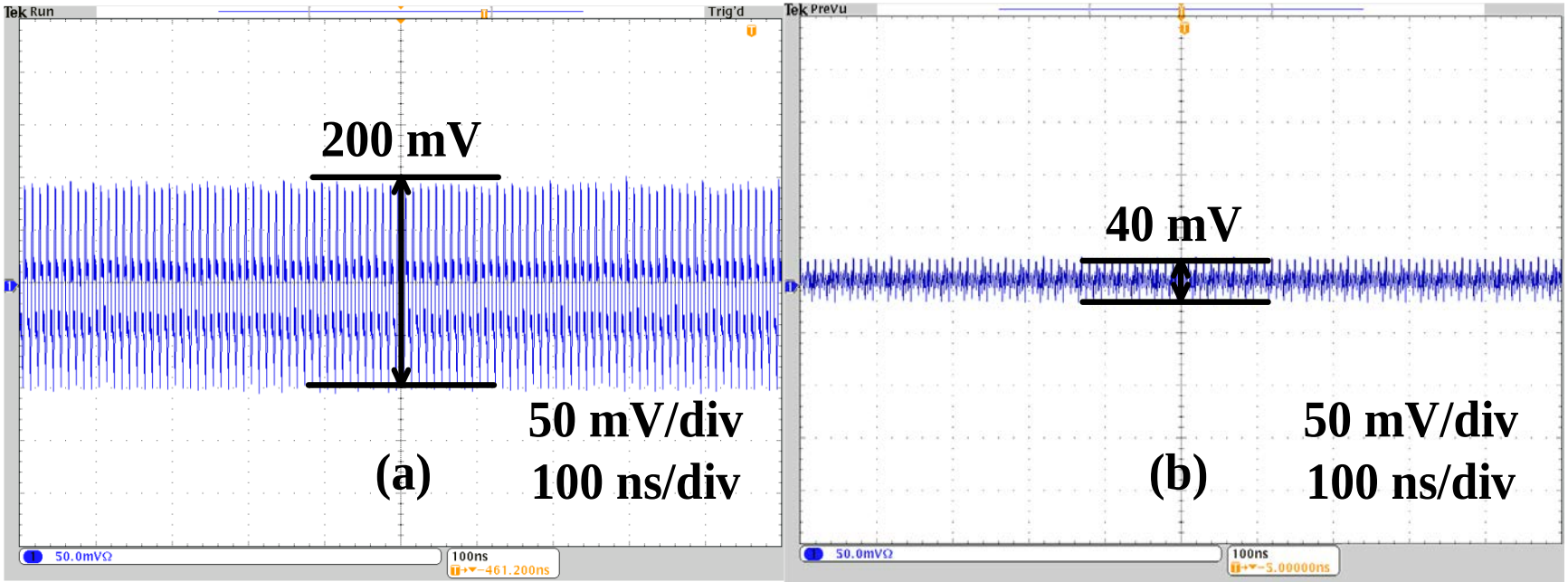
Measurement Results

Tech.	65 nm
# of Outputs	4
Input Voltage	1.8 V
Output Voltage	0.6–1.2 V
Total Load	1 A (250 mA/output)
Total Output Cap.	40 nF
Total Ind.	400 nH
Input Switching Frequency	20 MHz
Output Switching Frequency	100 MHz



Measurement Results

- **Output Voltage Ripple @ Full Load (250 mA)**

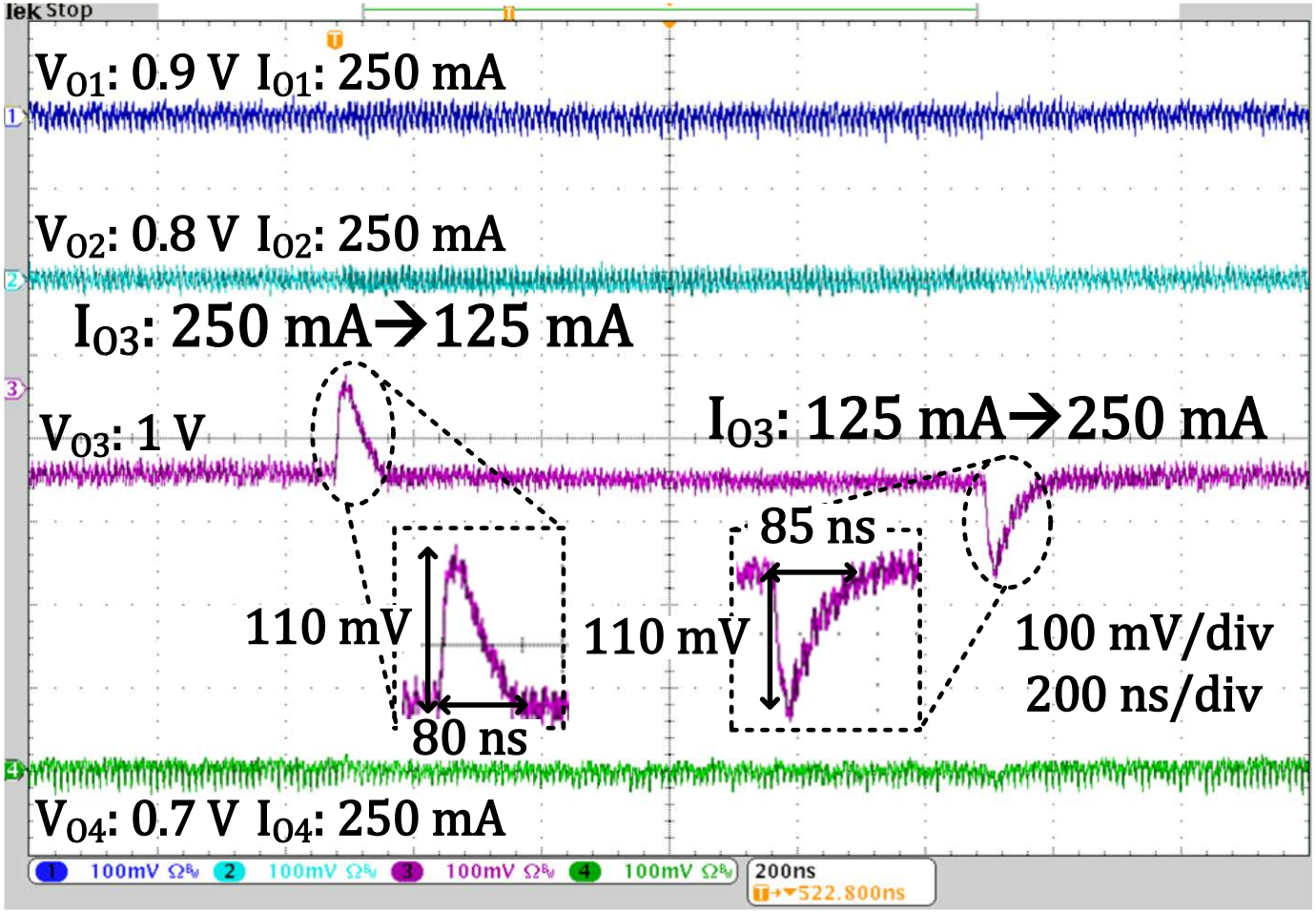


Single-capacitor filter

Proposed bond-wire-based filter

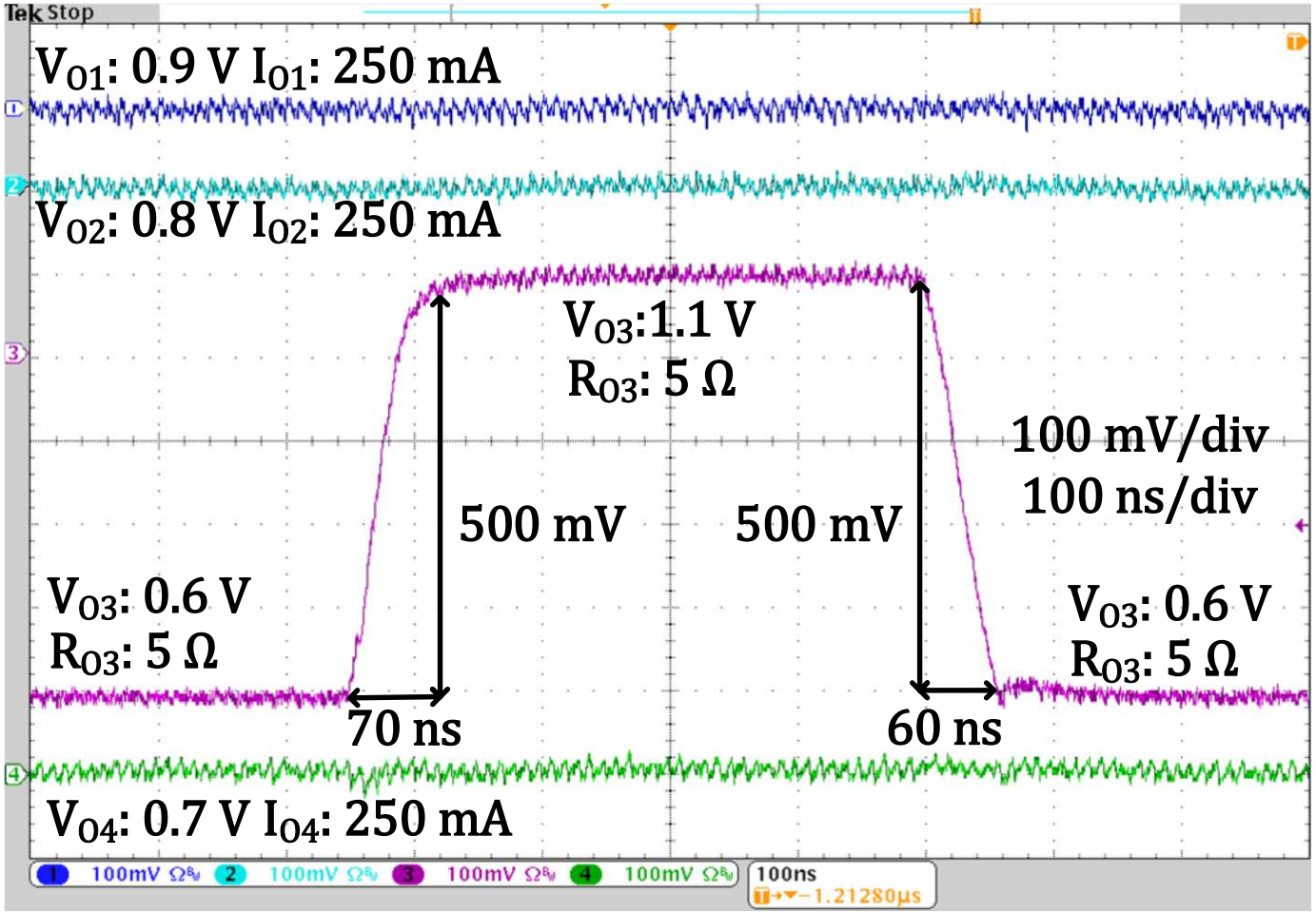
Measurement Results

- **Transient load regulation**



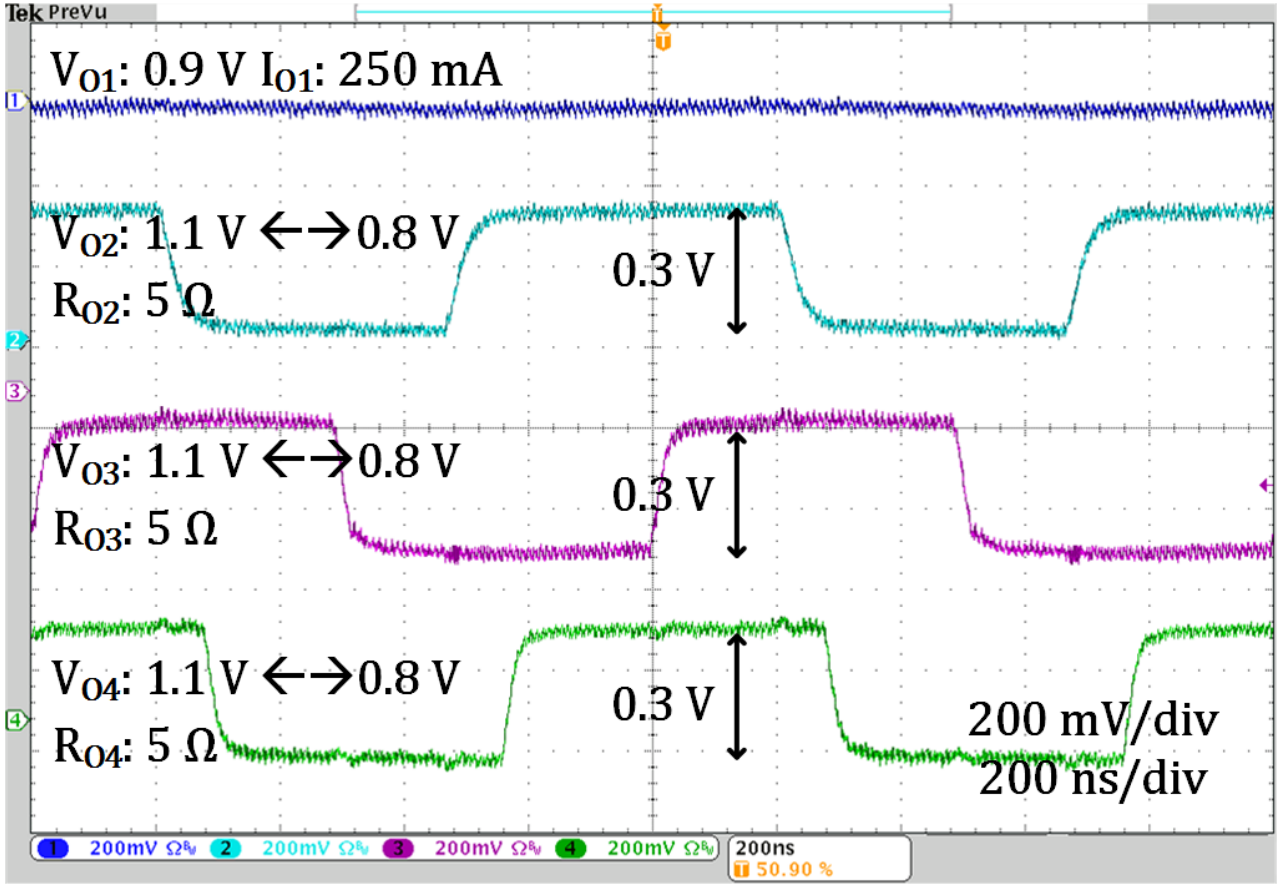
Measurement Results

- **Dynamic voltage scaling**



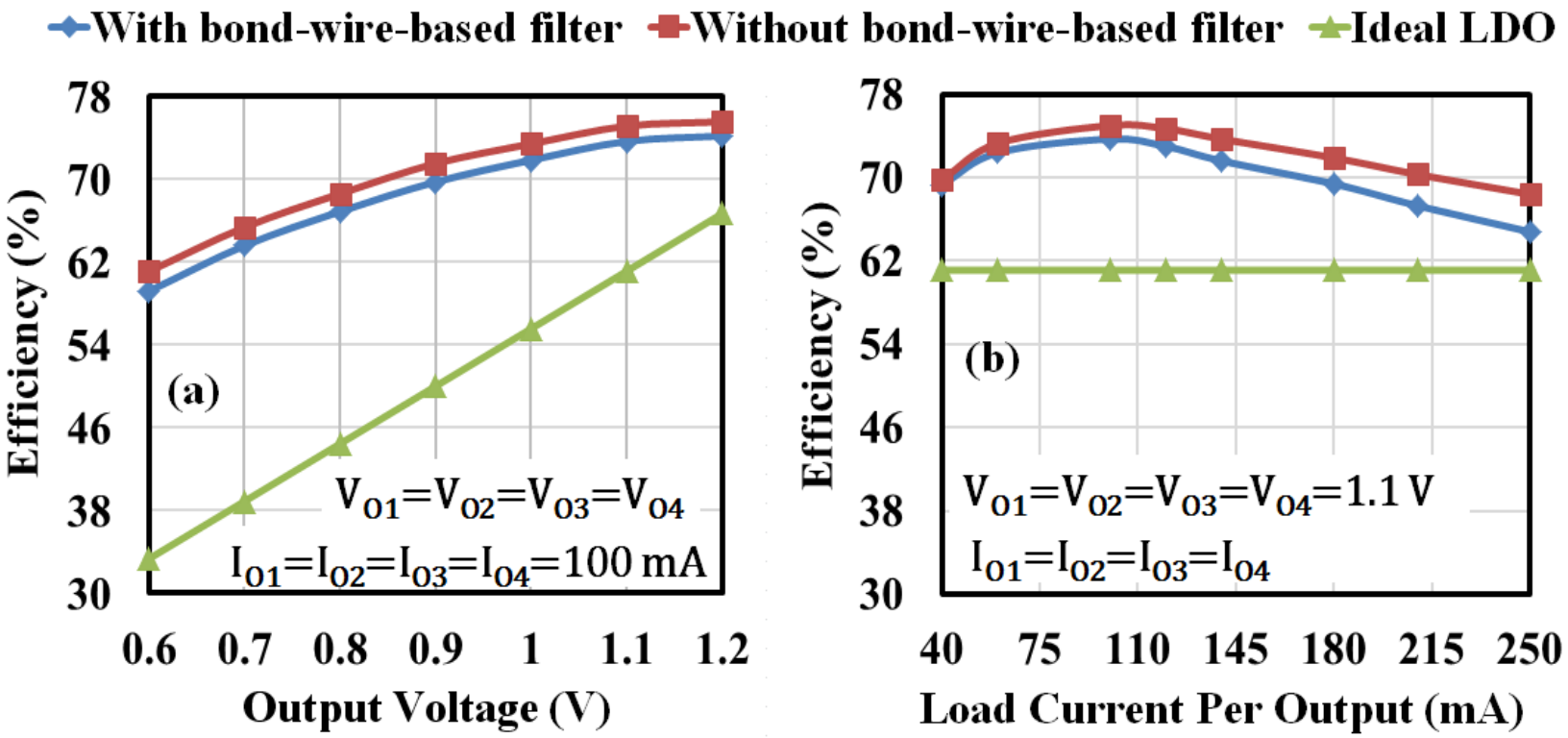
Measurement Results

- **Dynamic voltage scaling (multiple outputs)**
- **Excellent cross-regulation performance**



Measurement Results

- **Efficiency**



Comparison

Ref.	[1] 2014 ISSCC	[3] 2010 JSSC	[4] 2011 JSSC	[2] 2015 JSSC	This work
Topology	SIMO	SC	Buck	DF-SIMO	DF-DIMO
Tech.	0.35 μm	45 nm	0.13 μm	45 nm	65 nm
# of Outputs	4	1	1	5	4
Input Range	2.7–5 V	1.8 V	1.2 V	1.8 V	1.8 V
Output Range	0.9–1.8 V	0.8–1 V	0.3–0.88 V	0.6–1.6 V	0.6–1.2 V
Total Load	1.6 A	8 mA	0.3 A	0.11 A	1 A
Total Output Cap.	40 μF	1.2 nF	5 nF	13 nF	40 nF
Total Ind.	4.7 μH	None	2 nH	10 μH	400 nH
Peak Efficiency	87%	69%	74%	73%	74%
DVS	0.6V/10μs	0.2V/2μs	0.25V/0.65μs	0.6V/80ns	0.5V/60ns
Voltage Ripple	30 mV	50 mV	28 mV	80 mV	40 mV

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Summary

- **DF-DIMO topology is proposed to generate 4, 250-mA outputs with only 2-200 nH inductors and on-chip output capacitors**
- **Achieve 0.5-V/60-ns DVS and settling time of less than 85 ns for a 125-mA load step**
- **Proposed bond-wire-based filter reduces the output voltage ripple while allowing higher loads**

Reference

- [1] D. Lu, et al., “An 87%-peak-efficiency DVS-capable single-inductor 4-output DC-DC buck converter with ripple-based adaptive off-time control,” *ISSCC Dig. Tech. papers*, pp. 82–83, Feb. 2014.
- [2]C. Chen, et al., “A Low-Power Dual-Frequency SIMO Buck Converter Topology with Fully-Integrated Outputs and Fast Dynamic Operation in 45-nm CMOS,” *IEEE J. Solid-State Circuits*, Vol. 50, No. 9, pp. 2161-2173, Sept. 2015.
- [3]Y. Ramadass, et al., "A fully-integrated switched-capacitor step-down DC-DC converter with digital capacitance modulation in 45 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2557–2565, Dec. 2010.
- [4]S. Kudva, et al., “Fully-integrated on-chip DC-DC converter with a 450X output range,” *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1940–1951, Aug. 2011.

Acknowledgements

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