3.5-0.5V Input, 1.0V Output Multi-Mode Power Transformer for a Supercapacitor Power Source with a Peak Efficiency of 70.4%

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Talk Outline

- Design motivation
  - Supercapacitors voltage drop
  - LDO drawbacks
- Prior work & state of the art
- Wide input range, fixed output DC-DC converter
  - Topology reconfiguration
  - Voltage protection
  - Efficiency analysis
- Prototype design
  - Measurement results
- Summary & conclusions

Supercapacitor (Supercap/Ultracap)

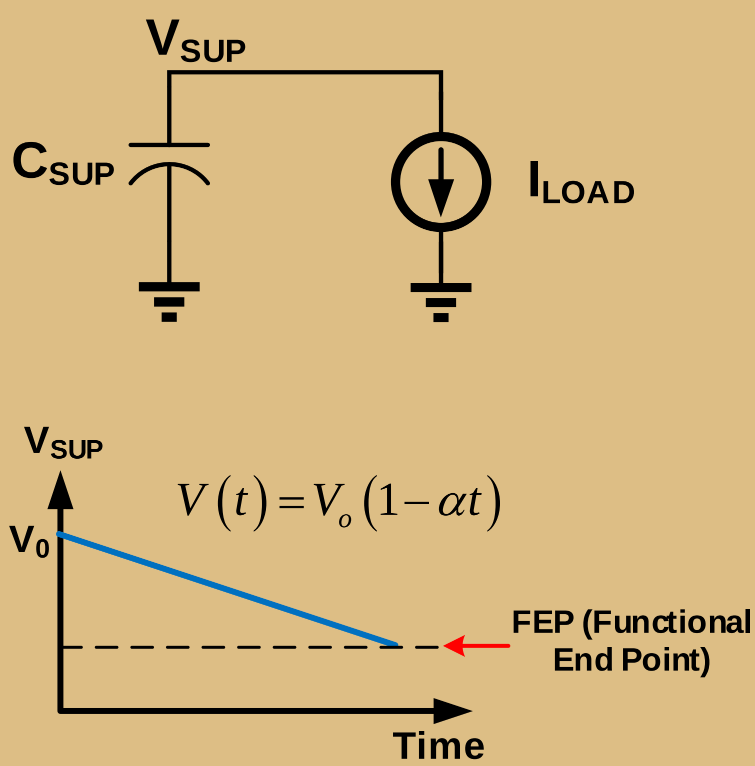
- **Applications for supercaps**
  - **High peak power, quick charge → hybrid vehicles**
  - **Effectively infinite number of charge/discharge cycles**

Function	Supercap	Lithium-ion
Charge time (second)		~4,000
Internal resistance (ESR	Ω	~0.2 Ω
Energy density (Wh/kg		~150
Instantaneous power density	0	~2,000
Operating temperature	-40 to +65 °C	0 to +40 °C
Bio compatibility	No harsh chemicals	Harsh chemicals
Shelf life (hours)	~1,000,000	~500

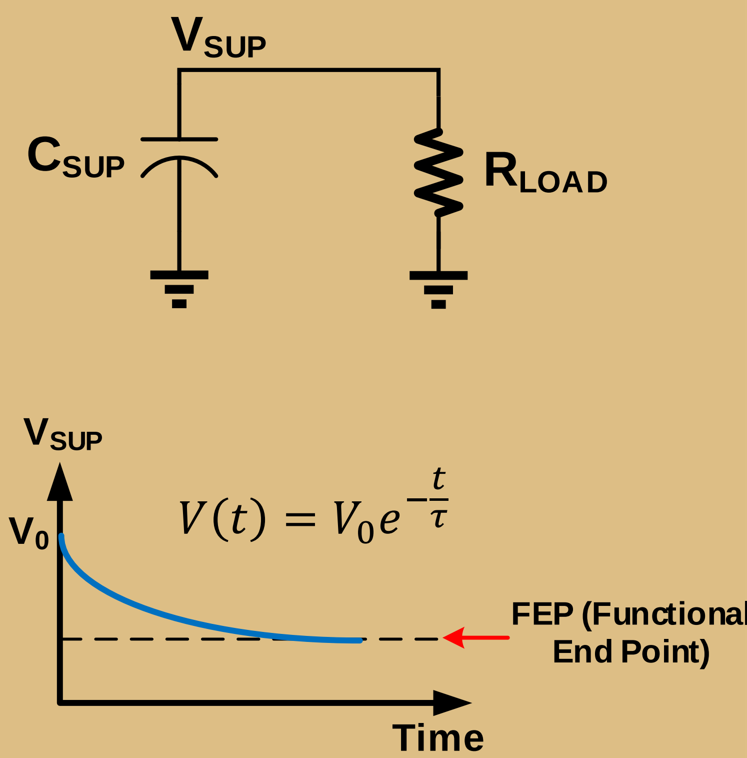
Supercap Voltage Discharge Curve

- **Supercap is after all a capacitor** $V_{\text{sup}} = \dfrac{Q}{C_{\text{sup}}}$

Fixed Current Load

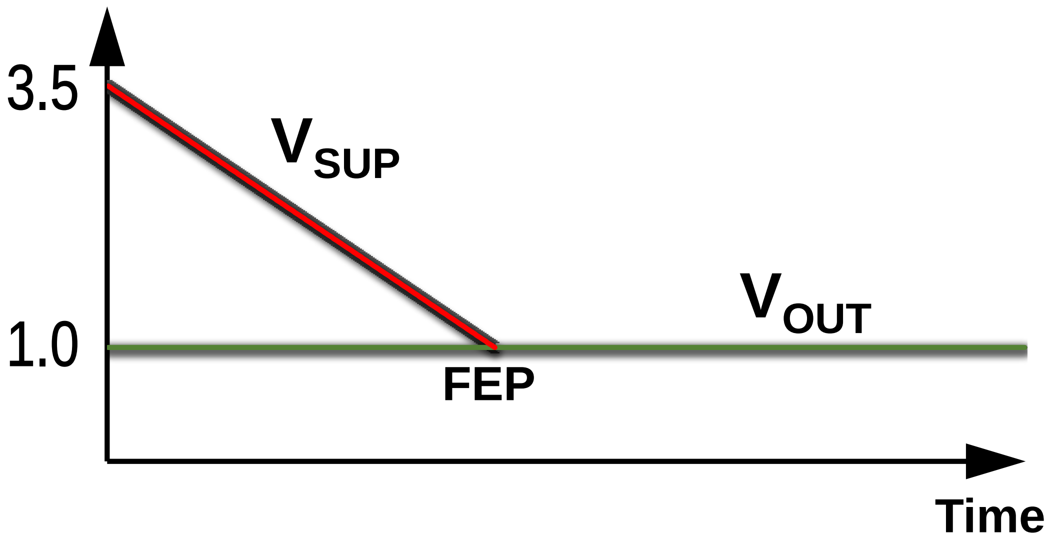


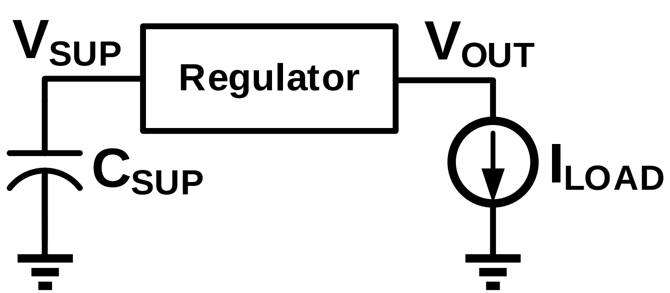
Fixed Resistor Load



Voltage Regulation: LDO

- Voltage regulation
  - Linear regulator or low-dropout (LDO) regulator
- Linear voltage drop ($I_{load} = I_{sup}$)
  - Peak voltage → device breakdown concerns
  - Energy lost in the regulator → series loss
  - FEP → wasted residual energy $$E_{RES} = \frac{1}{2} C_{SUP} {V_{SUP}}^2$$





LDO vs. Ideal "Transformer"

- **LDO**

$$I_{SUP} = I_{LOAD}$$

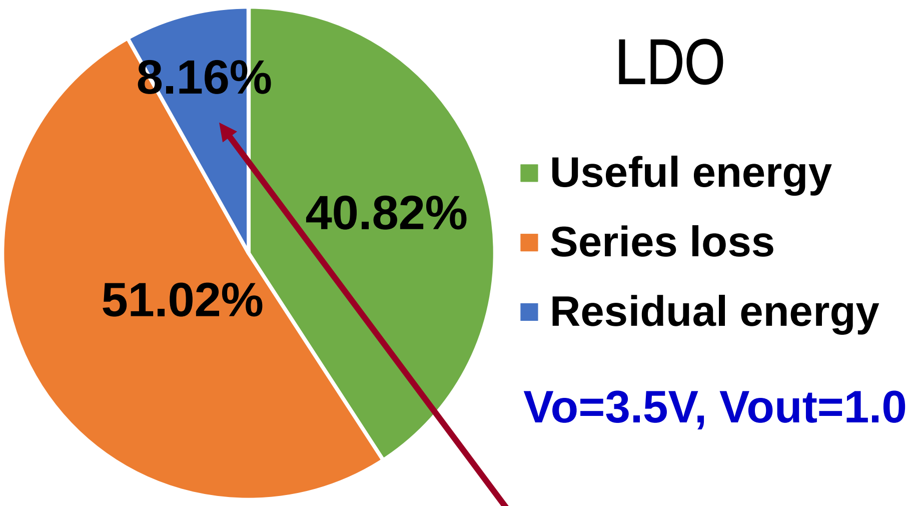
$$Efficiency = \frac{V_{out}}{V_{SUP}}$$

- **Ideal "Transformer"**

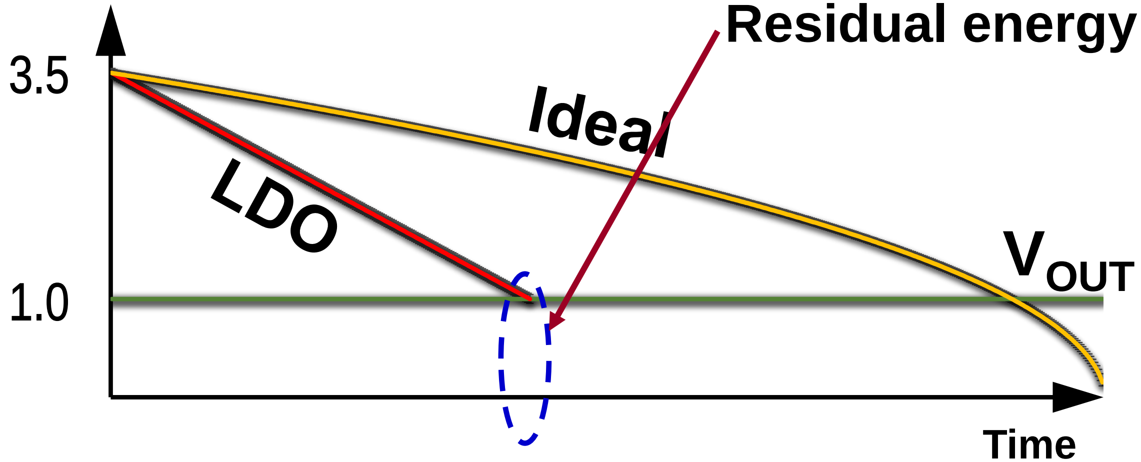
$$P_{SUP} = P_{out}$$

$$I_{SUP} \times V_{SUP} = I_{out} \times V_{out}$$

$$Efficiency = 100\%$$

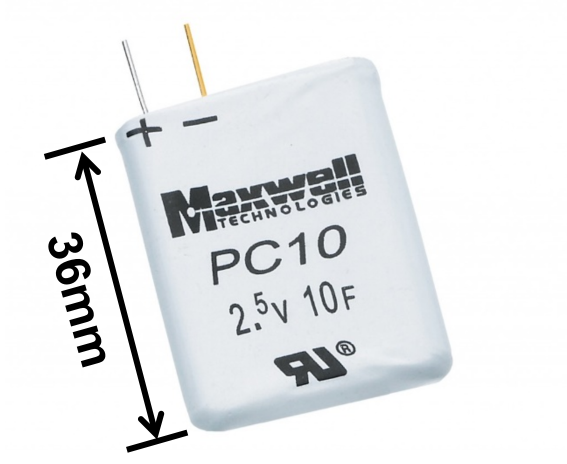


Residual energy

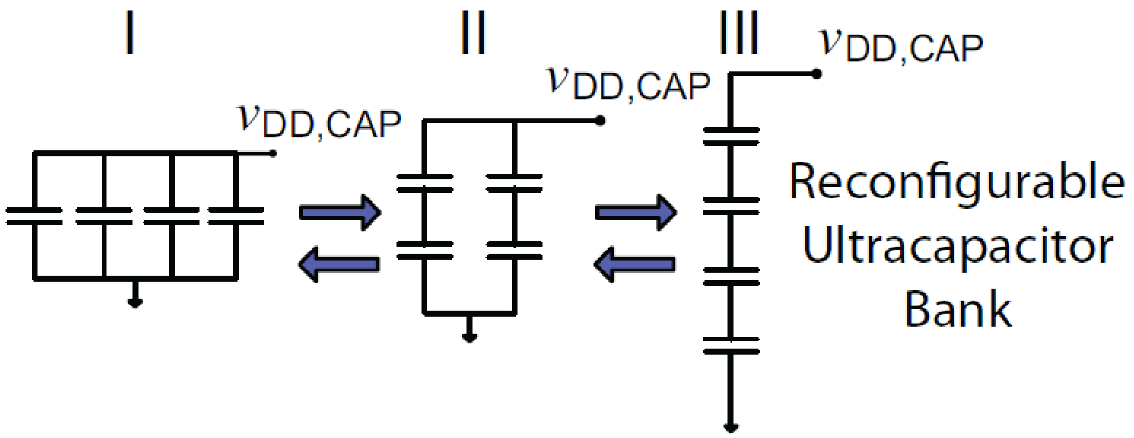


Prior Work & State of the Art (I)

- **Reconfigure the supercap bank**
  - **V_{IN}=1.25-2.5V, V_{OUT}=1.0V**
  - **Need a minimum of two supercaps**
  - **Supercaps are large off-chip components**



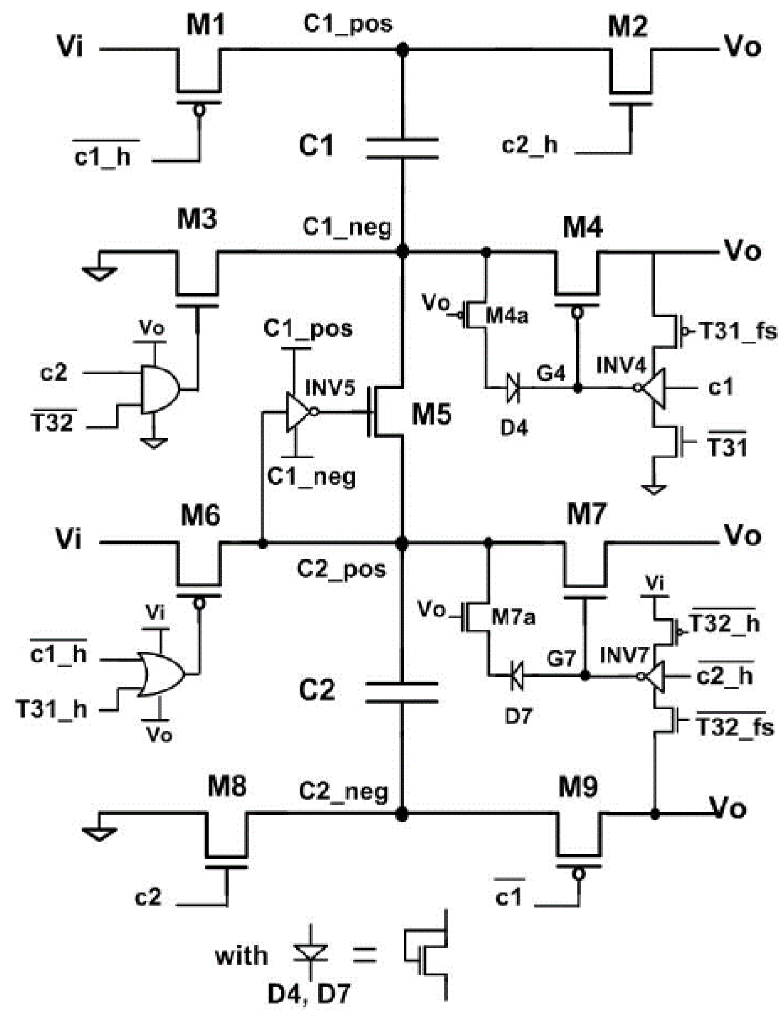
Maxwell, PC10
C_{SUP}=10F



[2] Sanchez' 10 VLSI

Prior Work & State of the Art (II)

- **Switched-capacitor DC-DC**
  - **V_{IN} = 2V, V_{OUT}=0.4-2.1V**
  - **Reconfigurable (3 modes)**
  - **Only step-down modes**
    - K=1/3, 1/2, 2/3

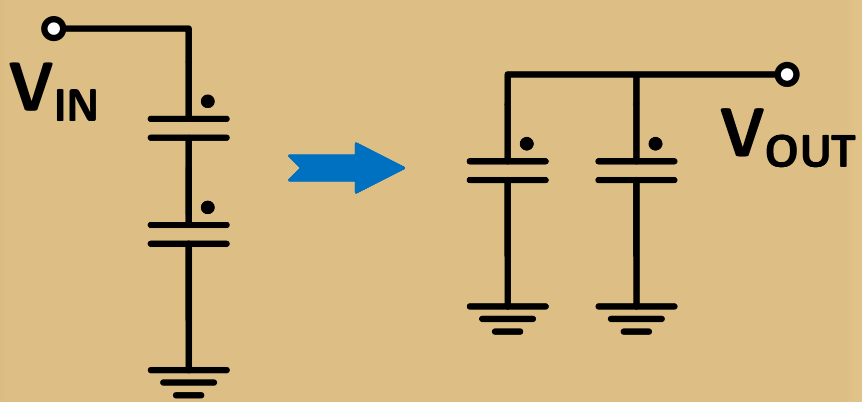


[3] Le'10 ISSCC

Switched-Capacitor DC-DC Converter

- Conversion ratio (1/2 and 2X) decided by mode

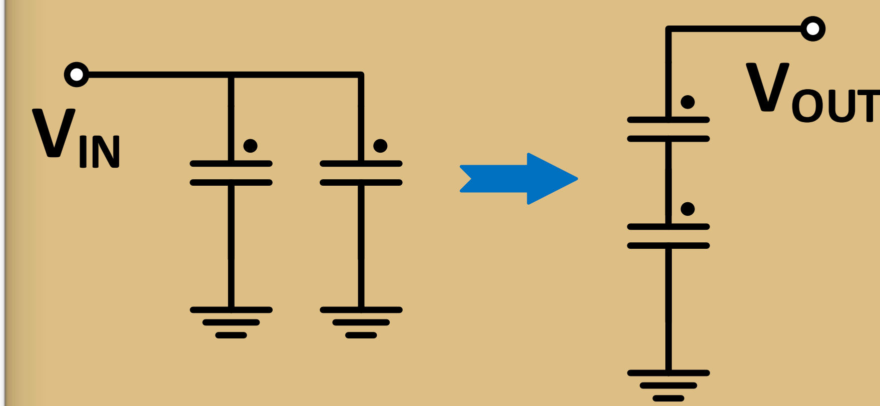
$V_{OUT} = ½ V_{IN}$
(Buck)



Phase 1
(Φ1)

Phase 2
(Φ2)

$V_{OUT} = 2 V_{IN}$
(Boost)



Phase 1
(Φ1)

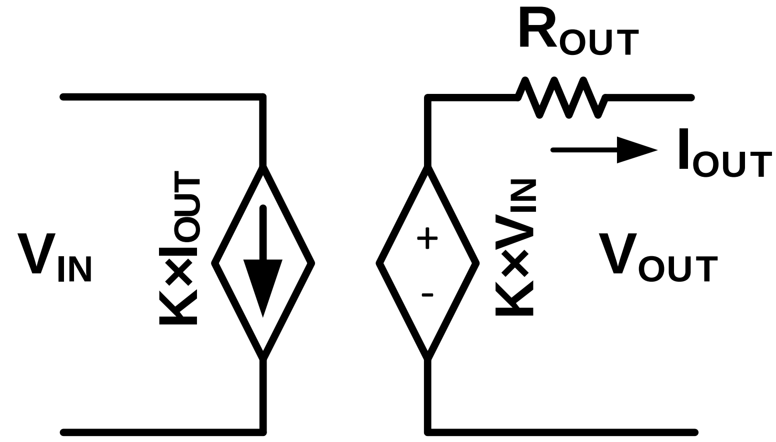
Phase 2
(Φ2)

Switched-Capacitor DC-DC Converter

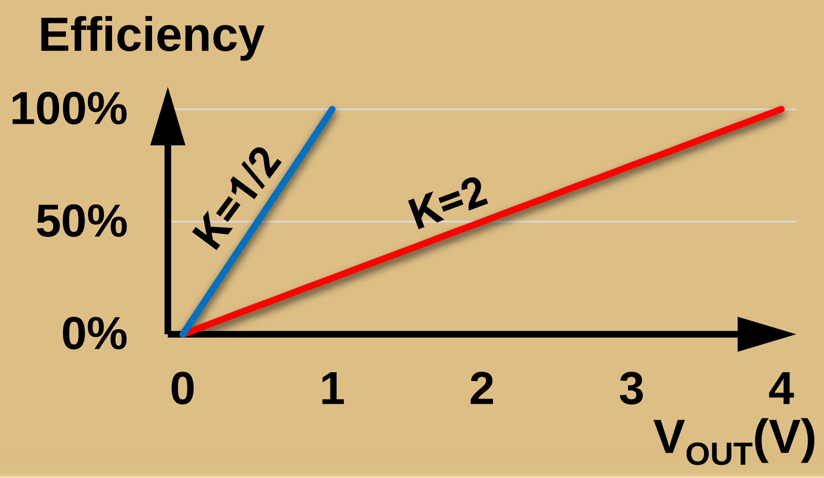
- **Dominant loss mechanism**
  - **Conduction loss**

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} I_{OUT}}{V_{IN} I_{IN}} = \frac{V_{OUT}}{K \cdot V_{IN}}$$

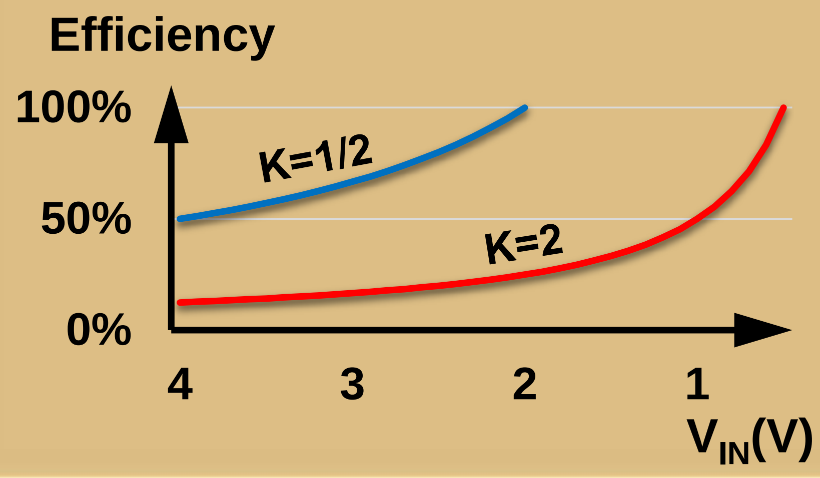
$$\boxed{\eta = \frac{V_{OUT}}{V_{\max}}}$$



Fixed V_{IN}=2V



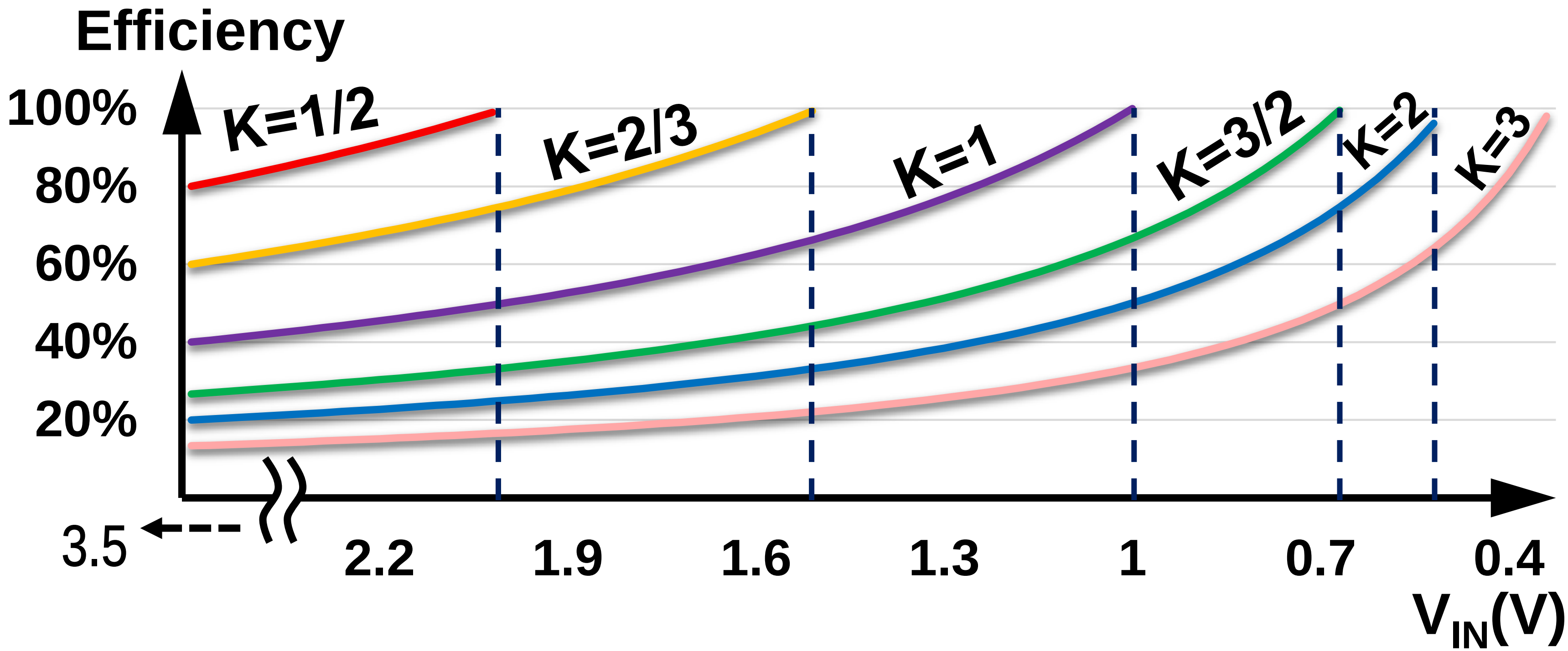
Fixed V_{OUT}=1V



SC DC-DC Converter: Reconfigurable

- **Efficiency loss mechanisms**
  - Dominant → Conduction loss
  - Bottom plate loss → process
  - Switch loss
  - Control circuit overhead

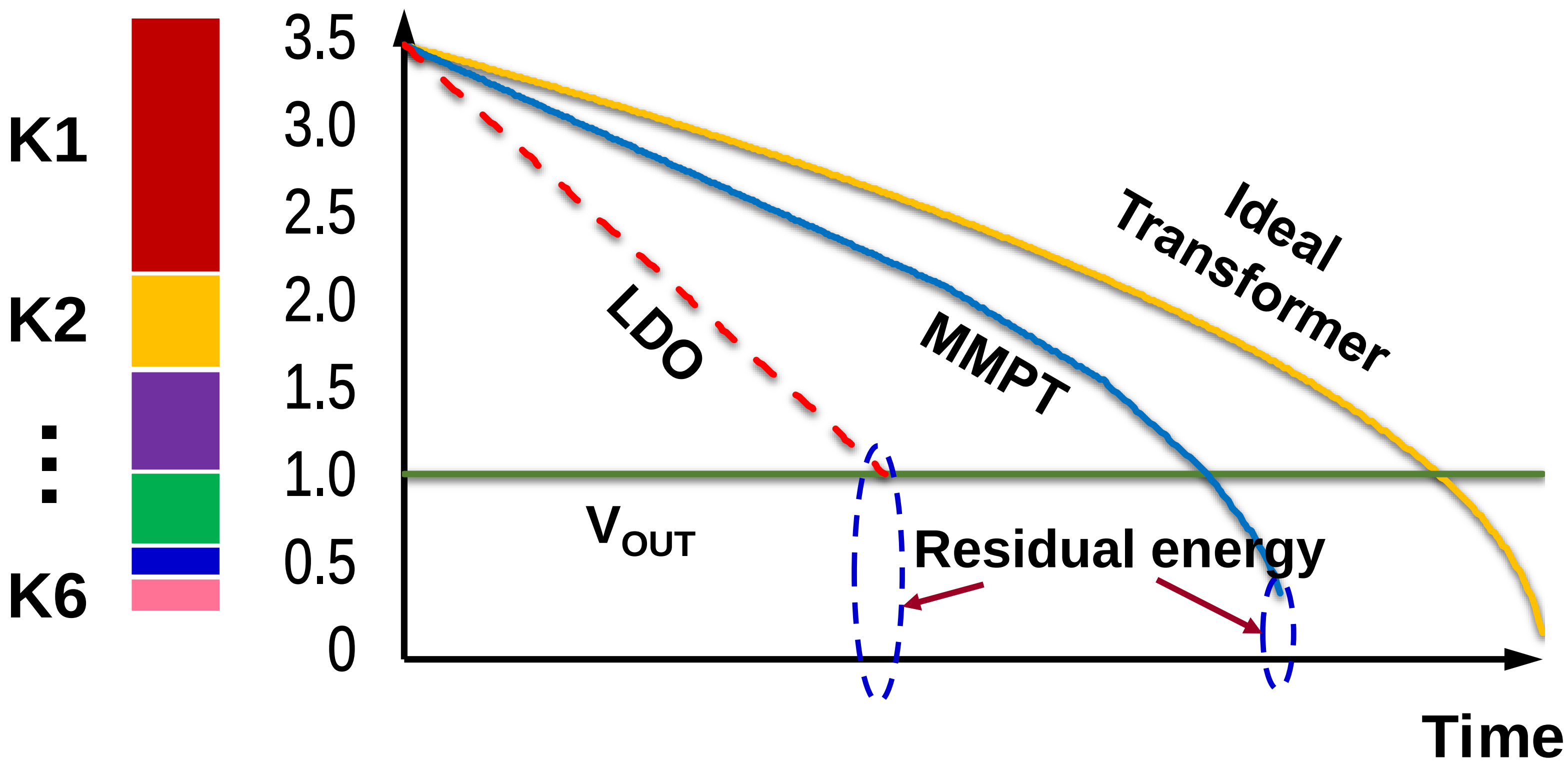
$$\eta = \frac{V_{OUT}}{K \cdot V_{IN}}$$



Multi-Mode Power Transformer (MMPT)

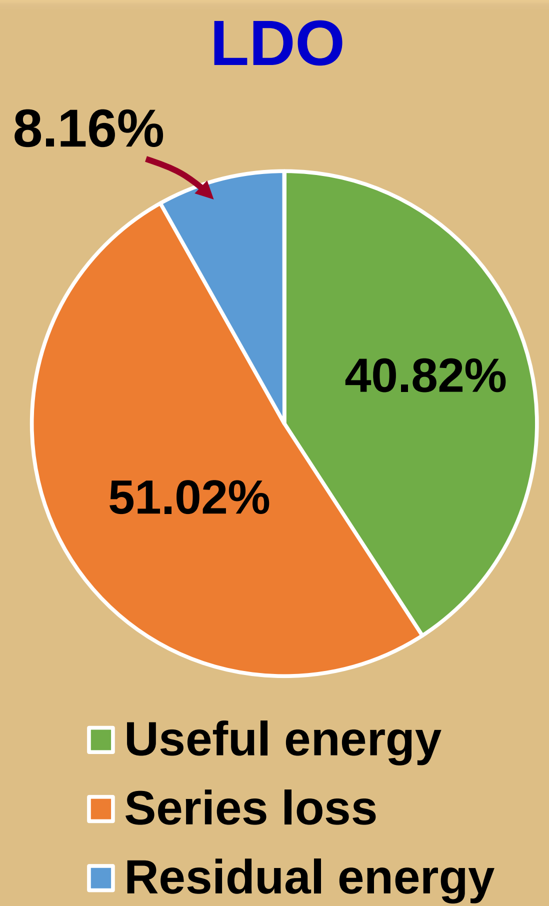
- Reconfigurable (6 modes)
  - SC converter based
- η limited by conduction loss

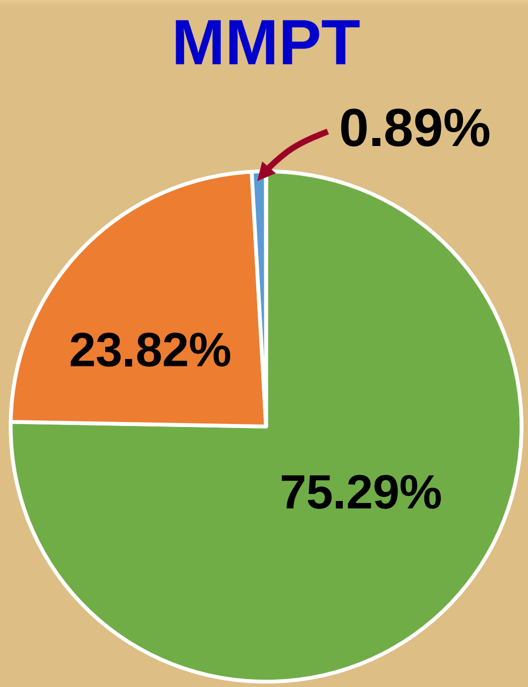
K1	K2	K3	K4	K5	K6
1/2	2/3	1	3/2	2	3



Energy Usage comparison

- MMPT has potential to nearly double operational time



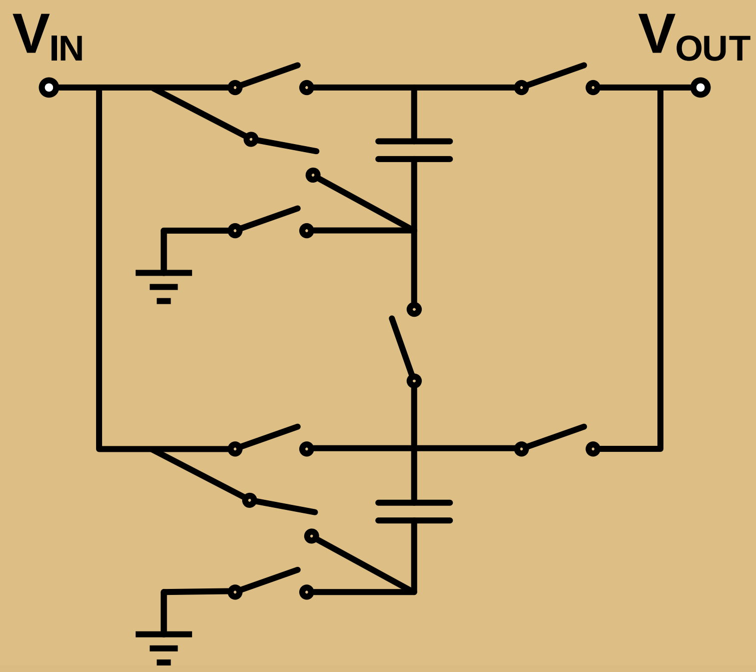


- Residual energy is 10 times less
- Useful energy is nearly doubled

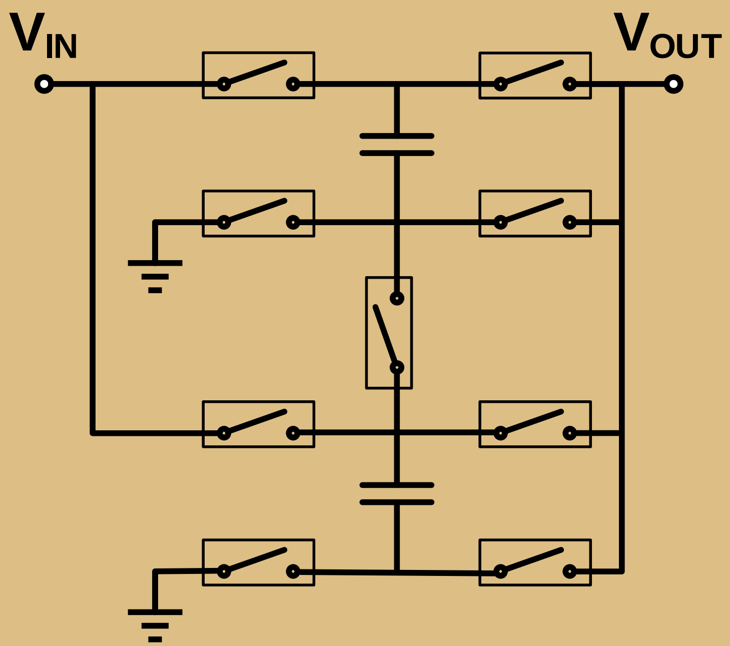
MMPT Implementation: K2 —— K6

- Reconfigurable (2 circuits cover 5 modes of operation)

Boost converter
V_{IN}=1~0V
K=3/2, 2, 3
Core device

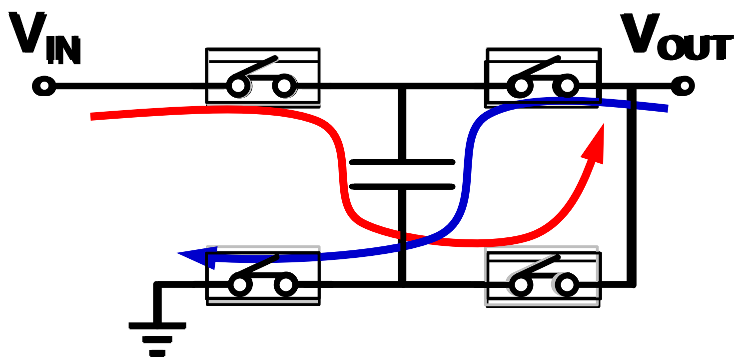


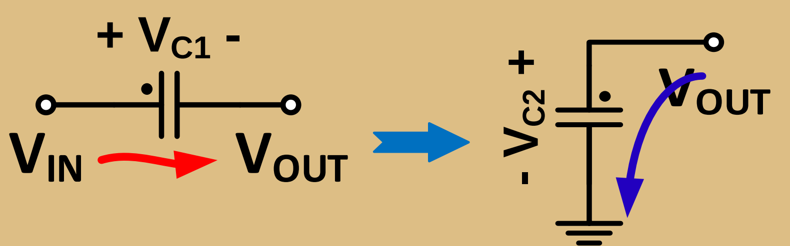
Buck converter
V_{IN}=2~1V
K=2/3, 1
I/O device



MMPT Implementation: K1

- I/O devices are not sufficient for highest input (3.5V)
  - How to implement switches?
  - How to drive switches?





Phase 1
(Φ1)

Phase 2
(Φ2)

$$V_{C1} = V_{IN} - V_{OUT}$$

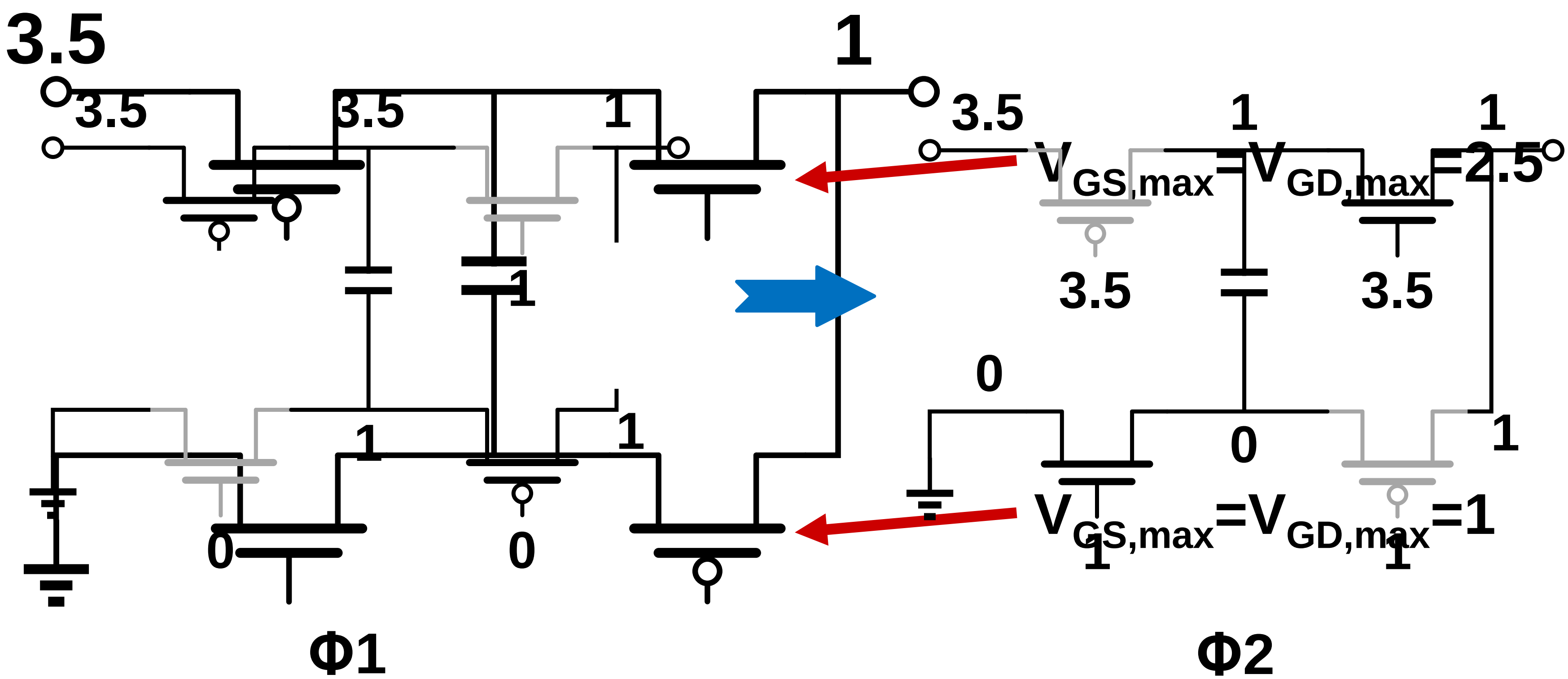
$$V_{C2} = V_{OUT}$$

$$V_{C1} = V_{C2}$$

$$V_{OUT} = \frac{1}{2} V_{IN}$$

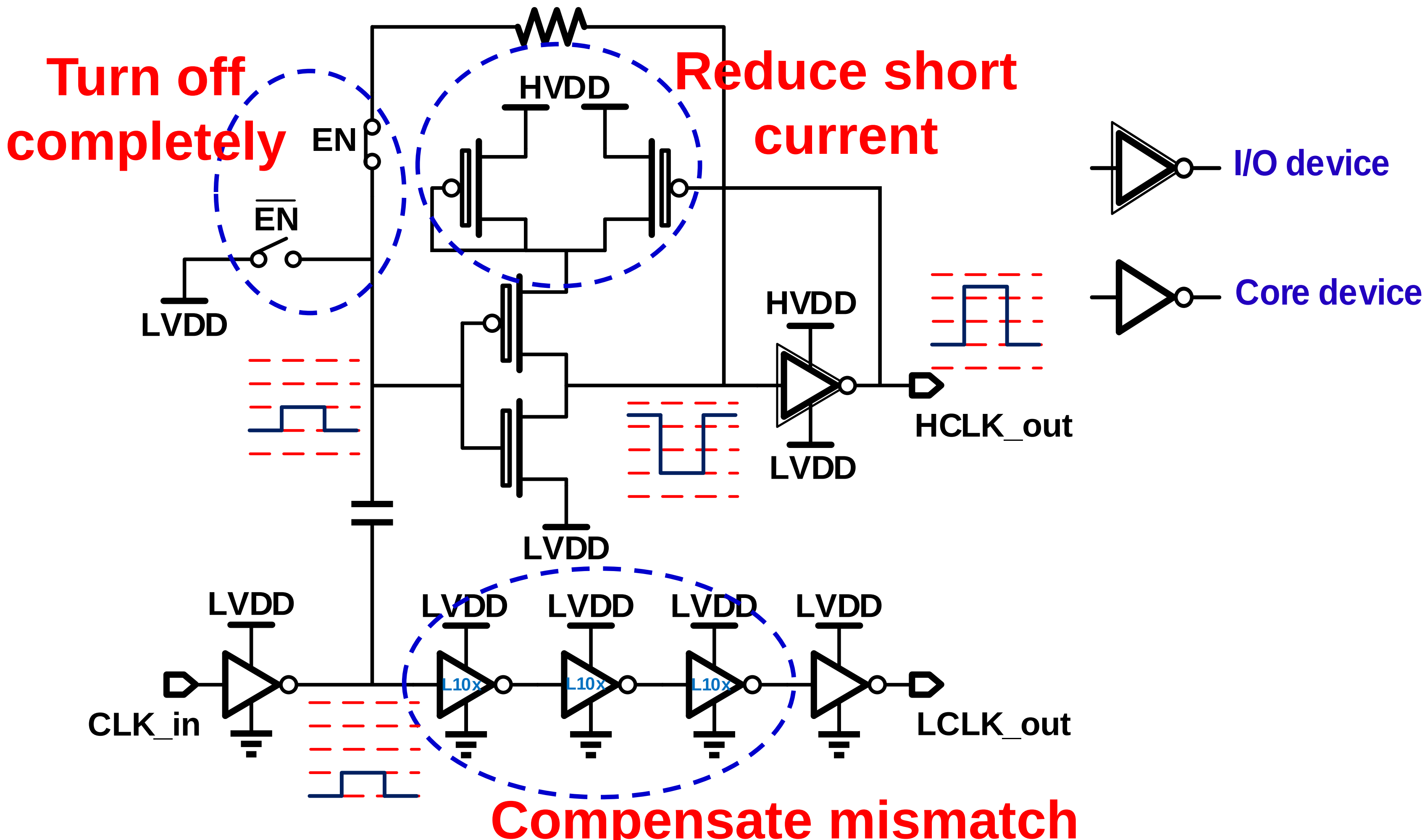
Voltage Protection: SC-Core

- Buck Converter
  - Switch drivers are not fully scaled toggle
  - Switches only “see” V_{IN}-V_{OUT} between nodes



Voltage Protection: High Voltage Clock

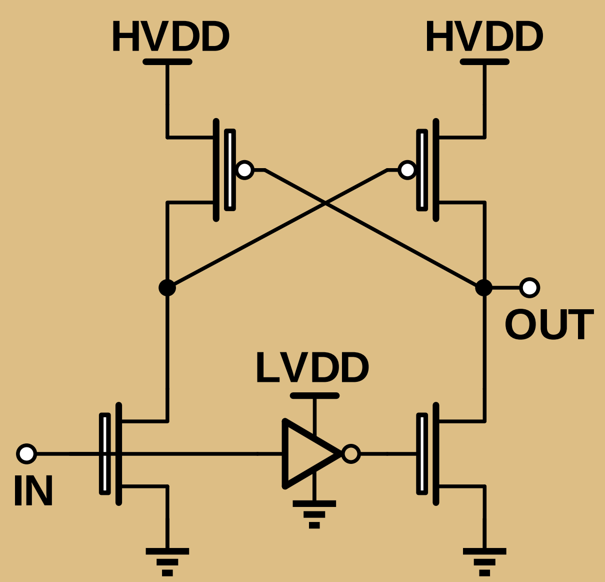
- Proposed AC coupled level shifter for HV clock



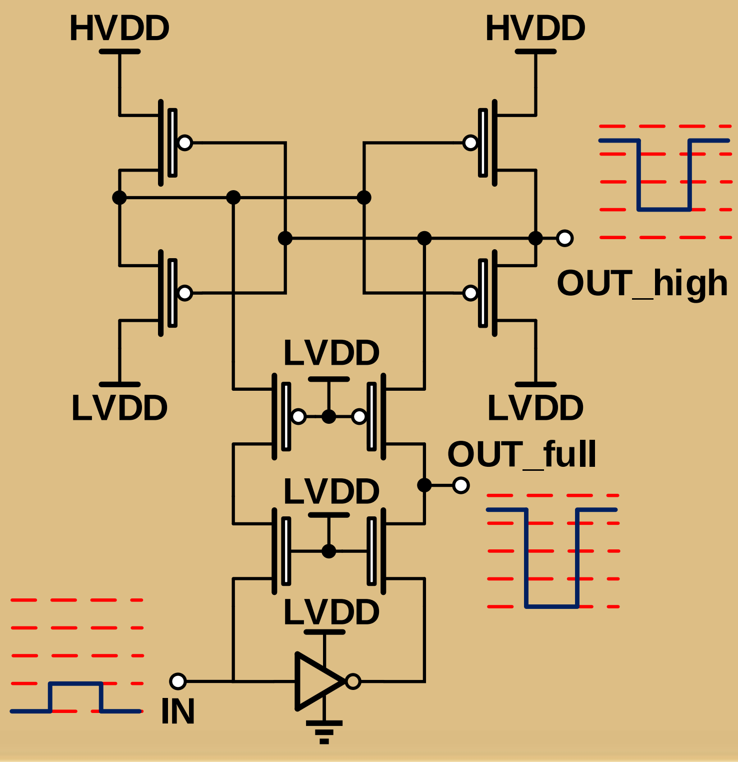
Voltage Protection: Level Shifter

- Full scale level shifter for control circuit
  - Also need voltage protection
  - Used in Mode selector & control loop

Conventional Level-Shifter

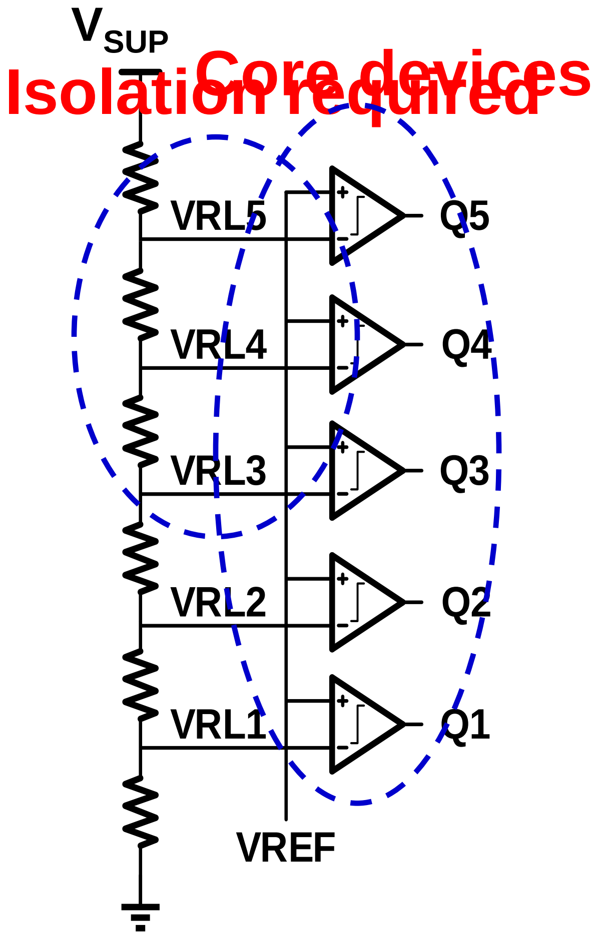


Proposed Level-Shifter

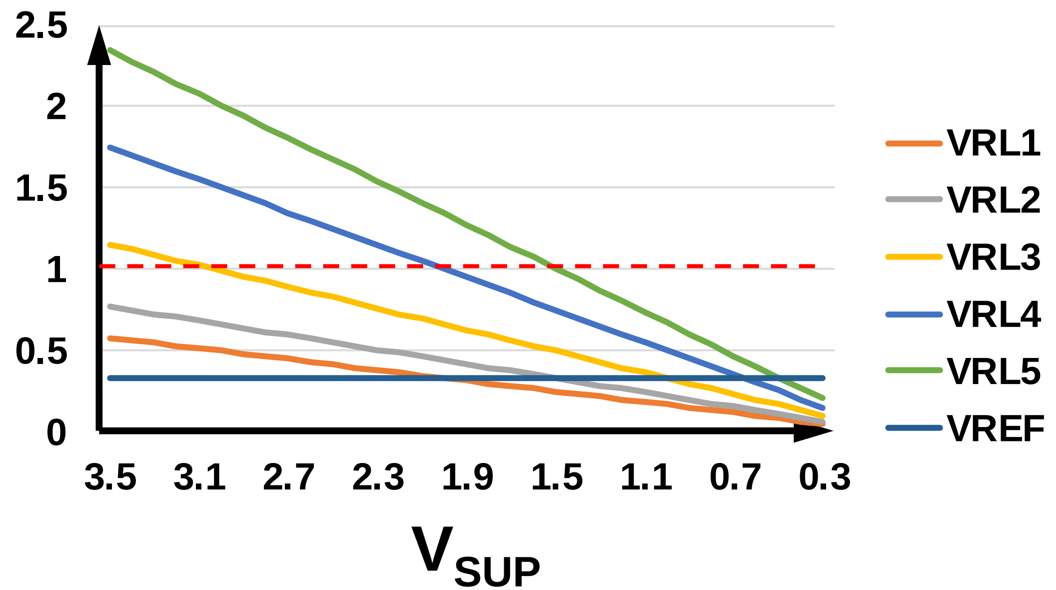


Voltage Protection: Mode Selector ADC

- Comparator



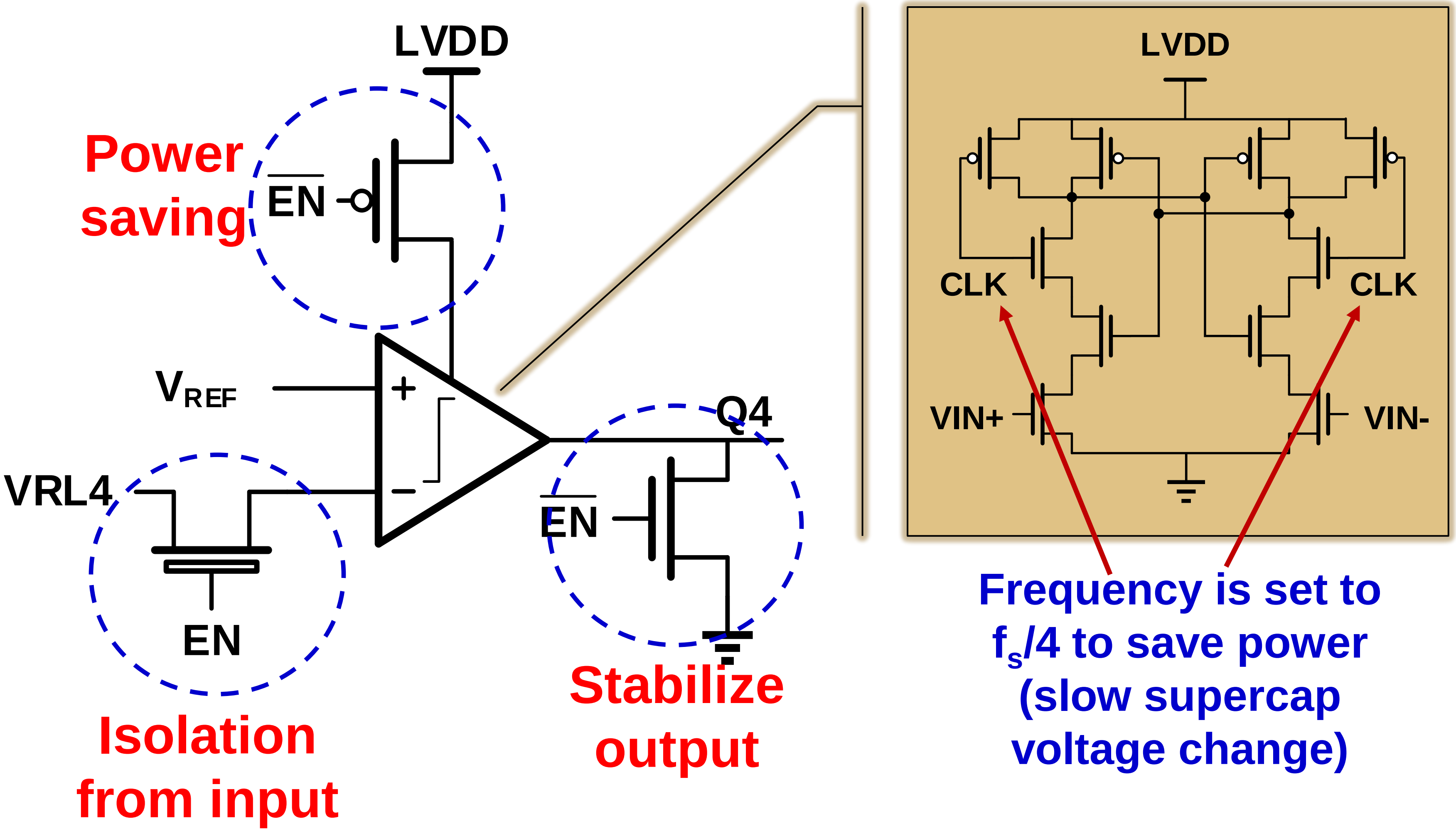
	K1	K2	K3	K4	K5	K6
Ratio	1/2	2/3	1	3/2	2	3
Turning Point (V)	2	1.5	1	0.67	0.5	x



Voltage Protection: Comparator

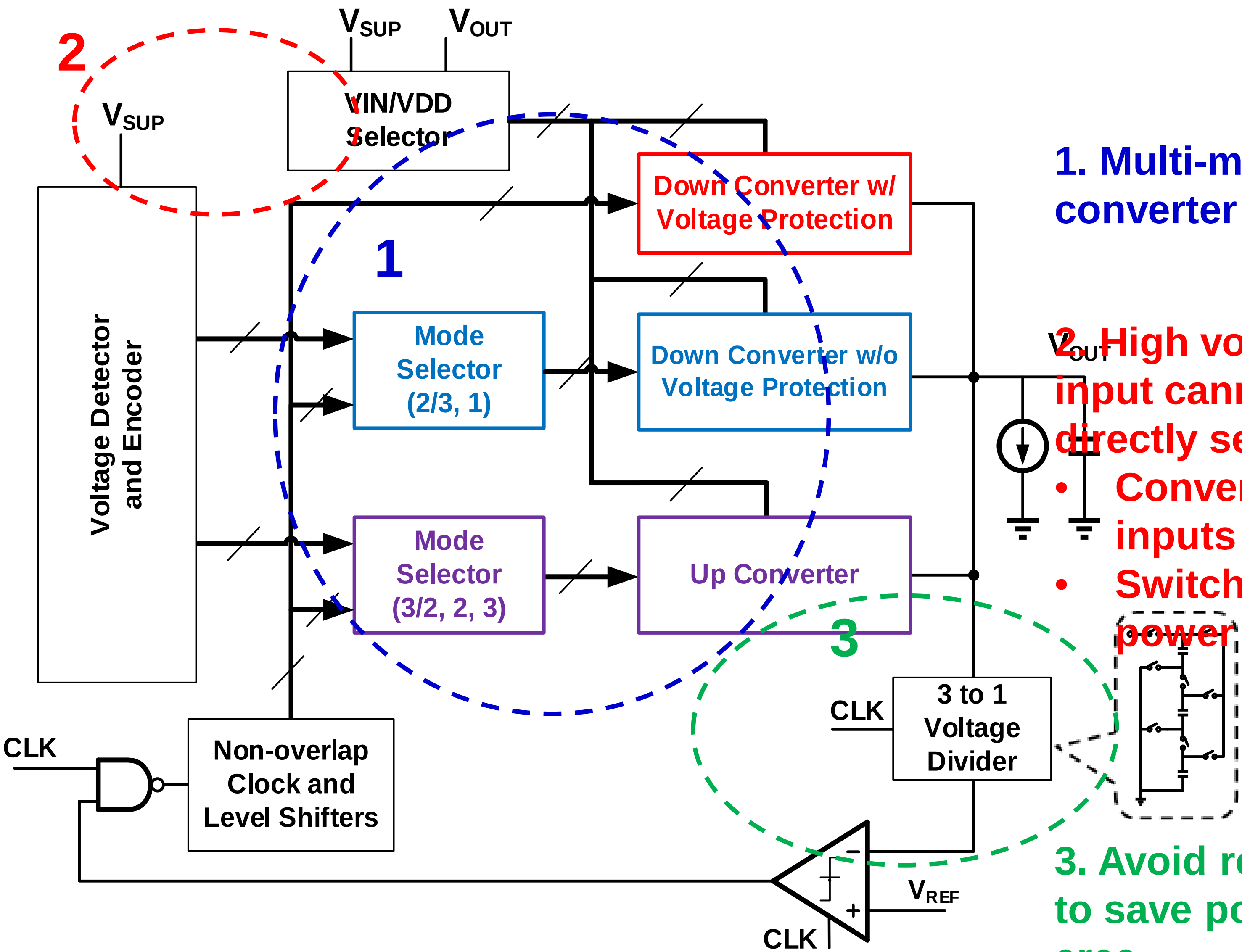
- Comparator

Conventional clocked strong-arm comparator



Frequency is set to $f_s/4$ to save power (slow supercap voltage change)

Overall Circuit Block Diagram



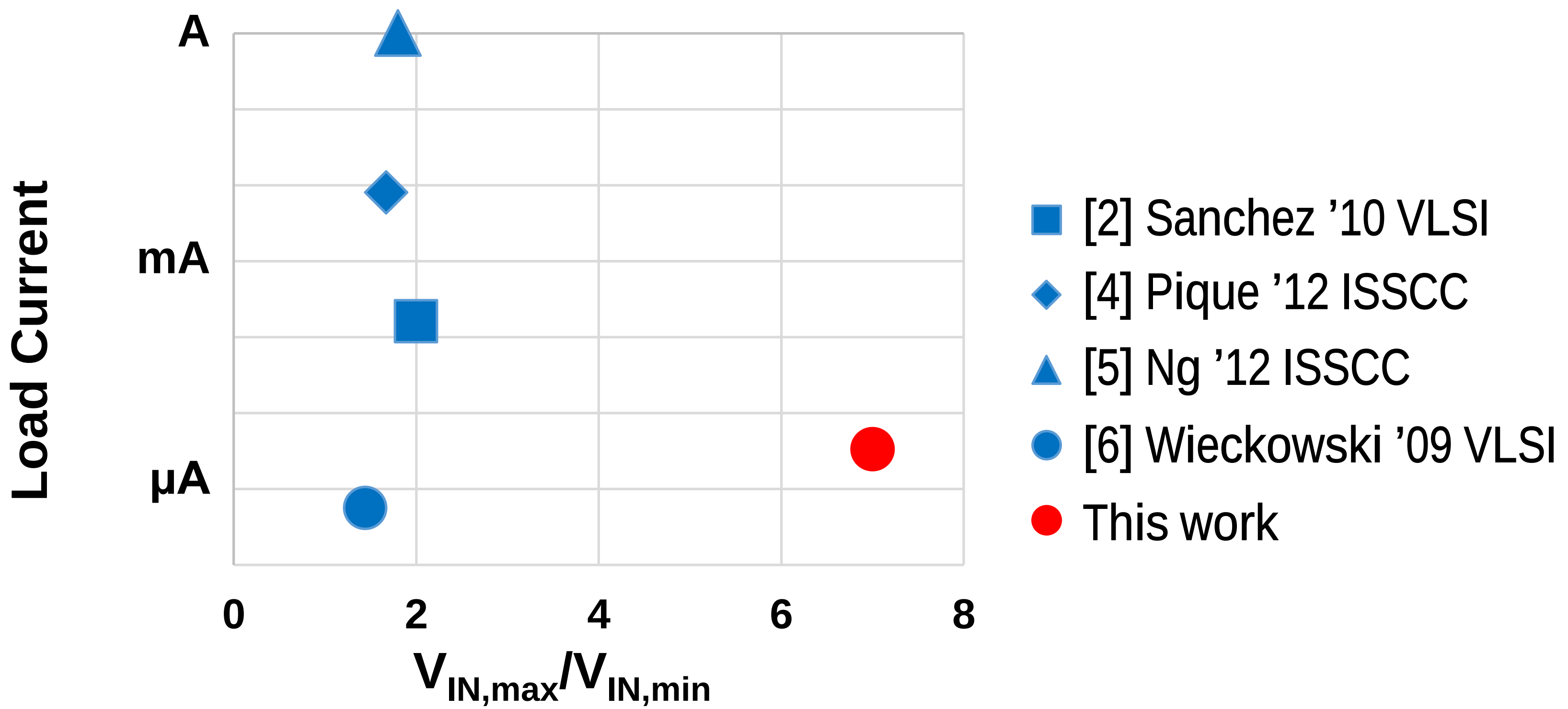
1. Multi-mode converter core

2. High voltage input cannot directly send to:
- Converter inputs
- Switch driver power supply

3. Avoid resistors to save power and area

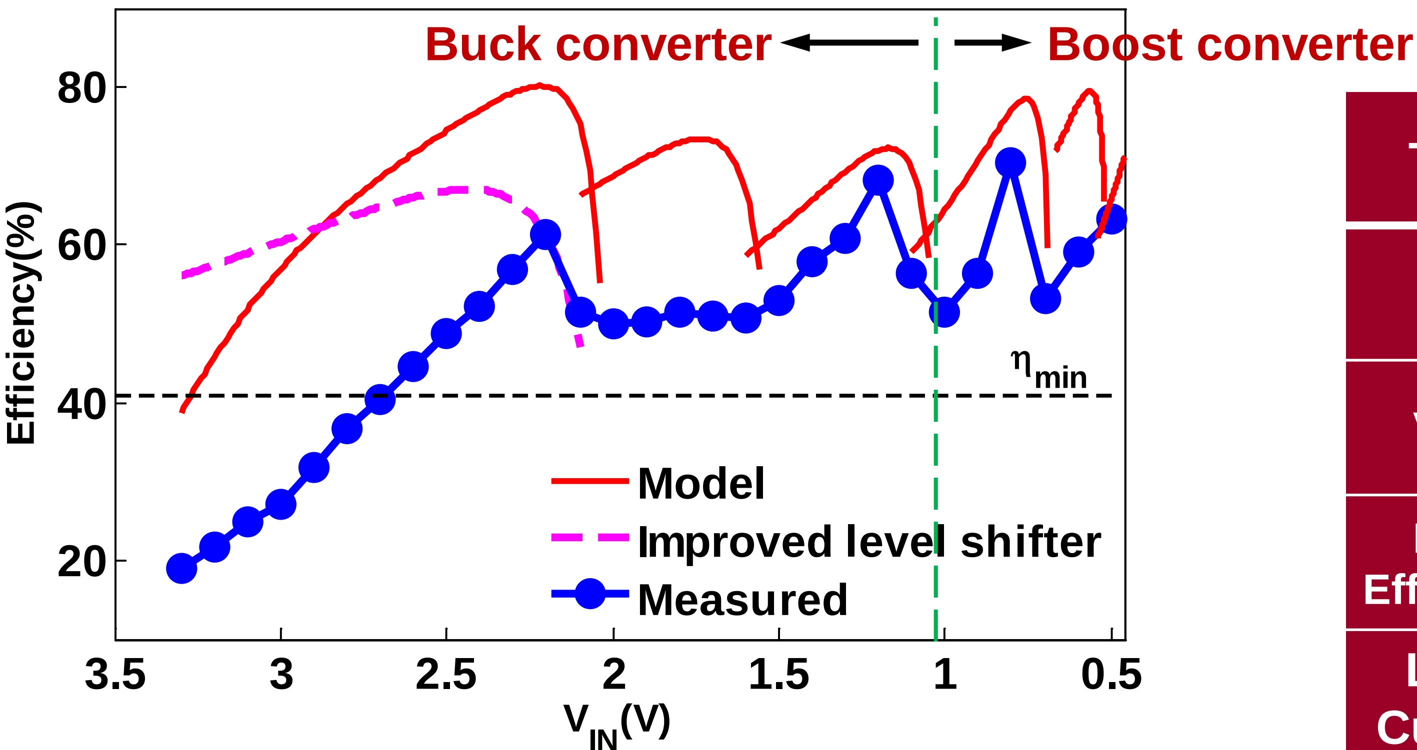
Comparison: Input Voltage Range

- Conversion ratio → largest $V_{IN,max}$ to $V_{IN,min}$ ratio
- Buck/boost → minimum residual energy lost
- Load current → lowest load current (everything matters)



Prototype design: Efficiency

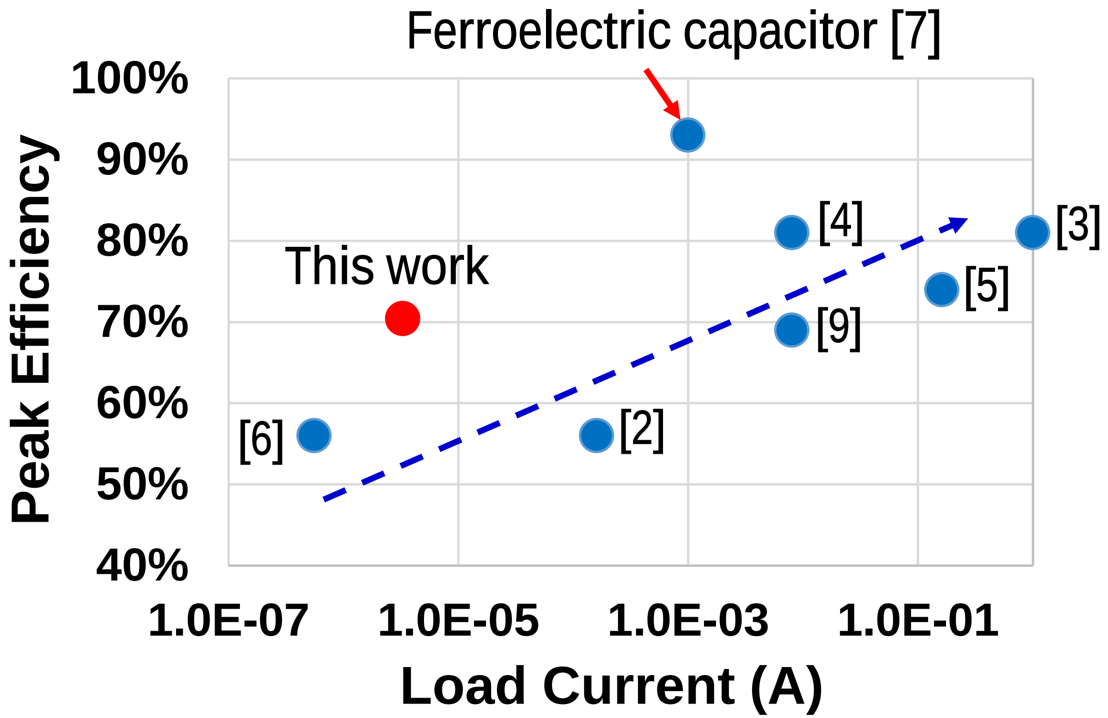
- Measured efficiency v.s. V_{IN}
- Lower efficiency at high V_{IN} than expected
  - Voltage protected level shifter leakage → can be improved

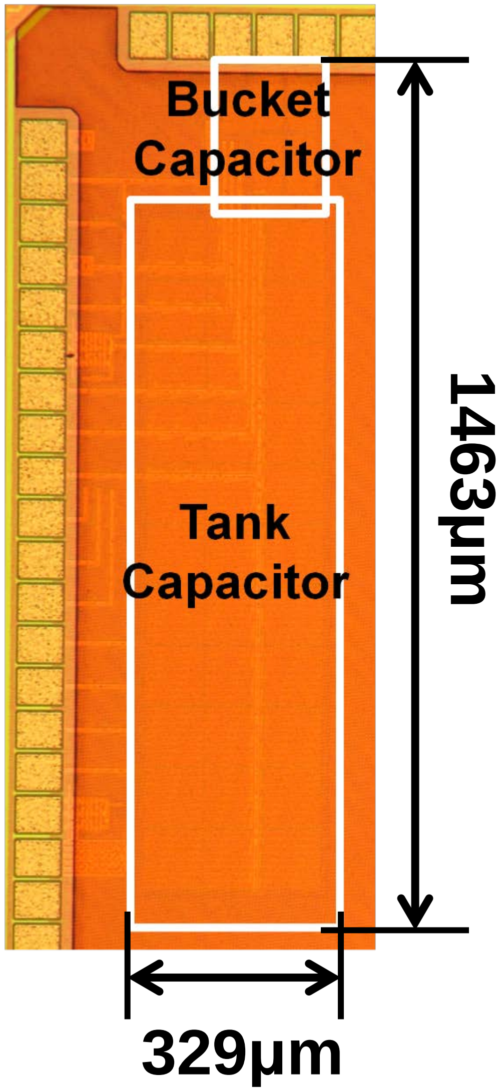


Tech	65nm
V_{IN}	3.5~0.5V
V_{OUT}	1.0V
Peak Efficiency	70.4%
Load Current	3μA

Comparison

- **High efficiency is difficult at small loads**





[7] El-Damak '13 ISSCC

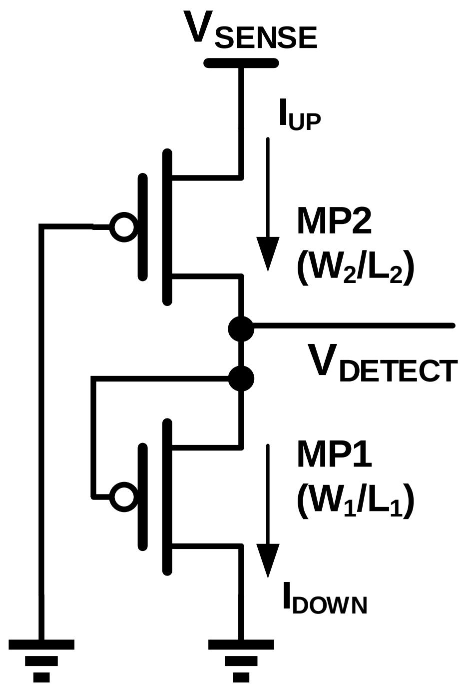
Summary & Conclusion

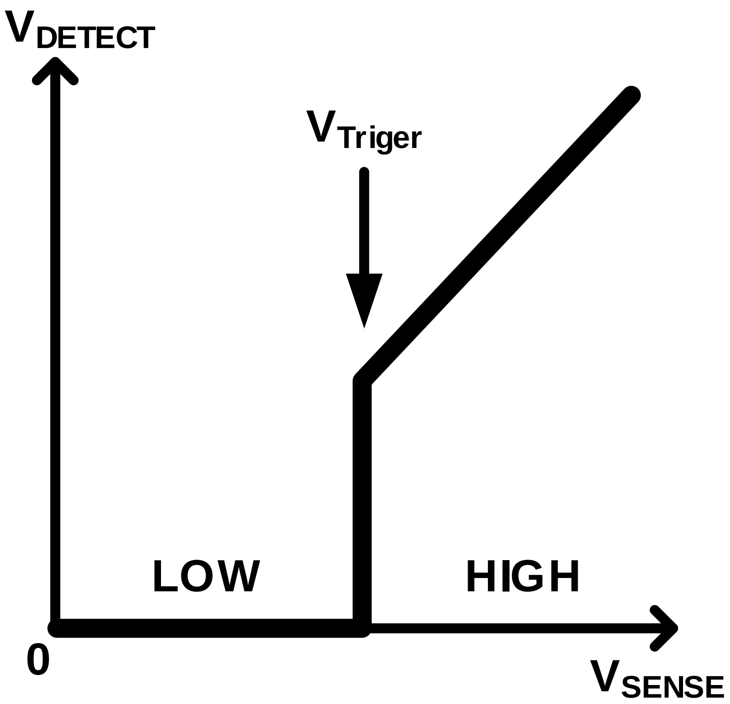
- Extend technology breakdown voltage
  - $V_{IN,max}$: 2.5V → 3.5V
  - Storage power increase 96% (V^2)
- Extract over 98% of energy in supercap
  - $V_{IN,min}$: 1.0V → 0.5V
- Usage time is nearly doubled
  - Useful energy: 40.8% → 75.3%
- Application → low power RFID for blood bags
  - I_{LOAD} = 3μA
- Require only one off-chip supercap
- Both buck & boost
- Techniques also useful for other application

Thank You & Questions

University of Minnesota

Start-up Circuits



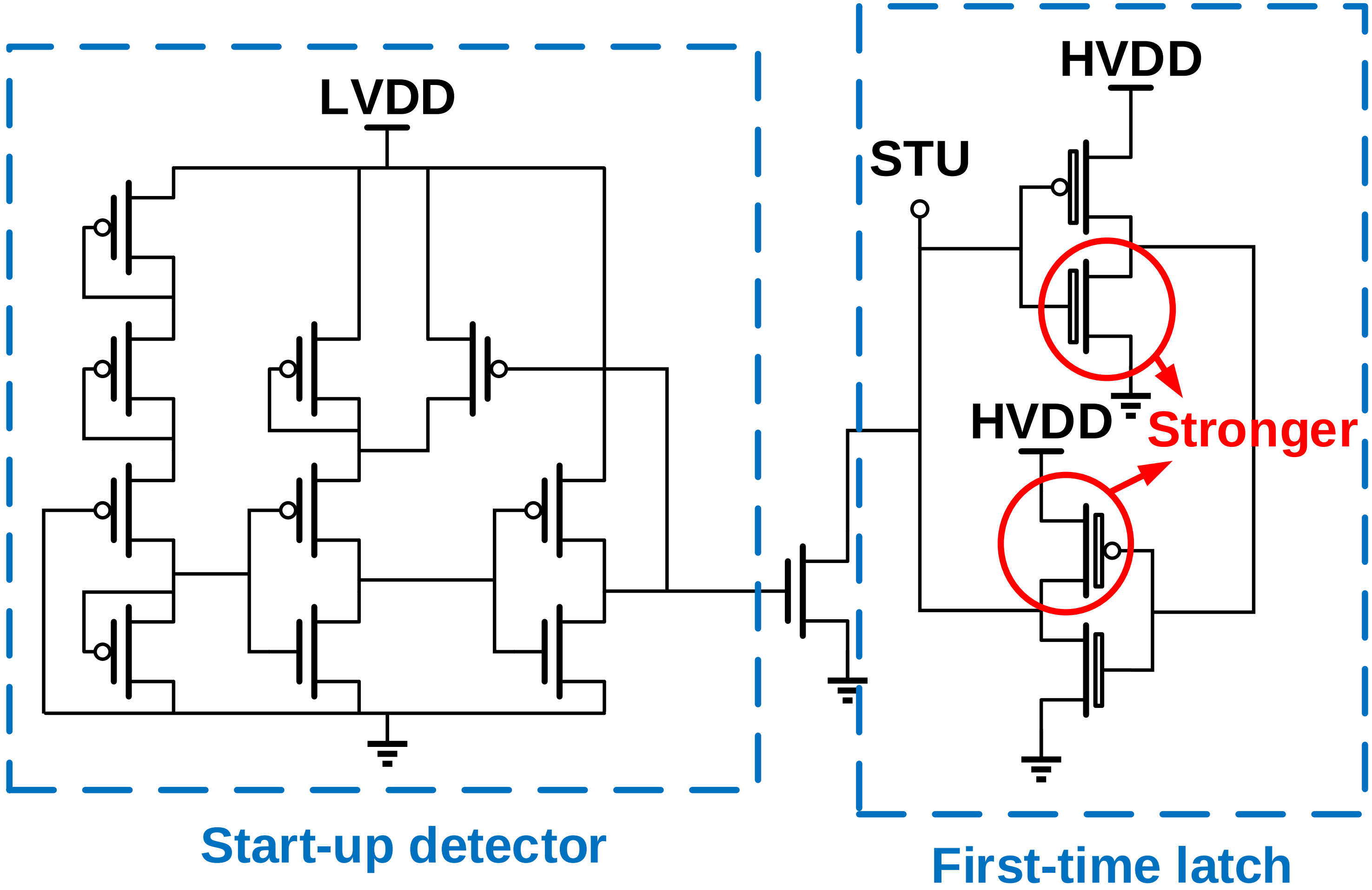


$$I_{UP} = K\frac{W_2}{L_2}e^{\frac{V_{SENSE}-V_{TH}}{mkT/q}}$$

$$I_{DOWN} = K\frac{W_1}{L_1}e^{\frac{-V_{TH}}{mkT/q}}$$

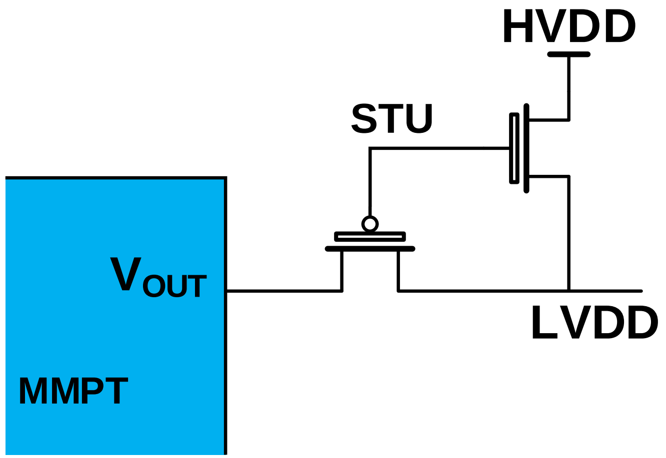
$$V_{Trigger} = \frac{mkT}{q}ln\left(\frac{W_1}{W_2} \times \frac{L_2}{L_1}\right)$$

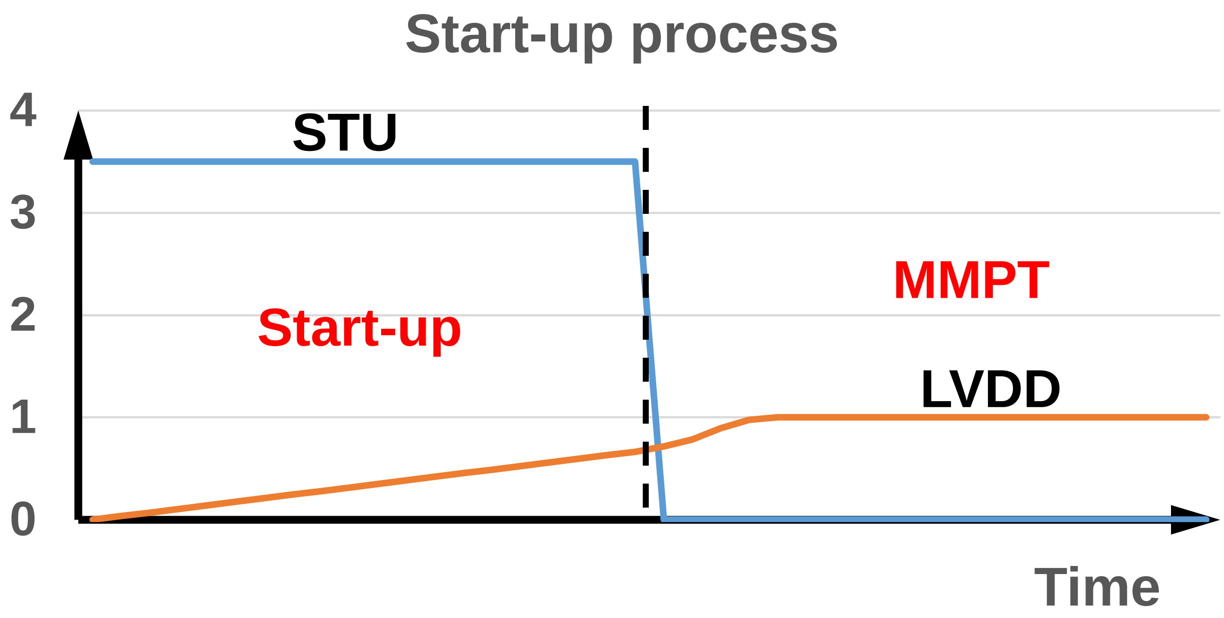
Start-up Circuits



Start-up Circuits

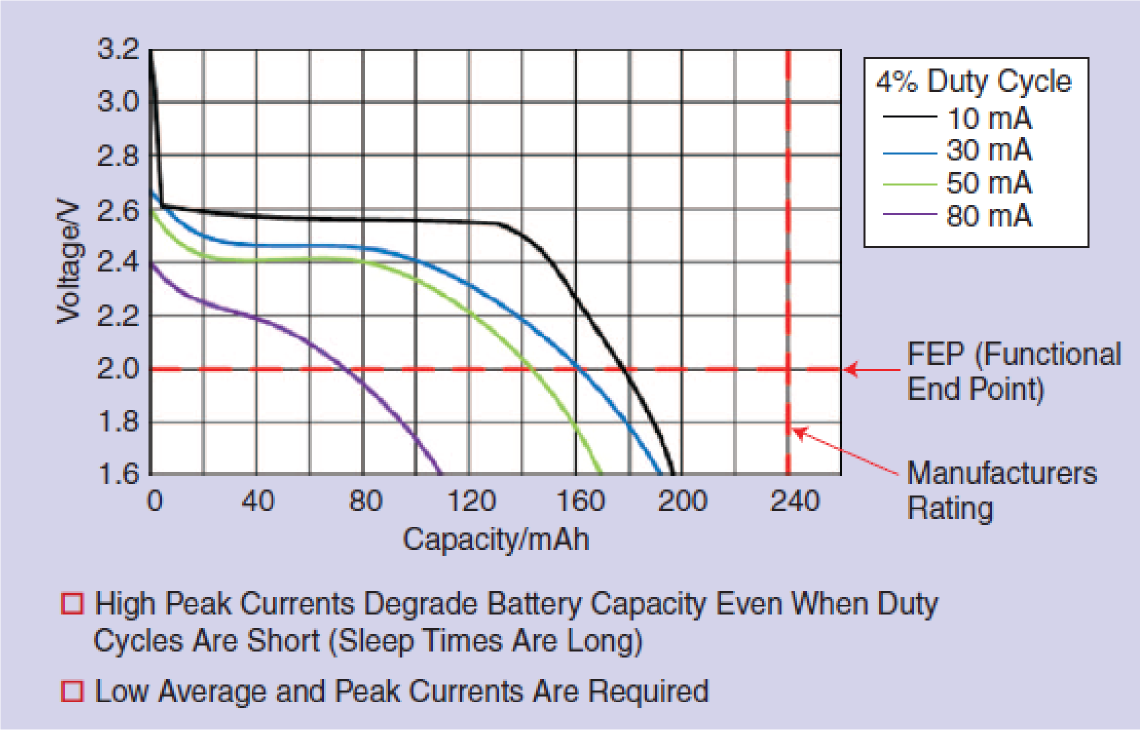
- Accumulate
- Detect
- Hand-over





Battery Voltage Droop

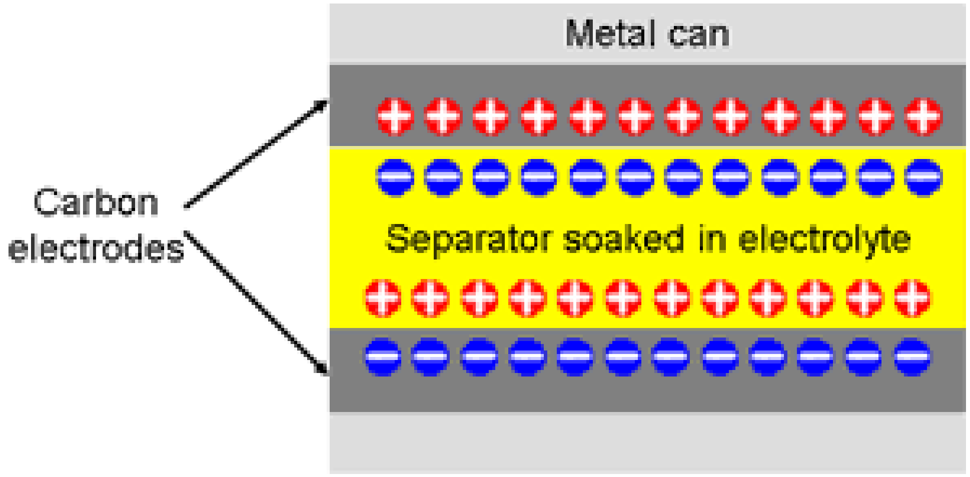
- **Discharge curve**
  - **Supercap: VSUP=Q/CSUP**
  - **Battery: also not constant for large load**



[8] Toumaz '13 SSC

What is supercapacitor

- **Electrochemical double-layer capacitors (EDLC)**
  - **Two carbon electrodes**
  - **Organic electrolyte**
  - **Phenomenon of “double-layer”**

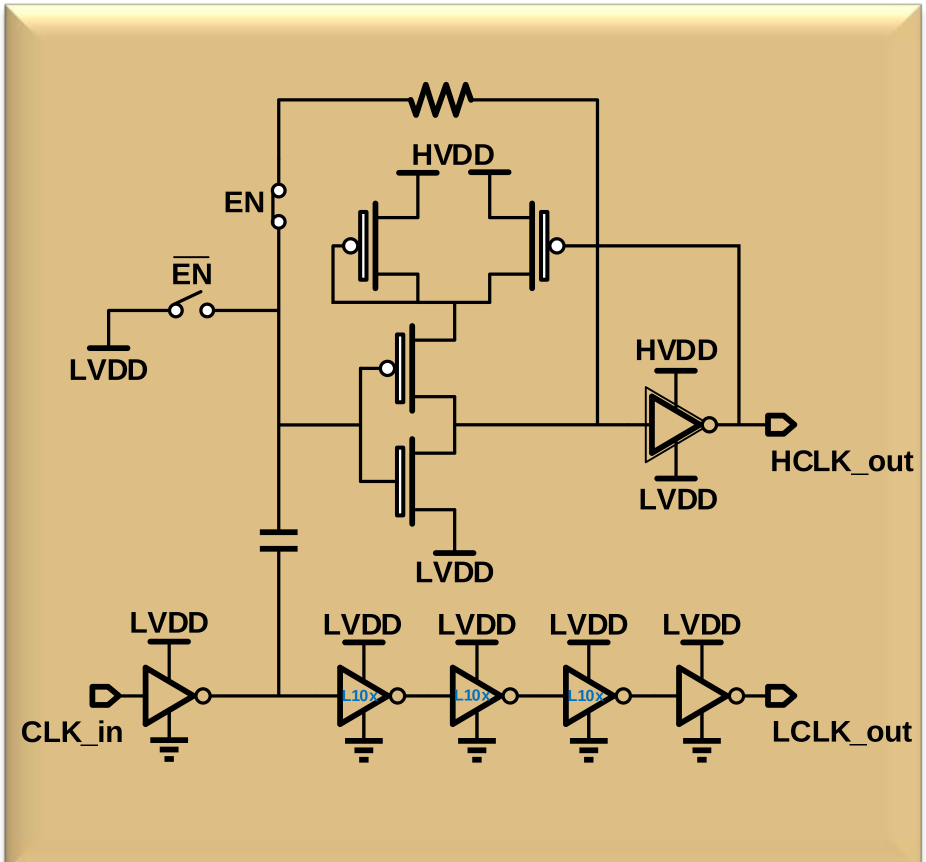


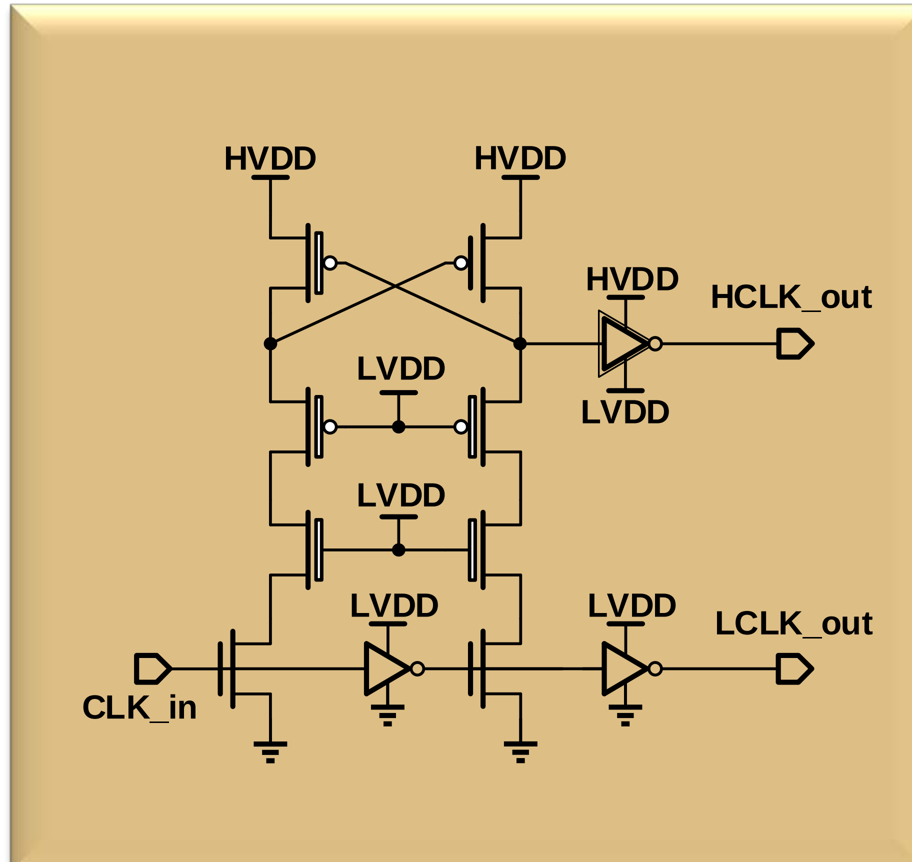
Double Layer Capacitor

[10] Electrooaedia/Batterry and Energy Technologies

Voltage protection level shifter

- **High leakage for high input voltage**
  - Can be improved to the right-hand-side one





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- [2] Sanchez, William, Charles Sodini, and Joel L. Dawson. "An energy management ic for bio-implants using ultracapacitors for energy storage." VLSI 2010.
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- [4] Pique, Gerard Villar. "A 41-phase switched-capacitor power converter with 3.8 mV output ripple and 81% efficiency in baseline 90nm CMOS." ISSCC 2012.
- [5] Ng, Vincent, and Seth Sanders. "A 92%-efficiency wide-input-voltage-range switched-capacitor DC-DC converter." ISSCC 2012.
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- [7] El-Damak, Dina, Supriyo Bandyopadhyay, and Anantha P. Chandrakasan. "A 93% efficiency reconfigurable switched-capacitor DC-DC converter using on-chip ferroelectric capacitors." ISSCC 2013.
- [8] Burdett, Alison. "Ultra-Low-Power Wireless Systems: Energy-Efficient Radios for the Internet of Things." Solid-State Circuits Magazine, IEEE 7.2 (2015): 18-28.
- [9] Ramadass, Yogesh, et al. "A 0.16mm^2 Completely On-Chip Switched-Capacitor DC-DC Converter Using Digital Capacitance Modulation for LDO Replacement in 45nm CMOS" ISSCC 2010.
- [10] http://www.mpoweruk.com/supercaps.htm