CICC 2015
Session 18.2

A Flash-Based Non-Uniform Sampling ADC Enabling Digital Anti-Aliasing Filter in 65nm CMOS

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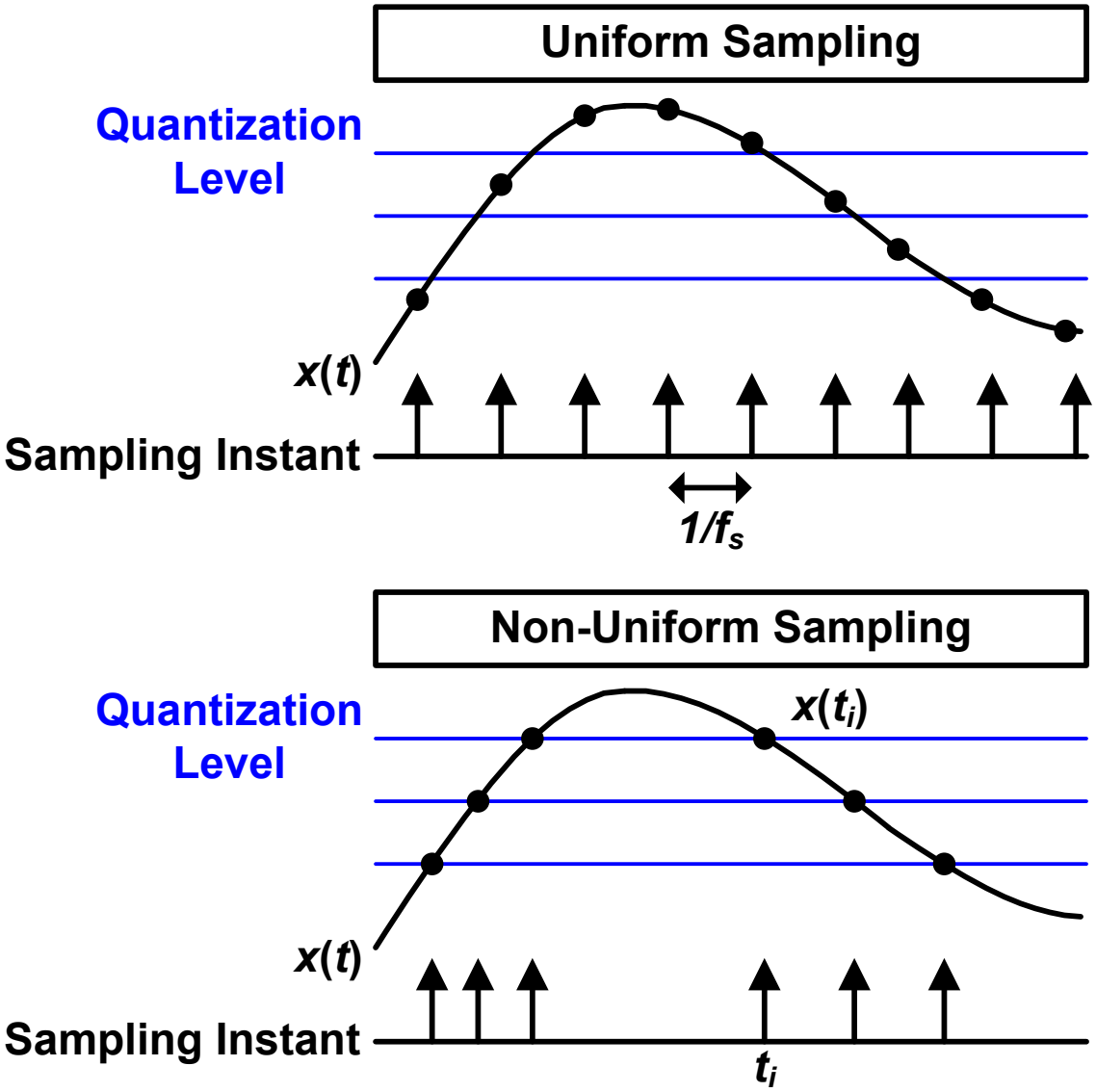
Outline

- Motivation
- ADC Implementation
  - Voltage Quantizer
  - Time Quantizer
- Measurement Results
- Conclusion

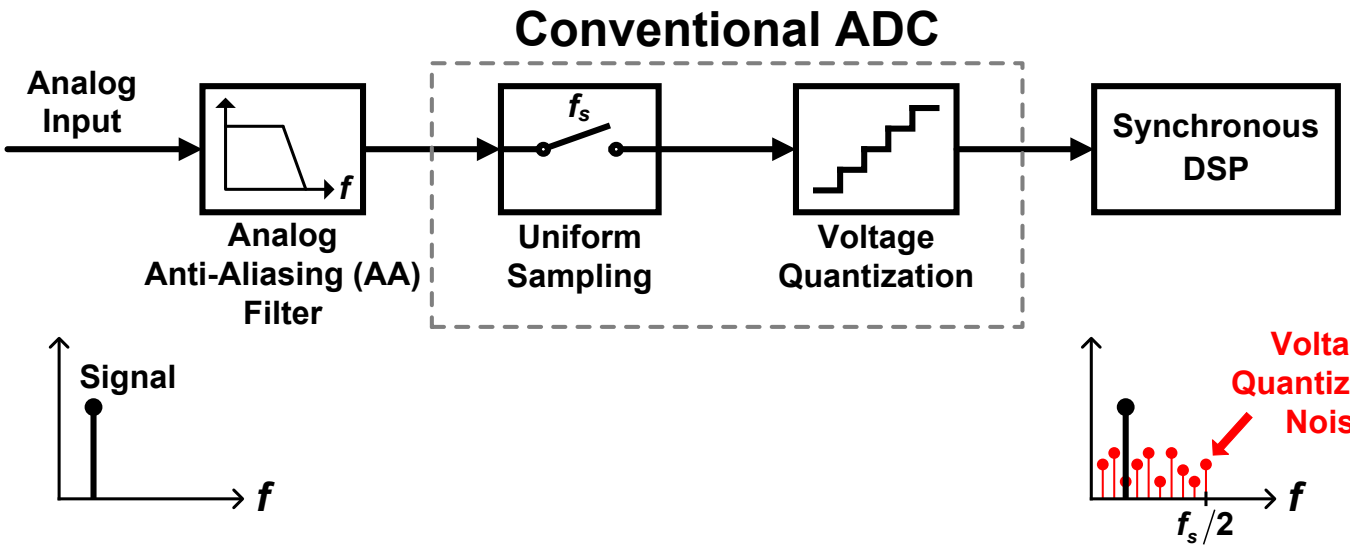
Uniform vs. Non-Uniform Sampling



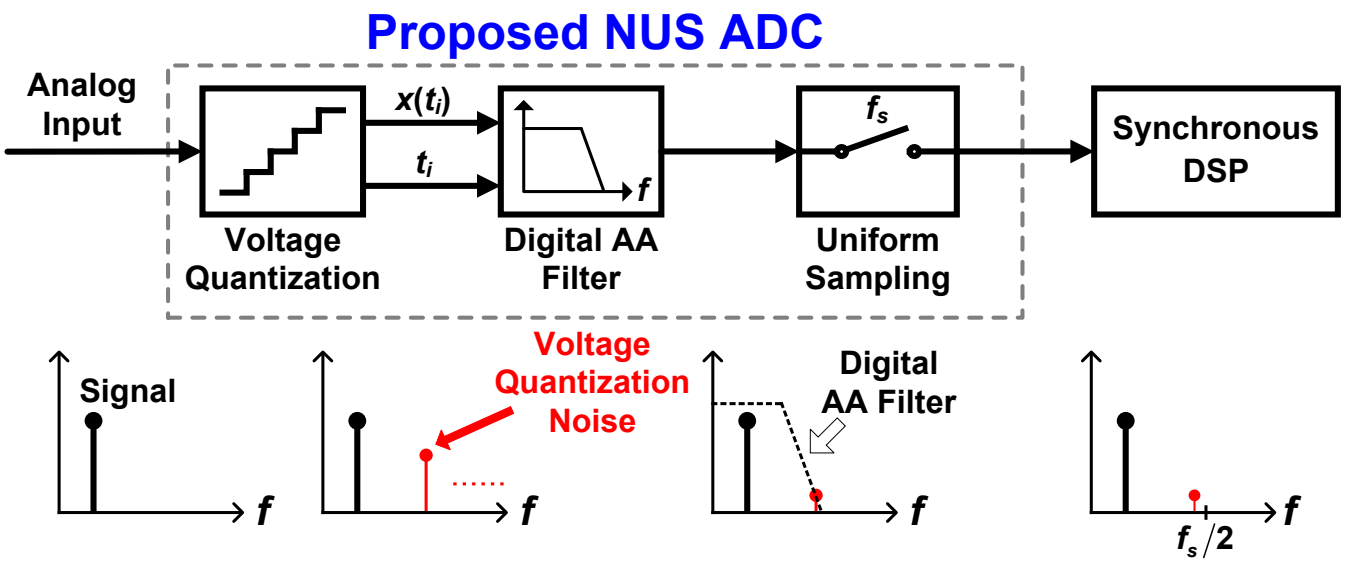
Fixed Clock Frequency
➔ Spectral Aliasing

No Clock
➔ Alias-Free
➔ Event-Driven

ADC Architecture



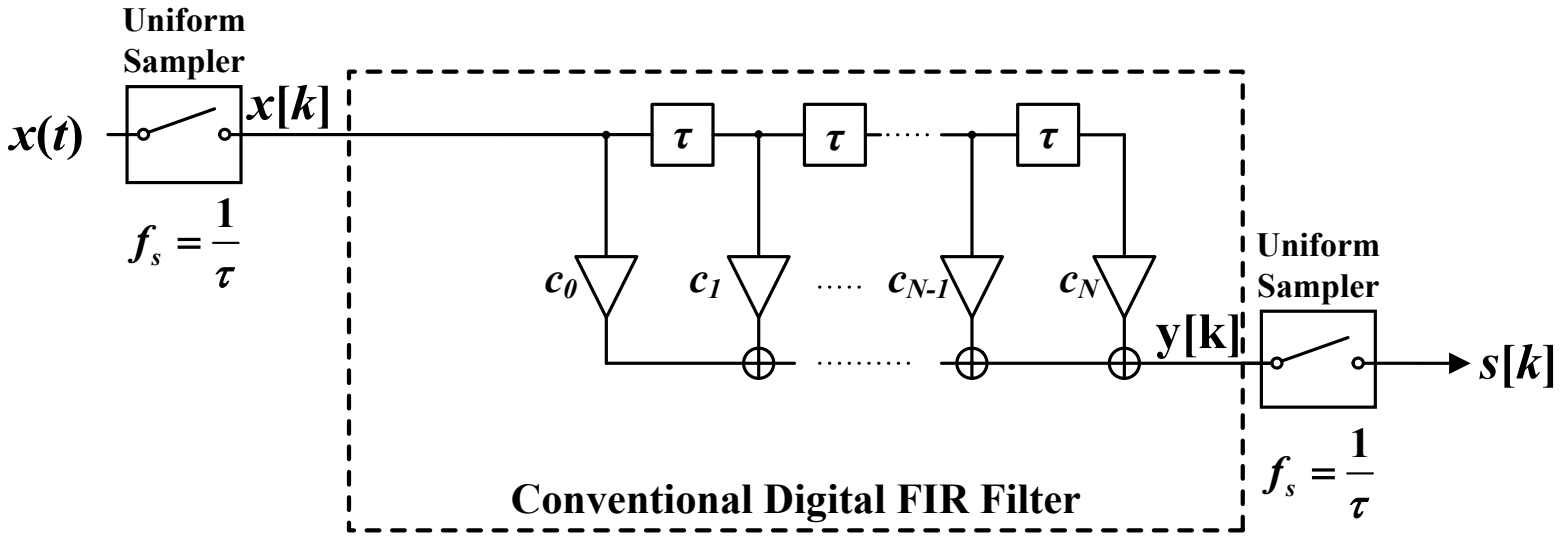
$$\text{SQNR(dB)} = 6.02 \times \text{bit} + 1.76$$

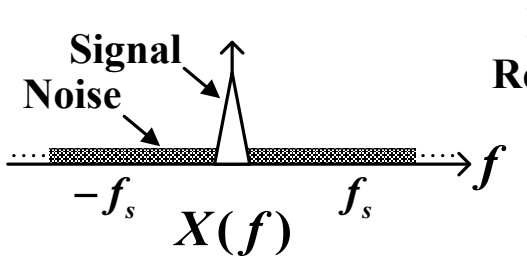


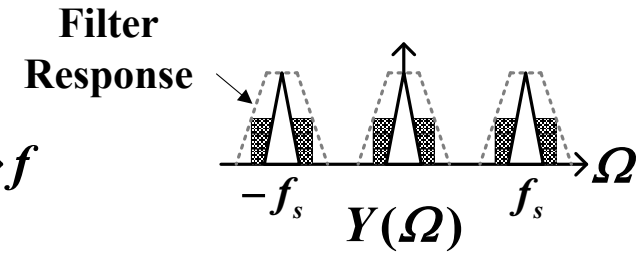
$$\text{SQNR(dB)} \gg 6.02 \times \text{bit} + 1.76$$

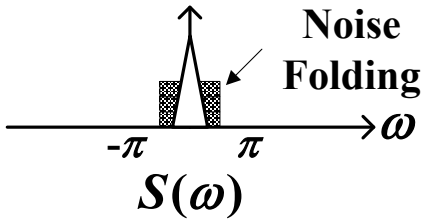
Conventional Digital Filter

- **Frequency response repeats every f_s**





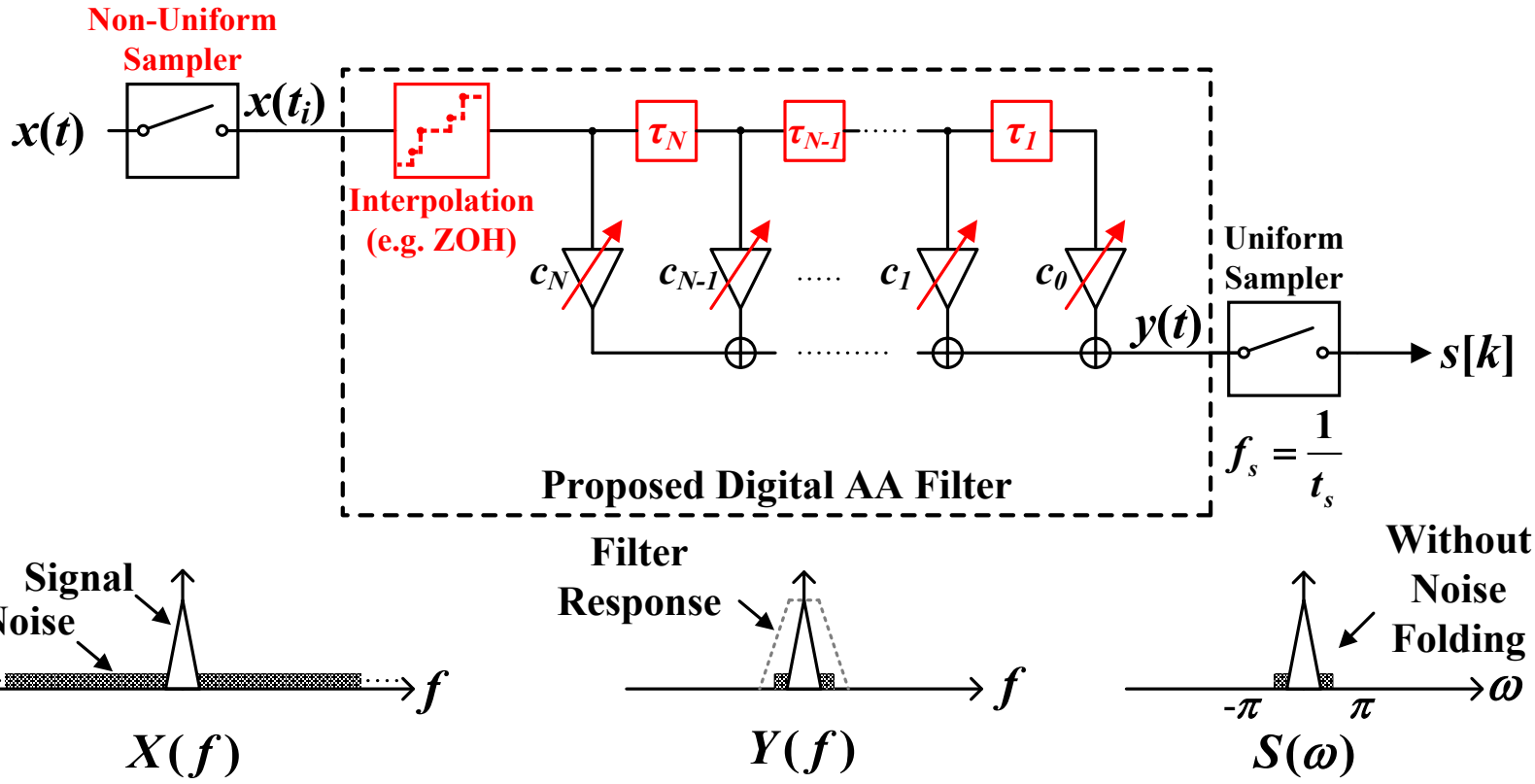




$$s[k] = \sum_{i=0}^{N} x[k-i] \cdot c_i$$

Proposed Digital Anti-Aliasing Filter

- True Analog filter response but in digital domain

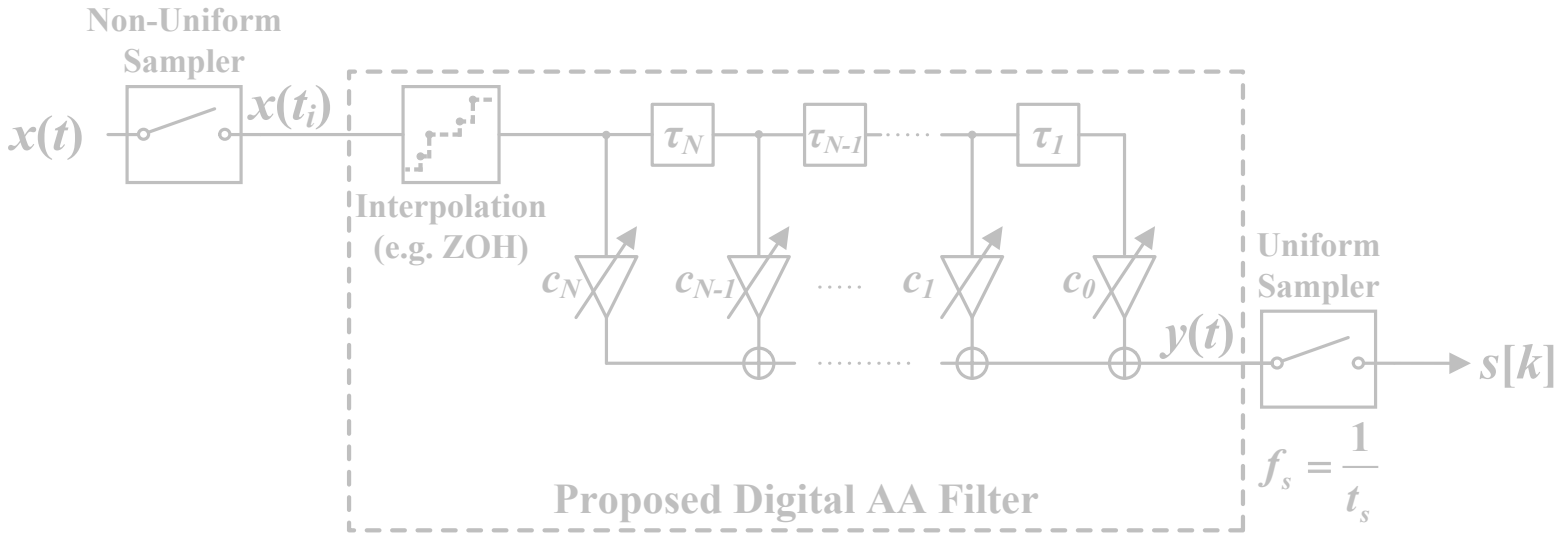


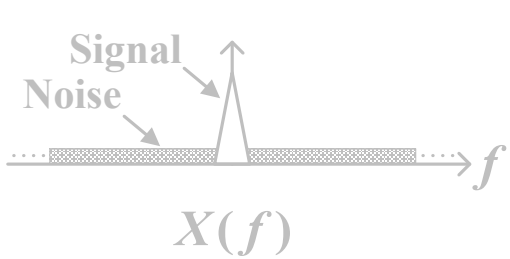
$$s[k] = \sum_{i=0}^{N} x(t_i) \cdot \underbrace{\int_{t_i}^{t_{i+1}} h(kt_s - t)dt}_{c_i}$$

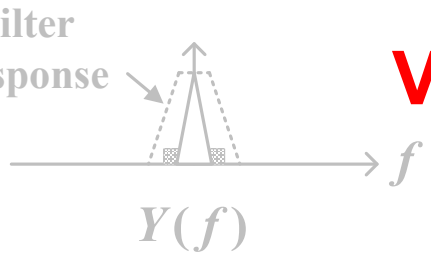
Ref: D. Hand and M. Chen, "A non-uniform sampling ADC architecture with embedded alias-free asynchronous filter," *GLOBECOM*, 2012.

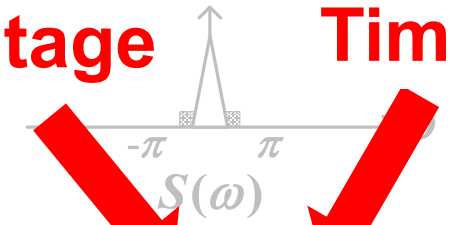
Proposed Digital Anti-Aliasing Filter

- True Analog filter response but in digital domain









Voltage **Time**

$$s[k] = \sum_{i=0}^{N} x(t_i) \cdot \underbrace{\int_{t_i}^{t_{i+1}} h(kt_s - t)dt}_{c_i}$$

Ref: D. Hand and M. Chen, "A non-uniform sampling ADC architecture with embedded alias-free asynchronous filter," *GLOBECOM*, 2012.

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  - **Voltage Quantizer**
  - **Time Quantizer**
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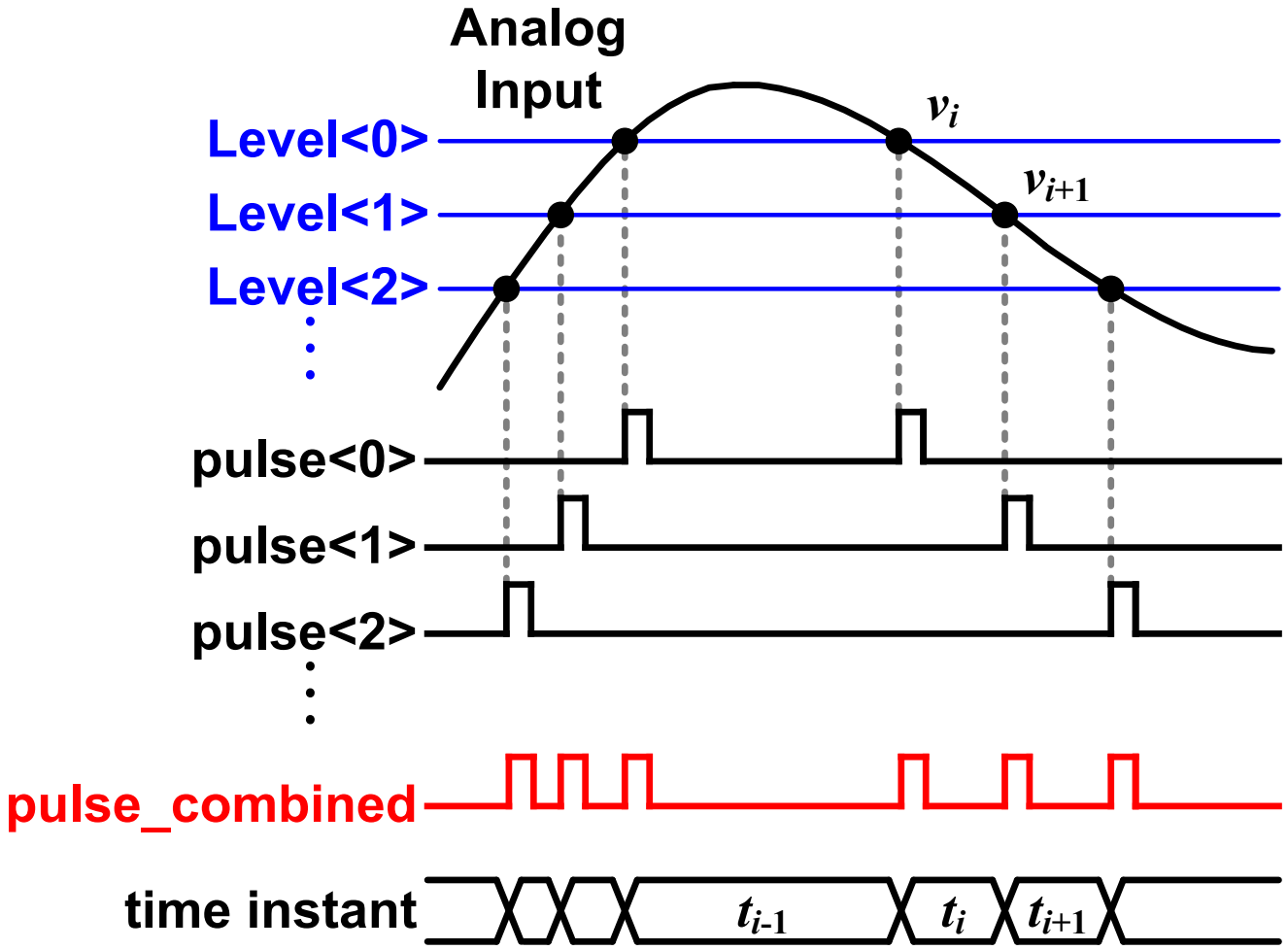
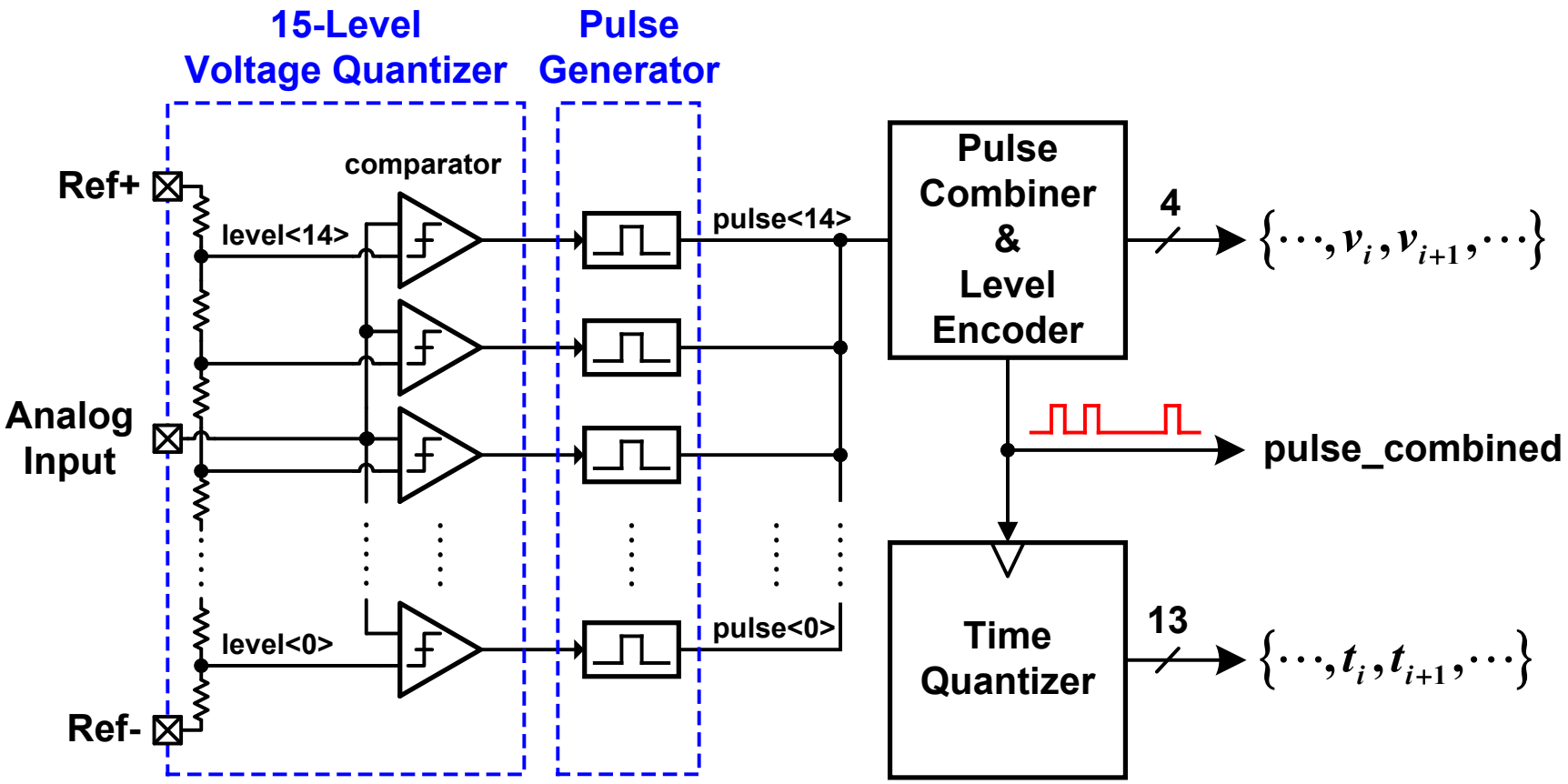
Level-Crossing Events

- Pulses are generated and combined from different levels

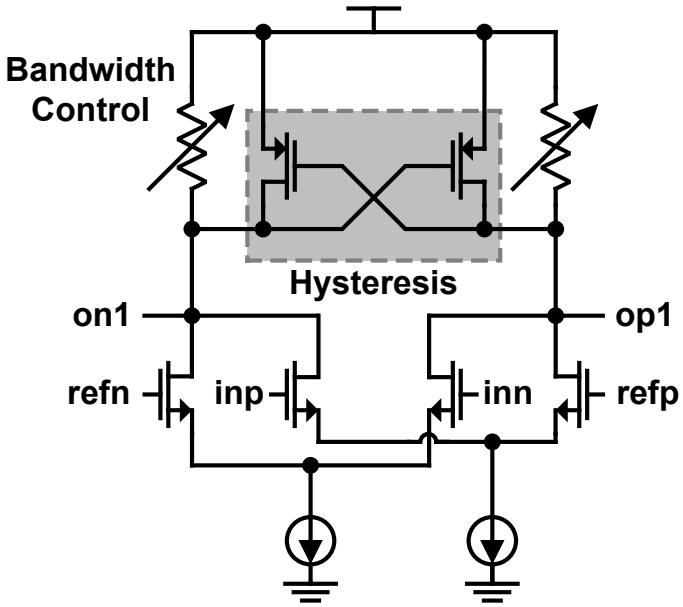


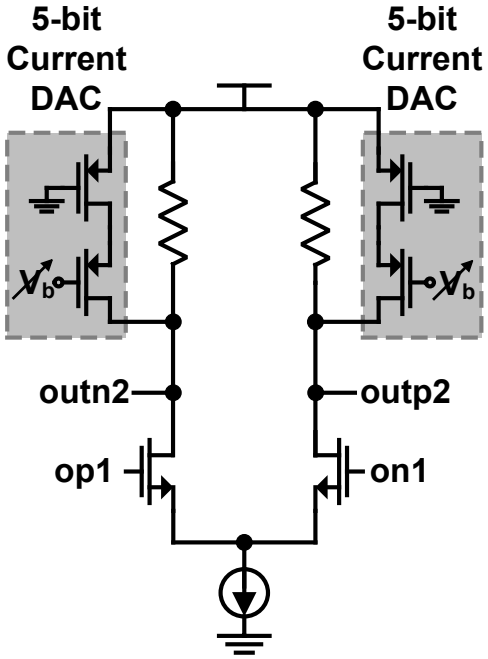
Proposed Flash-Based NUS ADC

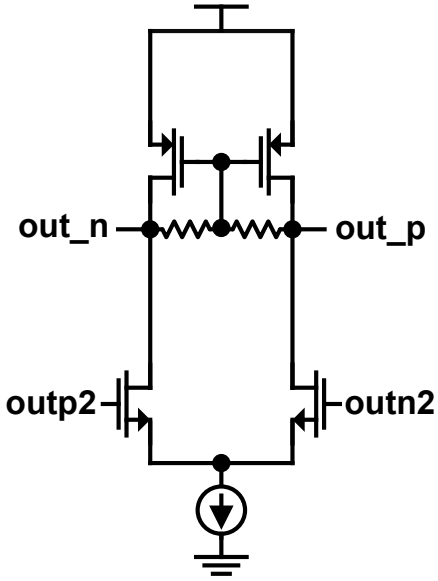


Comparator Design

- **Minimize the delay variations**
  1. **Different input slew rate**
     ➔ > 500MHz BW, > 40dB gain
  2. **Different input DC levels**

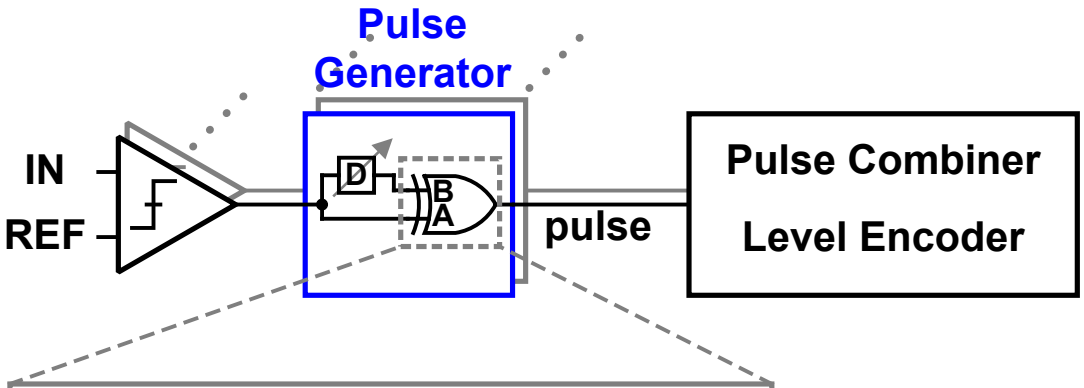


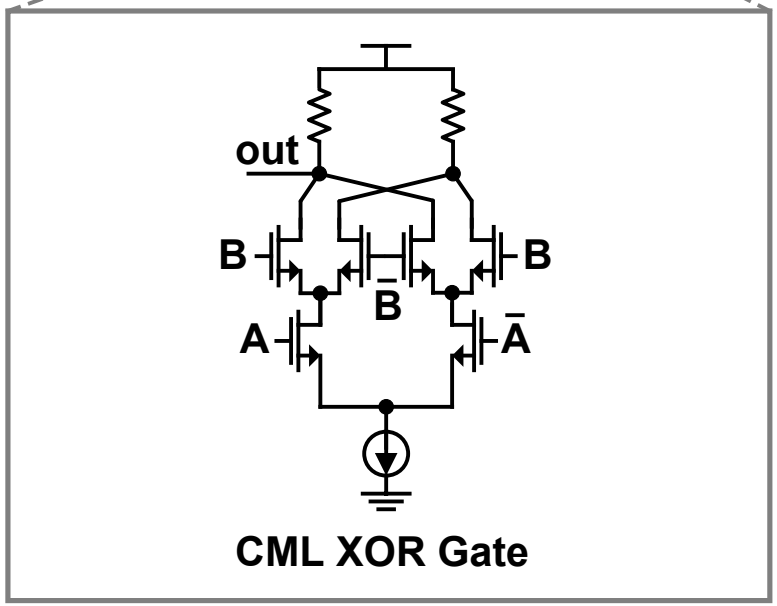


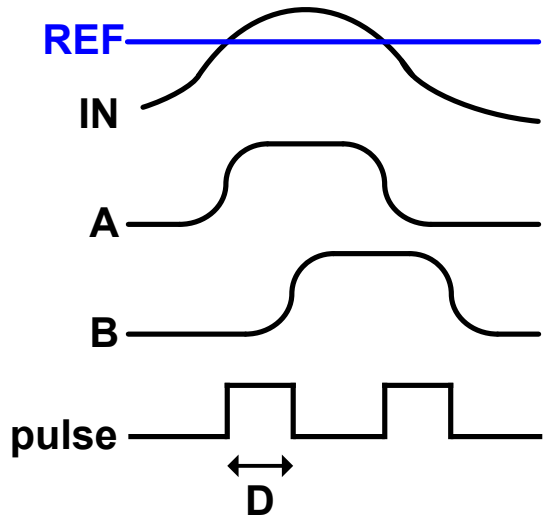


Pulse Generator

- **Use differential topology to reduce delay variation**



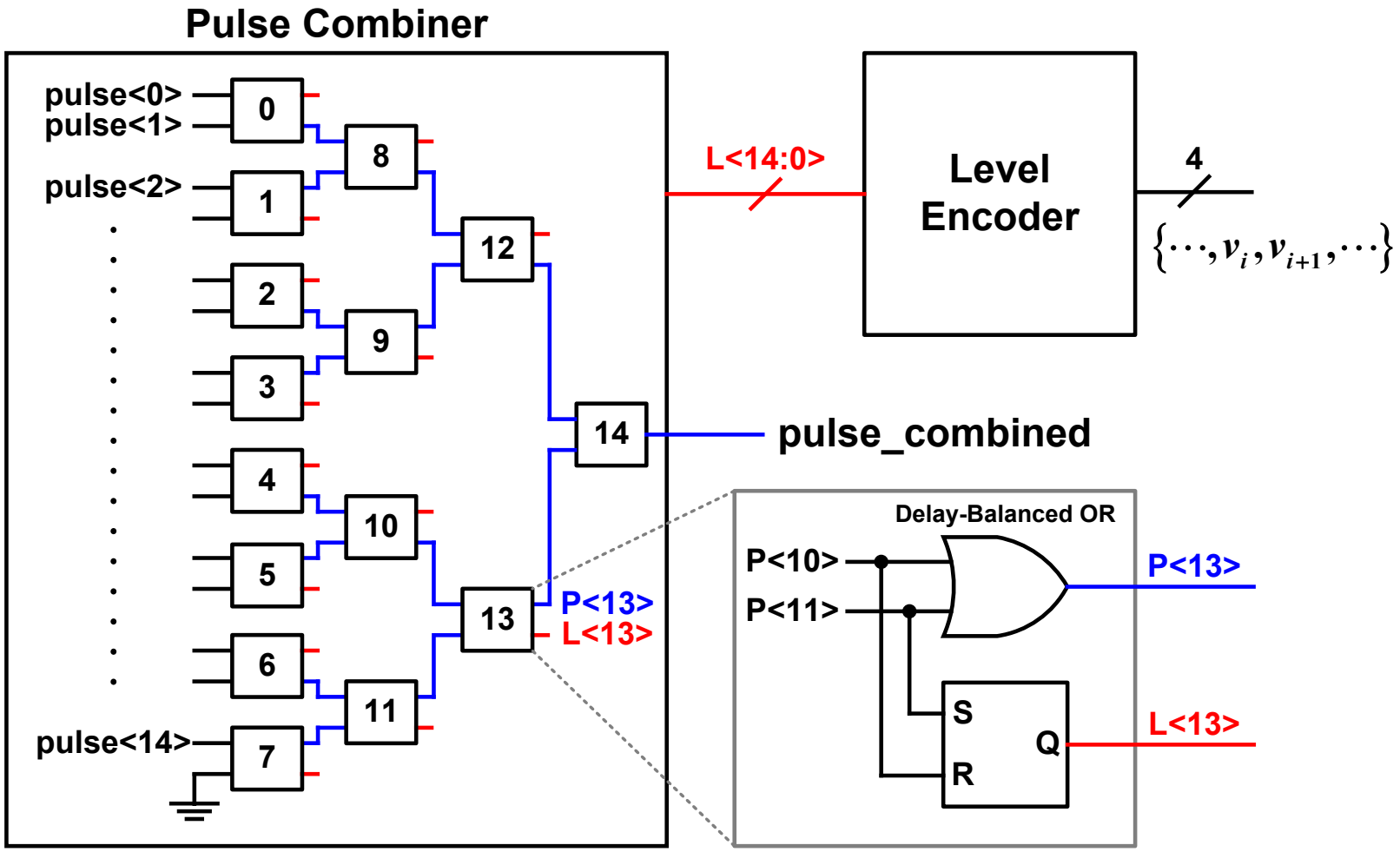




pulse width ~ 300ps to 400ps

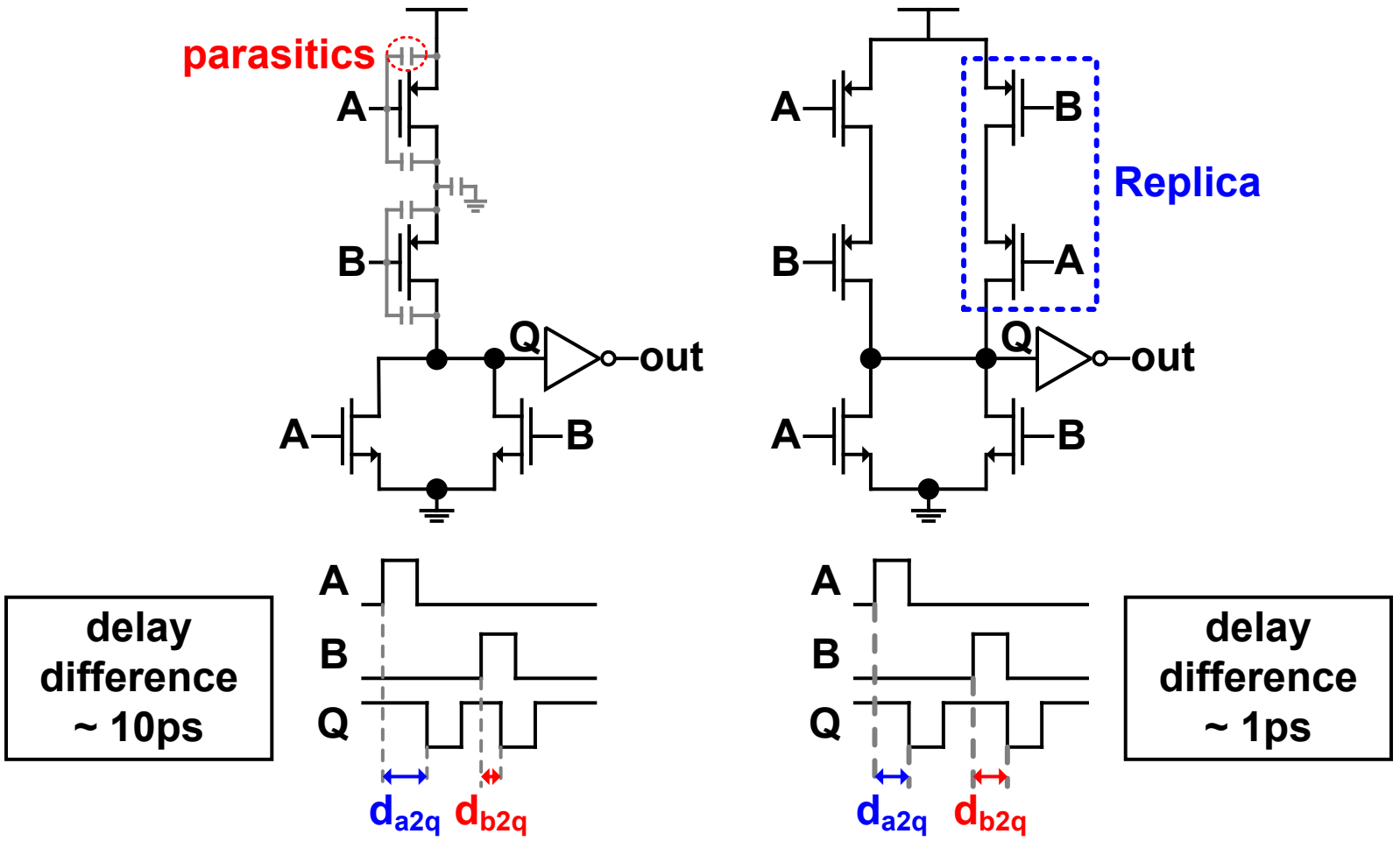
Pulse Combiner / Level Encoder

- **Tree structure to match delays on different paths**

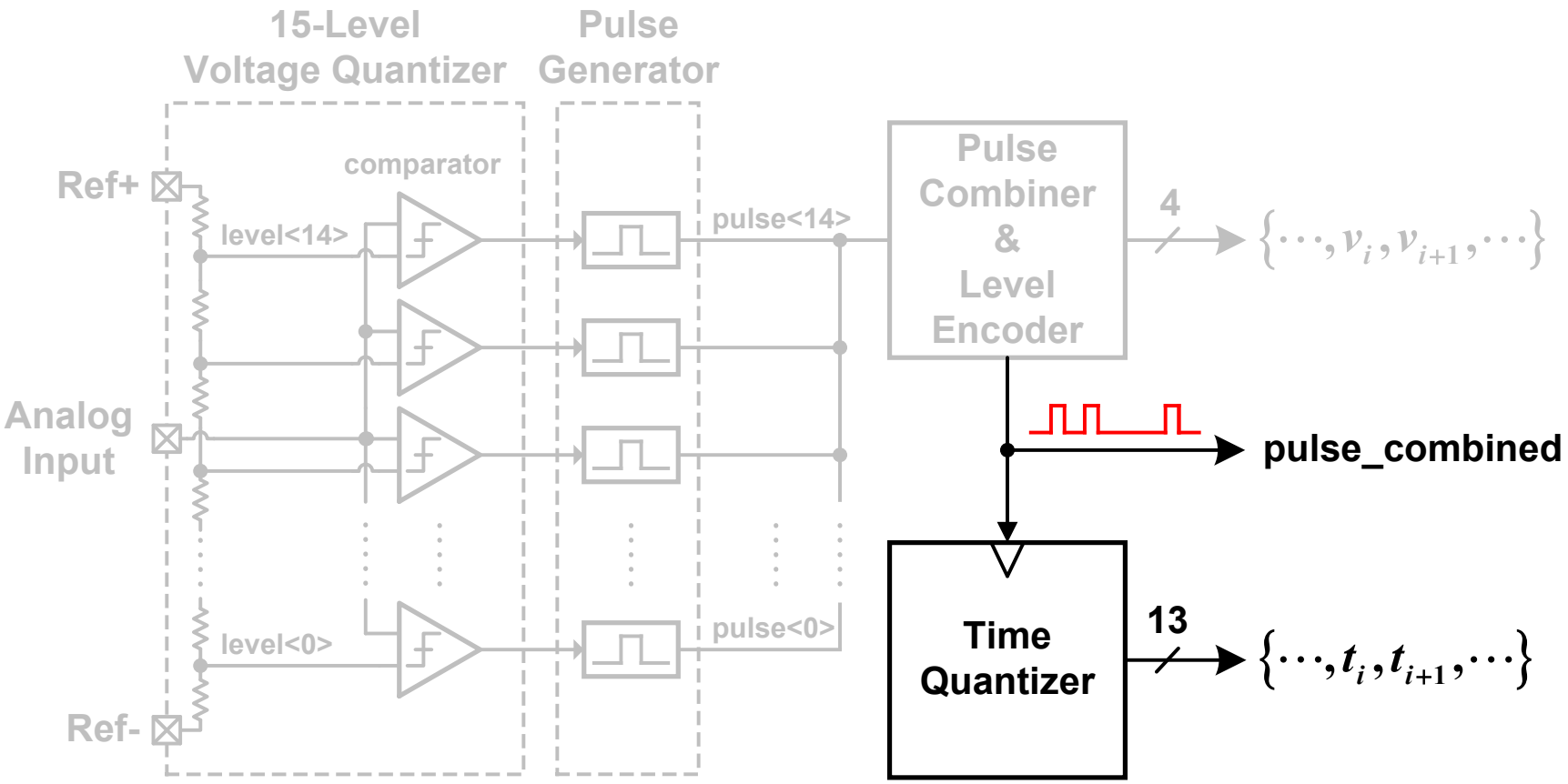


Delay-Balanced OR Gate

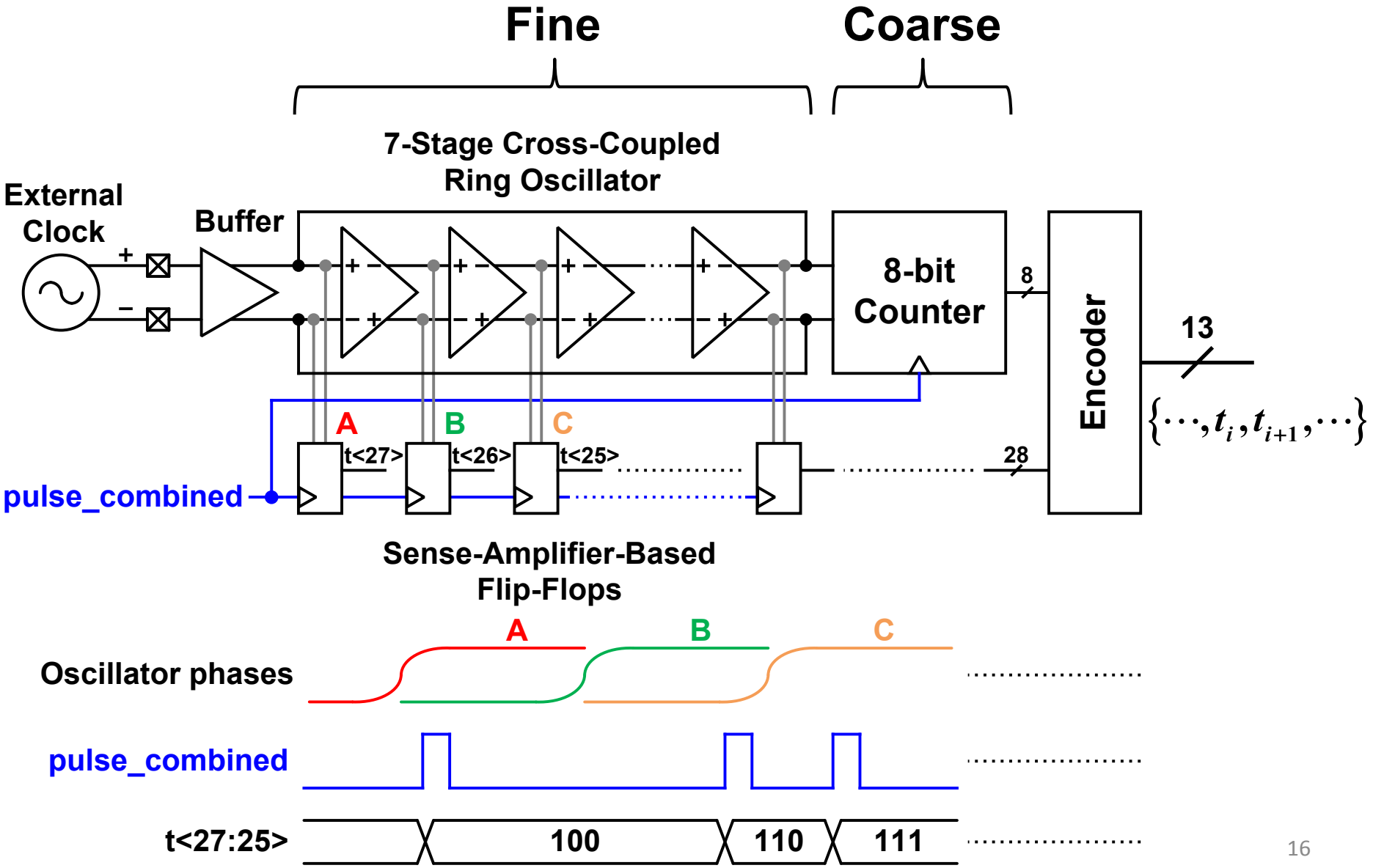
- **Match the delay at different ports due to unequal parasitics**



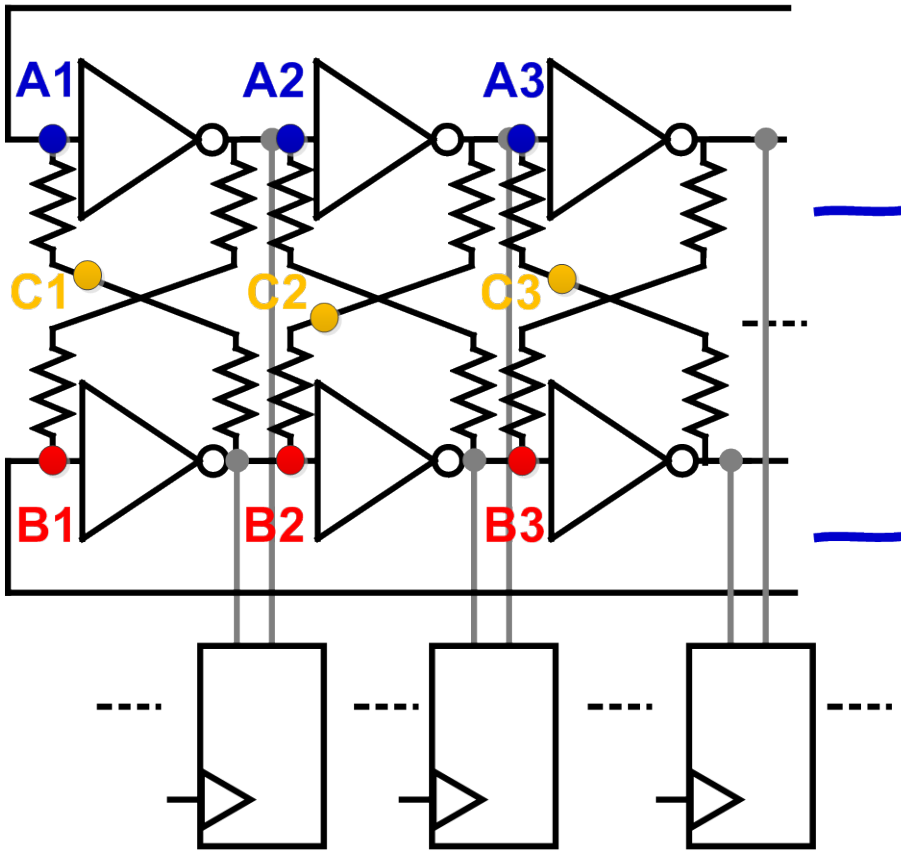
Time Quantization



Time Quantizer

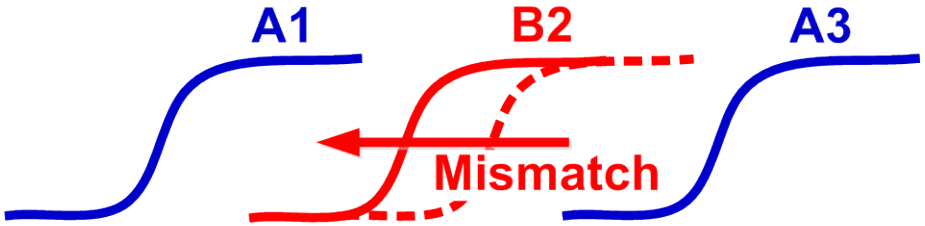


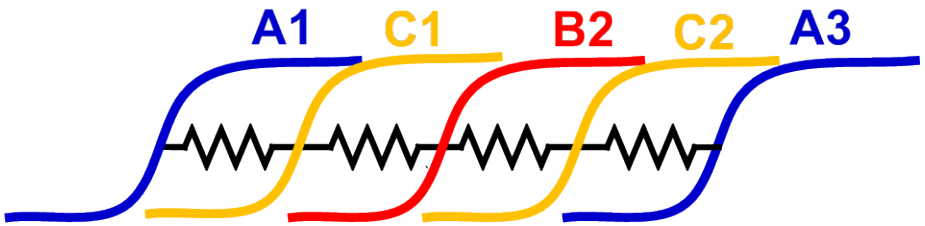
Passive Phase Interpolation



Sense-Amplifier-Based Flip-Flops

Without Passive Interpolation





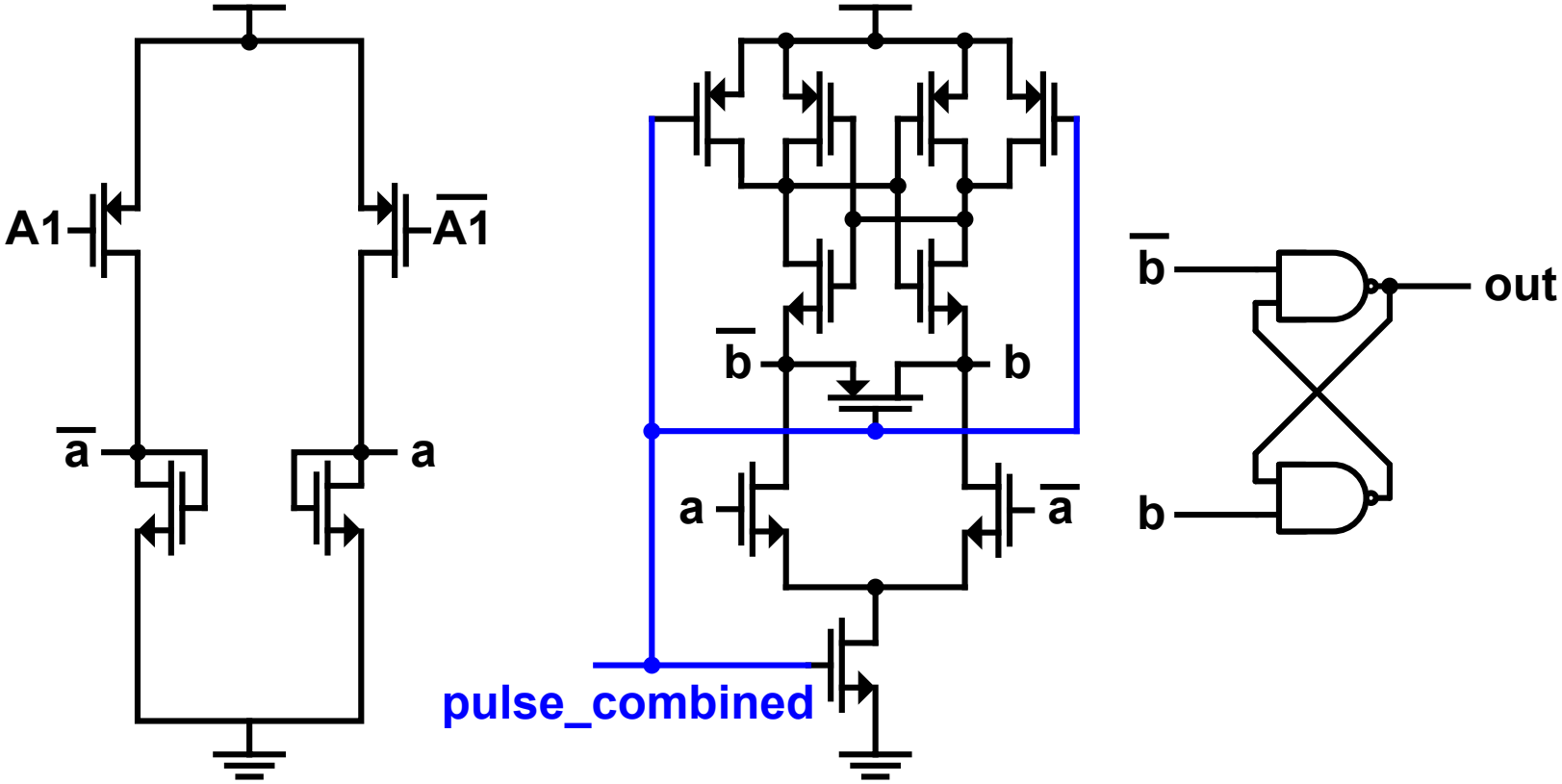
With Passive Interpolation

➔ **Mismatch averaged out**

➔ **Phase doubled**

Sense-Amplifier-Based Flip-Flop

- **Maximum operation frequency of 2 GHz**



Pre-amp **Sense-Amplifier** **Latch**

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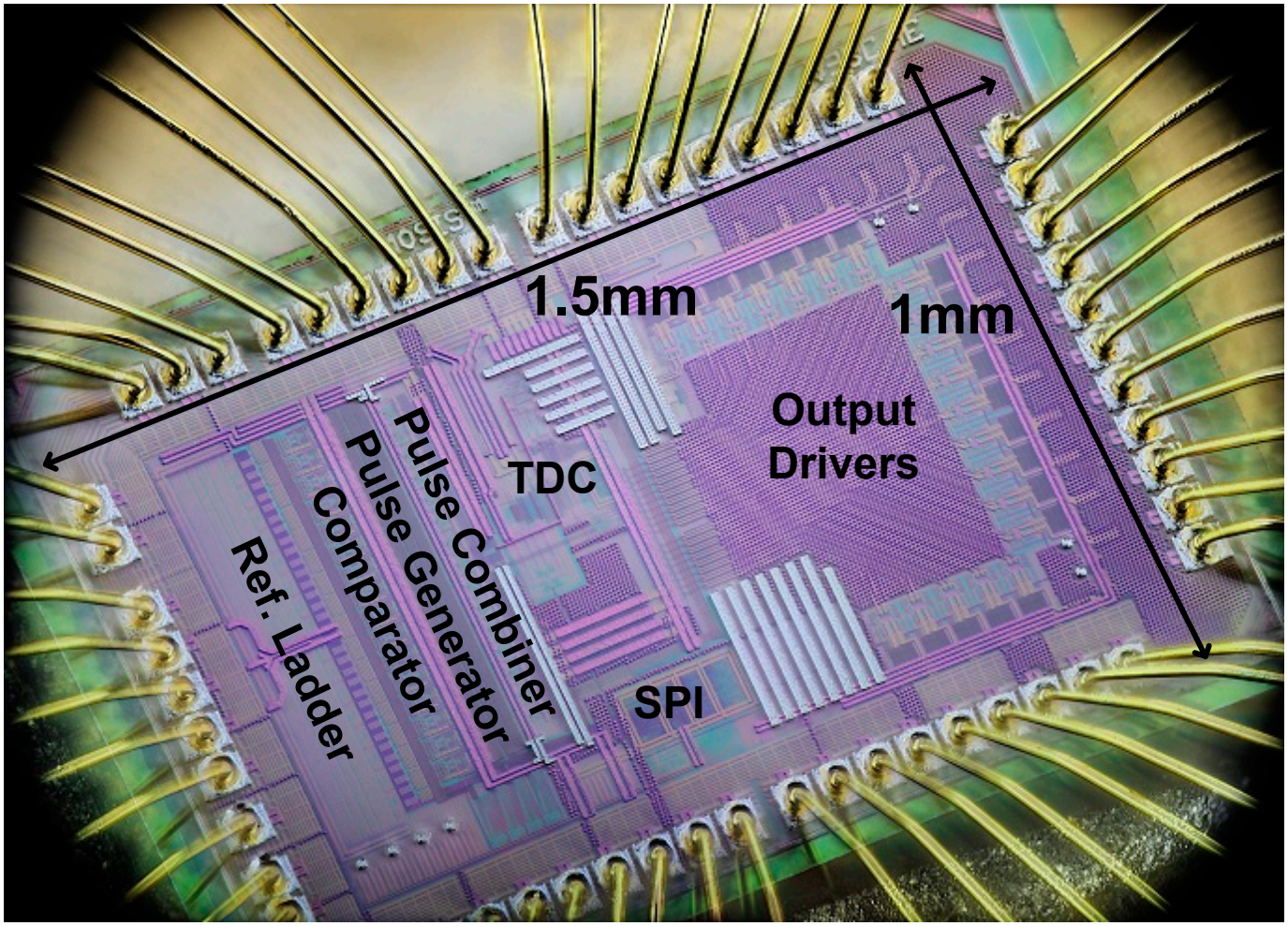
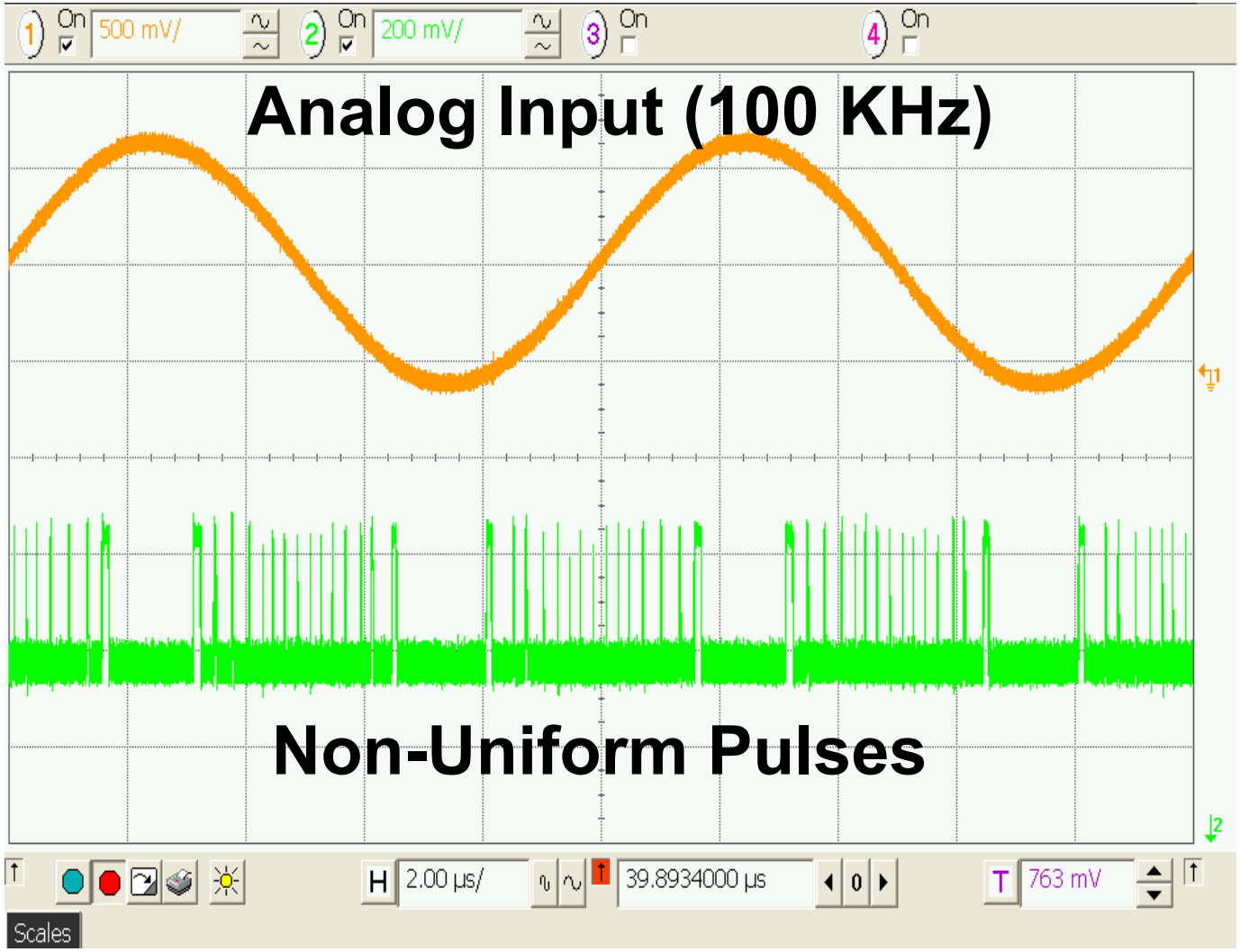
Chip Micrograph

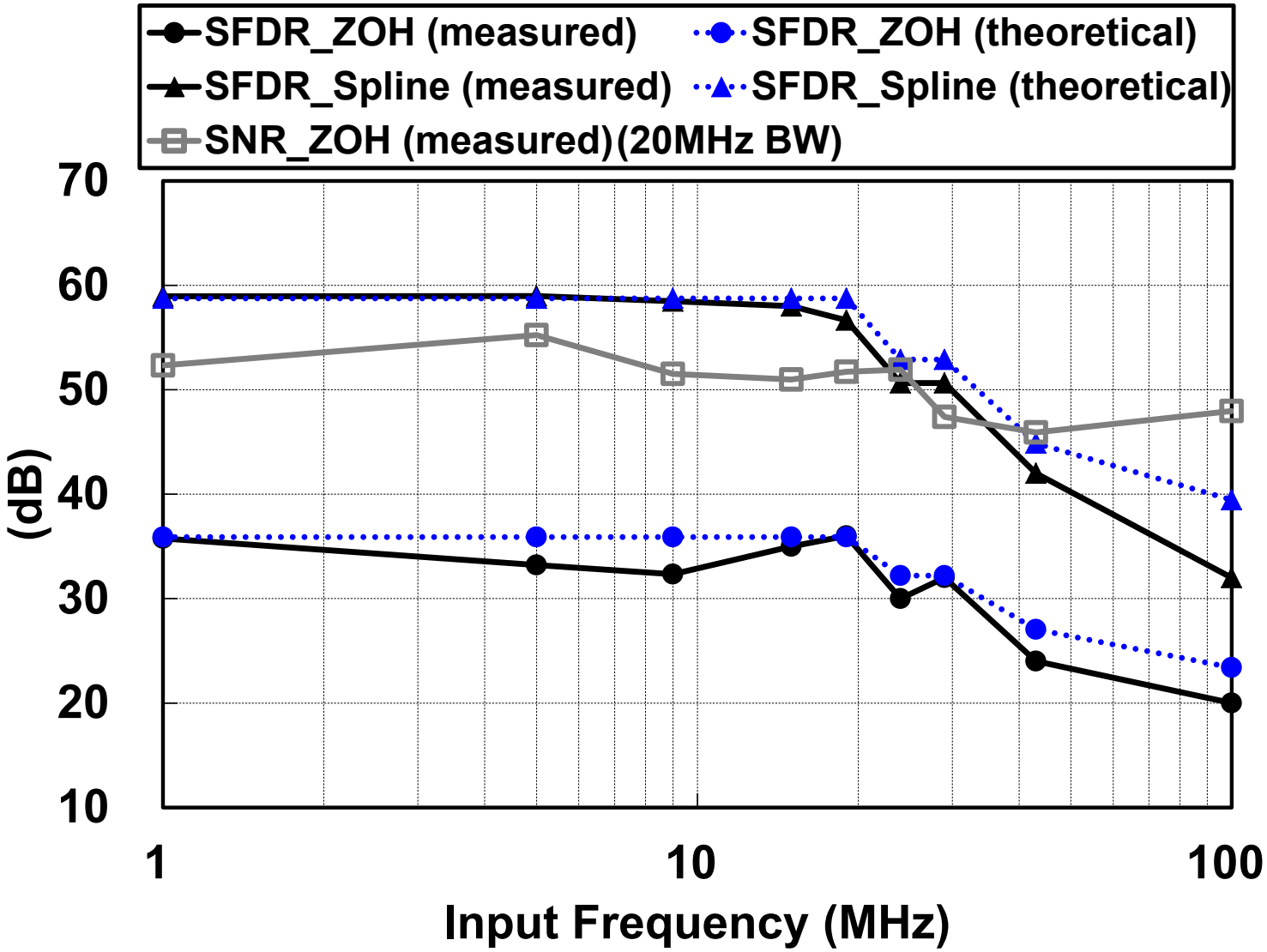


Active area = 0.3 mm^2

Measured Pulse Out

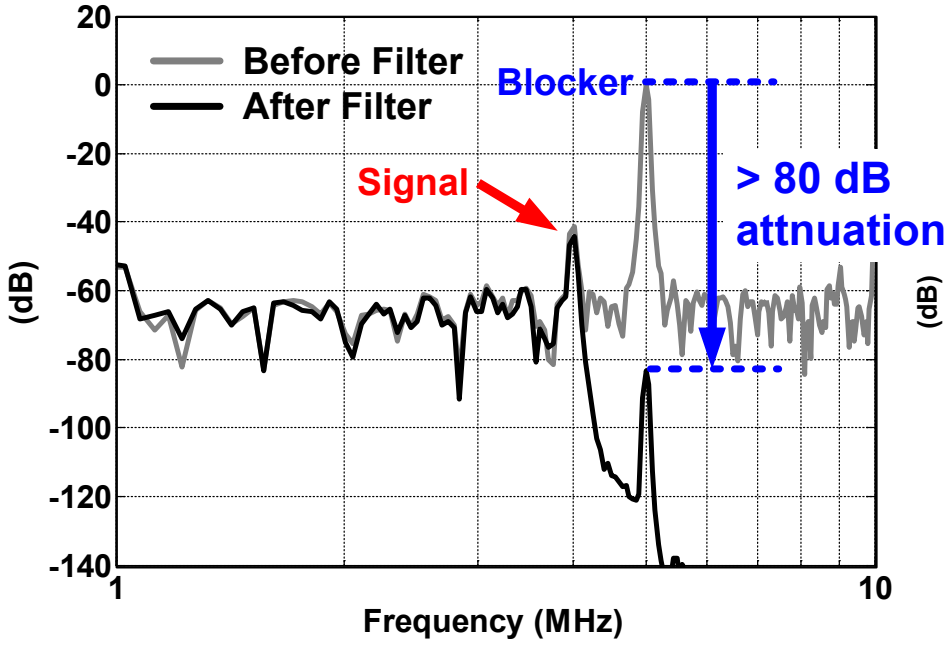


Single-Tone Test

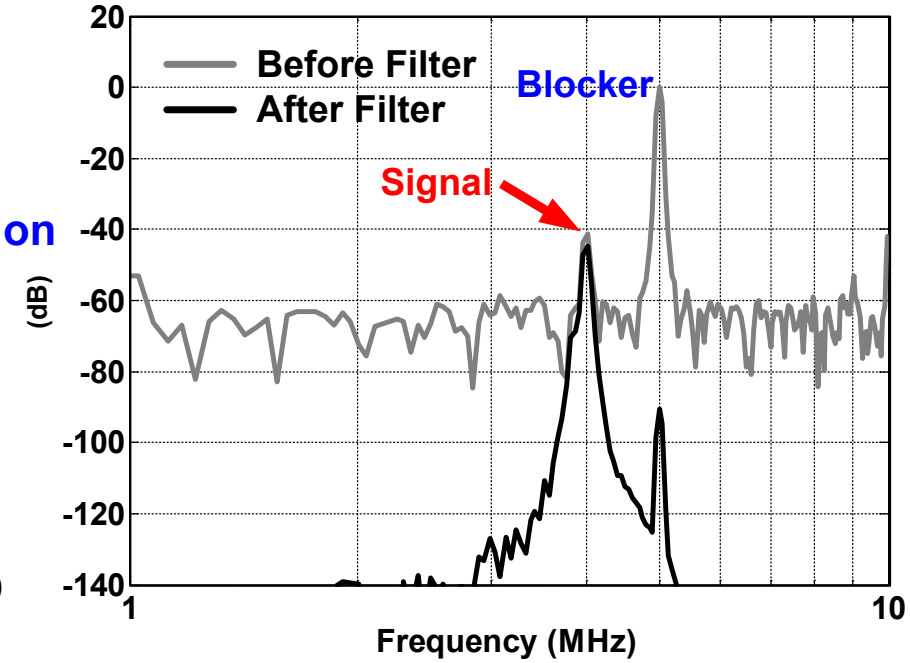


Two-Tone Test

- **Desired signal with 40 dB higher blocker**



Low-Pass Digital AA Filter

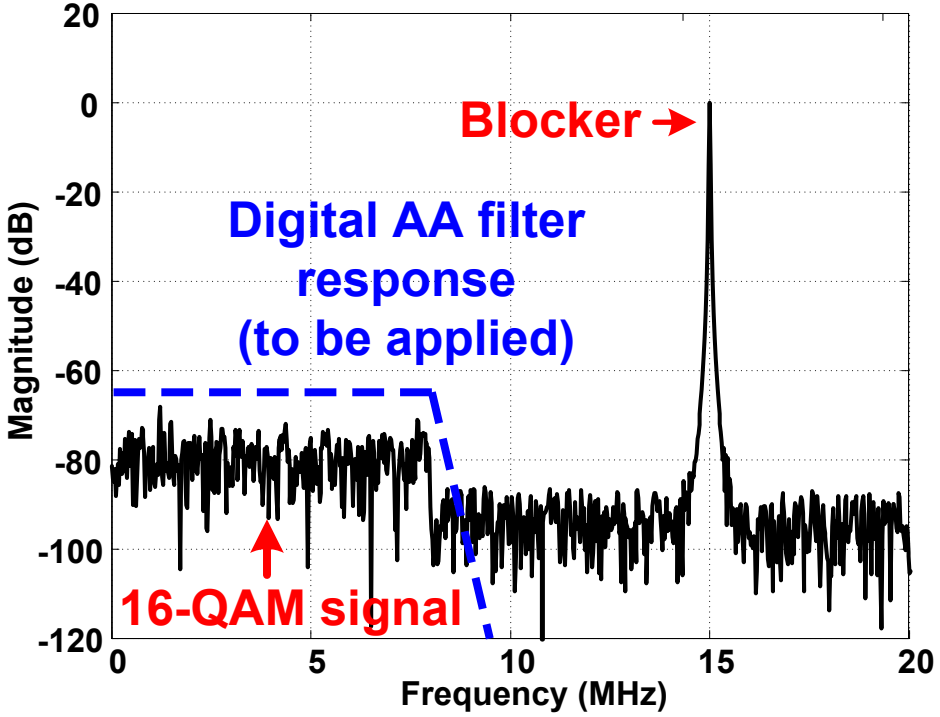


Band-Pass Digital AA Filter

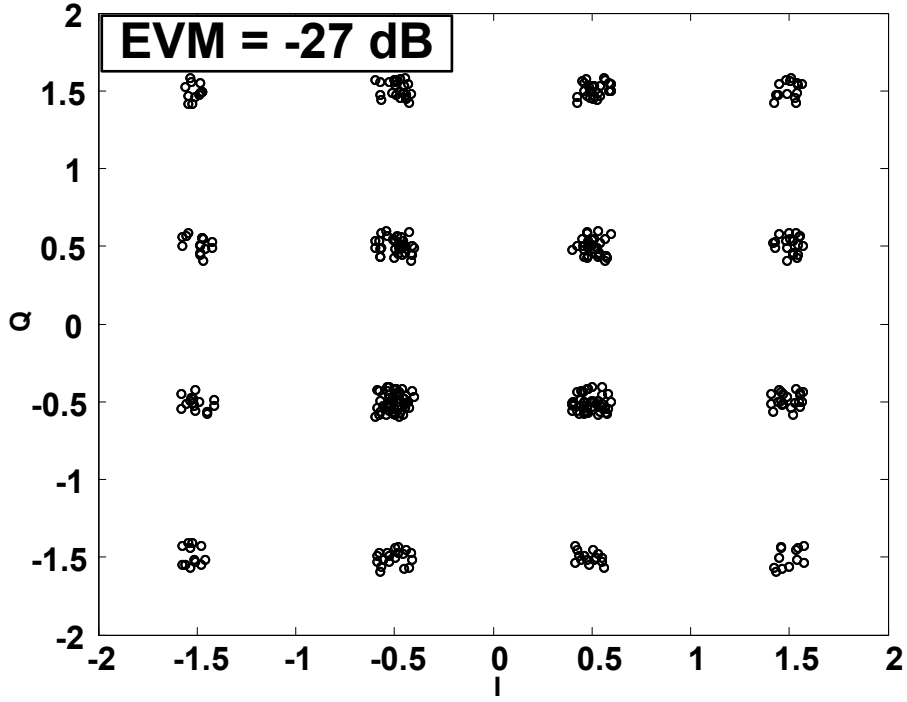
Modulated Signal

- 8 MHz 16-QAM signal with 50 dB higher blocker

Spectrum before Filter



Constellation after Filter



Performance Summary

	Proposed Flash-Based NUS ADC	B. Schell, ISSCC 2008	S. Naraghi ISSCC 2009
Alias-free Sampling	Yes	Yes	No
Alias-free Filtering	Yes	No	No
Synchronous Output	Yes	No	Yes
Voltage Quantization	15 levels	256 levels	1 level
Time Quantization	10 ps/step	No	500 ps/step
SFDR	56 dB (f_{in}=19MHz)	47 dB (f_{in}=4KHz)	58 dB (f_{in}=40KHz)
SNDR	50 dB (f_{in}=19MHz)	55 dB (f_{in}=2KHz)	49 dB (f_{in}=290KHz)
Power	30 mW	1.23 mW	14 uW

Conclusion

- **A flash-based non-uniform sampling ADC architecture is proposed to perform anti-aliasing filter in the non-uniform digital domain**

- **Hybrid quantization in both voltage and time domain favors technology scaling**

- **The proposed ADC architecture can be extended to different non-uniform sampling schemes → new opportunities**

Acknowledgements

The authors would like to thank Dr. Mark Rich from DARPA and the NSF Career Award for funding support.