A 5GS/s 10b 76mW Time-Interleaved SAR ADC in 28nm CMOS

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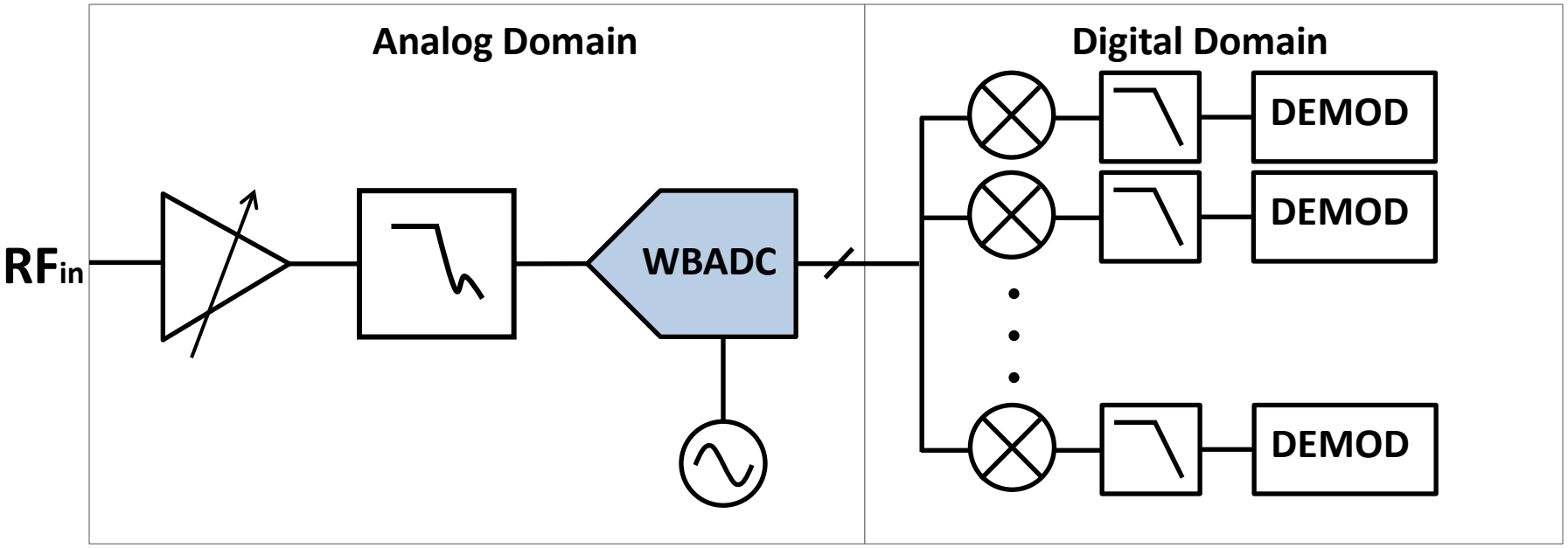
Outline

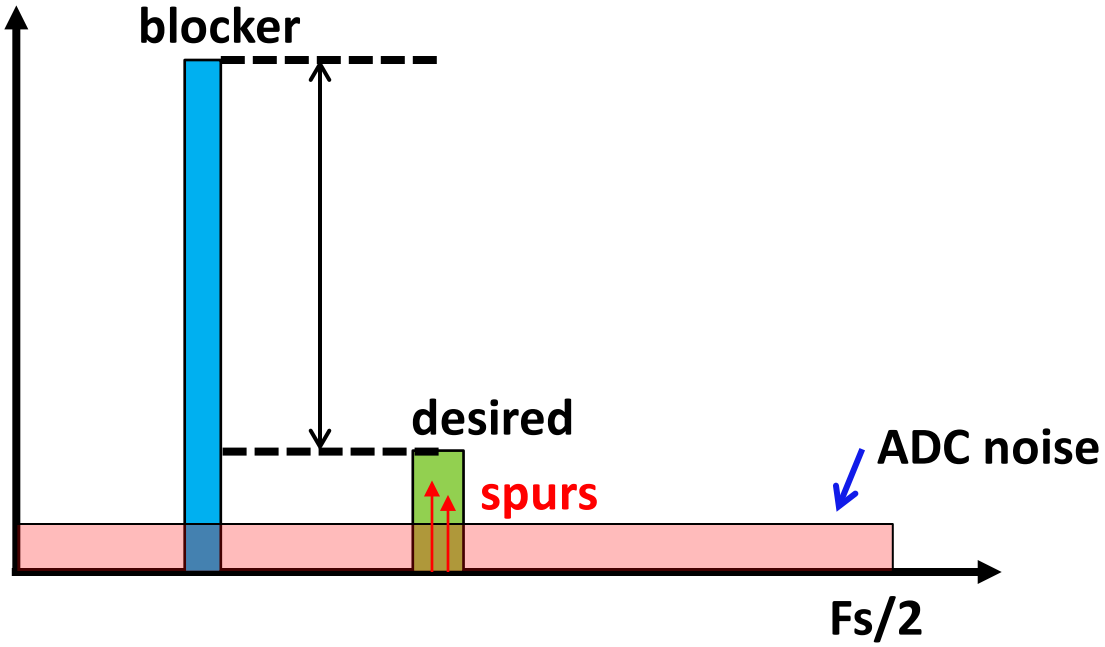
- Motivation
- Architecture
- Implementation
- Measurement Result
- Conclusion

Direct Sampling Receiver



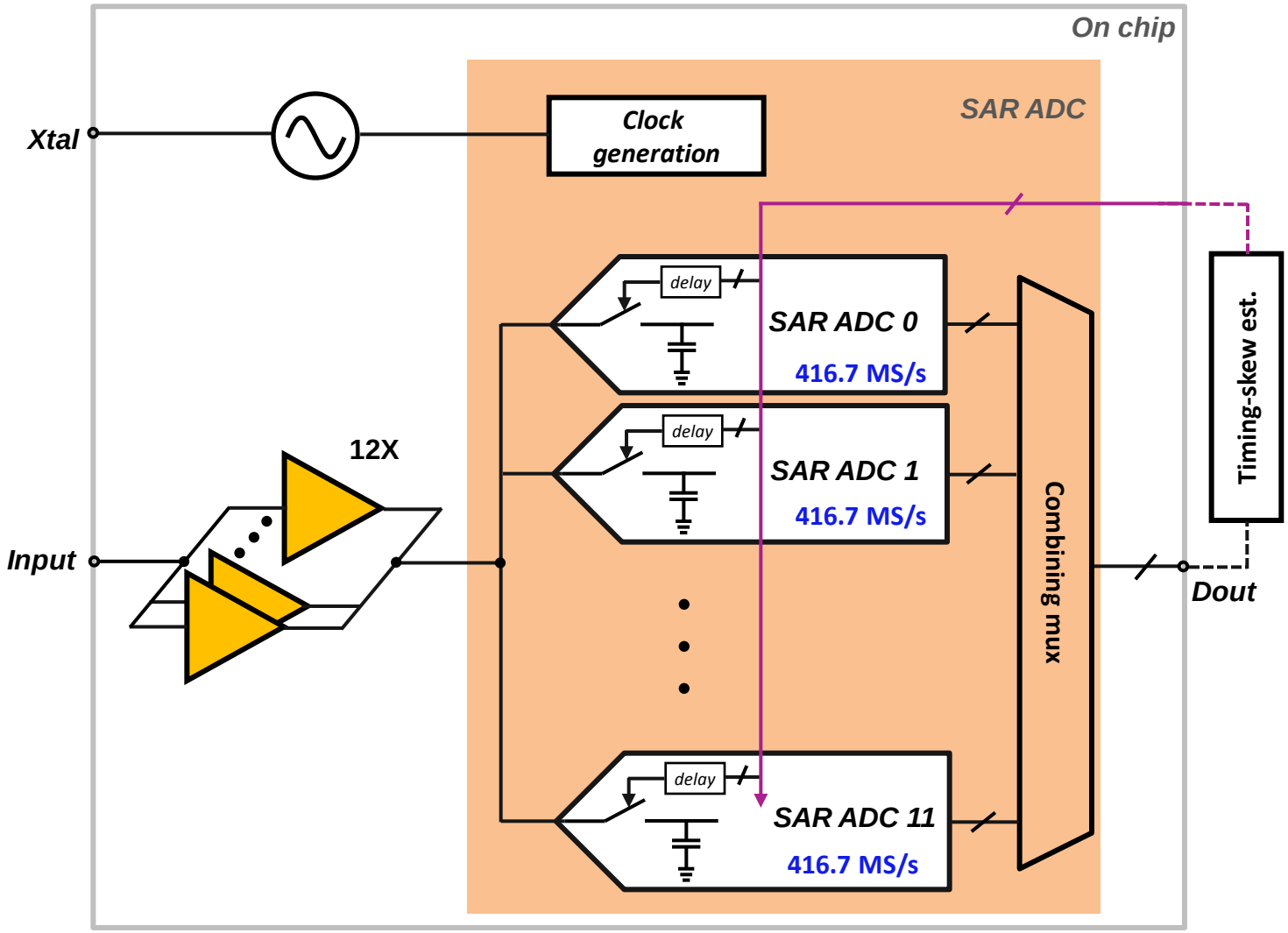
- **Multi-GHz direct sampling receiver for many communication systems such as set-top box receivers**
- **To efficiently receive multiple channels simultaneously**

ADC Requirements in RX



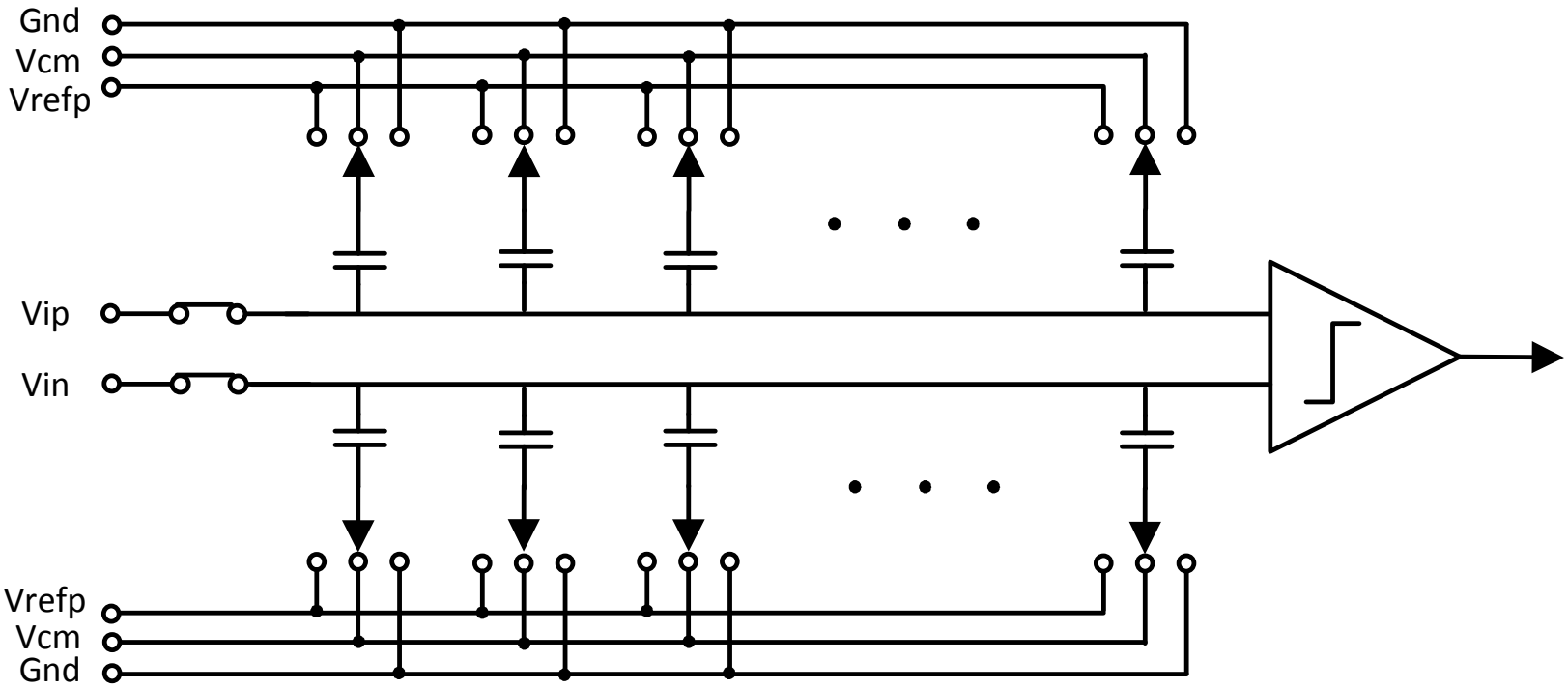
- Oversampling gain for ADC noise = 0.5Fs/Channel BW
- Spurs → SFDR requirement
- Blocker-to-desired ratio + peak-to-average ratio → ADC dynamic range

ADC Architecture



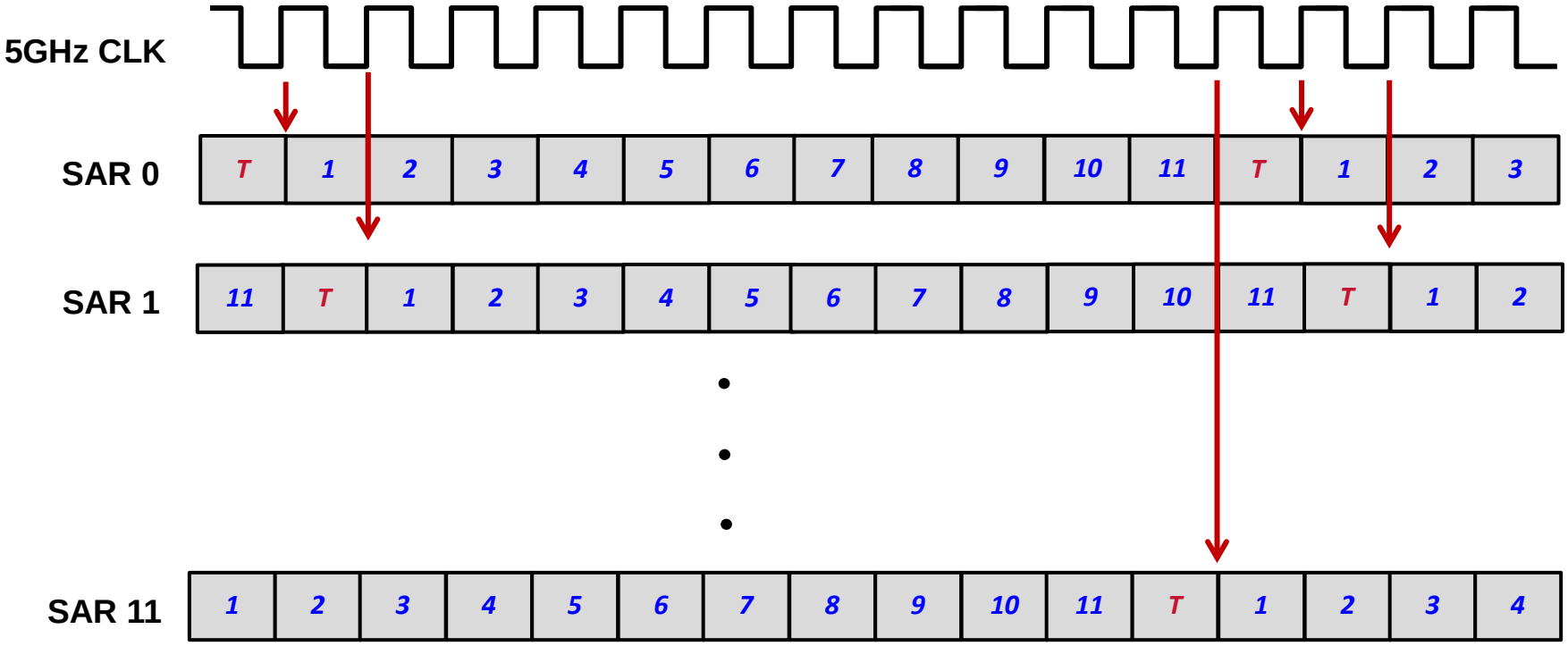
- 12 channel time-interleaved 416.7 MS/s SAR ADC → 5GHz sampling

Sub-ADC architecture



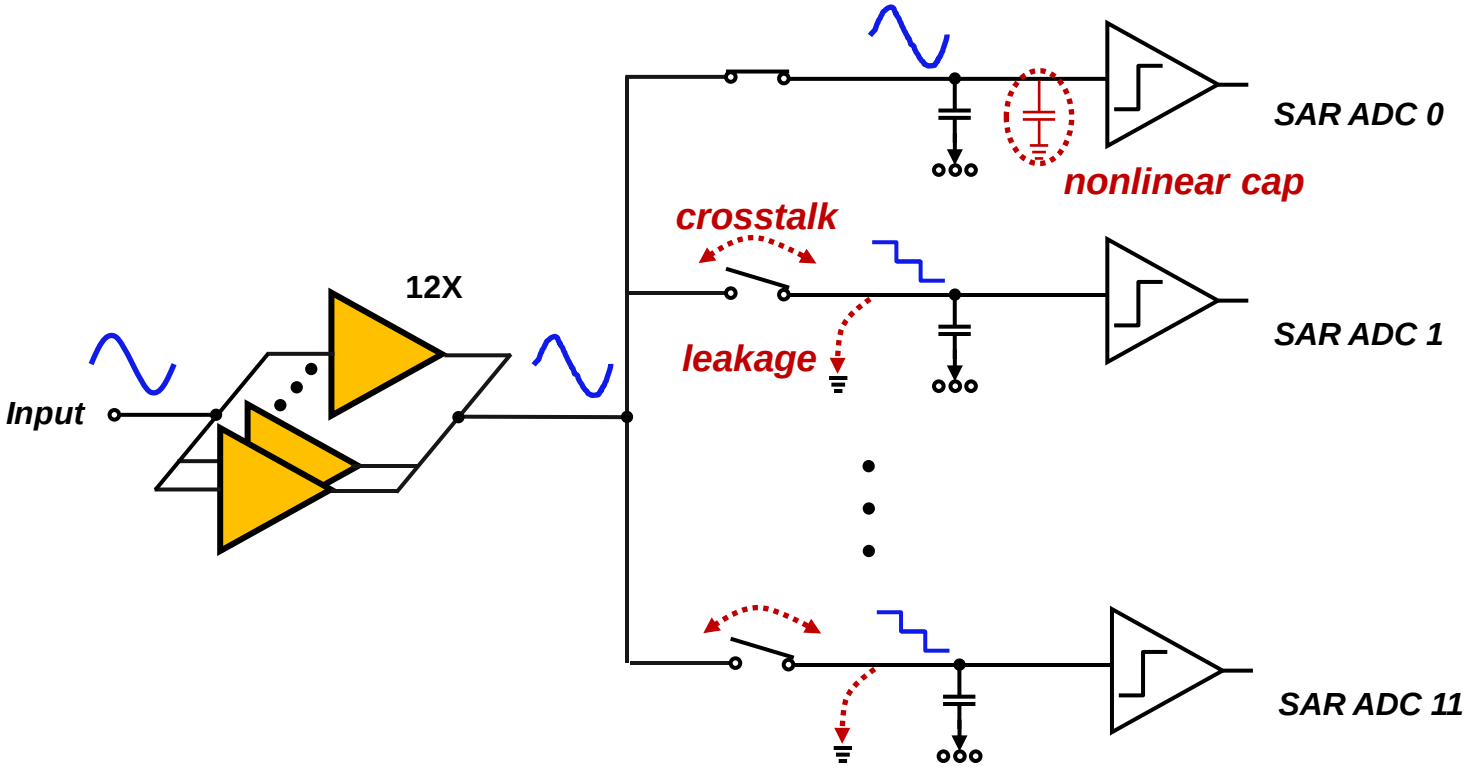
- **Top-plate sampling with Merged Capacitor Switching (MCS)**
- **11 bit reduced radix-2 CDAC with 1 bit redundancy**
- **Custom designed unit capacitor of 2fF**
- **Synchronous SAR logic**

Time-Interleaved Timing



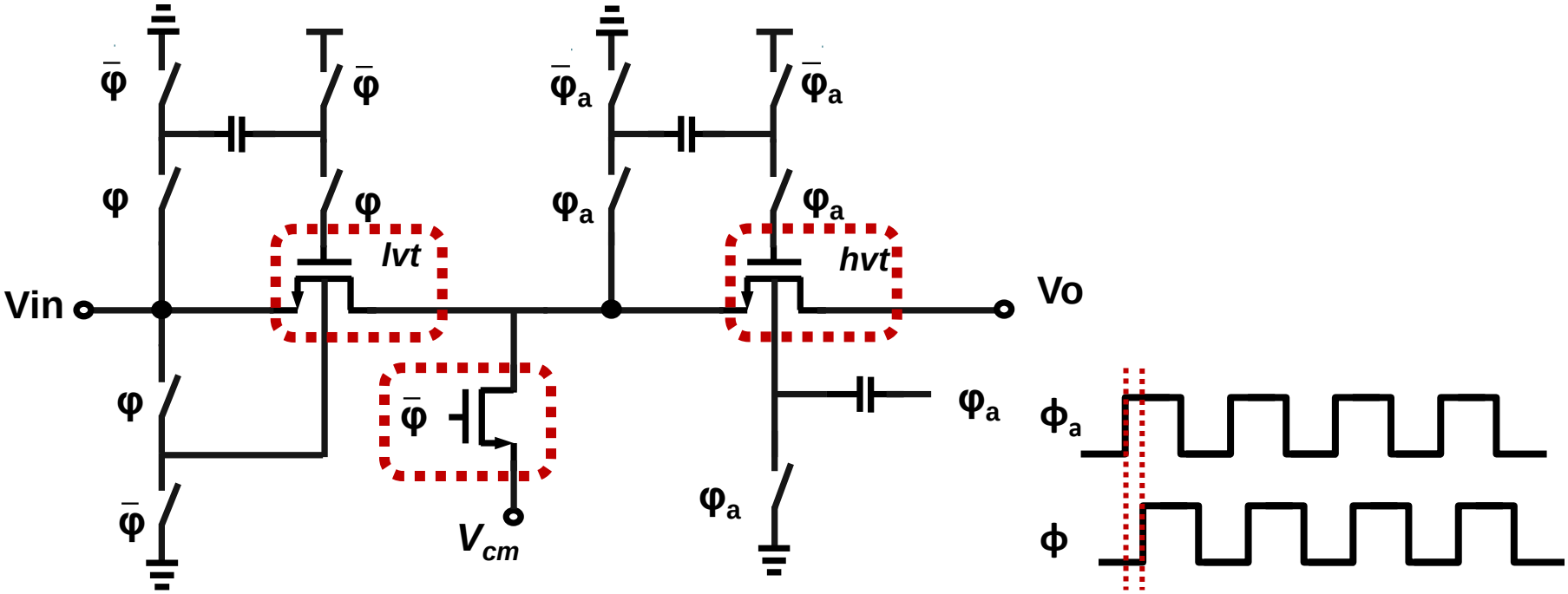
- 1 sampling cycle + 11 SAR conversion cycles for each slice
- The sampling instant for each ADC slice is aligned with the 5GHz clock

Sampling Issues



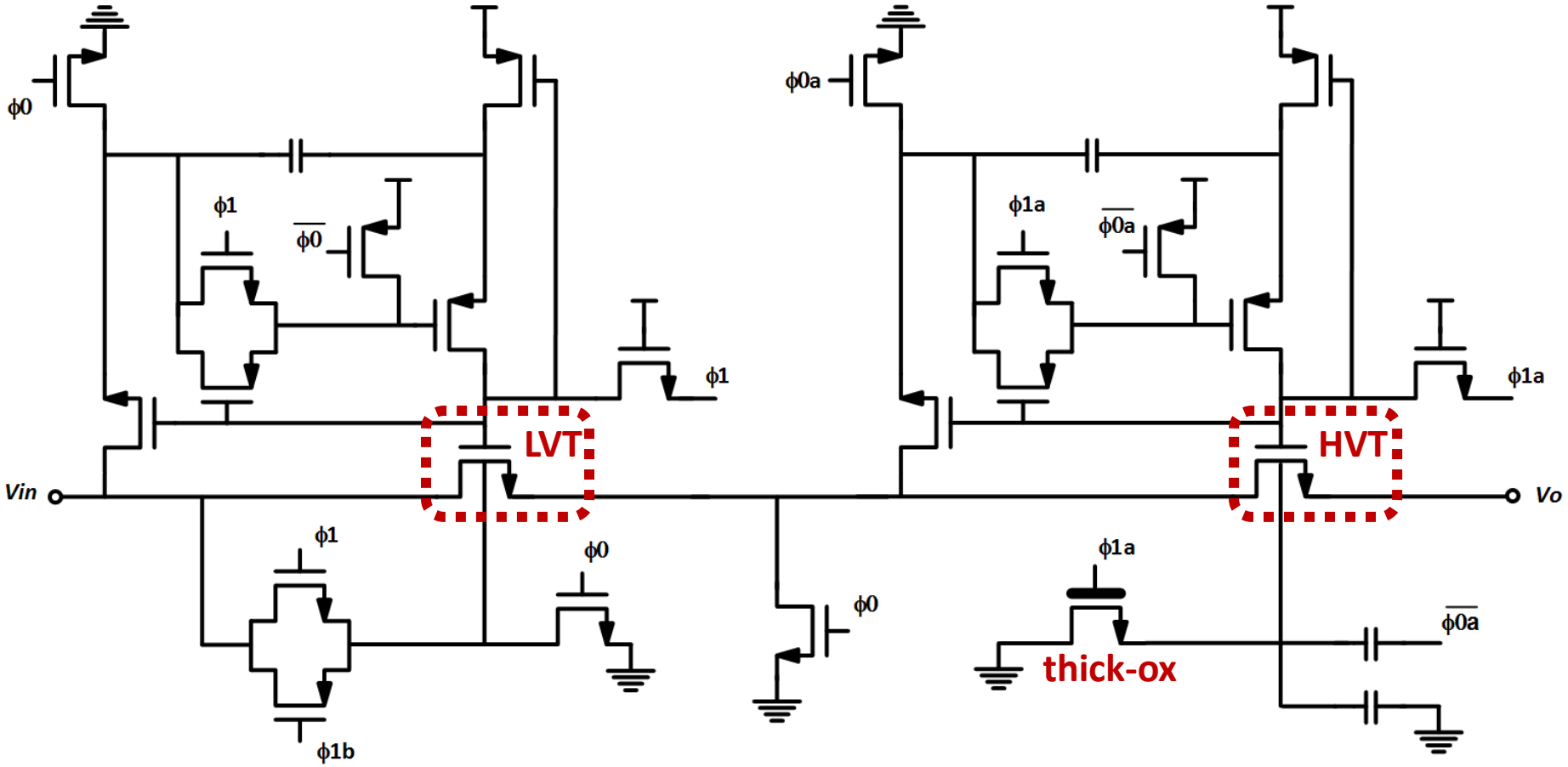
- Crosstalk among channels for top-plate sampling
- Switch leakage current during SAR conversions
- Linearity degradation due to the nonlinear capacitance

Sampling Switch



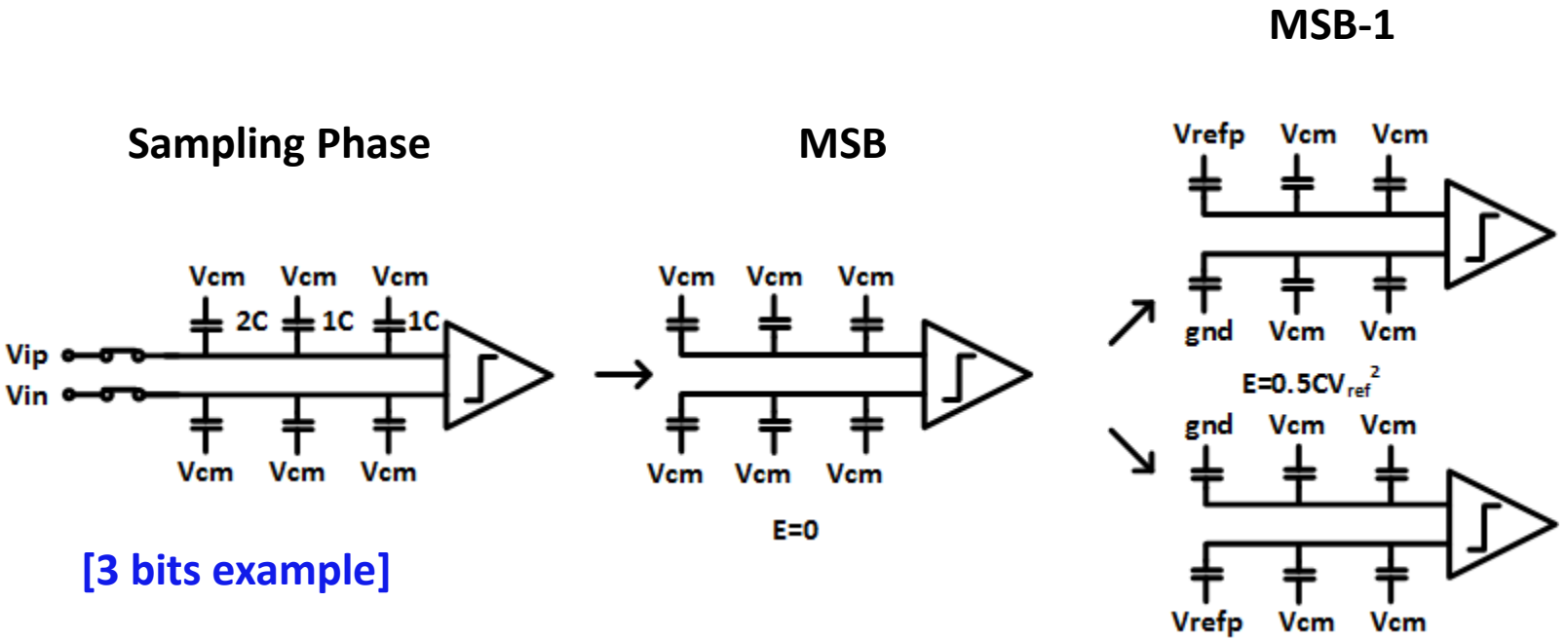
- V_{cm} switch → reduce crosstalk
- HVT switch with negatively boosted substrate → minimize leakage
- The falling edge of ϕa determines the sampling instant

Sampling Switch Details



- **Almost all thin-oxide transistors → better switch**

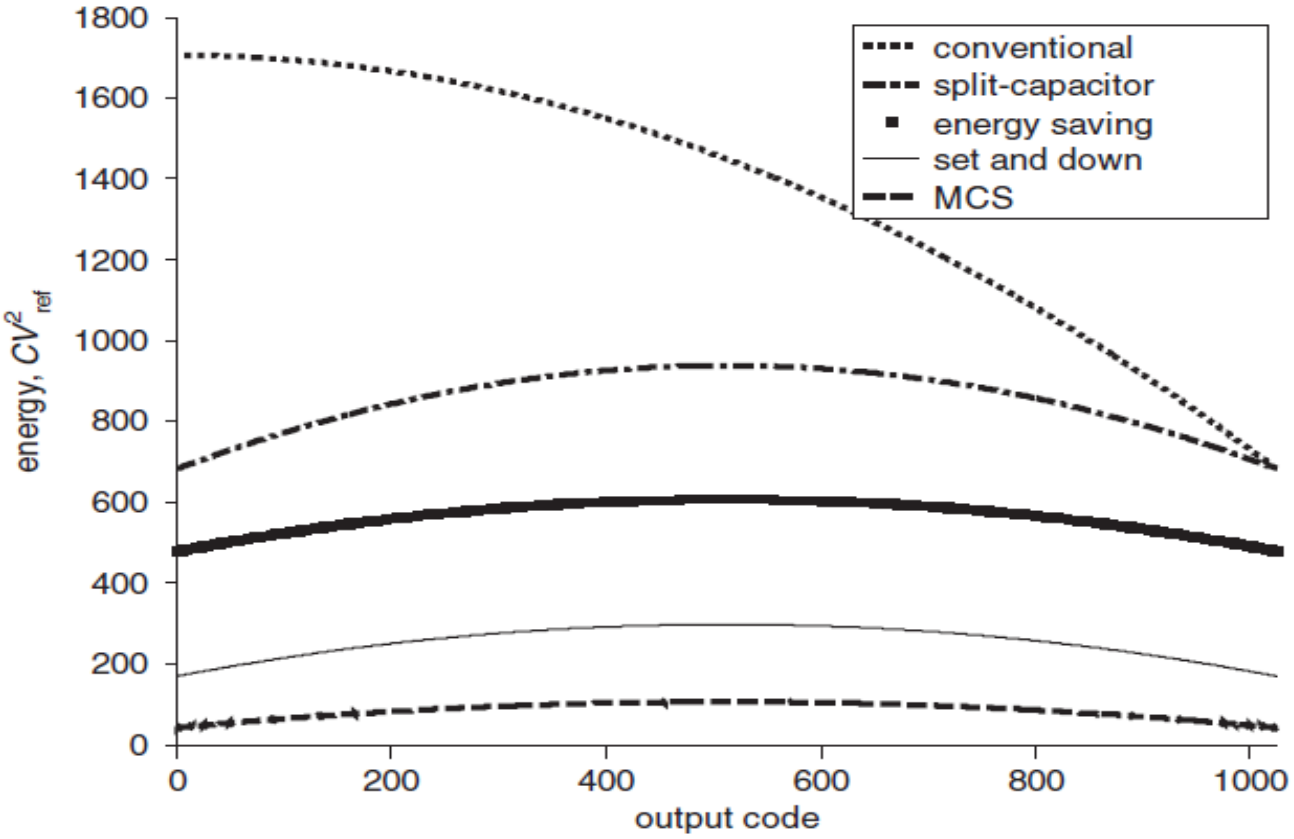
Charge Redistribution



[3 bits example]

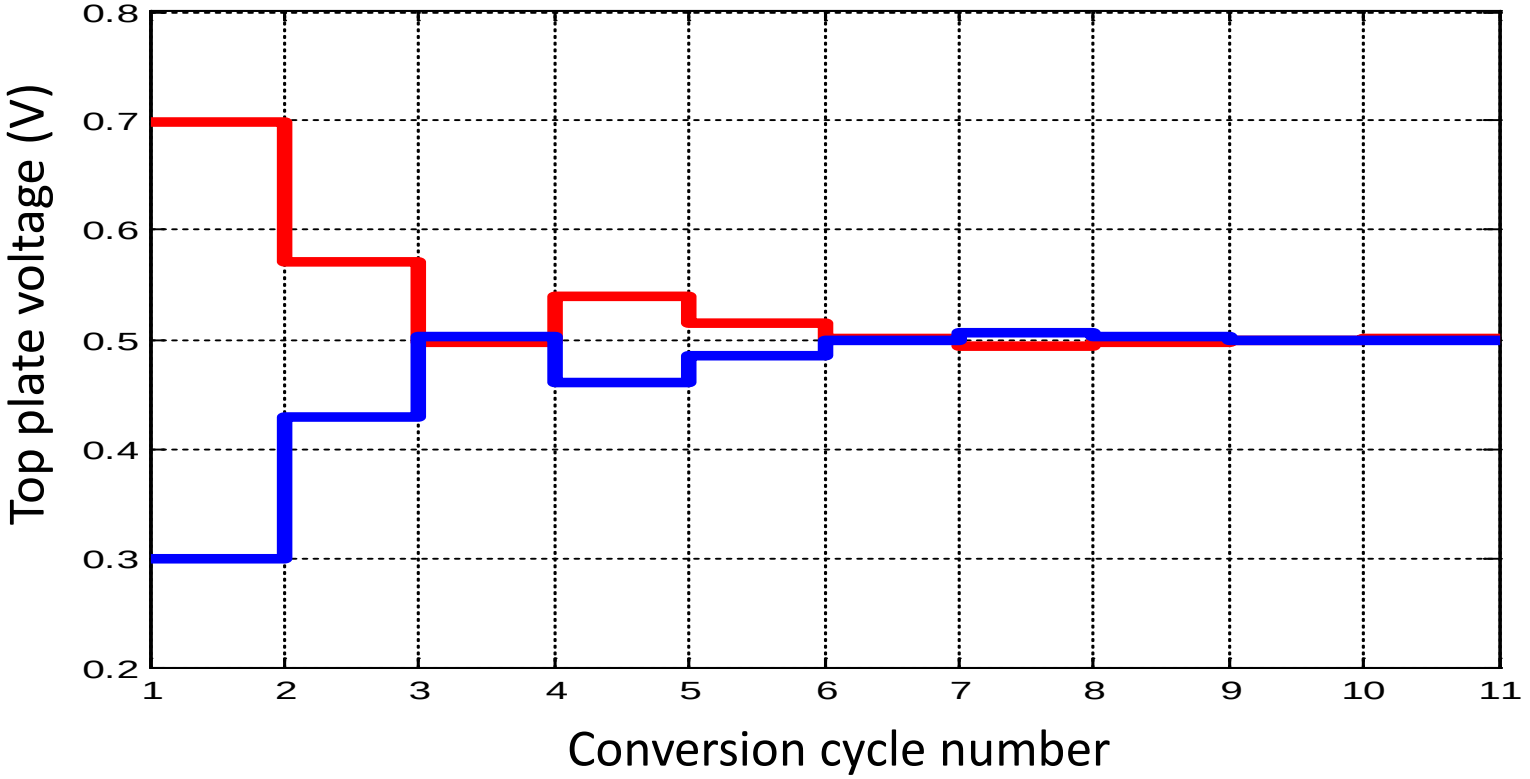
- No switching power for MSB conversion
- 3-level reference (adding Vcm) reduces voltage step/switching power

DAC Switching Efficiency



[Hariprasath & Al., Electronics Letters, Apr. 2010]

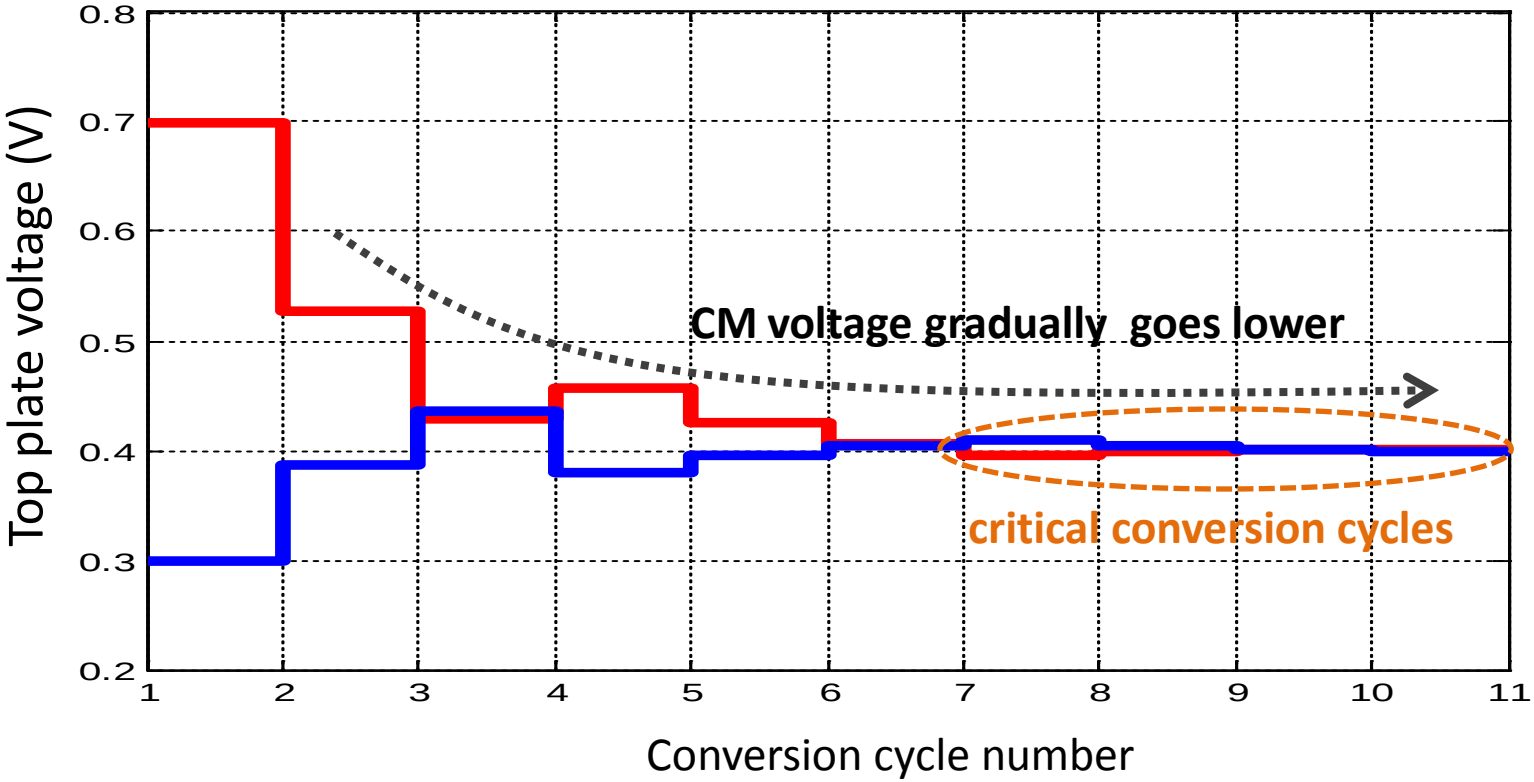
DAC Waveform for Vcm = Vrefp/2



- **Same CM voltage at top-plate of DAC during conversion**

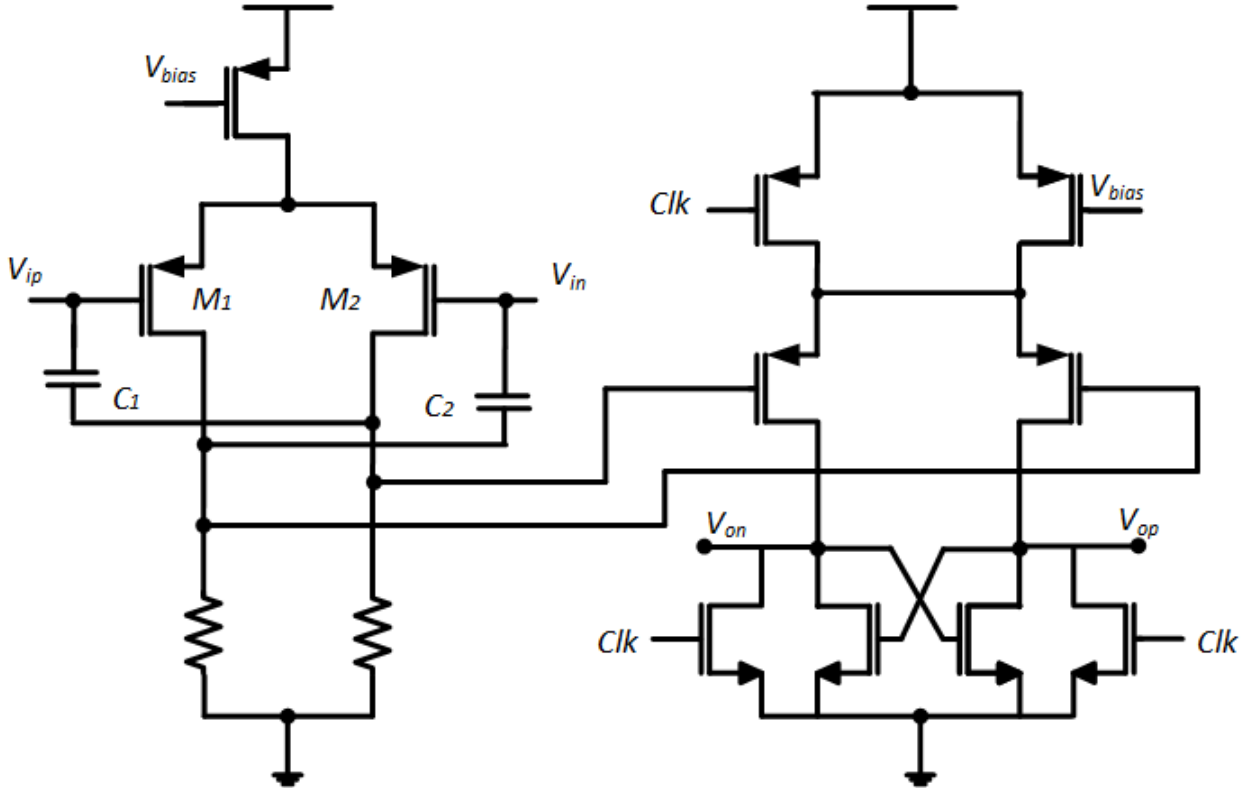
DAC Waveform for Vcm ≠ Vrefp/2

(This design)



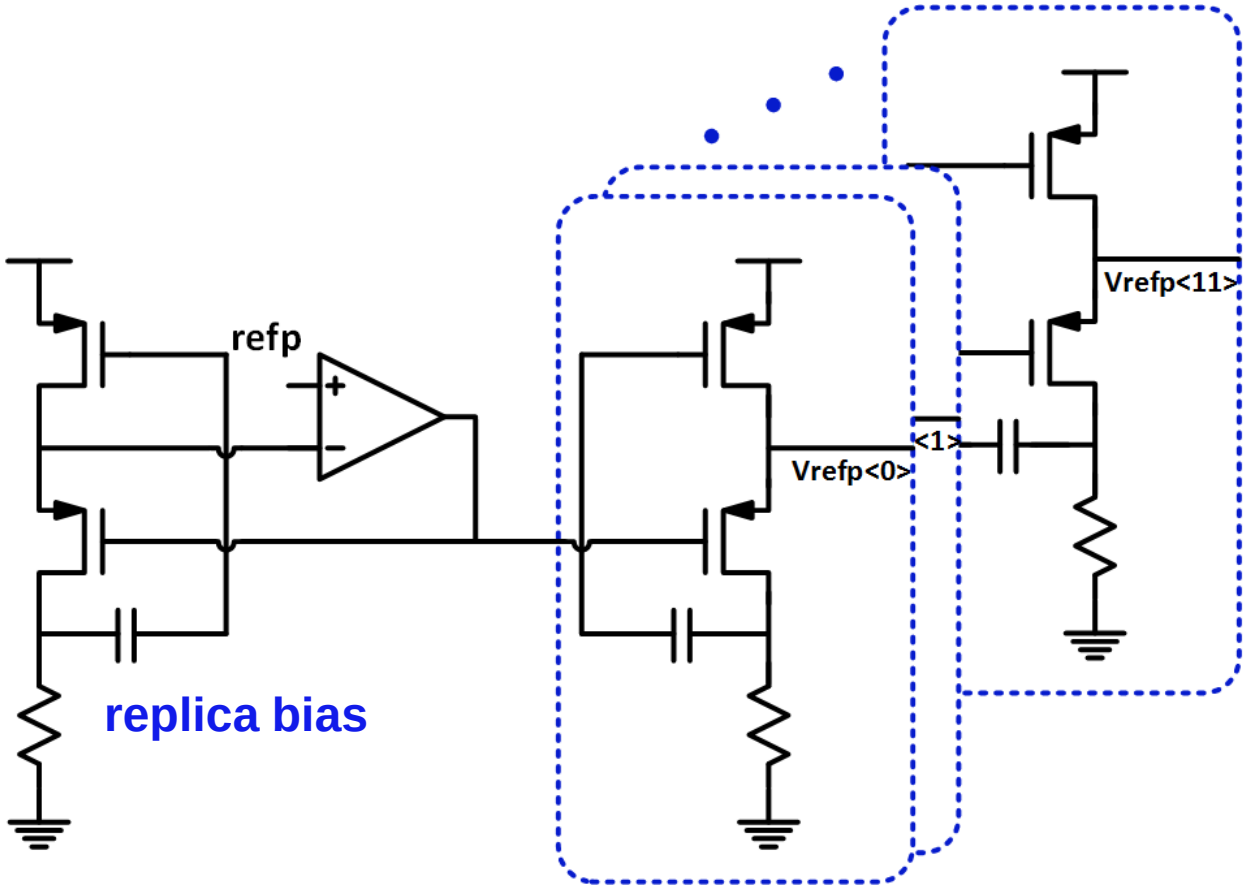
- **DAC top-plate CM voltage gradually goes lower**
  - **Desired for PMOS input comparator in this design**
- **Only the last conversion cycles are critical**
  - **Small voltage for comparator to resolve & No redundancy for LSBs of CDAC**

Comparator



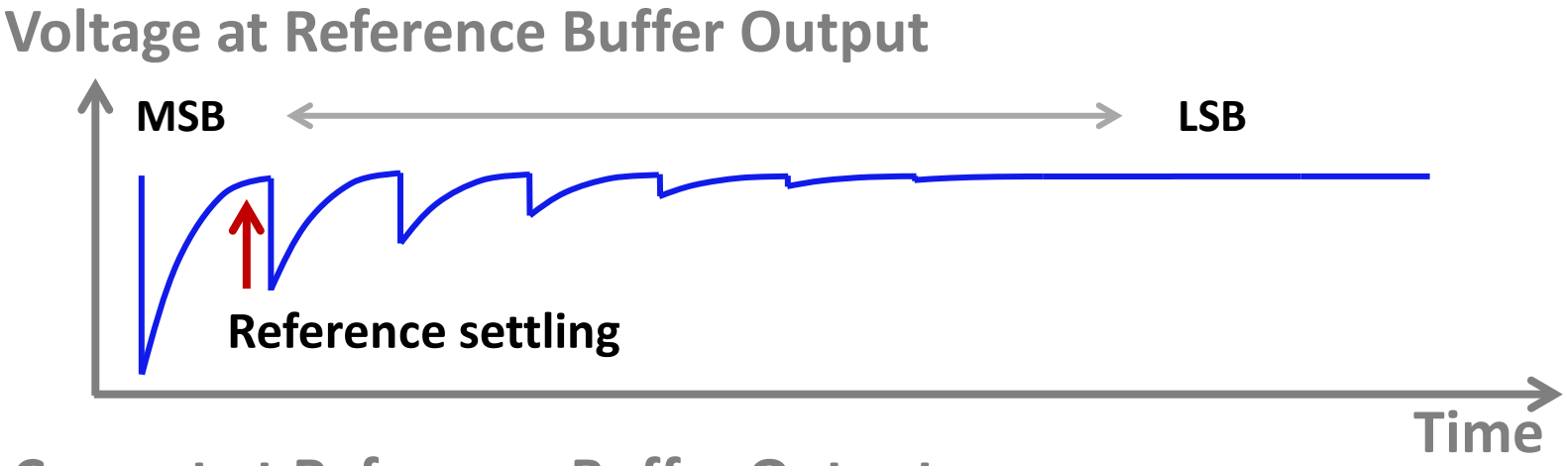
- **PMOS input headroom**
  - **Using Vcm > Vrefp/2 in CDAC to lower input CM → higher speed**
- **Pre-amplifier**
  - **Less noise & less kickback noise from latch**
  - **Cross-coupled C1 and C2 for neutralization → higher speed**

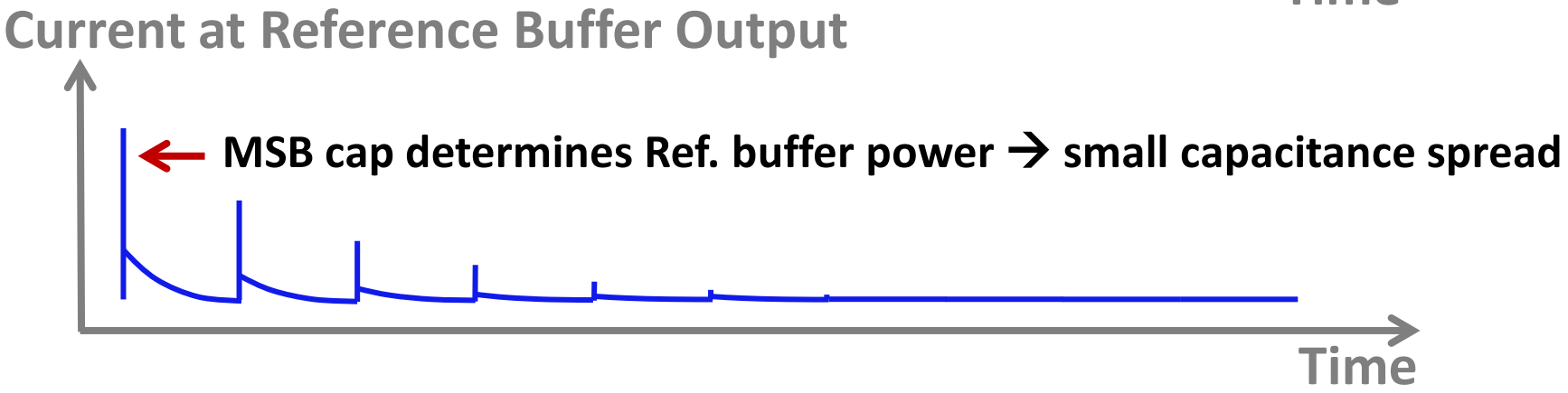
Reference Buffer



- Slow buffer → Too large area or off-chip capacitor for TI ADC
- Low-voltage super source follower for fast settling
- Reference voltage mismatch → Gain mismatch

Reference Considerations





- **Redundancy optimization**
  - Relaxing the buffer settling accuracy →Higher speed, lower power
  - Adding more conversion cycles → Lower speed
- **Small capacitance spread in CDAC for less power**

How to Select Capacitor Ratio?

(Example: 8 bit CDAC with 1 bit redundancy)

Option 1: [32 16 8 8 4 2 1 1]

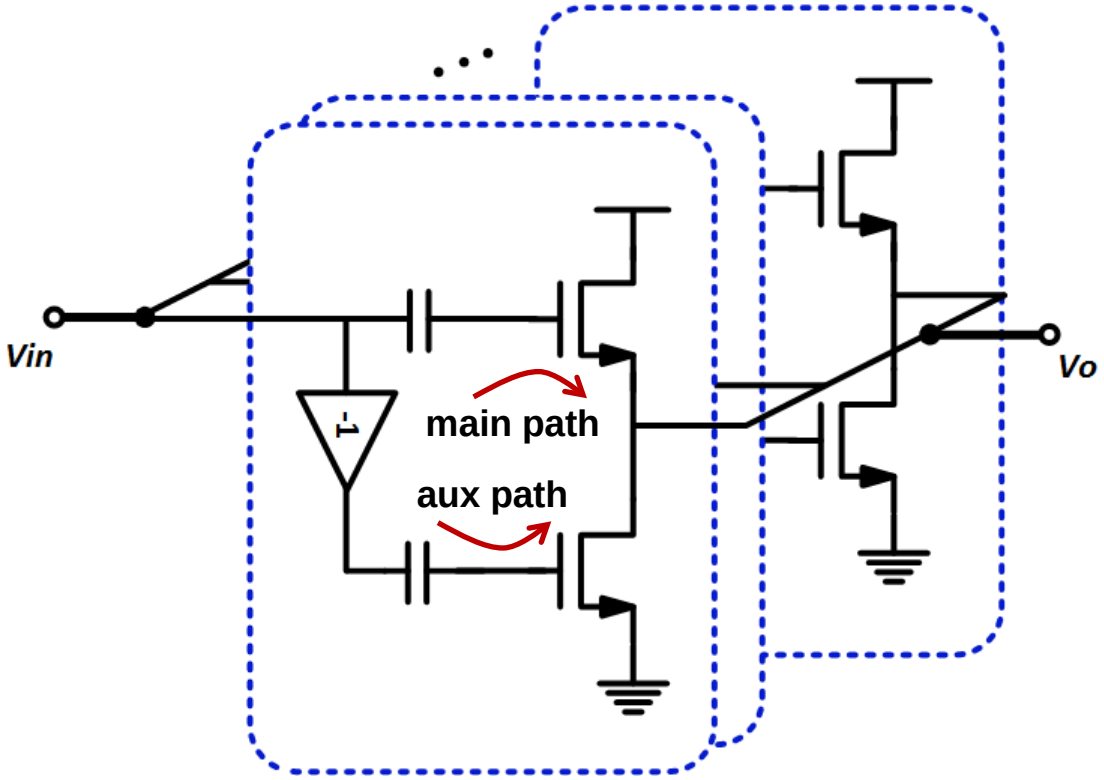
- One redundant bit for the MSBs → more recovery range
- Large MSB → higher power for fast reference buffer

Option 2: [26 18 12 8 4 2 1 1]

[used in this design]

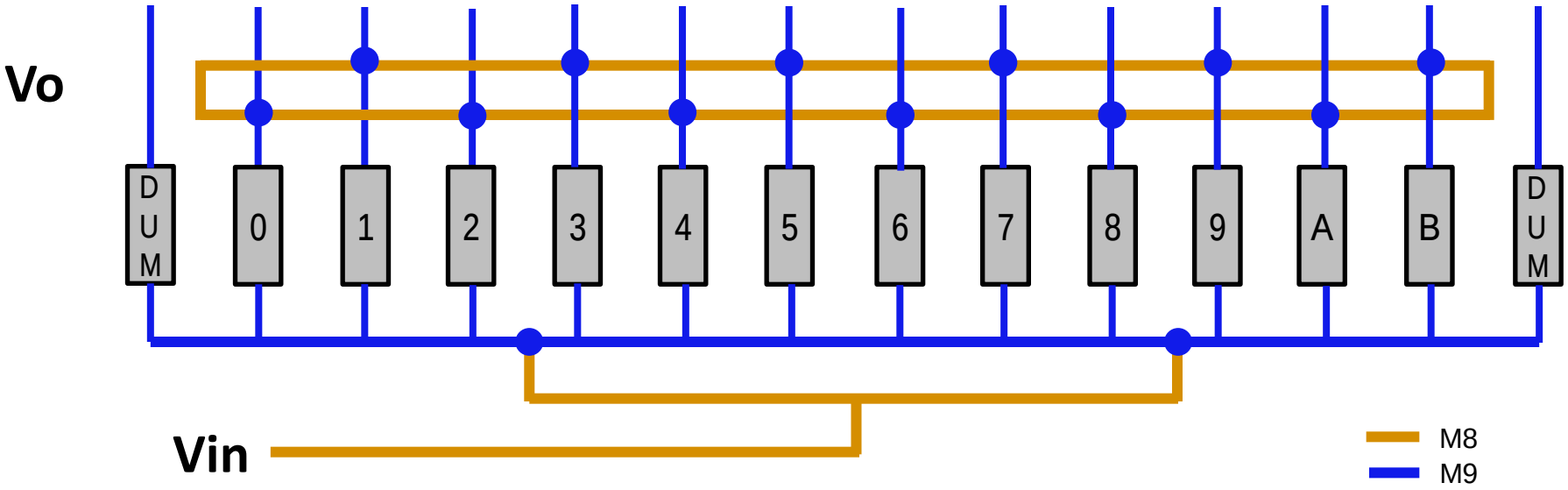
- Multiple redundant bits → slightly less recovery range
- Small capacitor spread
  - Less power for reference buffer
  - Less settling error during the MSBs conversion

Input Buffer



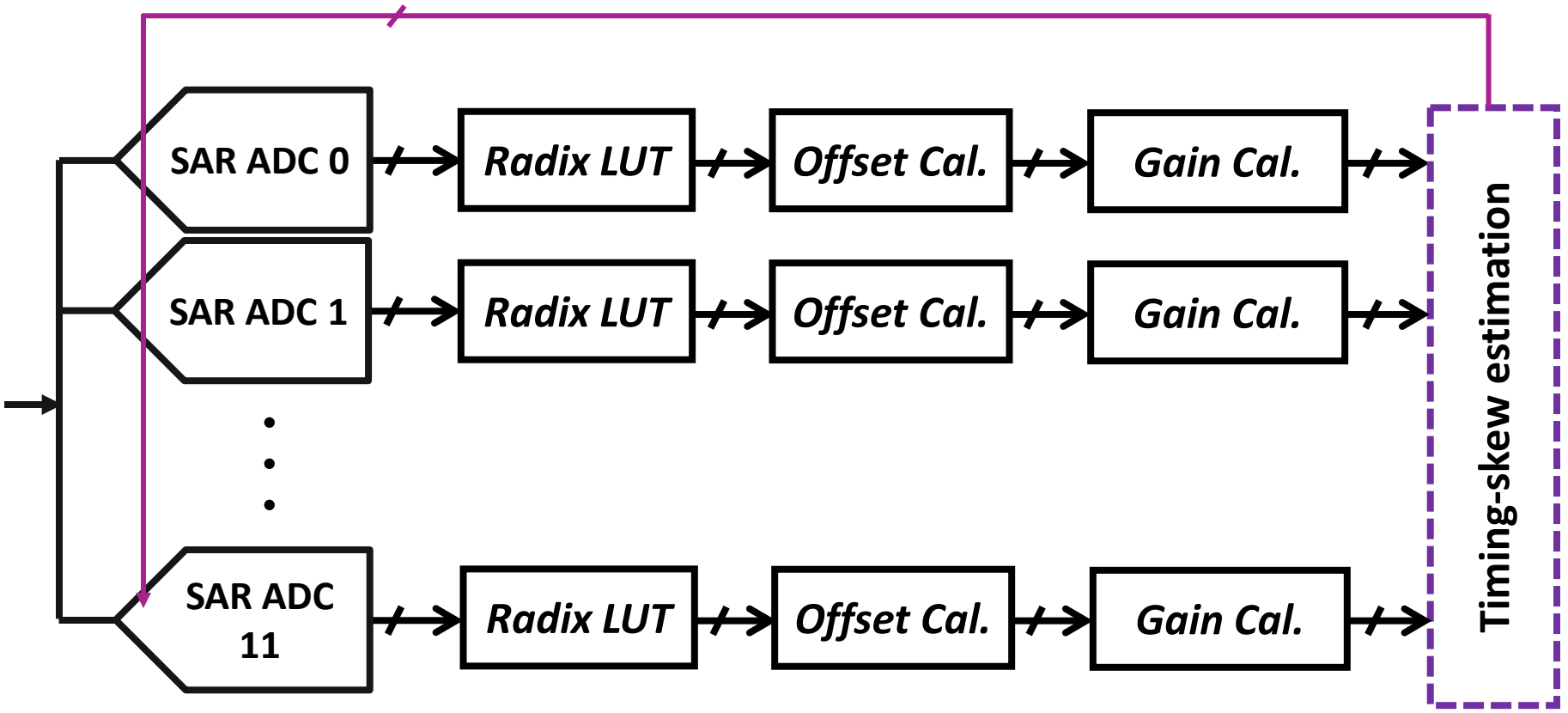
- Flat frequency response for slightly above unity gain
- Limiting ADC kickback to the front end
- Bandwidth & phase mismatch -- shorting output eliminates transistor mismatch

Input Buffer Layout



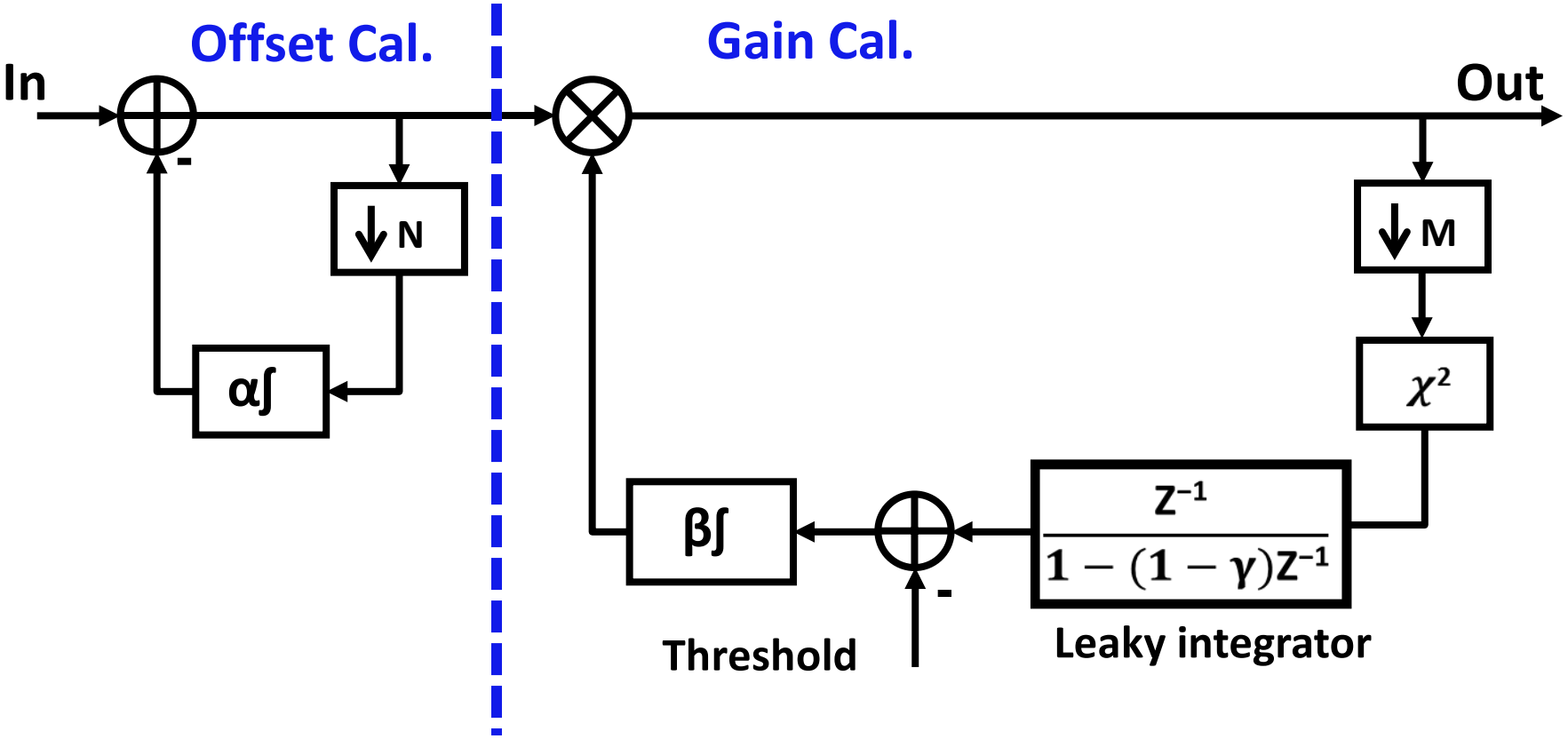
- **Equalizing routing load for both input and output to minimize phase mismatch**

Digital Calibration



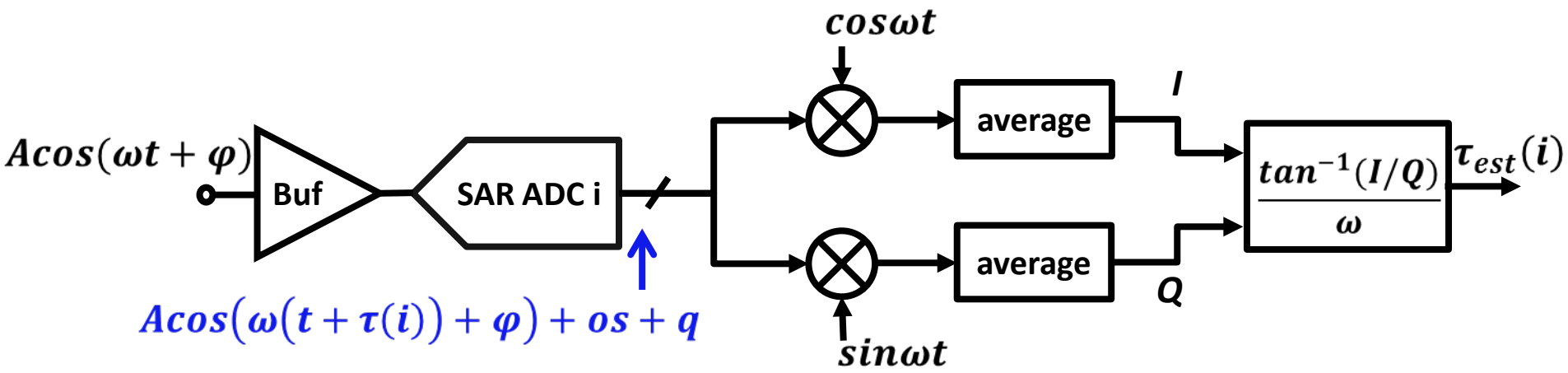
- Digital background calibration for redundancy, offset and gain
- Delay cells for sampling clock are tuned to minimize timing skew

Digital Offset & Gain Calibration



- Threshold sets the code range for all ADC lanes
- Decimation for less power
  - Both offset and gain of sub-ADC are moving slowly

Timing Skew Estimation



$$I=\overline{(A\cos(\omega(t+\tau(i))+\varphi)+os+q)\cdot\cos(\omega t)}=0.5A\cos(\omega\tau(i)+\varphi)$$

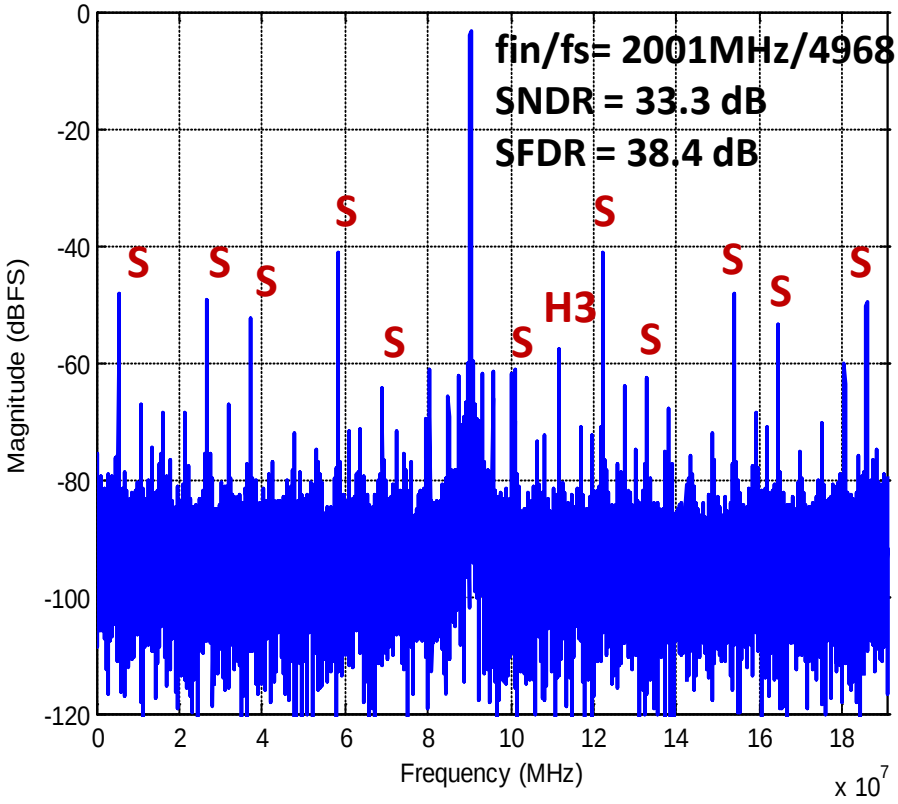
$$Q=\overline{(A\cos(\omega(t+\tau(i))+\varphi)+os+q)\cdot\sin(\omega t)}=0.5A\sin(\omega\tau(i)+\varphi)$$

$$\tau_{est}(i)=\frac{\arctan(Q/I)-\varphi}{\omega}$$

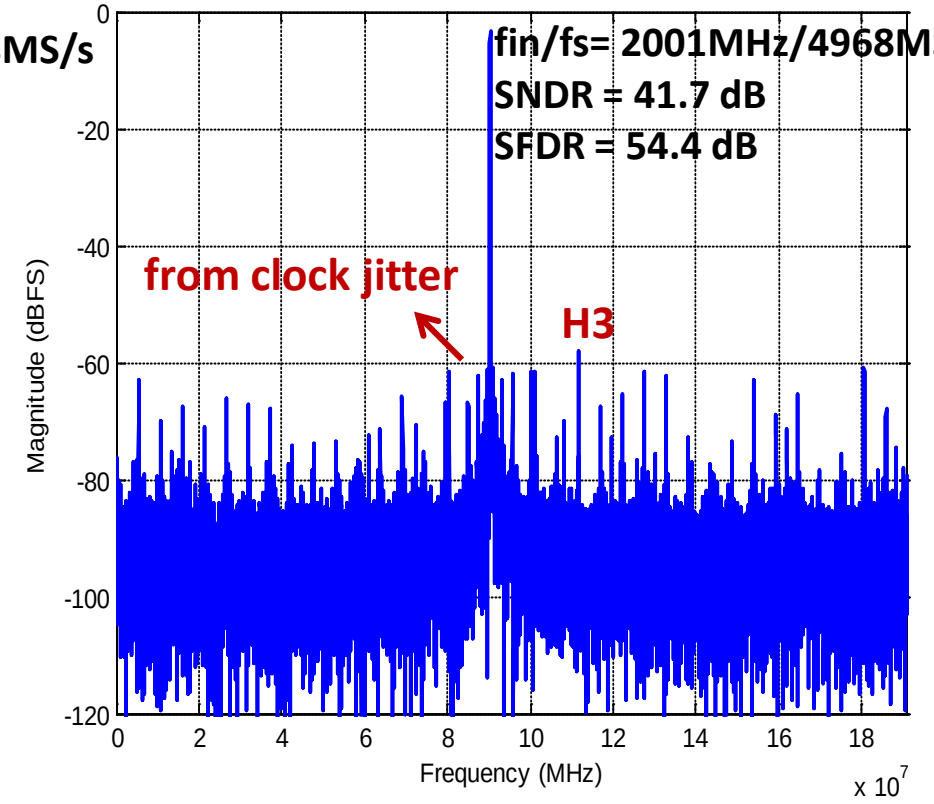
- **Insensitive to signal amplitude, offset and quantization noise**

Output Spectrum of ADC

Before timing Calibration

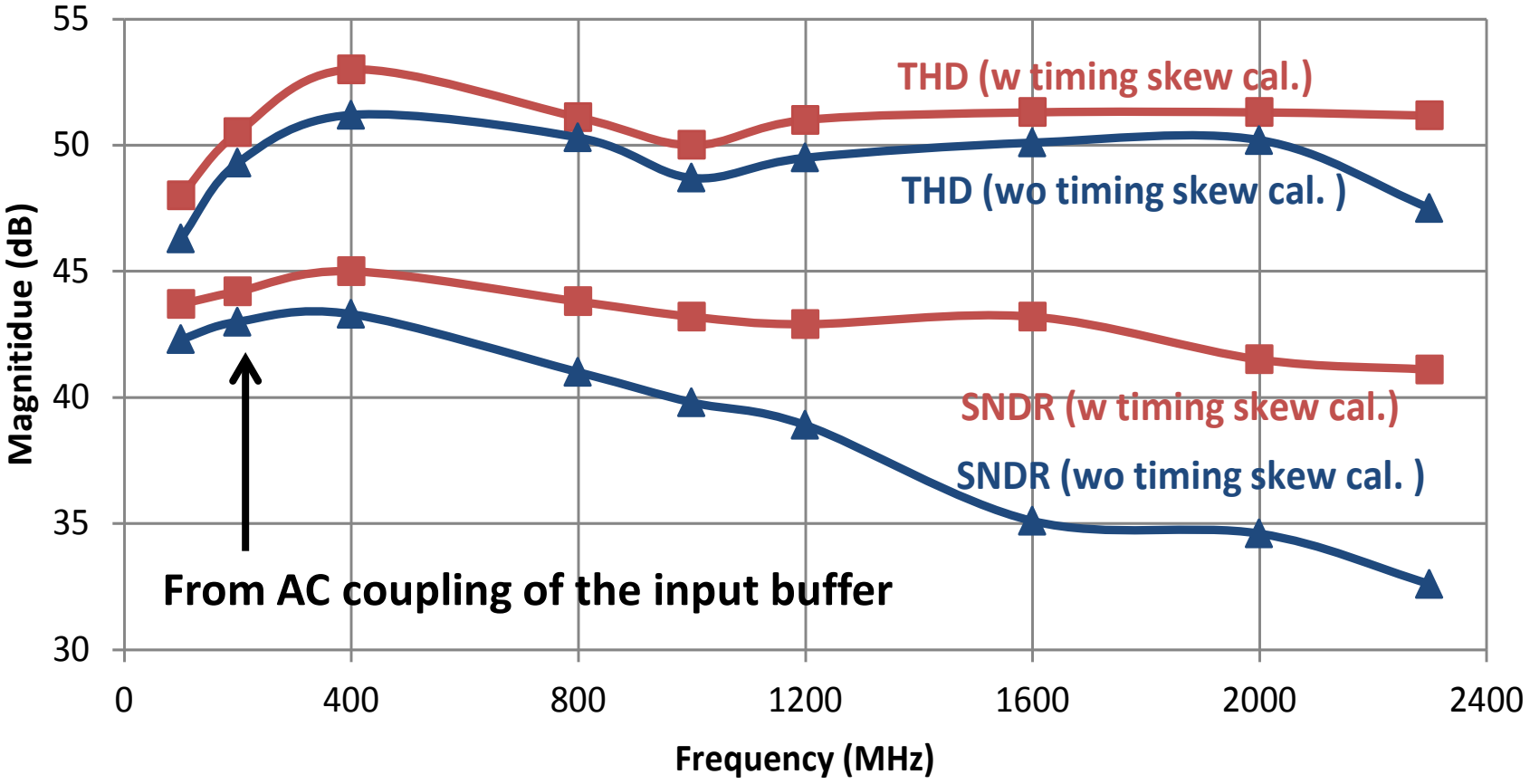


After timing calibration

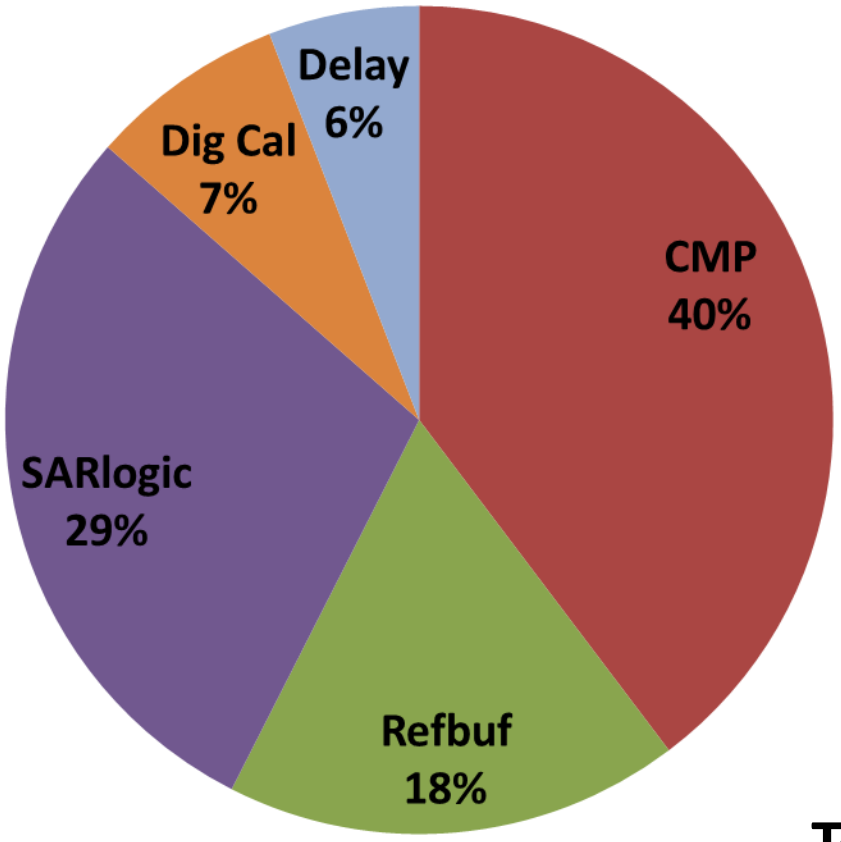


Note: Output data is decimated by 13

THD & SNDR versus Input Frequency

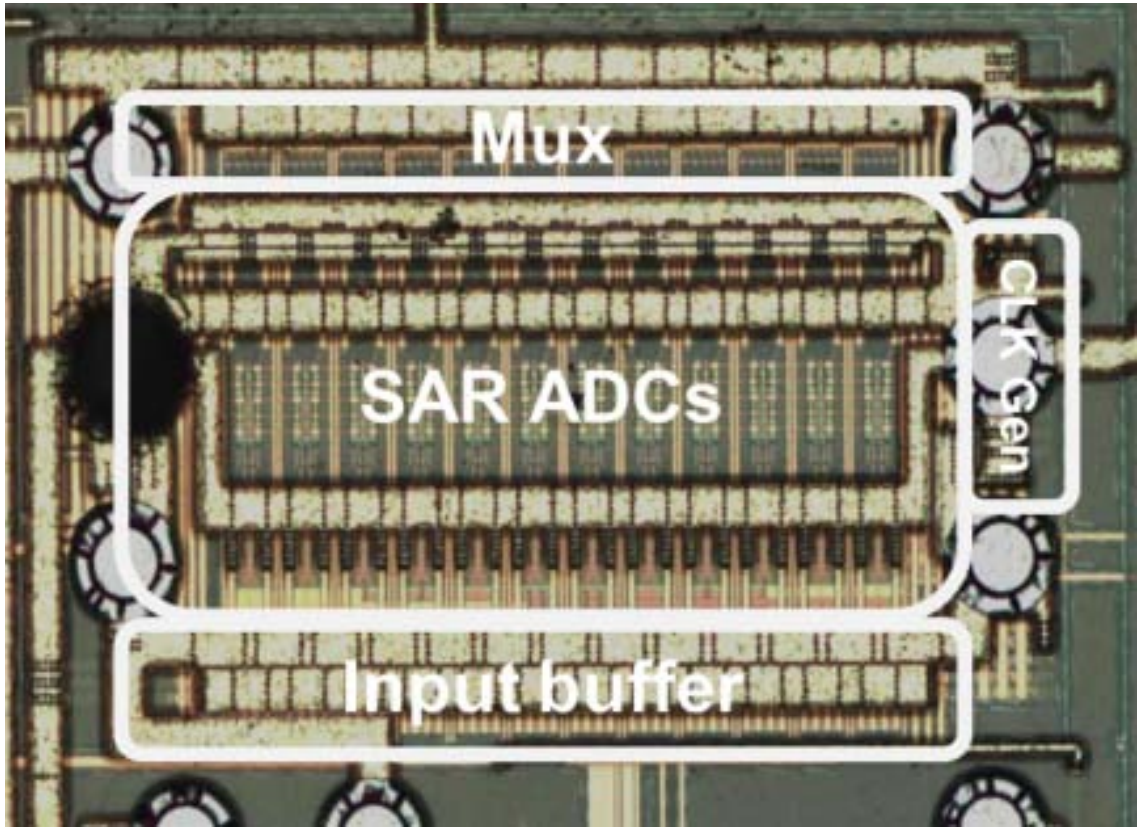


Power Breakdown



Total power: 76mW

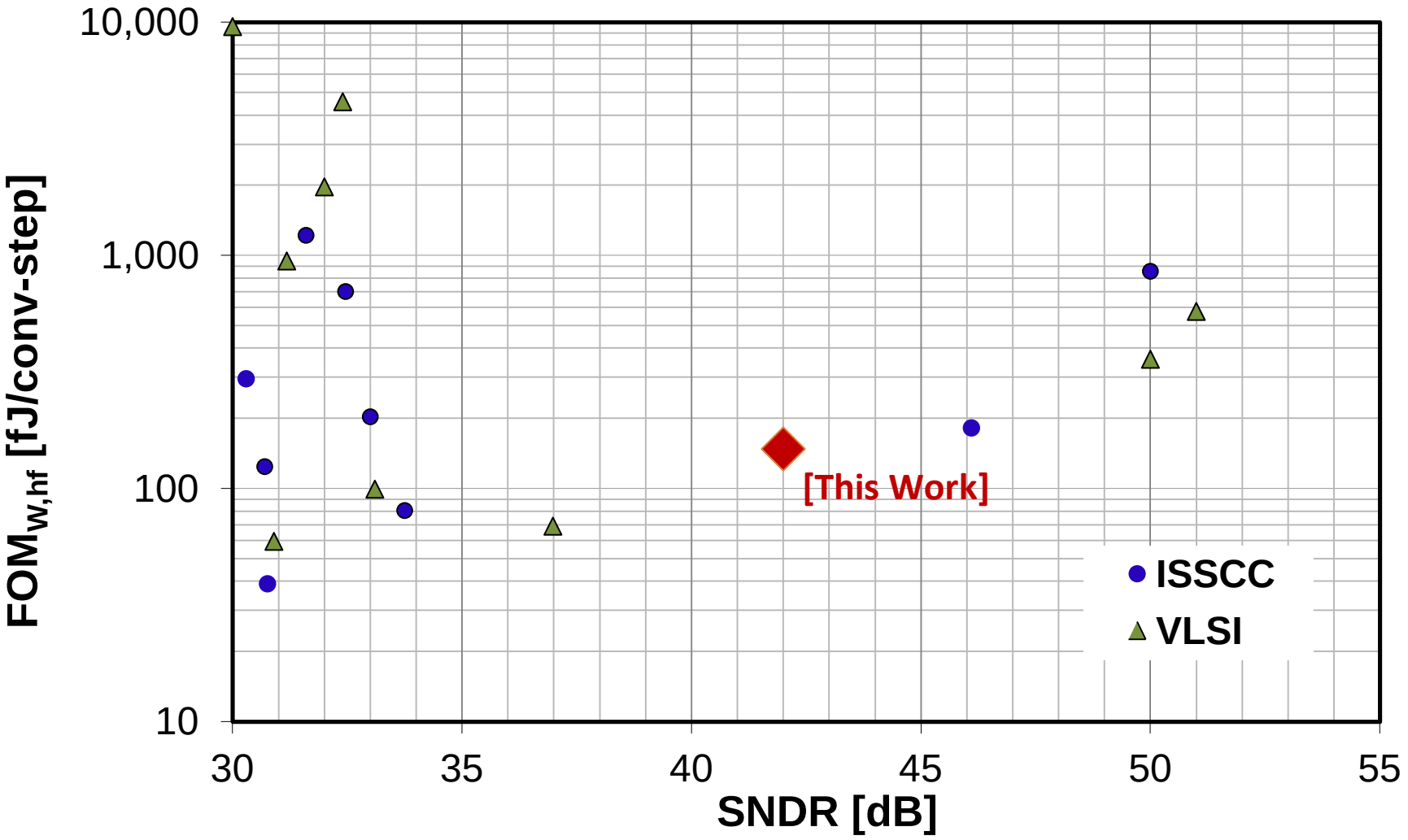
Die Photo



Measurement Results

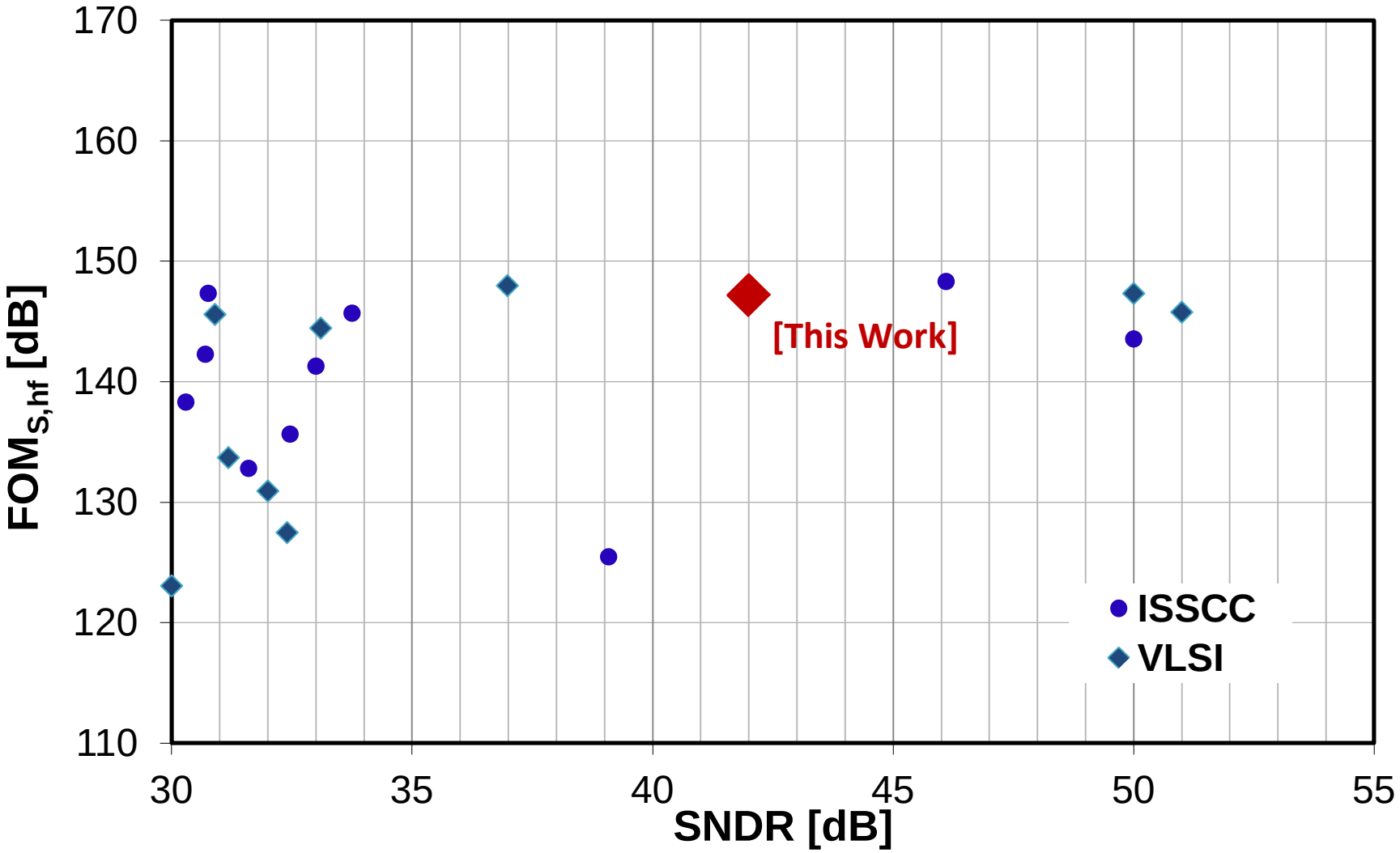
Parameters	[1] ISSCC2014	[2] ISSCC2013	[3] VLSI2013	[4] VLSI2013	This work
Architecture	TI SAR	TI SAR	TI Pipeline	TI SAR	TI SAR
Technology	40nm	65nm	28nm	32nm SOI	28nm
Supply voltage (V)	1.1	1.2	1	1	1
Fs (GS/s)	1.62	3.6	5.4	8.8	5
Resolution (bit)	9	11	12	8	10
SNDR @ Nyquist (dB)	48	50	50	37	42
Power (mW)	93	795	500	35	76
FoM (fJ/step)	279	855	358	68.9	165
Area (mm^2)	0.83	7.4	0.4	0.025	0.57

Walden FOM Comparison (Fs>3GHz)



- **Best Walden FOM for SNDR >40dB and Fs>3GHz**

Schreier FOM Comparison (Fs>3GHz)



- **Best-in-class Schreier FOM for SNDR >40dB and Fs>3GHz**

Conclusions

- **A 5GS/s 10b ADC for direct sampling receiver**
- **Analog techniques minimizing analog impairments**
- **Digital calibration solving lane-to-lane mismatches**
- **Achieving best Walden FOM and Schreier FOM for SNDR>40dB and Fs>3GHz**

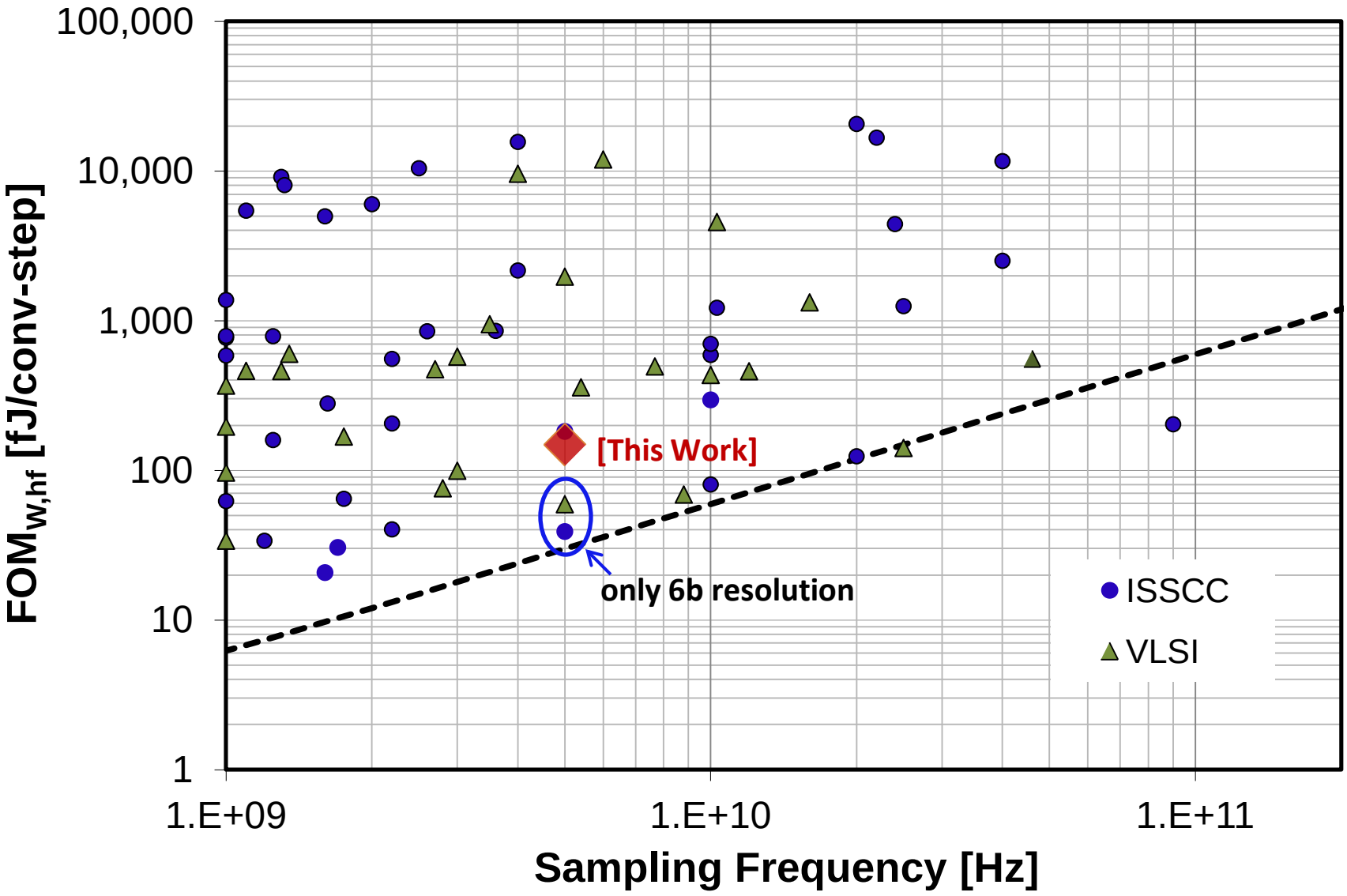
Acknowledge

- **Ardie Venes, Kim Ng, Bob Richens, and Maung Oo from Broadcom Corp.**
- **Jacob Abraham from University of Texas at Austin**

Thank You!

APPENDIX

Walden FOM Comparison



Schreier FOM Comparison