A 0.073-mm^2 10-GS/s 6-bit Time-Domain Folding ADC in 65-nm CMOS with Inherent DEM

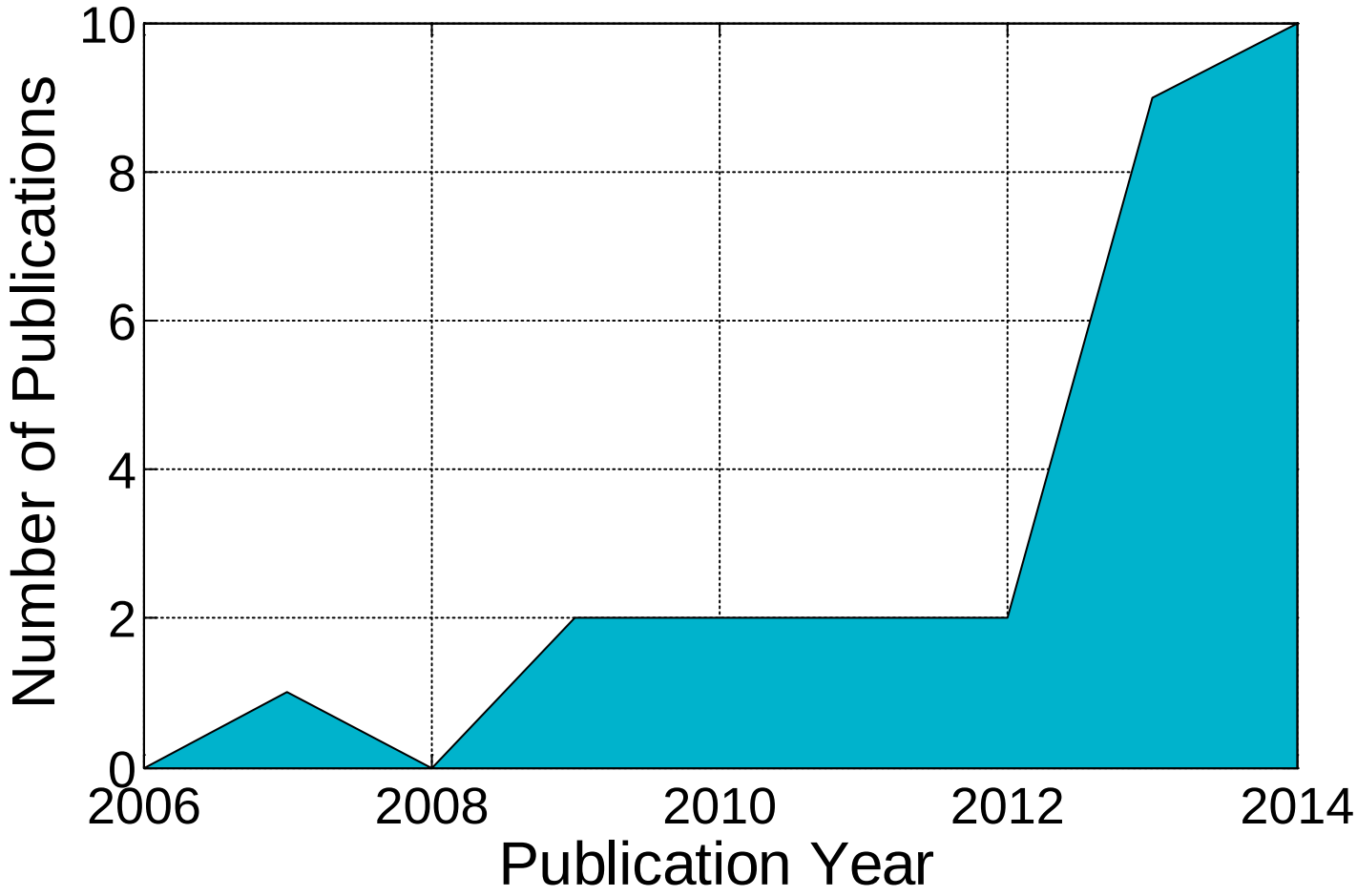
Shuang Zhu, Benwei Xu, Bo Wu, Kiran Soppimath, and Yun Chiu

Analog and Mixed-Signal Lab, Texas Analog Center of Excellence
University of Texas at Dallas

Outline

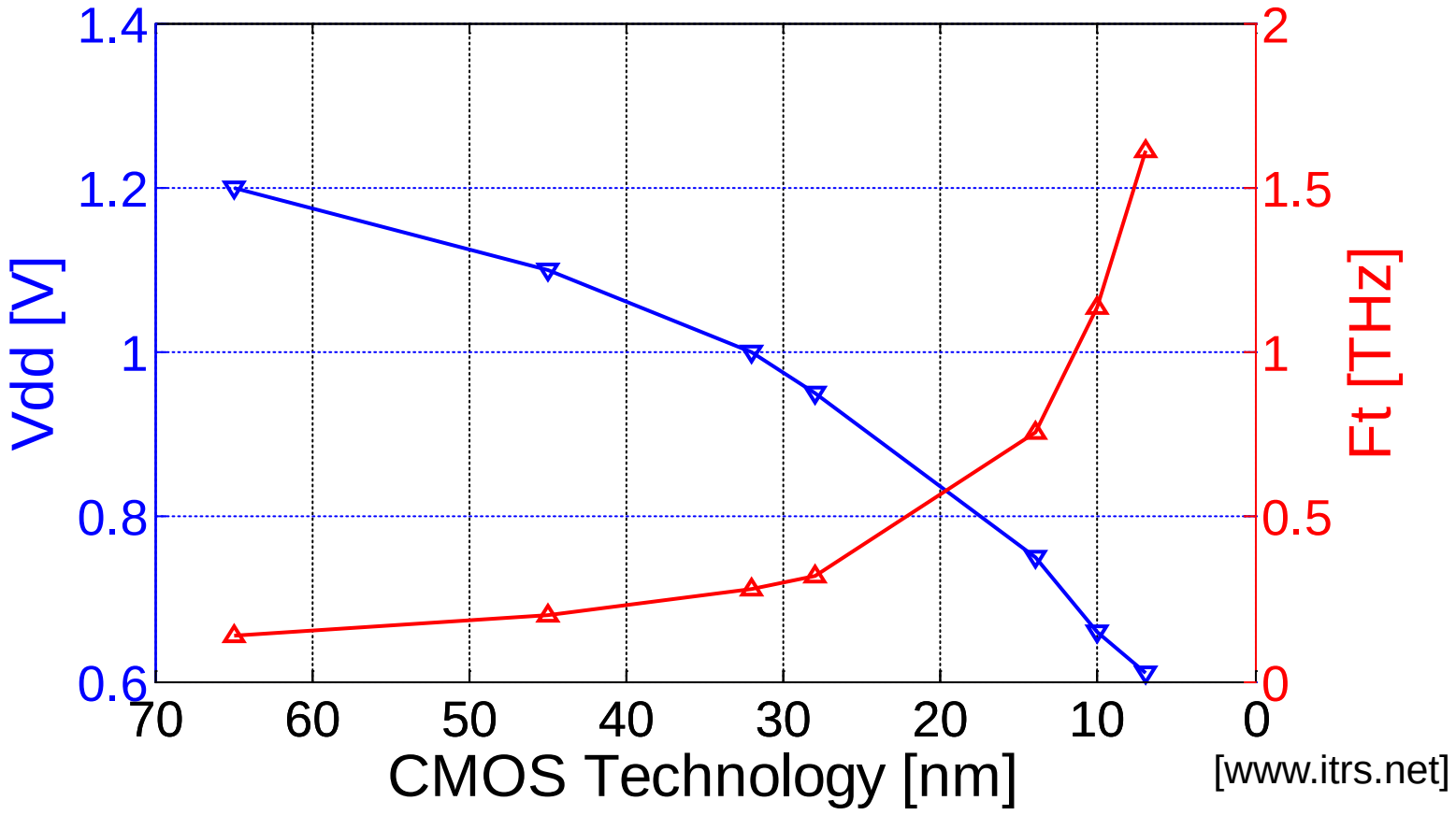
- **Motivation for Time Domain**
- Time to Digital Converter
- Voltage to Time Converter
- Other Circuits
- Measurement Results
- Conclusion

Publications of Time-Domain ADCs



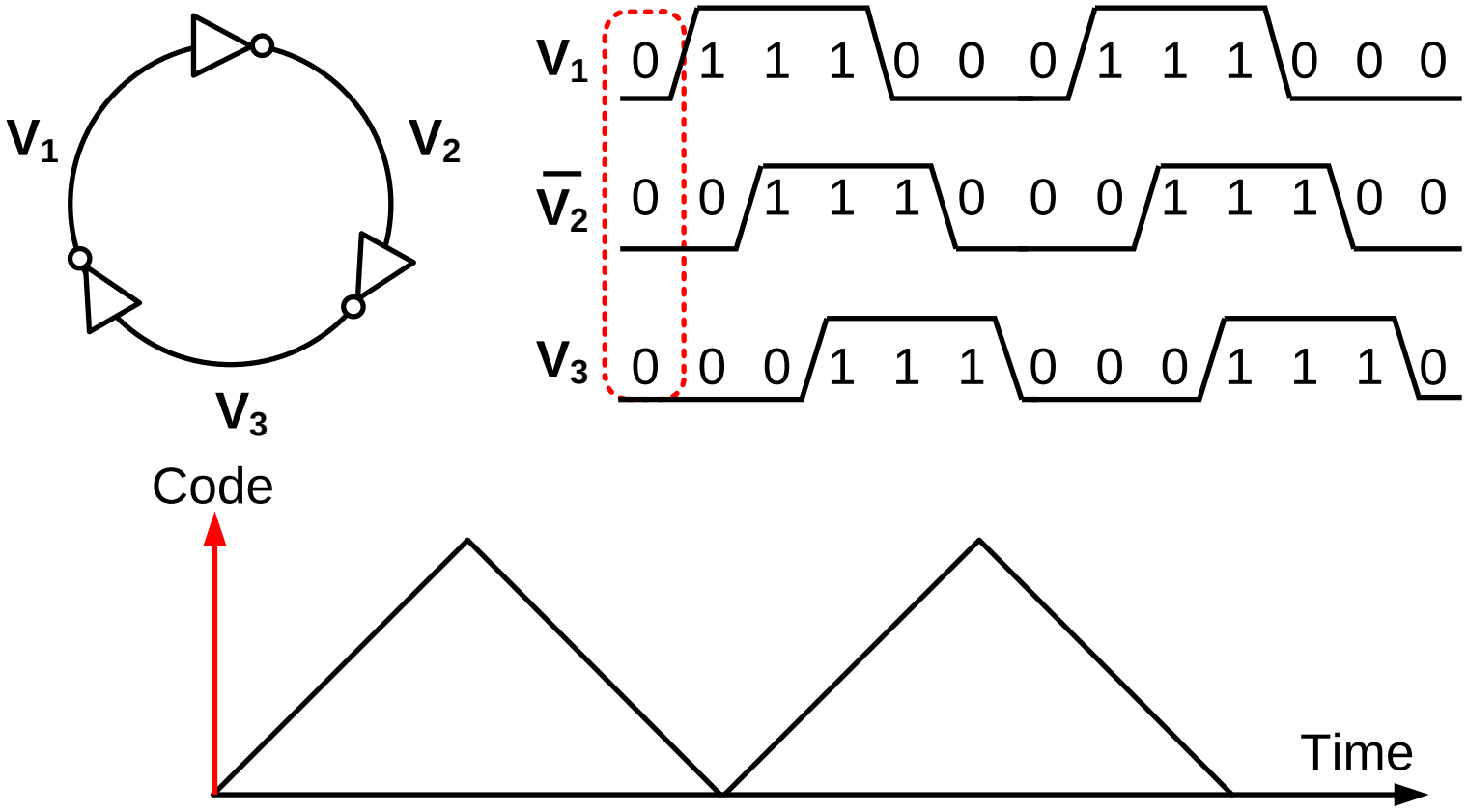
Source: ISSCC, VLSI, CICC, ESSCIRC, ASSCC

CMOS Technology Trend



- Supply voltage ↓→ voltage-domain losing resolution
- Ft ↑ → time-domain gaining resolution

Ring Osc. (RO) Based Folding TDC



- Folding – high area efficiency w/ flash-like speed
- Quantization – LSB size of inv. delay

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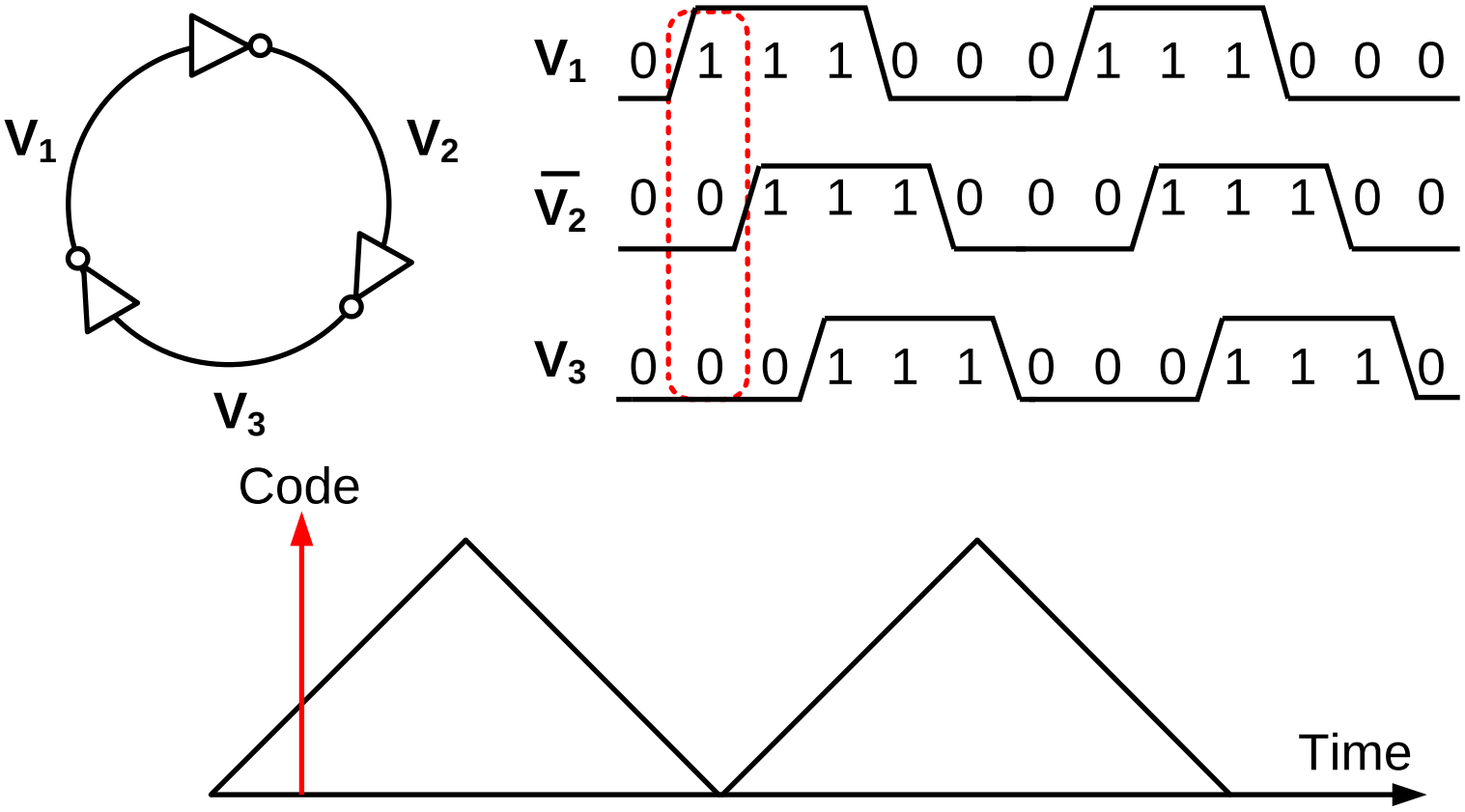

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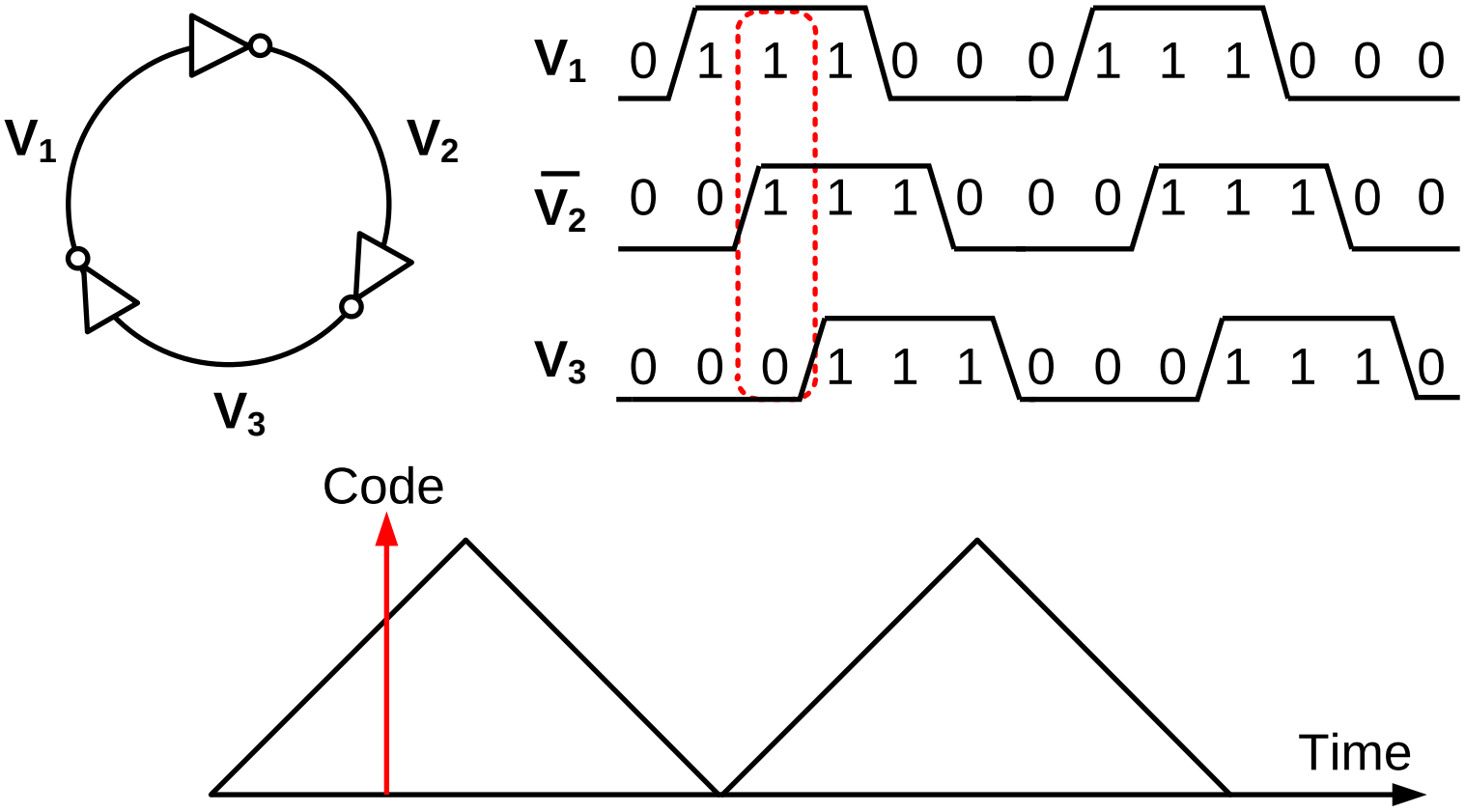

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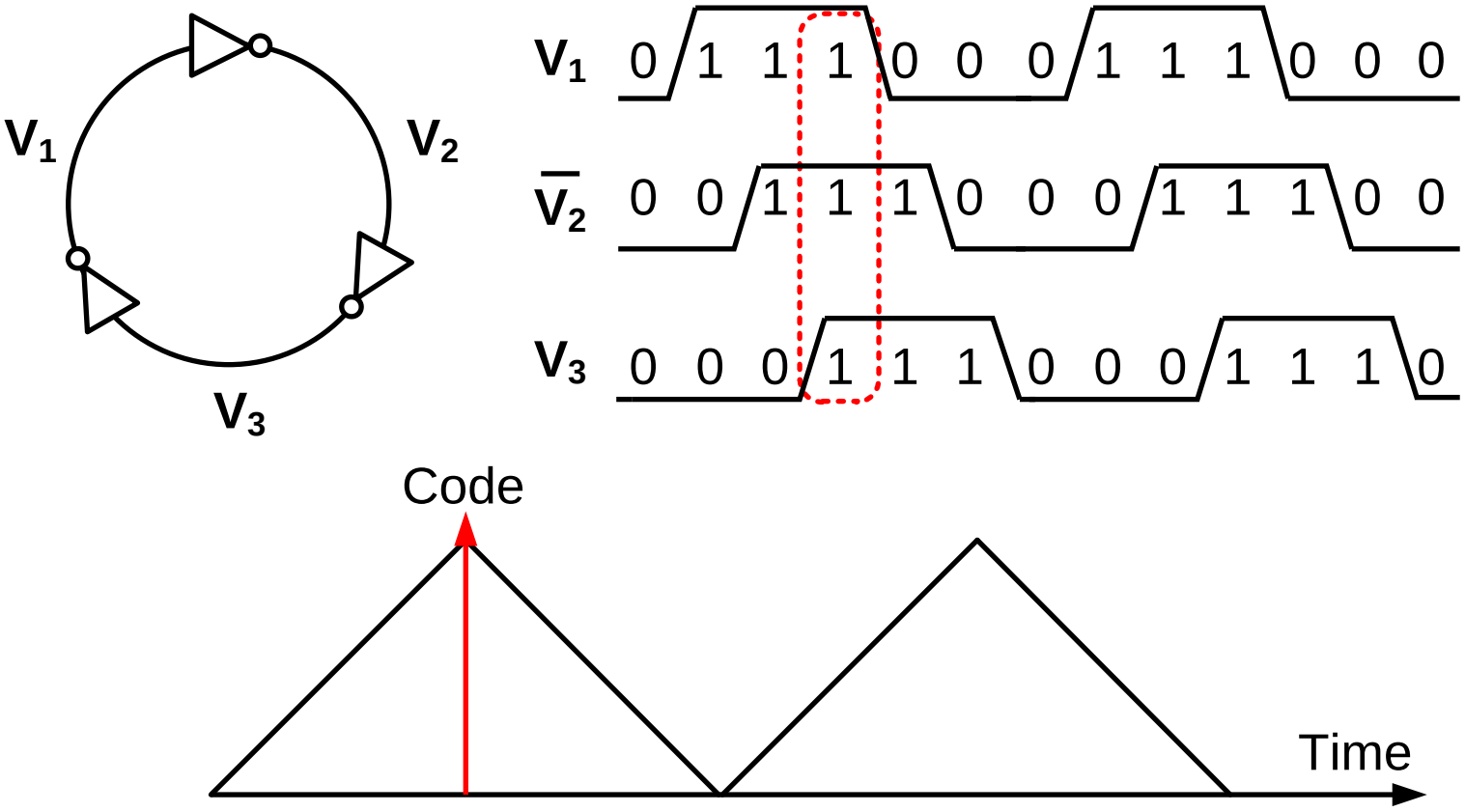

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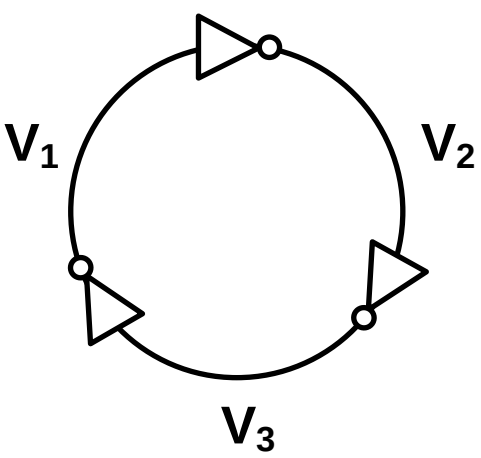

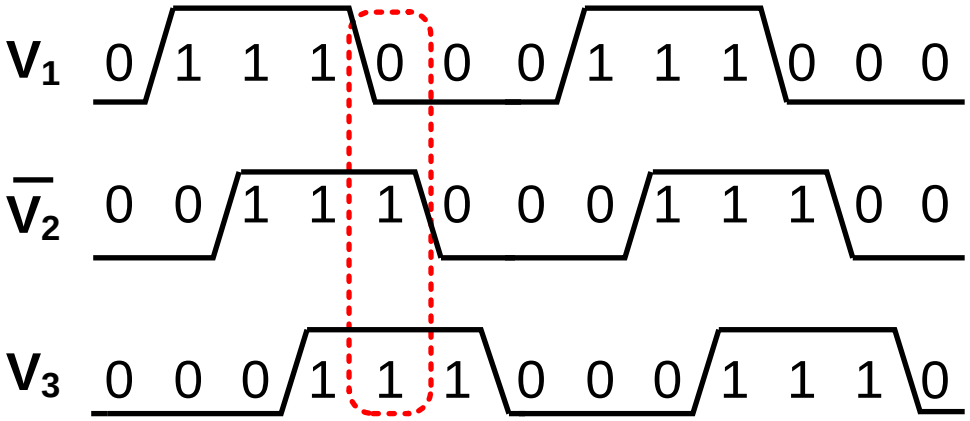

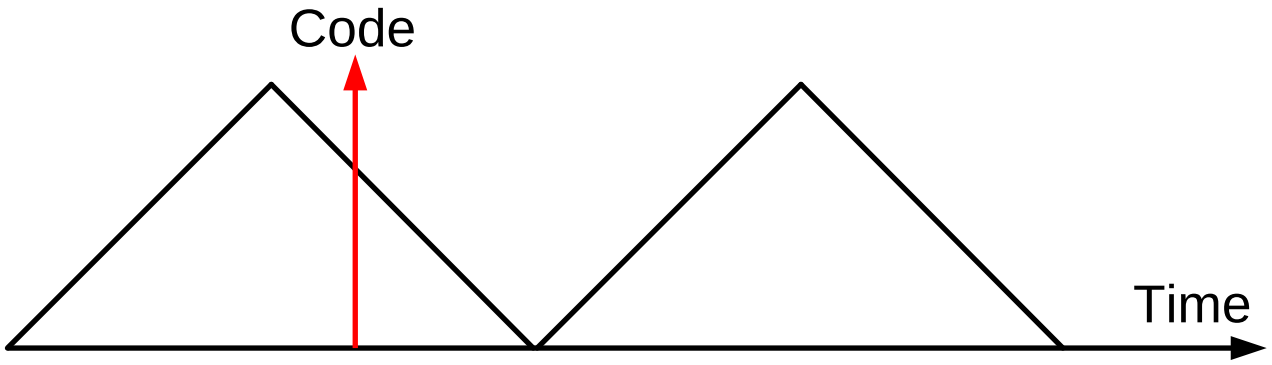

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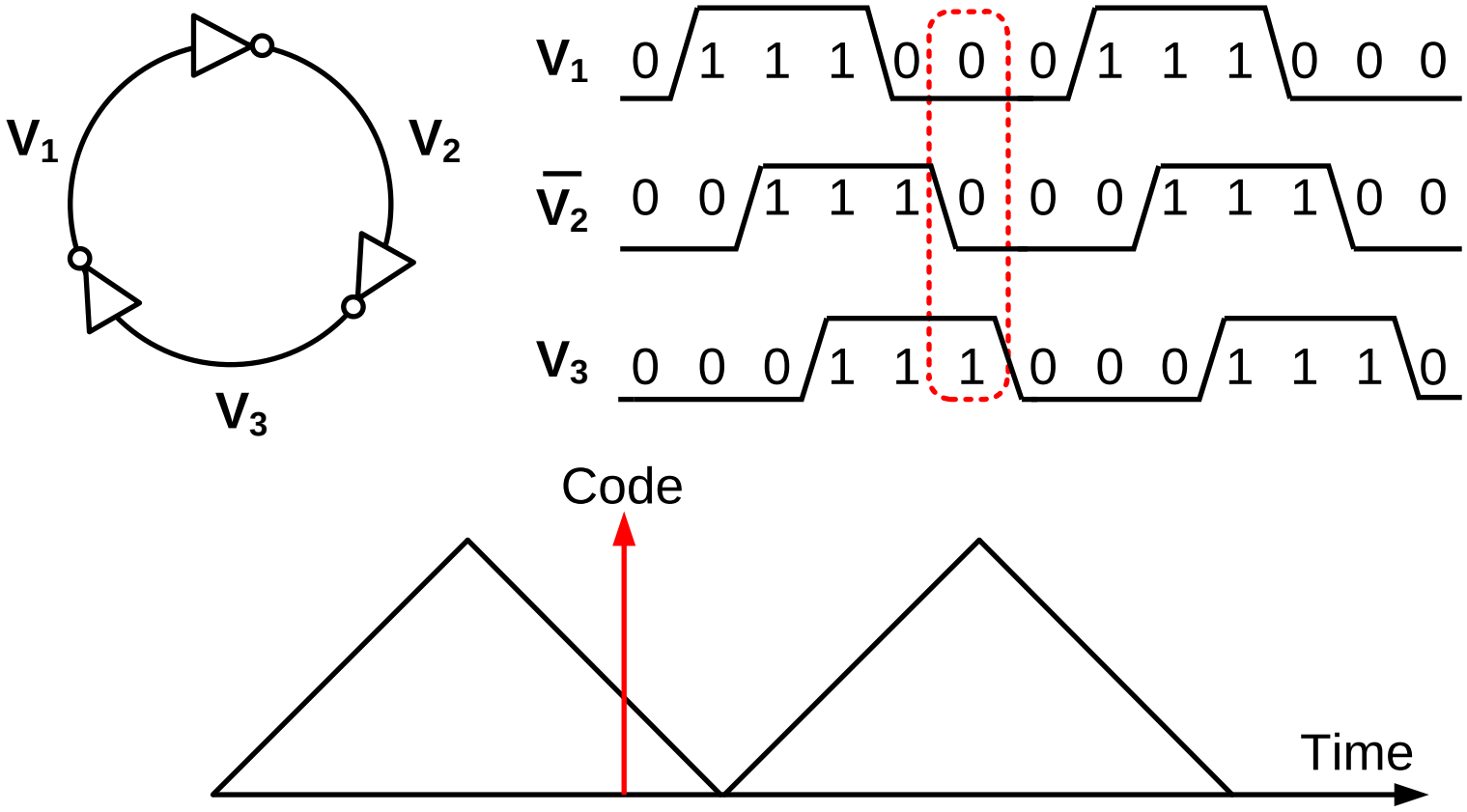

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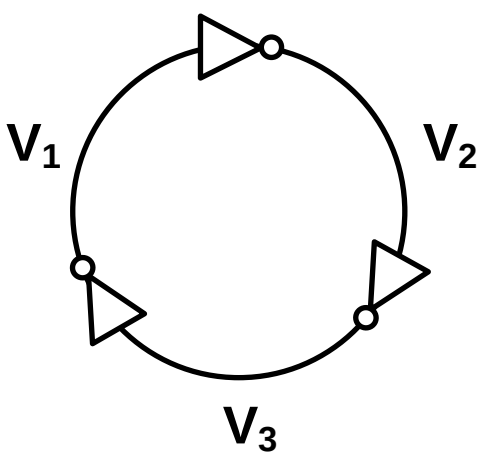

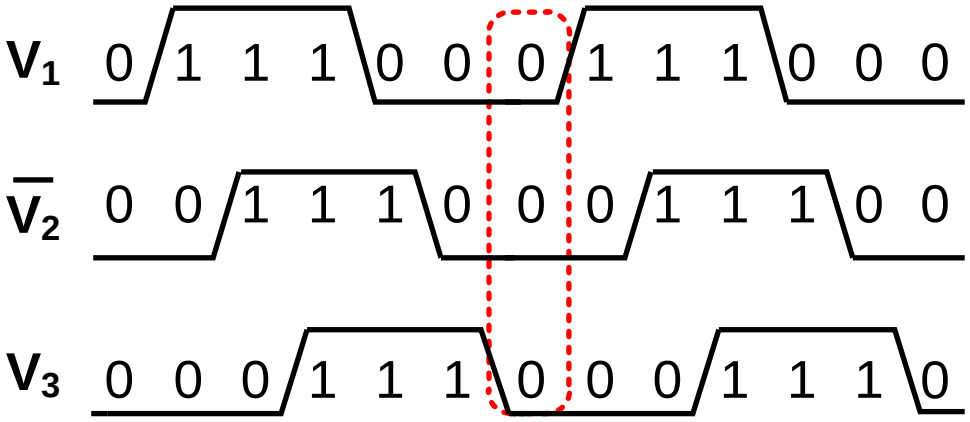

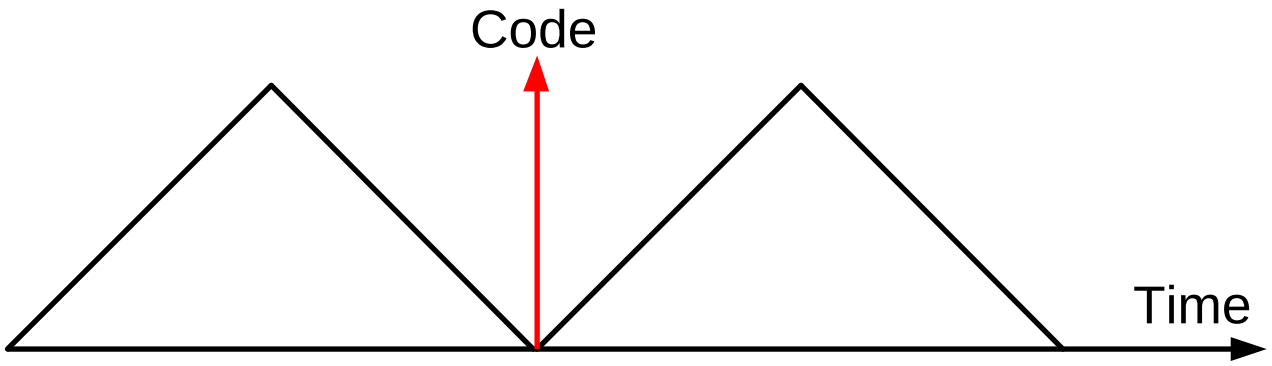

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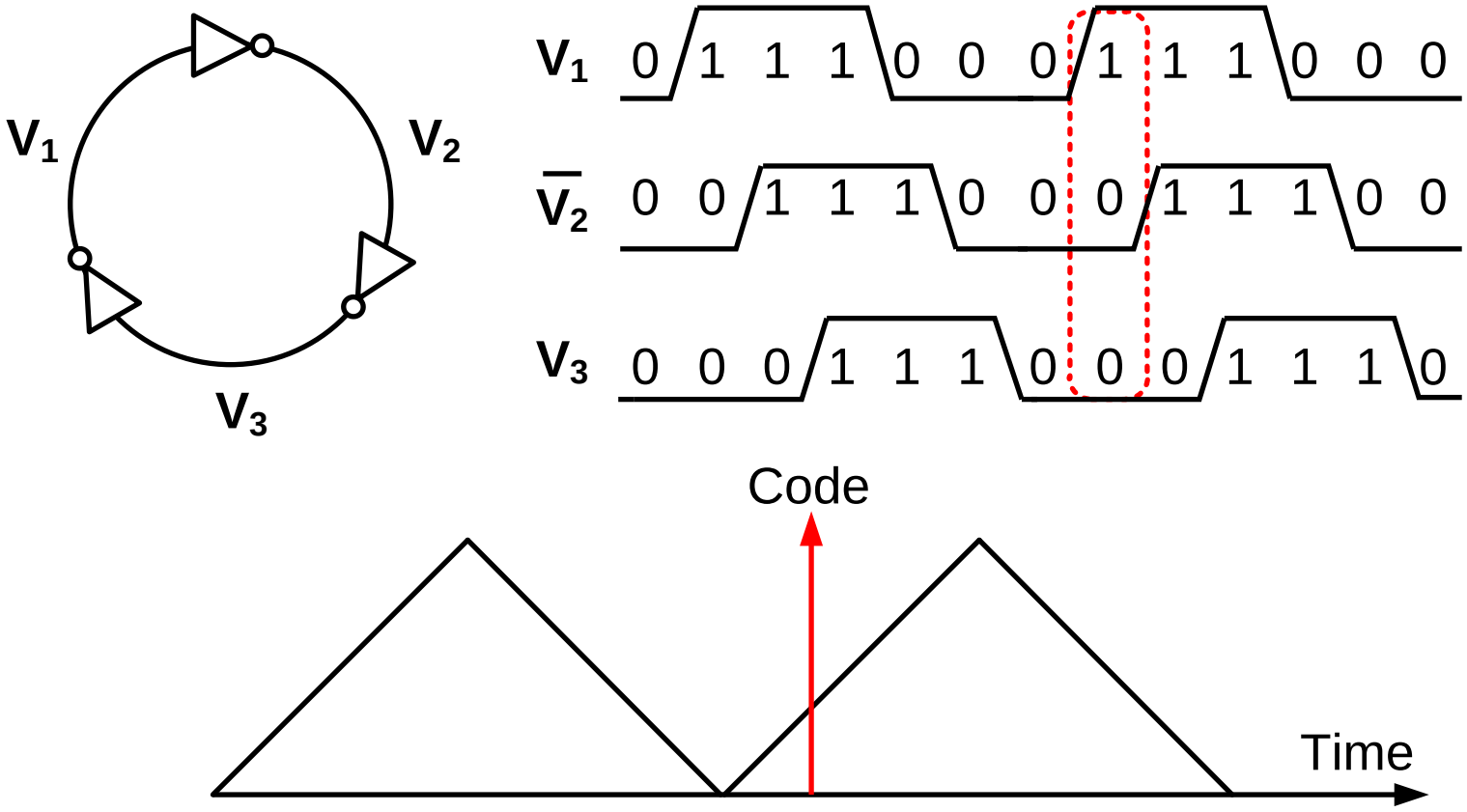

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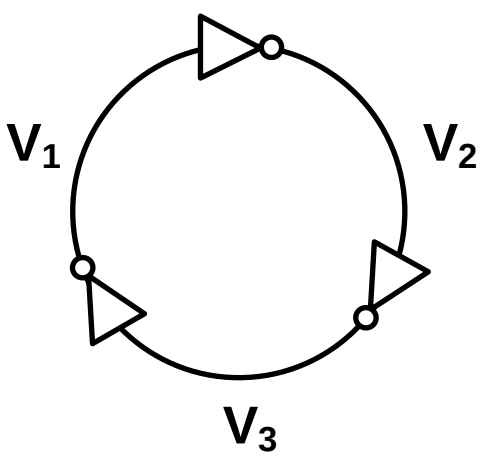

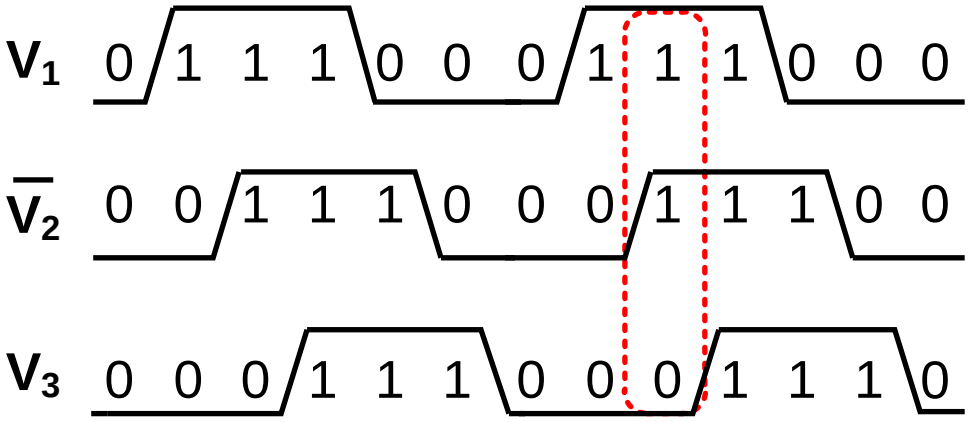

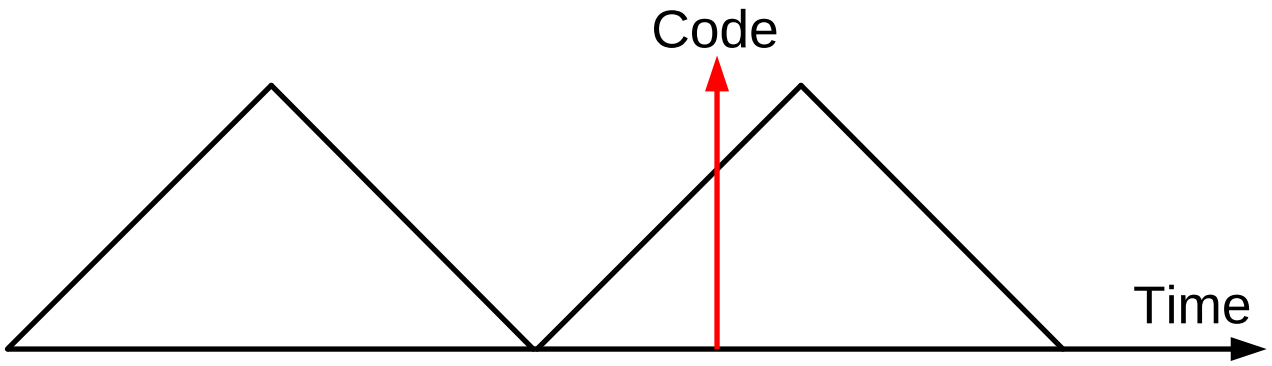

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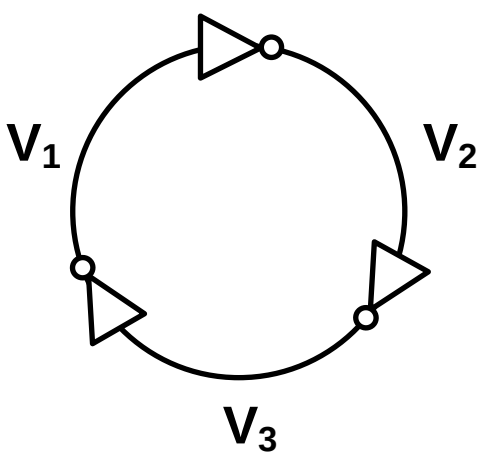

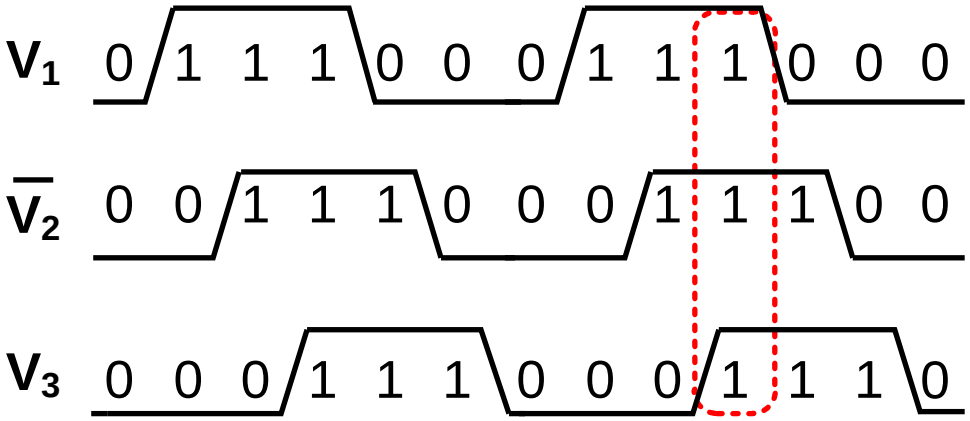

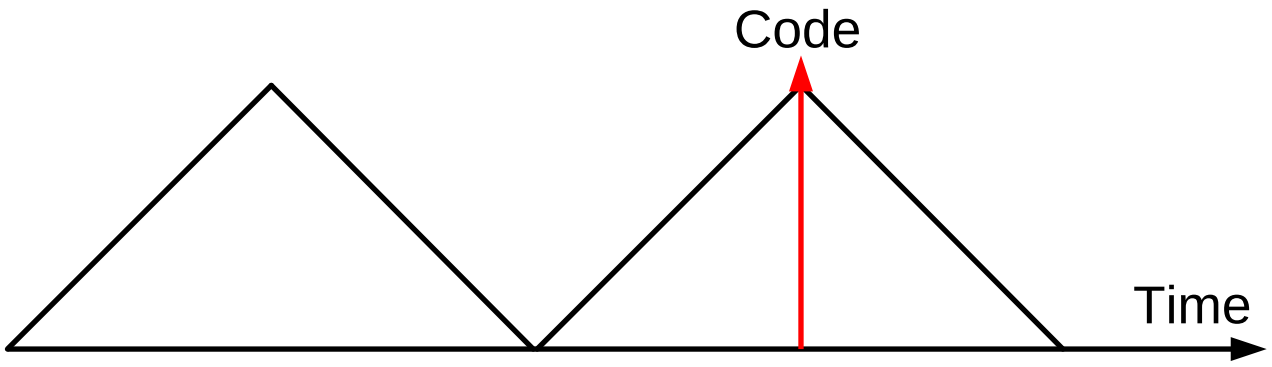

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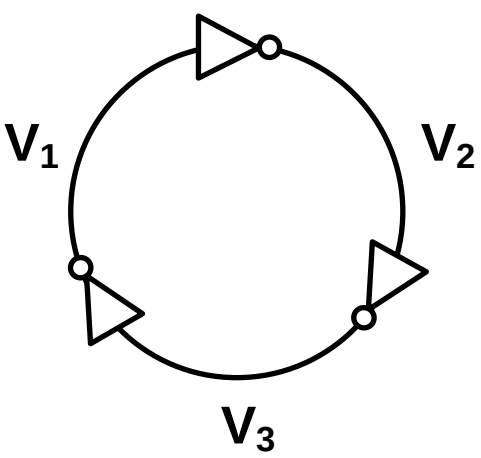

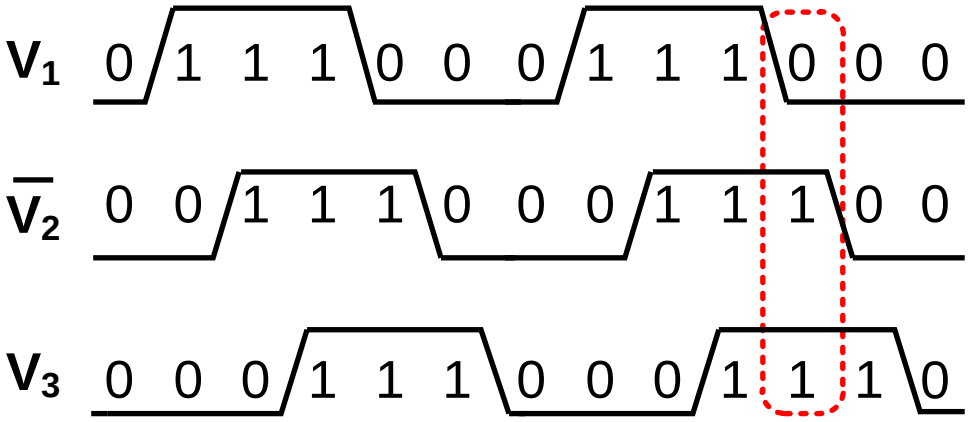

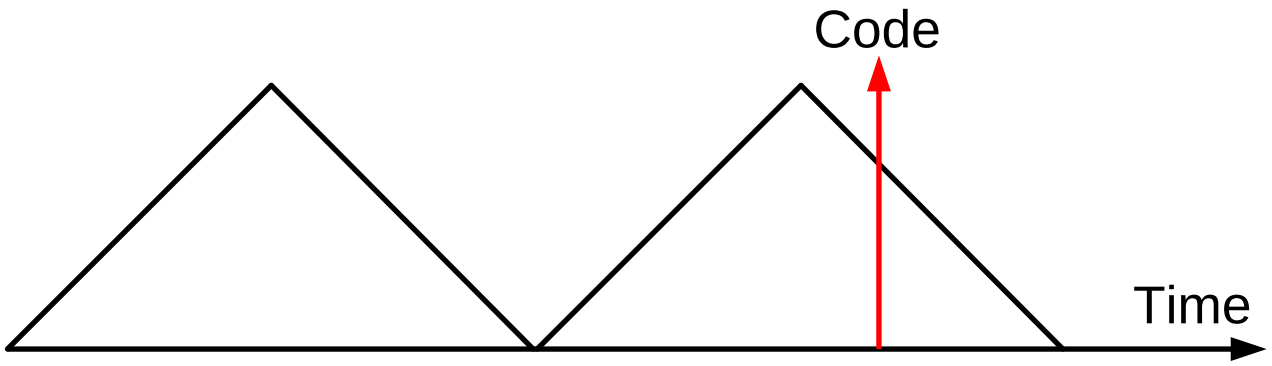

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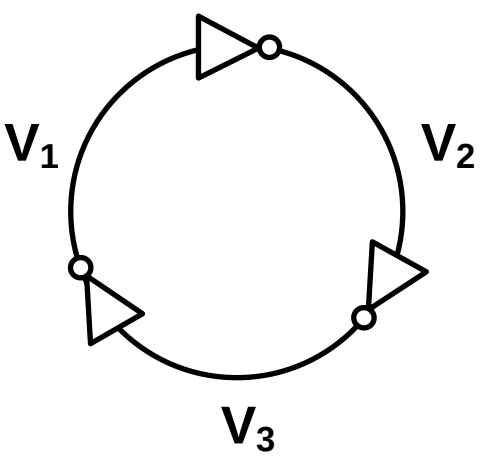

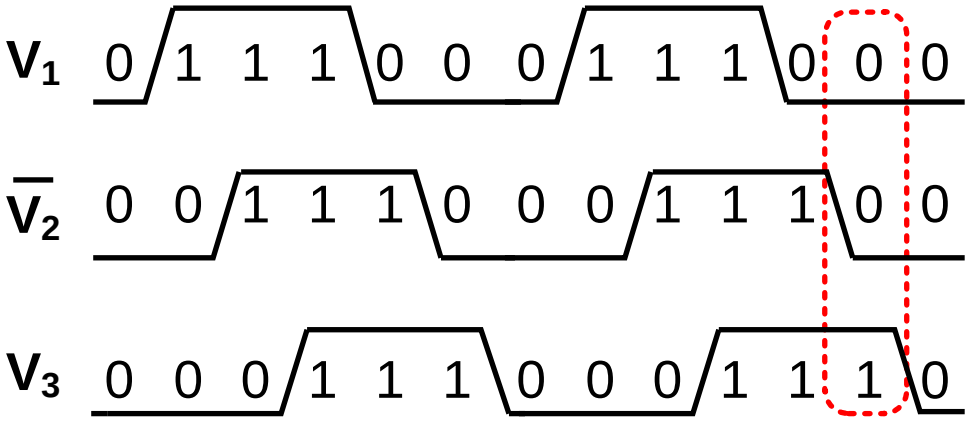

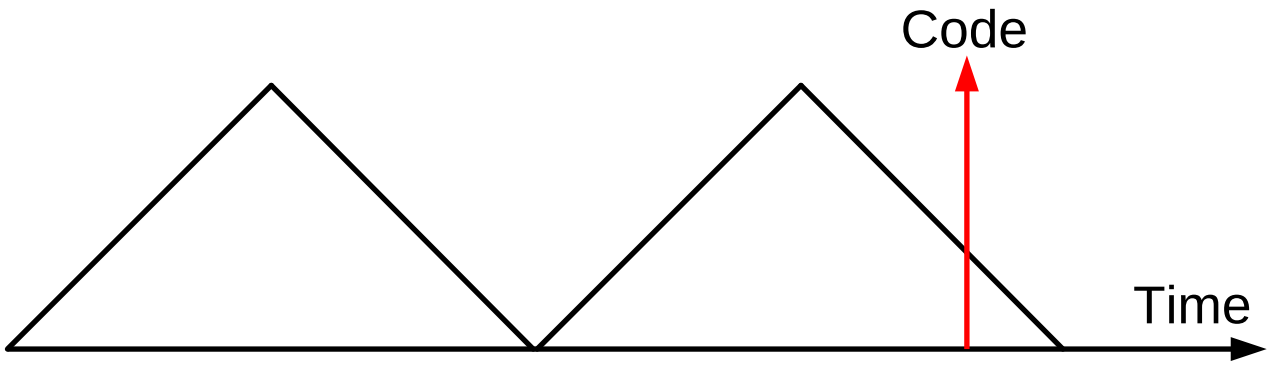

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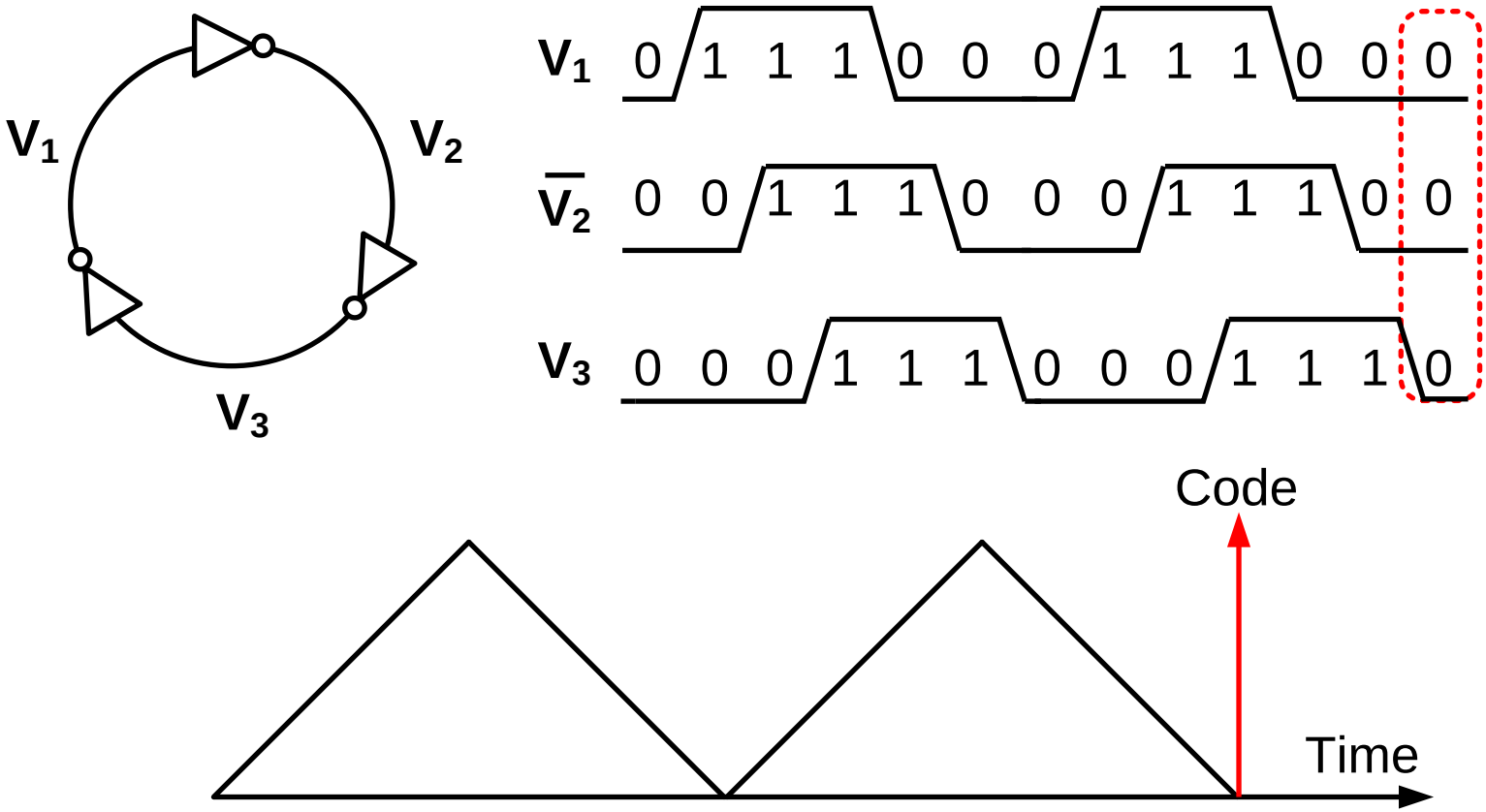

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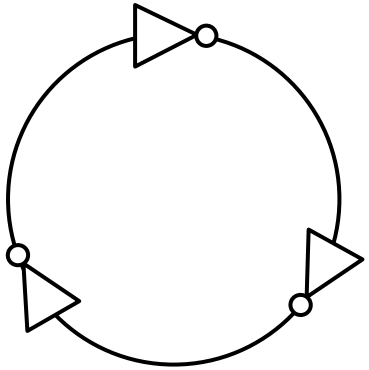
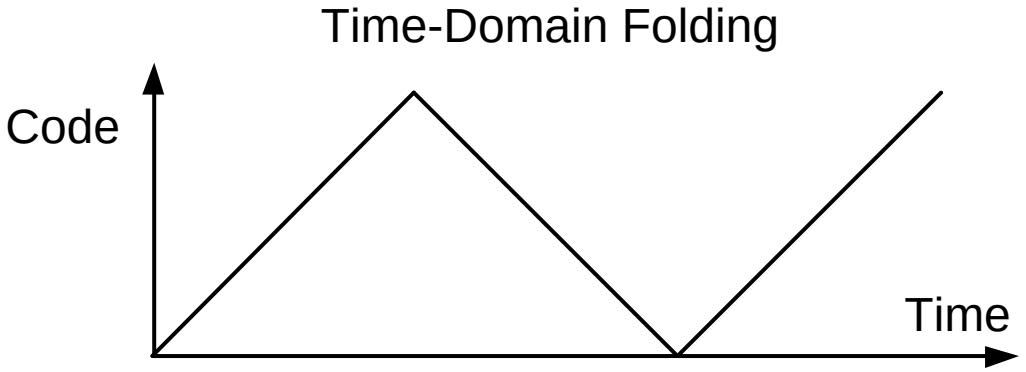
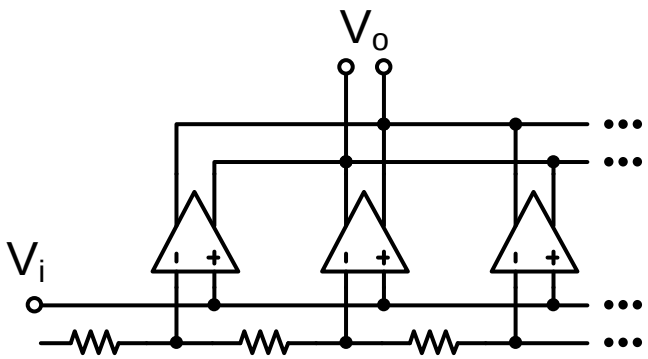
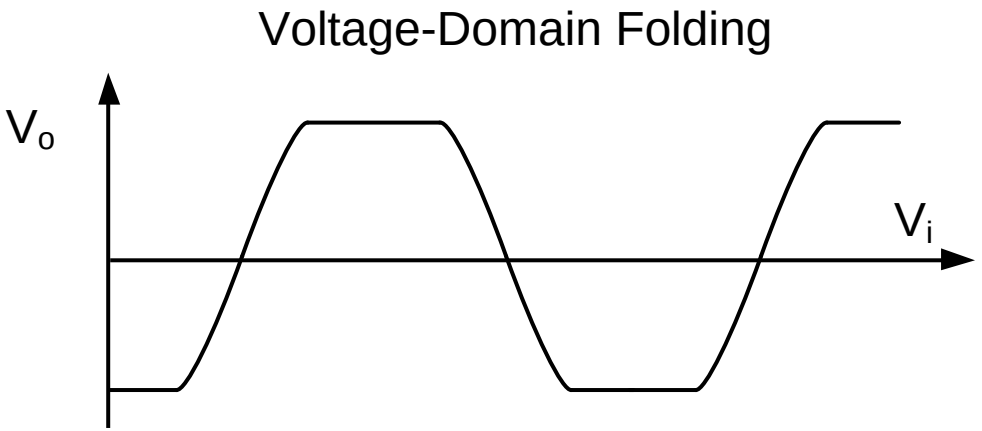
Time-Domain vs. Voltage-Domain Folding



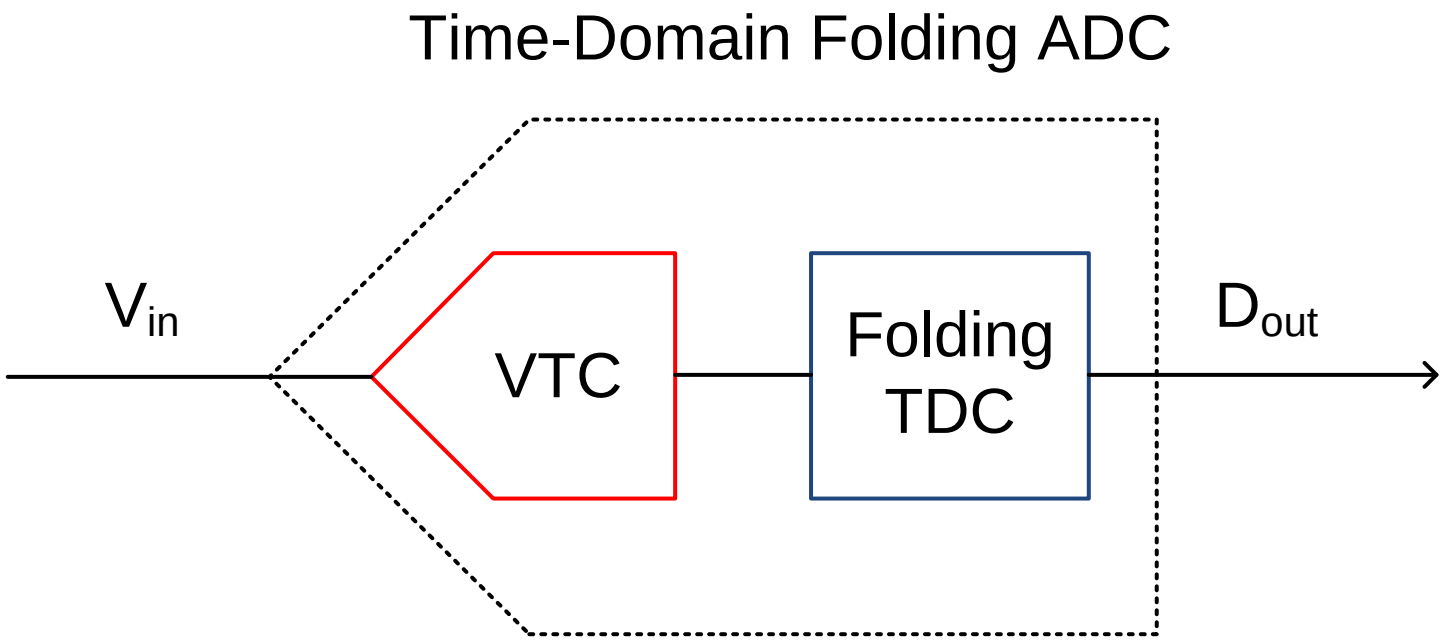






- Time-domain folding – linear, indefinite folding factor
- Voltage-domain folding – nonlinear, limited folding factor

Time-Domain Folding ADC



Targeting performance – 10 GS/s, 6 bits

Outline

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- **Time to Digital Converter**
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- Other Circuits
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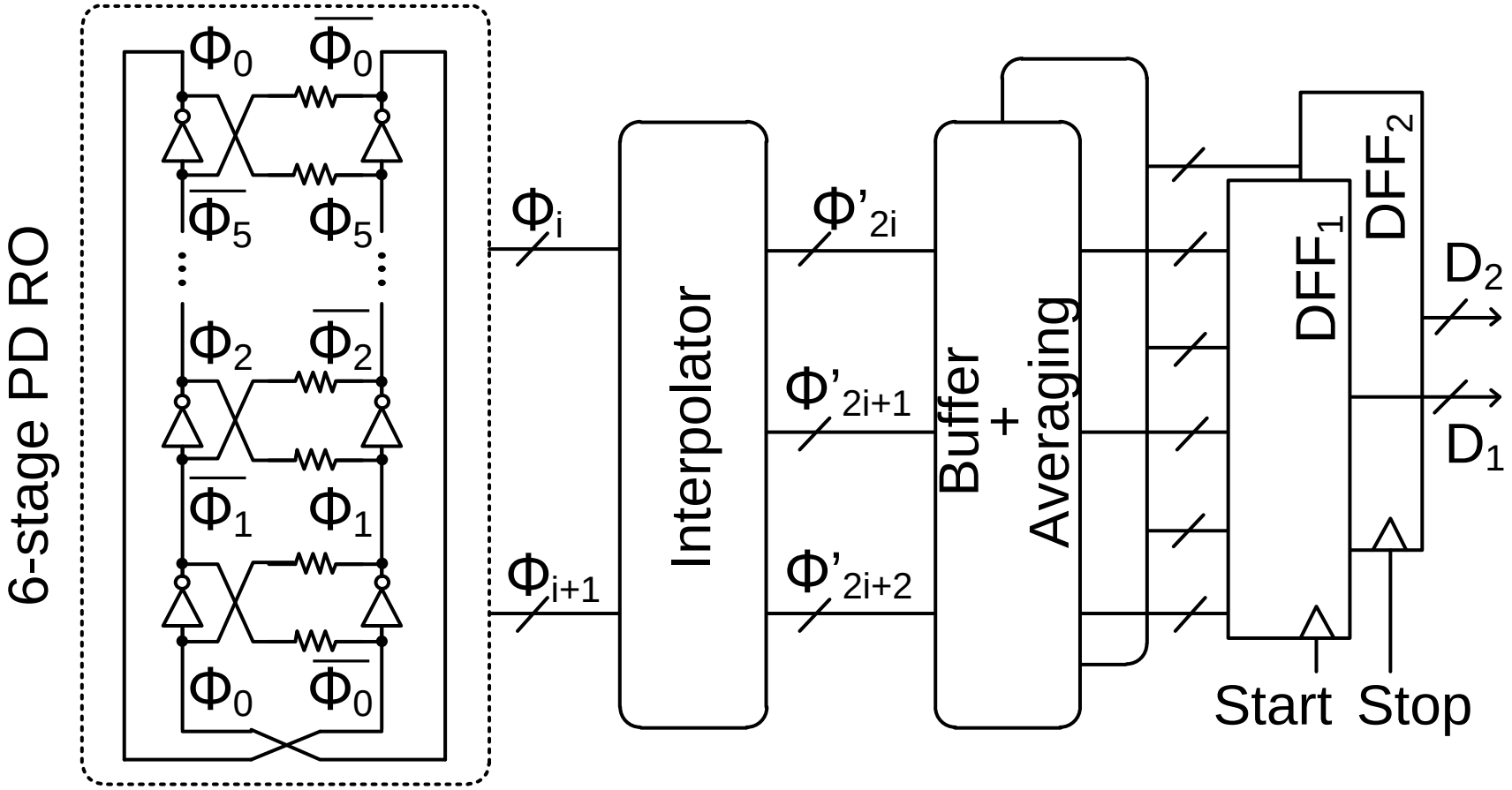
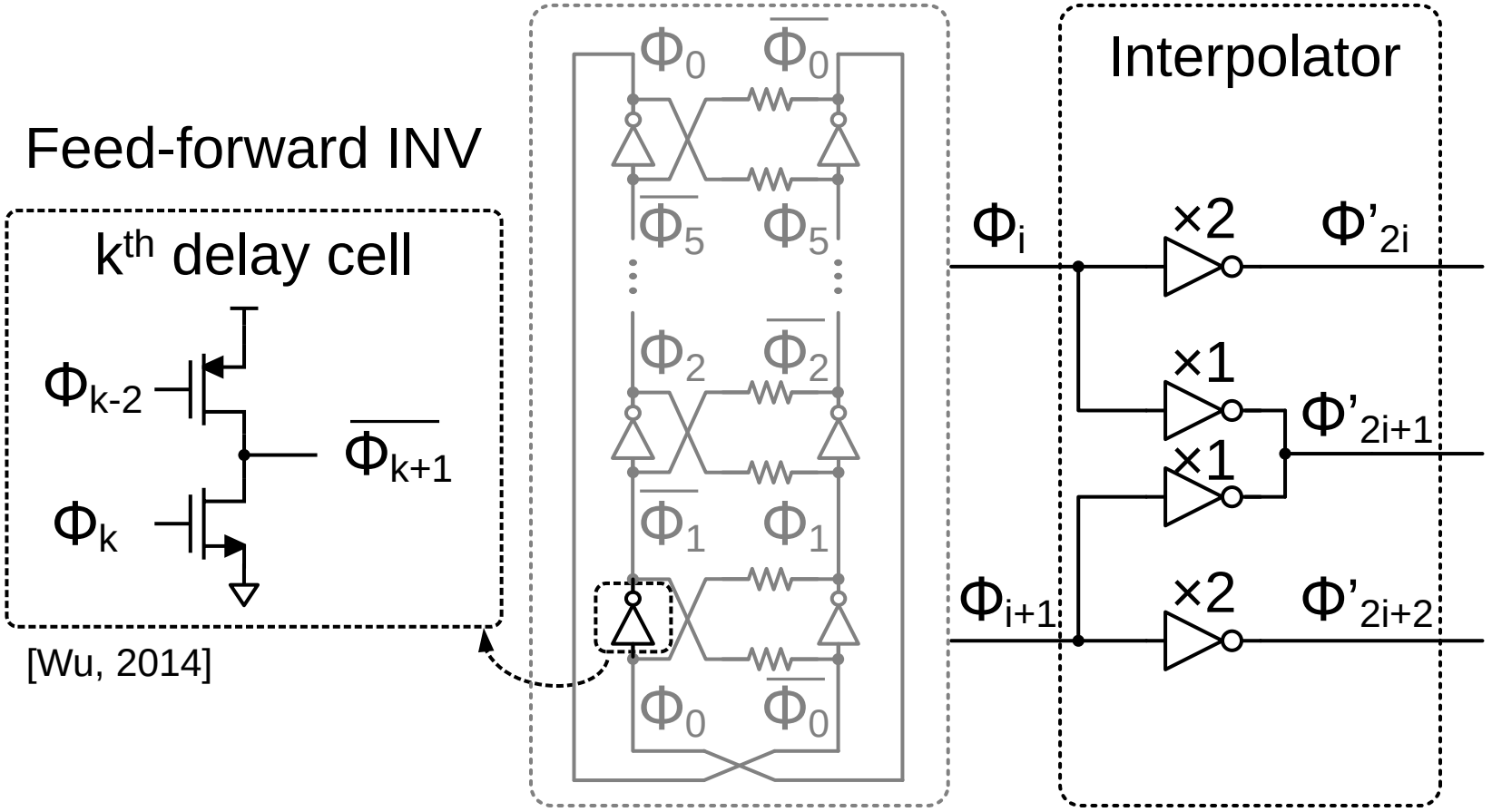
RO-Based TDC



6-stage pseudo-diff. RO
- common-mode rejection ↑
- delay uniformity ↑, DNL ↑

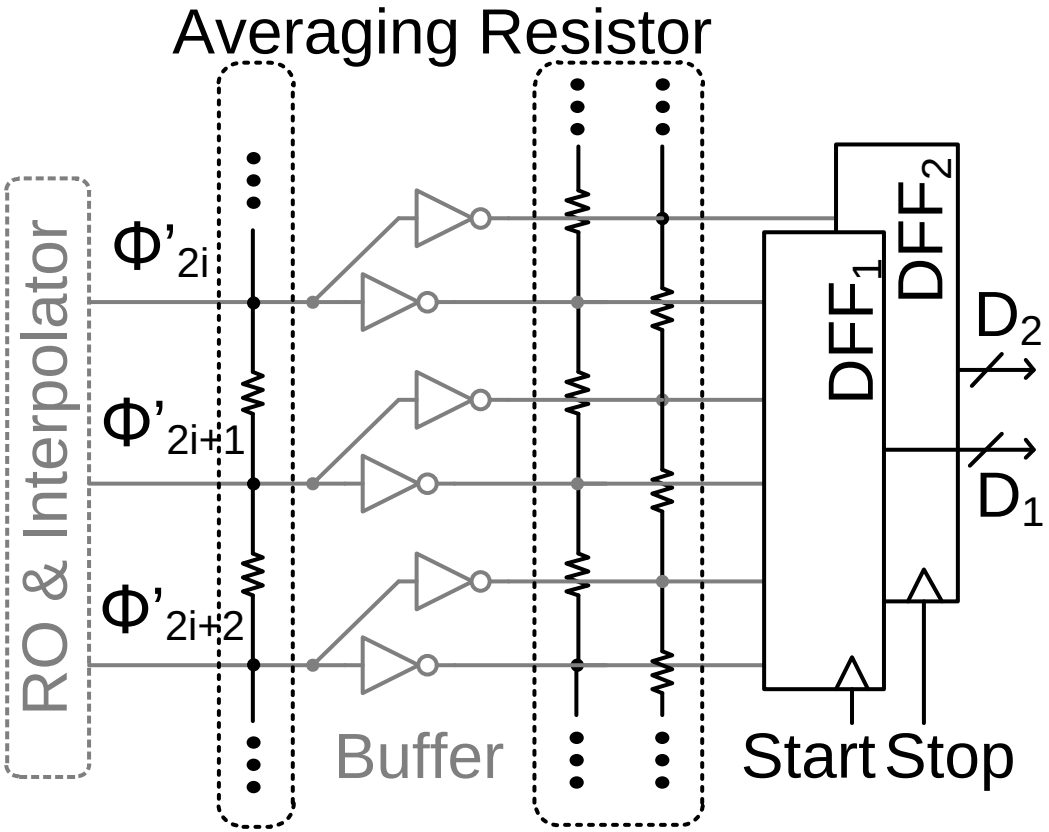
Speed-Up Techniques

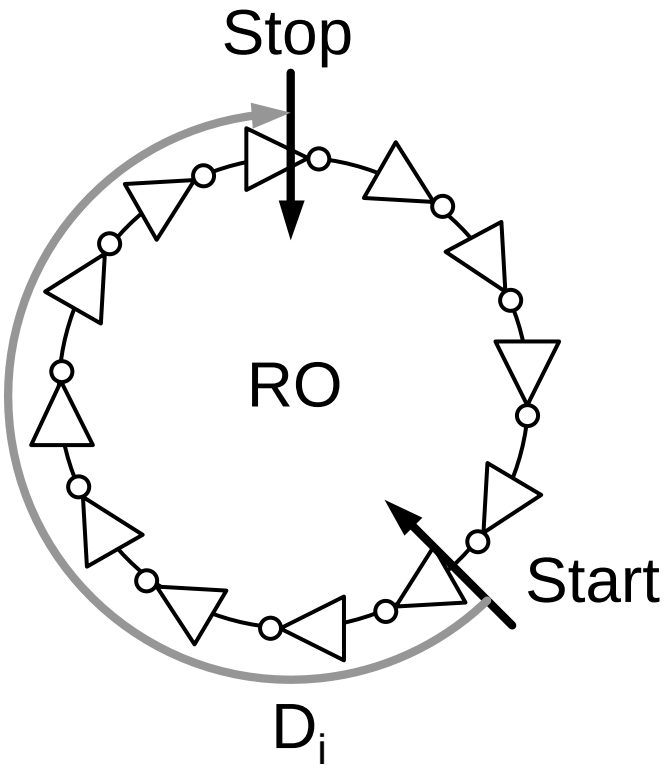


- Feed-forward
- 2× Interpolation

$$\text{LSB} = \frac{\text{inv.delay}(65\,\text{nm CMOS})}{4} = \frac{16\,\text{ps}}{4} = 4\,\text{ps}$$

Linearity Improvement Techniques





- Pseudo-diff. RO
- Resistor averaging
- Inherent DEM

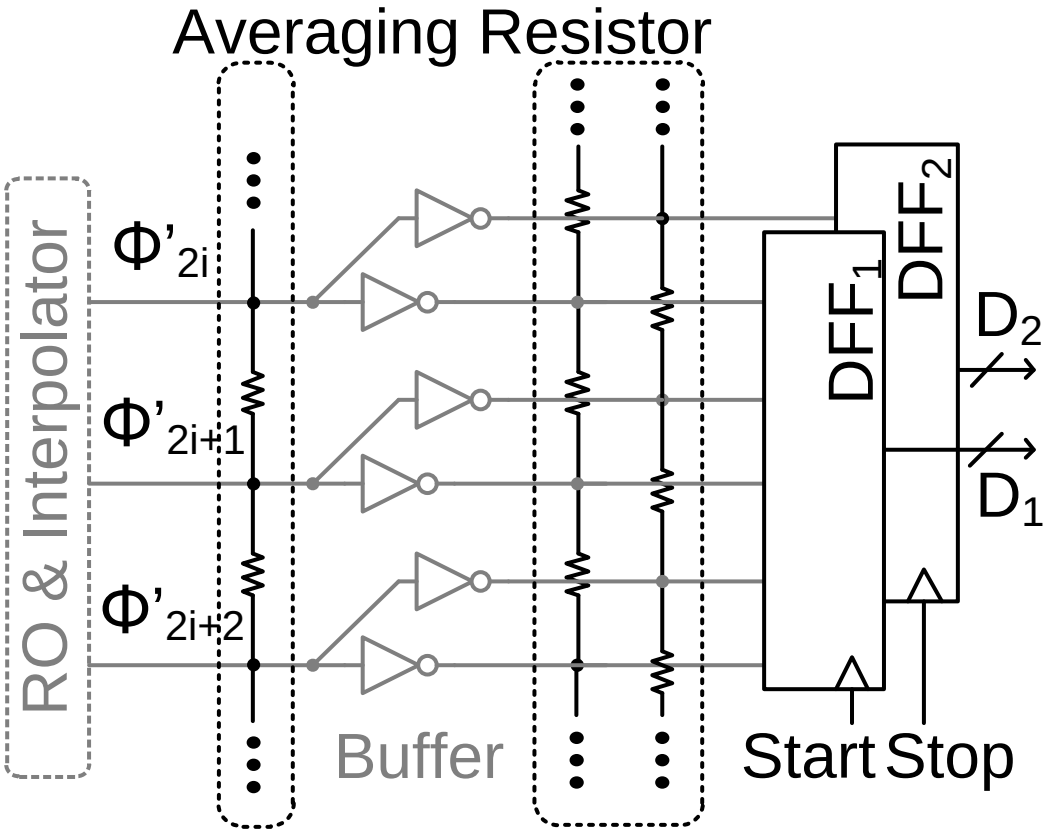
} linearity ↑

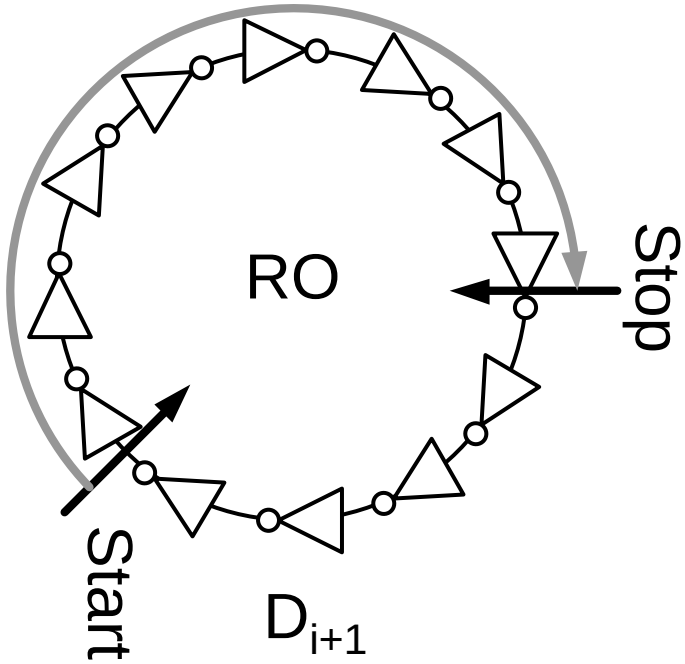
Double Sampling

√ inherent DEM

× 3 dB SNR penalty [Wu, 2014]

Linearity Improvement Techniques





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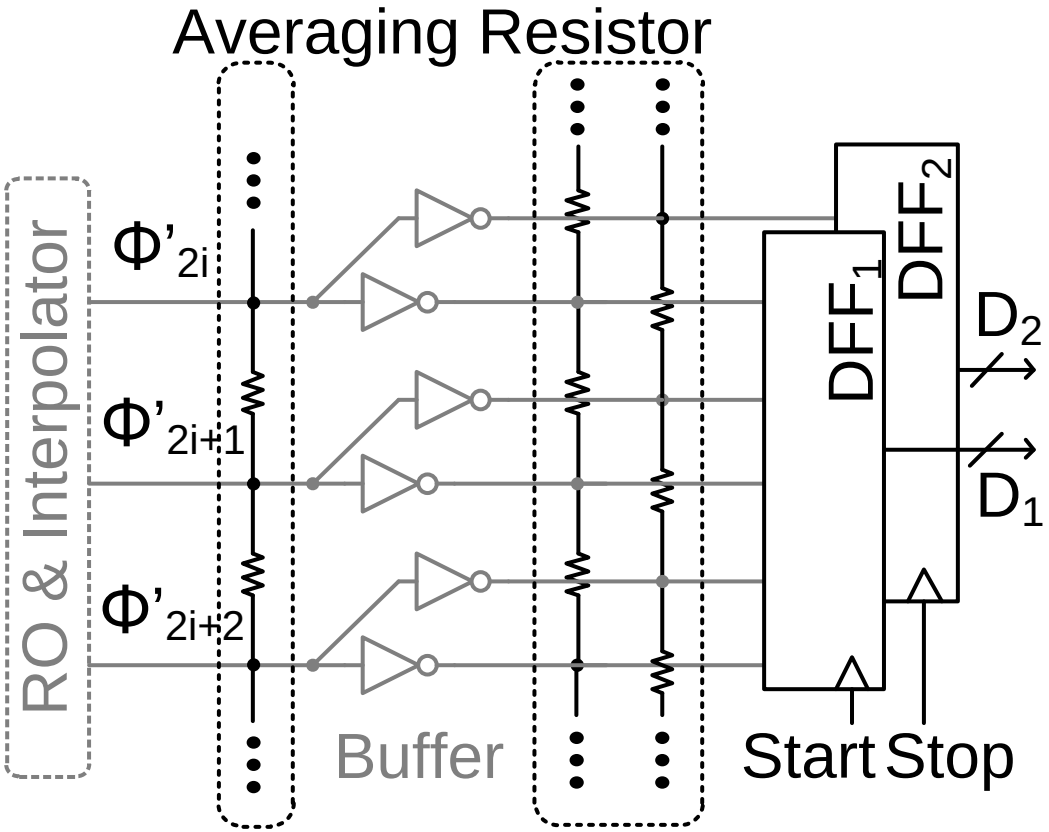

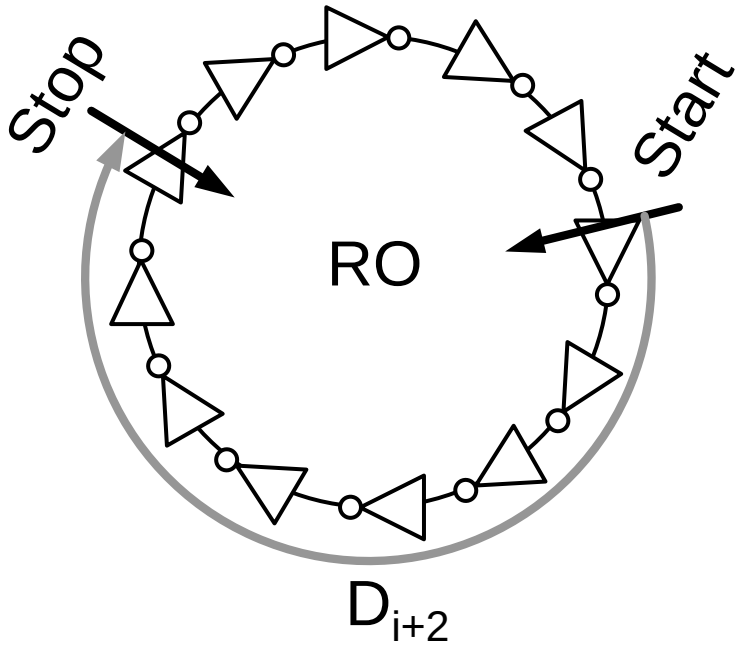

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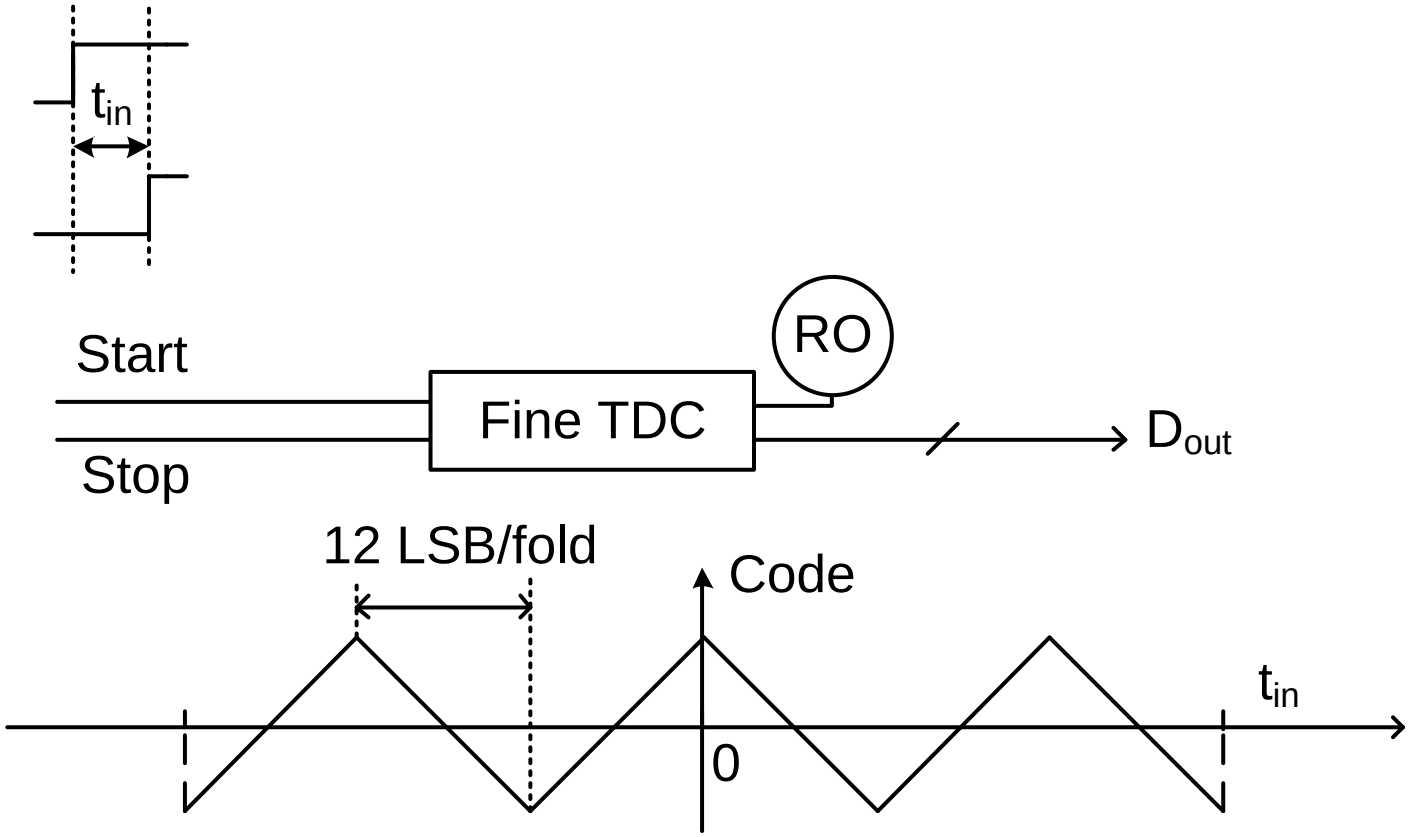
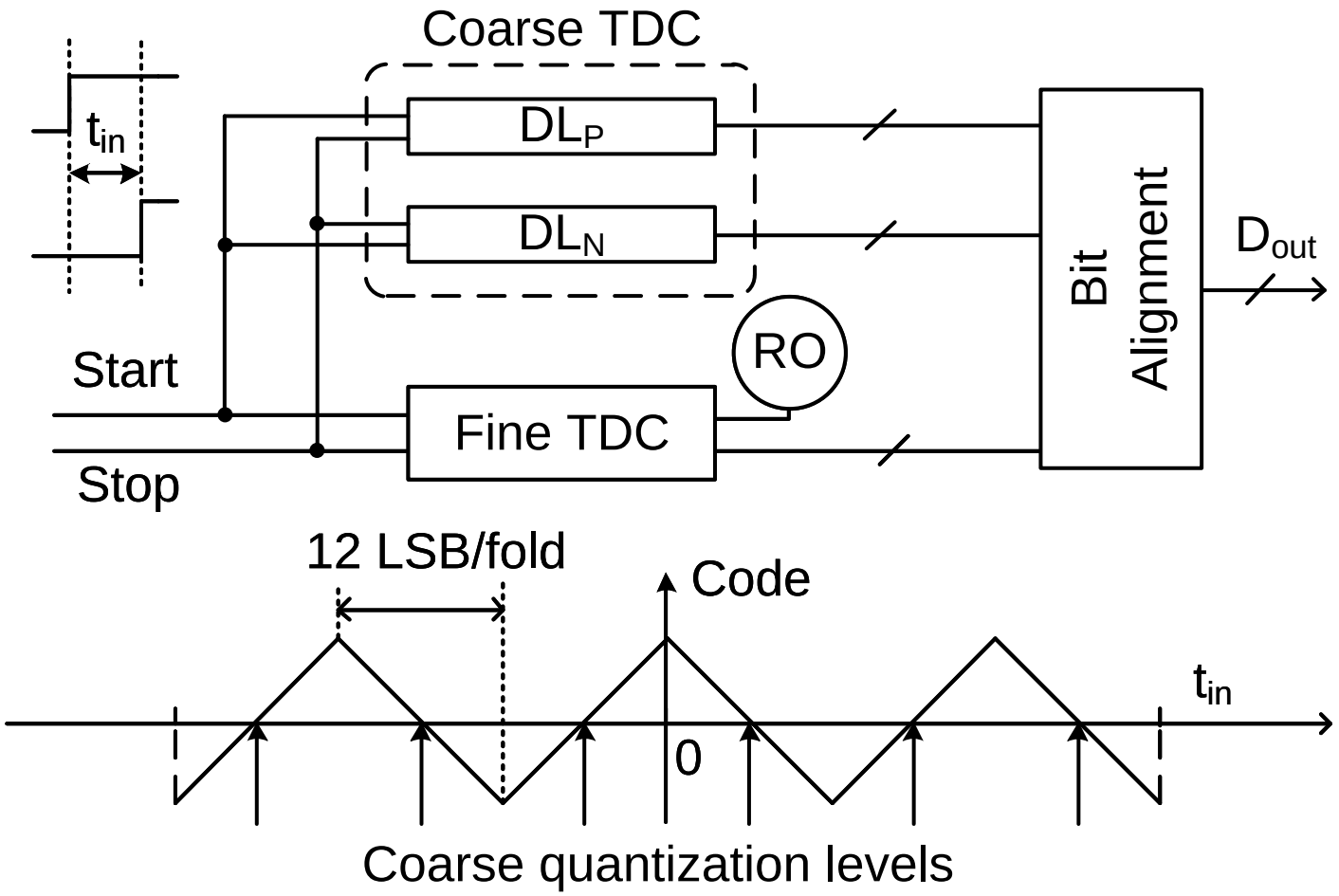
Overall TDC Diagram



- 12 LSB/fold x 6 folds = 72 levels → 6.2 bits
- Coarse TDC – folded differential DL [Stephan, 2010]

Overall TDC Diagram



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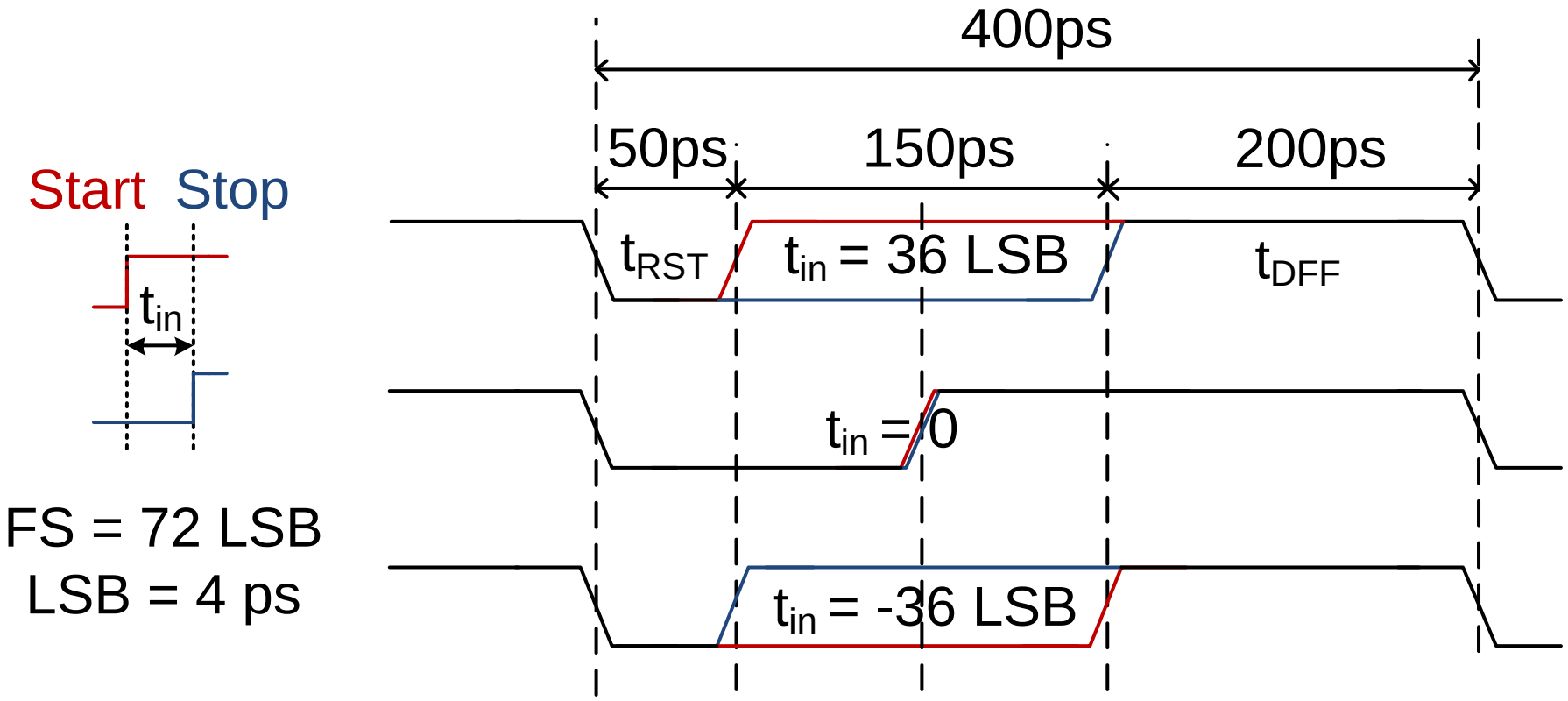
Simplified TDC Timing Diagram



- t_{in} span = $\pm$150ps ≈ $\pm$ 36 LSBs
- $T_{TDC} = t_{RST} + t_{in} + t_{DFF}$ = 400 ps → Max. speed is 2.5 GS/s

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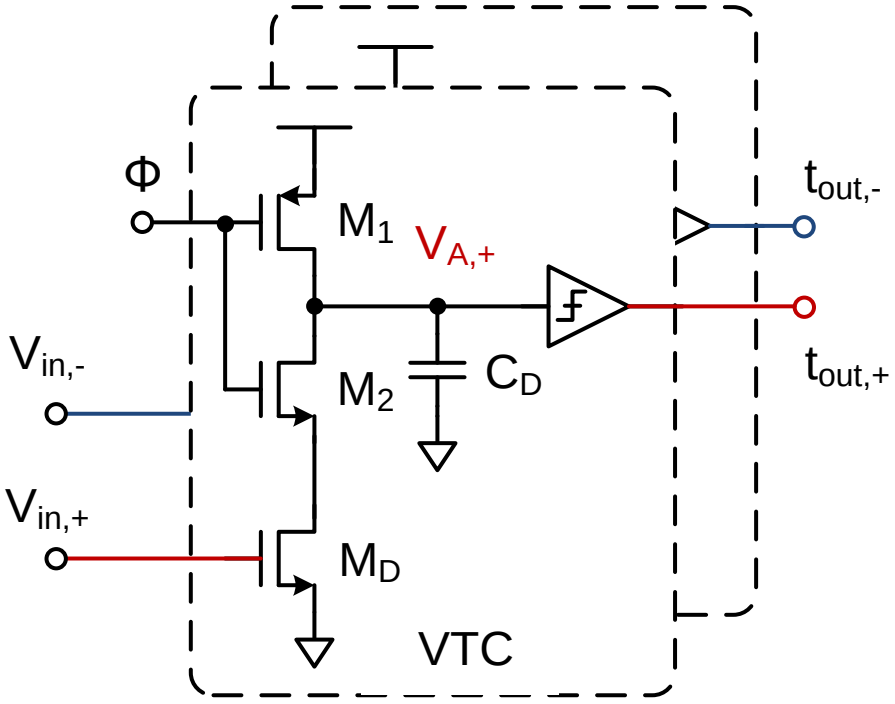
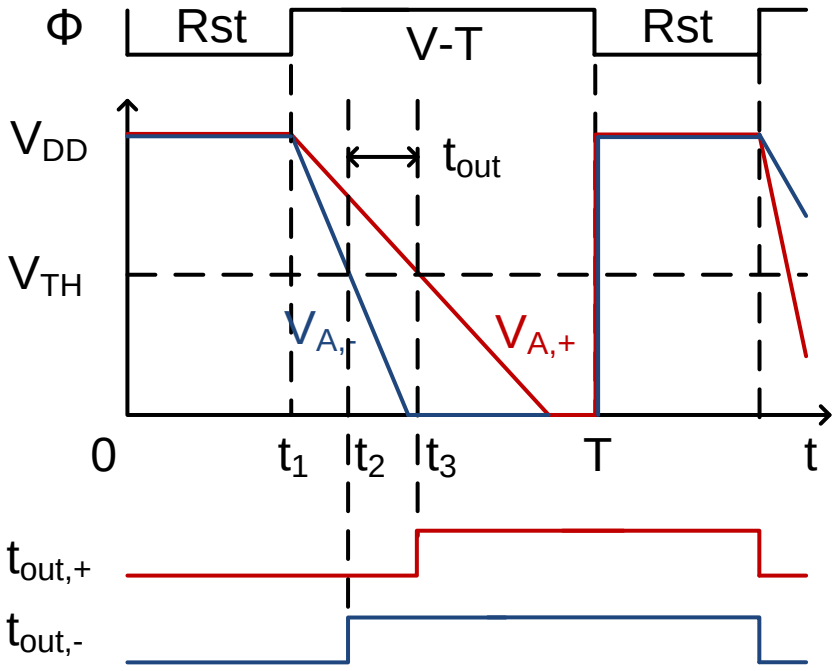
Current-Starved Inverter (CSI) Based VTC

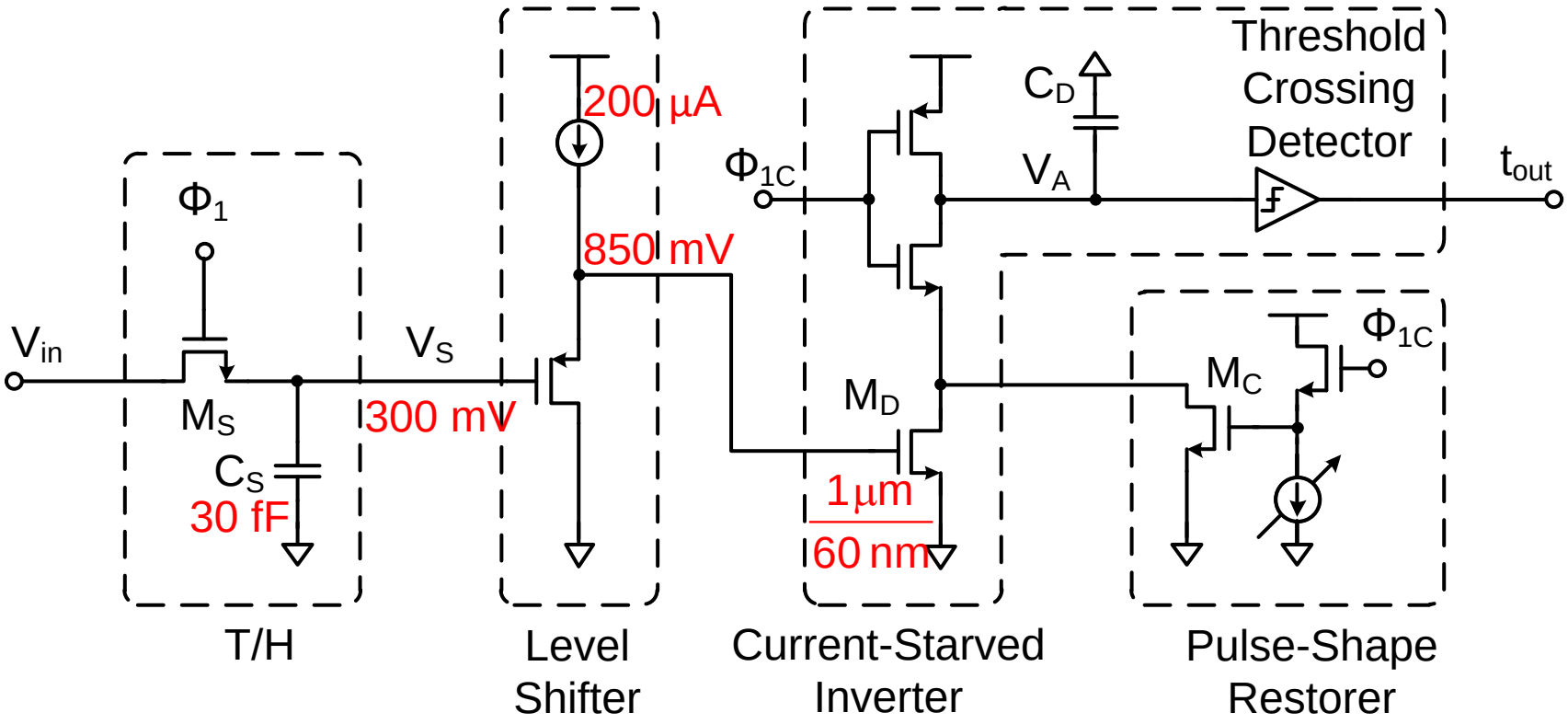


[Macpherson, 2013]



- The discharge current is controlled by V_{in}
- Pseudo-diff. structure improves linearity

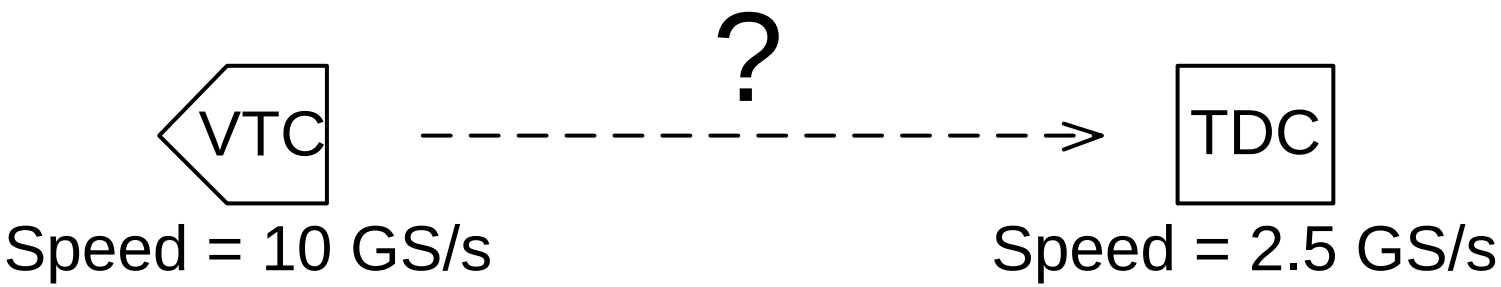
Overall VTC Schematic



Simulation shows:

- Speed =10 GS/s, linearity >= 6 bits
- Output range ~ ±20ps (T/2 = 50ps)

ADC (VTC + TDC) Architecture



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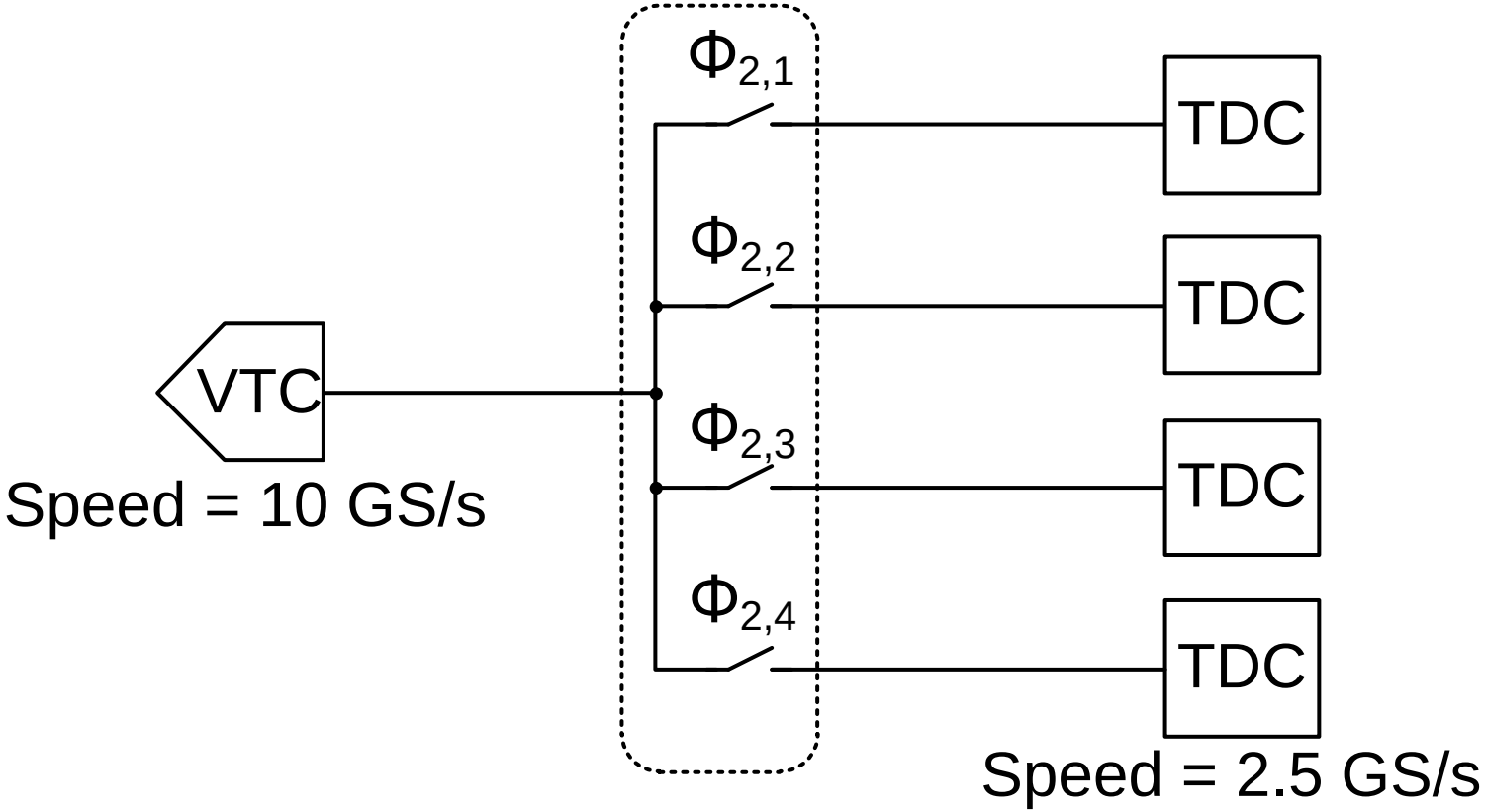

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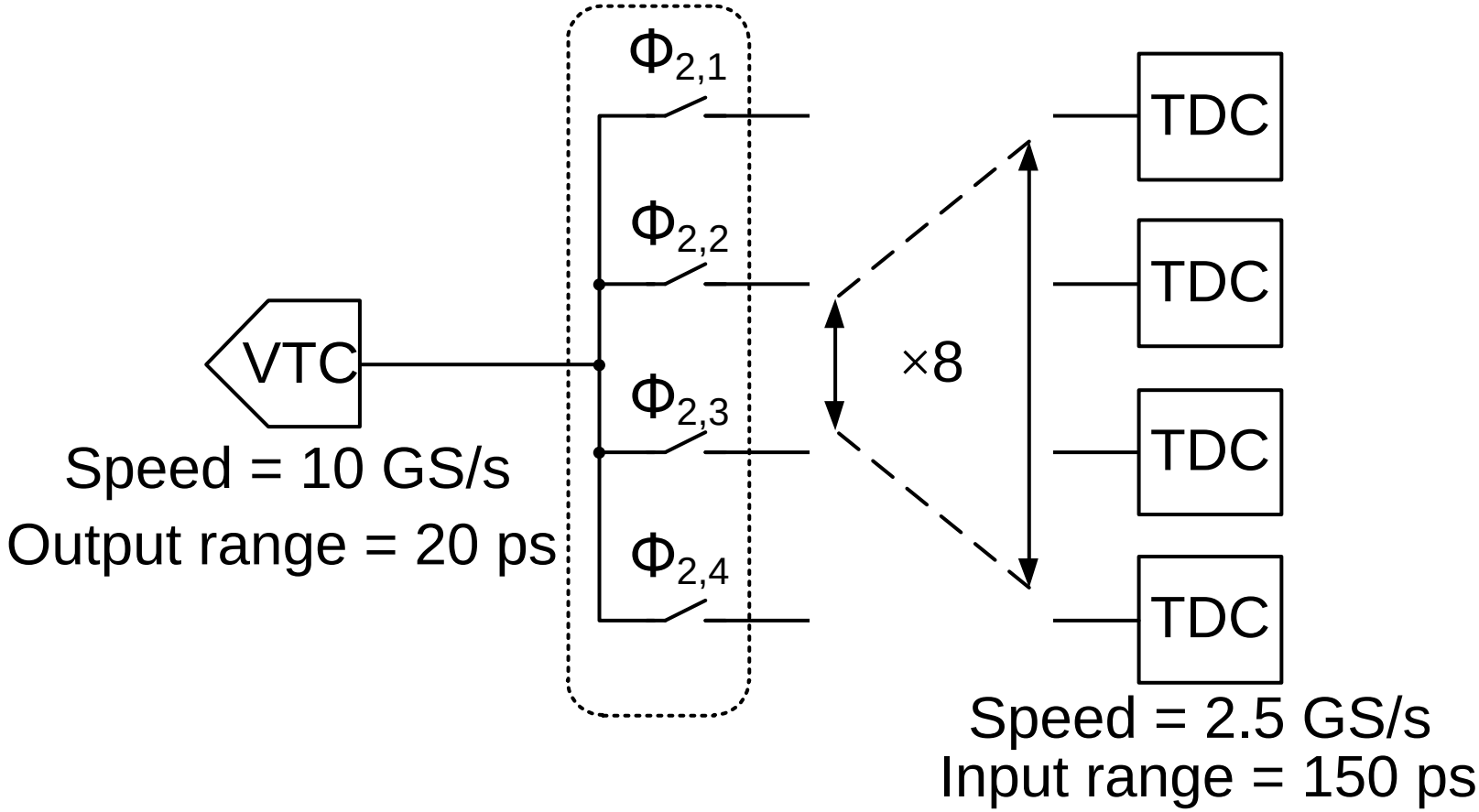

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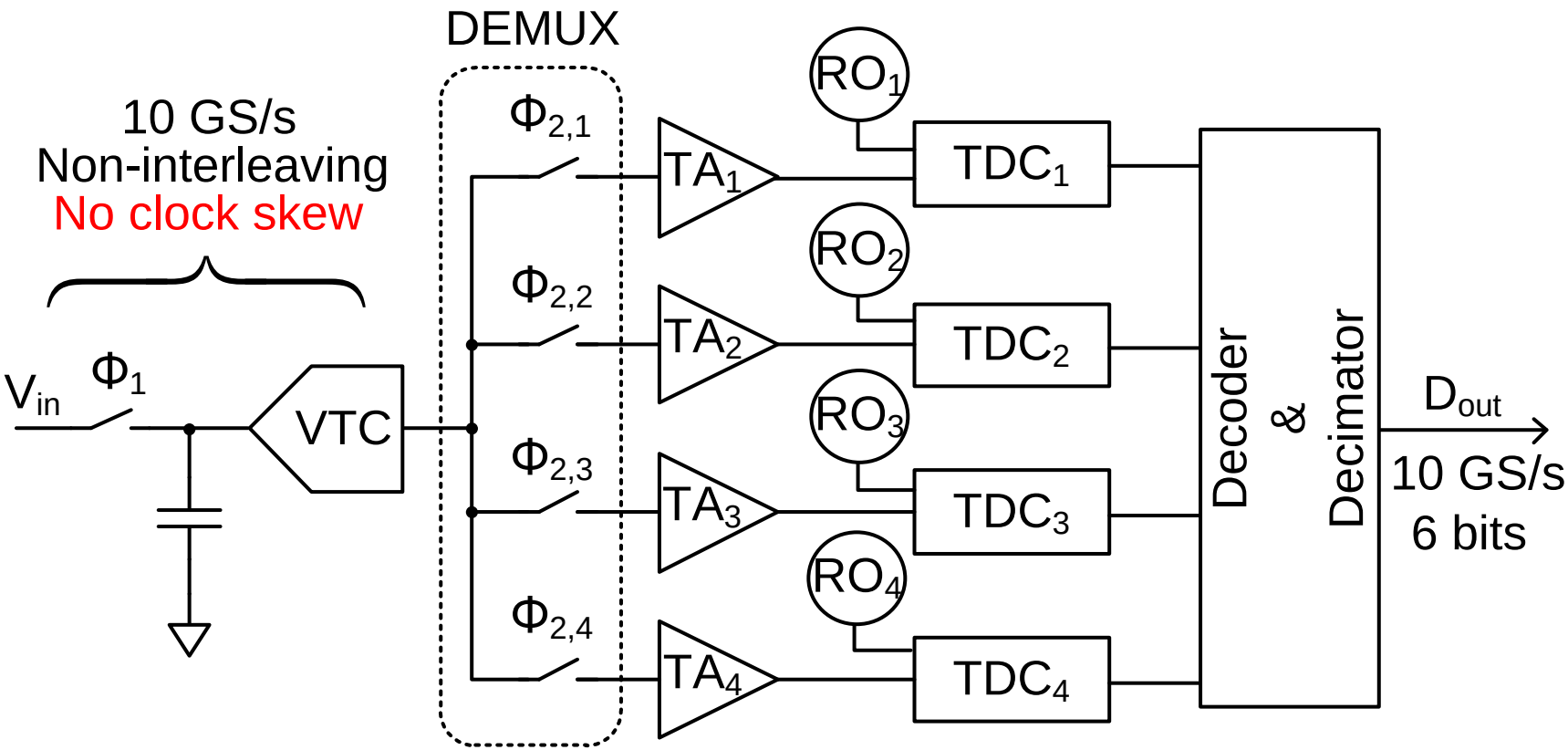

- Single VTC frontend at 10 GS/s
- 4 interleaved TDCs at 2.5 GS/s

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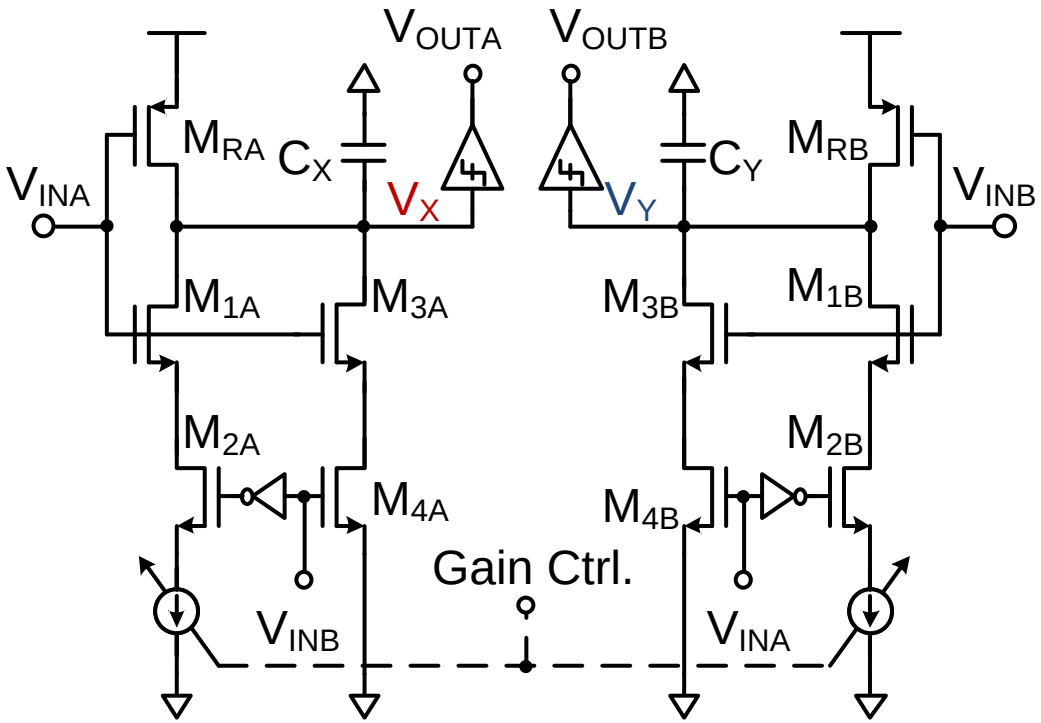
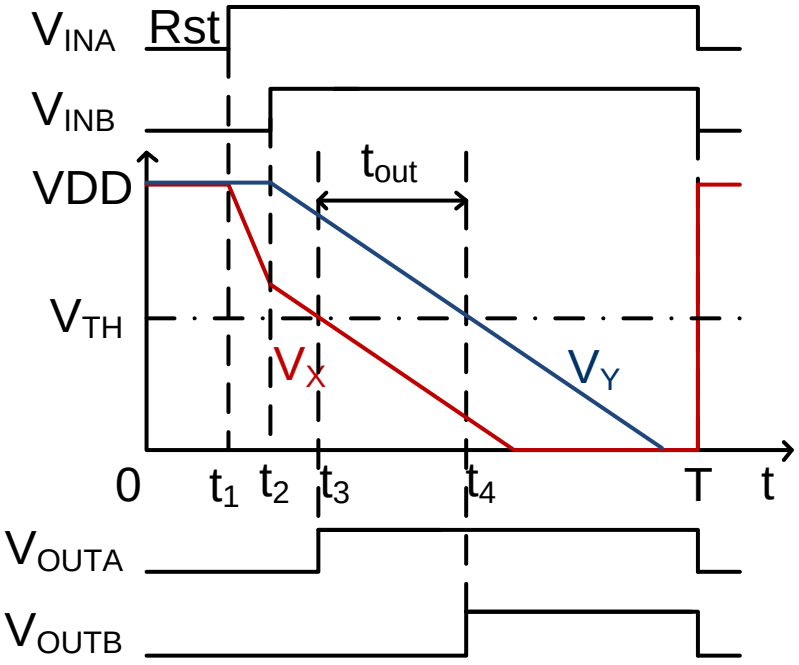
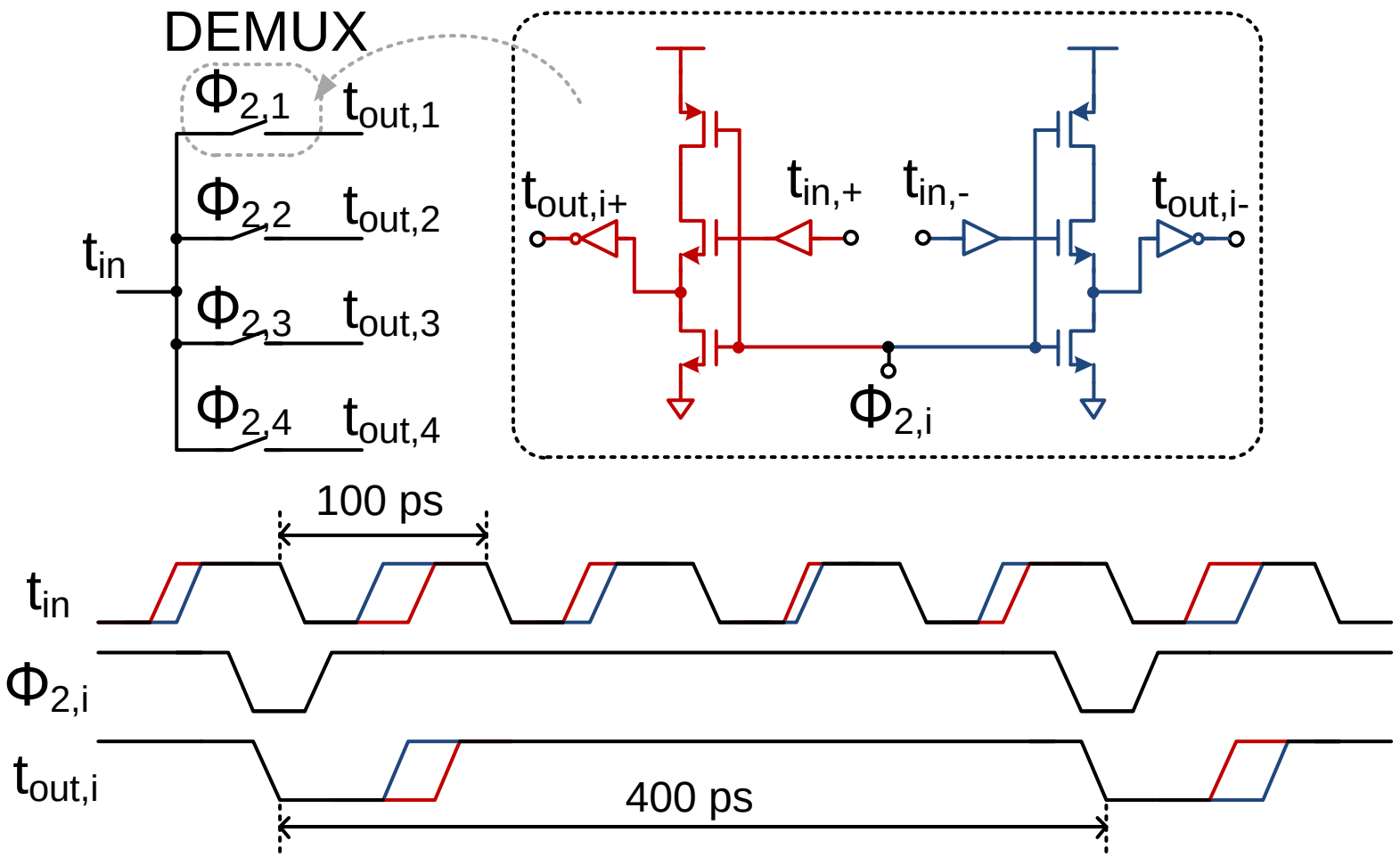
Time Amplifier





- Double-rate discharging TA [Hye-Jung, 2011]
- Gain = slope ratio between discharging steps
- Gain calibrated with 4-bit DAC

DEMUX

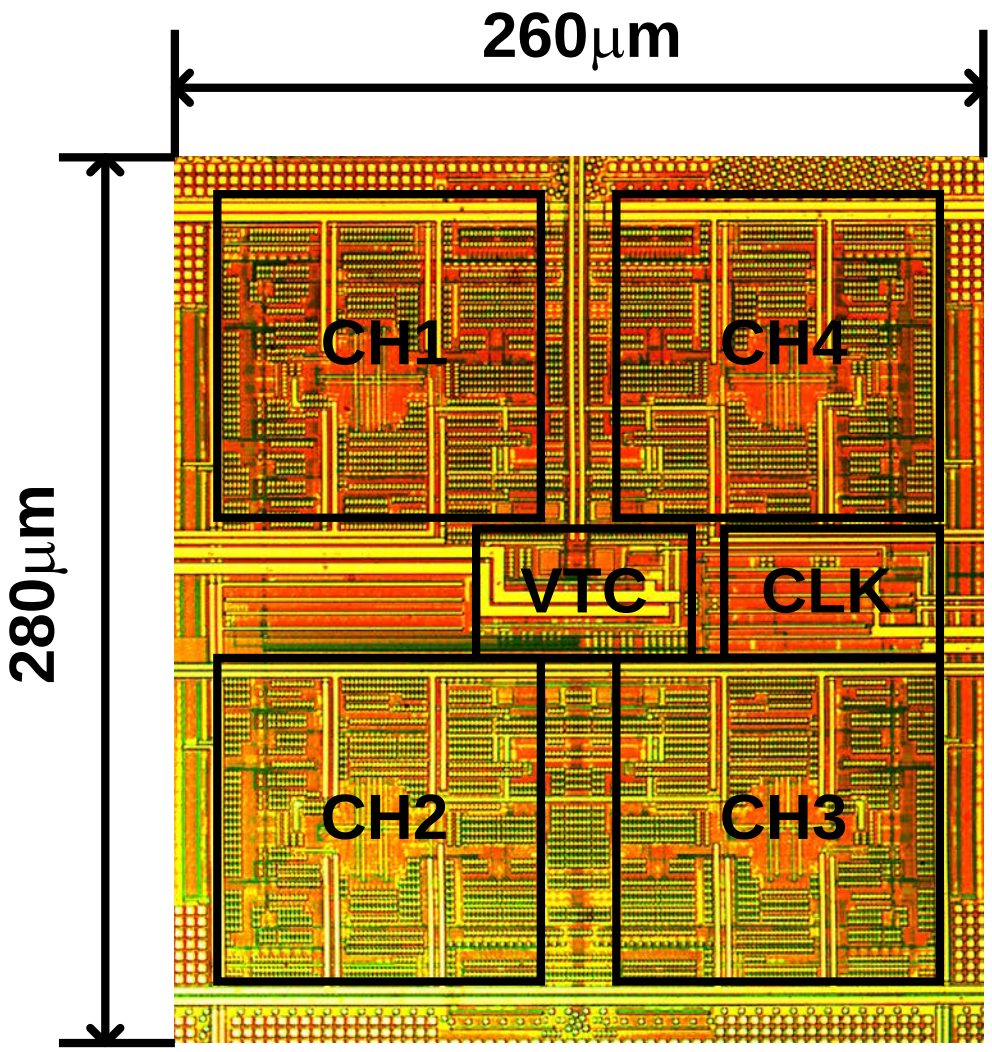


- Dyn. INV based DEMUX only passes rising edges

Outline

- Motivation for Time Domain
- Time to Digital Converter
- Voltage to Time Converter
- Other Circuits
- **Measurement Results**
- Conclusion

Die Photo

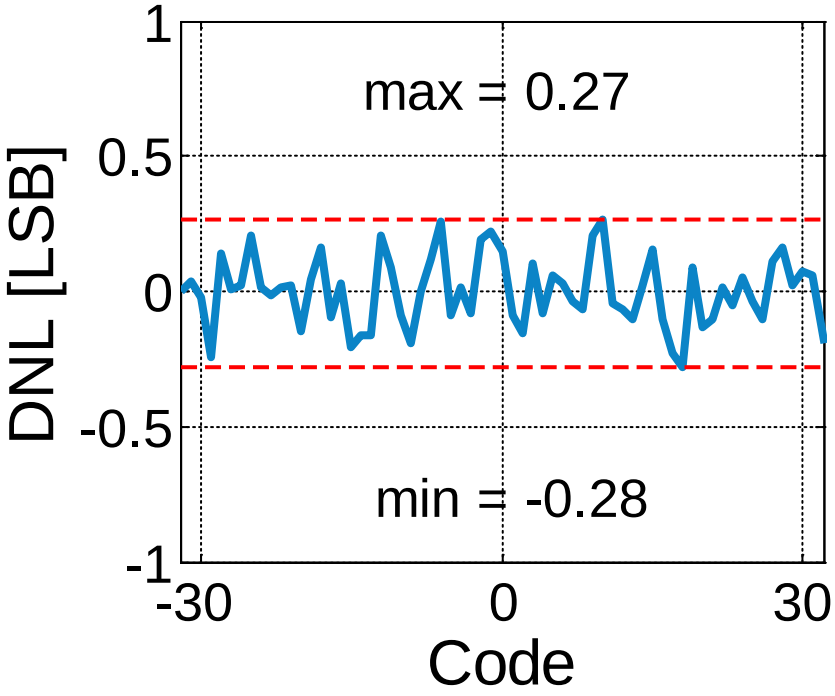


65nm LPE CMOS

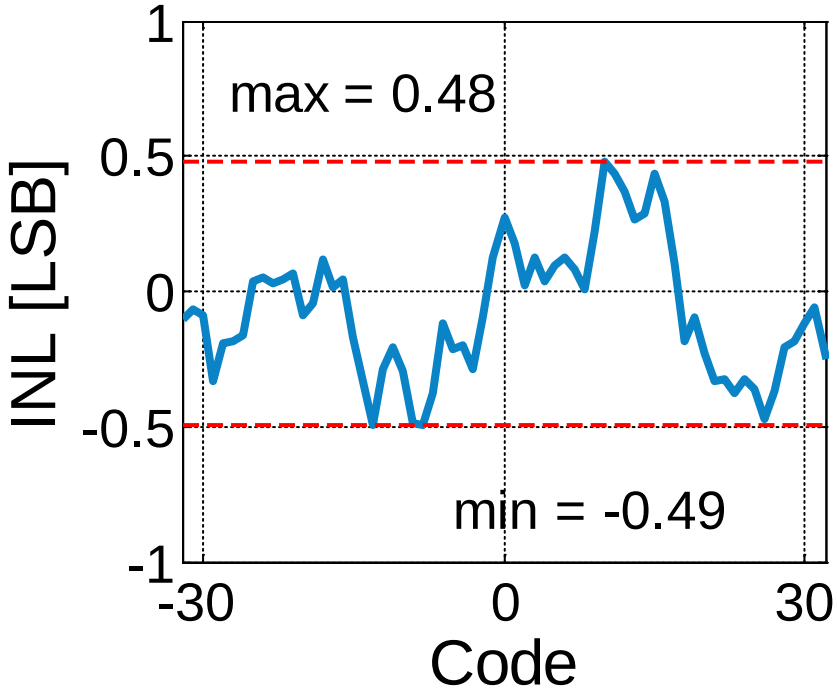
Area = 0.073 mm^2

Measured DNL and INL

DNL < 0.3 LSB

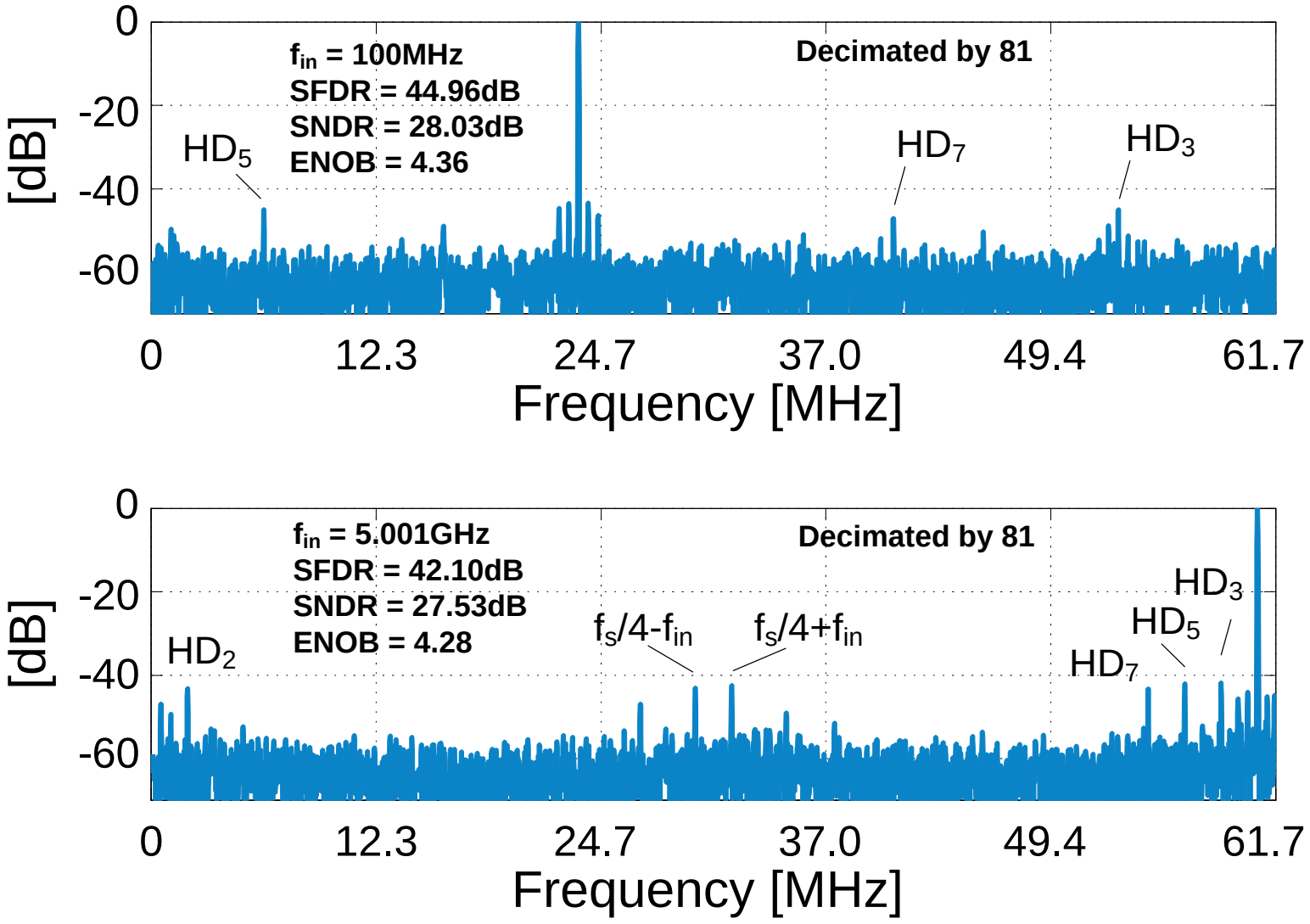


INL < 0.5 LSB

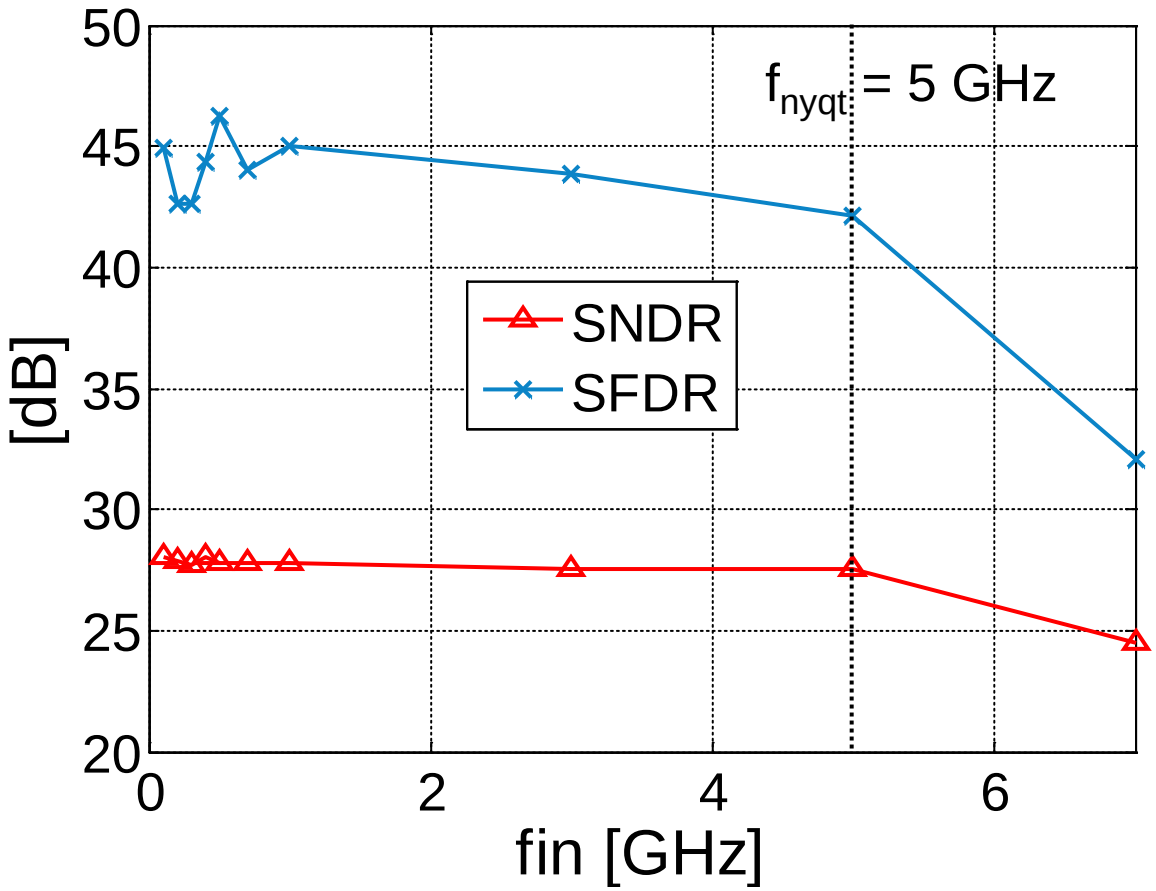


Test Conditions: VDD = 1.3 V, f_s = 10 GS/s

Measured Output Spectra

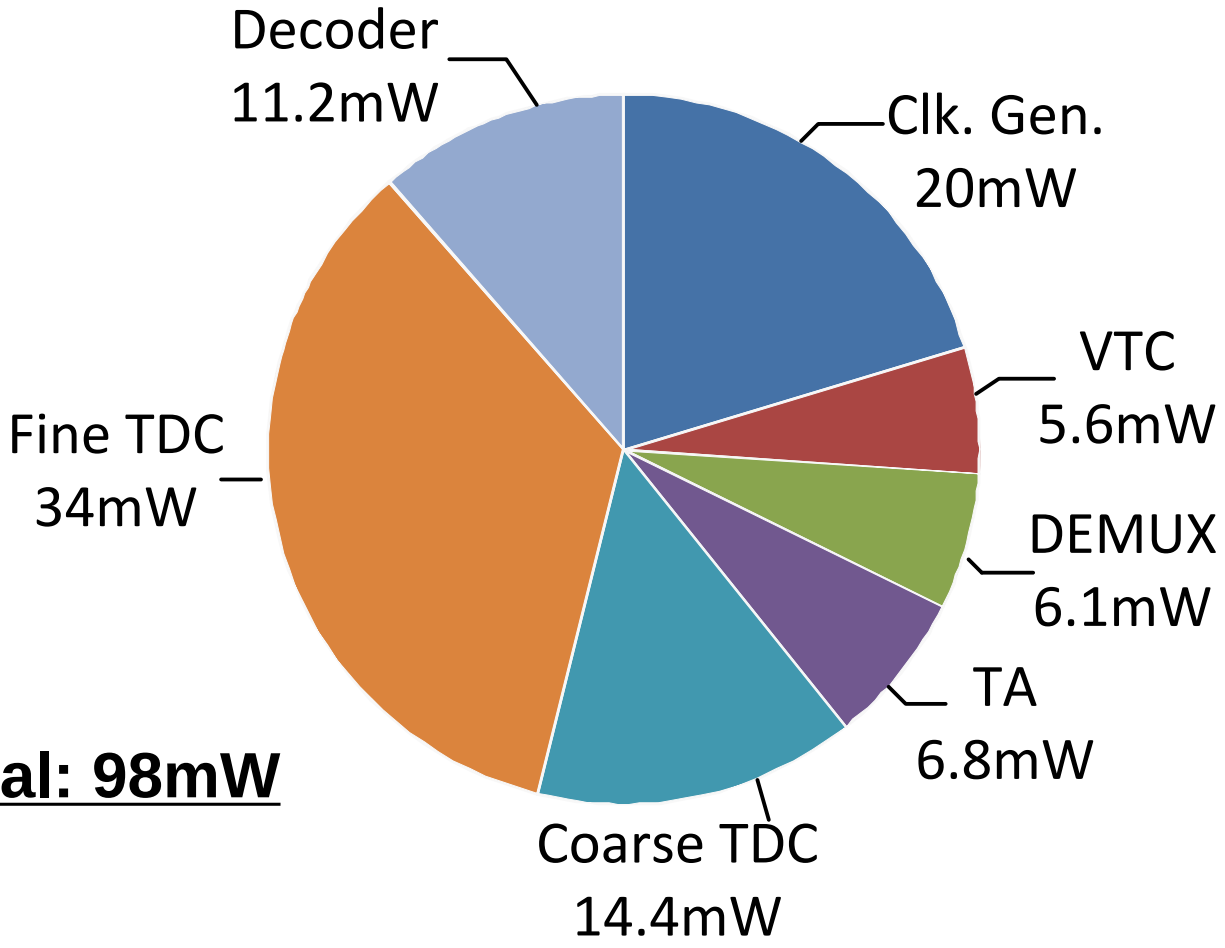


Measured Dynamic Performance



Test Conditions: VDD = 1.3 V, f_s = 10 GS/s

ADC Power Breakdown



Total: 98mW

Test Conditions: VDD = 1.3 V, f_s = 10 GS/s

Performance Comparison

	This work	CICC' 13 [4]	VLSI' 13 [1]	ISSCC' 13 [3]	ISSCC' 14 [3]
Architecture	**Time Domain**	Time Domain	TI SAR	TI Flash	TI Flash
Tech. (nm)	**65**	65	65	40	32 SOI
f_s (GS/s)	**10**	5	10	10.3	20
ENOB@Nyq. (bits)	**4.3**	2.8	4.0	5.1	4.8
SNDR@Nyq. (dB)	**27.2**	18.4	26.0	33	30.7
SFDR@Nyq. (dB)	**42.1**	22.3	36	NA	39.4
DNL (LSBs)	**0.28**	0.91	0.19	NA	0.47
INL (LSBs)	**0.49**	0.95	0.65	NA	0.42
Power (mW)	**98**	35	79.1	240	69.5
Area (mm^2)	**0.073**	0.08	0.52	0.27	0.25
FoM (fJ/step)	**504**	1000	480	700	124

Outline

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Conclusion

- A time-domain 10-GS/s, 6-bit folding flash ADC with high area efficiency is presented.
- The single VTC front-end requires no clock-skew calibration at 10 GS/s in 65-nm CMOS.
- The RO-based folding TDC achieves high area efficiency and high speed (2.5 GS/s) simultaneously.
- The inherent DEM of the RO-based TDC achieves excellent conversion linearity.

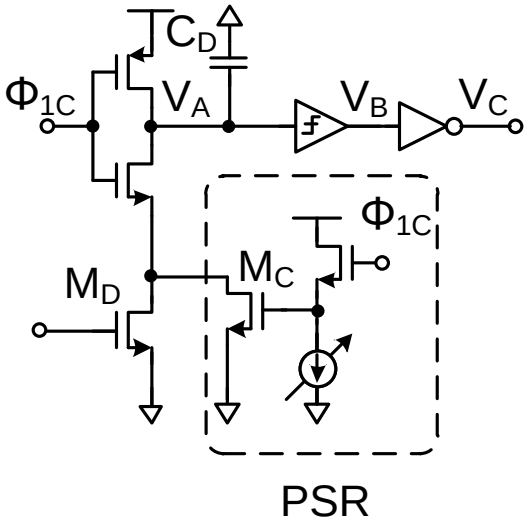
Acknowledgement

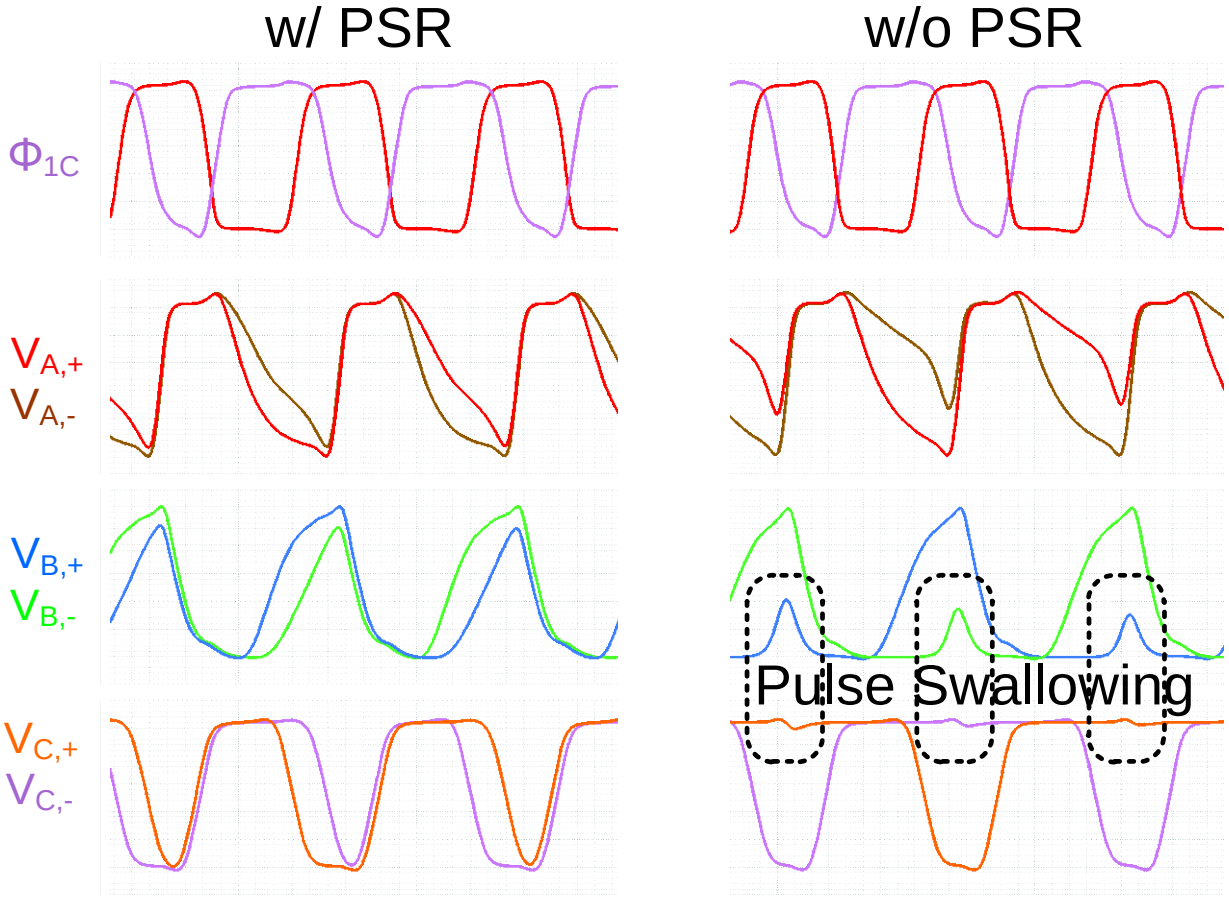
We thank SRC for the TxACE silicon fabrication program and Analog FastSPICE (AFS) Platform from Mentor Graphics.

Thank you!

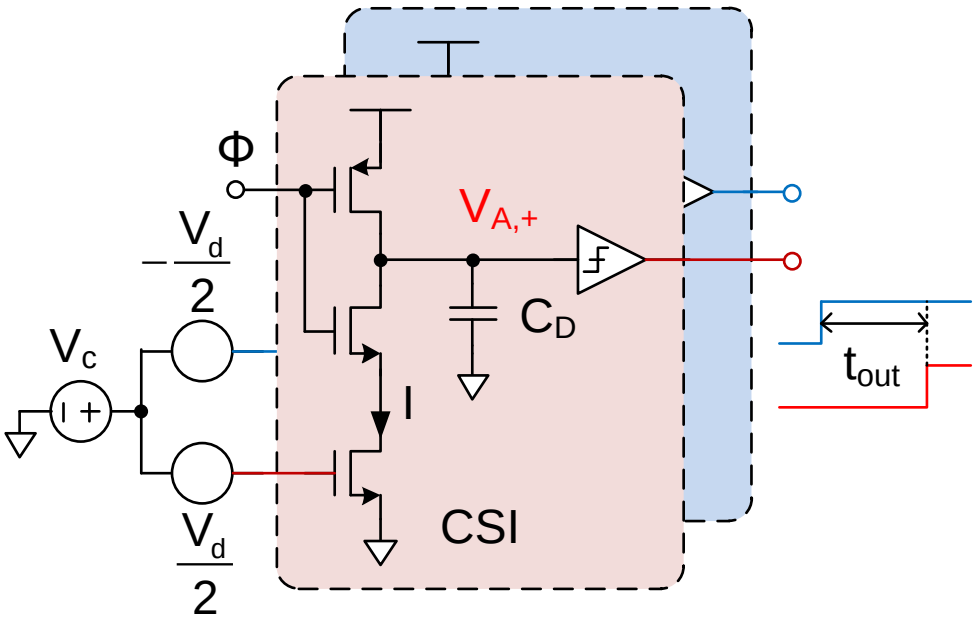
Backup slides

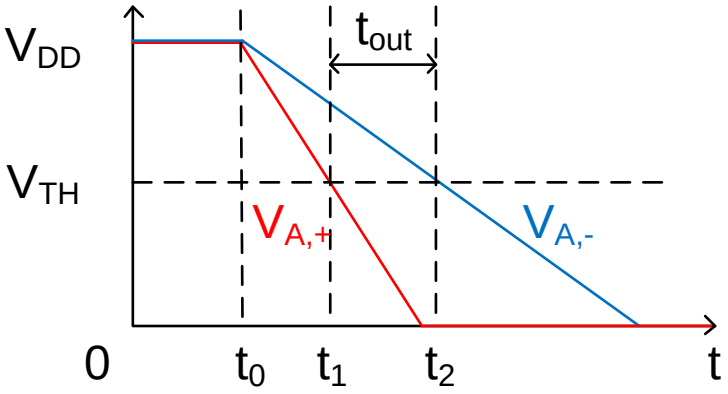
Pulse-Shape Restorer





Linearity of VTC





- CSI-based VTC

$$t_1 - t_0 = (V_{DD} - V_{TH}) \cdot \frac{C_D}{I} = \frac{K}{V_{ov}^2}$$

- Differential output time

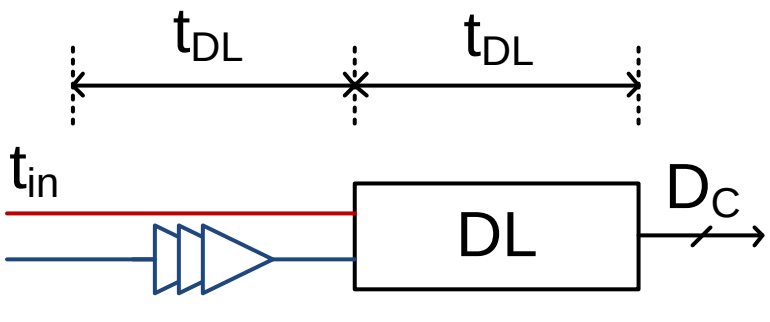
$$t_{out} = K \cdot \left(\frac{1}{V_{ov,+}^2} - \frac{1}{V_{ov,-}^2} \right)$$

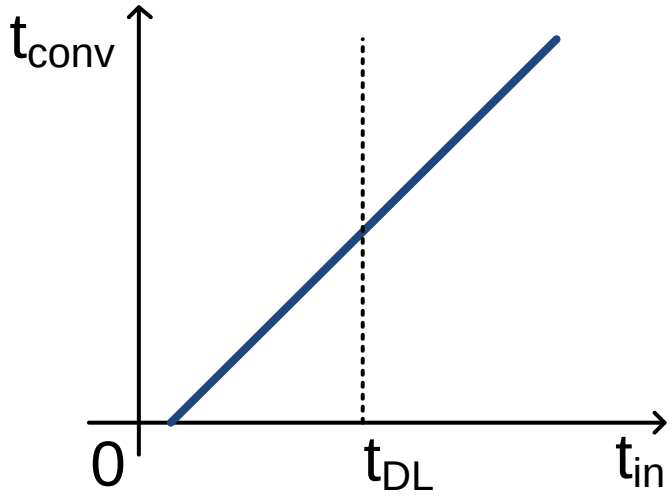
$$= -\frac{2K(V_c - V_{tn})V_d}{(V_c - V_{tn} + V_d/2)^2 \cdot (V_c - V_{tn} - V_d/2)^2}$$

$$\text{If } (V_c - V_{tn}) >> \left| \frac{V_d}{2} \right|, \; t_{out} \approx \frac{2K}{(V_c - V_{tn})^3} V_d$$

- $V_c \uparrow$, linearity $\uparrow$

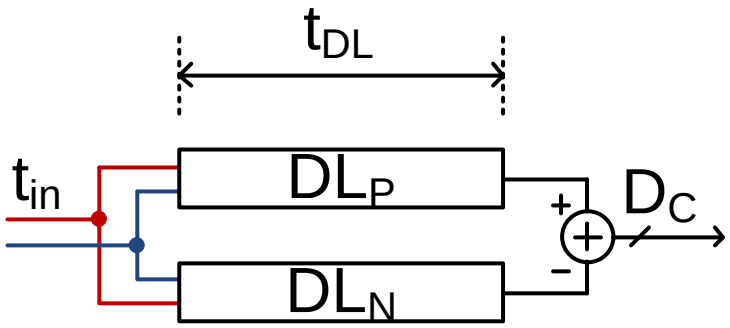
Coarse TDC

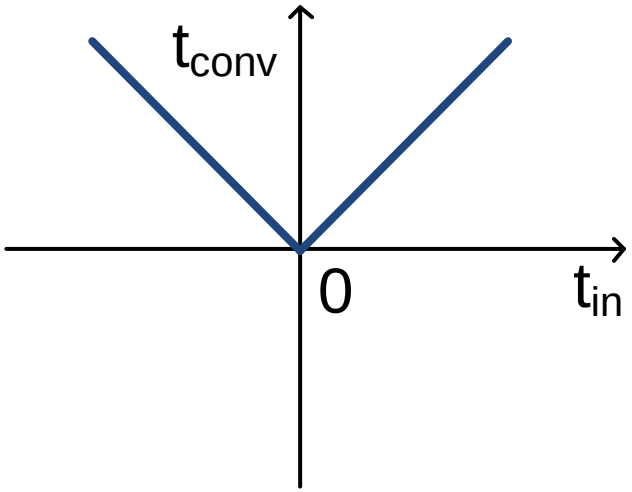




[5] Macpherson, CICC13

- Offset DL
- Twice conv. time cost

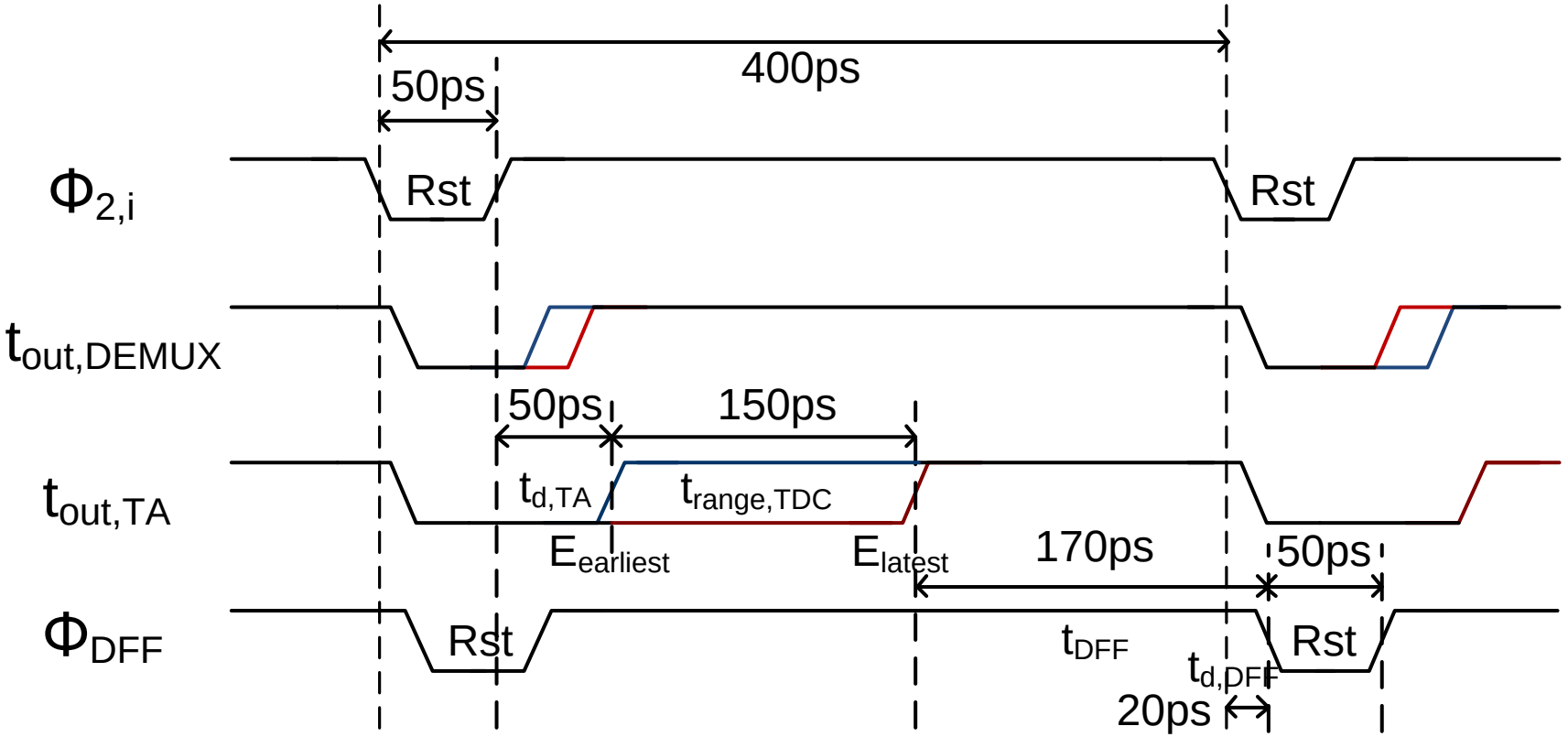




[4] Stephan, 2010

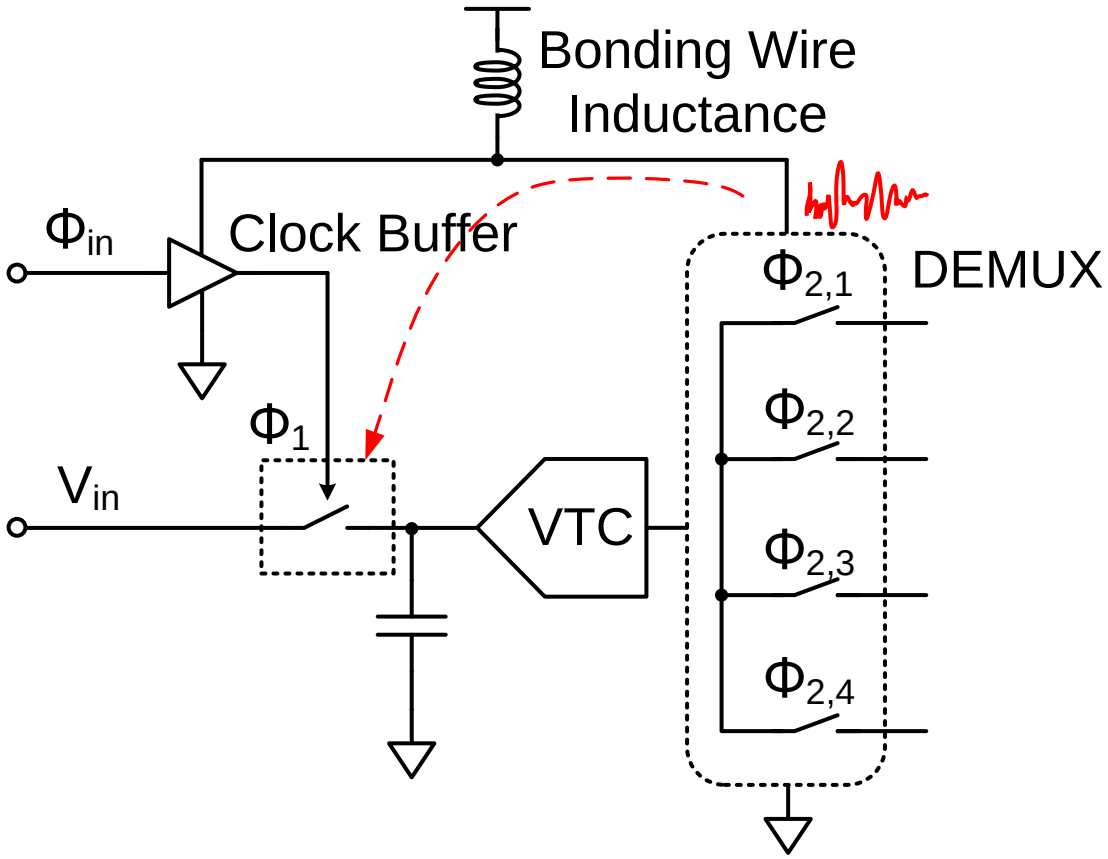
- Folded Differential DL
- No extra conv. time cost

Timing Diagram of TDC



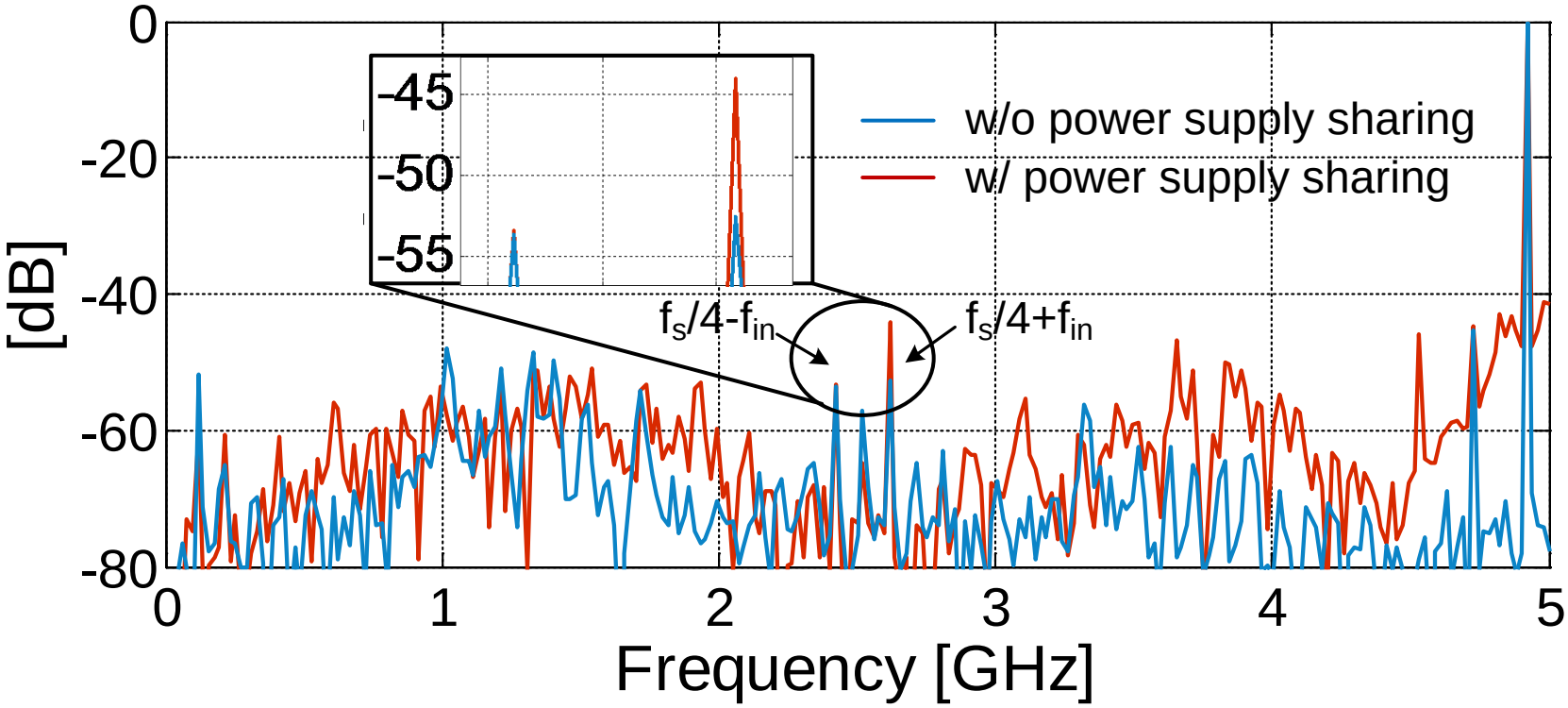
- Each channel has 400ps to complete quantization

Residual Interleaving Tones



- Residual Interleaving tone – sharing of the power supply of the DEMUX and the T/H's clock driver

Residual Interleaving Tones



- Post-layout simulation shows obvious residual interleaving tones with shared power supply