ADC Trends and Impact on SAR ADC Architecture and Analysis

Jeffrey Fredenburg and Michael P. Flynn

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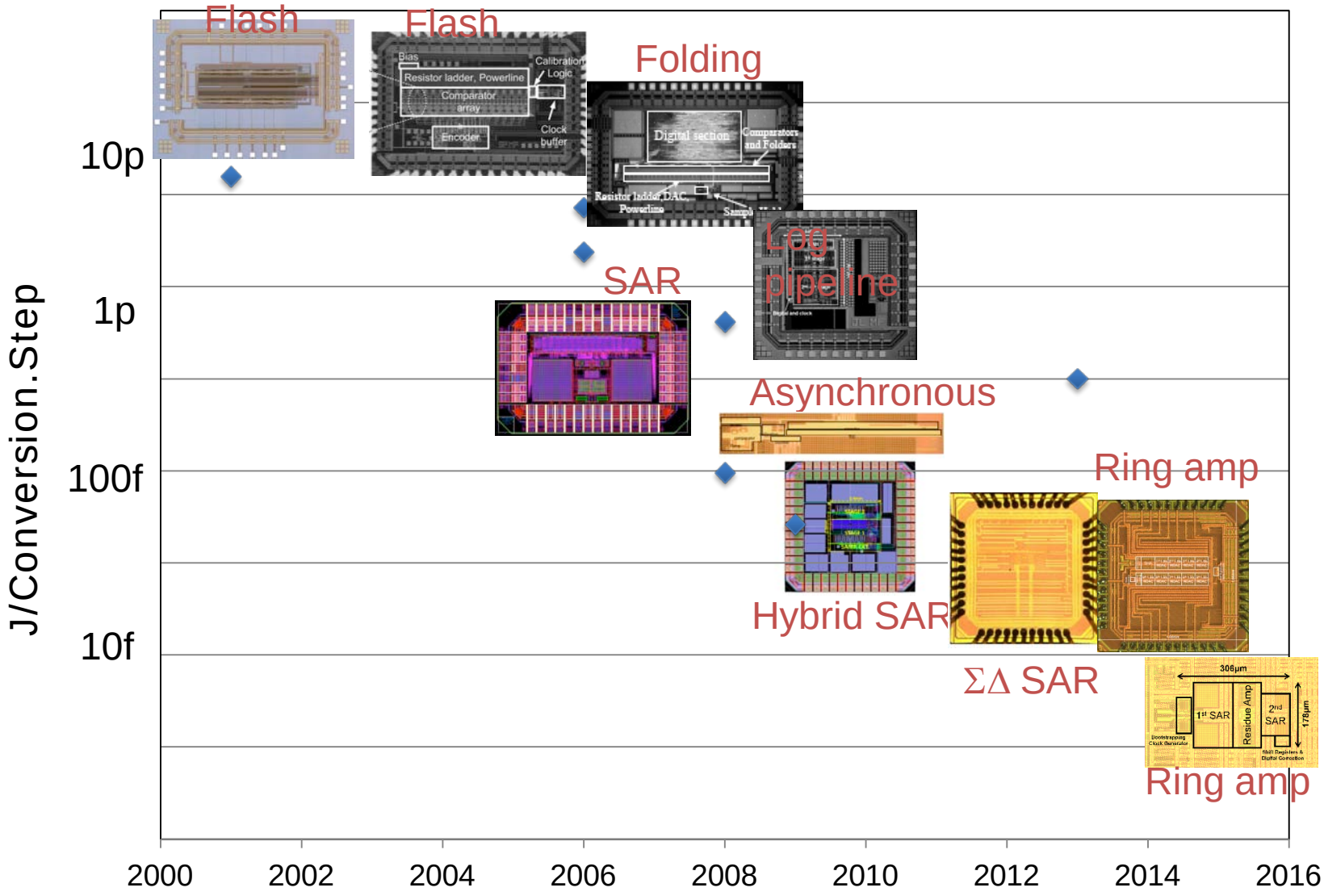
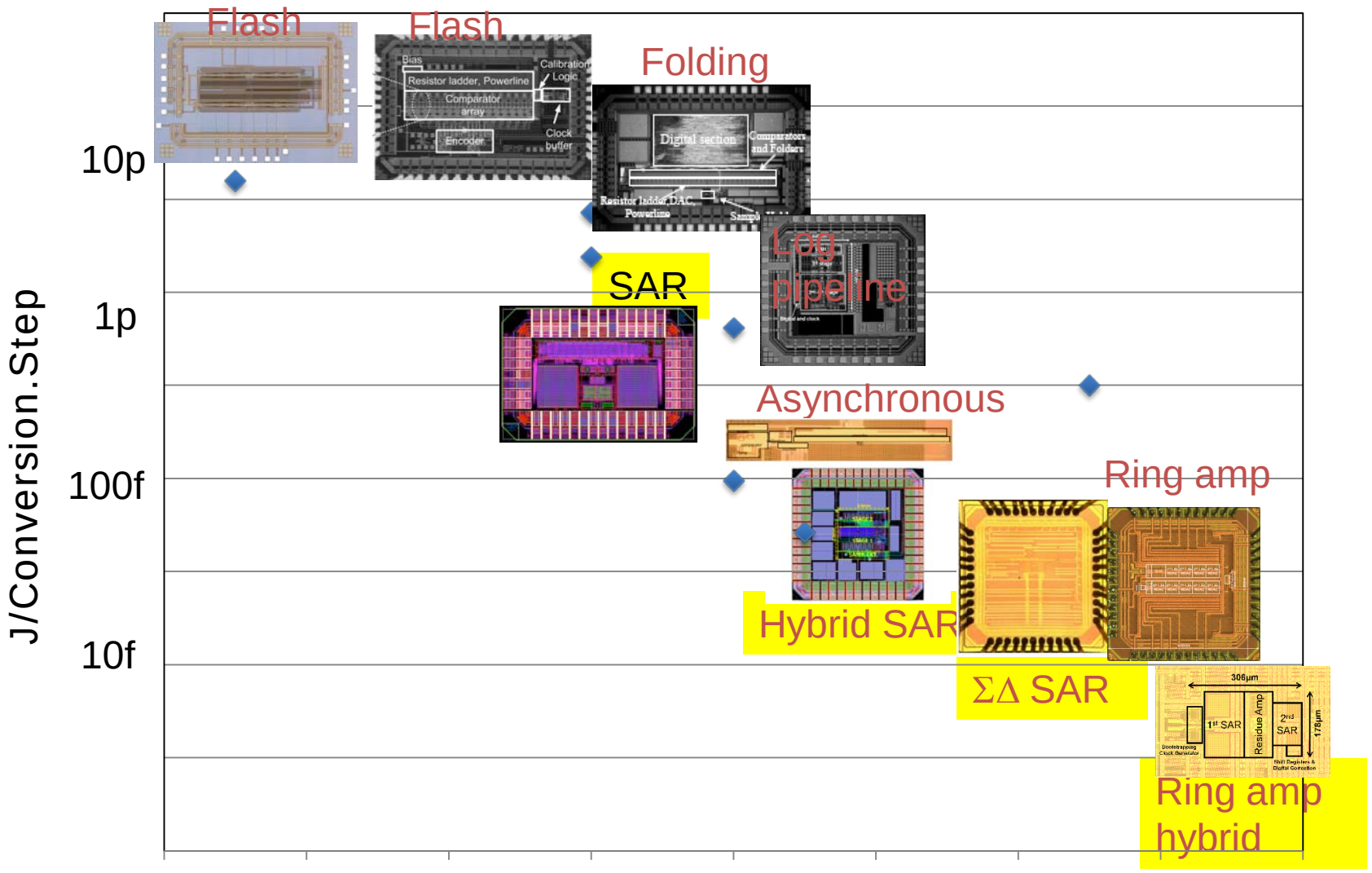
Improvement in ADC Energy Efficiency



Improvement in ADC Energy Efficiency



All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques—Part I

JAMES L. McCREARY, STUDENT MEMBER, IEEE, AND PAUL R. GRAY, MEMBER, IEEE

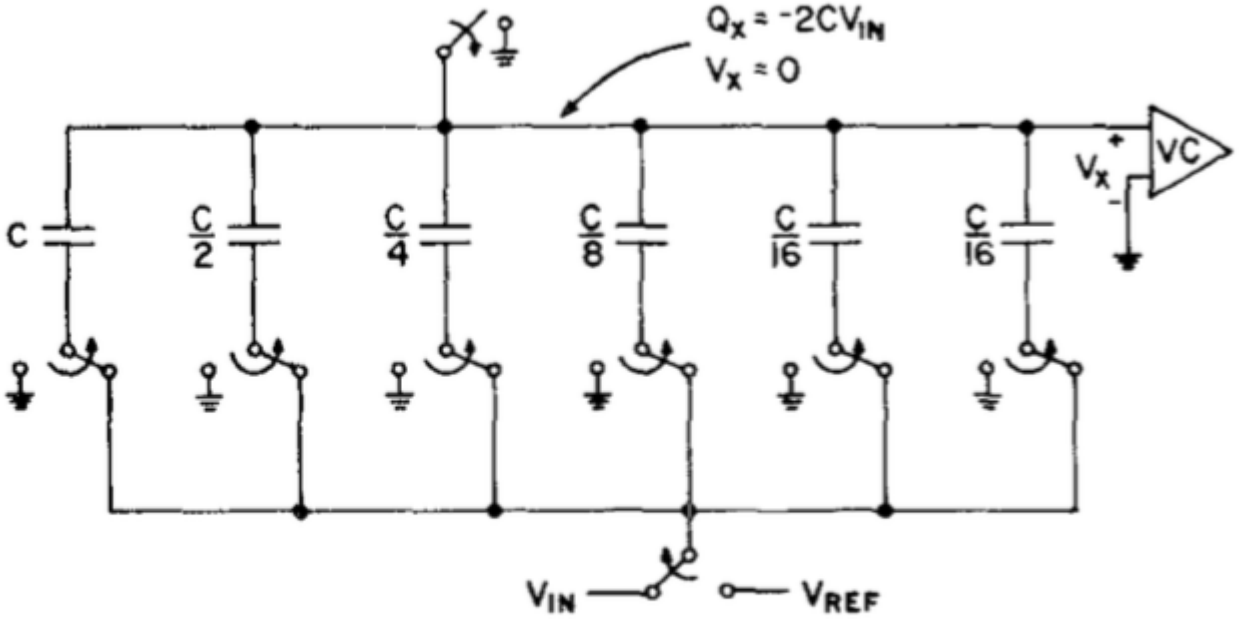
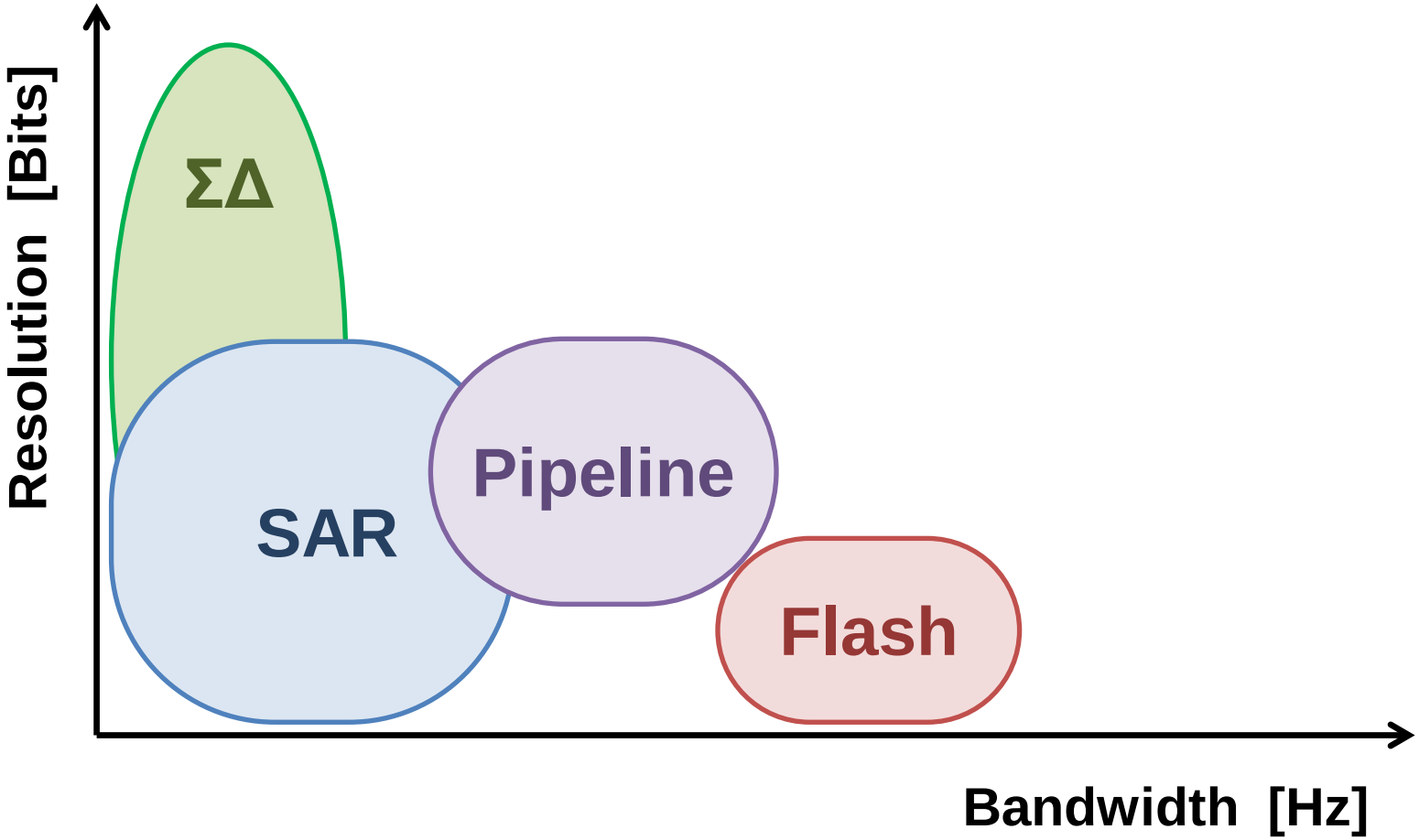


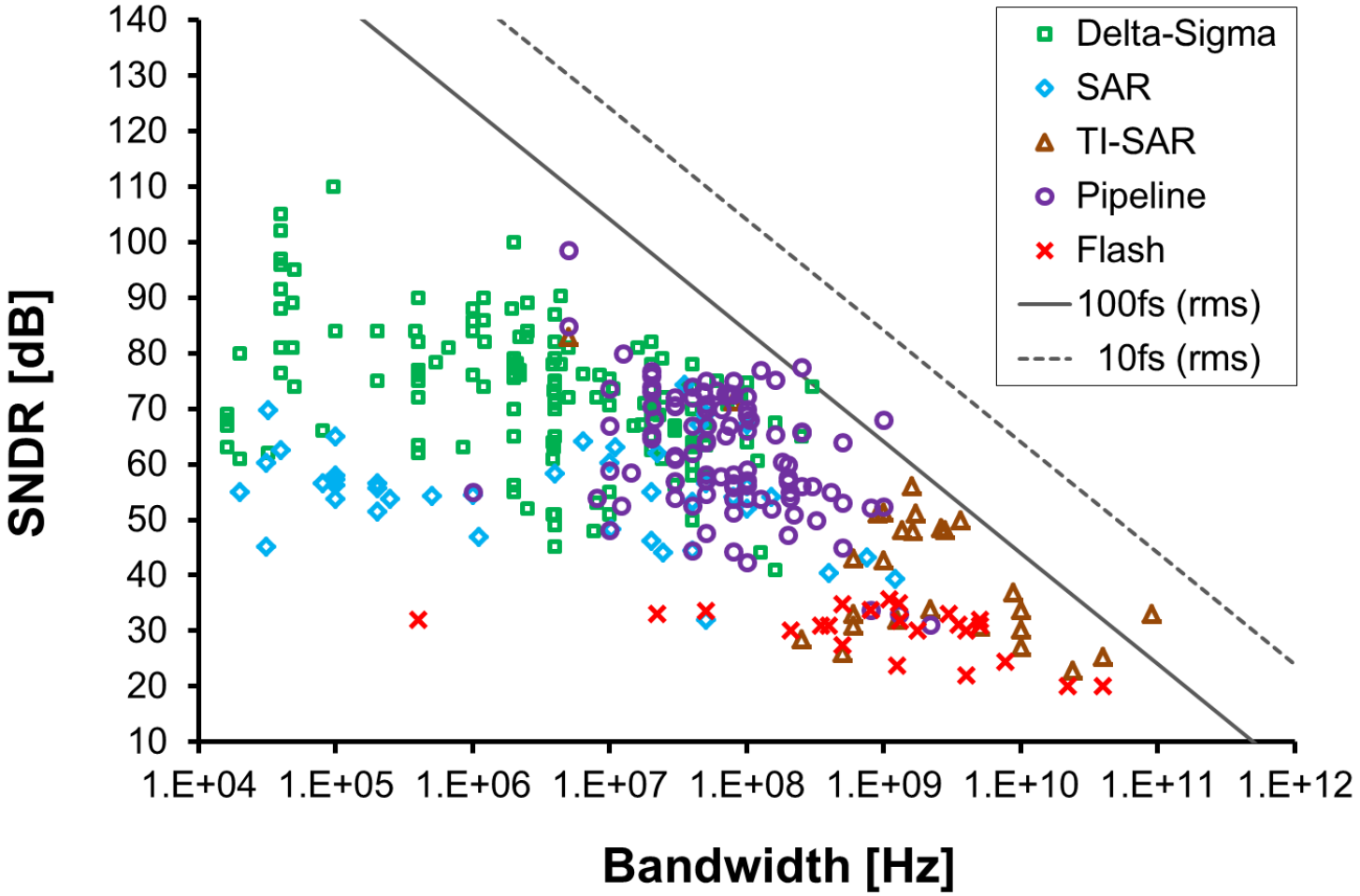
Fig. 1. Conceptual 5-bit A/D converter illustrating the sample mode operation.

[Book of the Dead - Wikipedia]

Overview

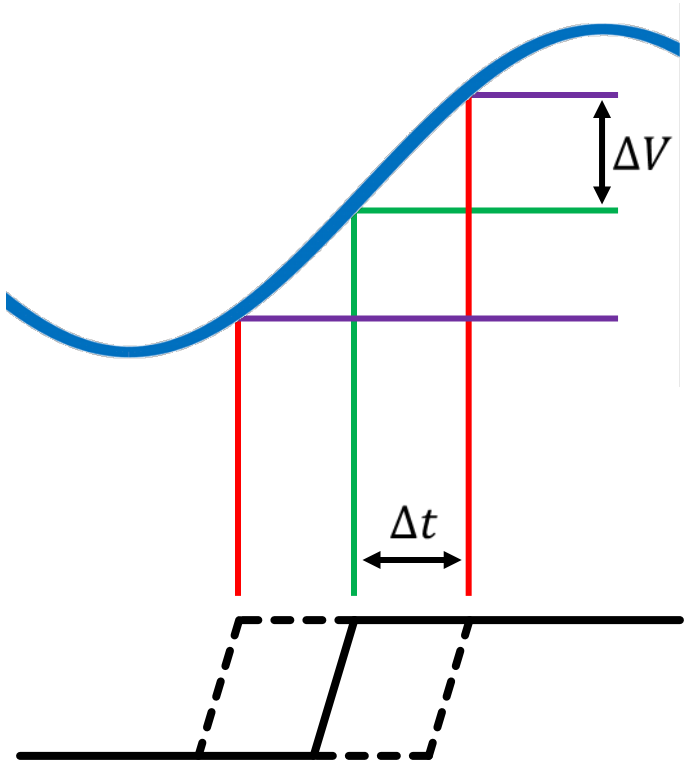
- Review of Trends
- Fundamentals
- Emerging Approaches


Resolution [Bits]
ΣΔ
SAR
Pipeline
Flash
Bandwidth [Hz]

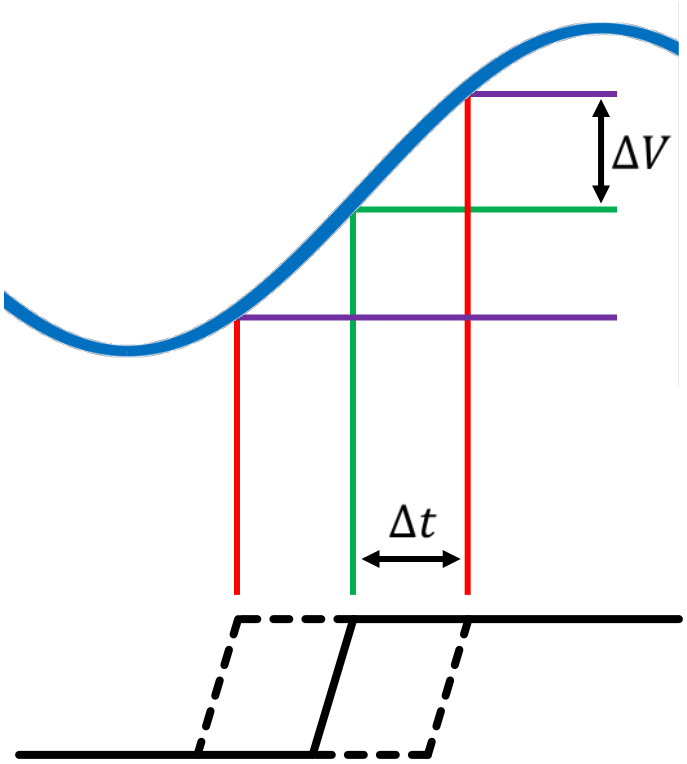


[Murmann, 2015]

Sampling Error



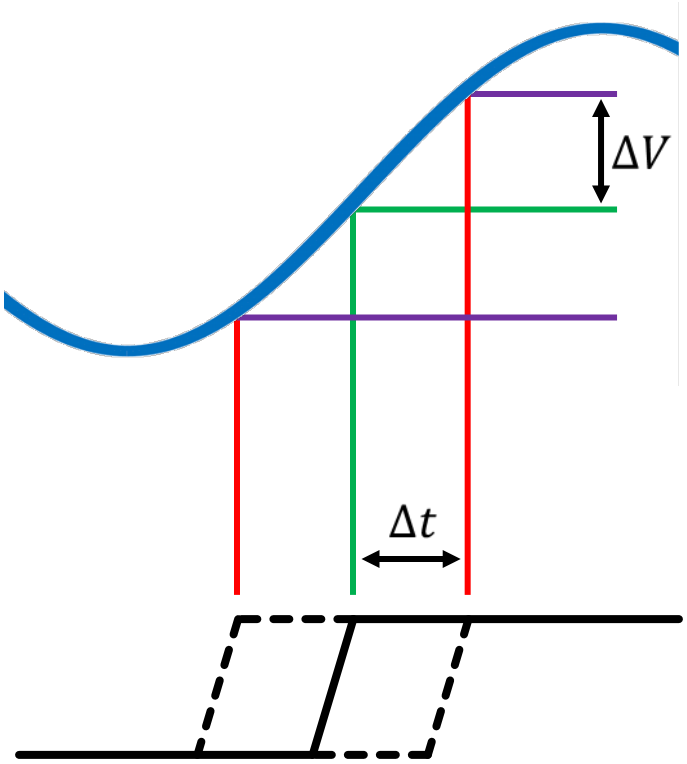
SNR-Jitter Limit



$$\Delta V \cong \frac{\partial V_{IN}}{\partial t}\Delta t$$

$$\Delta V \cong \pi\, V_{FS}\, f_{IN}\Delta t$$

SNR-Jitter Limit

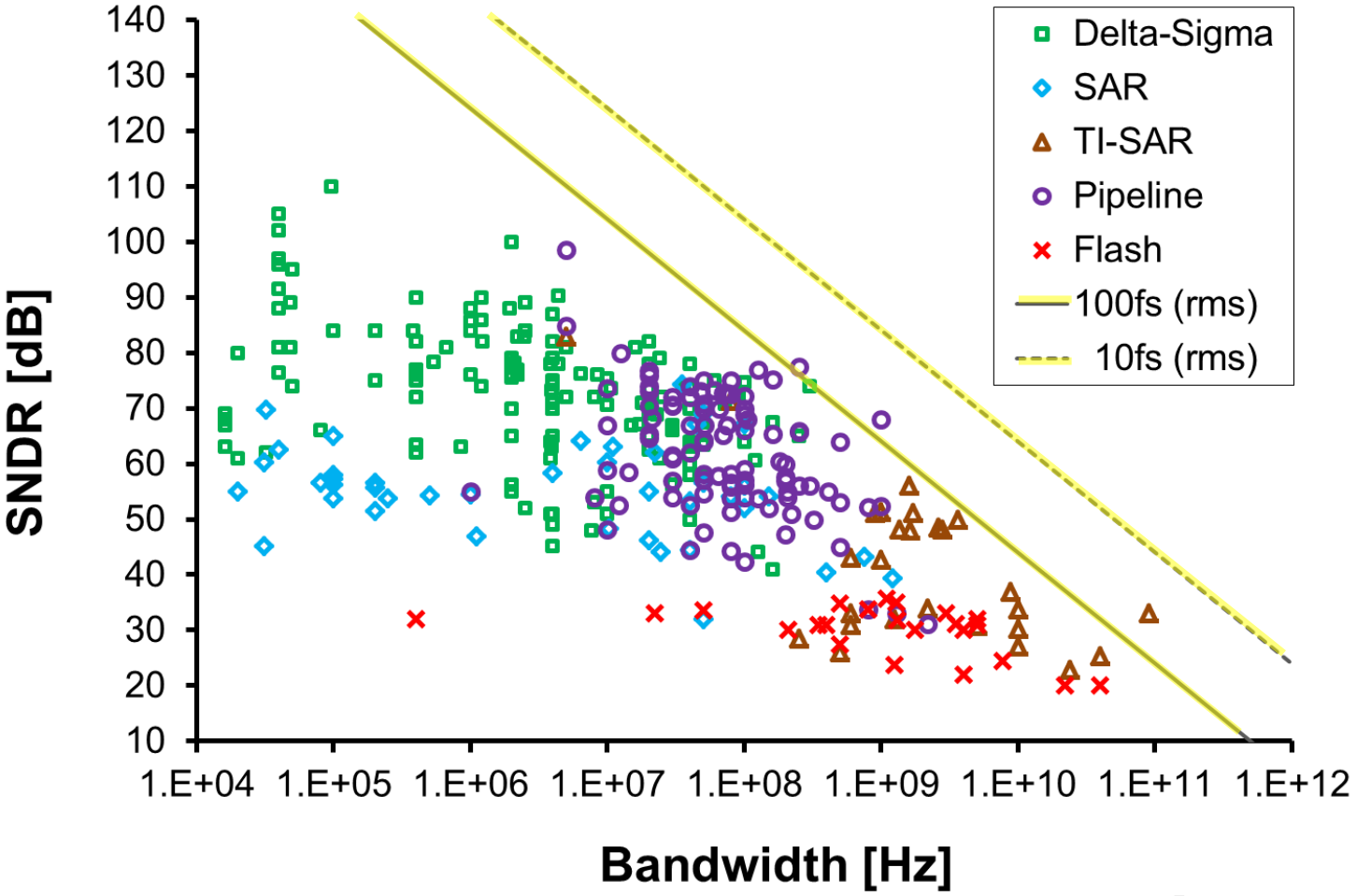


$$\Delta V \cong \frac{\partial V_{IN}}{\partial t}\Delta t$$

$$\Delta V \cong \pi\, V_{FS}\, f_{IN}\Delta t$$

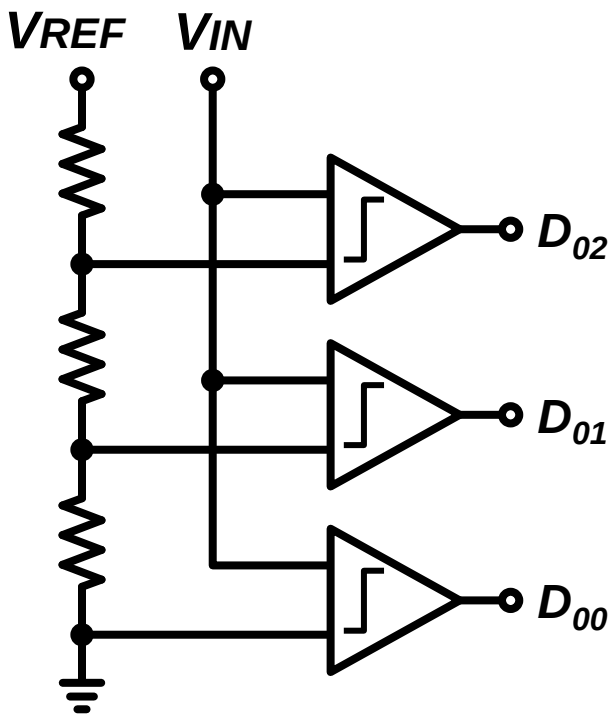
$$\boldsymbol{SNR \leq 20\, log_{10}\left[\frac{1}{\pi\, f_{IN}\sigma_{\Delta t}}\right]}$$

Bandwidth-Jitter Limit



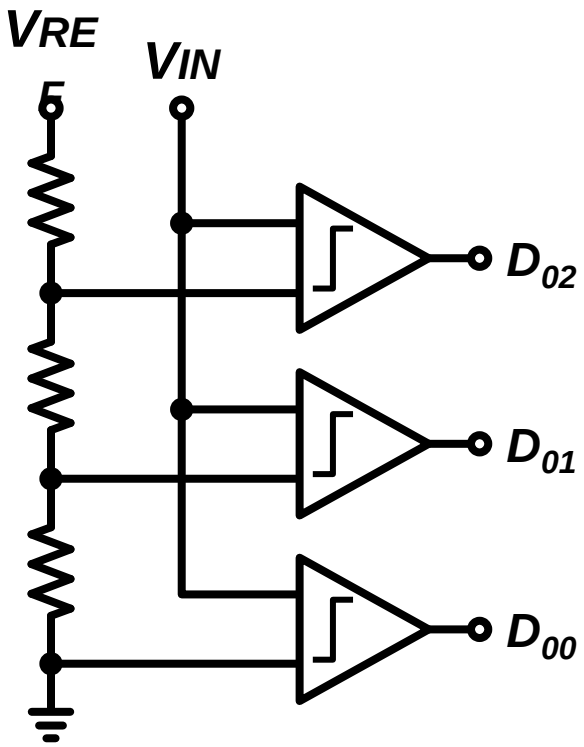
[Murmann, 2015]

Flash ADC



Power related to ~2^N Comparators

Walden FOM

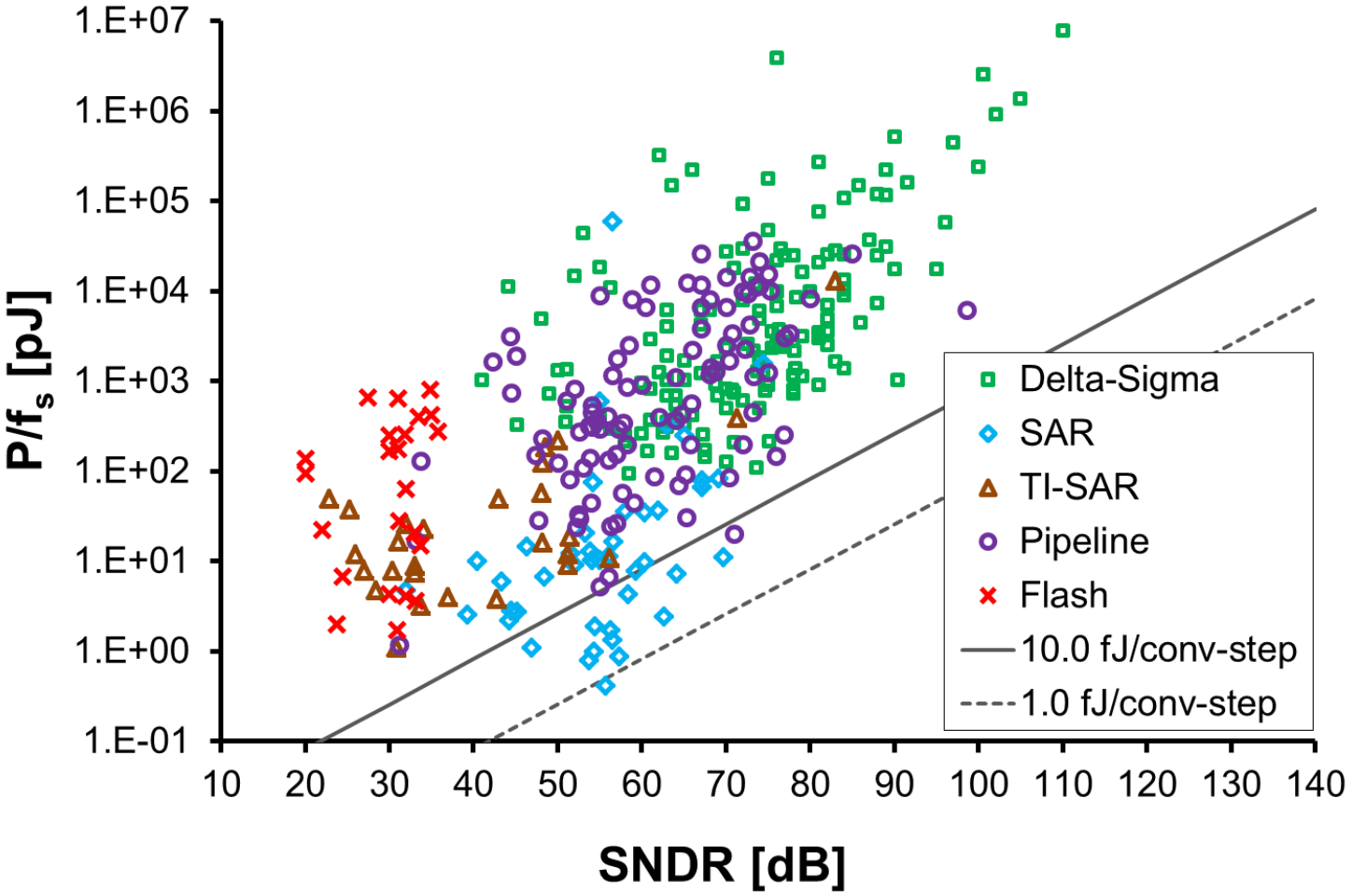


Power related to ~2^N Comparators

$$FOM_W = \frac{Power}{BW \times 2^{ENOB}}$$

[Walden, 1994]

Energy-Resolution



[Murmann, 2015]

Better FOM

Thermal Noise Limited

Trade Power for SNR

Walden FOM

$$FOM_W = \frac{Power}{BW \times 2^{ENOB}}$$

Modified Walden FOM

$$FOM_W = \frac{Power}{BW \times 2^{ENOB}}$$

$$FOM_S = \frac{Power}{BW \times 4^{ENOB}}$$

A More Useful Metric

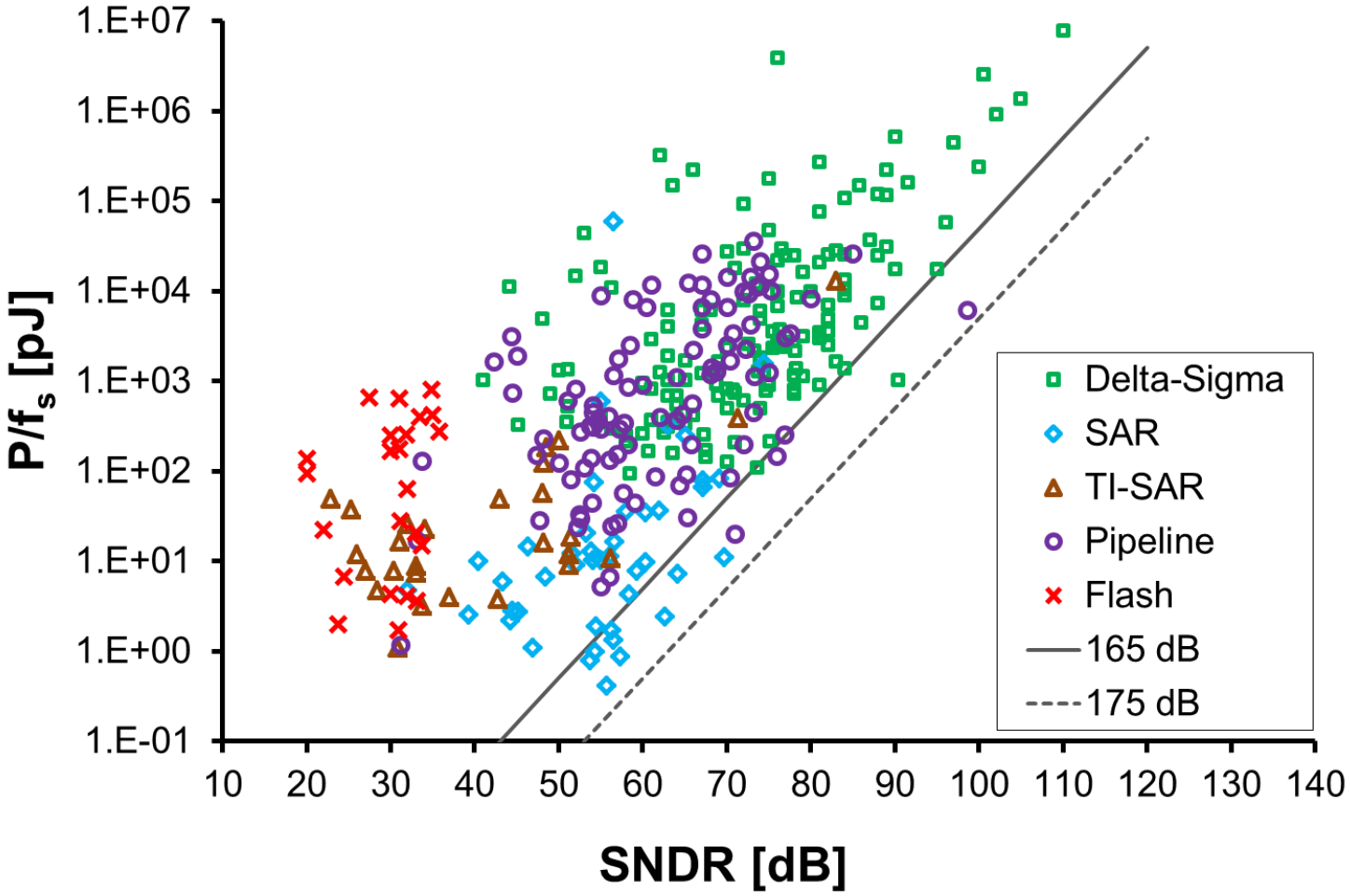
$$FOM_W = \frac{Power}{BW \times 2^{ENOB}}$$

$$FOM_S = \frac{Power}{BW \times 4^{ENOB}}$$

For ideal ADC

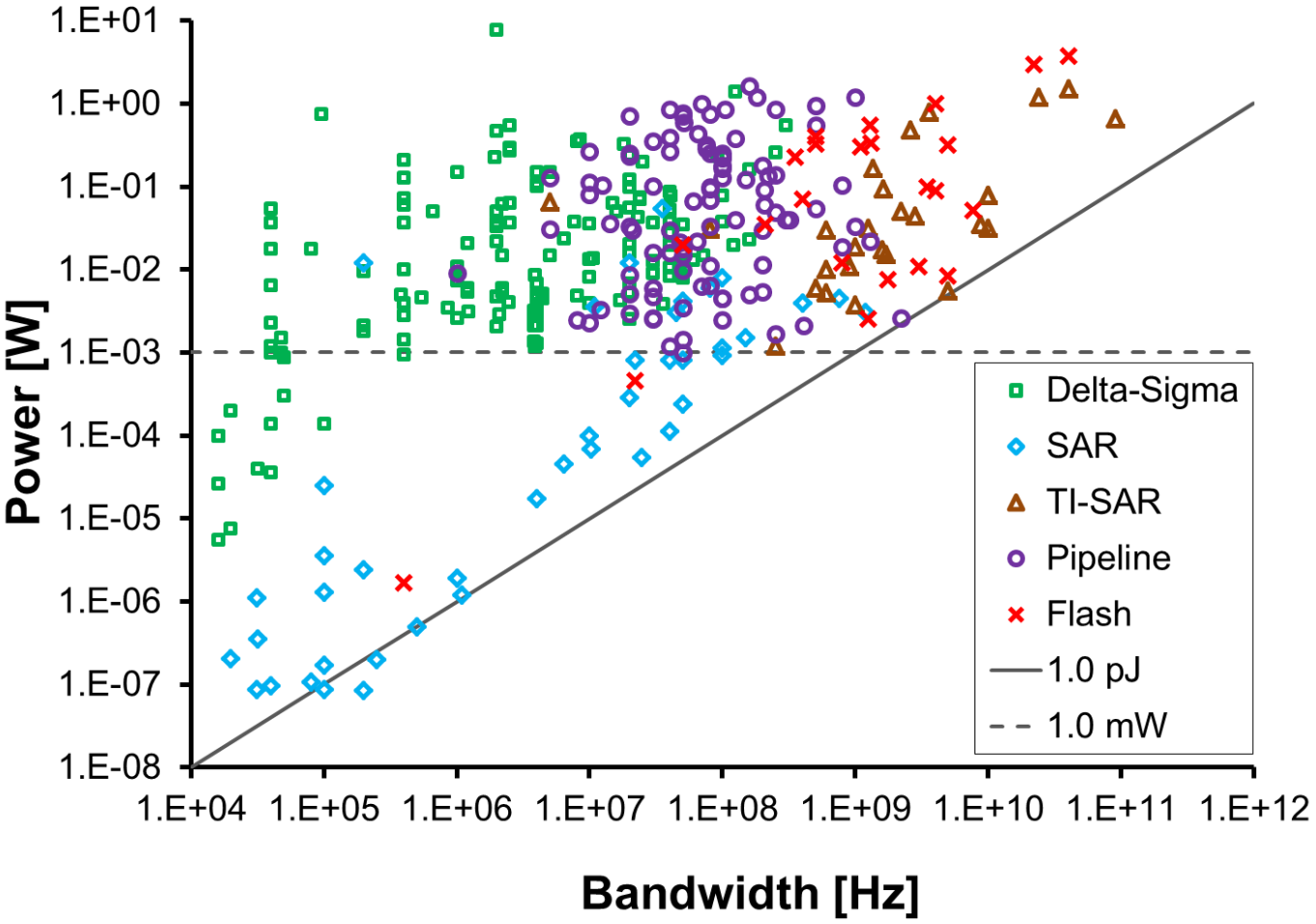
$$SNR = \frac{3}{2} \times 4^{ENOB}$$

‘Schreier’ FOM

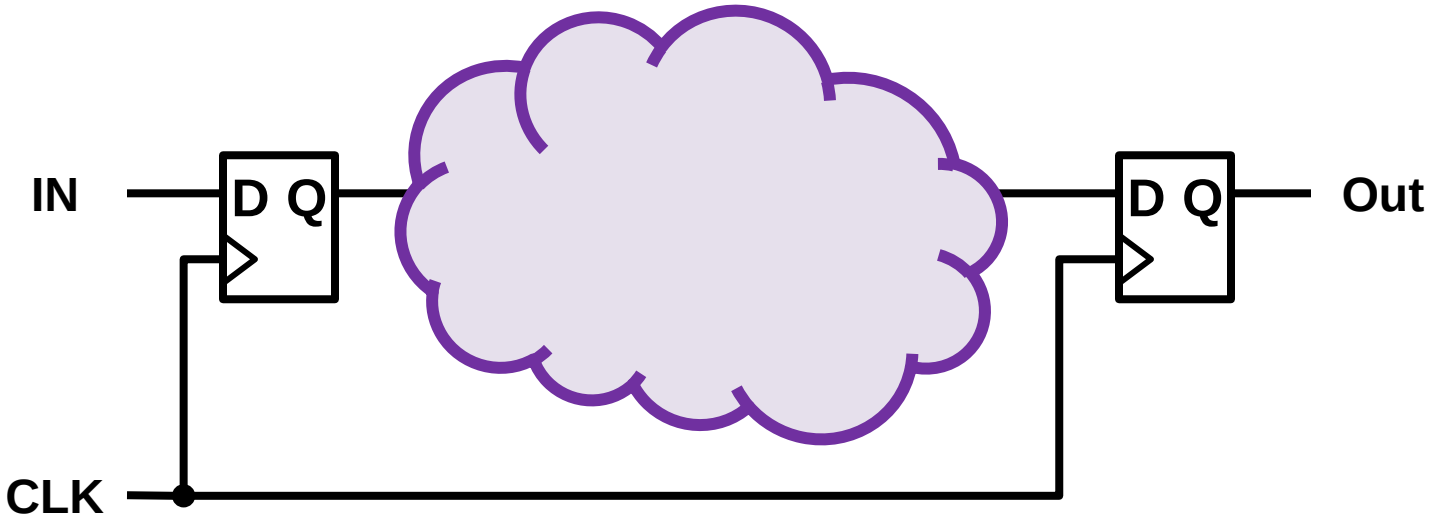


[Murmann, 2015]

Power-Bandwidth



Digital Circuits



$$\Delta E_{dig} \approx \sum \alpha_i C_i {V_{DD}}^2$$

Overview

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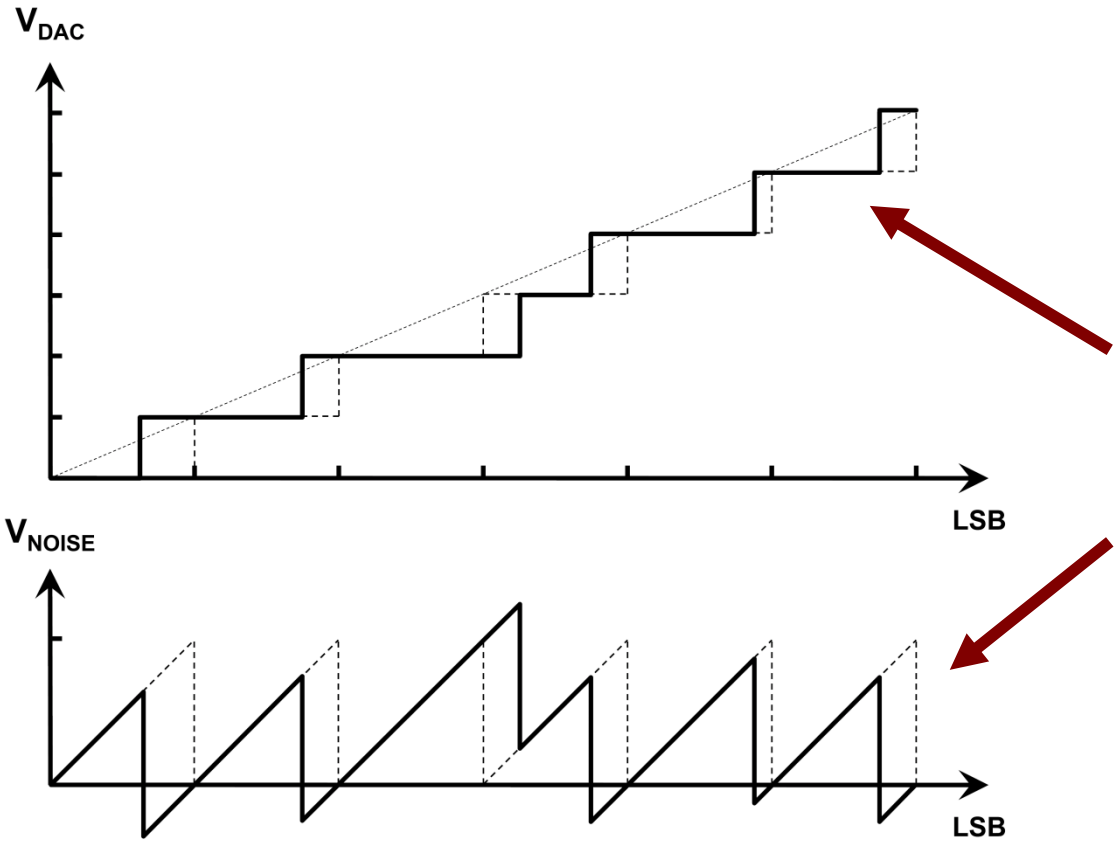
Capacitor Mismatch SNDR and Yield

[J. A. Fredenburg and M. P. Flynn, “Statistical Analysis of ENOB and Yield in Binary Weighted ADCs and DACS with Random Element Mismatch,” *IEEE TCAS I* July 2012]

Cap Accuracy Fundamentals



Cap Mismatch causes DNL/INL errors

First Find DNL

N bit binary DAC

LSB size

$$V_{DAC} = \sum_{i=1}^{N} b_i 2^{i-1}(1+\gamma_i)\Lambda$$

Error of binary cap i

DNL Pattern

3 bit binary DAC

$$D_3 = \{d_1 \quad d_2 \quad d_1 \quad d_3 \quad d_1 \quad d_2 \quad d_1\}$$

Error of due to LSB cap

- Only N unique DNL errors for N bit DAC

DNL at Code i

Already:

$$V_{DAC} = \sum_{i=1}^{N} b_i 2^{i-1}\left(1+\gamma_i\right)\Lambda$$

DNL

$$d_i = 2^{i-1}\gamma_i - \sum_{j=1}^{i-1} 2^{j-1}\gamma_j$$

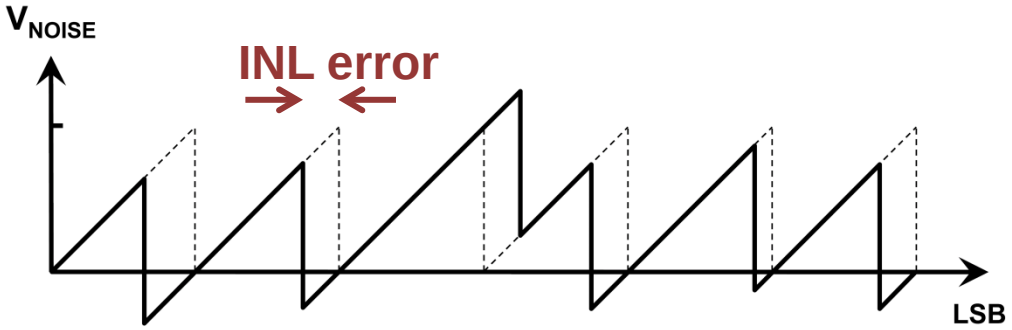
Unique DNL values

Noise Associated with Mismatch

Ideal ADC:

$$V_{noise}^{\ 2} = \frac{\Lambda^2}{12}$$

Non-ideal ADC:



$$V_{noise}^{\ 2} = \frac{\Lambda^2}{12} + \frac{\Lambda^2}{2^N}\sum_{i=0}^{2^N-1} INL_i^2$$

Noise Associated with Mismatch

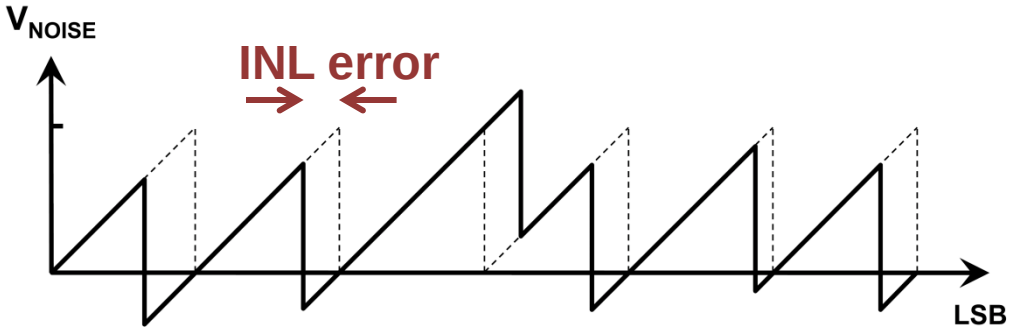
$$V_{noise}^{\ 2} = \frac{\Lambda^2}{12} + \frac{\Lambda^2}{2^N} \sum_{i=0}^{2^N-1} INL_i^2$$

$$\mathrm{I}NL_i = \sum_{j=1}^{i} \mathrm{D}NL_j$$

Using DNL pattern (folding symmetry)

$$V_{noise}^{\ 2} = \frac{\Lambda^2}{12} + \frac{\Lambda^2}{4} \left[\gamma_0^{\ 2} + \sum_{i=1}^{N} \left(2^{i-1} \gamma_i \right)^2 \right]$$

Cap Mismatch Noise



Noise vs mismatch

$$V_{noise}^{\ 2} = \frac{\Lambda^2}{12} + \frac{\Lambda^2}{4}\left[\gamma_0^{\ 2} + \sum_{i=1}^{N}\left(2^{i-1}\gamma_i\right)^2\right]$$

INL vs Cap Error

$$\text{Mean}\left(INL^2\right) = \frac{1}{4}\gamma_0^{\ 2} + \frac{1}{4}\sum_{i=1}^{N}\left(2^{i-1}\gamma_i\right)^2$$

ENOB vs Cap Mismatch

$$V_{noise}^{\ 2} = \frac{\Lambda^2}{12} + \frac{\Lambda^2}{4}\left[\gamma_0^{\ 2} + \sum_{i=1}^{N}\left(2^{i-1}\gamma_i\right)^2\right]$$

$$ENOB = N - \log_4\left[1 + 3\gamma_0^{\ 2} + 3\sum_{i=1}^{N-1}\left(2^{i-1}\gamma_i\right)^2\right]$$

$$\gamma_i = \frac{1}{2}\left(\gamma_{i,p} + \gamma_{i,m}\right) \quad i \in \{0,\ldots,N-1\}$$

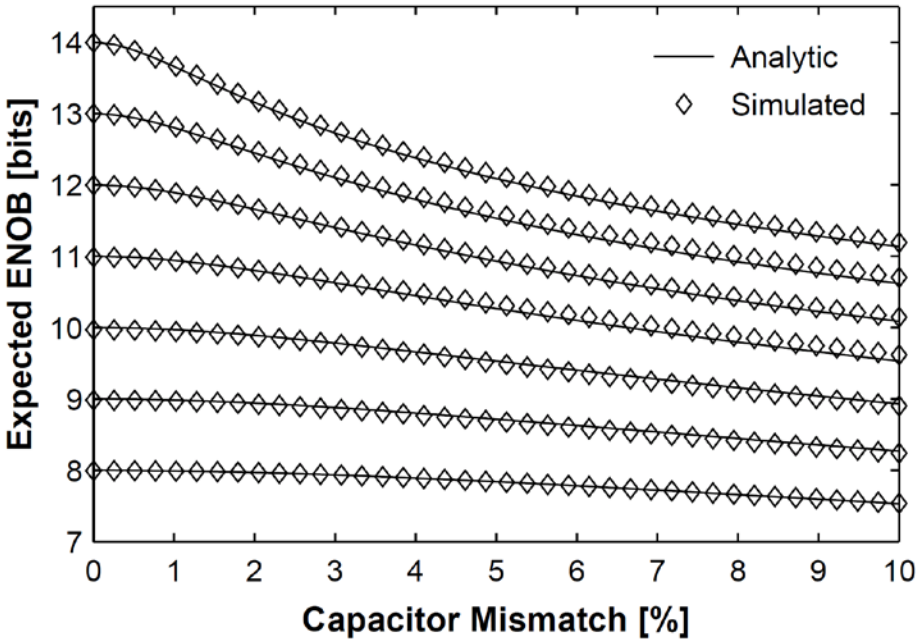
For uniformly distributed input

ENOB vs Cap Mismatch

Sinusoidal input

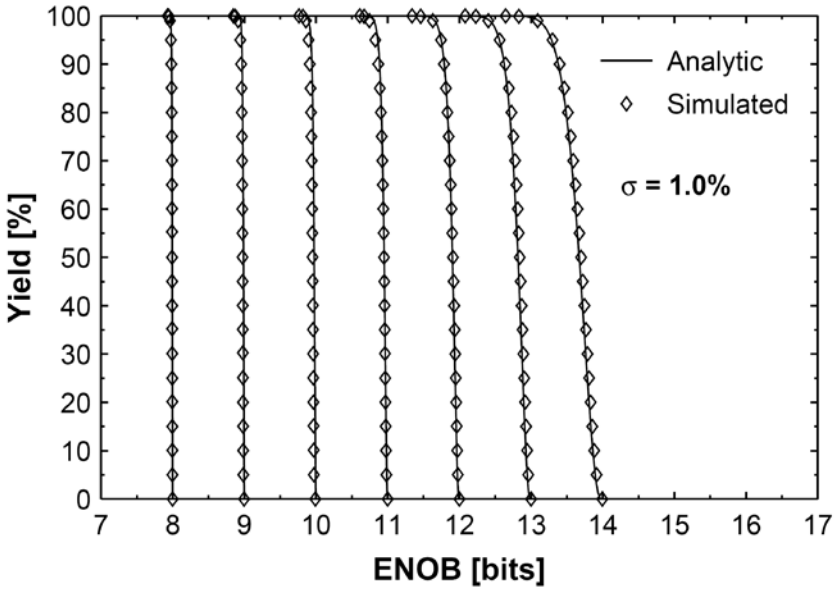
$$ENOB = N - \log_4\left[1 + 3\alpha\gamma_0^{\,2} + 3\alpha\sum_{i=1}^{N-1}\left(2^{i-1}\gamma_i\right)^2\right]$$

$$\alpha = \frac{3(4-\pi)}{\pi} \cong 0.8197$$



- First closed form expression for ENOB

Yield vs Cap Matching



$$\mathrm{P}(ENOB > ENOB_{MIN}) = \mathrm{P}(X < 4^{N-ENOB_{MIN}} - 1)$$

$$X = \sum_{i=0}^{N-1} \eta_i$$

$$\mathrm{F_X}(x) = \int_0^x \int_0^{\frac{\pi}{2}} \cdots \int_0^{\frac{\pi}{2}} \sum_{i=1}^{N/2} B_i e^{-\lambda_i t}\, d\theta_1 \cdots\, d\theta_{N/2}\, dt$$

$$B_i = \left[(\lambda_i - s) \prod_{j=1}^{N/2} \left(\frac{A_j}{\lambda_j - s} \right) \right|_{s \to \lambda_i}$$

$$A_i = \frac{1}{\pi \sigma_{2i-2} \sigma_{2i-1}} \qquad \lambda_i = \frac{\cos^2 \theta_i}{2\sigma_{2i-2}^2} + \frac{\sin^2 \theta_i}{2\sigma_{2i-1}^2}$$

- First closed form expression for ENOB CDF
  - Can take weeks for 14 bit

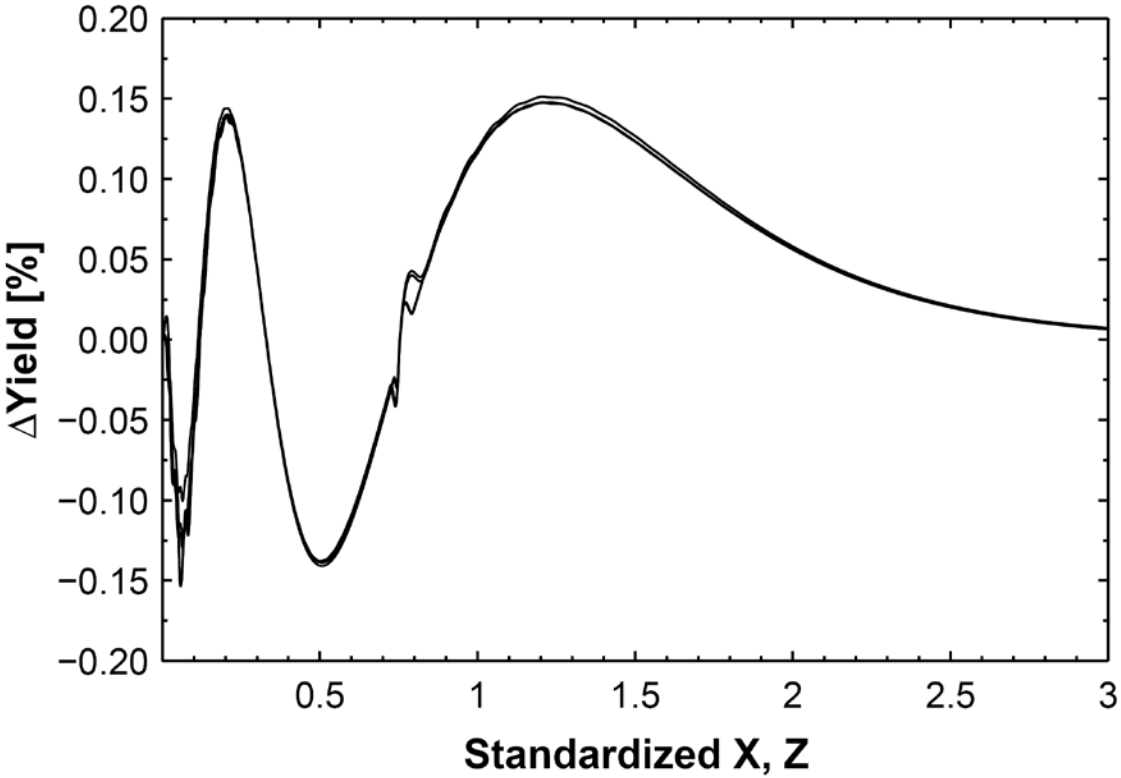
Useful Designer Equations

Simple Yield Equation

Simple Mismatch Equation

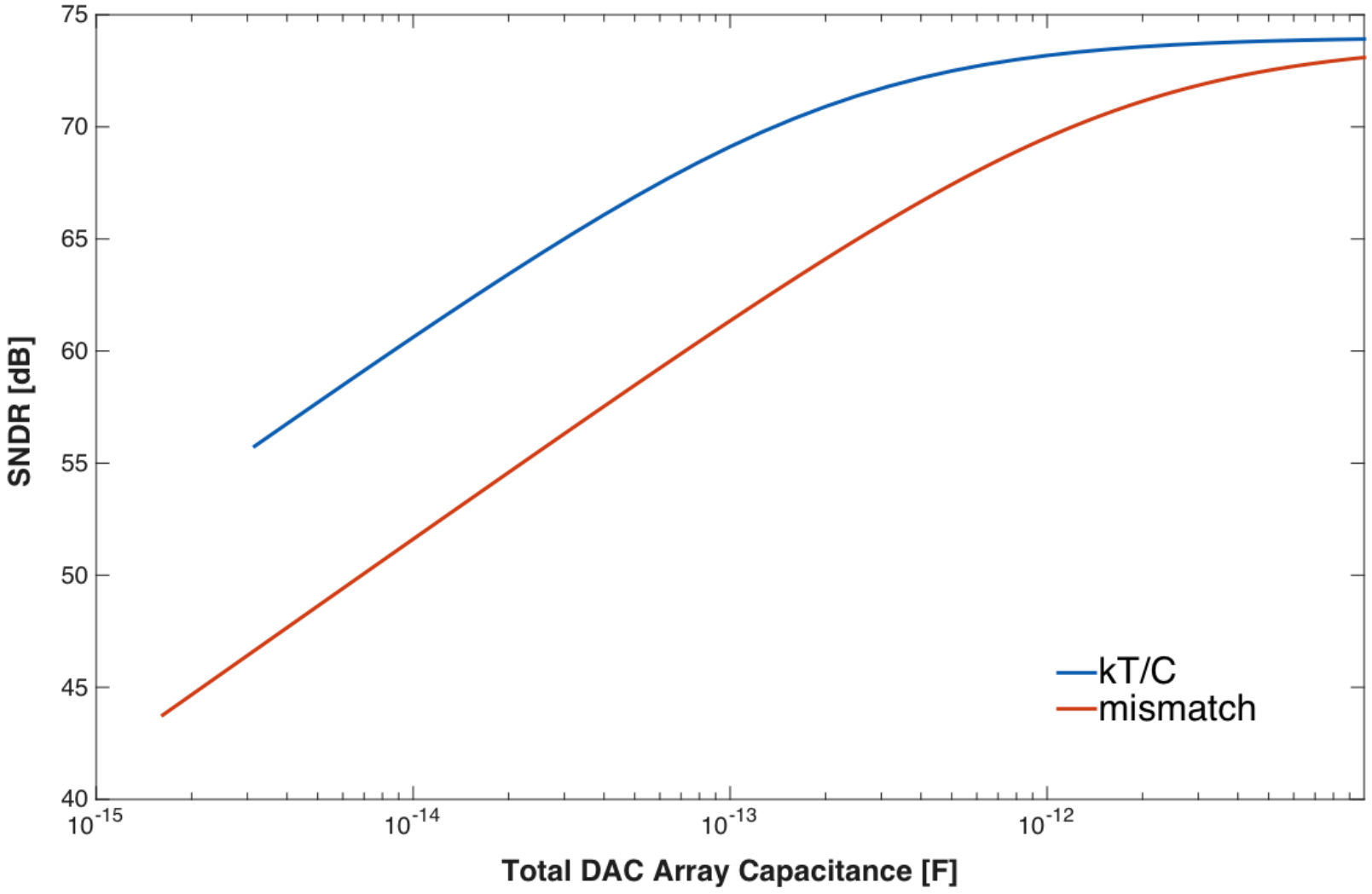
```
% Parameter Values
N = 9;  SIGMA = 0.1;  ENOB_MIN = 7.7;
YIELD = 0.95;  k = 7.944;  b = 13.146;

% Yield Calculation
X=4^(N-ENOB_MIN)-1;
Z=X/2^N/SIGMA^2;
YIELD=gammainc(b*sqrt(Z),k)

% Sigma Calculation
X=4^(N-ENOB_MIN)-1;
Z=(gammaincinv(YIELD,k)/b)^2;
SIMGA=sqrt(X/Z/2^N)
```

Accuracy of Design Equation



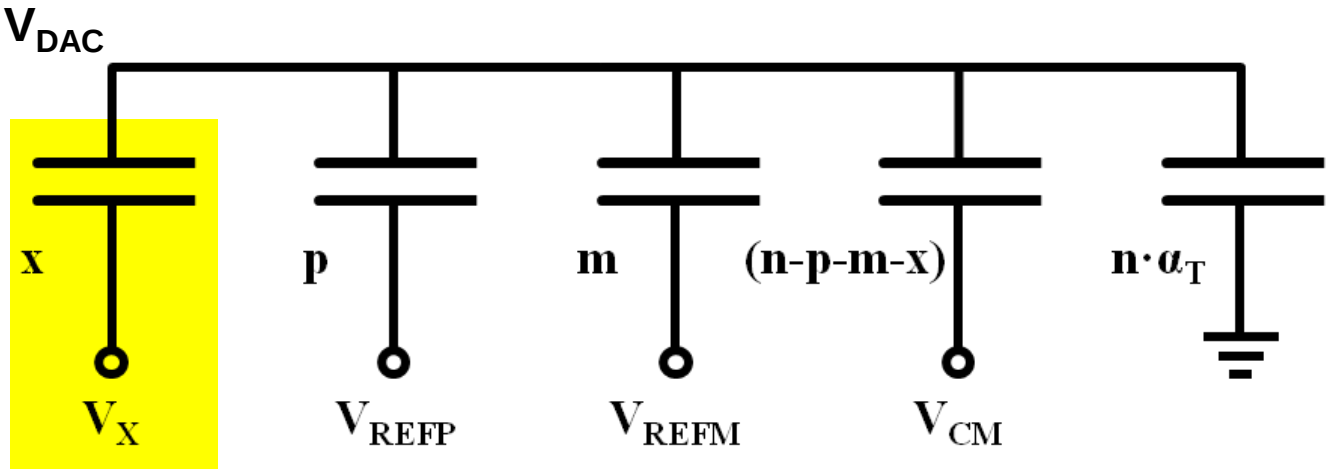
Predicted Yields are within **±0.2%** with simple design equation

12 bit Array Example



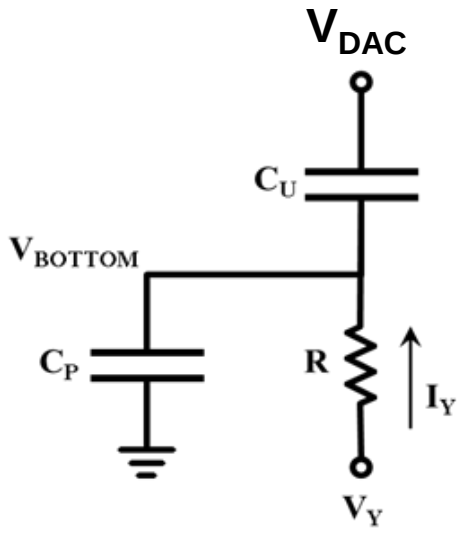
DAC Switching Energy

DAC Switching Energy



Switch x unit caps

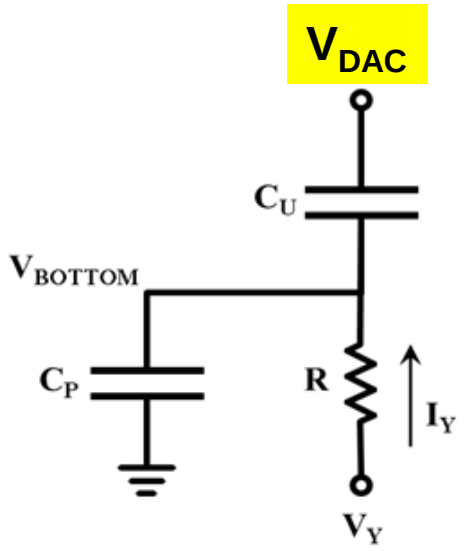
Unit Cap Model



Bottom plate
Parasitic cap

$$\Delta E_Y = \left[C_u \left(\Delta V_Y - \Delta V_{DAC} \right) + C_p \Delta V_Y \right] V_Y$$

Unit Cap Model



Bottom plate
Parasitic cap

$$\Delta V_{DAC} = \frac{x}{n(1+\alpha_T)}\Delta V_Y$$

$$\Delta E_Y = \left[C_u\left(\Delta V_Y - \Delta V_{DAC}\right) + C_p \Delta V_Y\right] V_Y$$

Energy from References

$$\Delta E = \Delta E_{\text{Indpendent}} + \Delta E_{\text{Depdendent}}$$

$$\Delta E_{\text{Indpendent}} = \tfrac{1}{8} C_u V_{FS}^{\,2} \left[x\left(1+\alpha_p\right) - \frac{x^2}{n\left(1+\alpha_T\right)} \right]$$

$$\Delta E_{\text{Dependent}} = \tfrac{1}{8} C_u V_{FS}^{\,2} \left[\frac{x\left(m-p\right)}{n\left(1+\alpha_T\right)} \right] \text{sign}\left(\Delta V_{X,\text{DIFF}}\right)$$

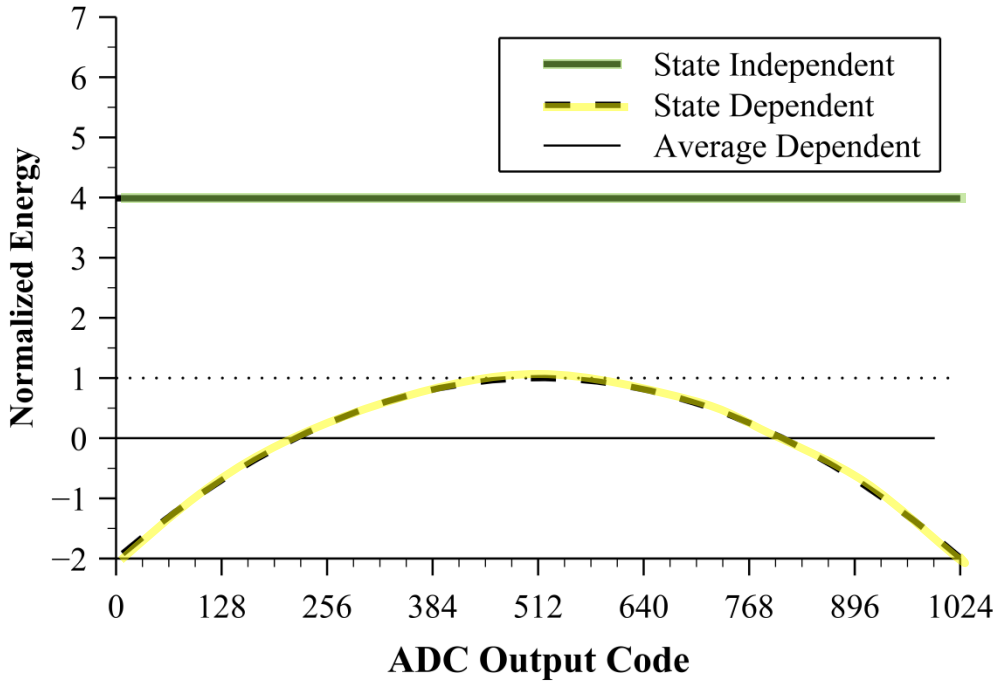
Function of DAC switching

Energy from References

$$\Delta E = \Delta E_{\text{Indpendent}} + \Delta E_{\text{Depdependent}}$$

$$\Delta E_{\text{Indpendent}} = \tfrac{1}{8} C_u V_{FS}^{\,2} \left[x\left(1+\alpha_p\right) - \frac{x^2}{n\left(1+\alpha_T\right)} \right]$$

$$\Delta E_{\text{Dependent}} = \tfrac{1}{8} C_u V_{FS}^{\,2} \left[\frac{x\left(m-p\right)}{n\left(1+\alpha_T\right)} \right] \text{sign}\left(\Delta V_{X,DIFF}\right)$$



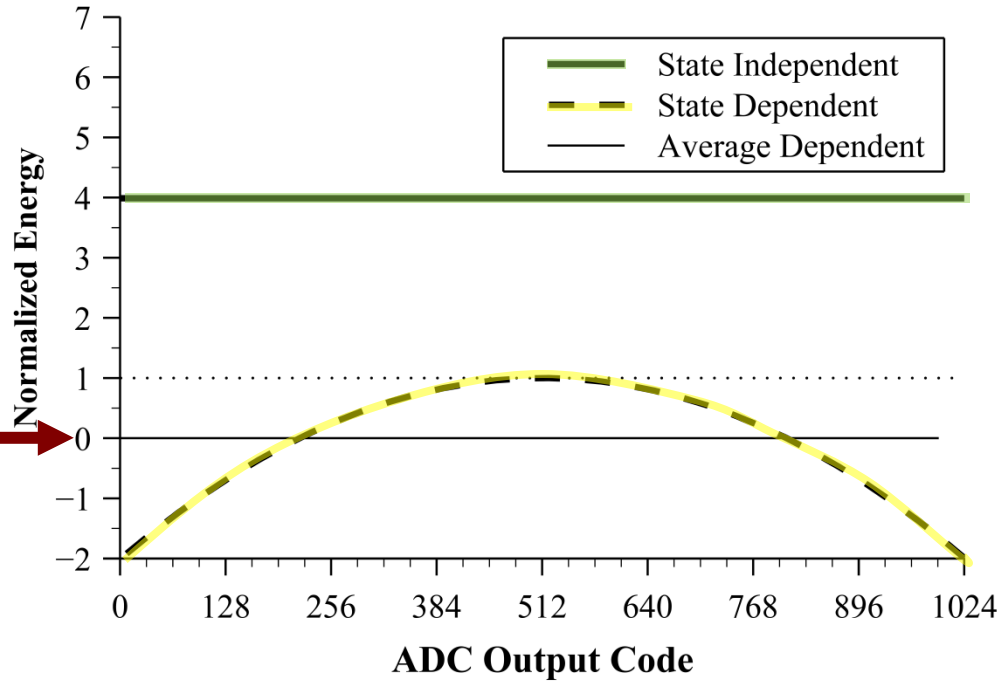
Energy from References

$$\Delta E = \Delta E_{\text{Indpendent}} + \Delta E_{\text{Depdependent}}$$

$$\Delta E_{\text{Indpendent}} = \tfrac{1}{8} C_u V_{FS}^{\,2} \left[x(1+\alpha_p) - \frac{x^2}{n(1+\alpha_T)} \right]$$

$$\Delta E_{\text{Dependent}} = \tfrac{1}{8} C_u V_{FS}^{\,2} \left[\frac{x(m-p)}{n(1+\alpha_T)} \right] \text{sign}(\Delta V_{X,DIFF})$$

Dependent averages to 0



Adding for all DAC Steps

$$\Delta E = \Delta E_{\text{Indpendent}} + \Delta E_{\text{Depdependent}}$$

$$\Delta E_{\text{Indpendent}} = \tfrac{1}{8} C_u V_{FS}^{\,2} \left[x(1+\alpha_p) - \frac{x^2}{n(1+\alpha_T)} \right]$$

$$\Delta E_{\text{Dependent}} = \tfrac{1}{8} C_u V_{FS}^{\,2} \left[\frac{x(m-p)}{n(1+\alpha_T)} \right] \text{sign}(\Delta V_{X,\text{DIFF}})$$

Add Independent terms for N bit complete cycle

$$\Delta E_{\text{DAC}} \cong \tfrac{1}{16} 2^N C_u (1+\alpha_p) V_{FS}^{\,2} \left[1 - \frac{1}{3(1+\alpha_T)(1+\alpha_p)} \right]$$

DAC Energy vs SNR

Complete N-bit cycle

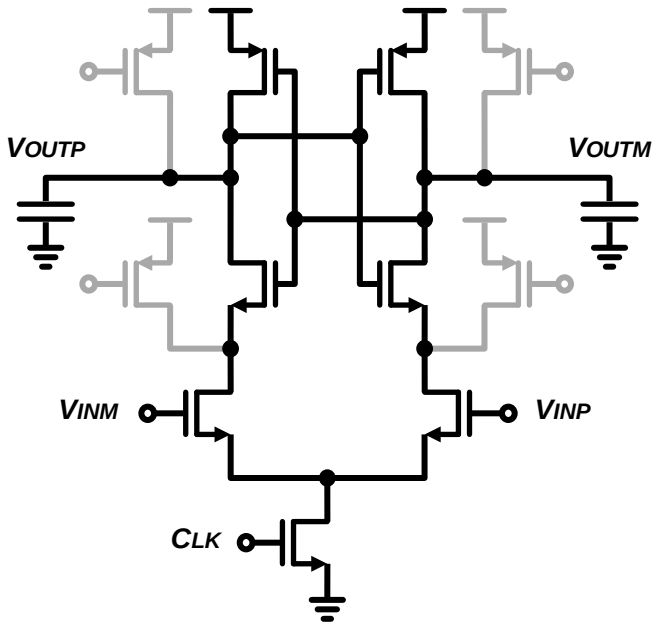
$$\Delta E_{DAC} \cong \frac{1}{16} 2^{N} C_{u} \left(1+\alpha_{p}\right) V_{FS}^{2} \left[1-\frac{1}{3\left(1+\alpha_{T}\right)\left(1+\alpha_{p}\right)}\right]$$

Energy vs SNR

$$\Delta E_{DAC} \cong \frac{kT}{2} \cdot SNR_{DAC} \cdot \left[(1+\alpha_{P})-\frac{1}{3(1+\alpha_{T})}\right]$$

Comparator Energy Consumption

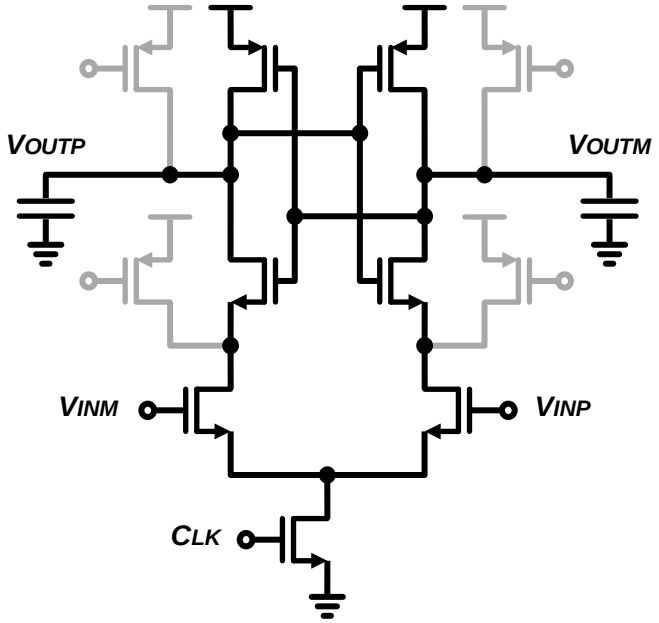
Dynamic Comparator



Latch

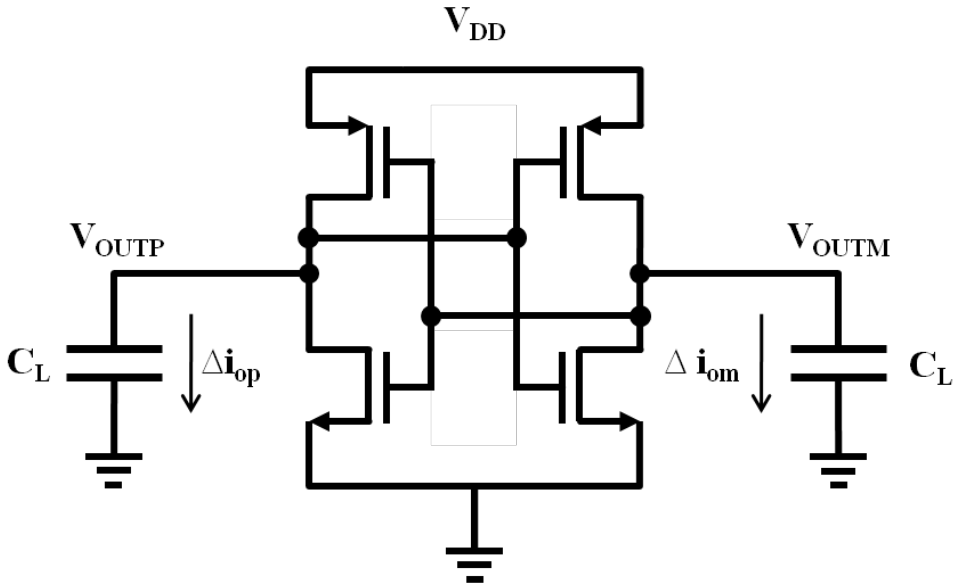
Diff Pair

Reset Energy



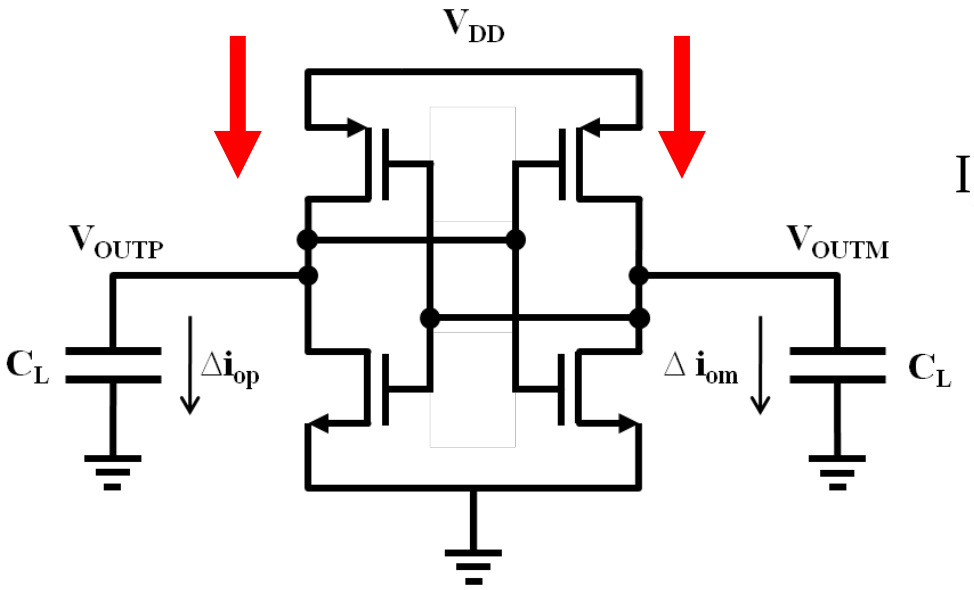
$$\Delta E_{RESET} = C_L V_{DD}^{\ 2}$$

Simplified Model for Amplification



$$\Delta E_{LATCH} \leq I_{DD,MAX} V_{DD} \Delta t$$

Simplified Model for Amplification

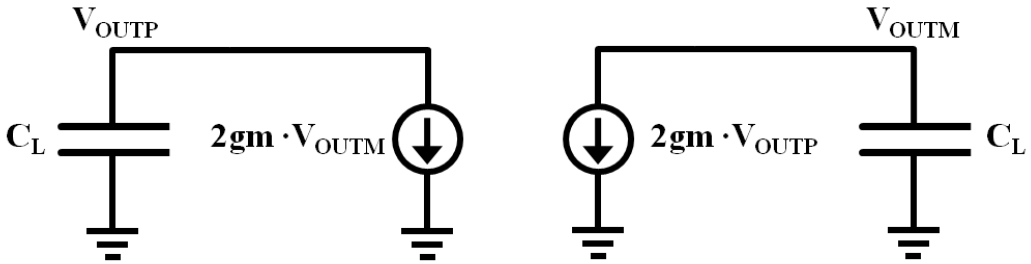


$$I_{DD,MAX} \cong gm\left|V_{GS} - V_{TH}\right| < \tfrac{1}{2} gmV_{DD}$$

$$\Delta E_{LATCH} \le I_{DD,MAX} V_{DD} \Delta t$$

Estimate Time Δt

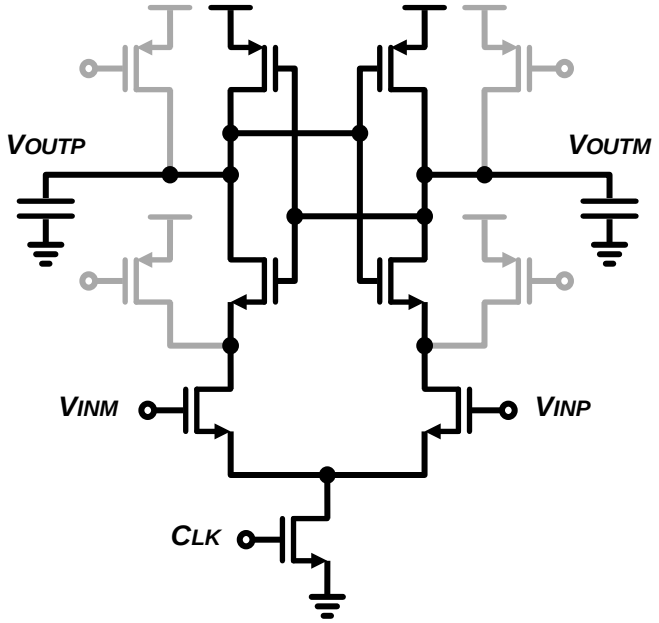
Use small signal model to estimate Δt



$$\Delta t = \frac{C_L}{2gm} \operatorname{arcsinh}\left[\frac{2V_{DD}}{\Delta V_{IN}}\right]$$

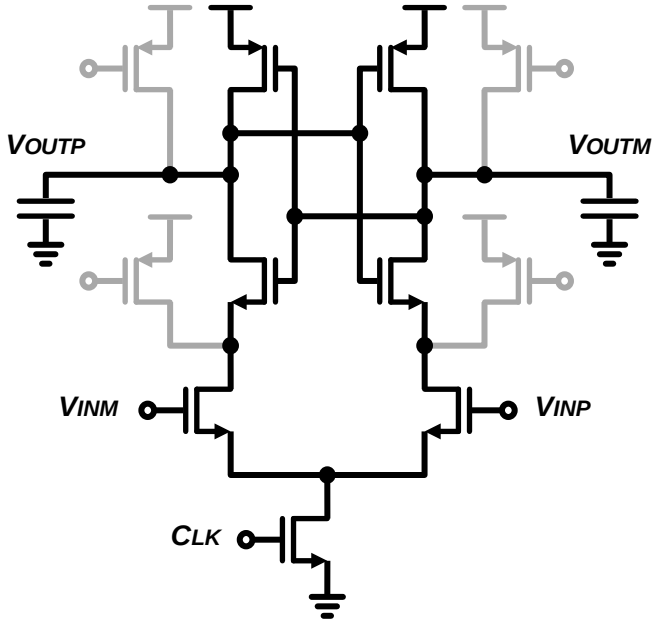
$$\Delta E_{LATCH} \leq I_{DD,MAX} V_{DD} \Delta t$$

Latch Energy



$$\Delta E_{LATCH}(\Delta V_{IN}) = \frac{1}{4} C_L V_{DD}^{\ 2} \operatorname{arcsinh}\left[\frac{2V_{DD}}{\Delta V_{IN}}\right]$$

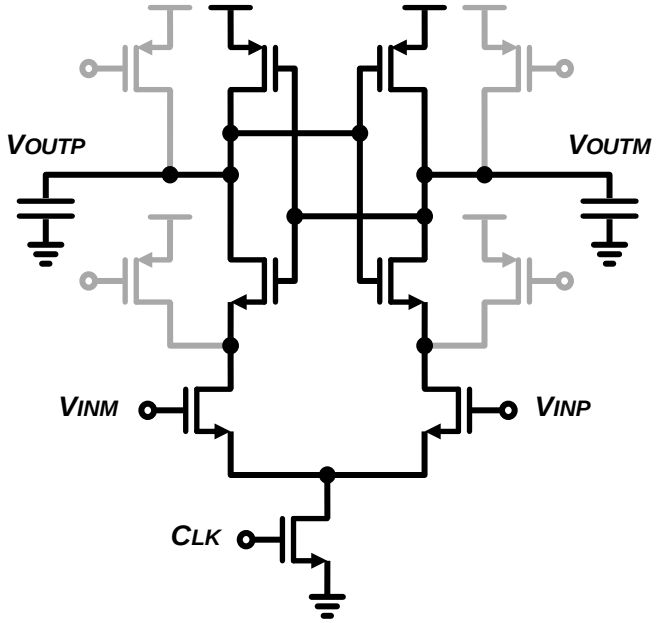
Latch Energy



$$\Delta E_{LATCH}(\Delta V_{IN}) = \frac{1}{4} C_L V_{DD}^{\ 2} \operatorname{arcsinh}\left[\frac{2V_{DD}}{\Delta V_{IN}}\right]$$

ΔV_{IN} ranges from 0 to VDD/2^m

Total Energy for N Cycle SAR



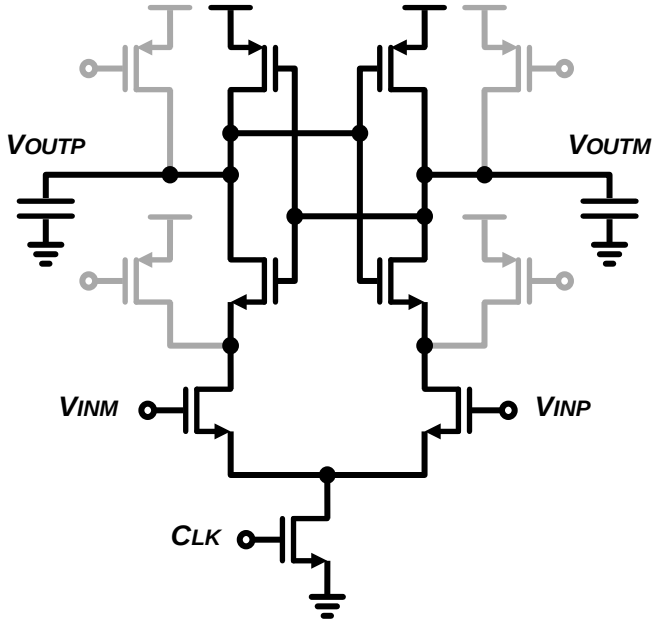
$$\Delta E_{COMP} = \Gamma_N \cdot C_L V_{DD}^{\ 2}$$

$$\Gamma_N = N + \frac{1}{2}\sum_{m=0}^{N-1} 2^m \int_0^{2^{-m}} \operatorname{arcsinh}\frac{2}{u}\,du$$

Reset

Amplification

Total Energy for N Cycle SAR



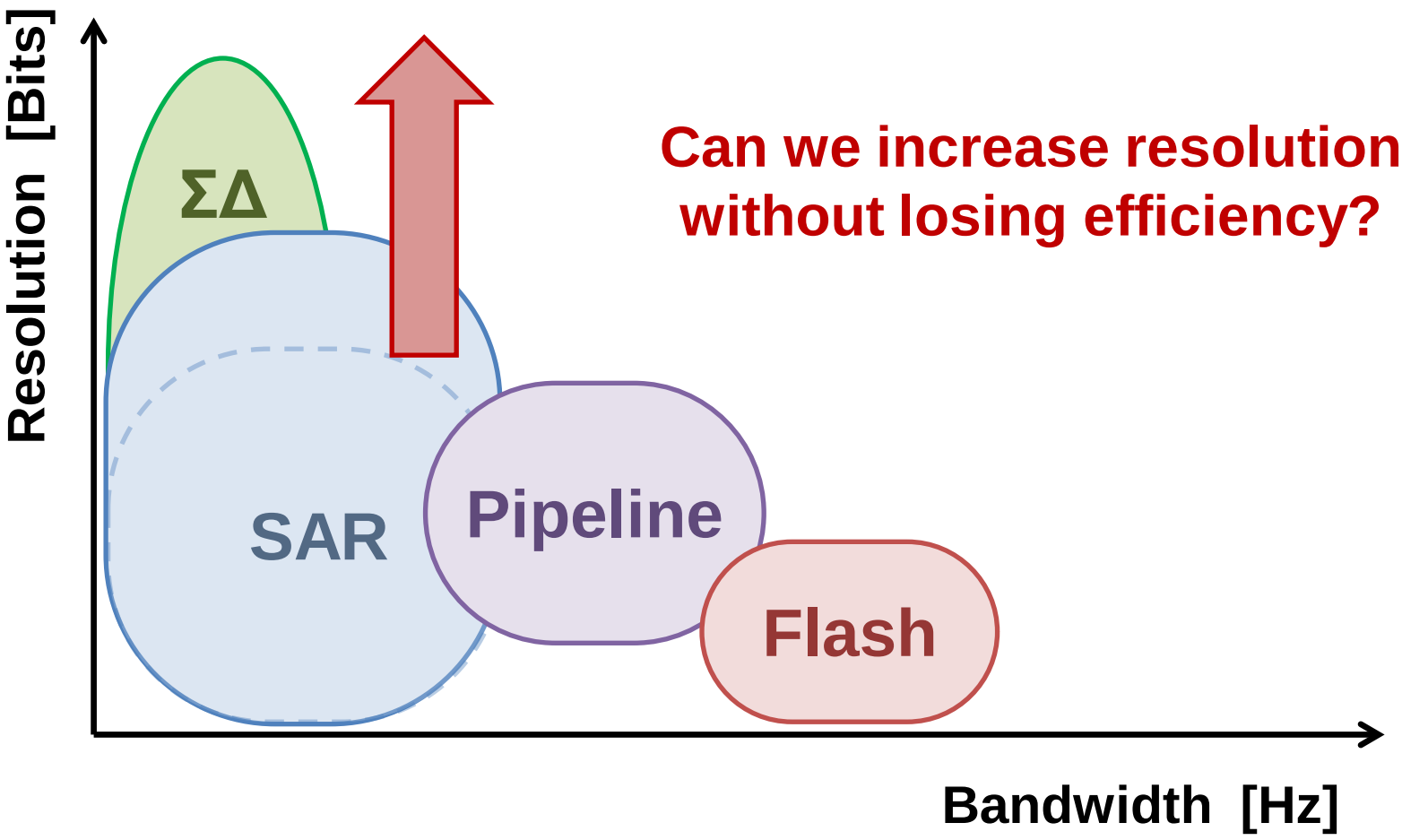
$$\Delta E_{COMP} \cong \frac{2kT}{23}\left[\frac{2^N}{\sigma_{COMP}}\right]^2\left[N^2+12N+2\right]$$

$$\Delta E_{COMP} \cong \frac{2kT}{3}\cdot SNR_{COMP}\cdot\ [N^2+12N+2]$$

Overview

- Review of Tends
- Fundamentals
- Emerging Approaches

Increase Resolution of SAR



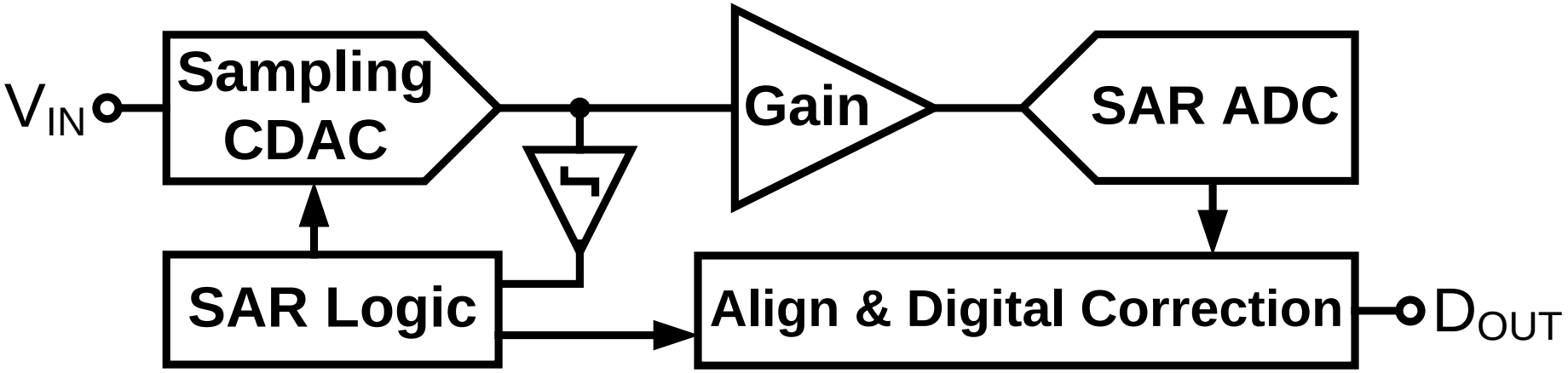
Can we increase resolution without losing efficiency?

Challenges

- Capacitor Matching
- DAC Energy consumption
- DAC speed
- Comparator Energy
  - i.e. Comparator Noise

Reduce Comparator Energy

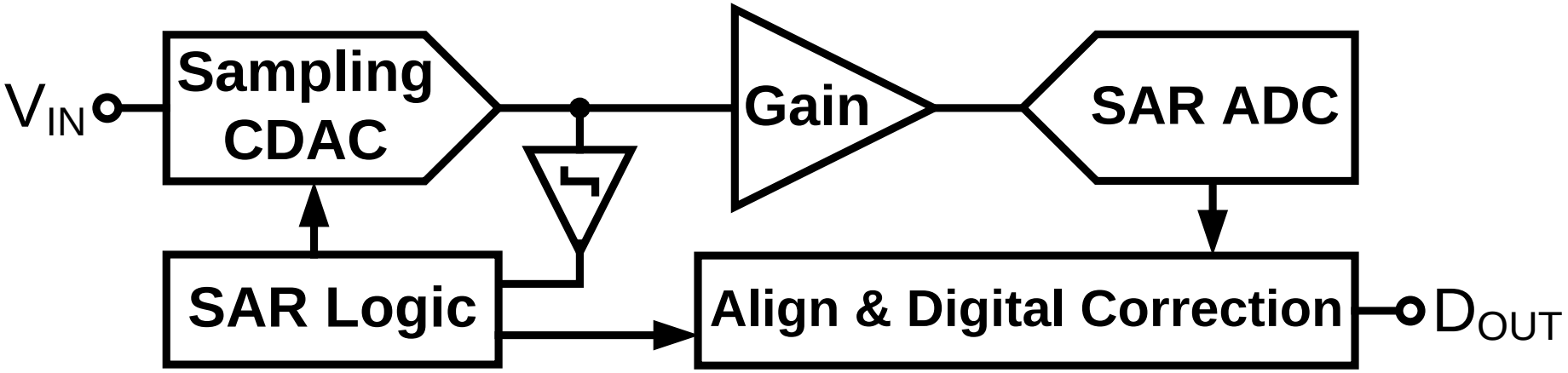
SAR-Assisted Two-Stage Pipeline ADC



- **Energy efficient hybrid for high resolution**

[C.C. Lee, M.P. Flynn *VLSI* 2010]

Benefits vs SAR

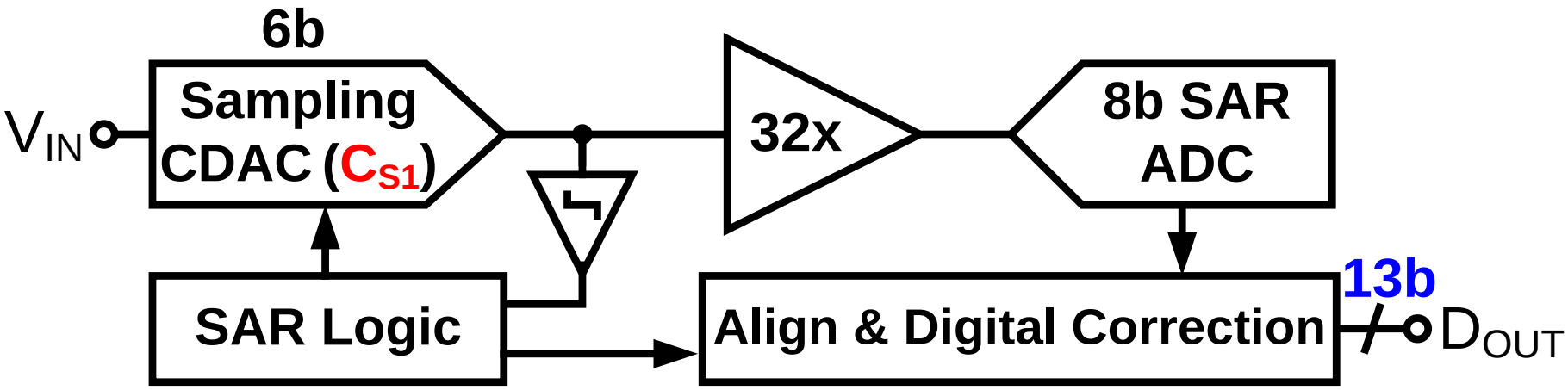


- Low resolution SAR → comparator power ↓
- Pipelining → speed ↑
- Large first stage resolution → linearity ↑

[C.C. Lee, M.P. Flynn *VLSI* 2010]

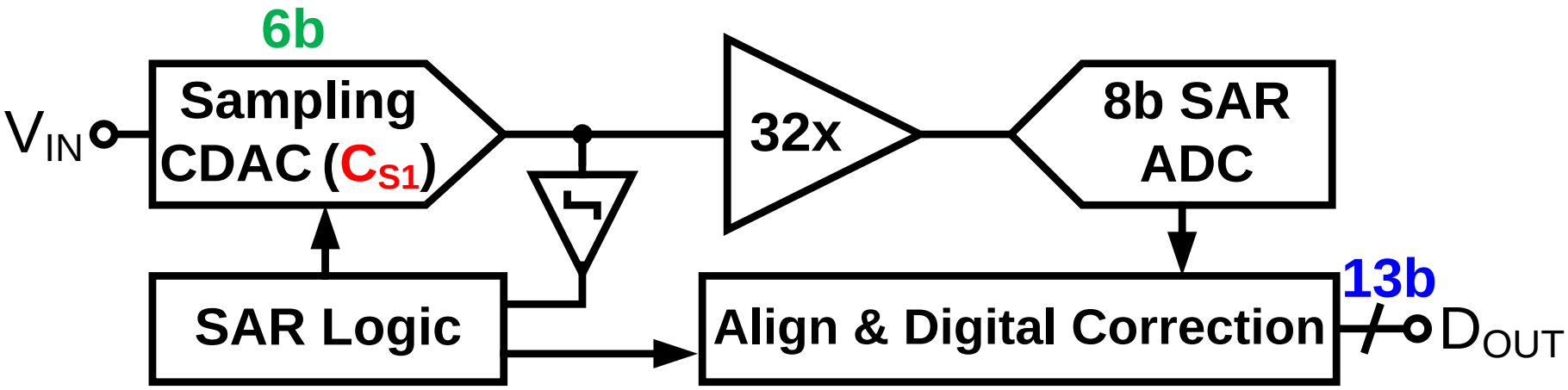
Reduce DAC Switching by splitting DAC

First DAC Noise Requirement



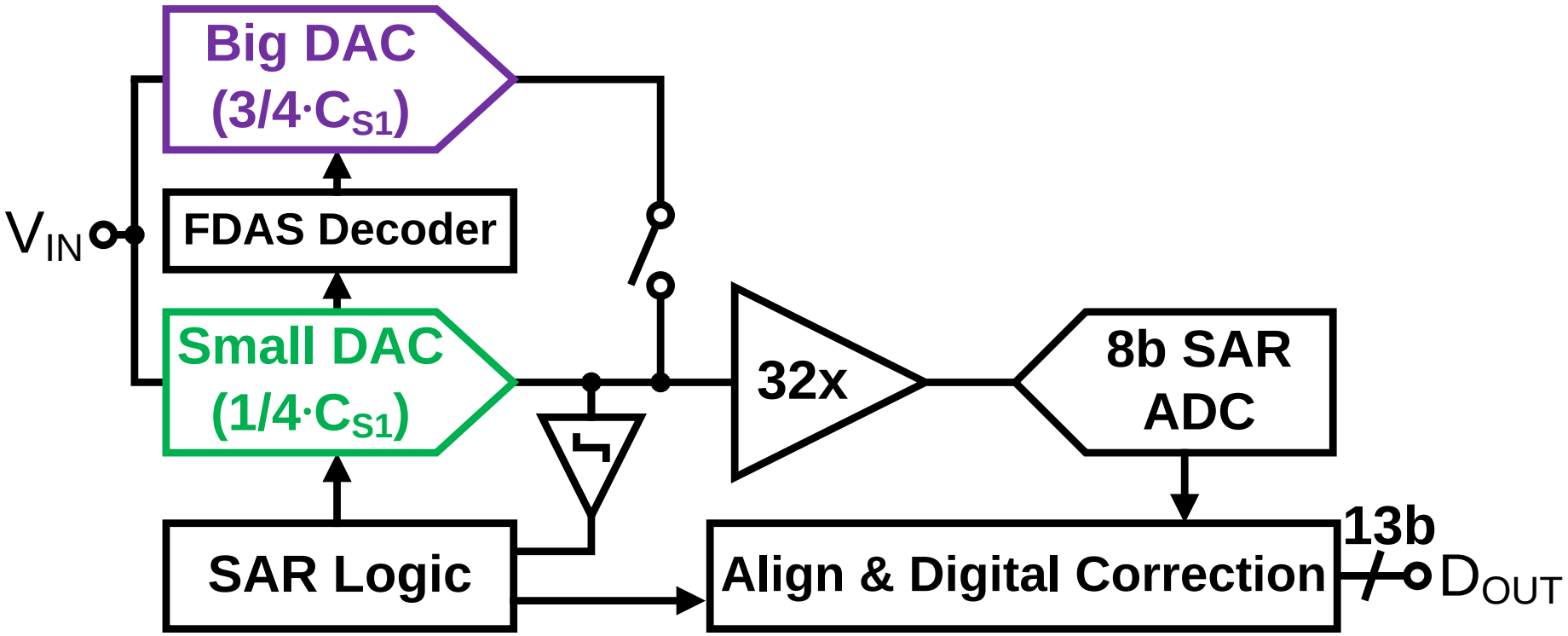
- DAC residue: 13b kT/C (C_{S1}=2pF)

First DAC Noise Requirement



- DAC residue: 13b kT/C (C_{S1}=2pF)
- 1st stage ADC: 6b kT/C noise

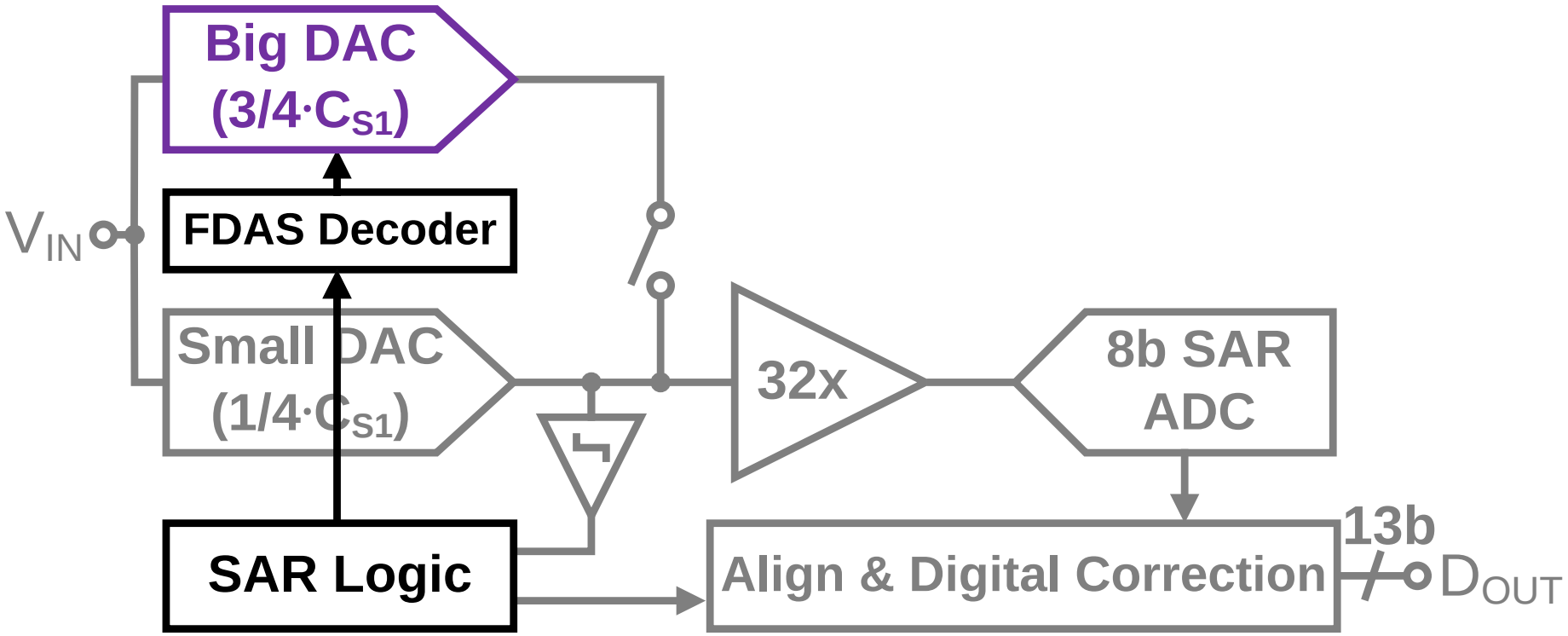
Divided First Stage DAC



- Reduce DAC switching energy & mismatch

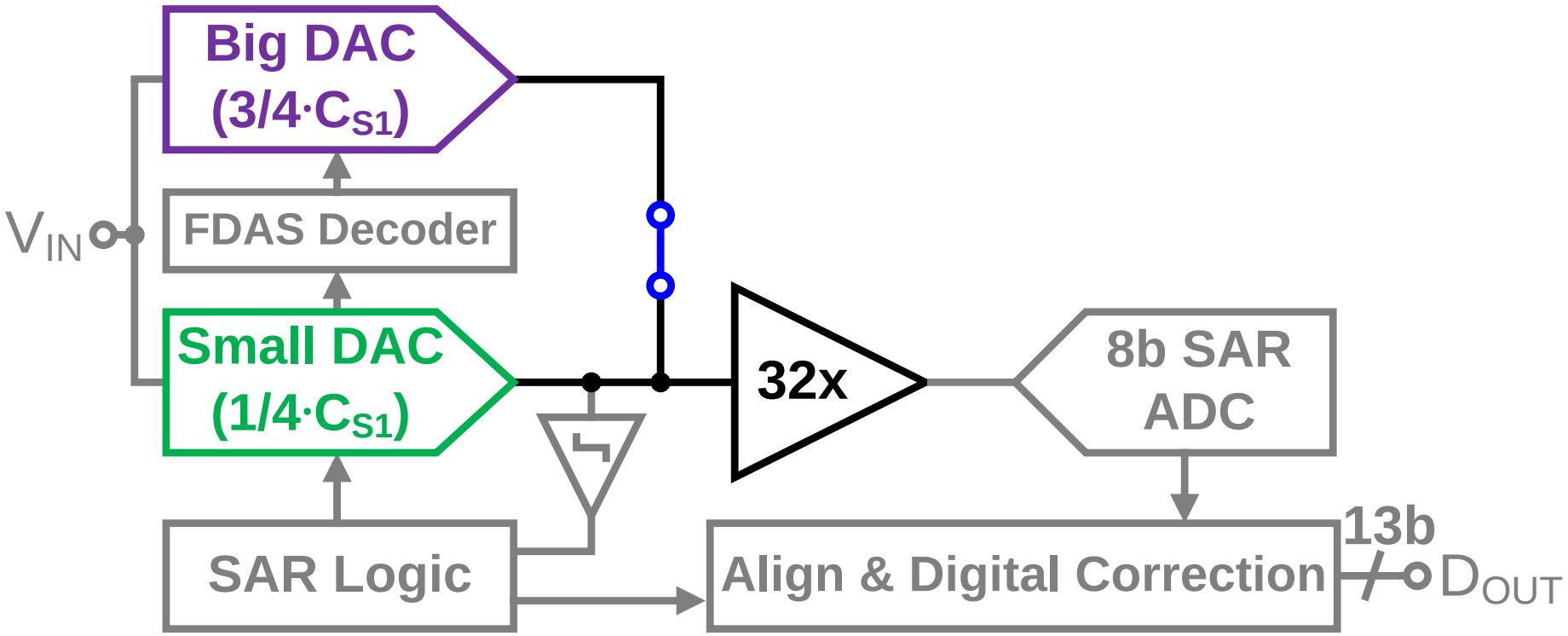
[Y. Lee, M.P. Flynn ISSCC 2015]

Big DAC Residue Generation (FDAS)



- **Floated Detect-and-Skip (FDAS)**
  - Energy efficient switching using small DAC SAR ADC result

Merge Big & Small DAC Residues

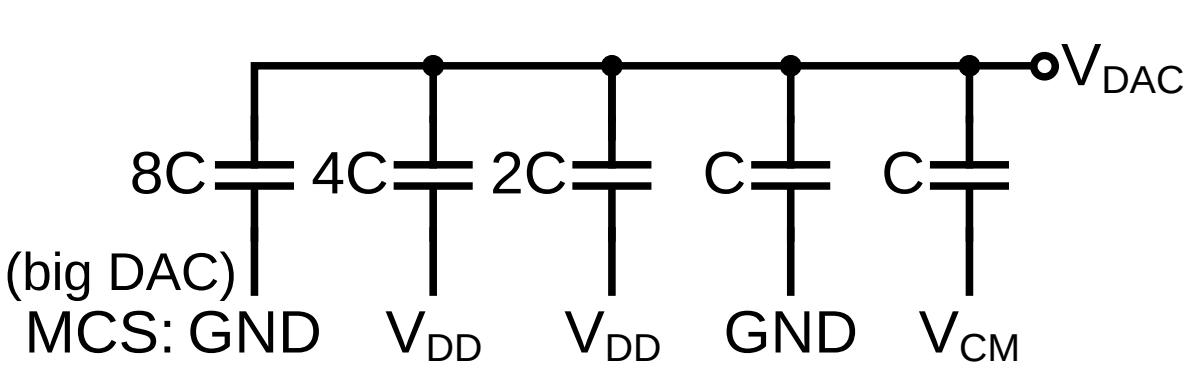


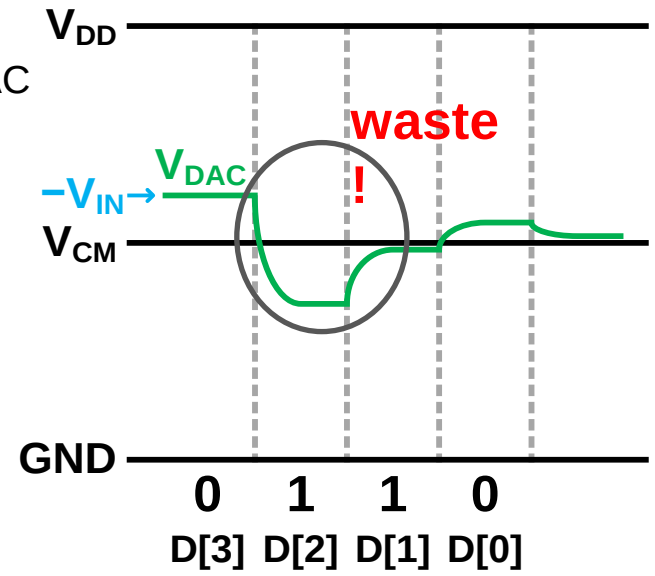
- **Meets 13b kT/C noise requirement**
- **Mismatch between big and small DACs**
  - Corrected by 1b stage redundancy

Floated Detect-and-Skip DAC Switching

Switching Energy Reduction

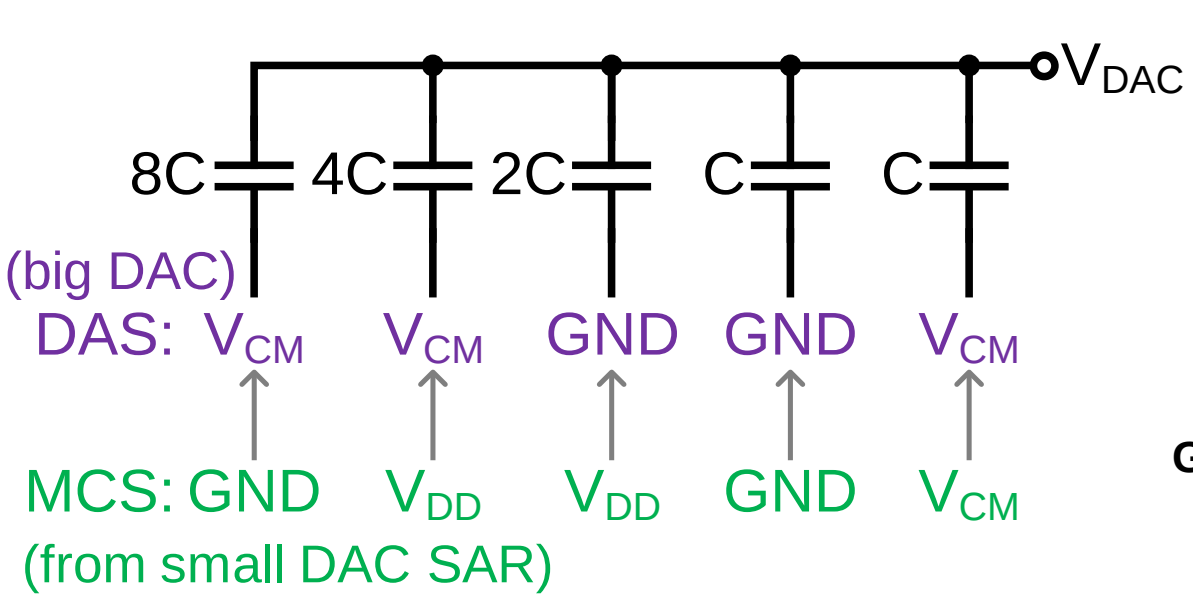
Big DAC Switching Energy Loss

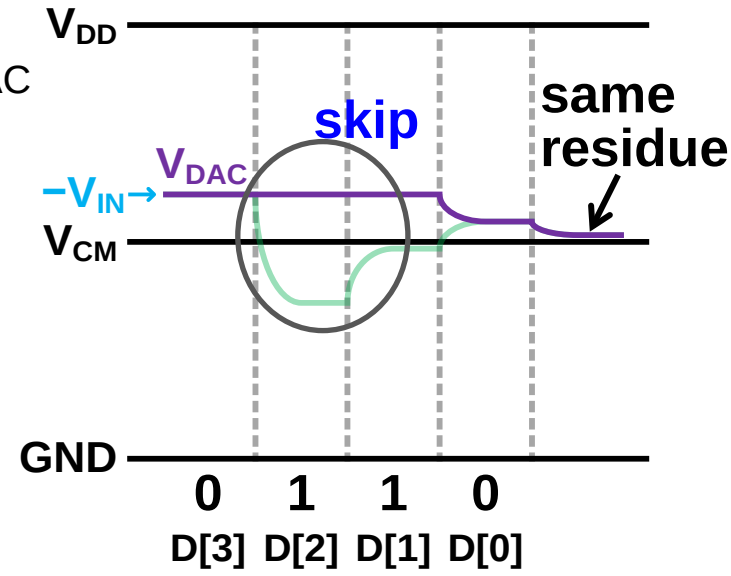




- **Binary search**
  - Opposite direction switching → **waste!**

Detect-and-Skip (DAS) Switching



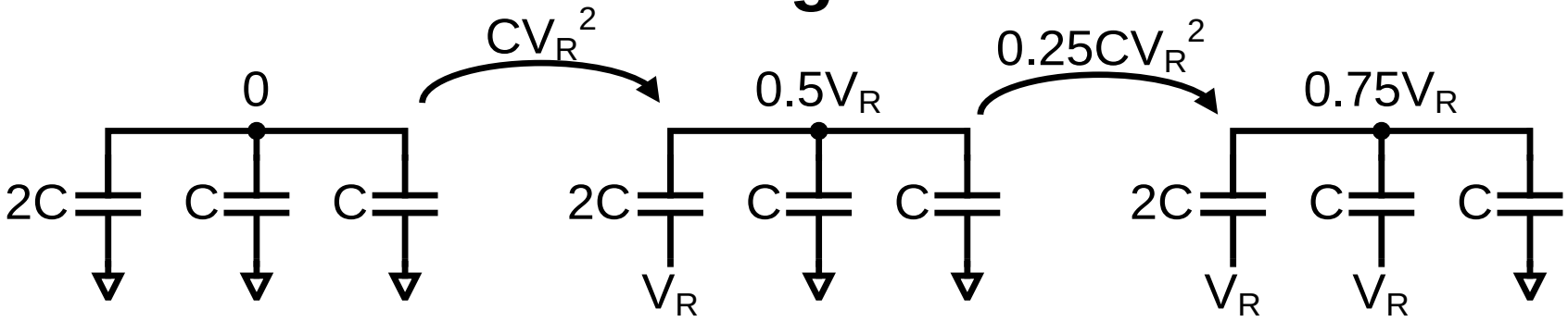


- **Skips opposite direction switching**
  - ☺ Saves energy

[H-Y Tai *ISSCC* 2014]

Big DAC Switching Energy Loss (2)

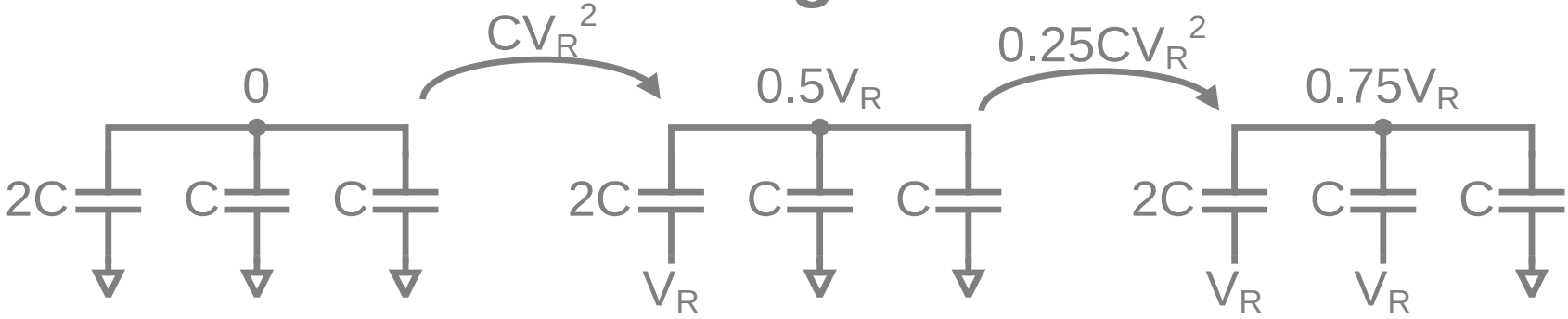
- **Successive switching**



Total energy: $CV_R^2 + 0.25CV_R^2 = 1.25CV_R^2$

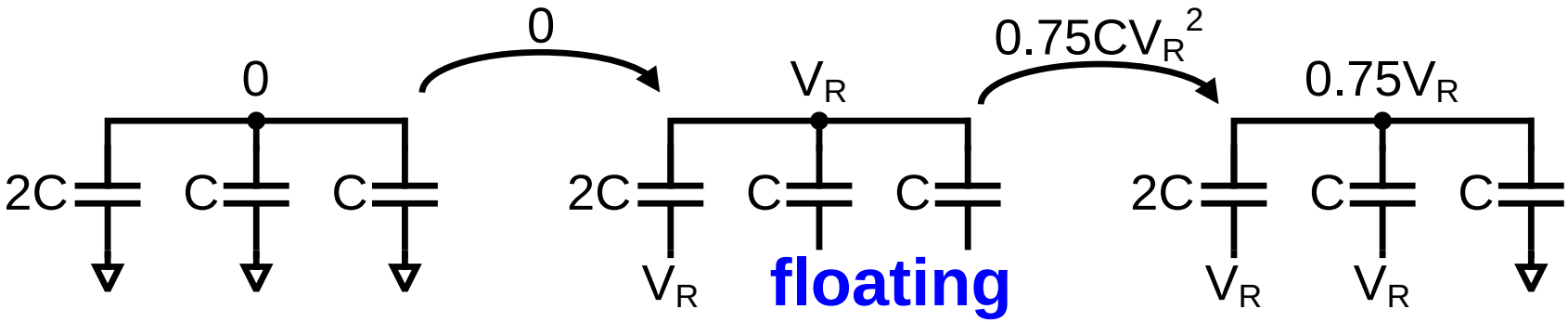
Big DAC Floated DAS Switching

- **Successive switching**



Total energy: $CV_R^2 + 0.25CV_R^2 = \mathbf{1.25CV_R^2}$

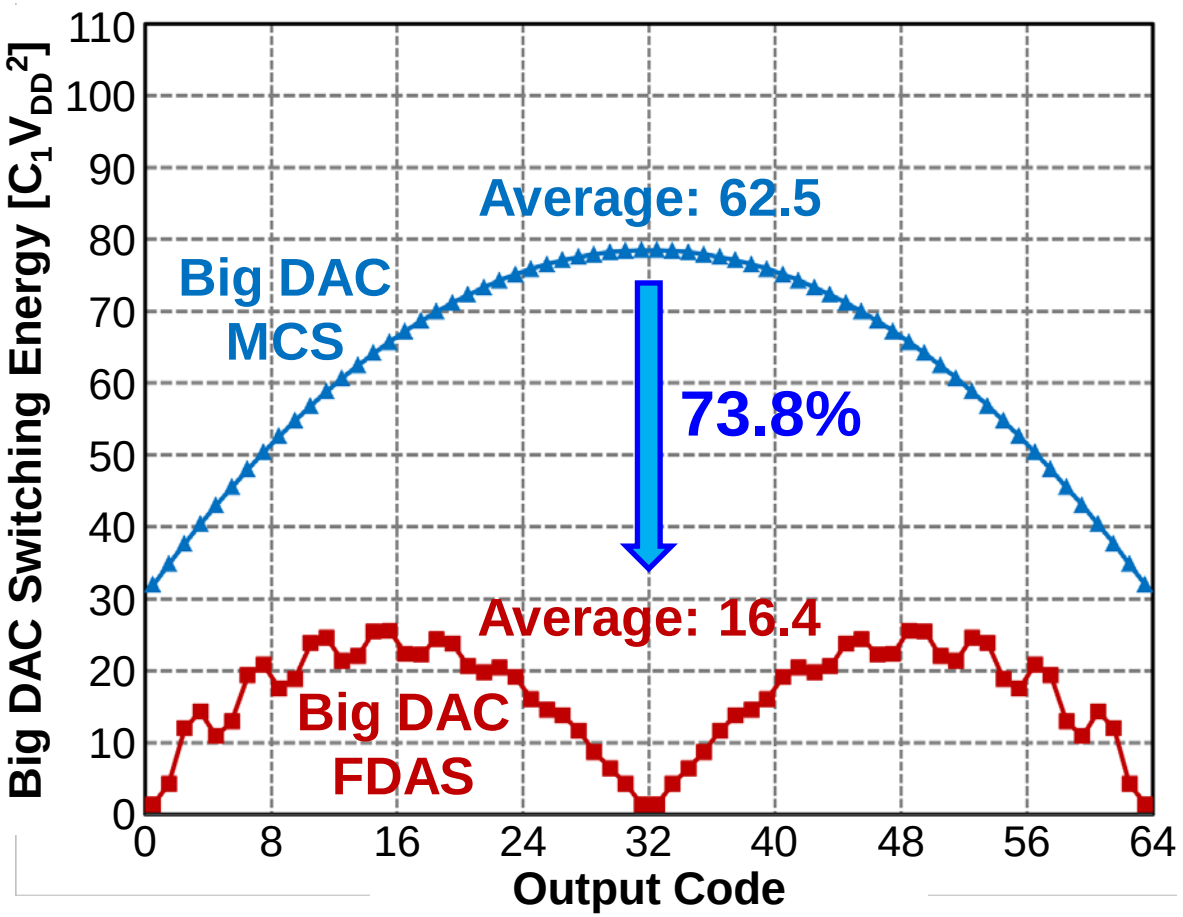
- **Floated DAS switching**



Total energy: $0.75CV_R^2$

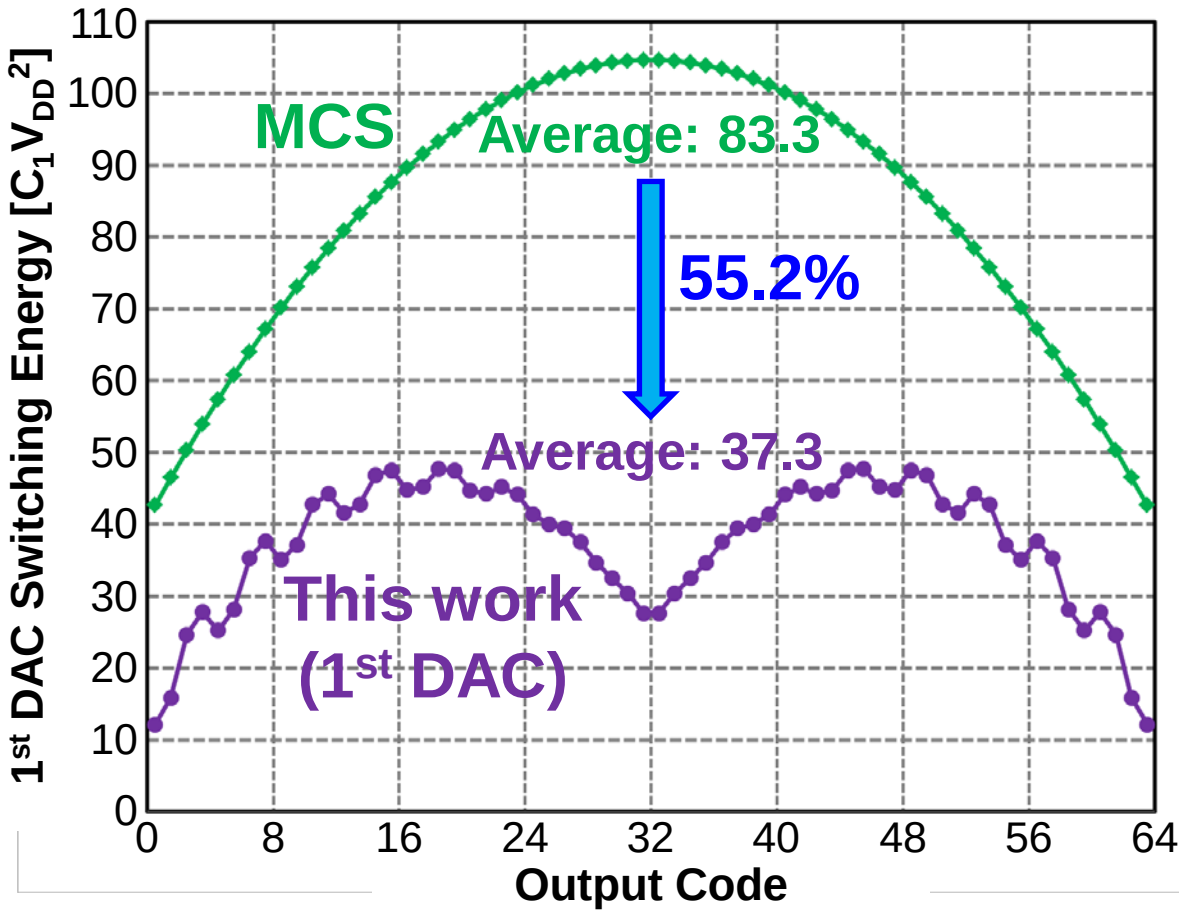
☺ **Save energy without additional settling time**

Big DAC Switching Energy Comparison



- Big DAC MCS vs. big DAC FDAS

1st DAC Switching Energy Comparison



- MCS vs. small DAC MCS + big DAC FDAS

Floated Detect-and-Skip DAC Switching

DAC Mismatch Reduction

MCS Worst Case INL

- **MCS**

[GND, V_{DD}, V_{DD} , V_{DD} , V_{DD} , V_{DD} , V_{CM}]

Worst case switching

[V_{MSB}, GND, GND, GND, GND, GND, V_{LSB}, V_{Dummy}]

MCS & FDAS Worst Case INL

- **MCS**

[GND,V_{DD}, V_{DD} , V_{DD} , V_{DD} , V_{DD} ,V_{CM}]

↕

[V_{DD},GND,GND,GND,GND,GND,V_{CM}]

- **FDAS**

[GND,V_{CM}, V_{CM} , V_{CM} , V_{CM} , V_{CM} ,V_{CM}]

↕

[V_{CM},GND,GND,GND,GND,GND,V_{CM}]

MCS & FDAS Worst Case INL

➤ MCS

[GND,V_{DD}, V_{DD} , V_{DD} , V_{DD} , V_{DD} ,V_{CM}]

↕

[V_{DD},GND,GND,GND,GND,GND,V_{CM}]

➤ FDAS

[GND,V_{CM}, V_{CM} , V_{CM} , V_{CM} , V_{CM} ,V_{CM}]

↕

[V_{CM},GND,GND,GND,GND,GND,V_{CM}]

also

↕

[V_{DD}, V_{CM}, V_{CM}, V_{CM}, V_{CM}, V_{CM}, V_{CM}]

[V_{CM}, V_{DD}, V_{DD}, V_{DD}, V_{DD}, V_{DD}, V_{CM}]

Worst Case INL Improvement

- **MCS**

  [GND, V_{DD}, V_{DD}, V_{DD}, V_{DD}, V_{DD}, V_{CM}]

  ↕

  [V_{DD}, GND, GND, GND, GND, GND, V_{CM}]

- **FDAS**

  [GND, V_{CM}, V_{CM}, V_{CM}, V_{CM}, V_{CM}, V_{CM}]

  ↕

  [V_{CM}, GND, GND, GND, GND, GND, V_{CM}]

  also

  ↕

  [V_{DD}, V_{CM}, V_{CM}, V_{CM}, V_{CM}, V_{CM}, V_{CM}]

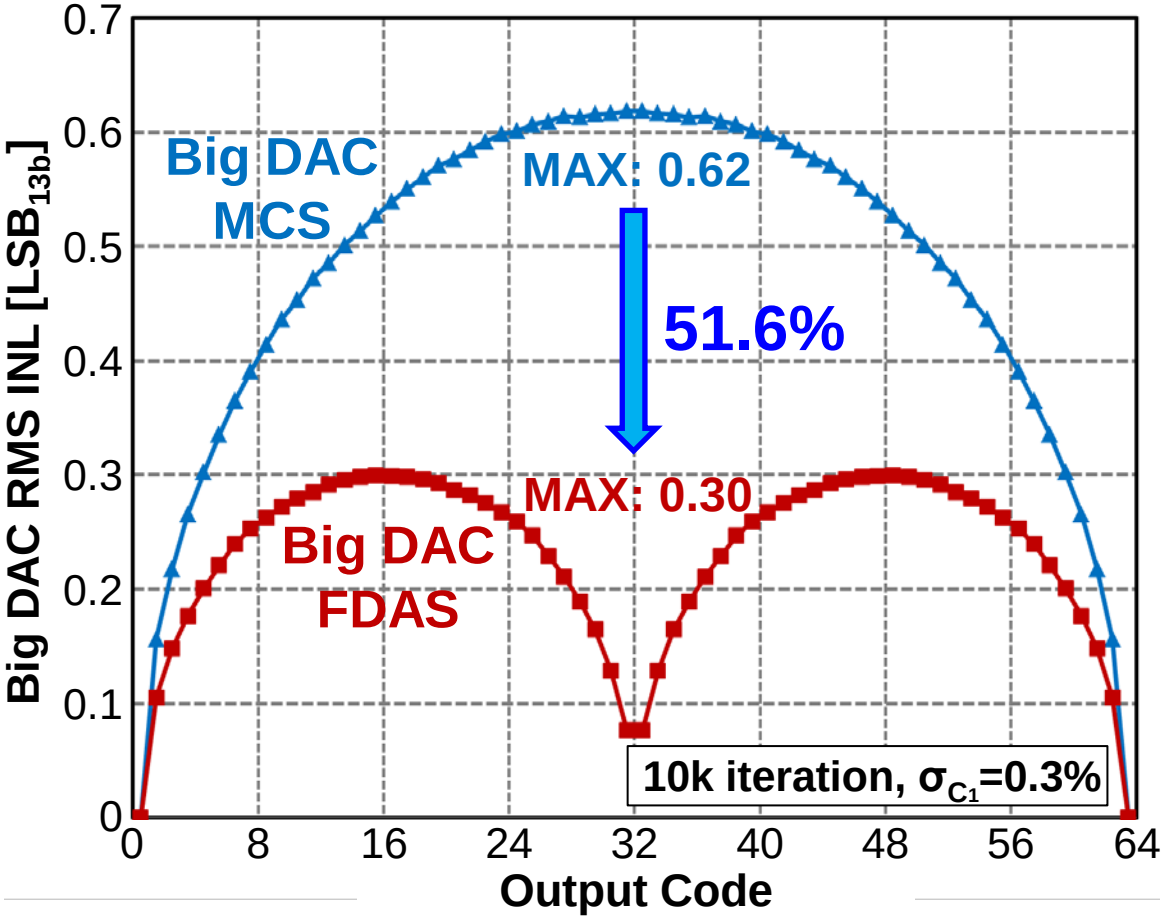
- **Voltage swing halved ($V_{DD} \rightarrow 1/2 \cdot V_{DD} (= V_{CM})$)**

  [V_{CM}, V_{DD}, V_{DD}, V_{DD}, V_{DD}, V_{DD}, V_{CM}]

  ☺ Worst case INL halved

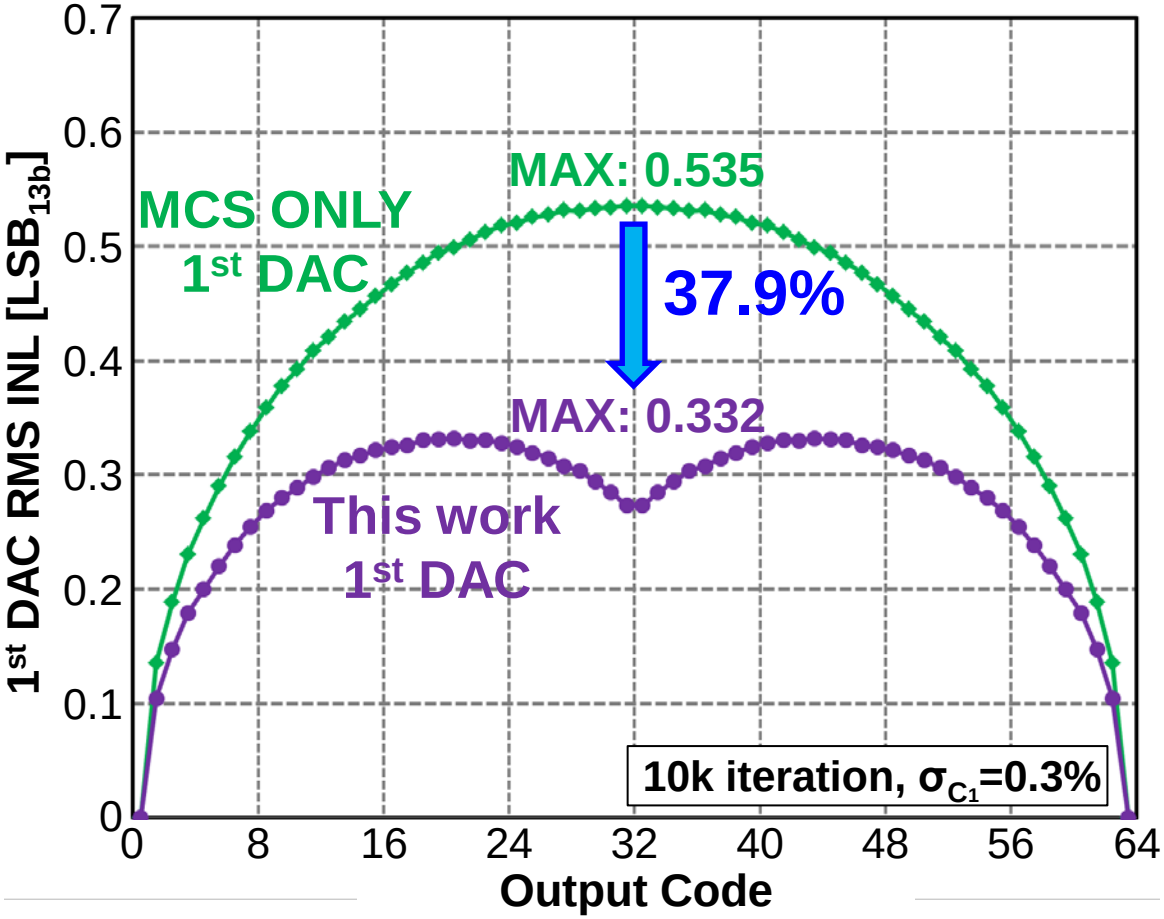
Similar work: [J. Guerber *ISCAS* 2012]

Simulated RMS INL Comparison



- Big DAC MCS vs. big DAC FDAS

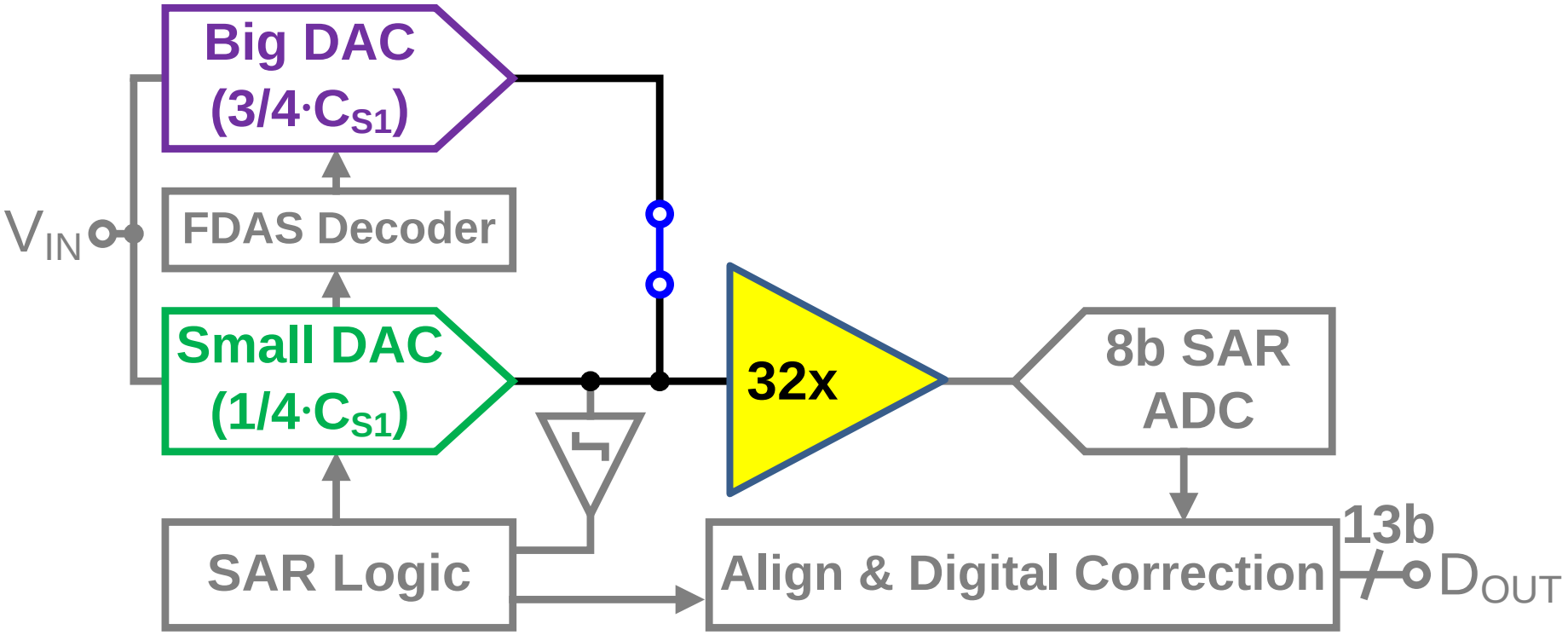
Simulated RMS INL Comparison



- MCS 1st DAC vs. new1st DAC

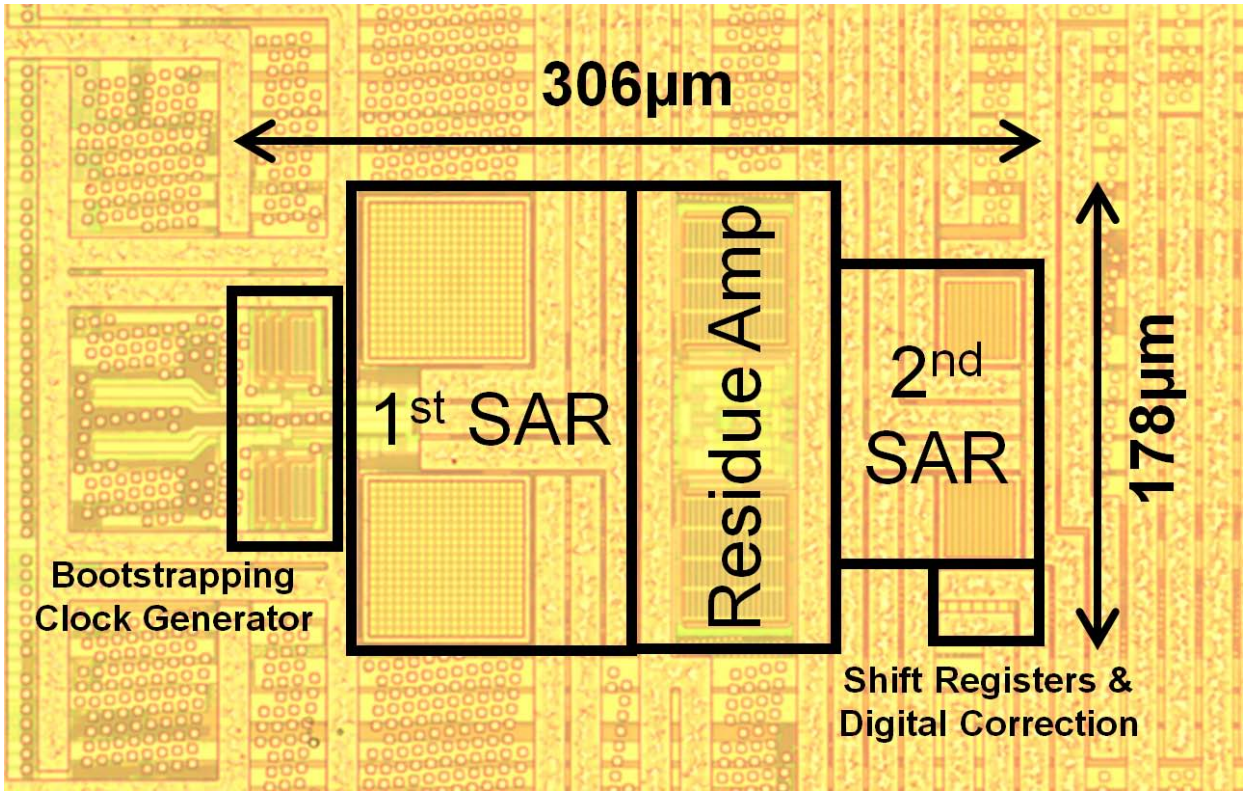
Prototype
SAR Assisted Pipeline

Ring Amp



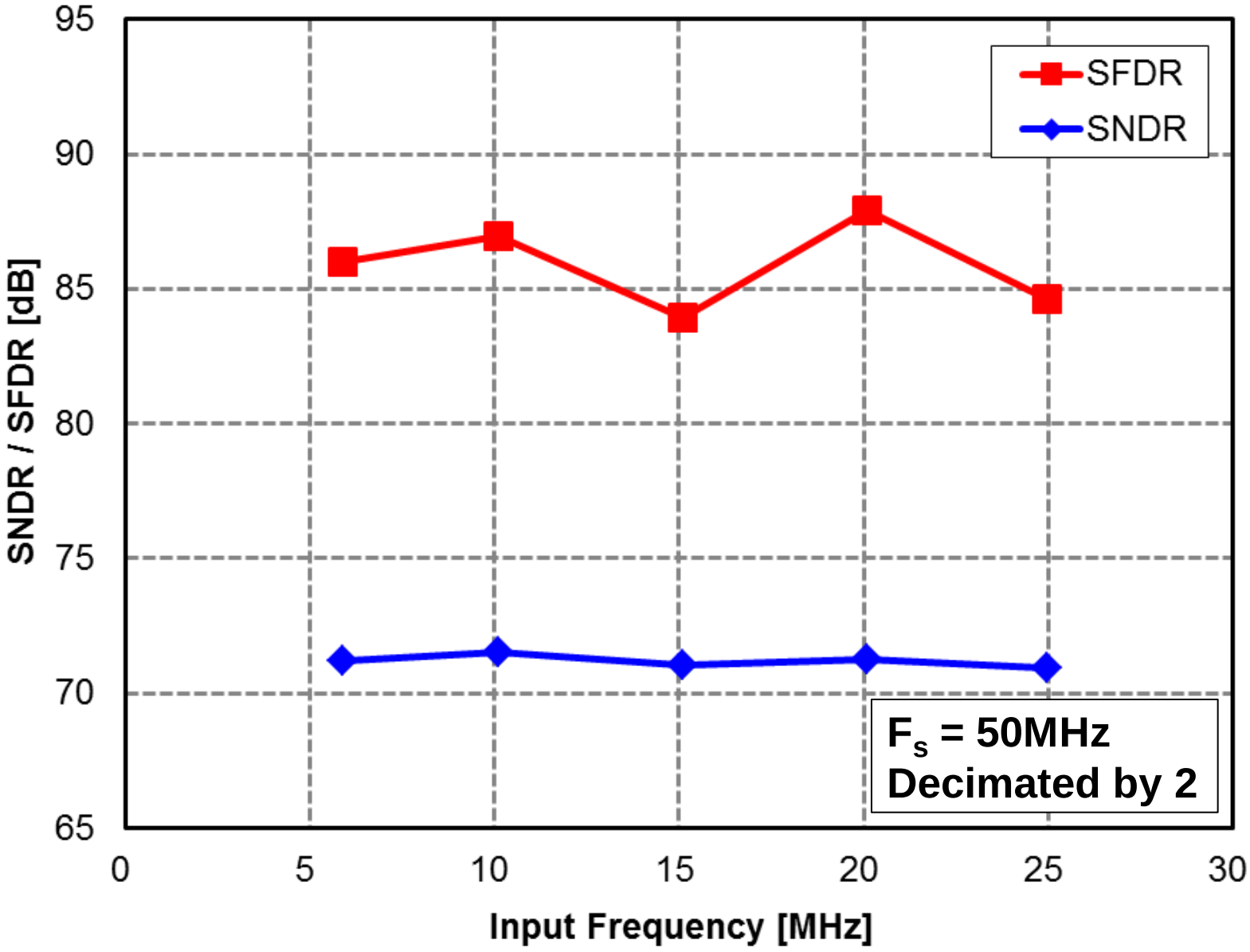
[Y. Lee, M.P. Flynn ISSCC 2015]

ADC Die Photo

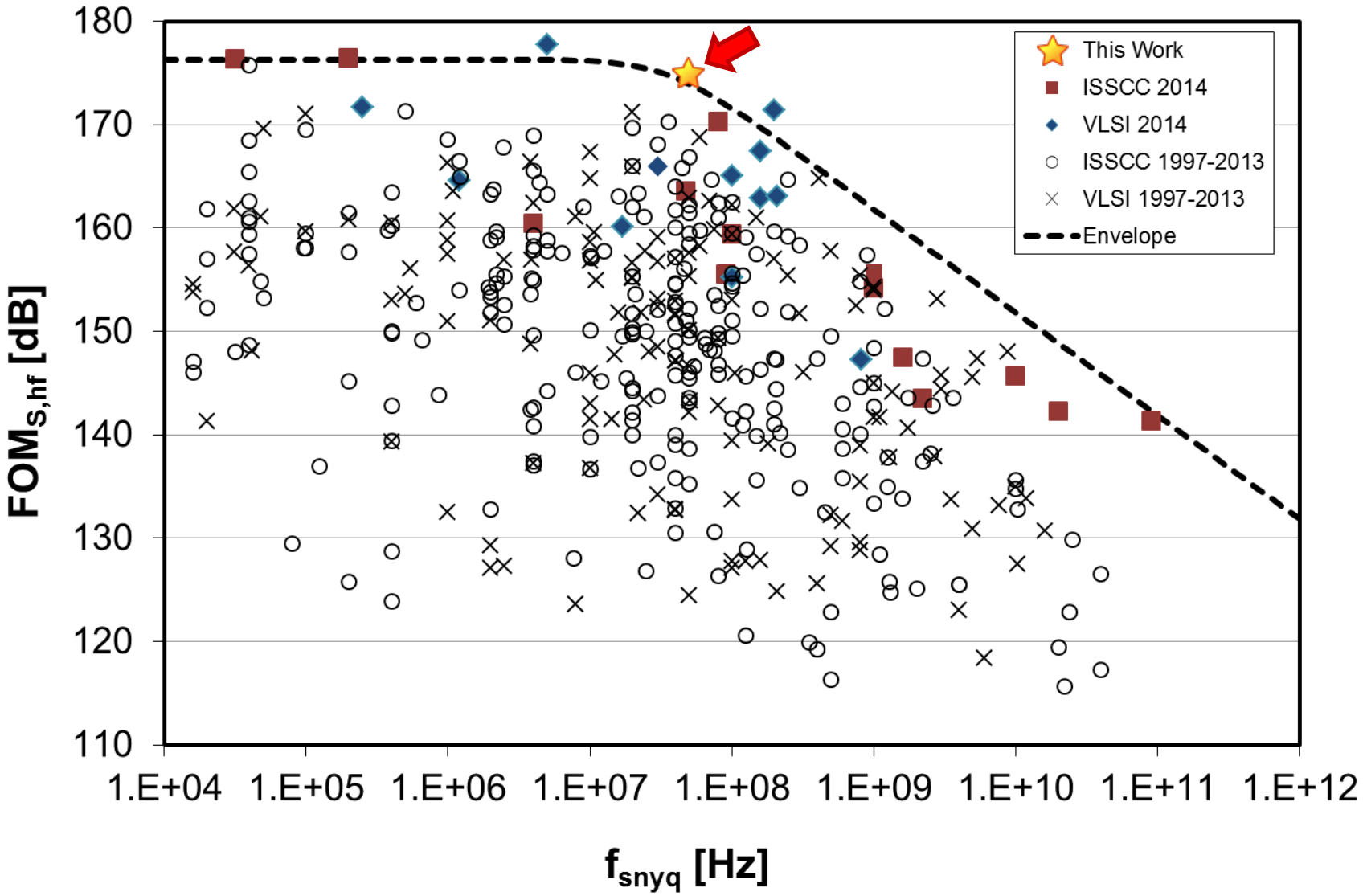


- **50MS/s, 11.5b ENOB, 1mW**
  - 65nm CMOS: 0.054mm^2

Dynamic Performance



FoM_S Comparison

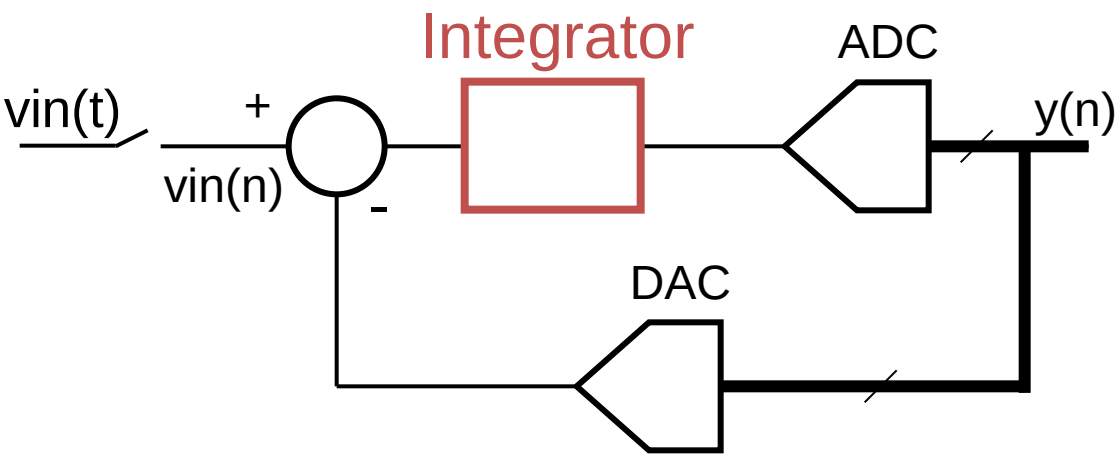


[B. Murmann, ADC Performance Survey 1997-2014]

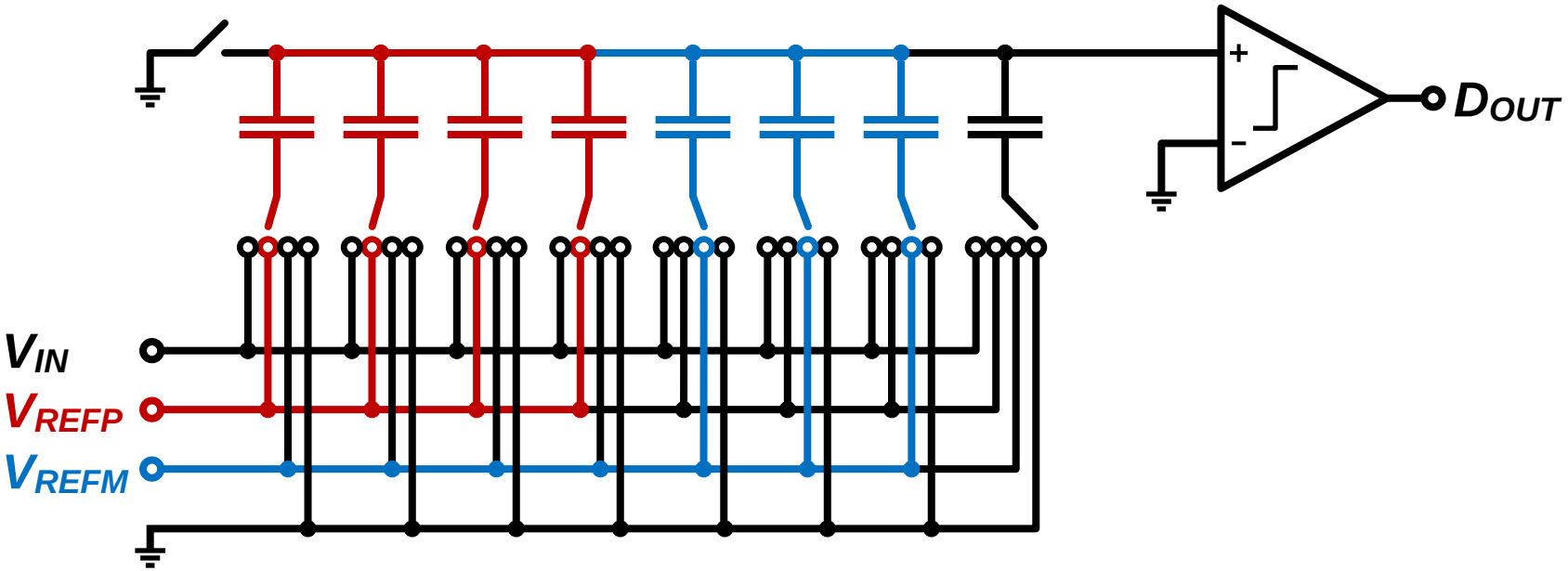
Noise-Shaping SAR ADC

[Fredenburg and Flynn ISSCC 2012, JSSC 12]

1st Order ΣΔ Modulator

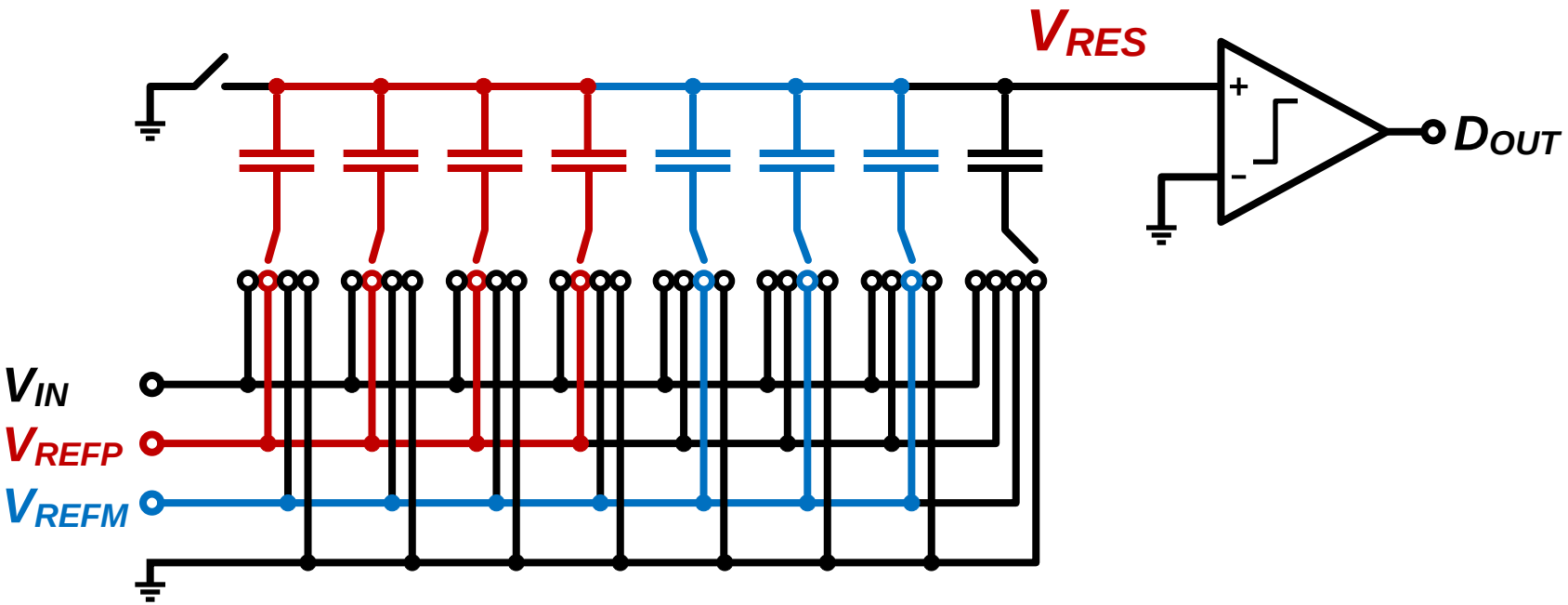


Digital Conversion



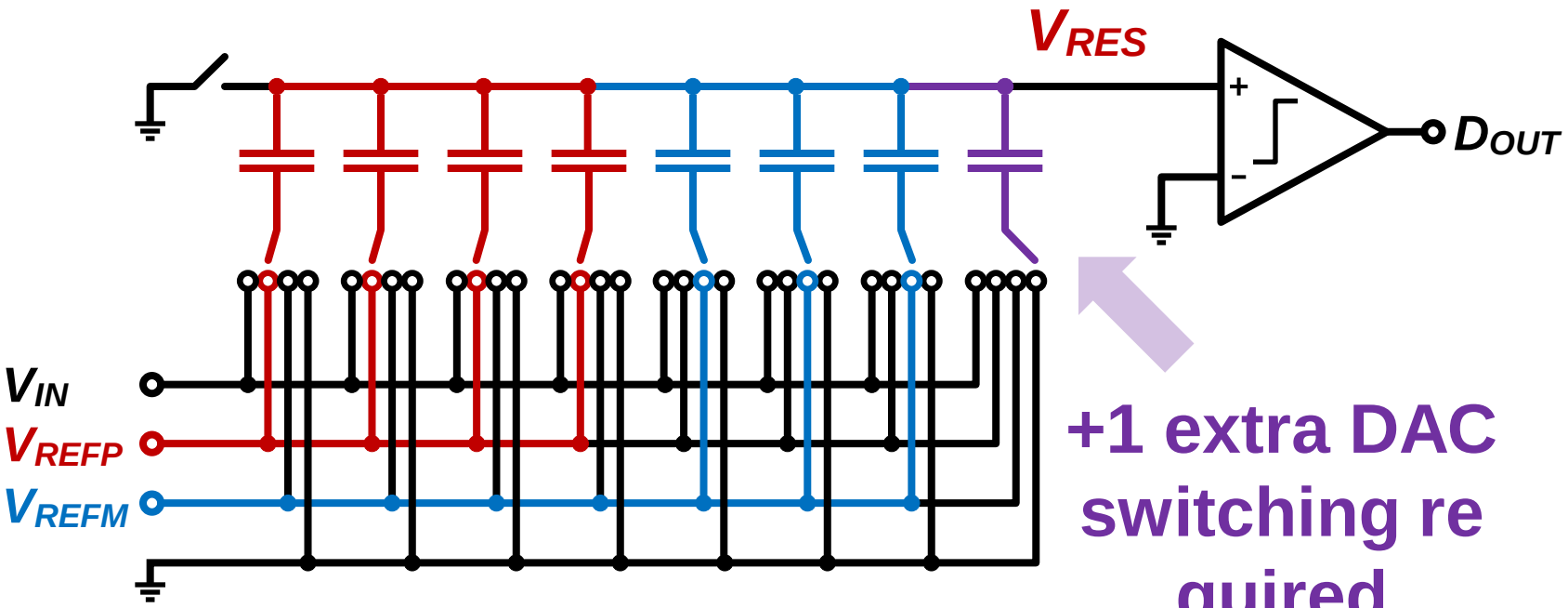
$$D_{OUT} = V_{IN} + Q$$

Conventional DAC Residue



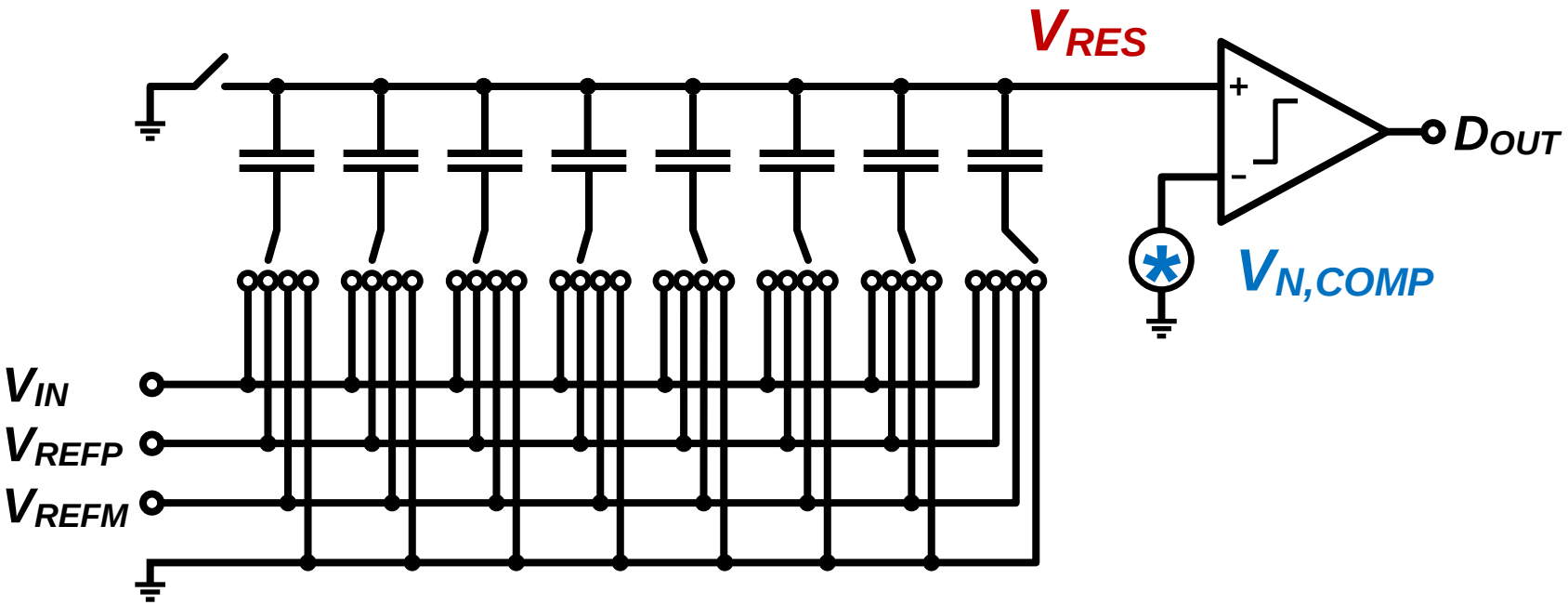
$$V_{RES} \neq D_{OUT} - V_{IN}$$

Extended DAC Residue



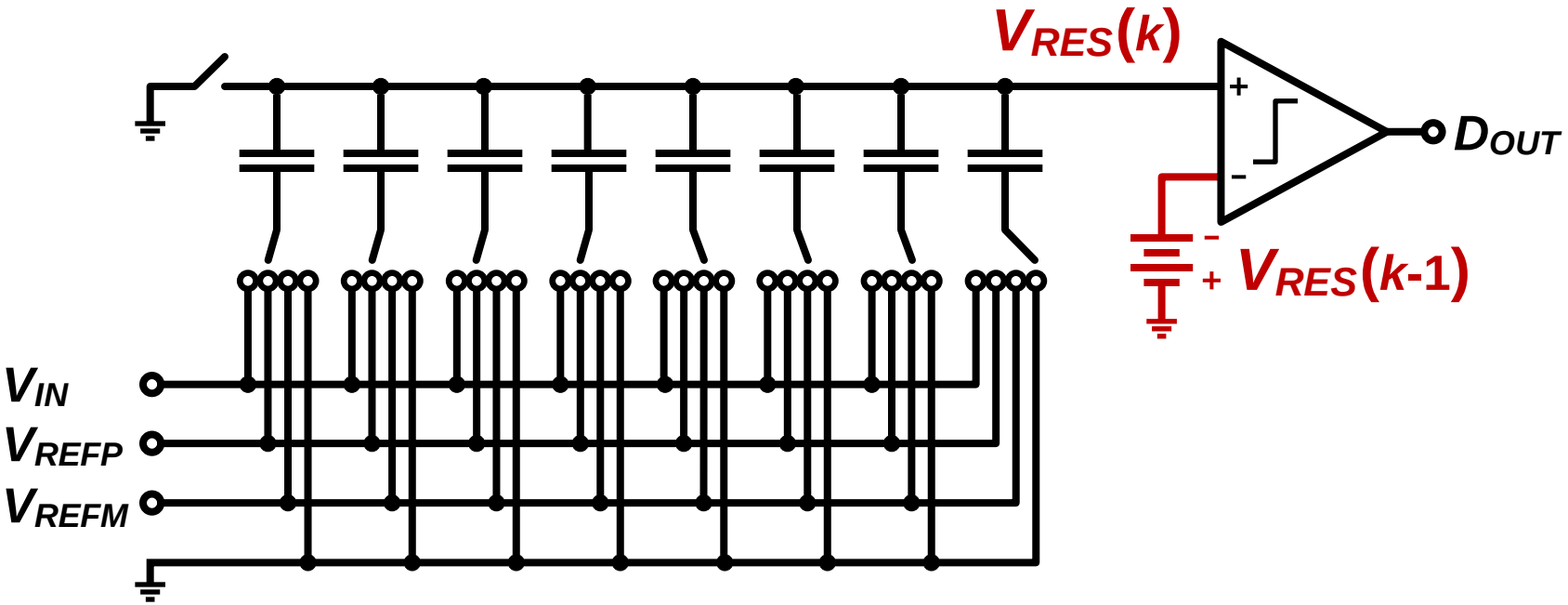
$$V_{RES} = D_{OUT} - V_{IN}$$

DAC Residue



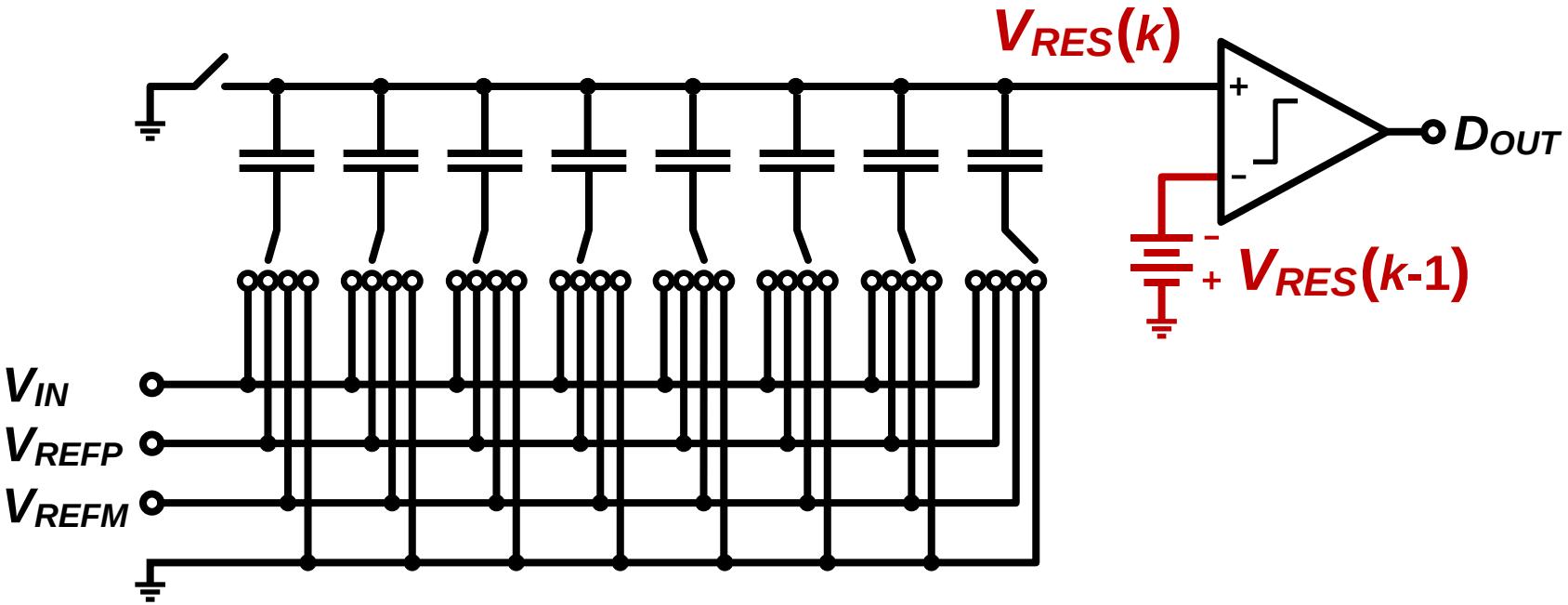
$$V_{RES} = D_{OUT} - V_{IN} + V_{N,COMP}$$

Simple SAR Noise Shaping



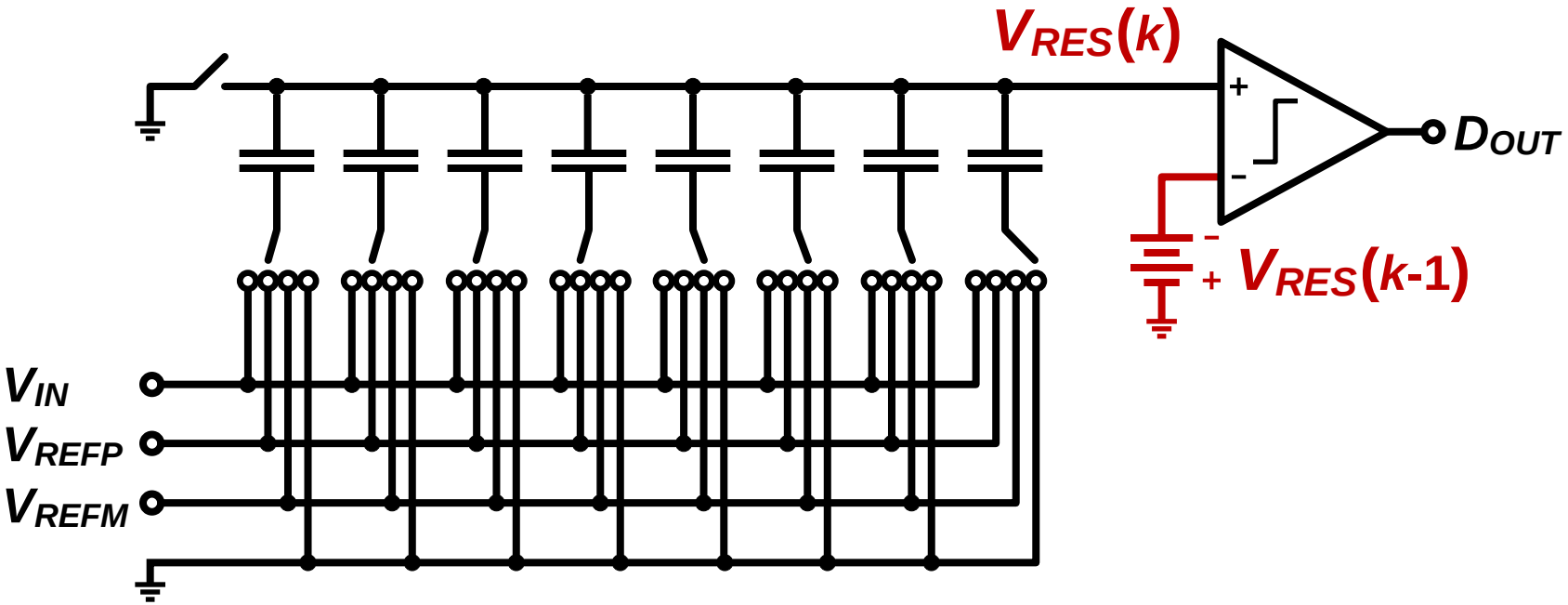
$$D_{OUT}(k) = V_{IN}(k) + Q(k) - V_{RES}(k\text{-}1)$$

Simple SAR Noise Shaping



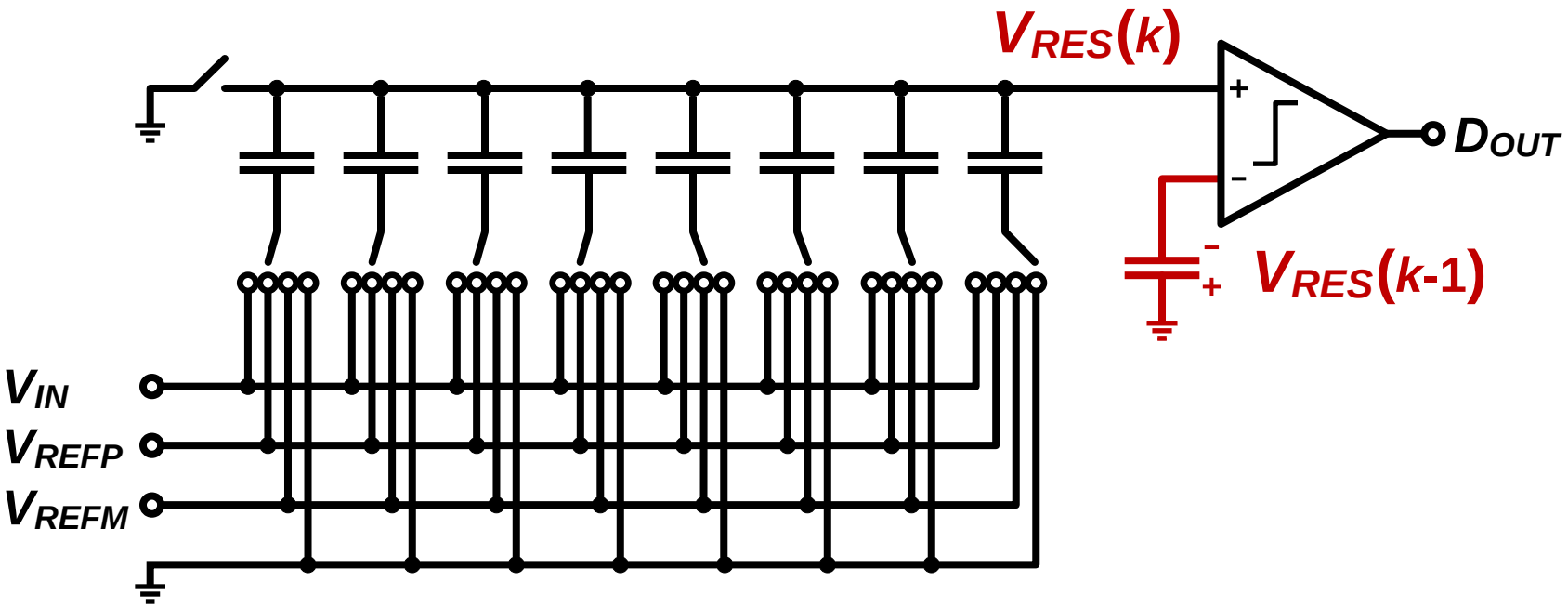
$$V_{RES}(k) = D_{OUT}(k) - V_{IN}(k)$$

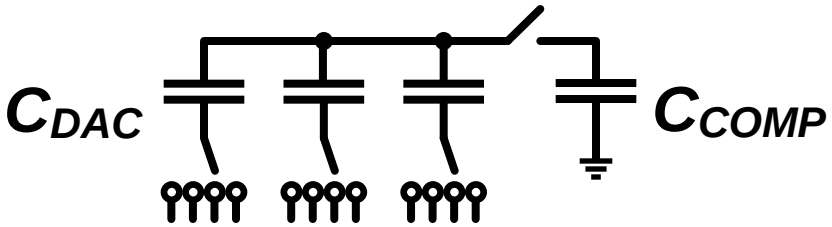
Simple SAR Noise Shaping



$$D_{OUT}(z) = V_{IN}(z) + \frac{1}{1+z^{-1}}\left[Q(z) + V_{N,COMP}(z)\right]$$

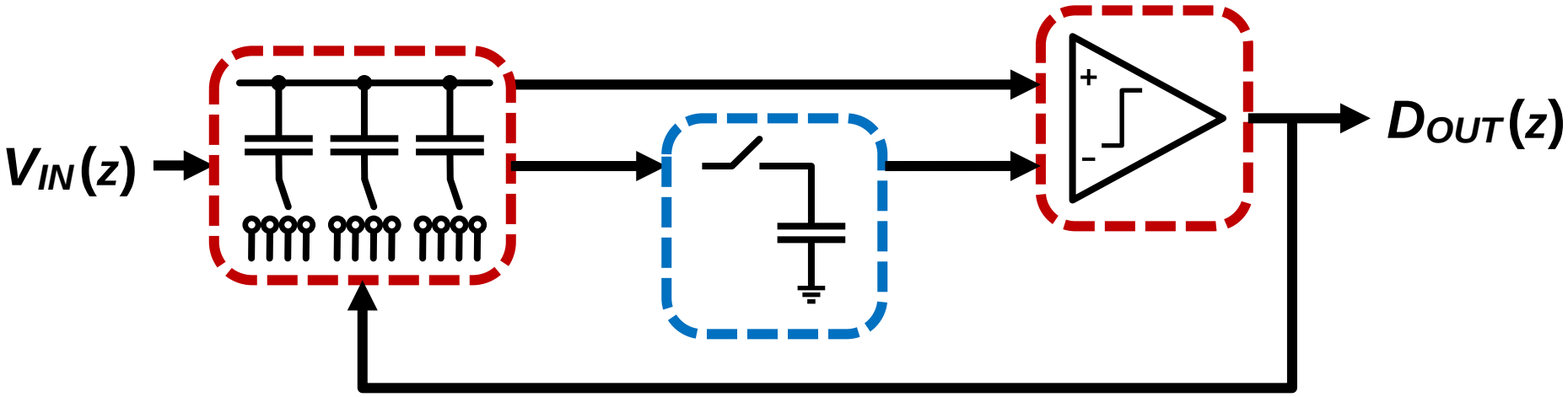
How To Do It



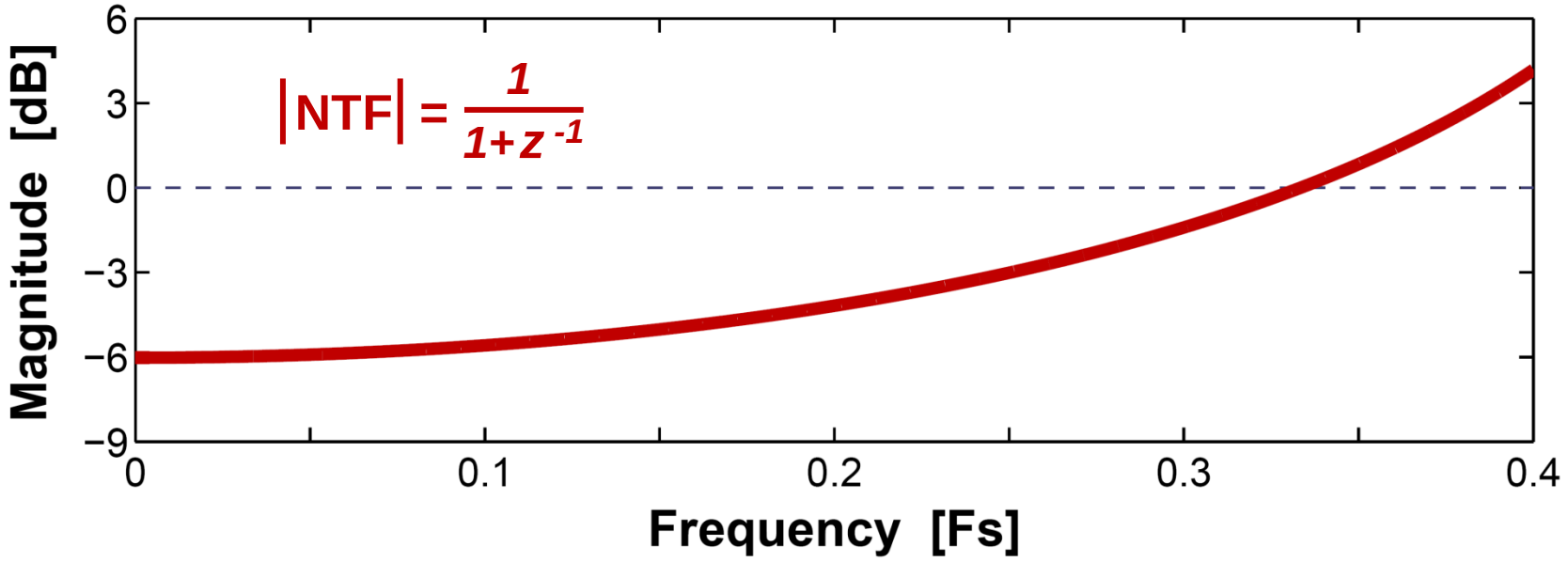


Passively Sample Residue

Signal Flow Diagram

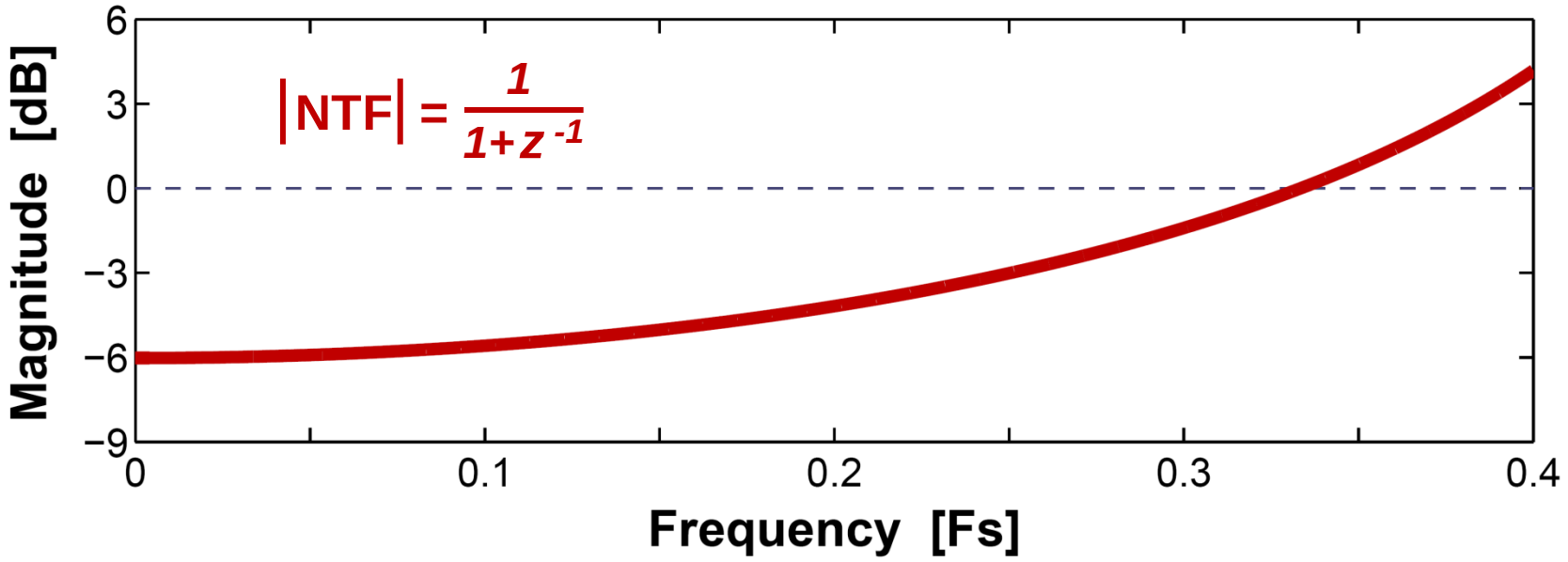


Advantages



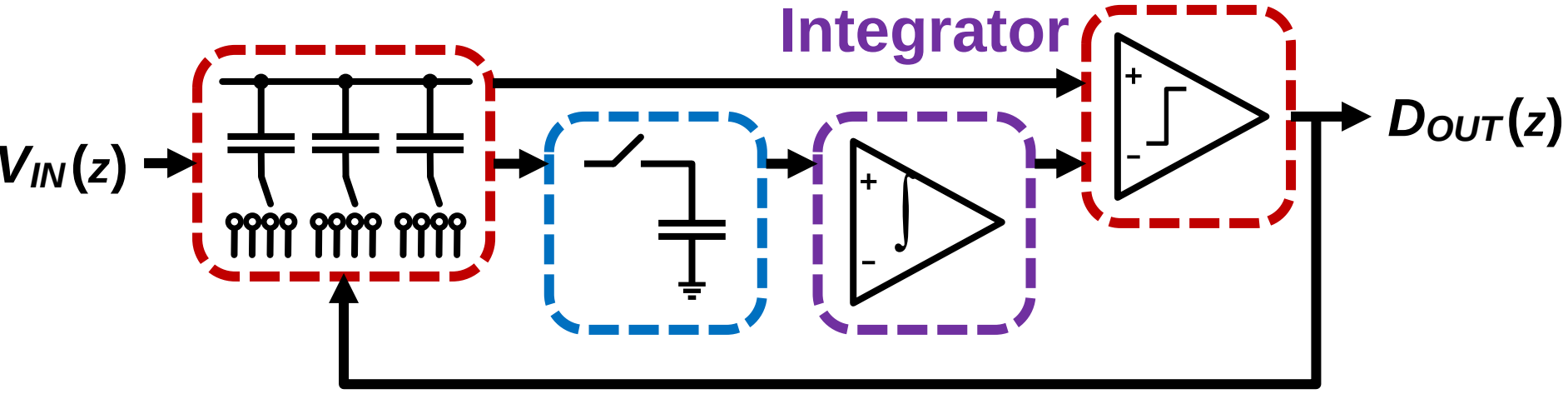
- ✓ Shapes quantization noise
- ✓ **Also shapes comparator noise**

Disadvantages

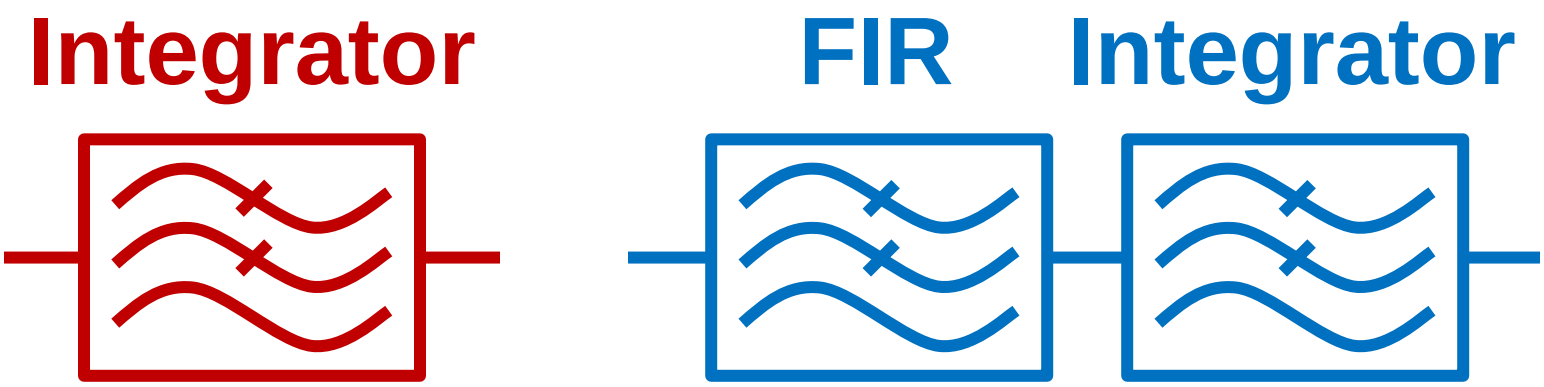


- ✗ Small resolution improvement

Improved SAR Noise Shaping

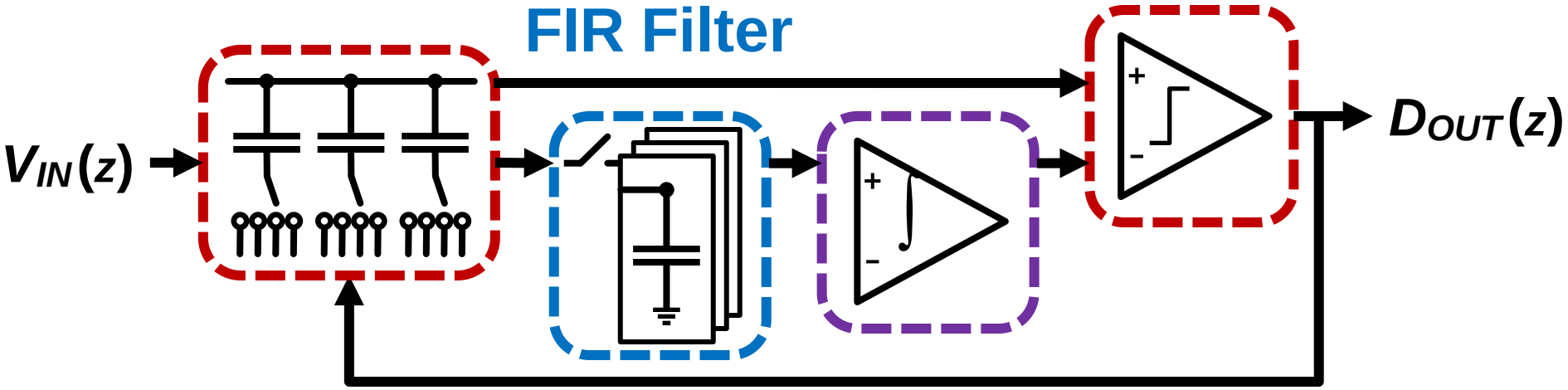


Improve the Integration Filter



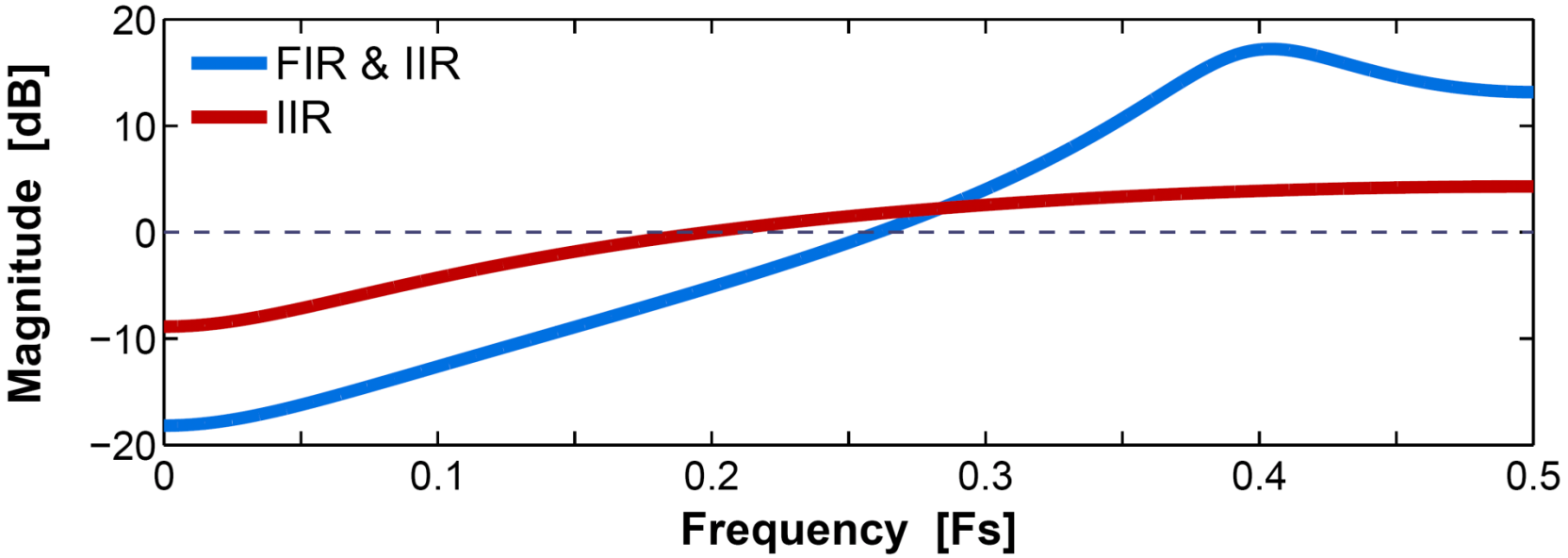
One good filter ➡ Two OK filters

Even Better Noise Shaping



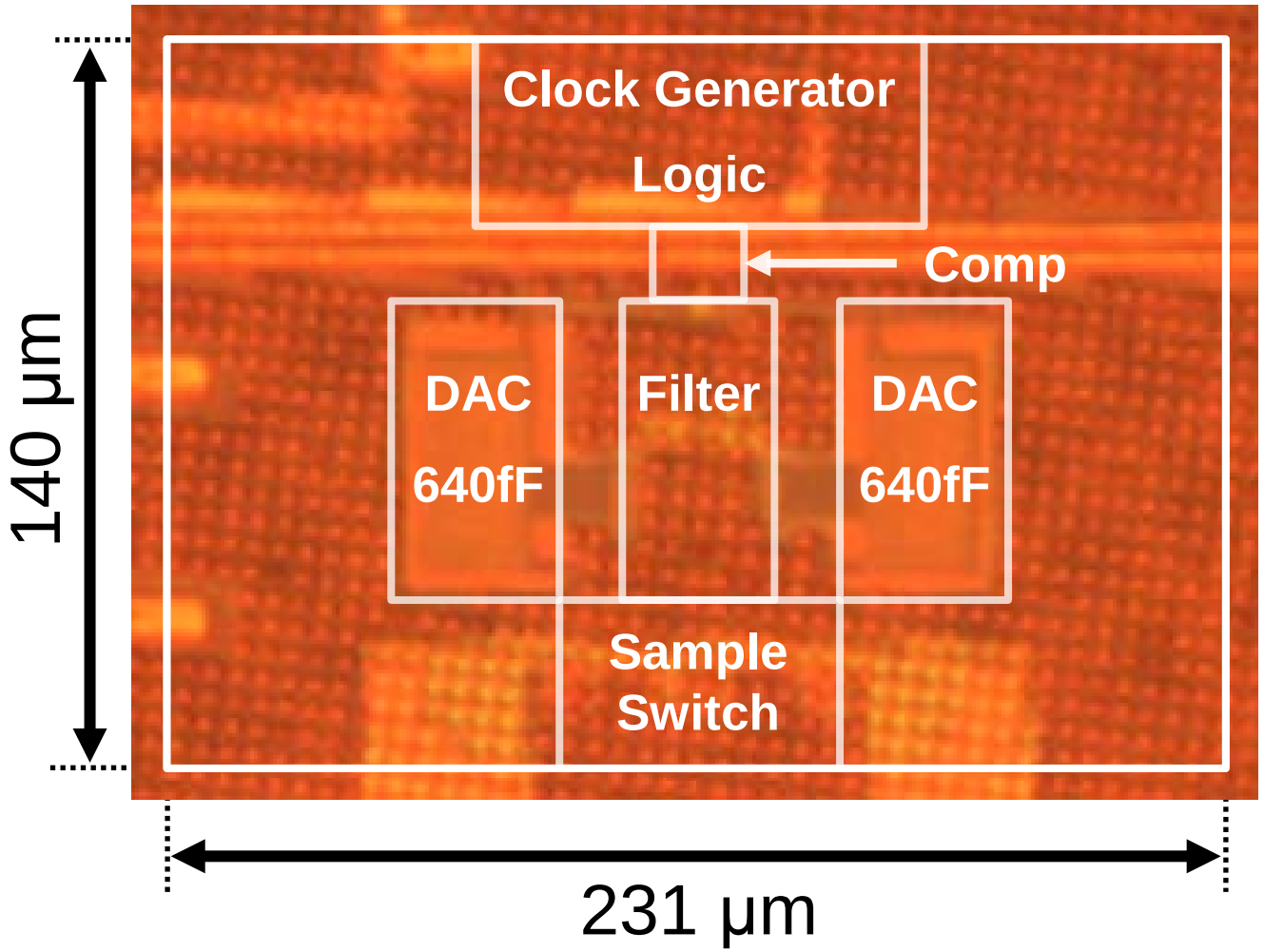
Adding this simple switch-capacitor FIR filter enhances the overall noise shaping

Better Noise Transfer Function



- ✓ Enhances a lossy IIR filter
- ✓ Widens attenuation bandwidth

Die Micrograph



65nm CMOS

0.03 mm^2

11 MHz BW

800µW

10 bit ENOB

36 fJ/conv-step

Conclusions

- **SAR ADCs are driving ADC efficiency**
- **Fundamentals of yield and power**
- **New architectures exploit SAR for higher performance**