Two-step Beat Frequency Quantizer Based ADC with Adaptive Reference Control for Low Swing Bio-potential Signals

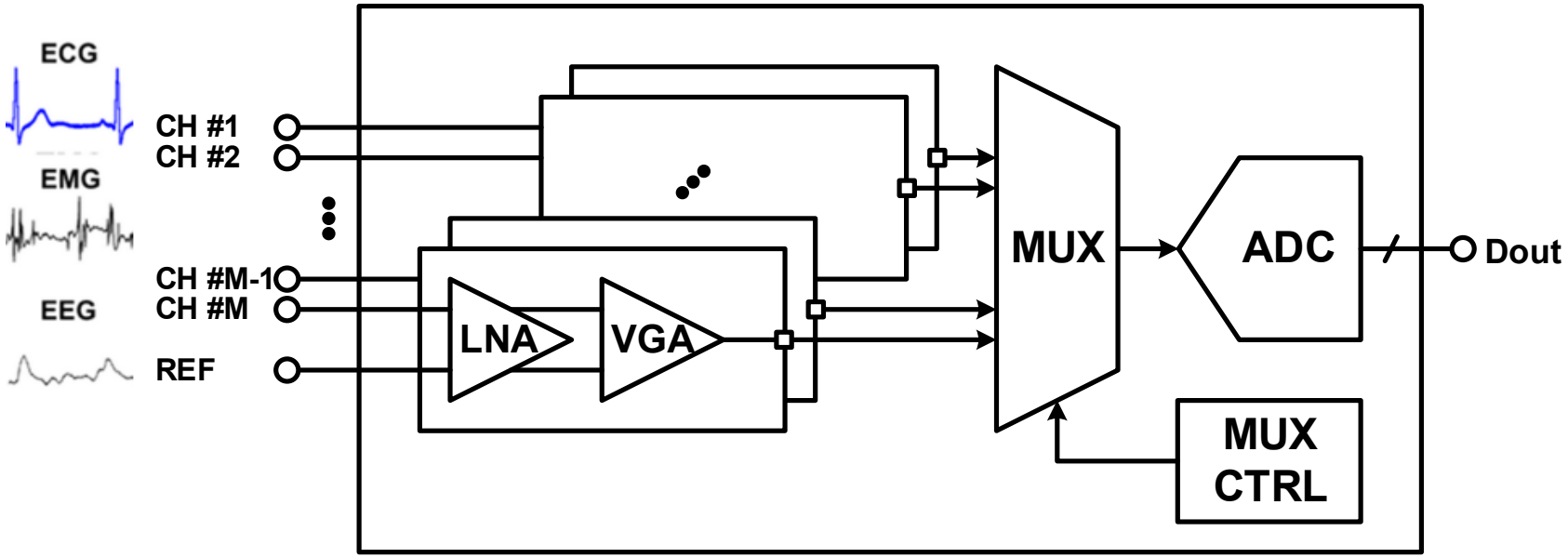
Somnath Kundu[1], Bongjin Kim[1,2], Chris H. Kim[1]

[1]Dept. of ECE, University of Minnesota, Minneapolis, MN
[2]Rambus Inc., Sunnyvale, CA

Outline

- Motivation
- Conventional Linear VCO based ADC
- Beat Frequency ADC
- Proposed Two-step Beat Frequency ADC
- 65nm Circuit Implementation Details
- Measurement Results
- Conclusion

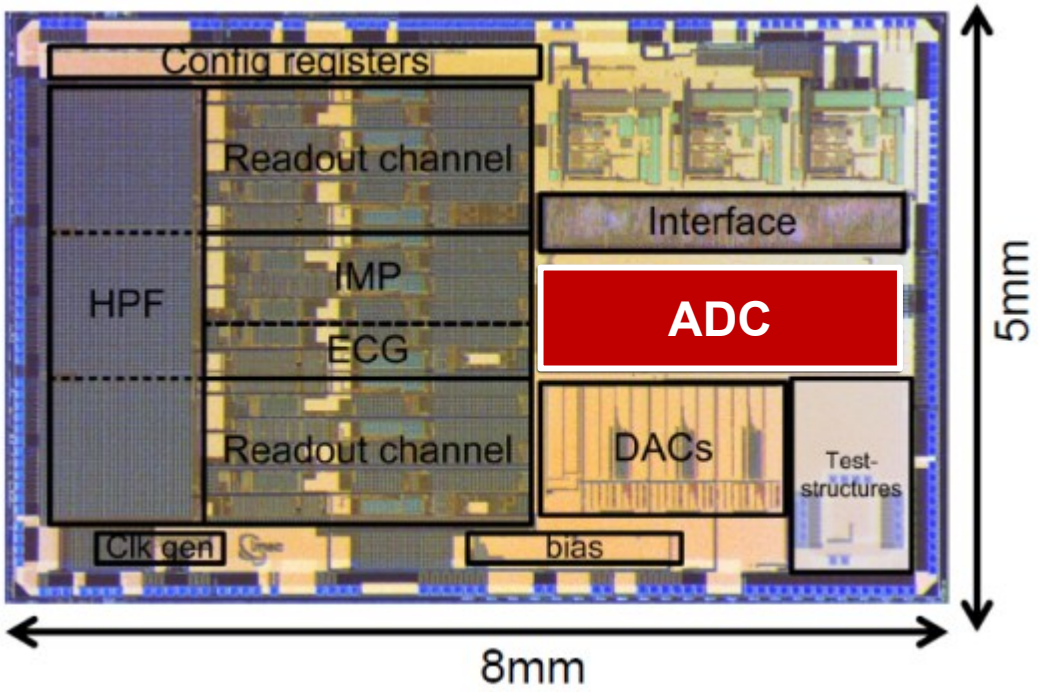
Typical Bio-Signal Sensing Block



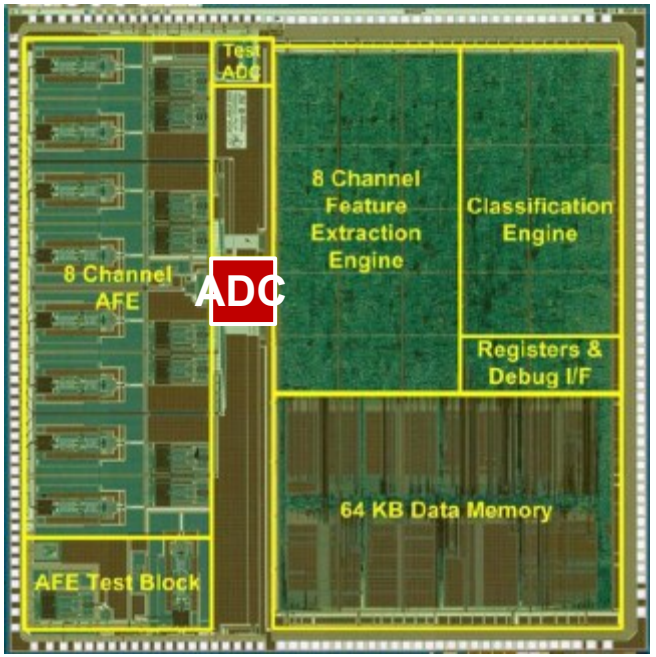
- Consists of amplifiers/filters, A/D converter (ADC), etc.
- Multi-channel amplifiers with active or passive filters
- ADC converts a time-multiplexed analog input to N-bit digital outputs → processed by on-chip or off-chip DSP

State-of-the-art Bio-potential Acquisition ASICs

N. Helleputte, ISSCC 2012

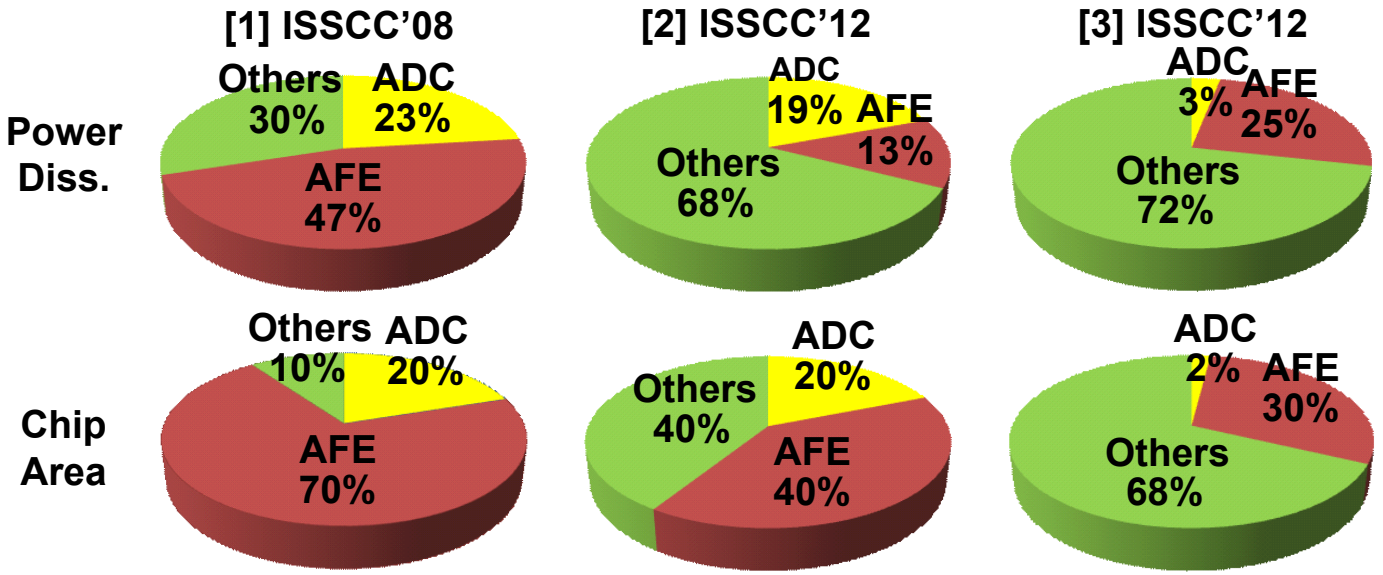


J. Yoo, ISSCC 2012



- ADC area is small
- A significant portion of the chip area is occupied by frontend amplifiers/filters

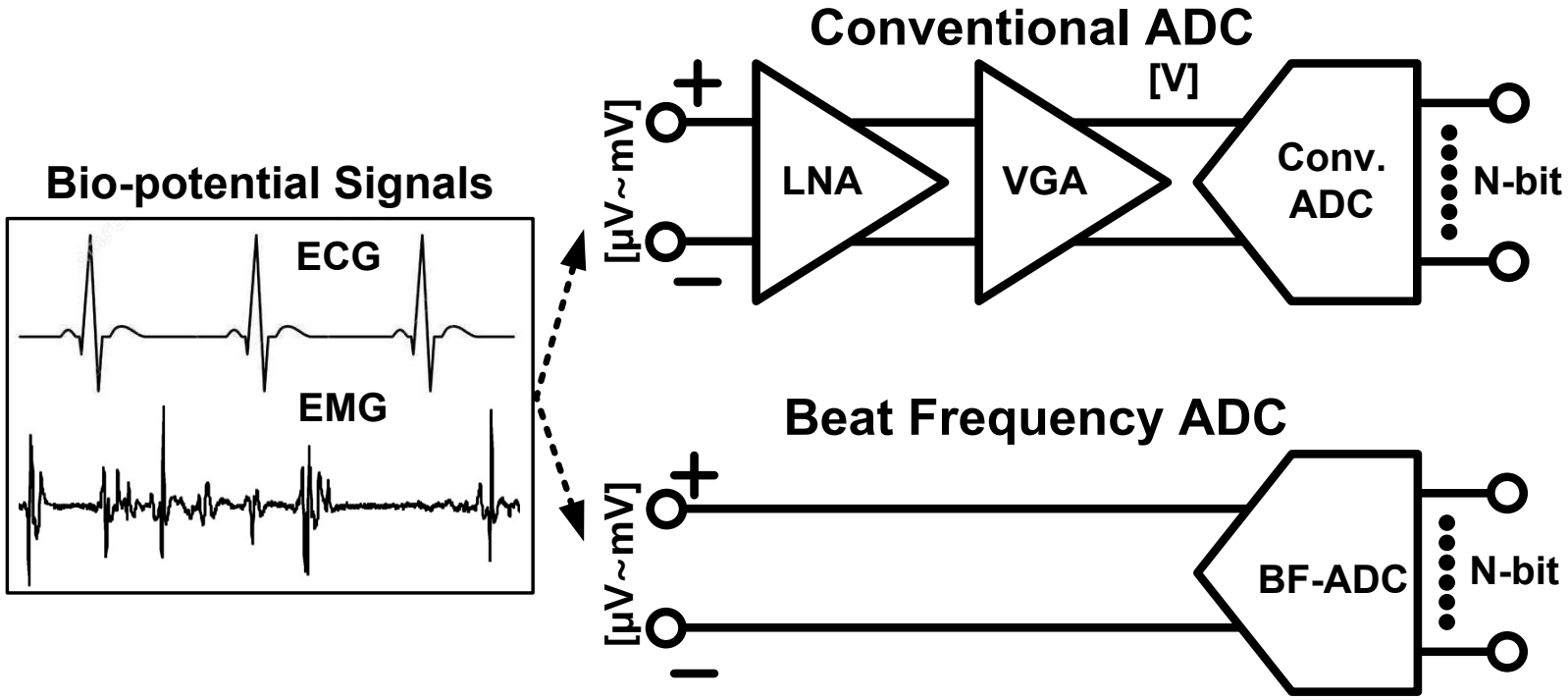
Area and Power Break-up in Bio-potential Acquisition ASICs



*AFE= analog front-end *Others include filters, bias and rest digital circuits

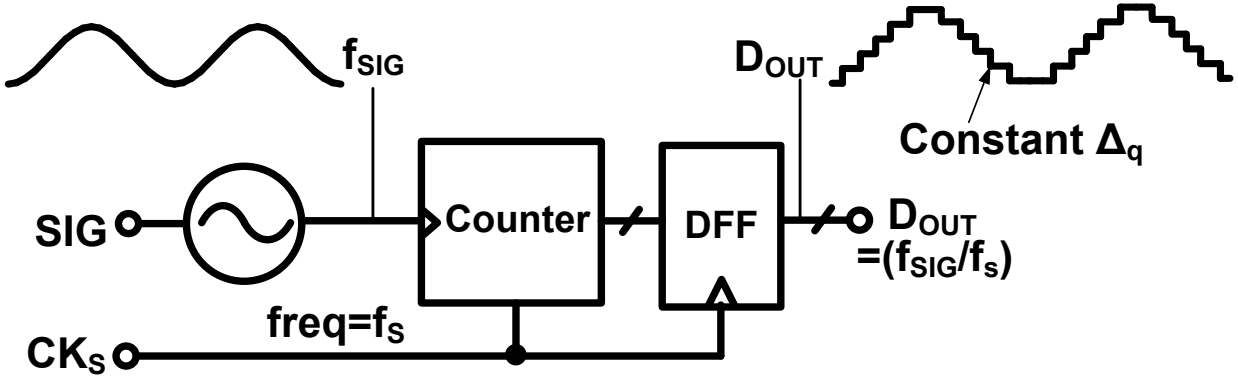
- ADC designs typically don't account for the design complexity, area and power overhead of the AFE circuits
- Motivation of this work: Direct conversion of low-swing (<10mV) signal to simplify or even eliminate AFE circuits

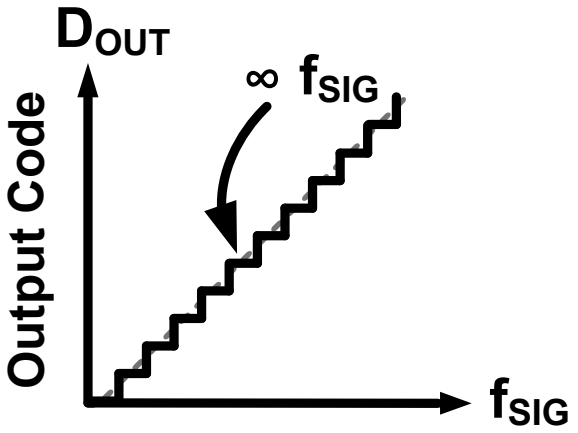
AFE Overhead Reduction by Beat Frequency ADC

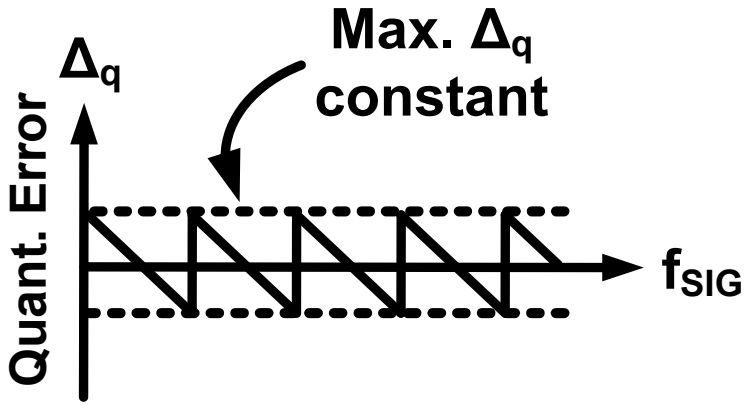


- **Beat frequency ADC can simplify or eliminate signal pre-conditioning amplifiers (LNA/VGA)**

Conventional VCO Based Linear ADC

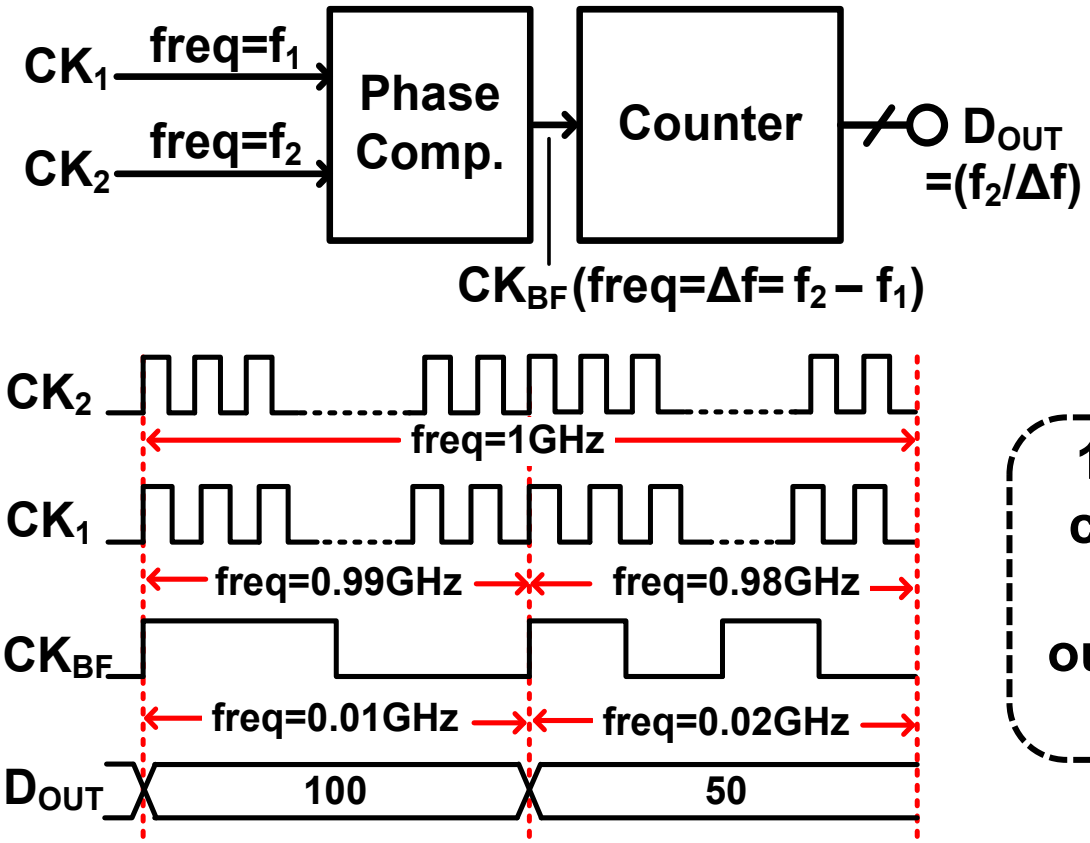






- Linear signal detection by VCO
- Poor resolution for low swing signals

Beat Frequency Detection

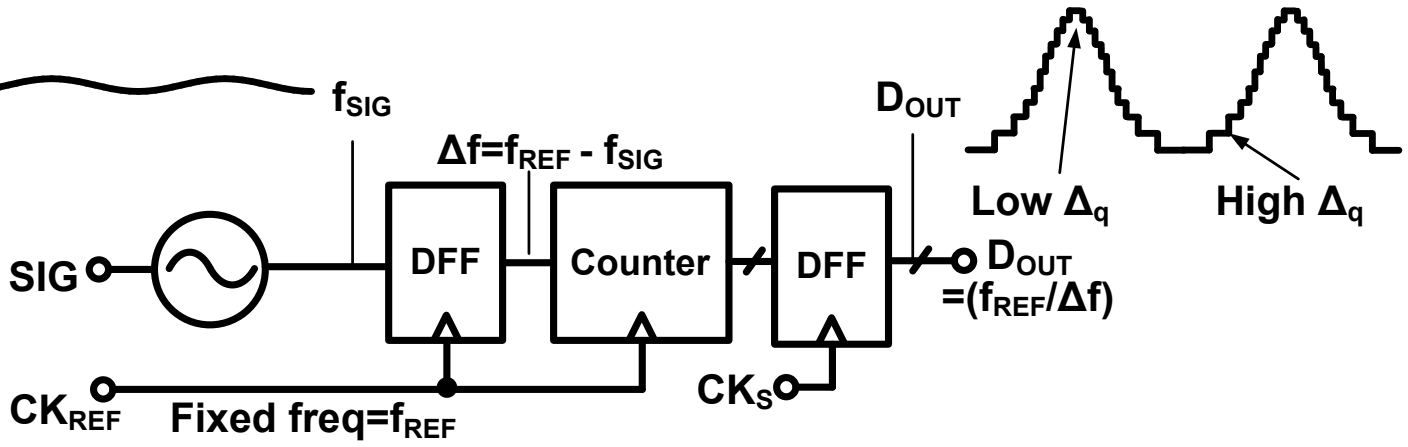


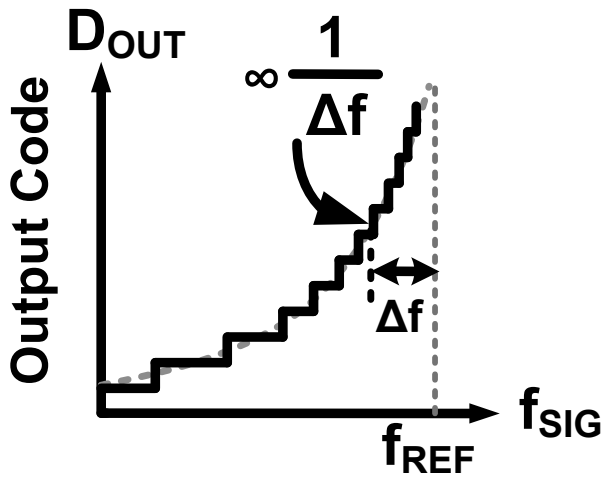
1% frequency change in CK_1 changes the output count by 50%

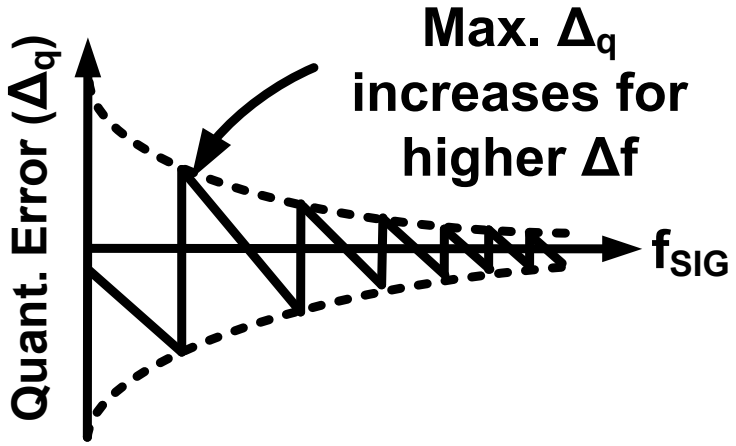
- Frequency sensing resolution inversely proportional to signal swing

[ref] T. Kim, VLSI 2007, JSSC 2008

Single Step Beat Frequency ADC



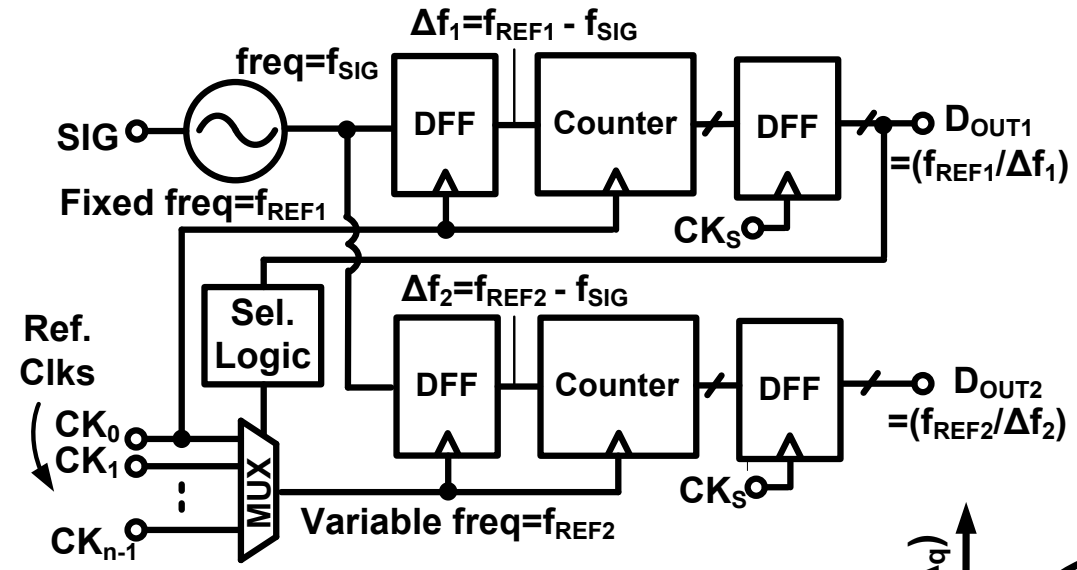


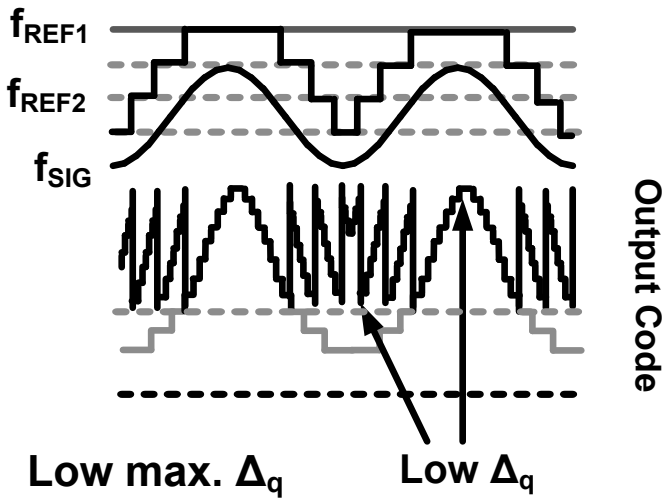


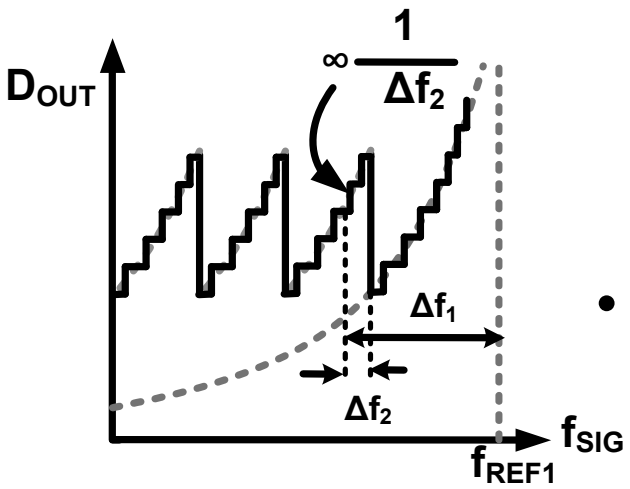
- High resolution beat frequency detection
- Resolution degrades as frequency difference increases

[ref] B. Kim, CICC 2013, CICC 2014

Two-Step Beat Frequency ADC

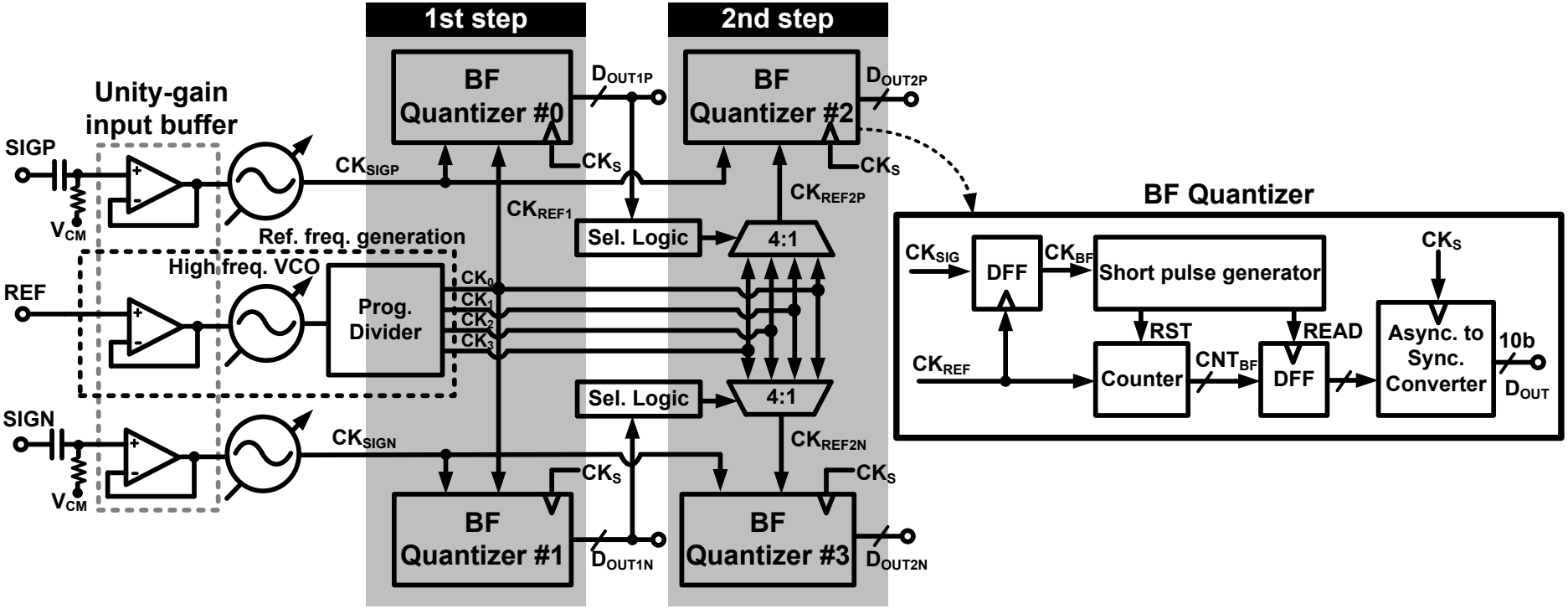






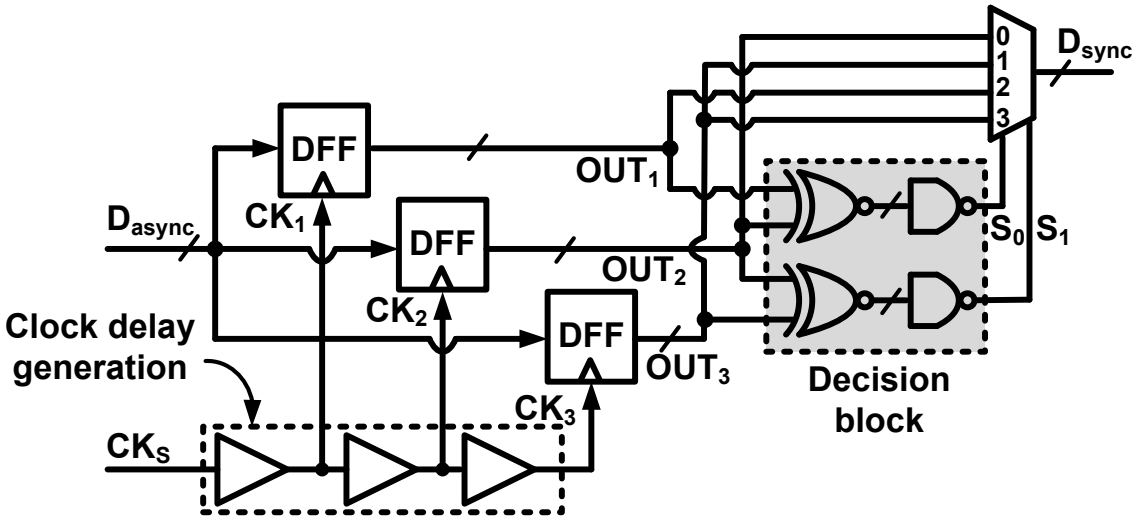
- **Two step detection scheme to change the reference depending on signal**

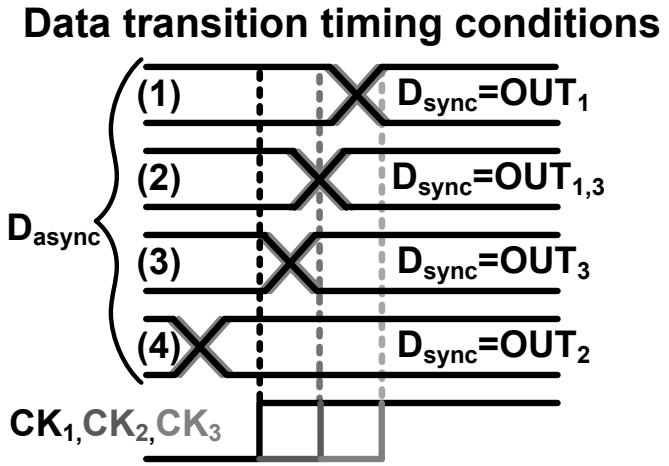
65nm Circuit Implementation

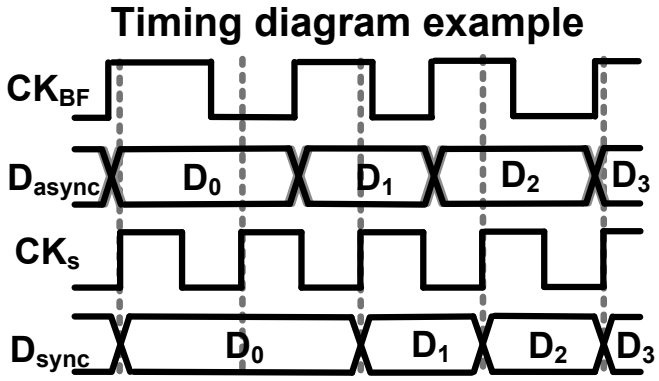


- **Multiple references are generated by diving a high speed reference oscillator**
- **Same input clock (CK_{SIGP}, CK_{SIGN}) applied in both steps**

Triple Sampling Synchronization

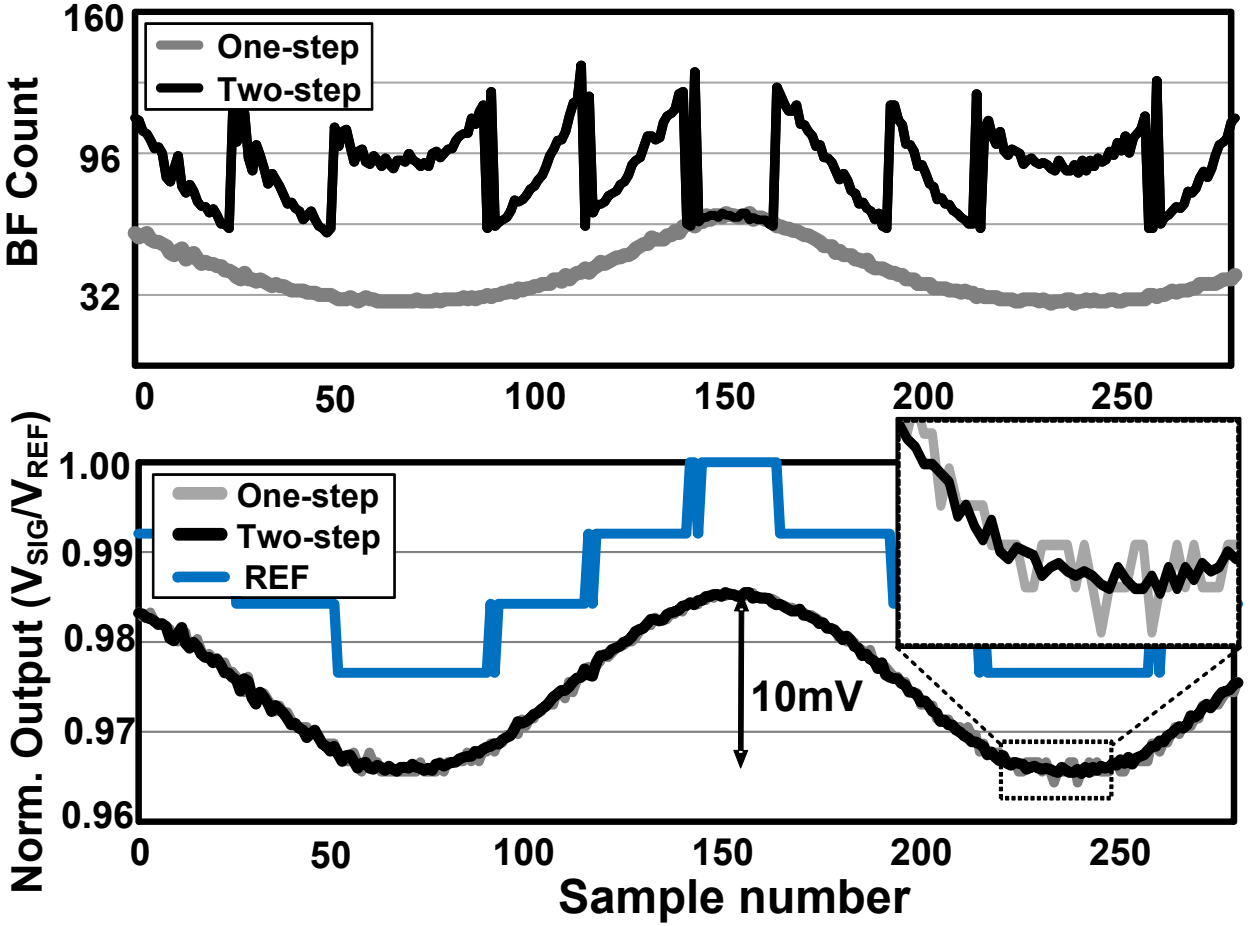






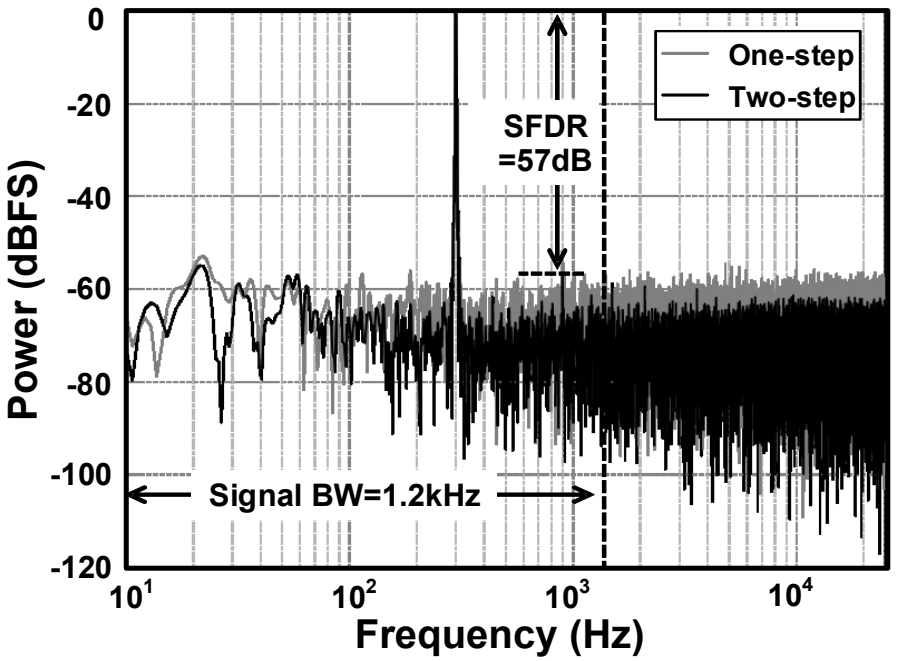
- **BF quantizer output data is sampled at a fixed rate without meta-stability**

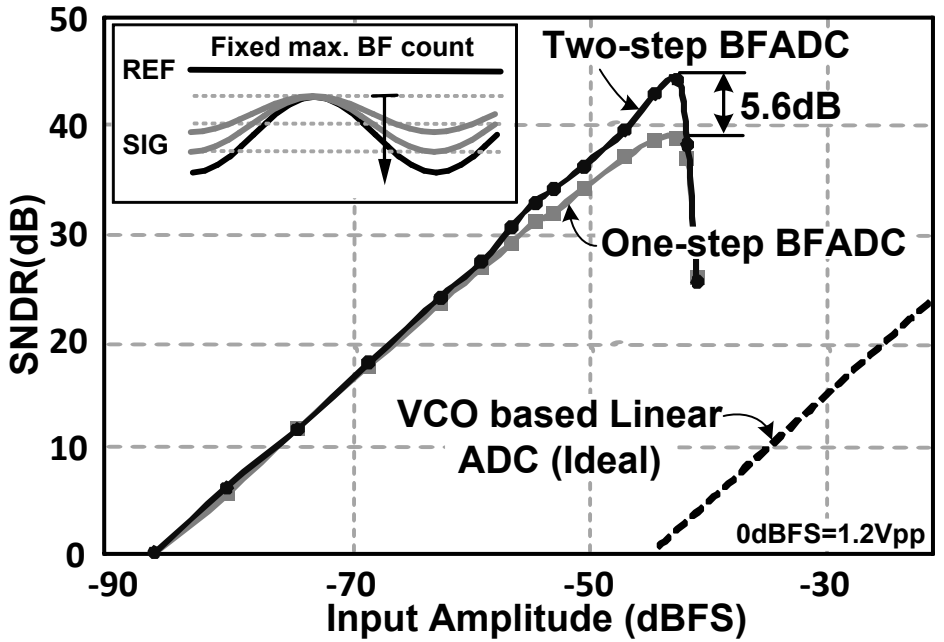
Measured BF Count and Reconstructed Signal



- **Input: 300Hz, 10mVpp differential sinusoidal wave**

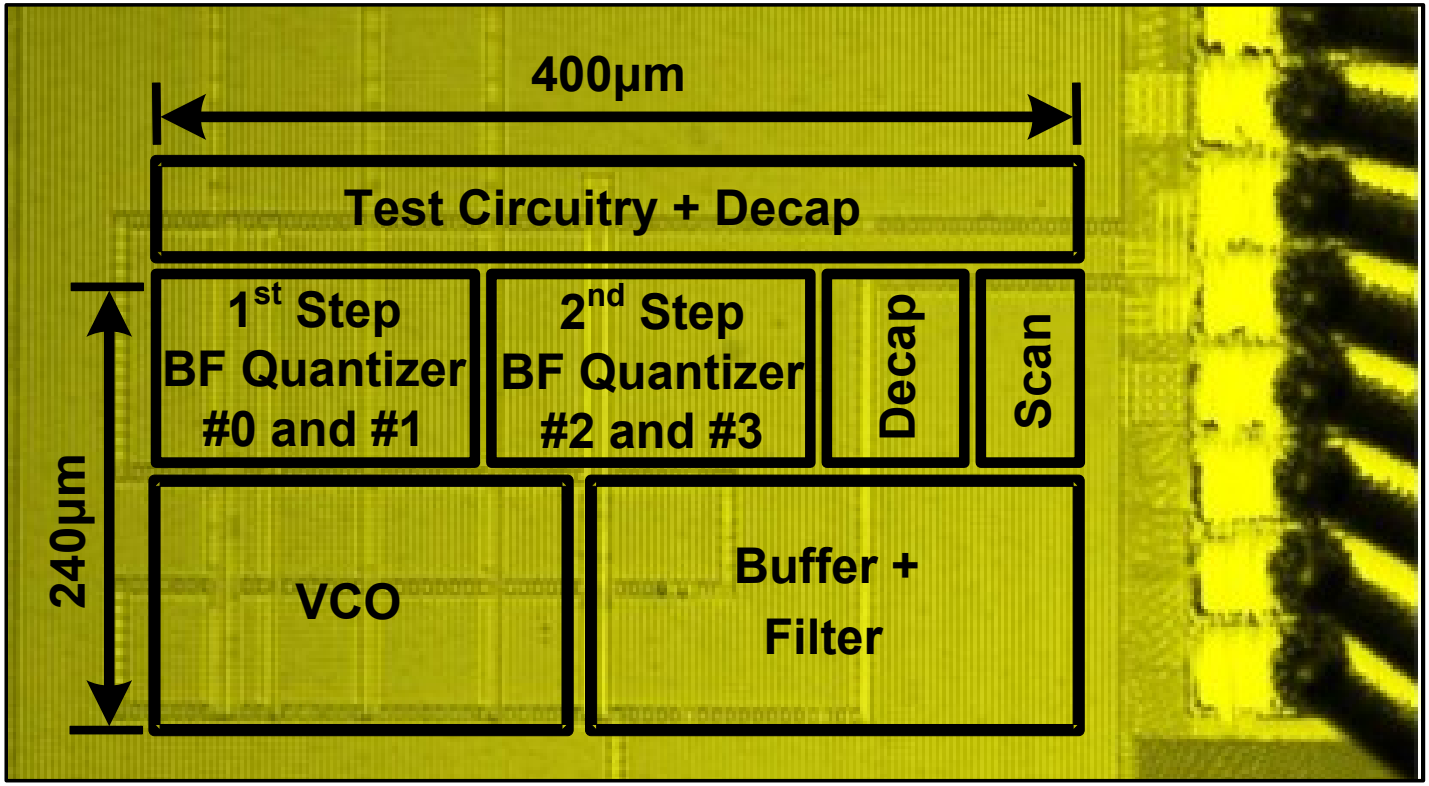
Measured FFT and SNDR vs. Input Amplitude





- SNDR @ 10mV=44.5dB for two-step, 38.9dB for single step
- Ideal linear ADC has better SNDR for input amplitude >-40dBFS

65nm Die Photo



- Core chip area 0.096mm^2

Performance Comparison

Parameters	This Work		[4] ESSCIRC'11	[10] VLSI'11	[11] VLSI'12	[12] CICC'14
ADC Type	One- step Beat freq.	Two- step Beat Freq.	CT- ΣΔ	VCO Based	Two-step ΣΔ	PWM Based ΣΔ
Process/Supply	65nm/1.2V		0.18µm/1.4V	90nm/1.15V	0.13µm/1.2V	0.18µm/1.8V
Input freq./BW	300Hz/1.2kHz		21Hz/256Hz	30kHz/8MHz	500kHz/5MHz	221.5kHz/1MHz
Sampling Rate	50kHz		57kHz	640MHz	80MHz	144MHz
IN_{0dB}[dBFS]*	-86		-80	-65	-71	-54
$SNDR_{10mVpp}$**	38.9dB	44.5dB	40dB	20dB	22dB	20dB
$ENOB_{10mVpp}$**	6.17	7.1	6.35	3.03	3.36	3.03
Power	34µW	38µW	13.3µW	4.3mW	8.1mW	2.7mW
FoM_{10mVpp}[pJ/Conv]***	197	115	318	33	79	165.3
Chip area	0.096mm^2		0.51mm^2	0.1mm^2	0.37mm^2	0.0275mm^2

**Input amplitude at SNDR=0dB, **SNDR/ENOB for 10mVpp, ***FoM =* $\frac{Power}{2^{ENOB_{10mVpp}} * 2 * BW}$

Conclusion

- **Two-step VCO based beat frequency detection scheme is designed using 65nm CMOS for direct A-to-D conversion**
- **A triple sampling synchronization technique is implemented to sample ADC output at a fixed sampling rate**
- **44.5dB SNDR (i.e. 7.1 ENOB) is achieved for a 10mVpp differential input signal**