An On-chip Stochastic Sigma-tracking Eye-opening Monitor for BER-optimal Adaptive Equalization

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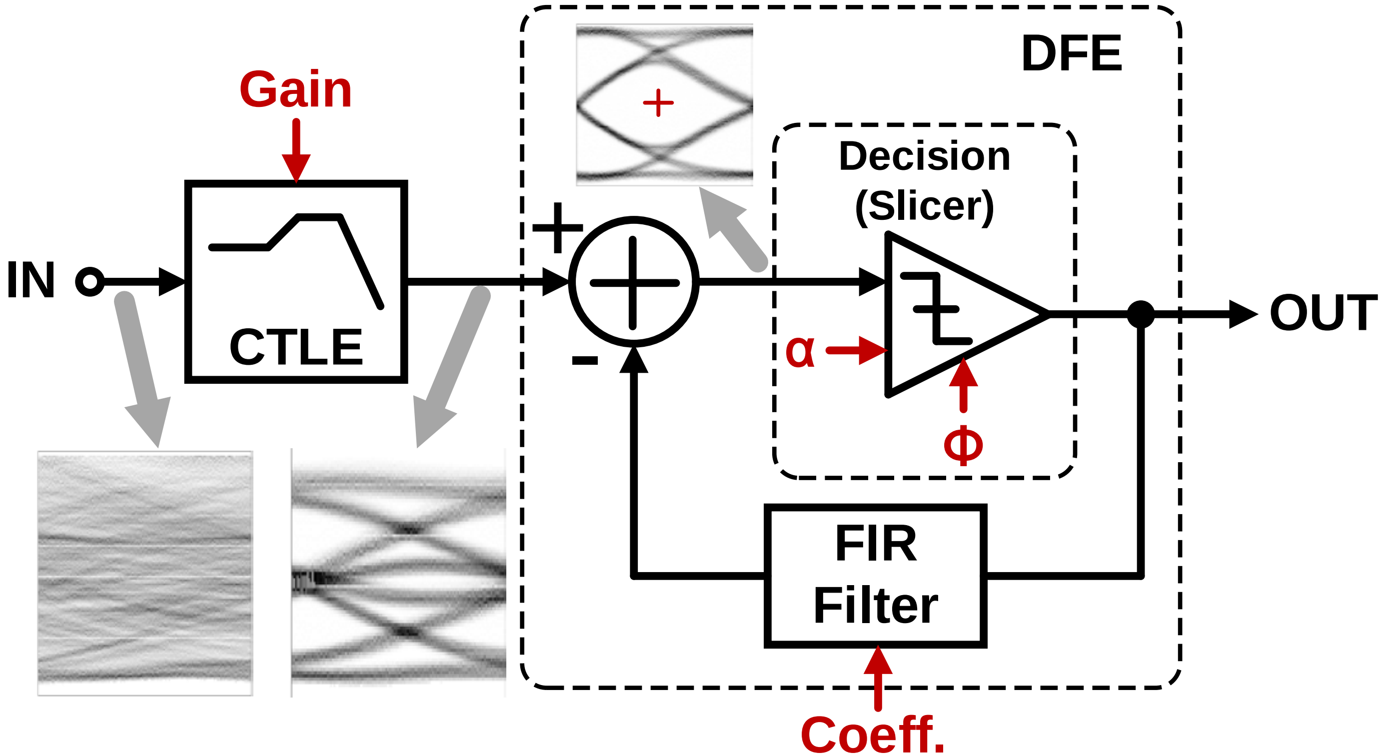
NANOSCALE ADVANCED INTEGRATED SYSTEMS LAB

Outline

- Introduction
- Stochastic sigma-tracking eye-opening monitor (SSEOM)
  - Optimal sampling point adaptation
  - CTLE/DFE adaptation
  - Background adaptation
- Measured results
- Summary

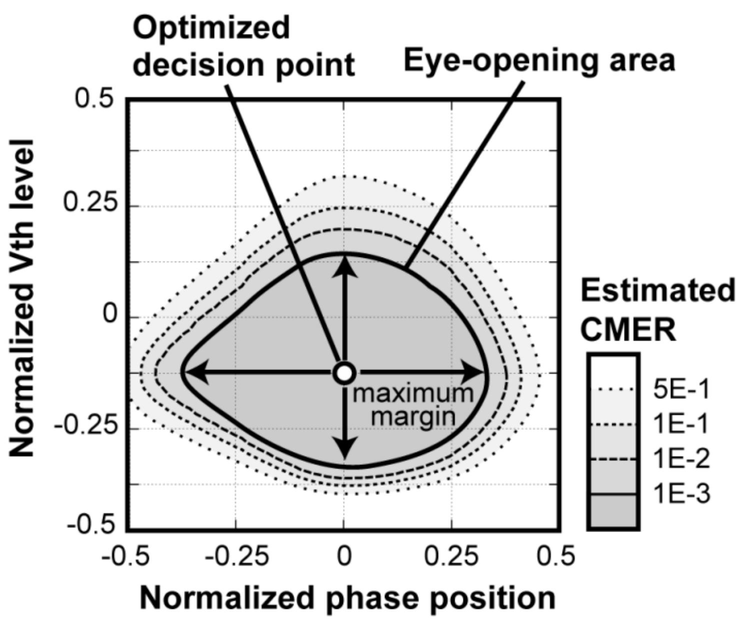
BER Optimization in RX



- Equalizers : CTLE gain, DFE coefficients
- Sampling point : Threshold α, clock phase Φ
- No single solution to adapt all parameters

Optimal Sampling Point

- Determined by BER results
- Low-BER serial-link (e.g. $< 10^{-12}$)
  ➔ Huge amount of time & silicon area
- Adaptive decision-point control (H. Noguchi, 08)

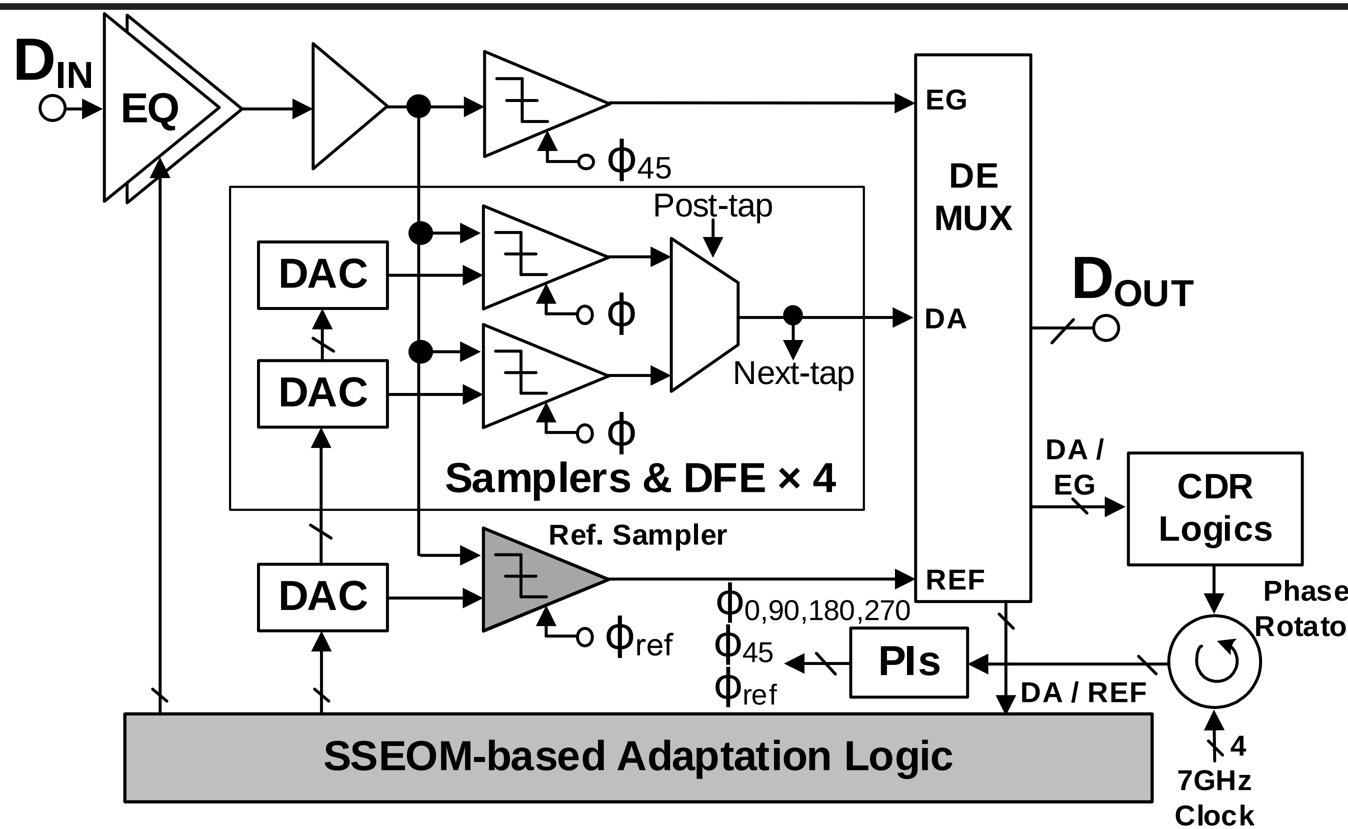


➔ Large memory size
➔ Complicated logic

Proposed SSEOM

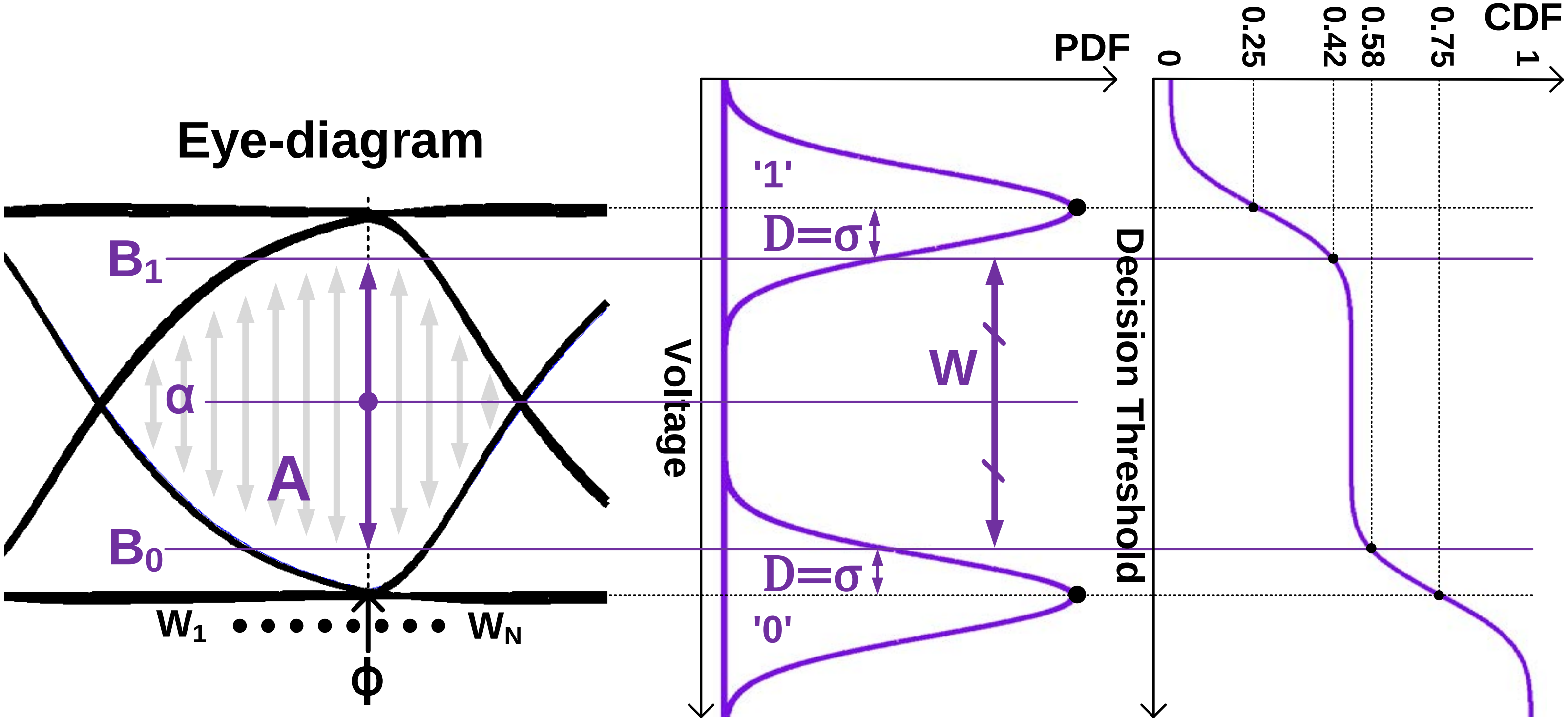
- CTLE & DFE adaptation
- Optimal sampling point
- Background adaptation
- On-chip implementation

Top Block Diagram – 28Gb/s CDR



- Quad-rate phase rotator-based PLL
- Two-stage CTLE & One-tap loop-unrolled DFE
- SSEOM logic & Auxiliary reference sampler

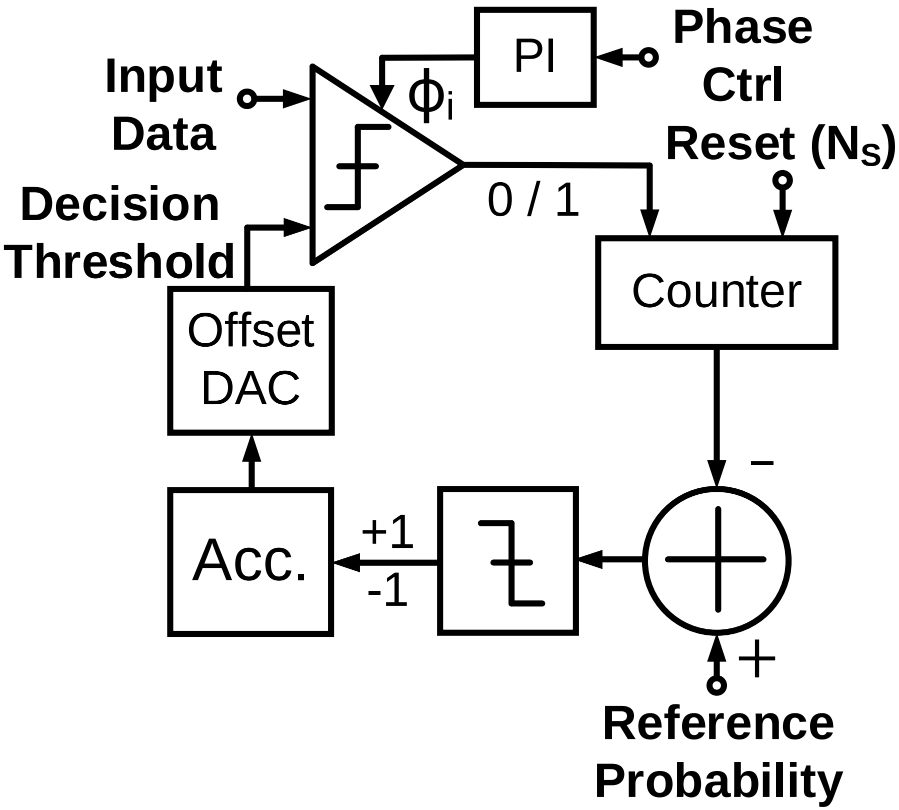
Concept of SSEOM



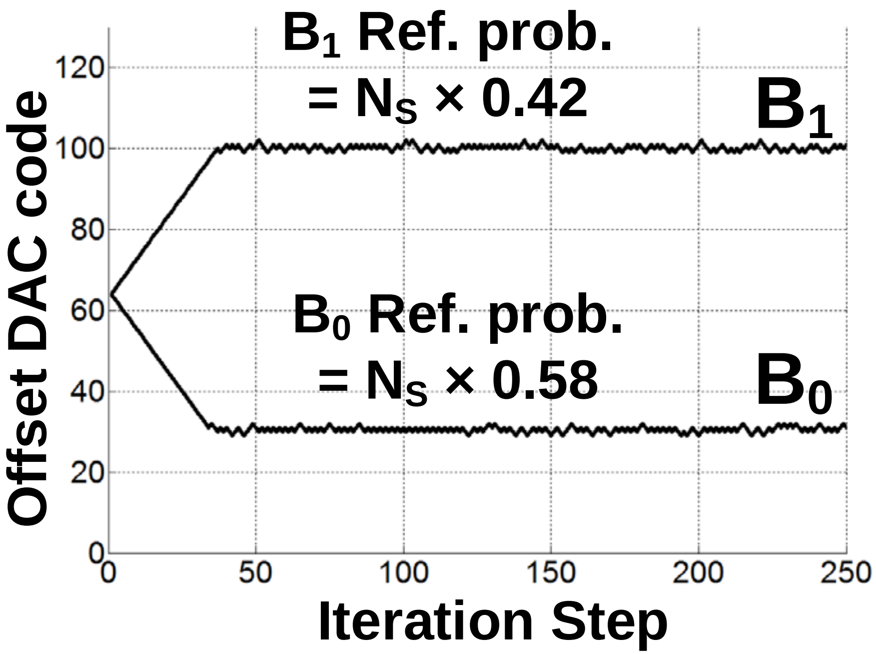
- $W = B_1 - B_0$: Effective eye-opening size
- $\alpha = (B_1 + B_0)/2$: Optimal decision threshold
- Φ : Optimal sampling clock phase
- A : Effective eye-opening area

Measuring B_1 and B_0

- **Feedback loop Implementation**



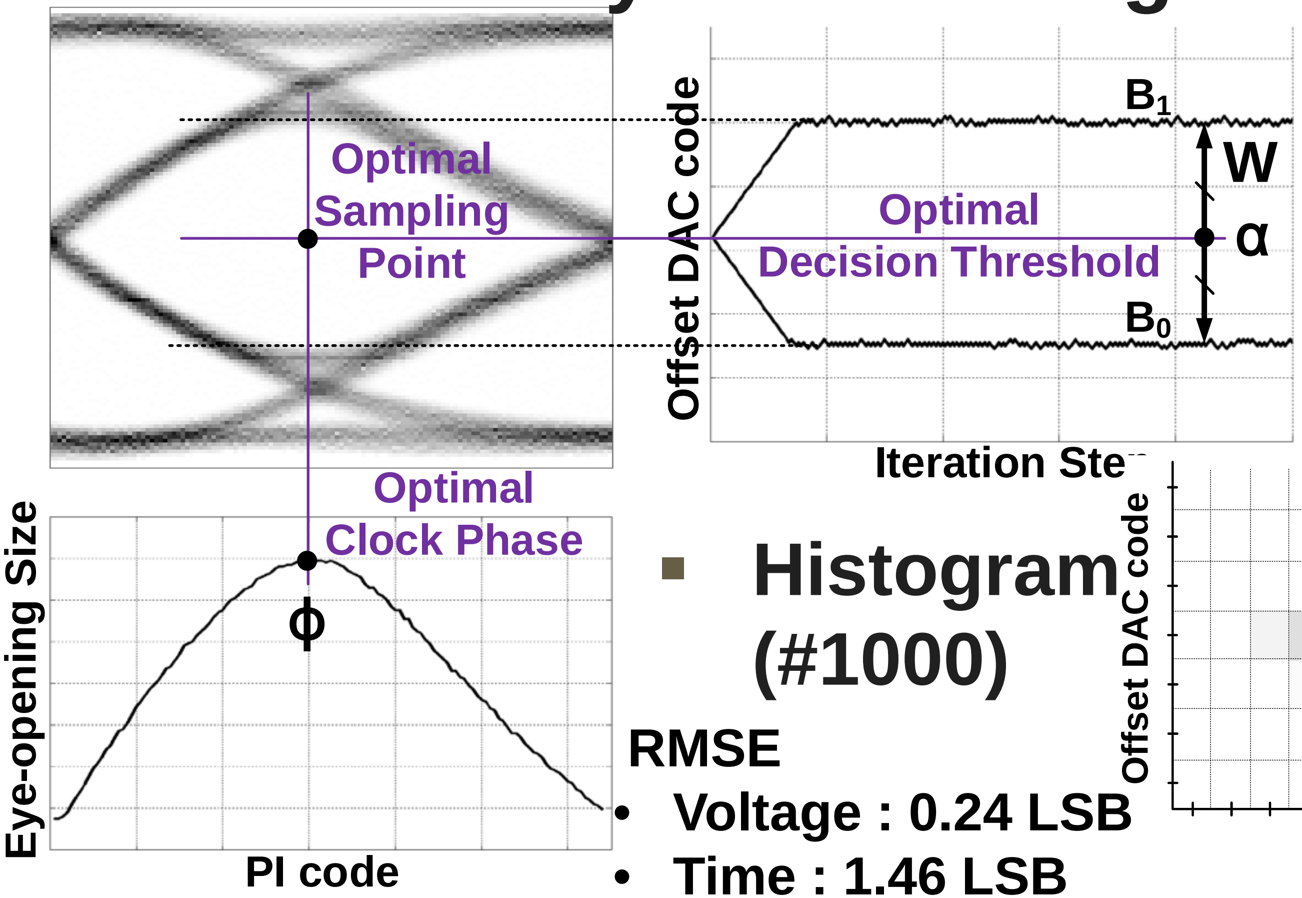
- **Measured B_1 & B_0**



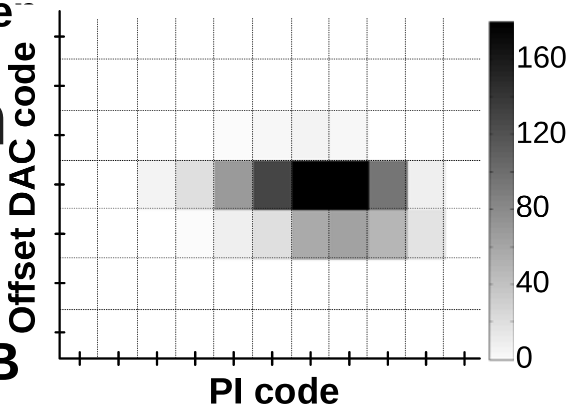
(N_S = 2048)

Optimal Sampling Point

- Found optimal sampling point in the internal eye-monitoring result



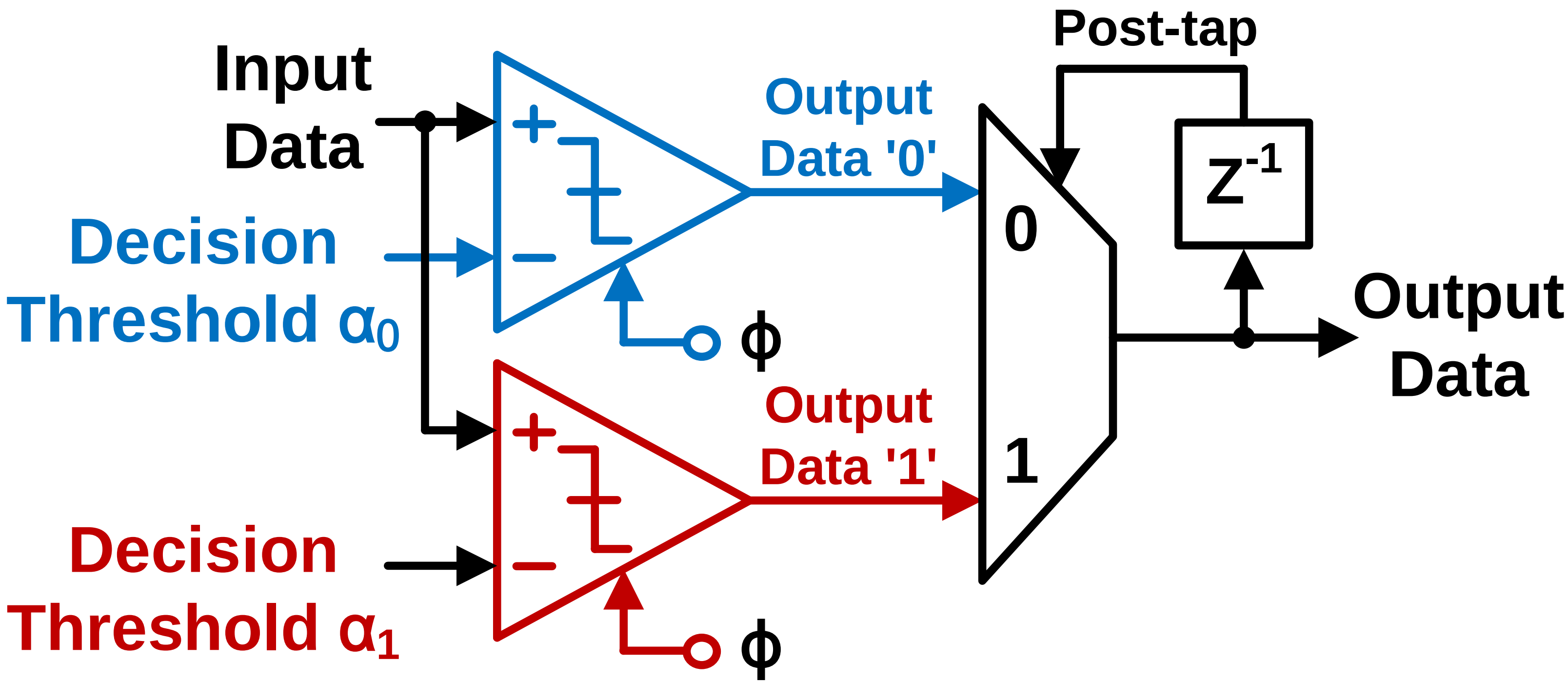
- Histogram (#1000)



RMSE

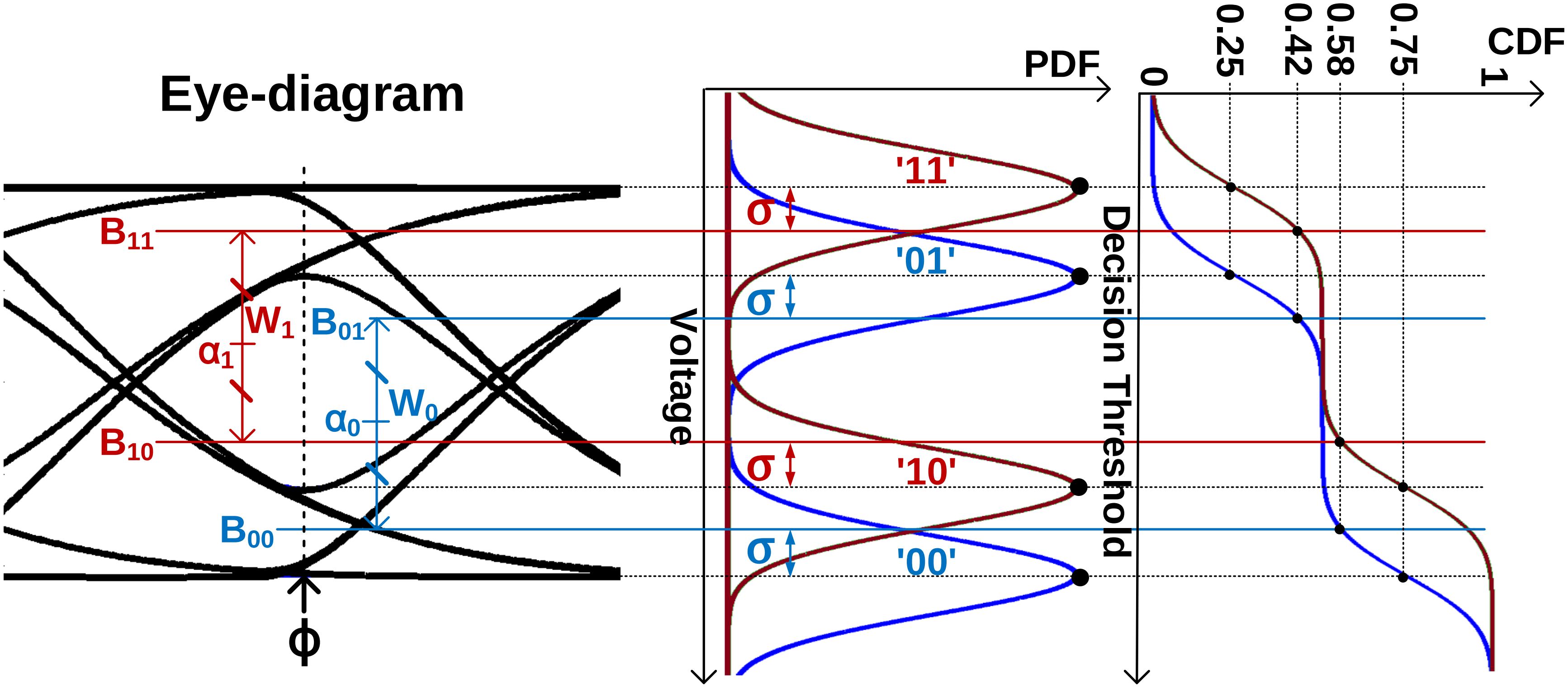
- Voltage : 0.24 LSB
- Time : 1.46 LSB

Loop-unrolled DFE



- Relaxed timing constraint rather than direct feedback DFE
- Adaptation ➔ Determine optimal decision threshold α_0 and α_1

SSEOM with ISI

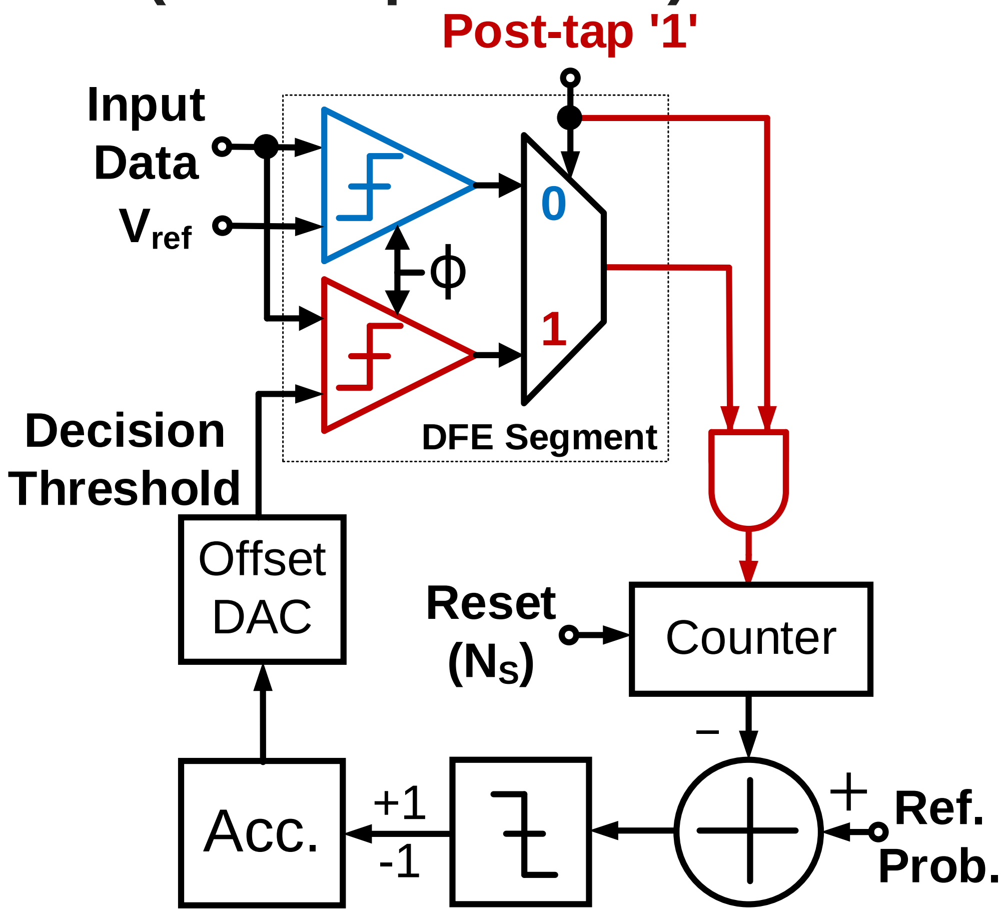


- **Post-tap '1' : B_{11}, B_{00}, Post-tap '0' : B_{01}, B_{00}**
- **W_1, W_0 : Effective eye-opening size**
- **α_1, α_0 : Optimal decision threshold**

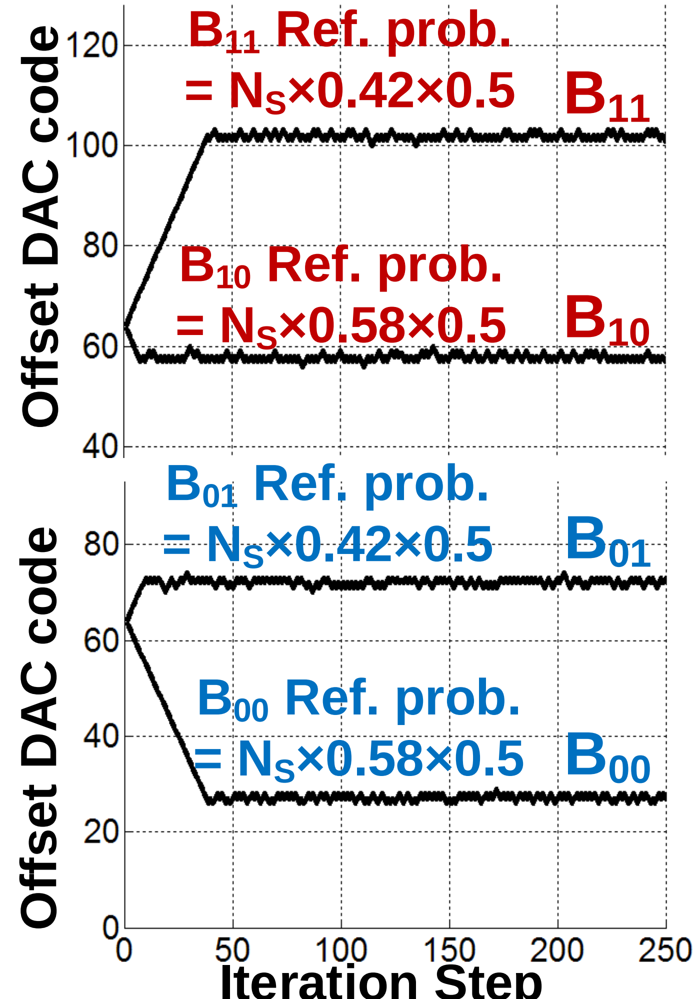
Measuring B_{xy}

- **Implementation**

  (Post-tap '1' case)

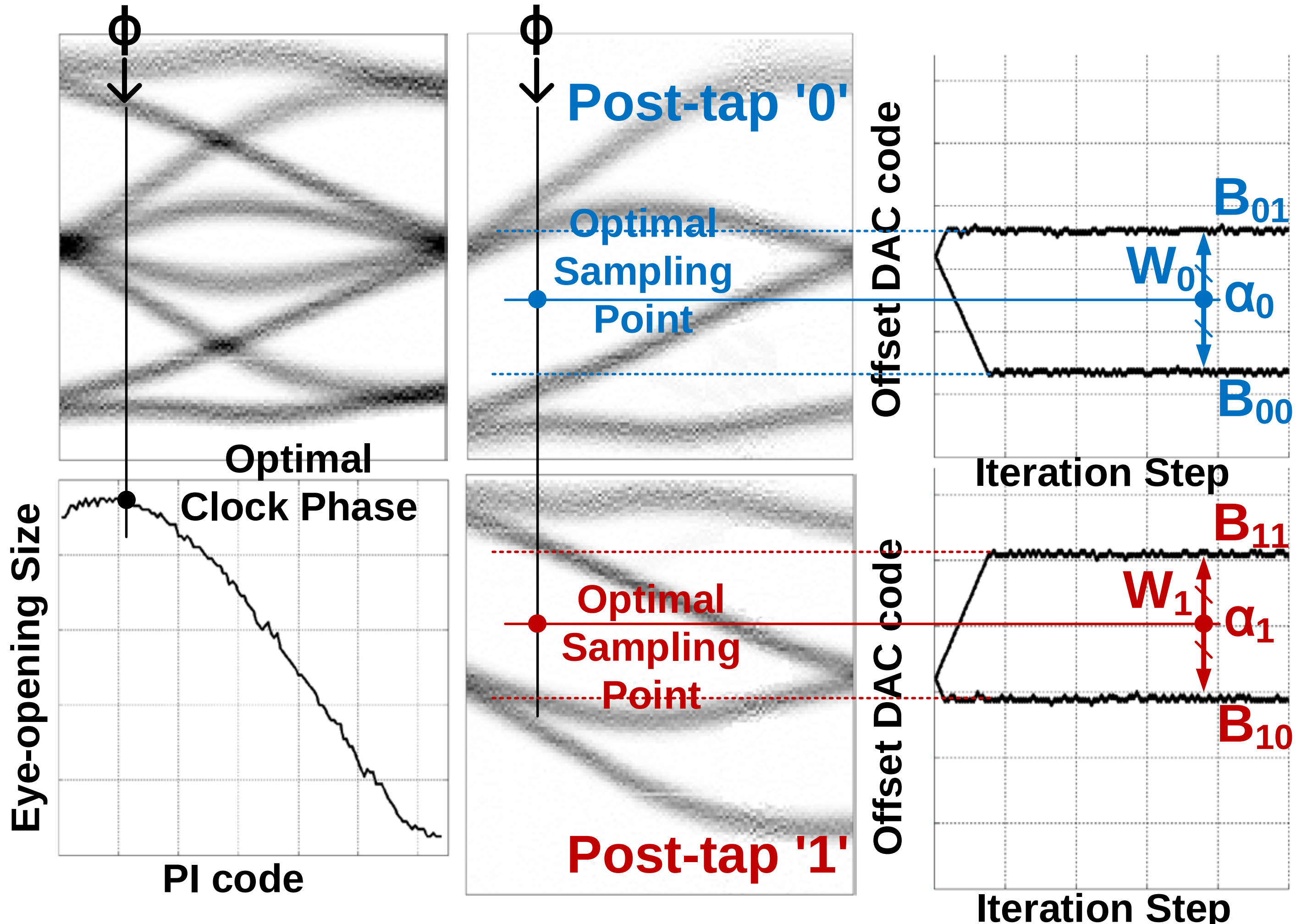


- **Measured B_{xy}**



Optimal Sampling Point under ISI

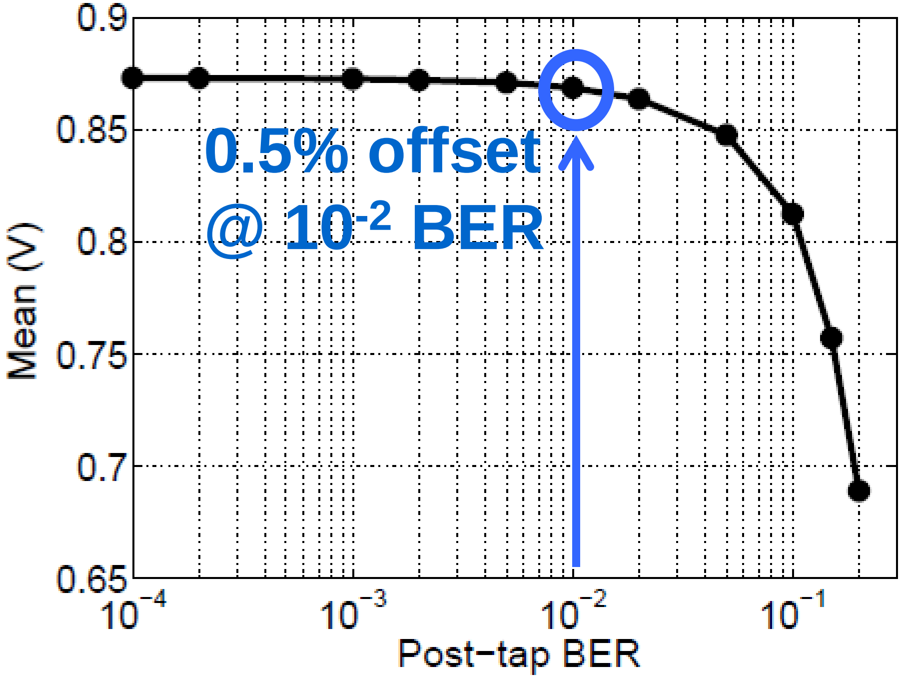
- Found optimal sampling point in eye-diagram



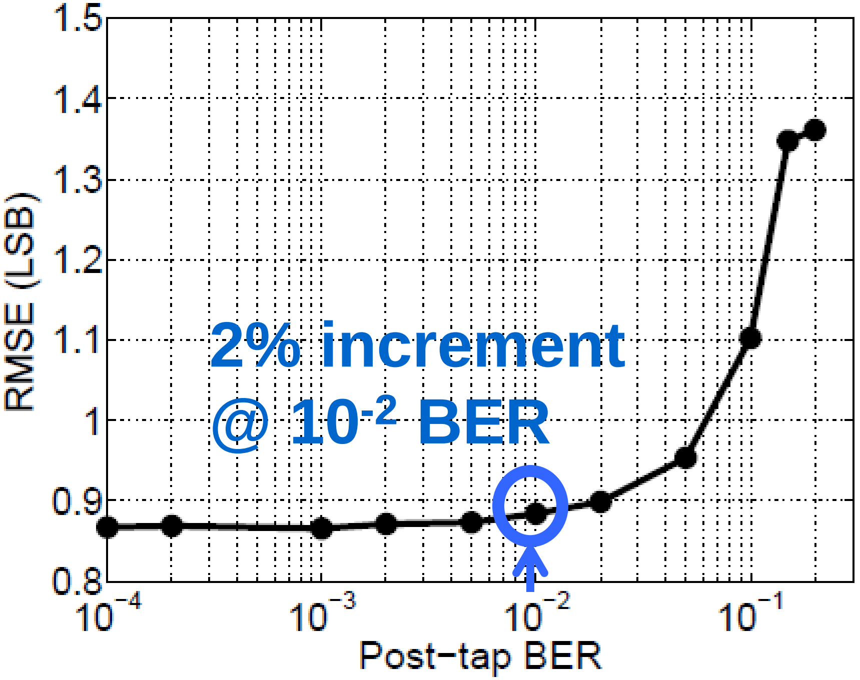
Effects of high-BER of post-tap

- High-BER of post-tap value
  ➔ Low accuracy of SSEOM

- Mean value of B_{11}

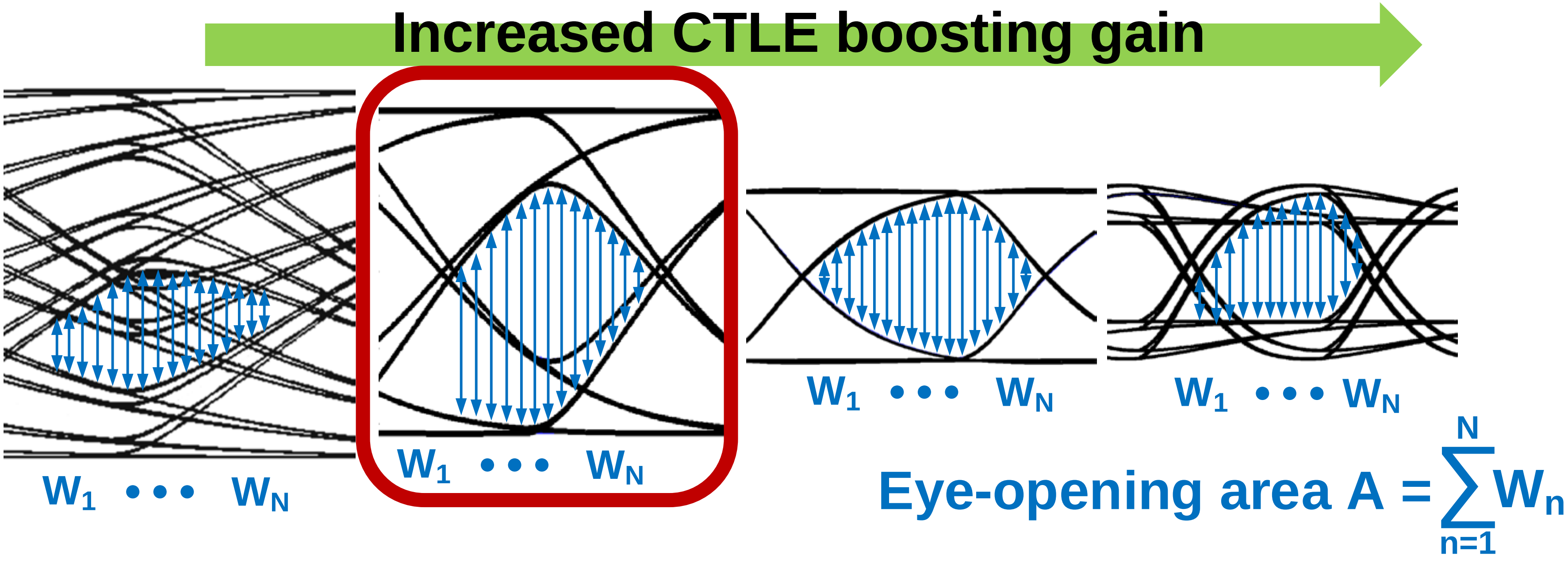


- RMSE of B_{11}



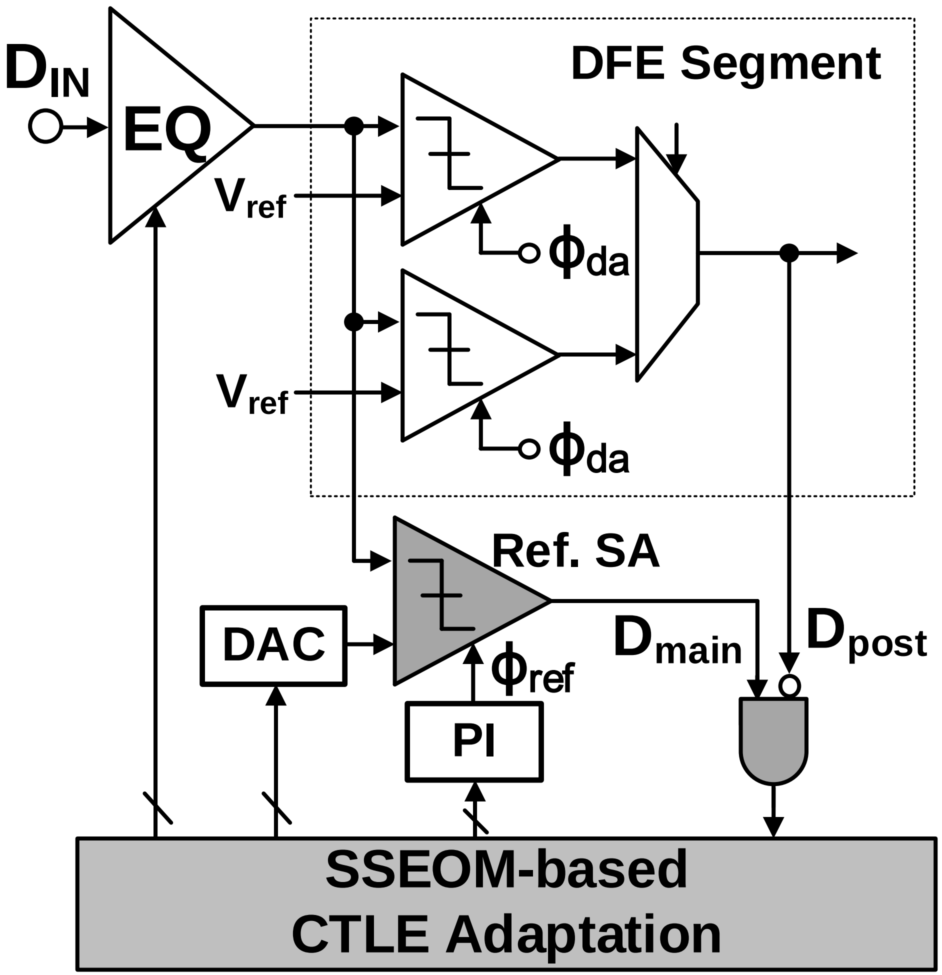
CTLE Adaptation

- **Optimal CTLE boosting gain ➔ Maximize A**
- **Existing DFE ➔ Maximize A of optimally DFE-compensated eye-diagram**
- **Pattern-filtered eye-diagram (Post-tap '0')**



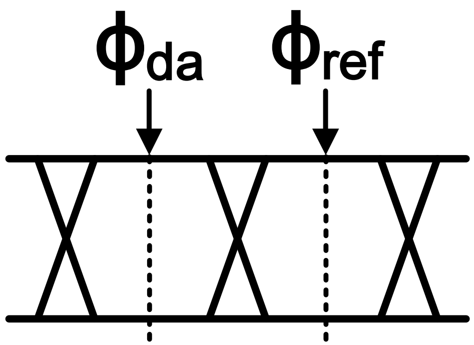
CTLE Adaptation by SSEOM

- **Implementation**



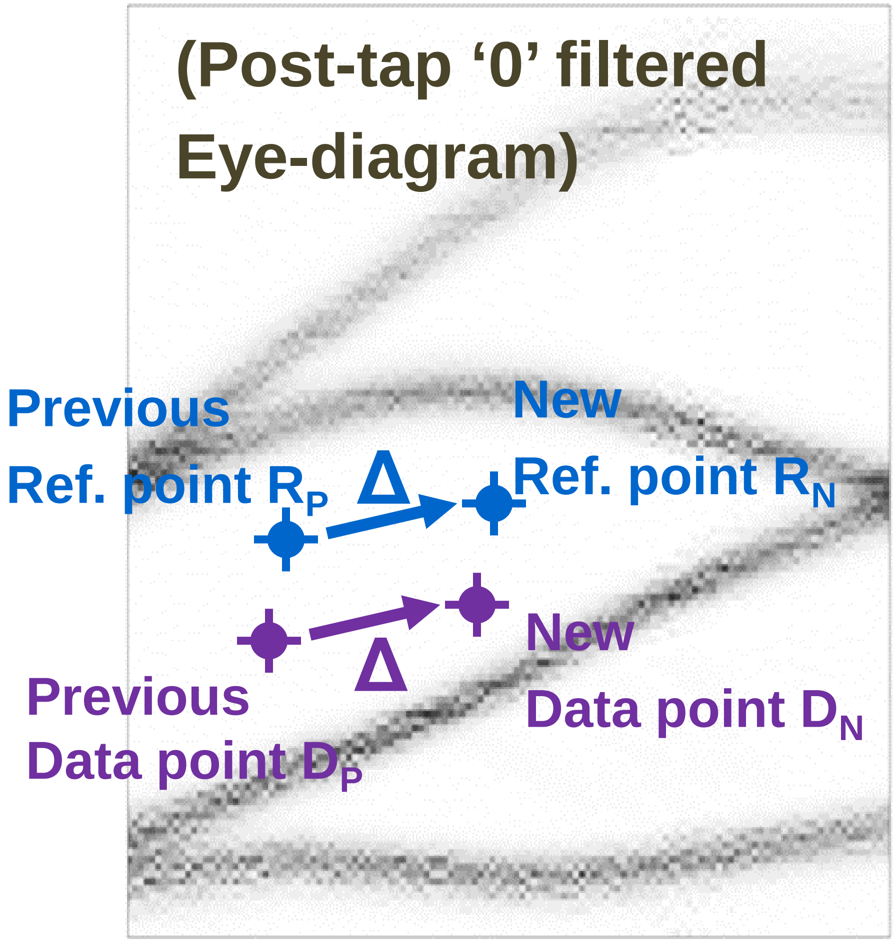
- **Pattern filtering**
  - ✓ Ex) D_{post} = '0'

- **Phase relationship**



Background Adaptation

- **Concept**



- **Opt. point variation**
  - $\Delta = R_N - R_P$
- **New data point**
  - $D_N = D_P + \Delta$
- **Update freq. ≈ 26 Hz**

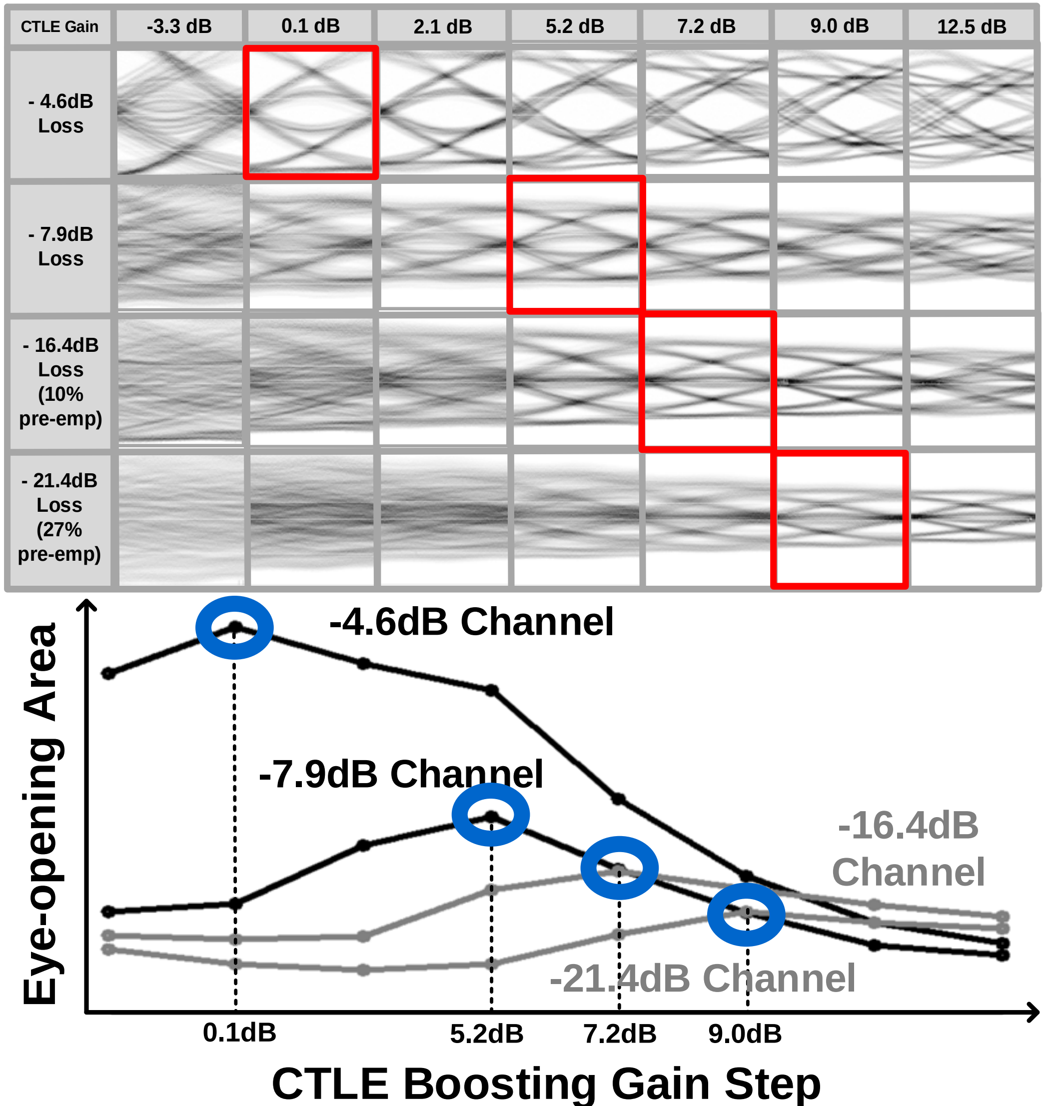
Power-up Sequence

- **DC offset cancellation**
  - Analog front-end & all samplers
- **Clock recovery**
  - Turn on the PLL
- **CTLE adaptation**
  - Pattern filtering by SSEOM
- **DFE adaptation**
  - Optimal sampling point of all data samplers
- **Background adaptation**
  - Monitoring & updating Δ by ref. sampler

Meas. Results of CTLE Adpt.

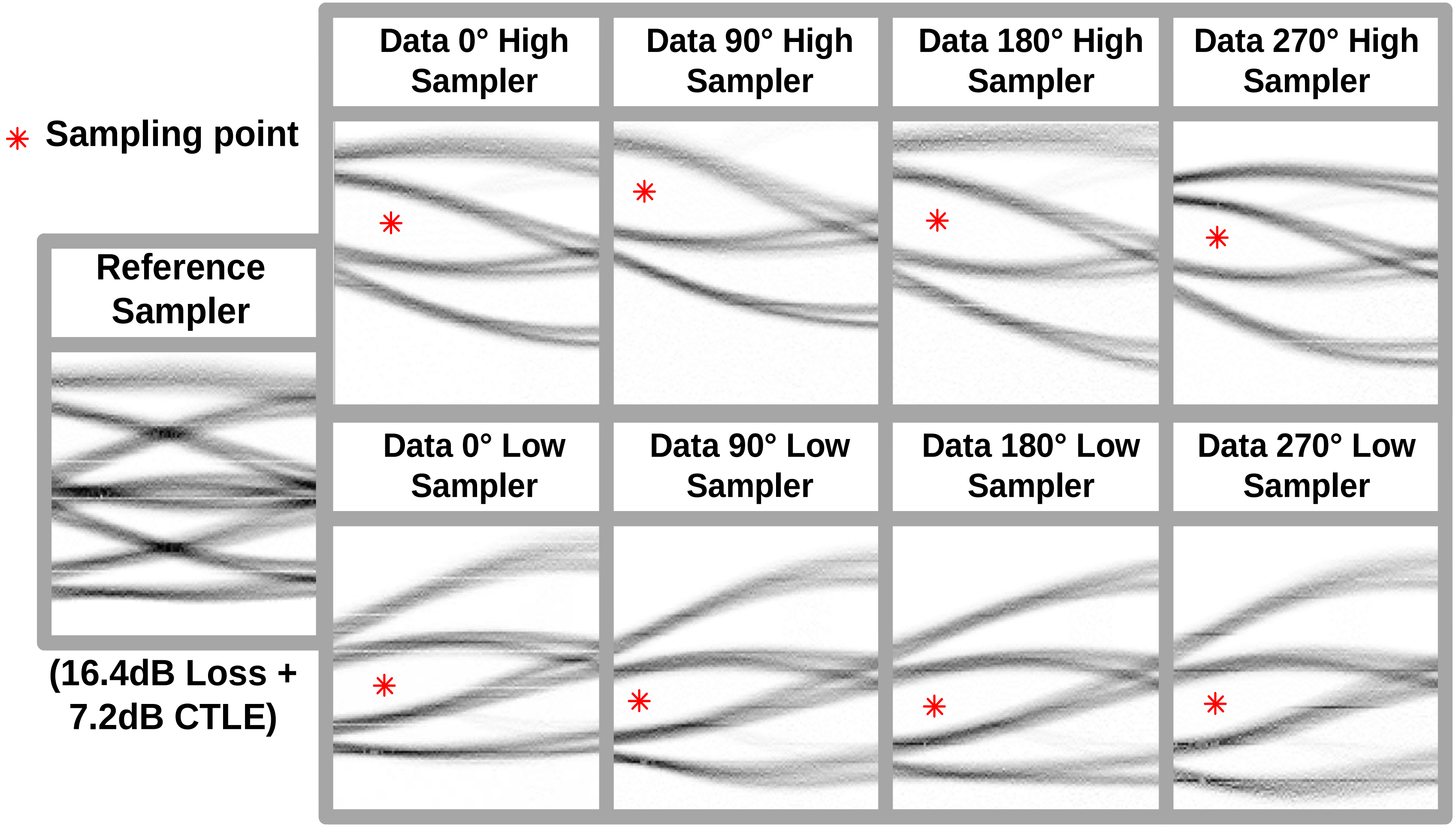
- Internal eye-monitor results of the CTLE output

- Plots of the corresponding eye-opening area



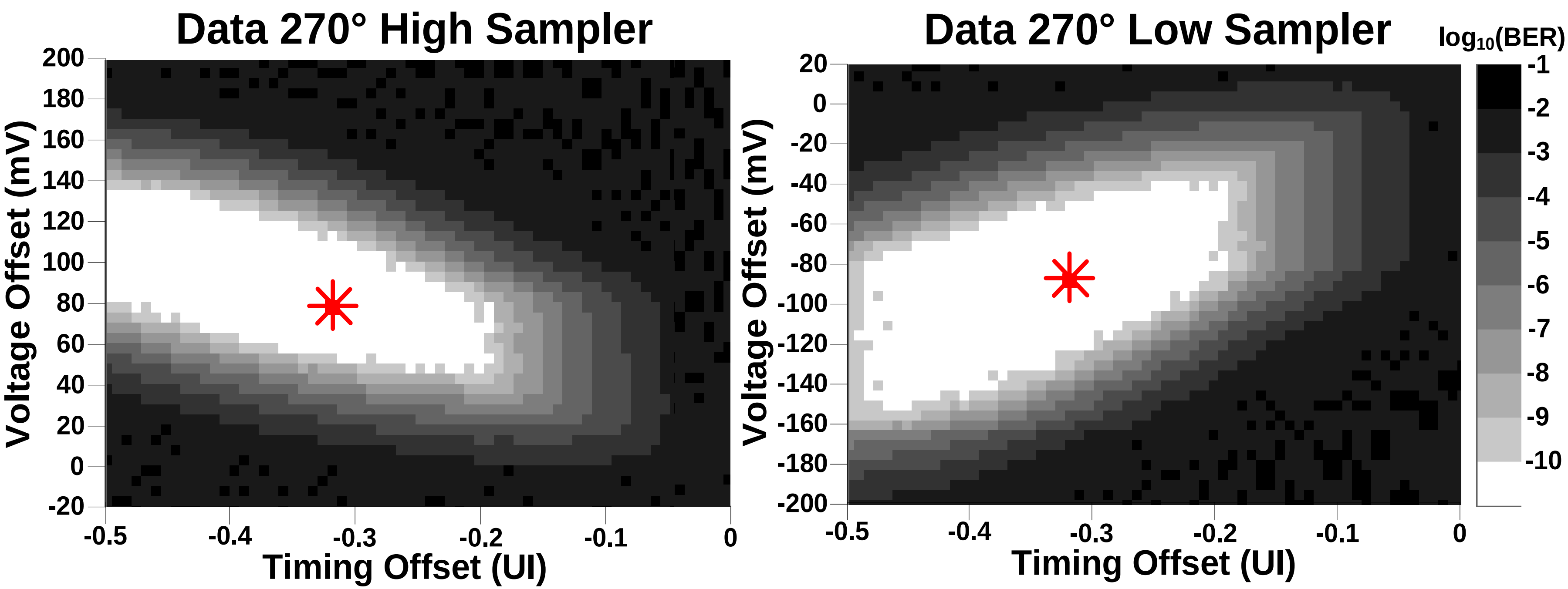
Measured Results of DFE Adpt.

- **Found optimal sampling point of each sampler**



Measured Results of DFE Adpt.

- BER contour of 270° data samplers



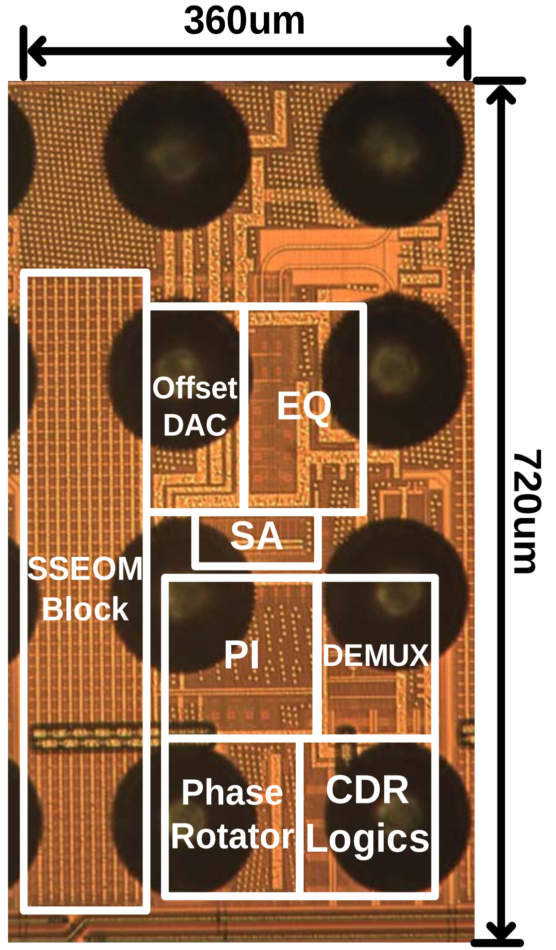
- Total run time : 364ms

Comparison & Die Photo

- **Comparison**

	Algorithm	Adaptive Equalizer	Sampling Point	Backg. Adpt.	On-chip
V. Balan	Sign-sign LMS	CTLE, FIR/IIR-DFE	I/Q phase	Yes	Yes
V. Stojanovic	Pattern filtering	FIR-DFE	-	Yes	Yes
E.-H. Chen	Pseudo-BER	TX-FFE, RX-DFE	Edge phase	Yes	Yes
C.-K. Seong	Pattern filter histogram	FIR-DFE	-	-	No
Y. Hidaka	Pattern matching	CTLE, FIR-DFE	Decision thre.	Yes	Yes
D. Dunwell	Slope of PDF	CTLE	Decision thre.	No	No
W.-S. Kim	Asynchronous sampling	CTLE	-	No	Yes
This Work	**SSEOM**	**CTLE, FIR-DFE**	**Dcs. thre., Multiphase**	**Yes**	**Yes**

- **Die photo**



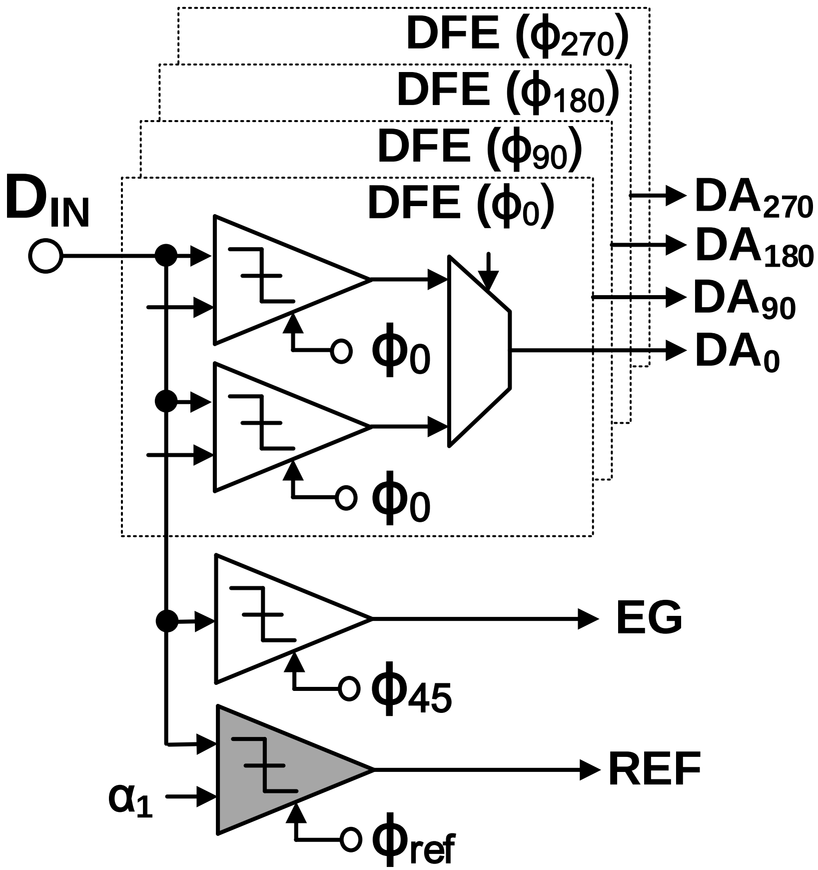
Summary

- CTLE & DFE adaptation
- Optimal sampling point
- Background adaptation
- Fully-integrated and fast run-time
- Suitable for area-sensitive low-power parallel I/O designs
- PAM signaling (PAM4 / PAM8)

Thank You!

(Appendix) Clock Recovery

- **Data/Edge sampling**



- **Bang-bang logic**

Normal
$$UP = DA_{270} \cdot DA_0 \cdot EG \cdot \overline{DA_{90}}$$
$$DN = DA_{270} \cdot DA_0 \cdot \overline{EG} \cdot \overline{DA_{90}}$$

ϕ_0 Adpt.
$$UP = DA_{270} \cdot REF \cdot EG \cdot \overline{DA_{90}}$$
$$DN = DA_{270} \cdot REF \cdot \overline{EG} \cdot \overline{DA_{90}}$$

ϕ_{90} Adpt.
$$UP = DA_{270} \cdot DA_0 \cdot EG \cdot \overline{REF}$$
$$DN = DA_{270} \cdot DA_0 \cdot \overline{EG} \cdot \overline{REF}$$

- **Phase relationship**

Normal : ϕ_{270} ϕ_0 ϕ_{45} ϕ_{90}

ϕ_0 Adpt. : ϕ_{270} ϕ_{ref} ϕ_{45} ϕ_{90}

ϕ_{90} Adpt. : ϕ_{270} ϕ_0 ϕ_{45} ϕ_{ref}