Paper # 15-6

A 0.622-10Gb/s Inductorless Adaptive Linear Equalizer with Spectral Tracking for Data Rate Adaptation in 0.13-μm CMOS

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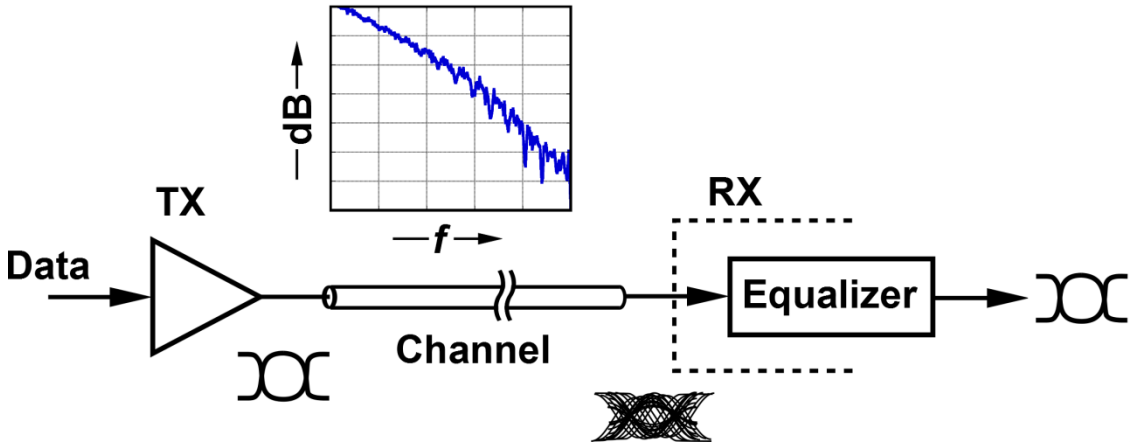
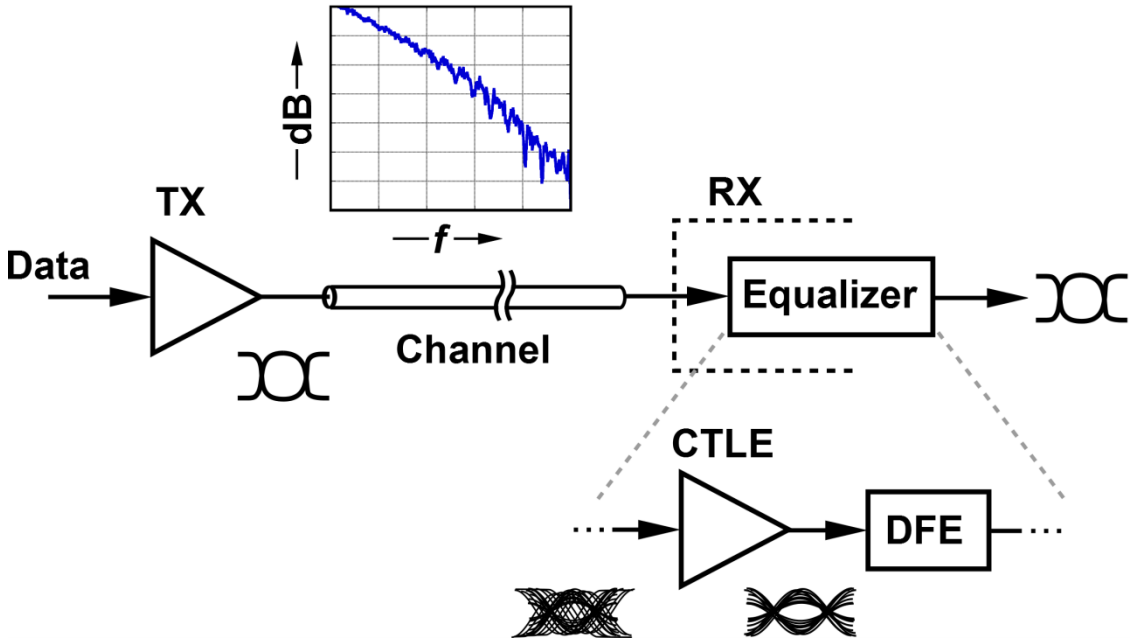
OUTLINE

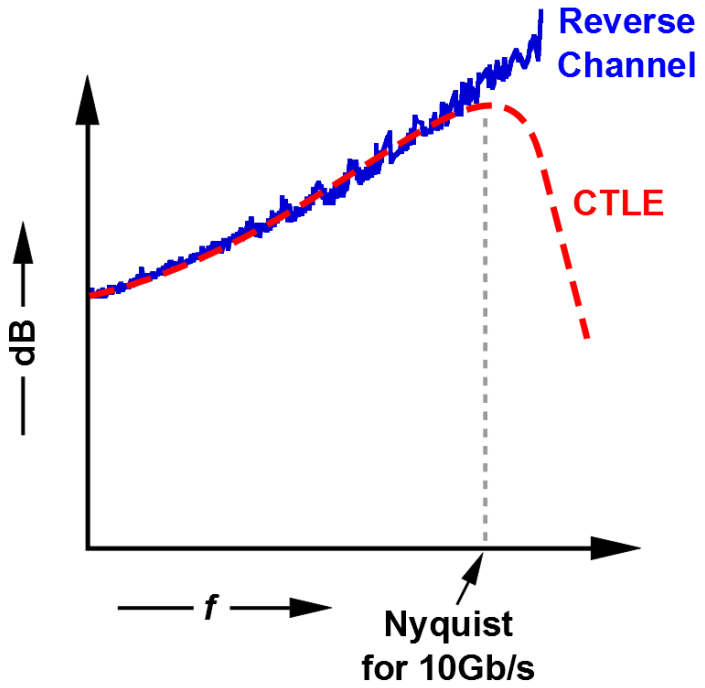
- Introduction
- Adaptive Linear Equalization
- Data Rate Adaptation
- Proposed Architecture
- Simulation and Measurement Results
- Conclusion

INTRODUCTION



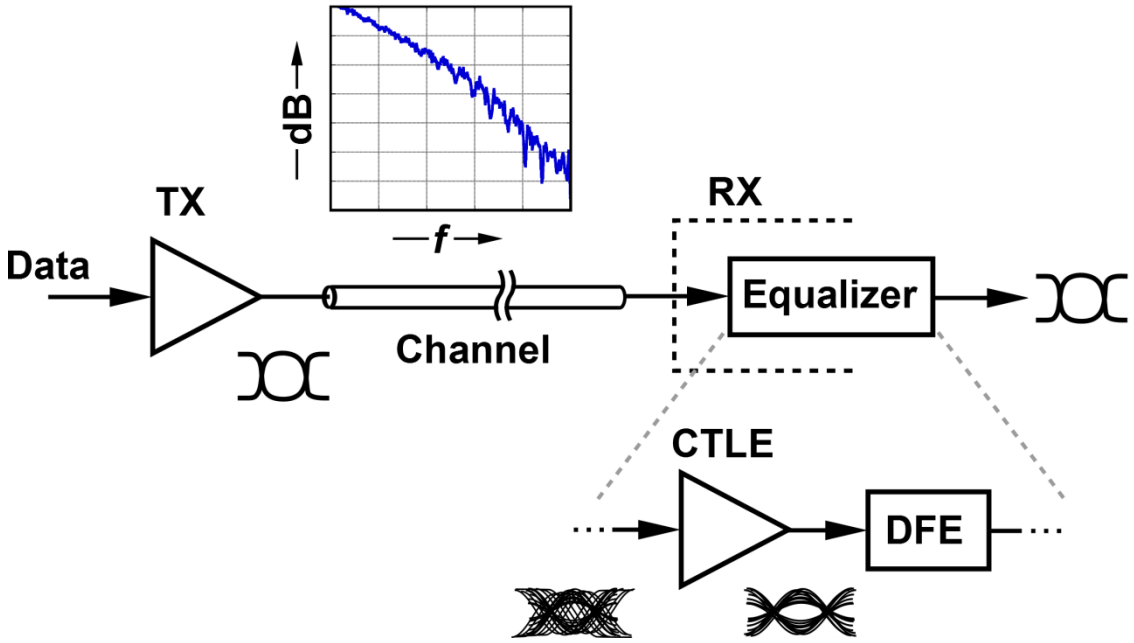
INTRODUCTION

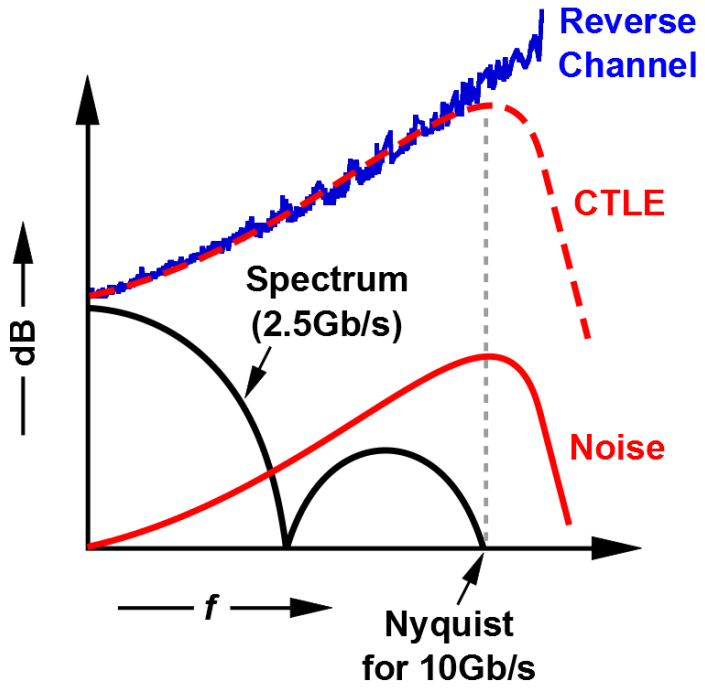




- CTLE relaxes equalization load of DFE
- I/O links may operate at different data rates

INTRODUCTION





- CTLE reduces equalization effort of DFE
- I/O links may operate at different data rates
- Adaptive CTLE for a fixed rate is not optimized

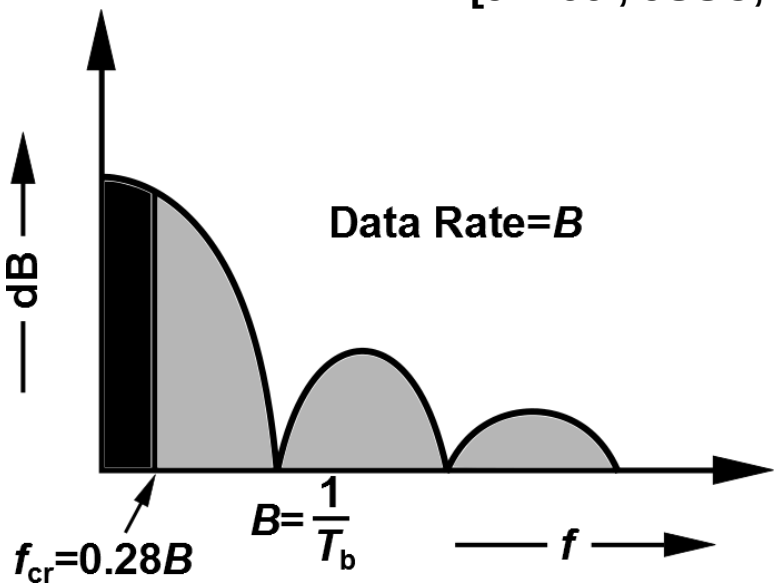
SPECTRAL BALANCING

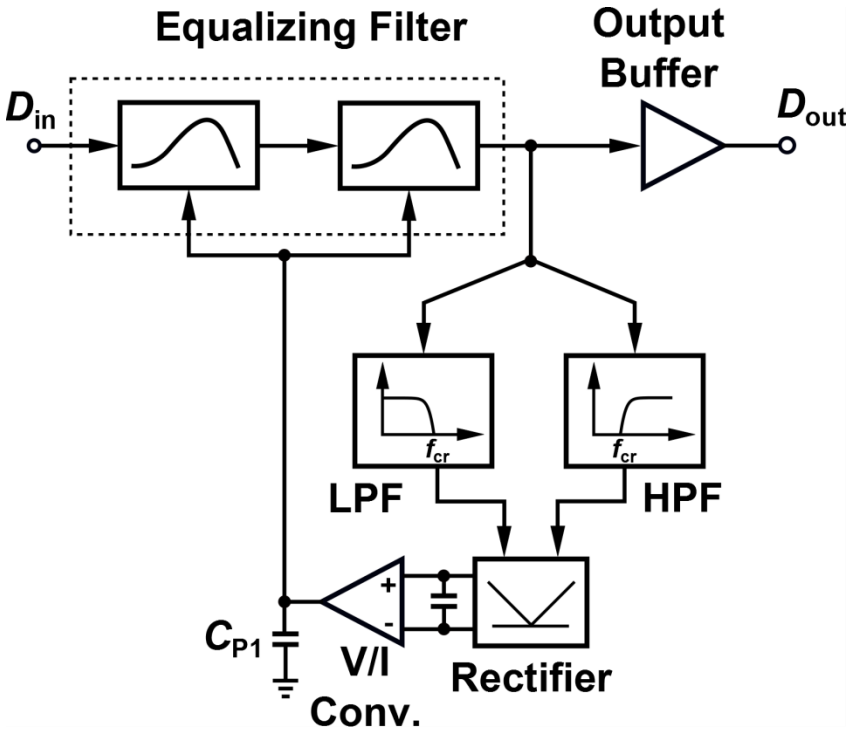
$$S_x(f) = T_b\left[\frac{Sin(\pi f T_b)}{\pi f T_b}\right]^2$$

$$\int_0^{f_{cr}} S_x(f)df = \int_{f_{cr}}^{\infty} S_x(f)df$$

Solving, $f_{cr} = \frac{0.28}{T_b}$

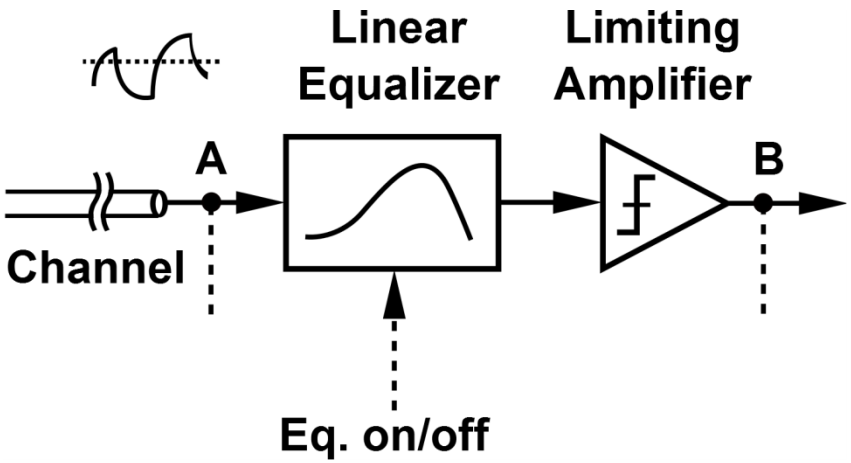
[J. Lee , JSSC,'06]

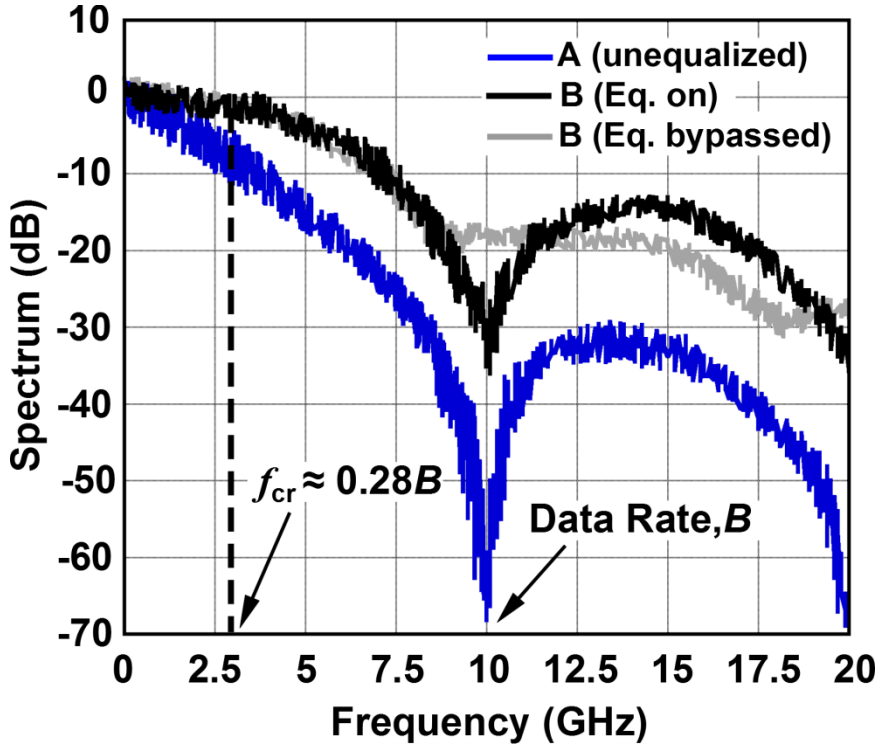




- Energy equated across f_{cr}
  - Fixed data rate
  - High BER for lower rates!

SLICING UN-EQUALIZED DATA





Spectral resemblance of pure and sliced PRBS

+

Main lobe contains 90% power

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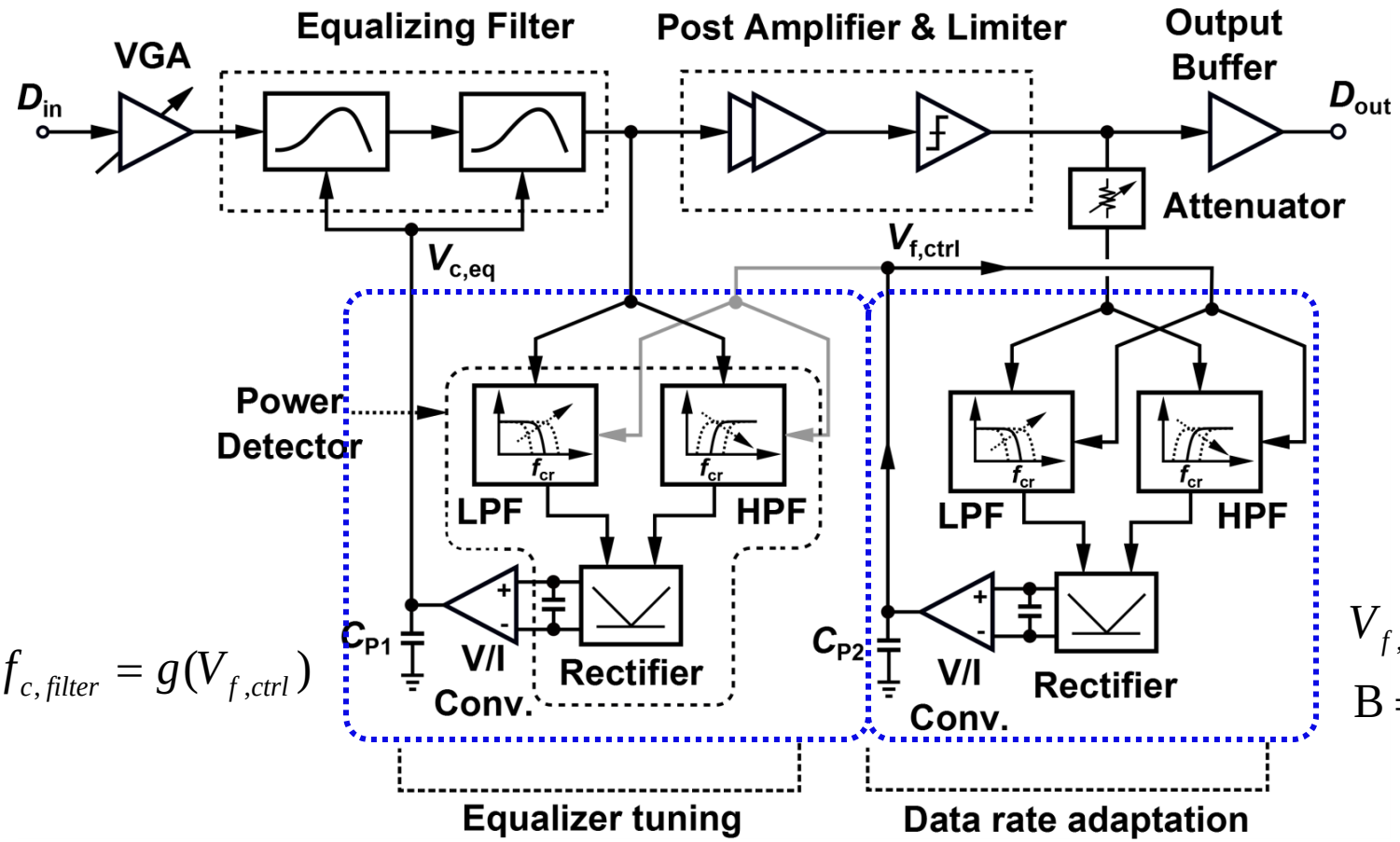
$f_{cr} \approx 0.28B$, even if sliced after imperfect equalization

EQUALIZER ARCHITECTURE



$$f_{c,filter} = g(V_{f,ctrl})$$

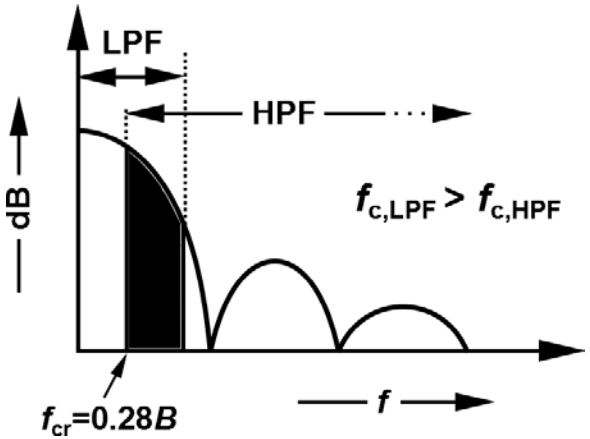
$$V_{f,ctrl} = f(B);$$

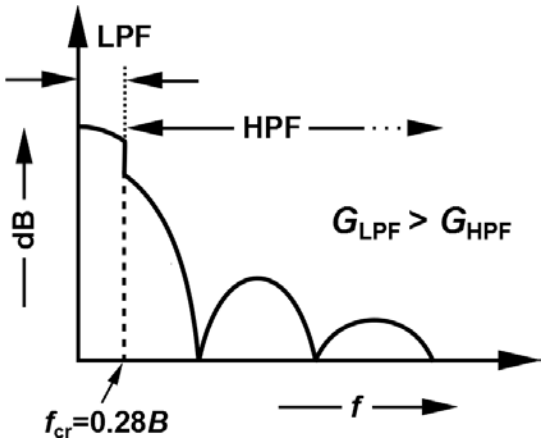
B = Data Rate

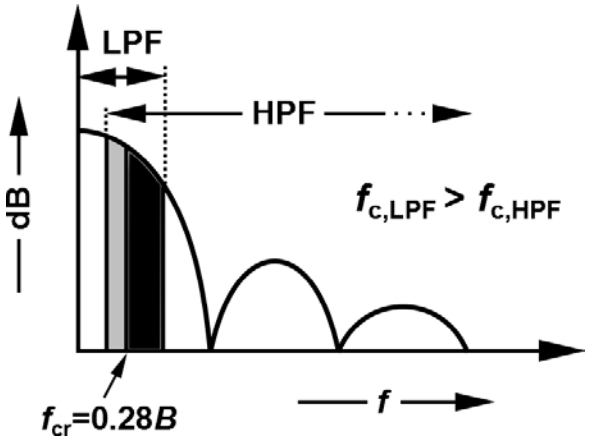
$$g \equiv f^{-1}$$

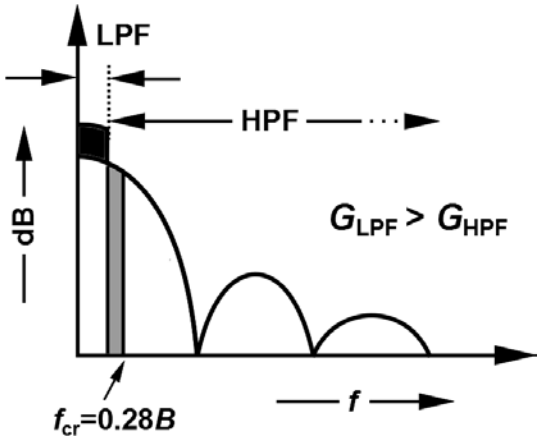
$$\Rightarrow f_{cr} \approx 0.28B$$

FILTER MISMATCH



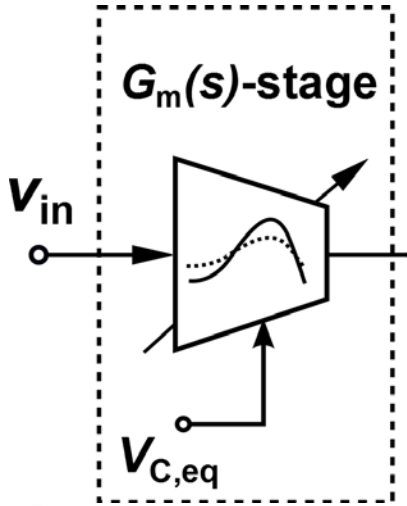


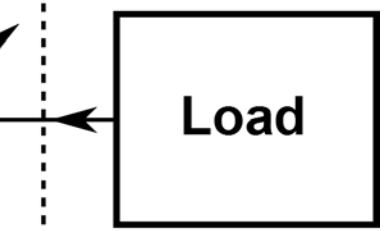


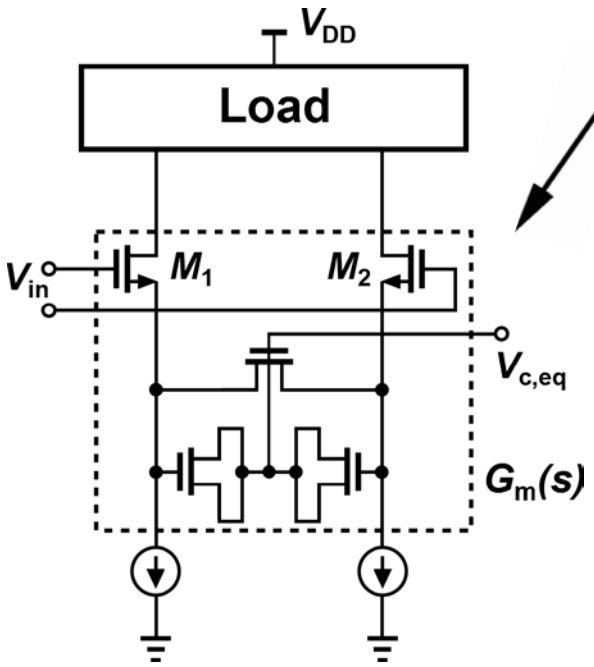


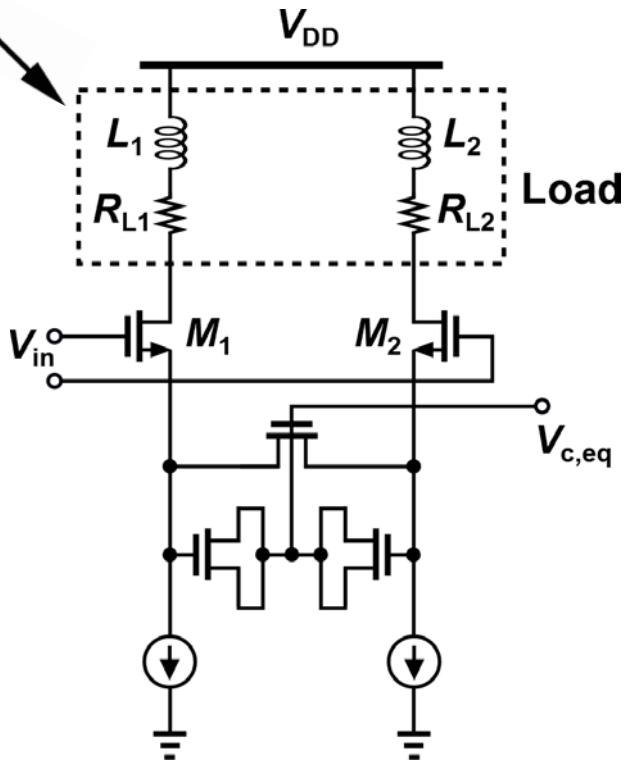
- **Filter Gain/BW mismatch**
  - **Loop adjusts f_c**
  - **Power equality restored**

EQUALIZING FILTER



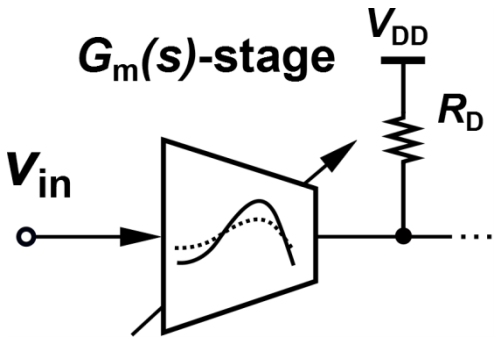




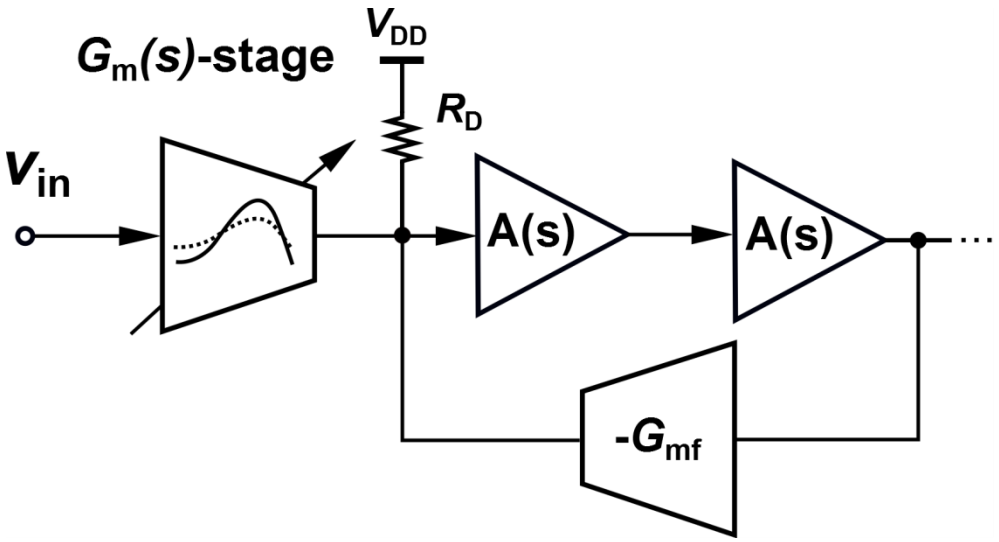


- **Capacitive deg.**
- **Resistive loading**
  - **Gain boosting**
  - **BW**
  - **DC gain**
- **Shunt peaking**
  - **Large area**

CAN WE MODIFY THE LOADING?

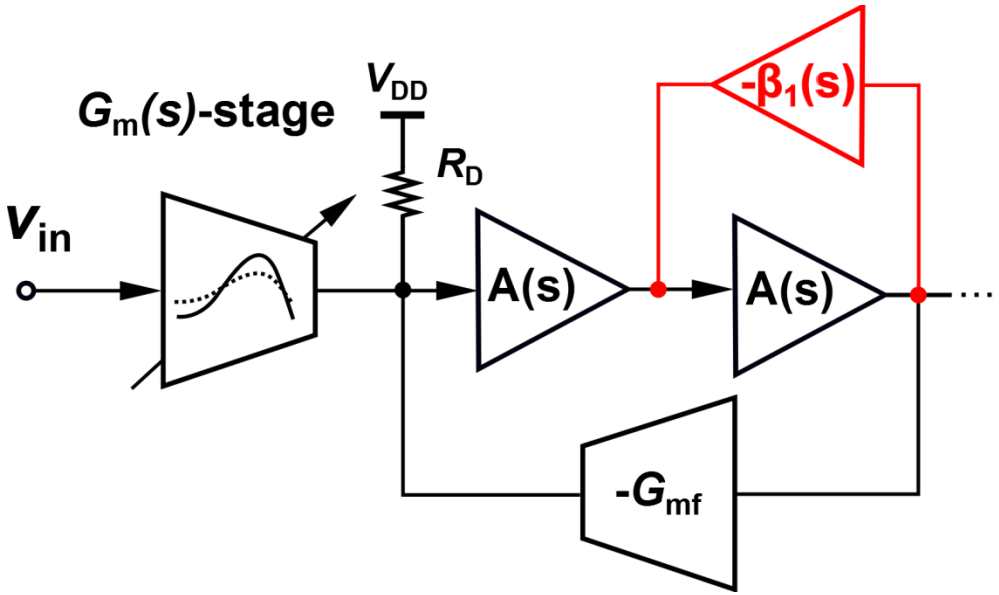


3RD-ORDER FEEDBACK



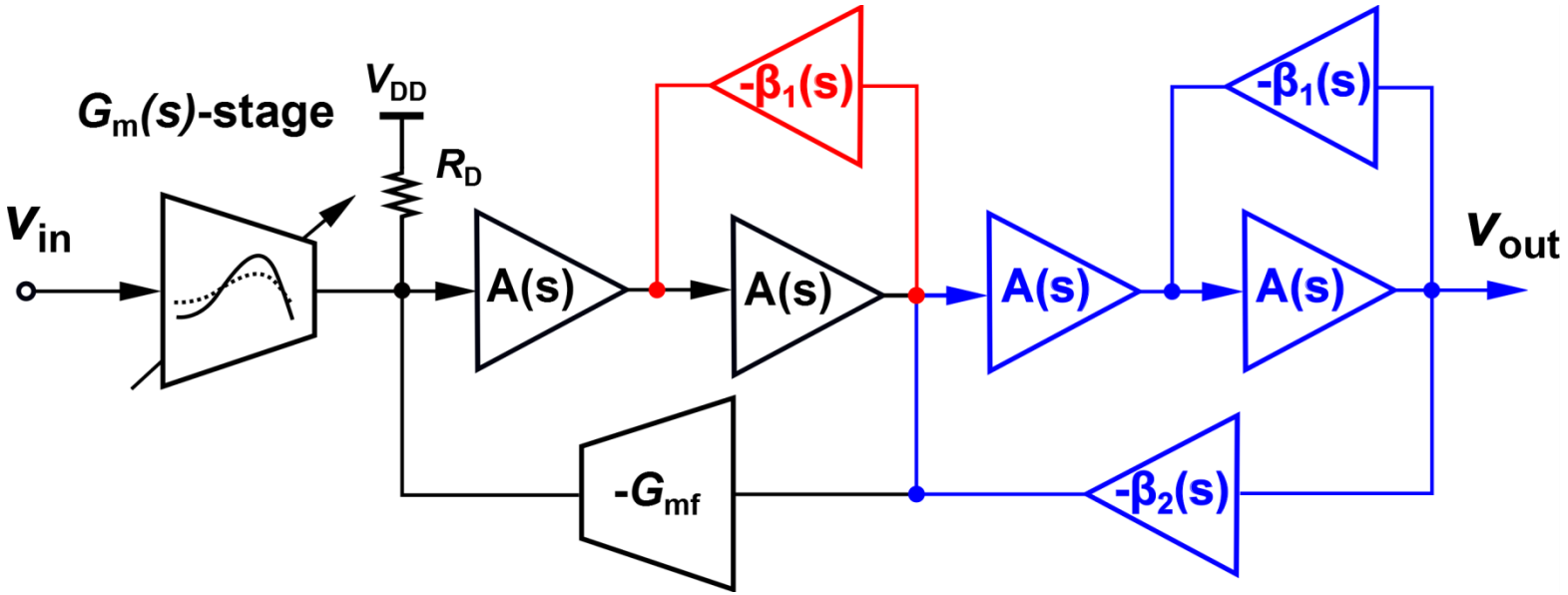
- **Core bandwidth limitation**
- **High jitter**

3RD-ORDER NESTED FEEDBACK



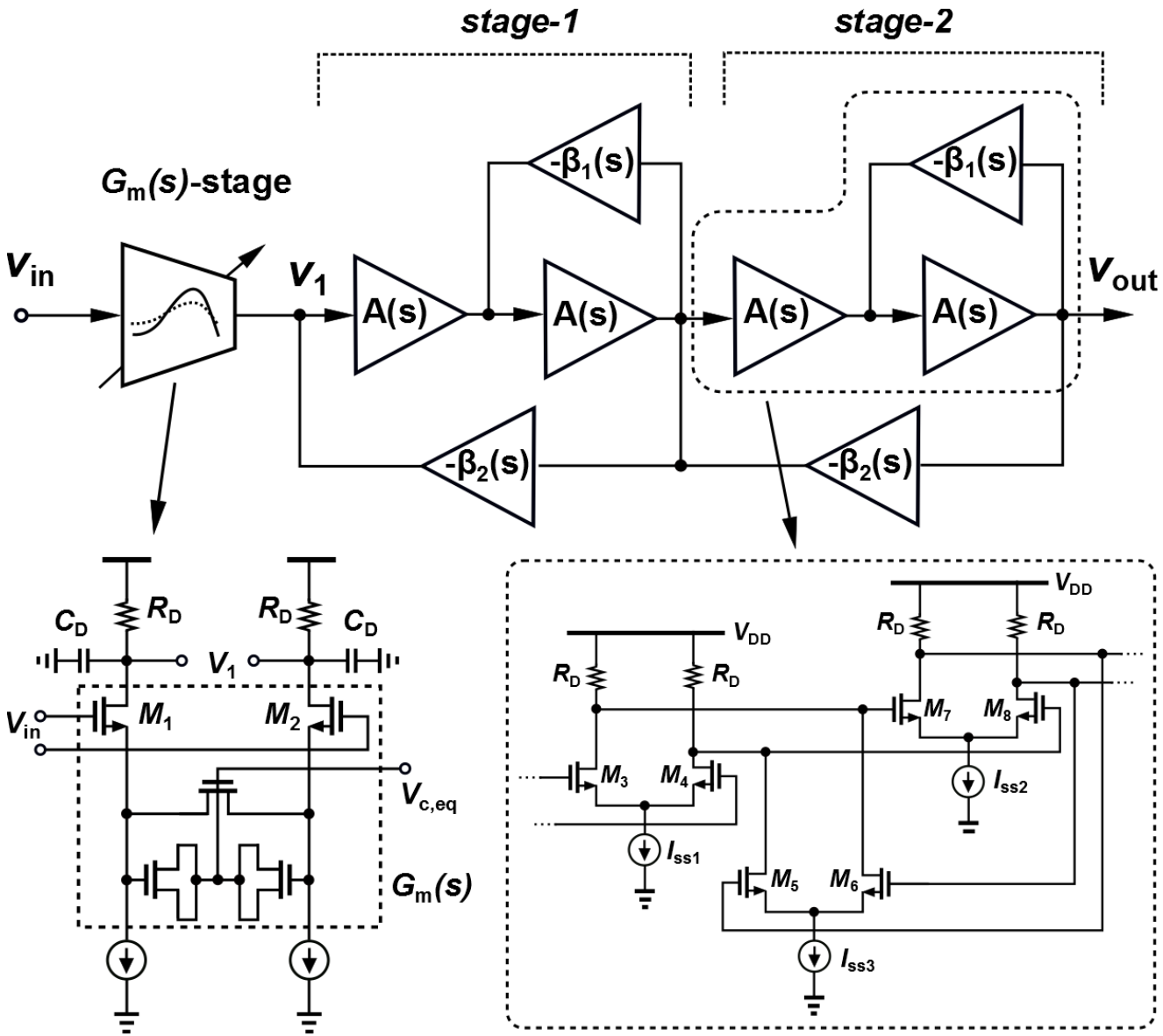
- $\beta_1(s)$ increases BW of core stage
- Feedback gain can be higher

SECONDARY LOADING

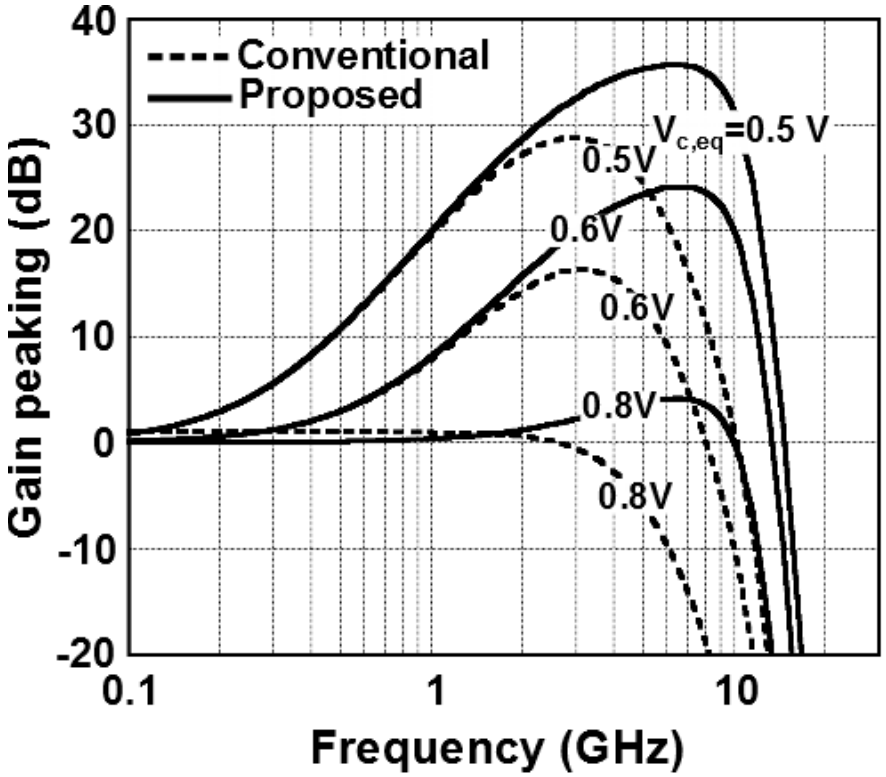


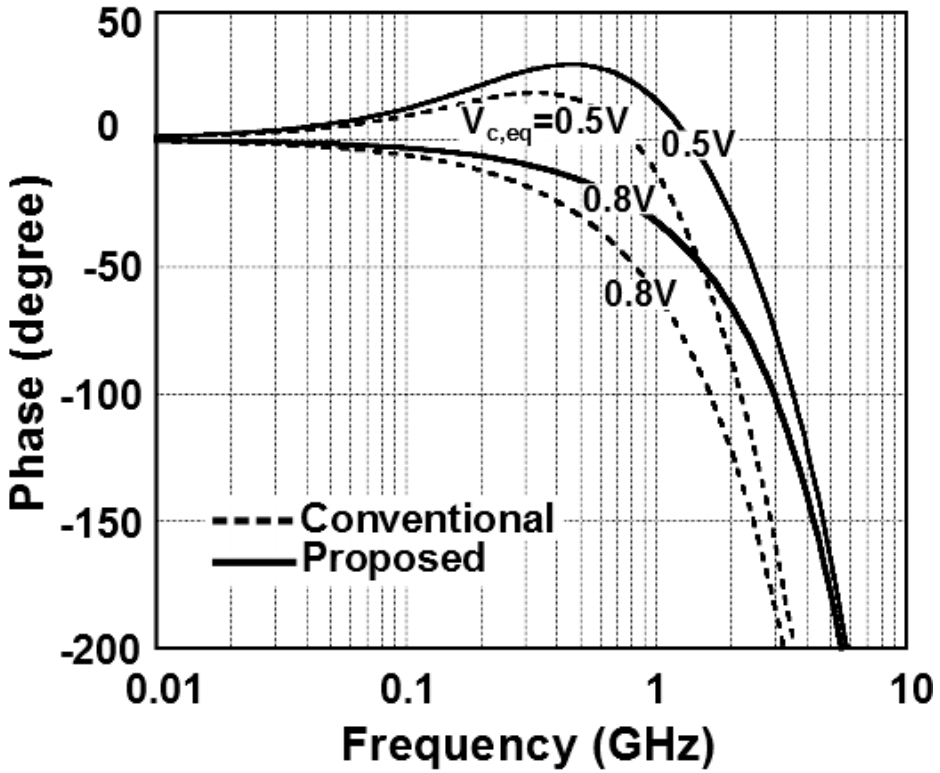
- $\beta_1(s)$ increases BW of core stage
- Feedback gain can be higher
- reduces transient jitter
- improves DC gain

COMPLETE EQUALIZER



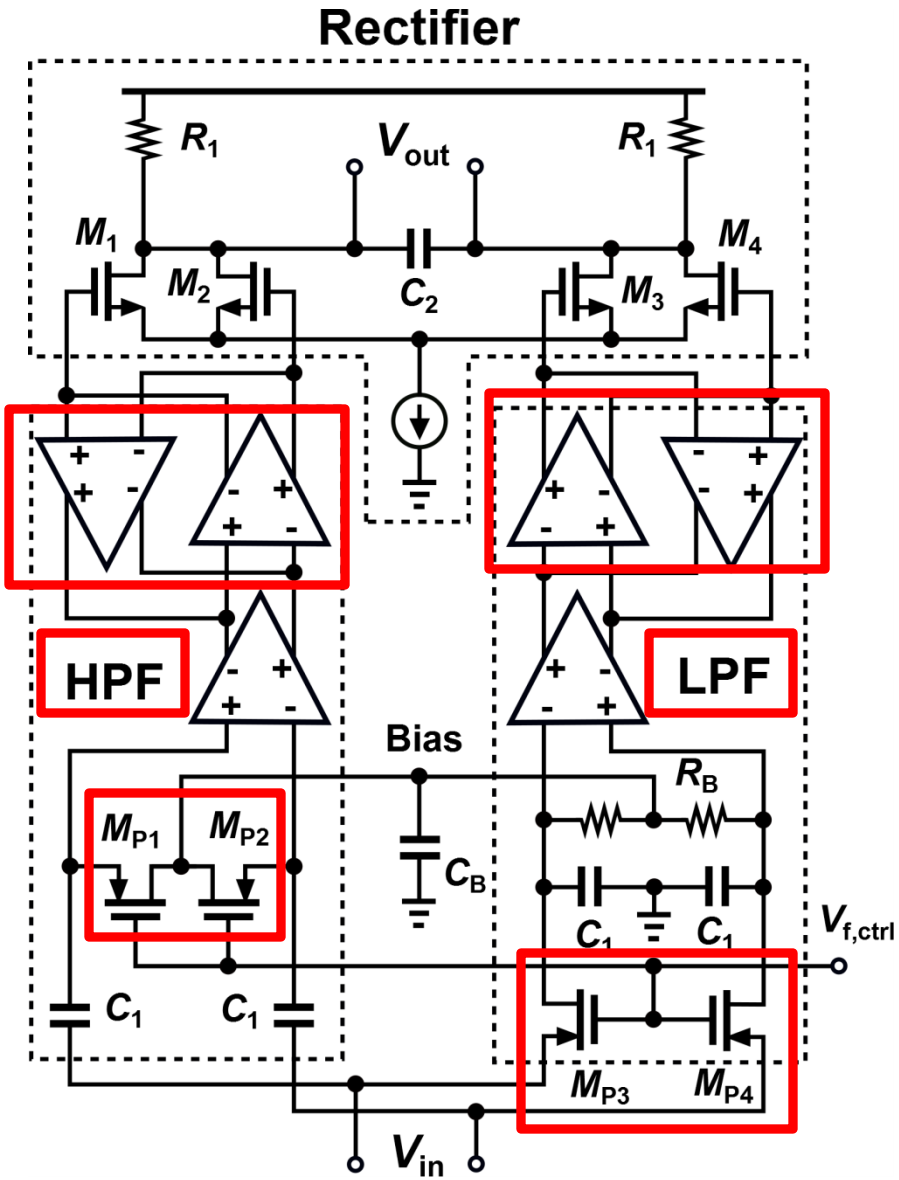
SIMULATION





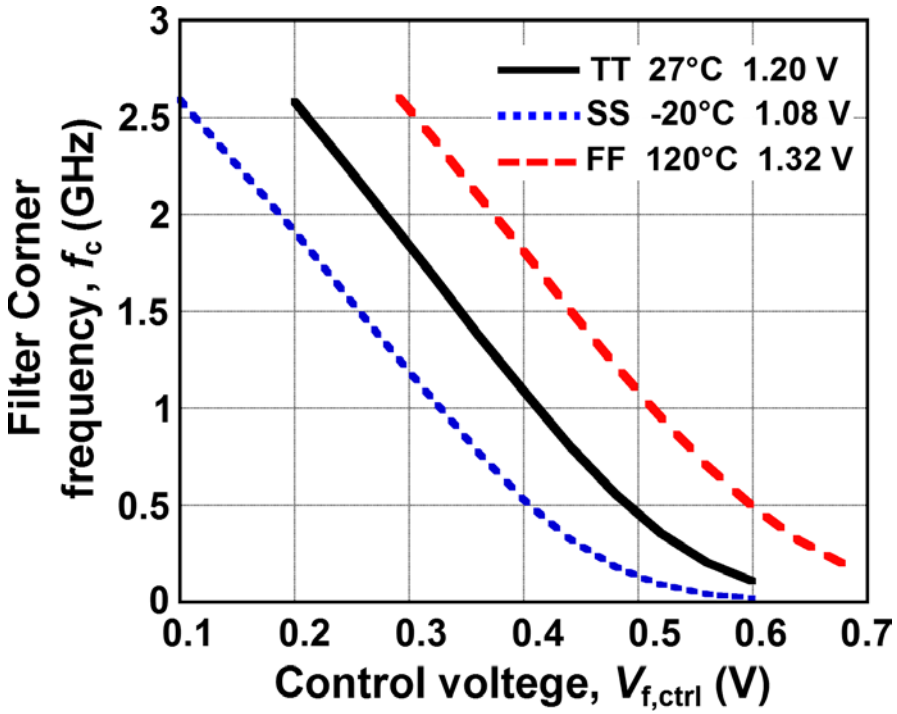
- **Higher peaking and phase compensation**
- **Higher bandwidth**

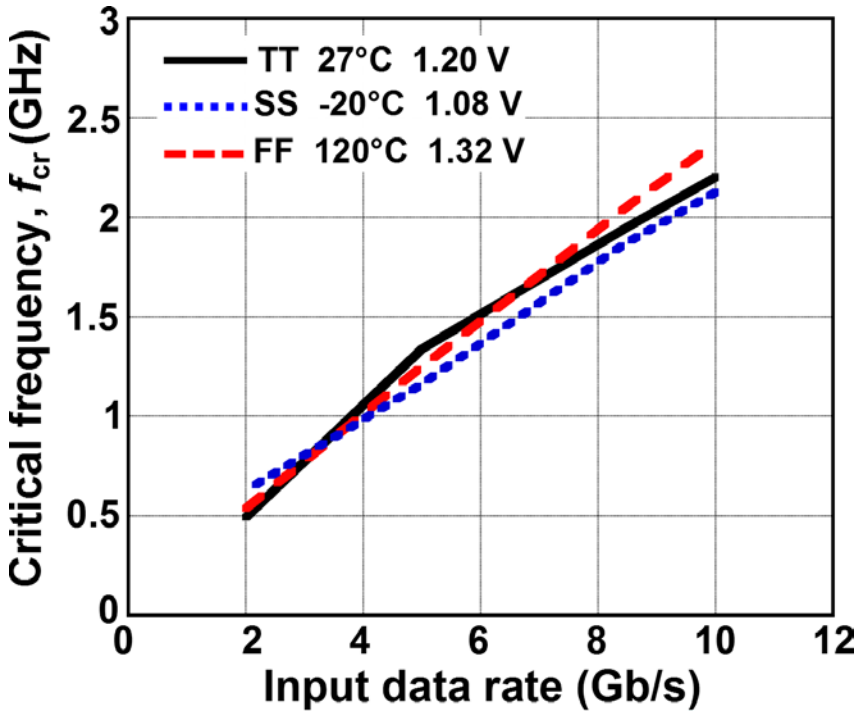
TUNABLE FILTER & RECTIFIER



- HF & LF power detector
- 100's of MHz to 2.8GHz
- PMOS for tuning
- 2nd-order amplifier

SIMULATION





PVT variation effects filter control curve

+

$V_{f,ctrl}$ experiences complementary variations

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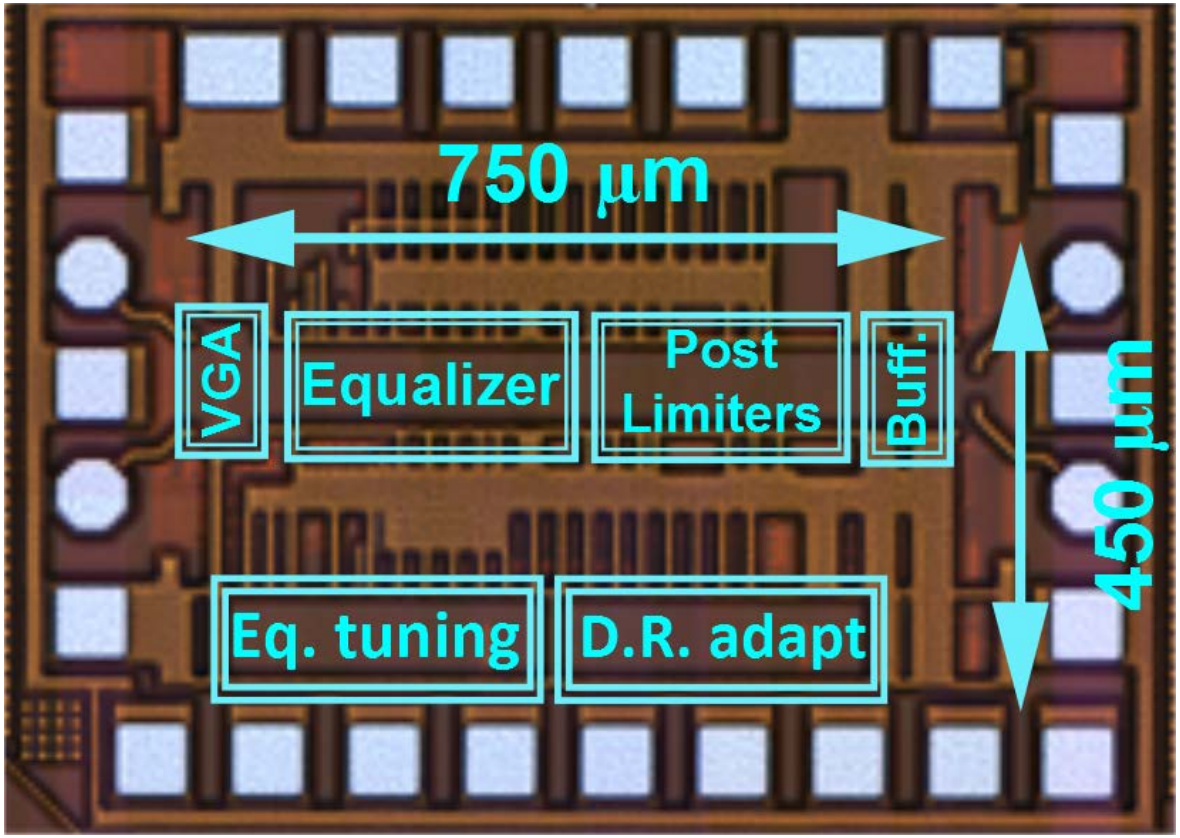
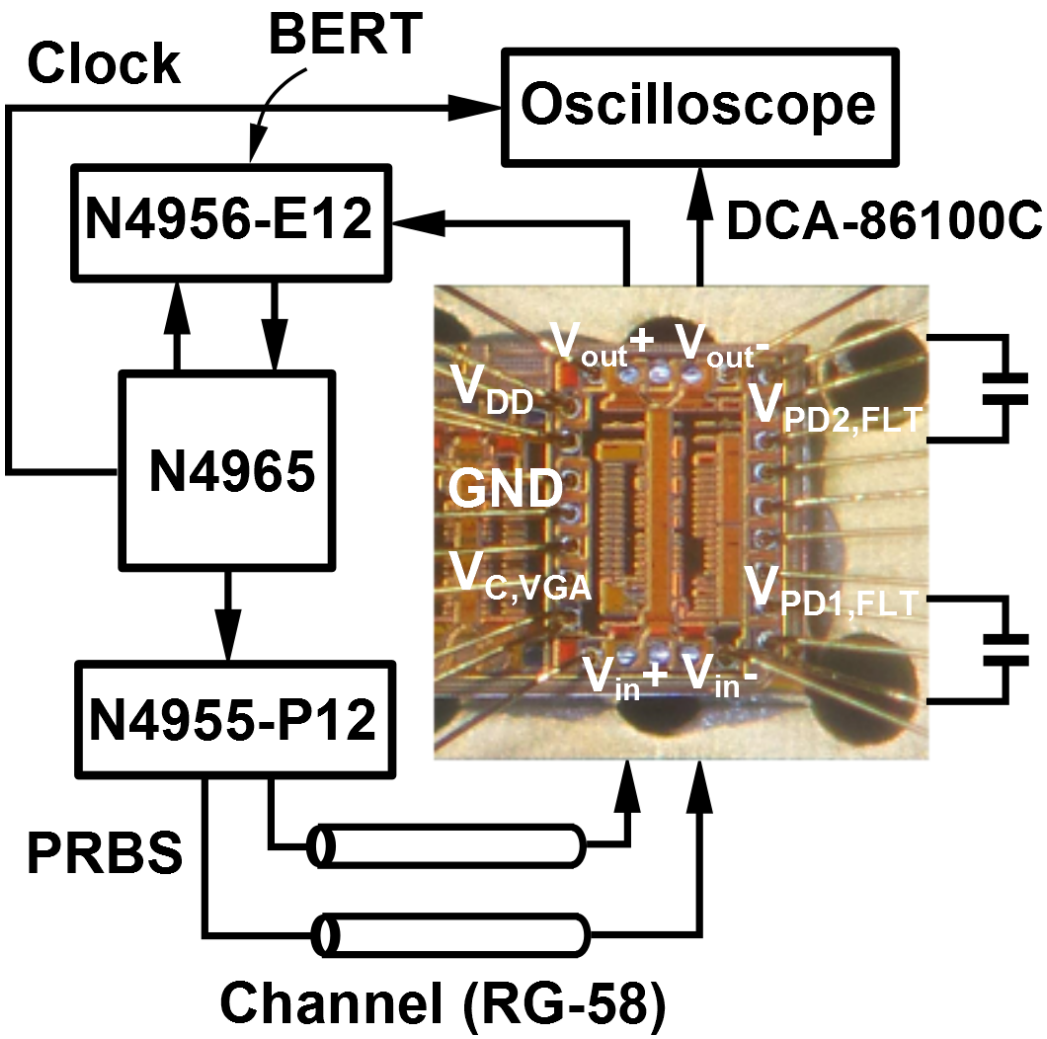
Identical blocks → variation compensated ($g = f^{-1}$)

DIE MICROGRAPH



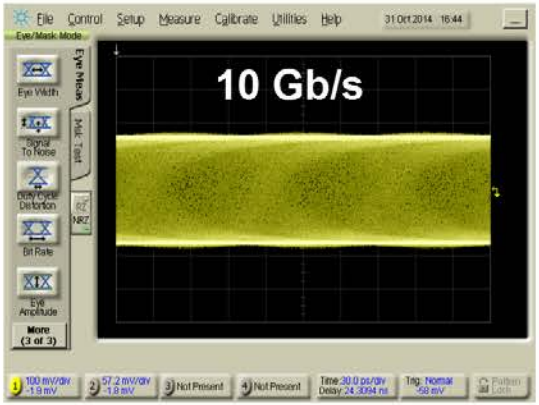
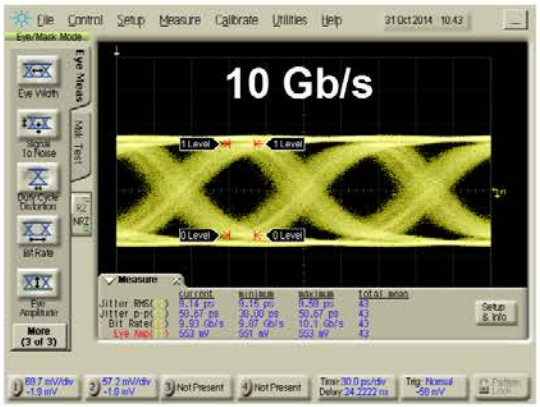
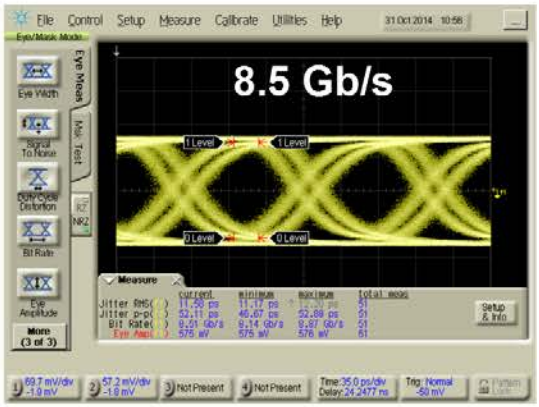
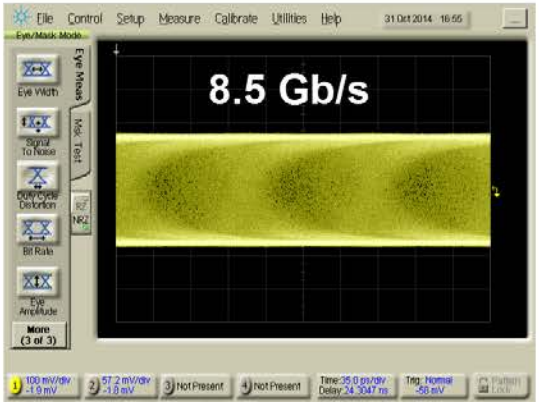
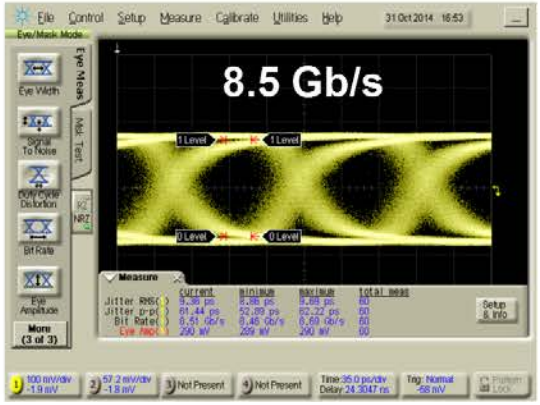
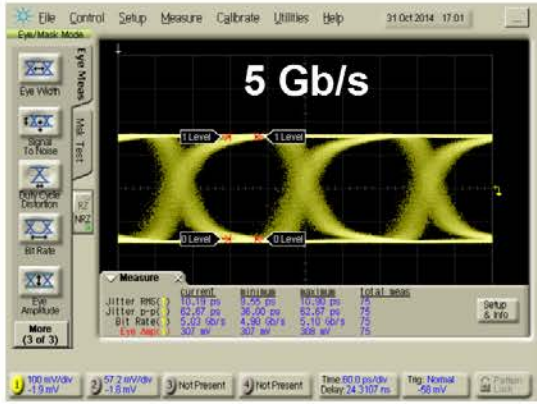
- **Fabricated in IBM-0.13µm CMOS technology**
- **V_{DD}=1.2 V**

MEASUREMENT SETUP



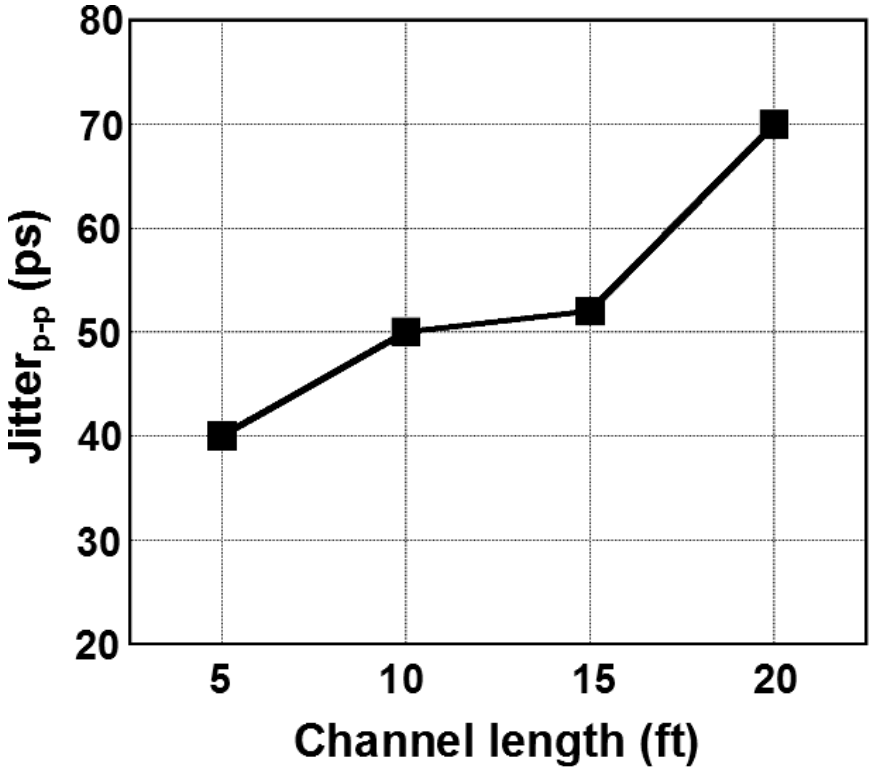
- RG-58 as channel
- Data rate swept for each length
- No change of bias or circuit condition

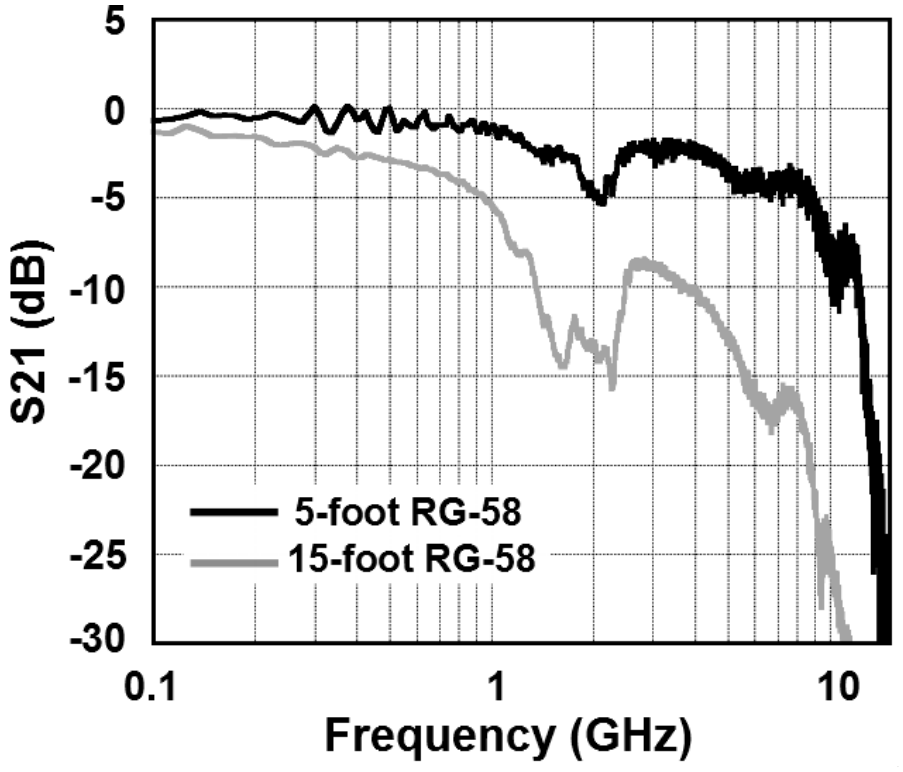
MEASURED EYE DIAGRAMS

	Equalizer off	Equalizer on	Equalizer on
15ft RG-58			
20ft RG-58			

- **Rate & Channel adaptation settings unchanged**
- **Constant BER (<10^{-12}) for different channel & data rates**

MEASUREMENT RESULTS





PERFORMANCE SUMMARY

Parameter	JSSC,'06	ISSCC,'05	TCAS-II,'10	This Work
Technology	0.13-μm CMOS	0.13-μm CMOS	0.18-μm CMOS	0.13-μm CMOS
Data Rate	20 Gb/s	10 Gb/s	2~6.4 Gb/s	0.622~10 Gb/s
Inductors	Yes	Yes	No	No
Multi-rate	No	No	Yes	Yes
Jitter	14 ps,pp	20 ps,pp	41 ps,pp	9.5 ps, rms
Peaking Gain	15dB @10GHz	20dB @5GHz	12dB @3.2GHz	15dB @5GHz
BER	10^{-15} @20Gb/s(1)	N/A	10^{-12}	10^{-12}
Supply	1.5 V	1.2 V	1.8 V	1.2 V
Power	60 mW	25 mW	85 mW	130 mW(2)
Area (mm^2)	0.8x0.25	0.45x0.36	0.63x0.55	0.75x0.45(2)

(1): BER increases at lower data rates.

(2): including VGA and limiting amplifier.

CONCLUSION

- **Adaptive equalizer in CMOS technology needed for low cost/high performance wireline receiver**
- **Inductorless design attractive for area efficient/ moderate speed implementation**
- **Architecture for PVT robust adaptive equalization with data rate adaptation presented**
- **A10Gb/s CMOS equalizing filter without using inductors proposed in 0.13-μm CMOS**

ACKNOWLEDGEMENT

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Thank You !!