A 190mW 40Gbps SerDes Transmitter and Receiver Chipset in 65nm CMOS Technology

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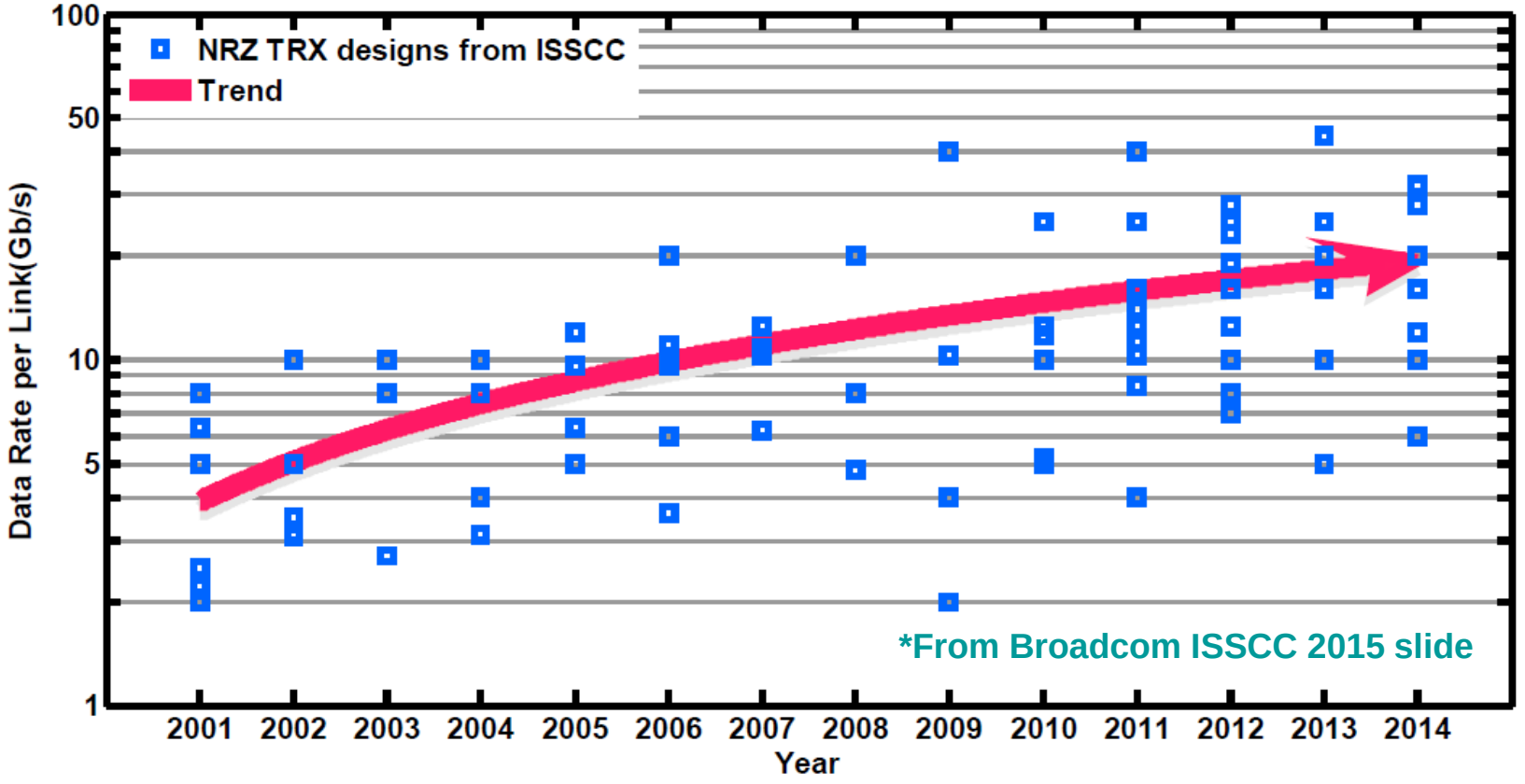
Outline

- Background
- Receiver architecture and design techniques
- Transmitter architecture and design techniques
- Measurement results
- Conclusion

Background

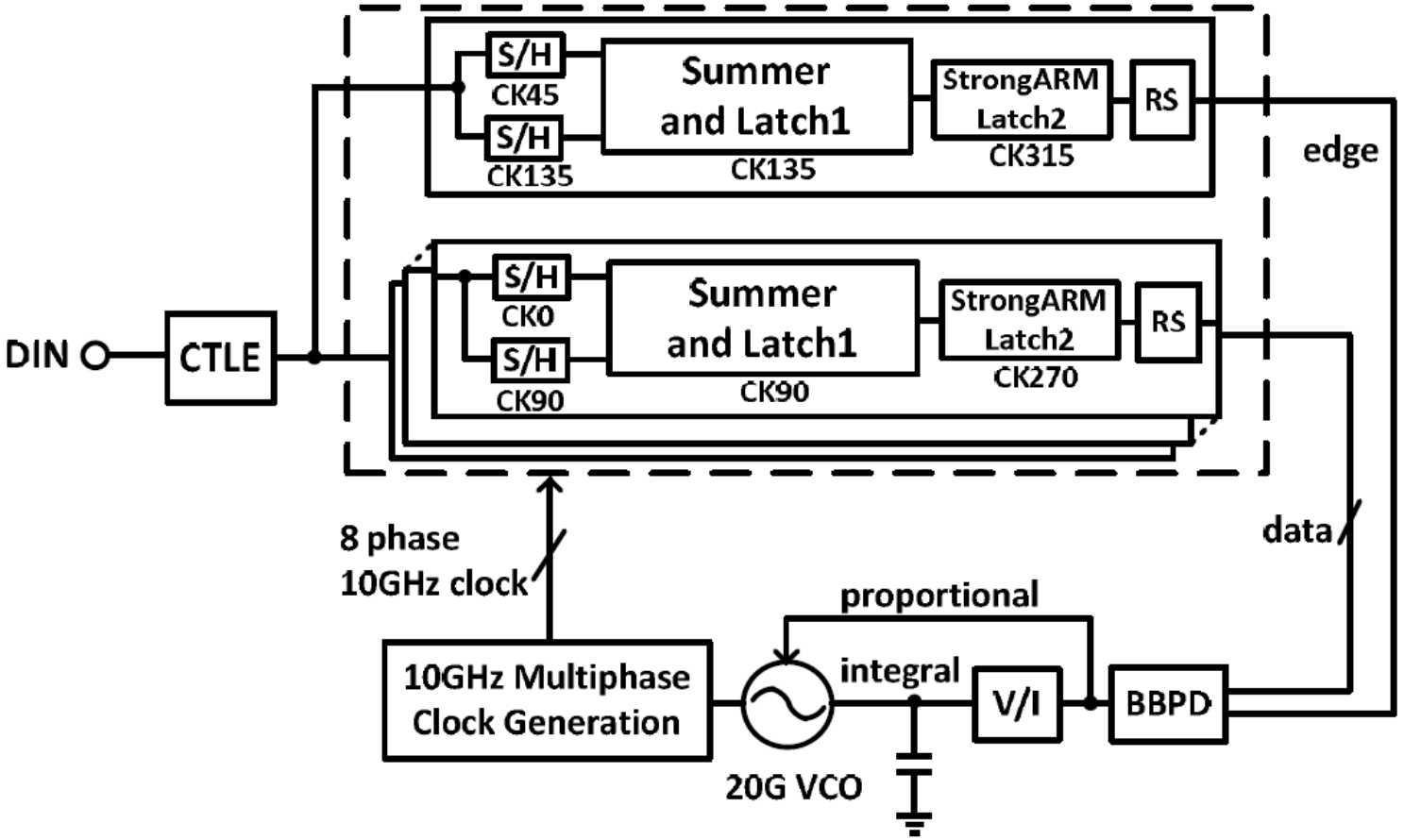


- Standards and applications such as OC-768, OUT-3, 400GbE and so on demand TRX to support data rate around and even beyond 40Gb/s.

Problems and Design Target

- Problems:
- TX timing hard to meet under PVT variation
- FFE: 1UI delay is difficult to generate
  - FFE based on transmission line: power and area penalty
  - FFE based on flip-flop: power penalty, large CK-Q delay
- CDR stability issue
- High power consumption
- Design target: Low power 40Gb/s transceiver for short range communication

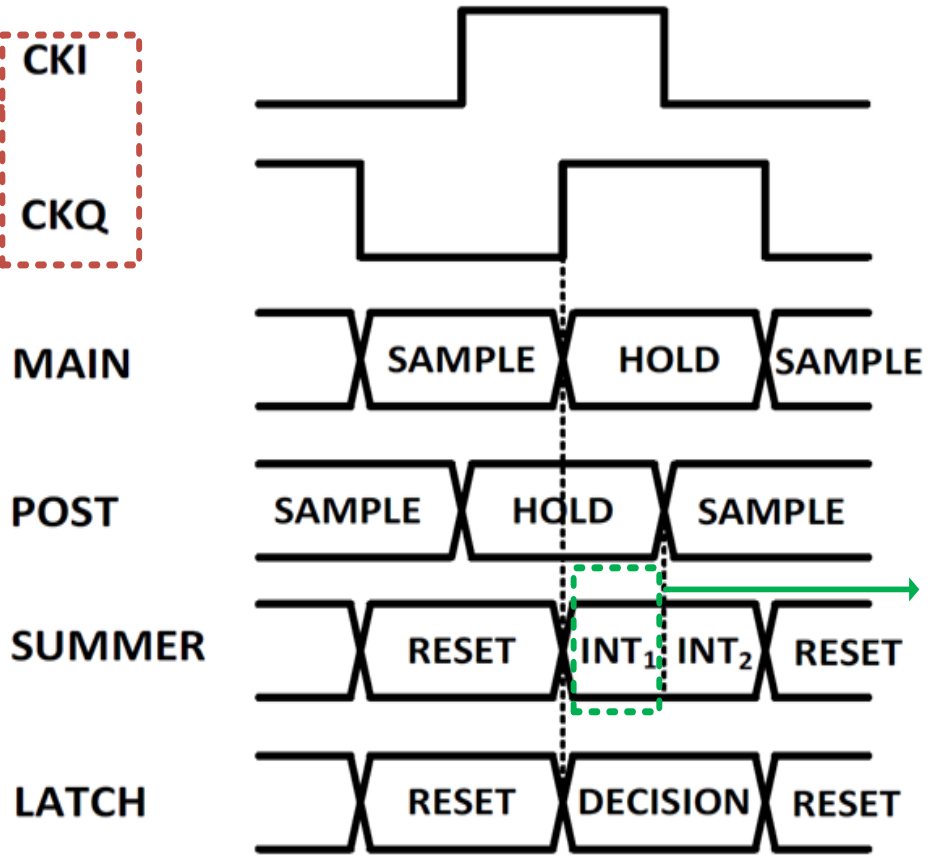
Receiver Architecture



- 2-tap RX FFE with current integrating summer
- Dynamic latches cascaded to increase RX sensitivity
- Bang-bang CDR with separated integral and proportional path

RX Timing

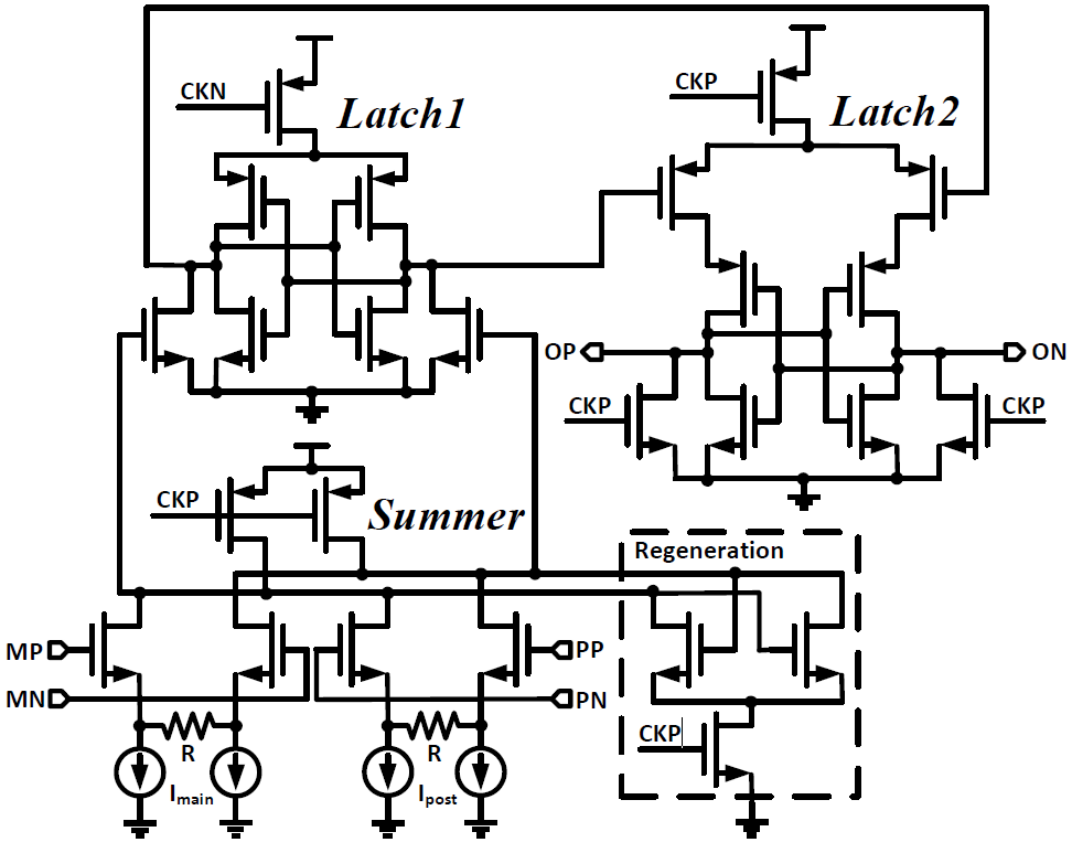
10GHz quadrature clocks are used to sample and hold data, reducing clock tree power

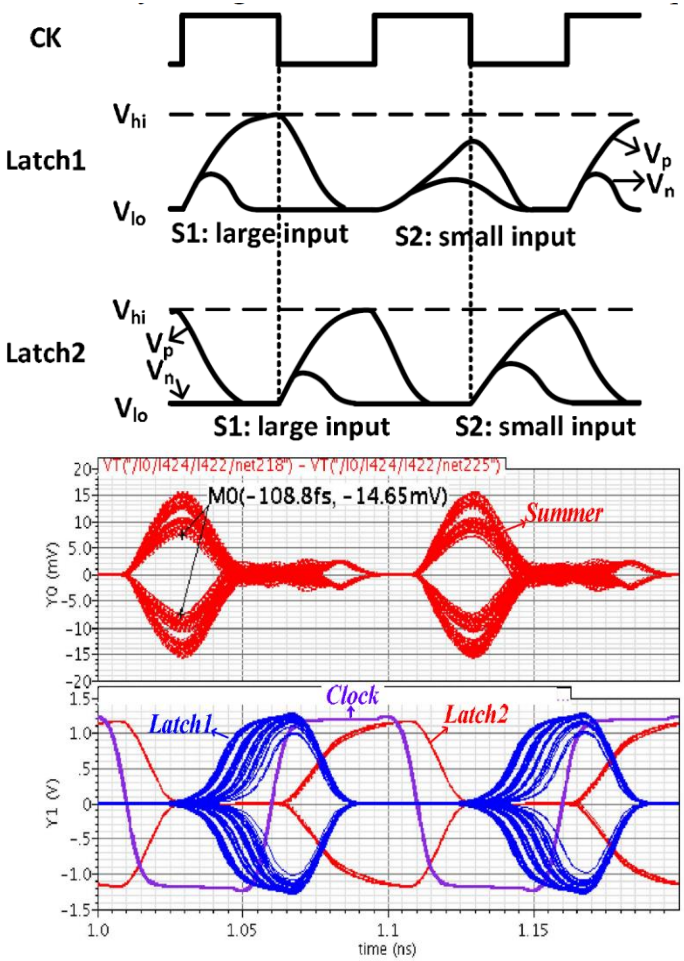


Integrating summer output drops below transistor V_{th} during INT_1 to eliminate ISI introduced by INT_2

- Discrete time 2-tap FFE

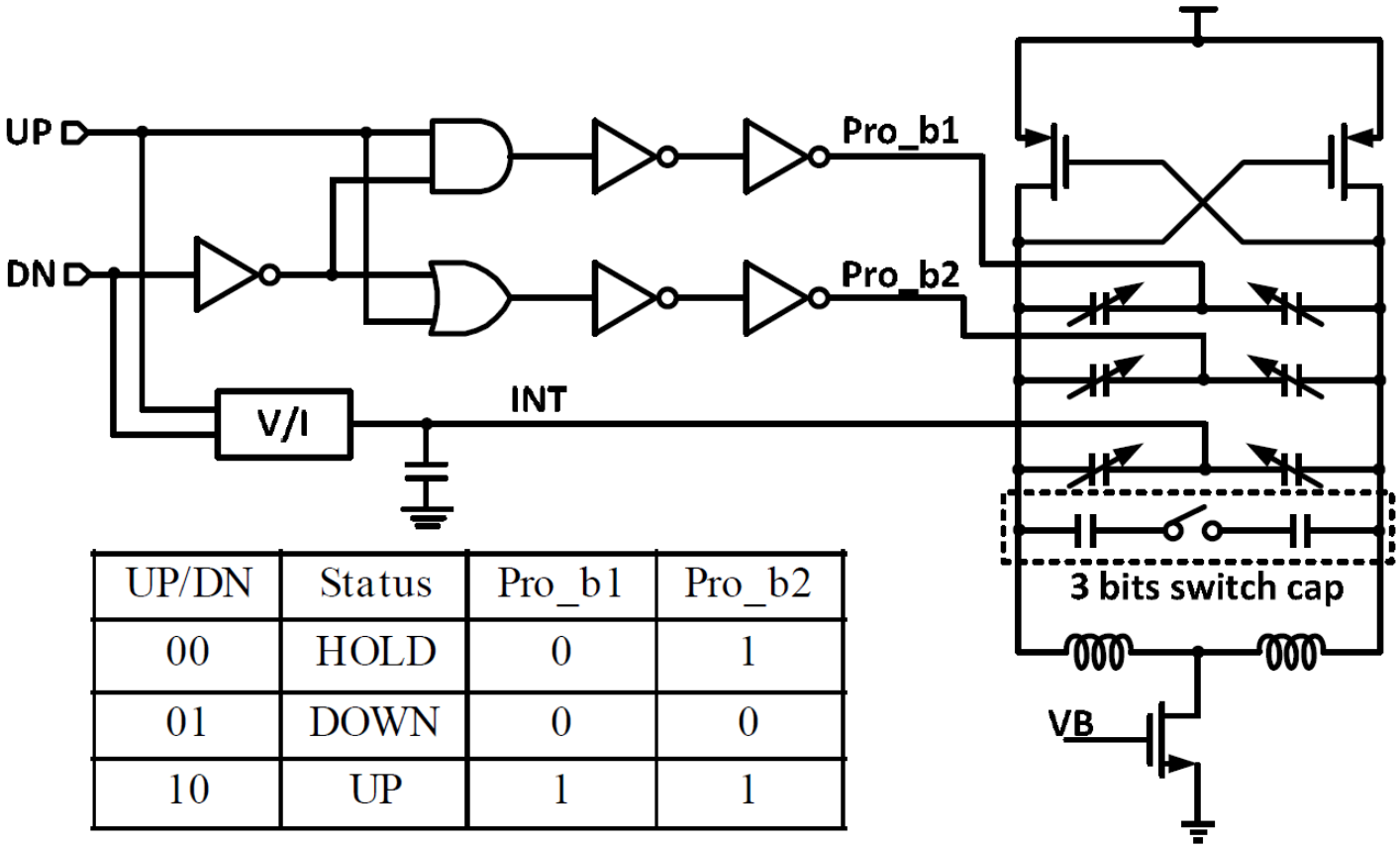
Cascaded dynamic latches





- Limited regeneration time degrades slicer performance
- Double tail comparator + StrongArm comparator

CDR design

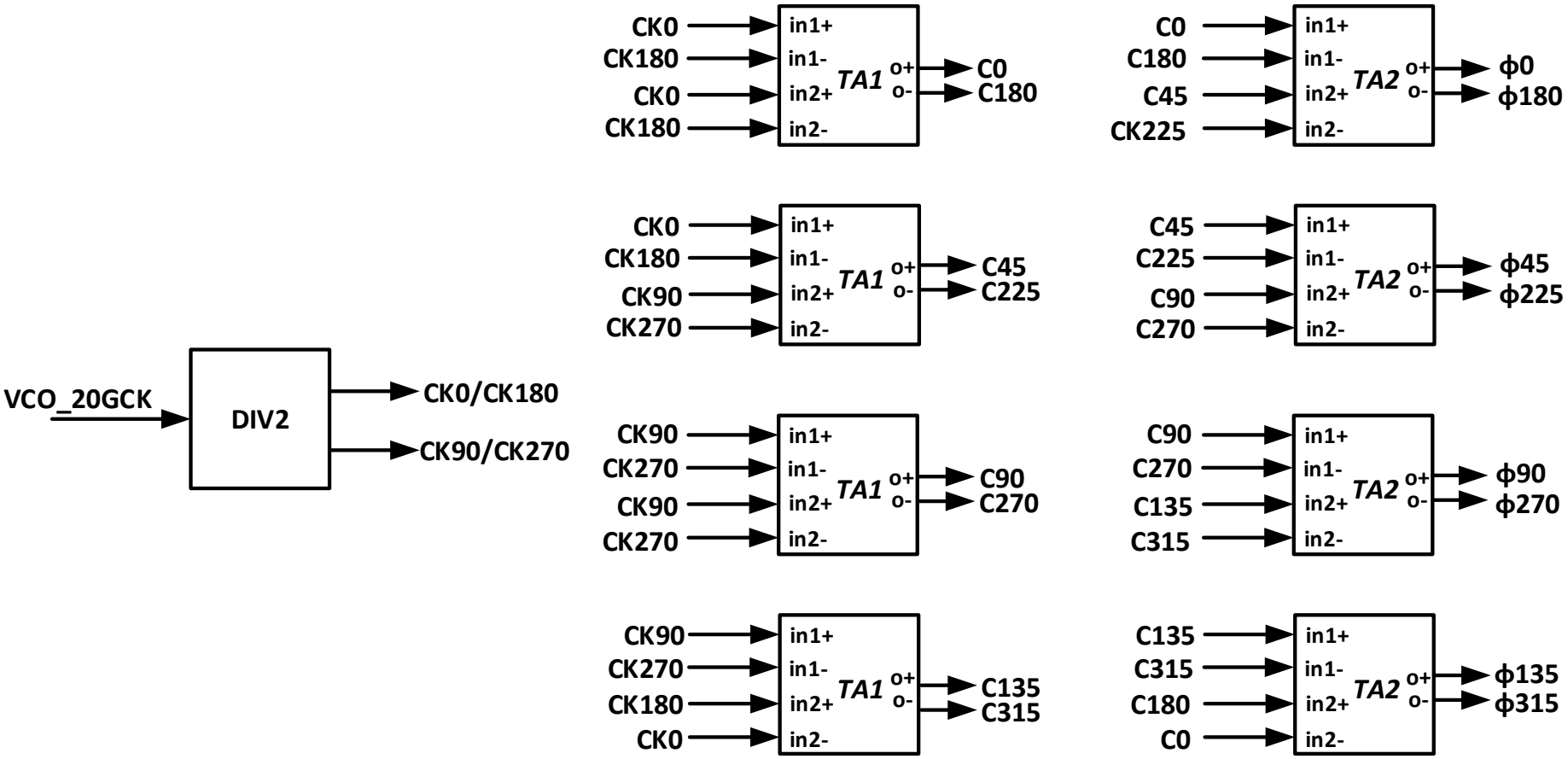


UP/DN	Status	Pro_b1	Pro_b2
00	HOLD	0	1
01	DOWN	0	0
10	UP	1	1

- Separated proportional and integral path alleviate stability problem*

***Shoujun Wang, CICC 2005**

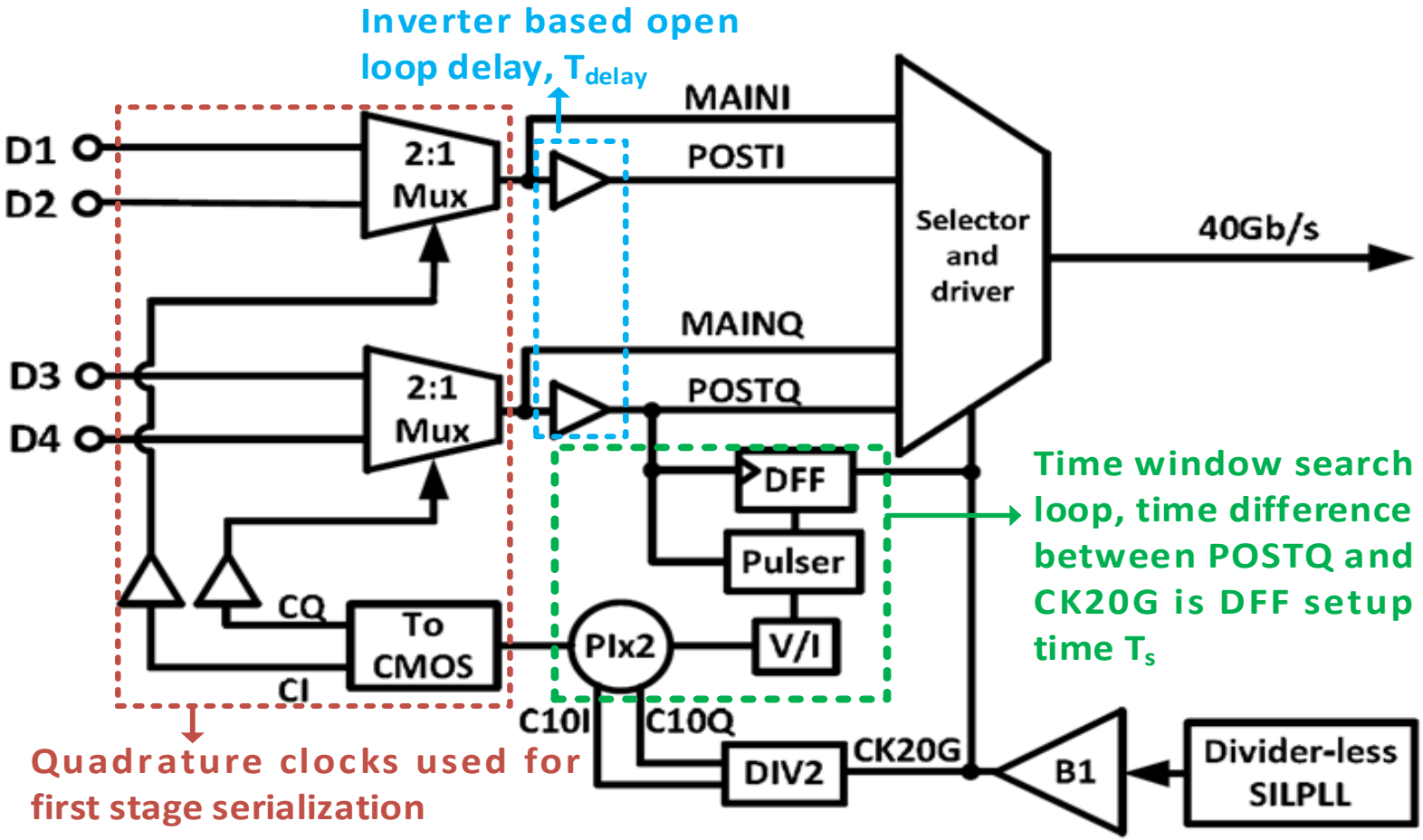
Multiphase clock generation



- 2 stage time-averaging, improving multiphase clock amplitude and phase separation uniformity*

***Kurd, JSSC 2009**

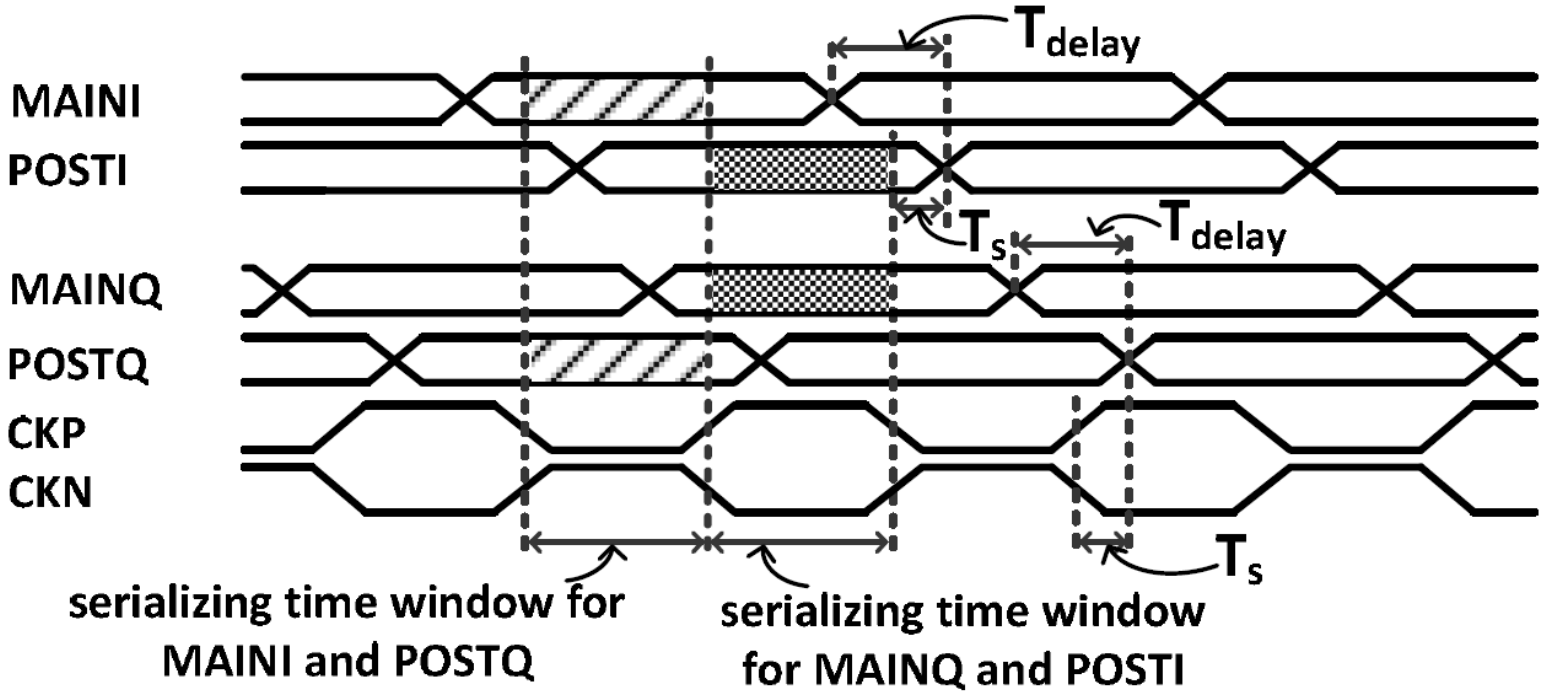
Transmitter Architecure



- Time window search loop to guarantee timing*
- Open loop delay for TX FFE 1-UI delay generation

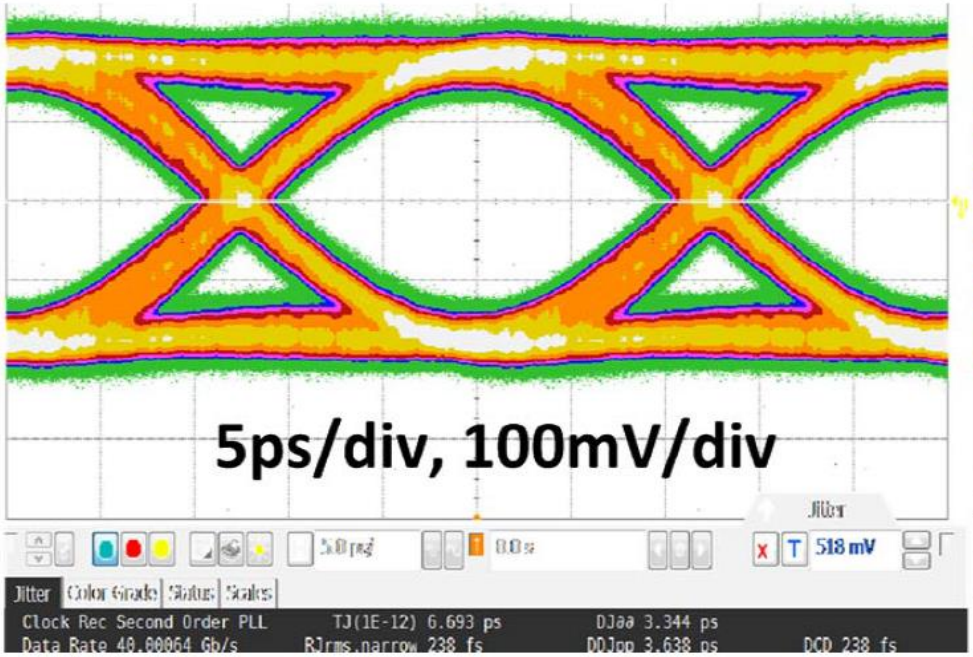
*** K Huang, CICC 2014**

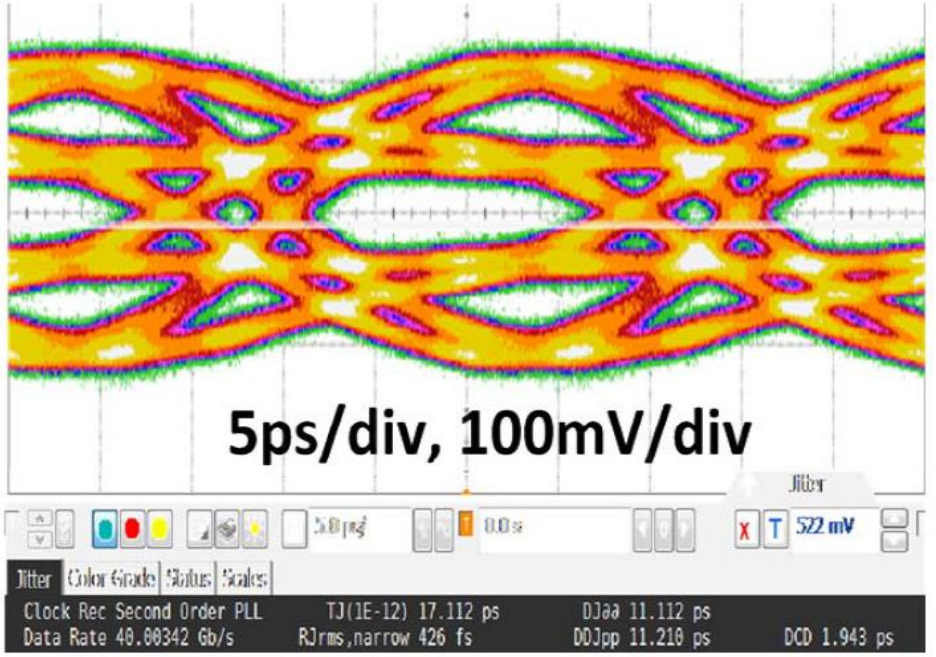
Transmitter timing



- Open loop delay requirement: $T_s < T_{delay} < T_s + 25ps$
- T_s is configurable, a default value is 6.25ps
- Simulation results:$15.5ps < T_{delay} < 23ps$ under PVT

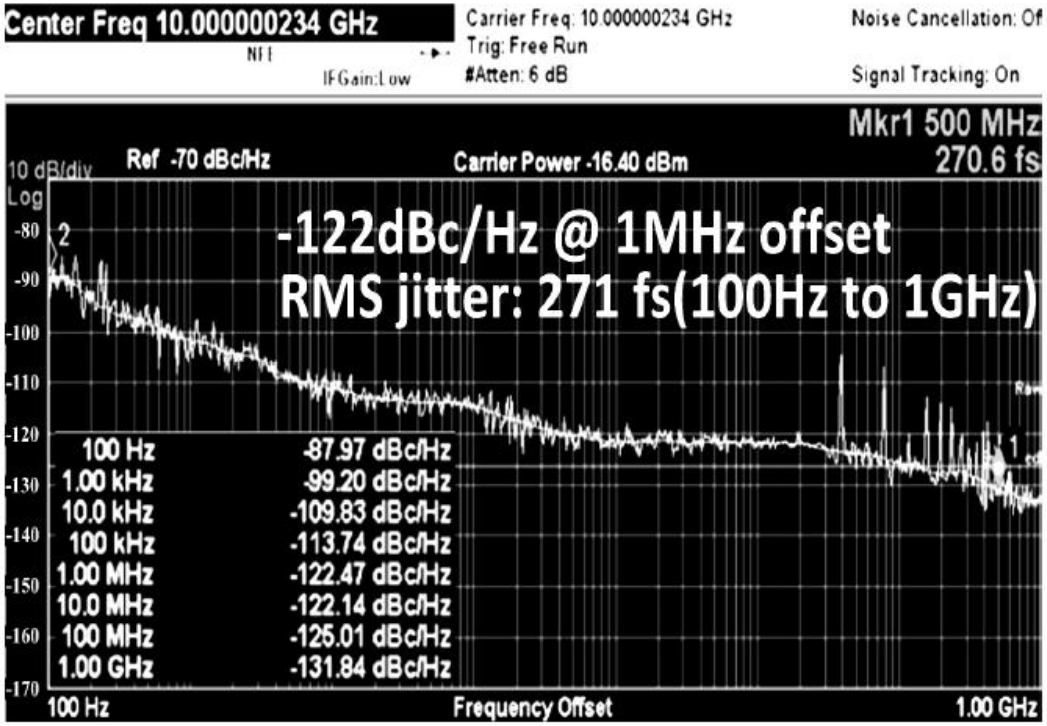
TX eye diagram

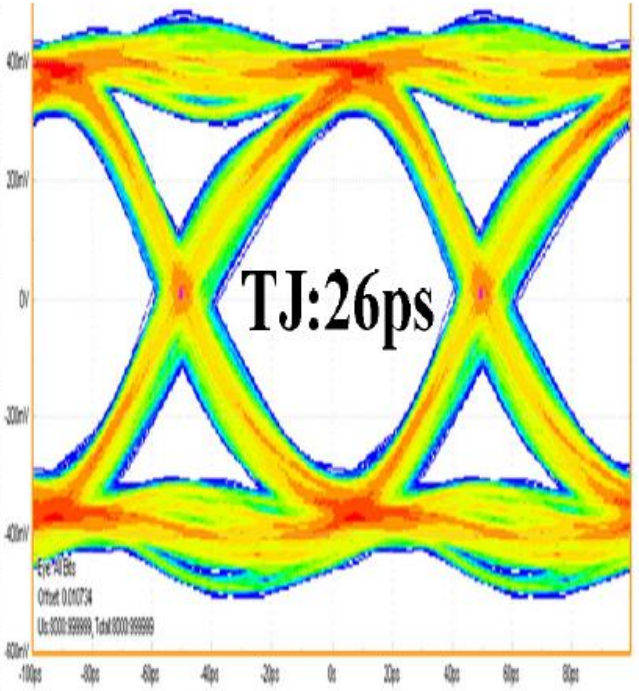




- TX 40Gb/s no equalization and 9.5dB pre-emphasis
- TX total jitter: 6.7ps

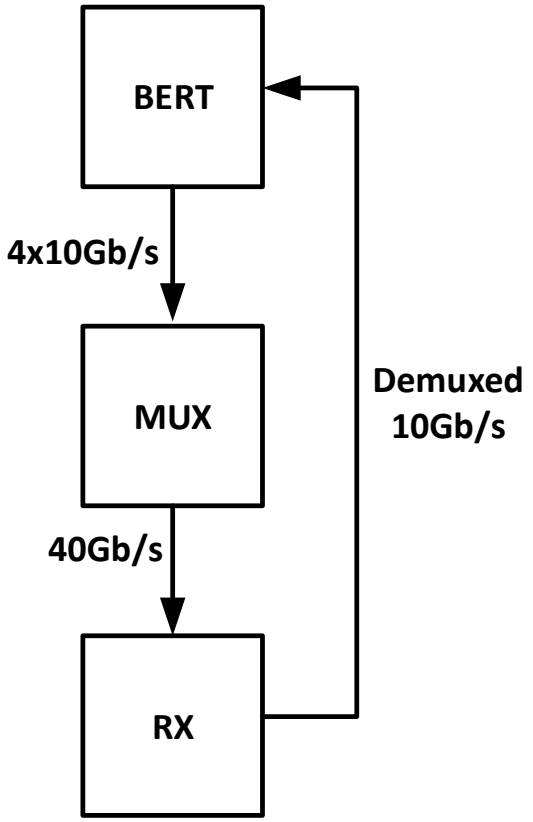
RX recovered clock and demuxed data

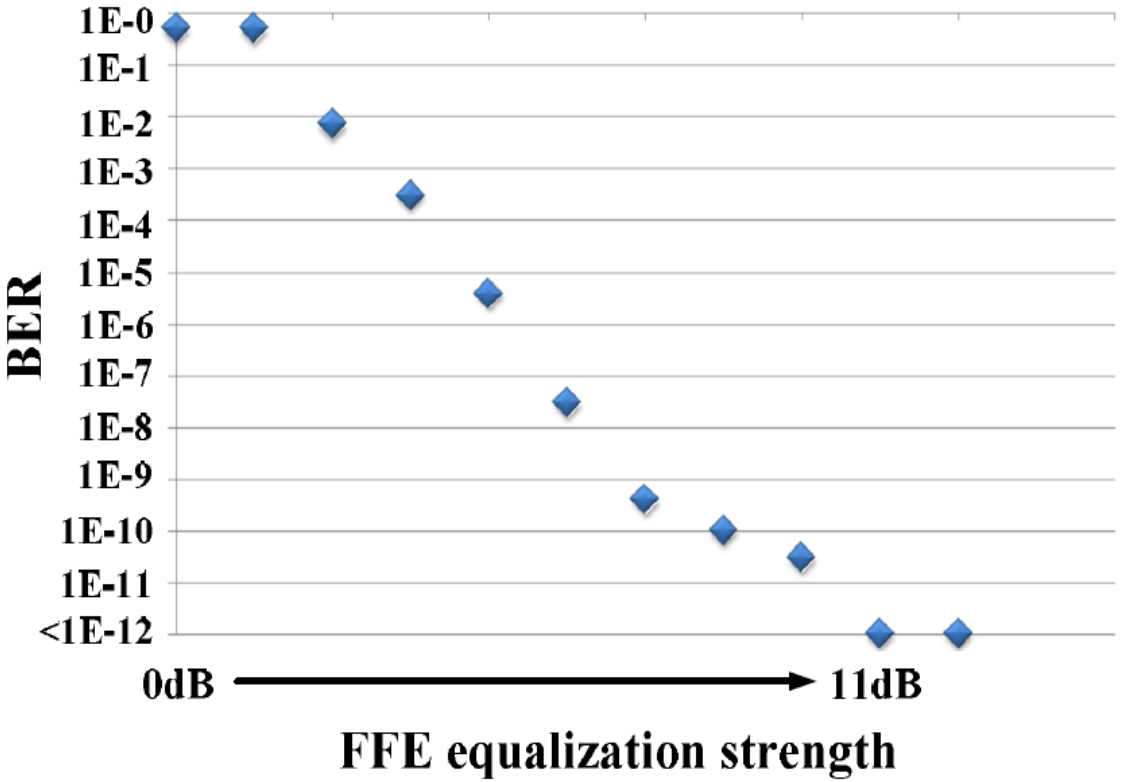




- RMS jitter: 271fs
- phase noise: -122dBc @ 1MHz
- 10Gb/s data total jitter: 26ps

RX Equalization





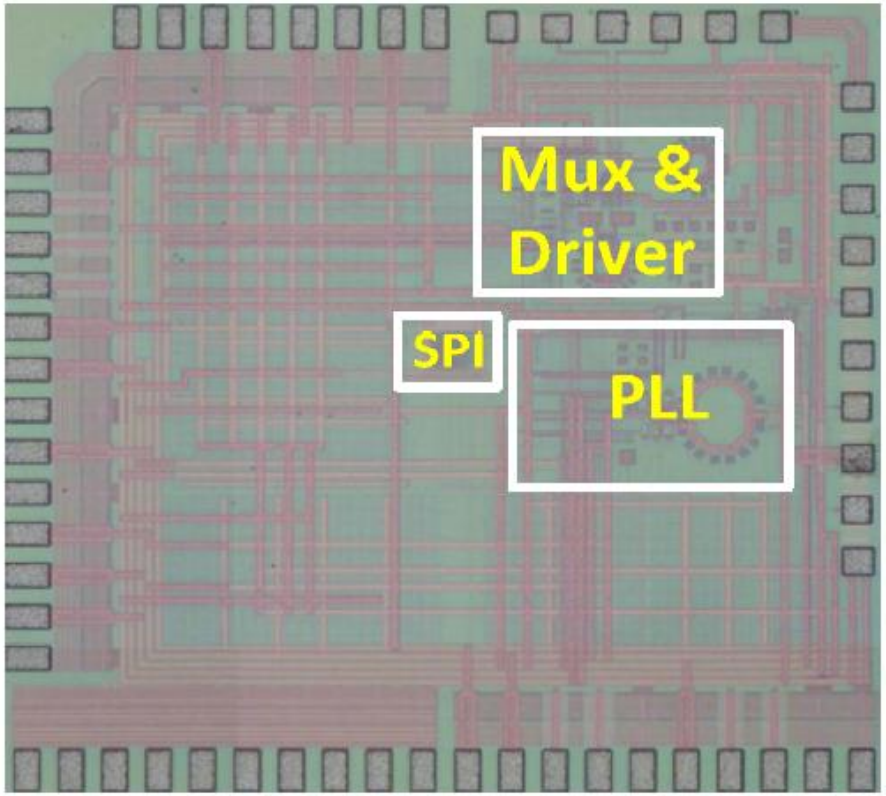
- Channel: A short lossy cable, SMA connector, a 1.5cm FR4 trace and bonding wire.
- 11dB FFE + 4dB CTLE

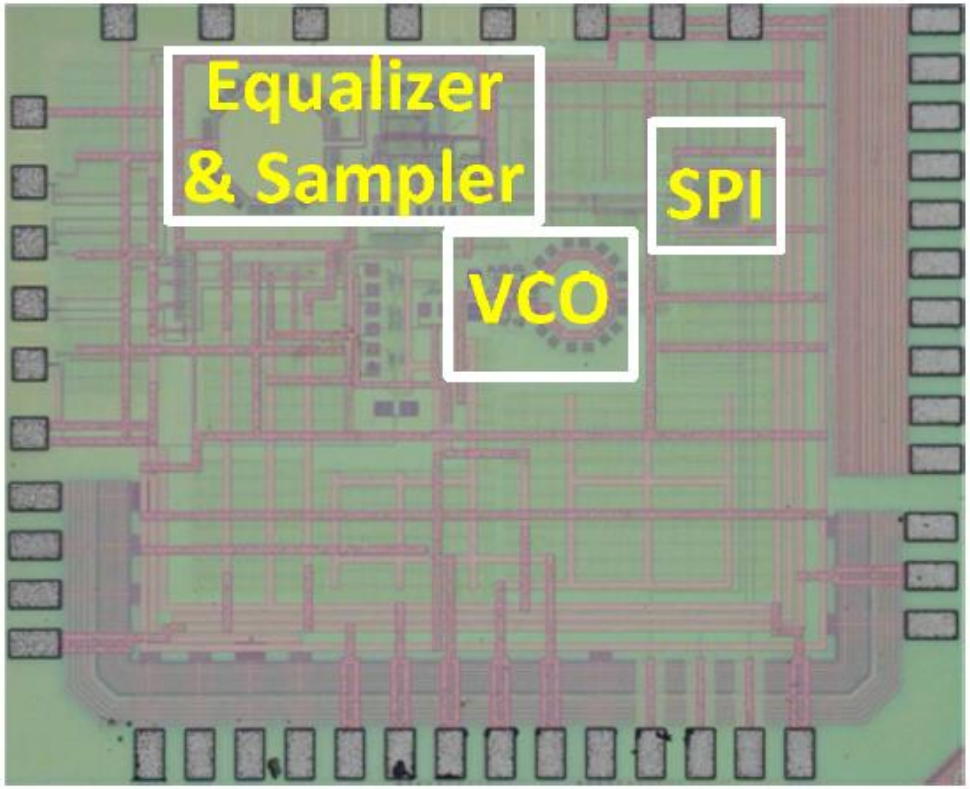
Performance Summary

	This work	[3][b],Lee, JSSC 2012
Data rate	40 Gb/s (38.4 Gb/s - 46.4Gb/s)	40Gb/s (38.8 Gb/s - 42Gb/s)
Technology	65nm	65nm
TX eye jitter	6.7 ps	Not given
Recovered clock jitter	271 fs, rms	319 fs, rms
Recovered data jitter	26 ps, peak-peak	59.1 ps, peak-peak
Power supply	1.2 V	TX:1.2V RX:1.6 V
Power	TX:80mW RX:110mW	TX:135mW RX:520mW
BER	$< 10^{-12}$, 2^7-1 PRBS (15dB loss @20GHz)[a]	$< 10^{-12}$, 2^7-1 PRBS (19dB loss @20GHz)
Chip area	TX: 0.7x0.75mm^2 RX: 1x0.6mm^2	TX: 0.9x0.7 mm^2 RX: 1.1x0.6 mm^2

[a] loss is estimated [b] TX serializer is not implemented

Chip micrograph





TX core: 0.7x 0.75 mm^2

RX core: 1x 0.6 mm^2

Conclusion

- A 40Gbps SerDes transceiver consuming only 190mW power for short range communication is presented. TRX BER is below 1e-12 under 15dB channel loss and TX eye total jitter is 6.7ps for 1e-12 BER.
- Design techniques are employed to reduce power consumption and improve performance, including TX timing calibration, TRX power-efficient FFE, RX cascaded dynamic comparators and RX CDR with separated integral and proportional path.

Acknowledgement

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