A 5.4-mW 4-Gb/s 5-Band QSPK Transceiver for Frequency-Division Multiplexing Memory Interface

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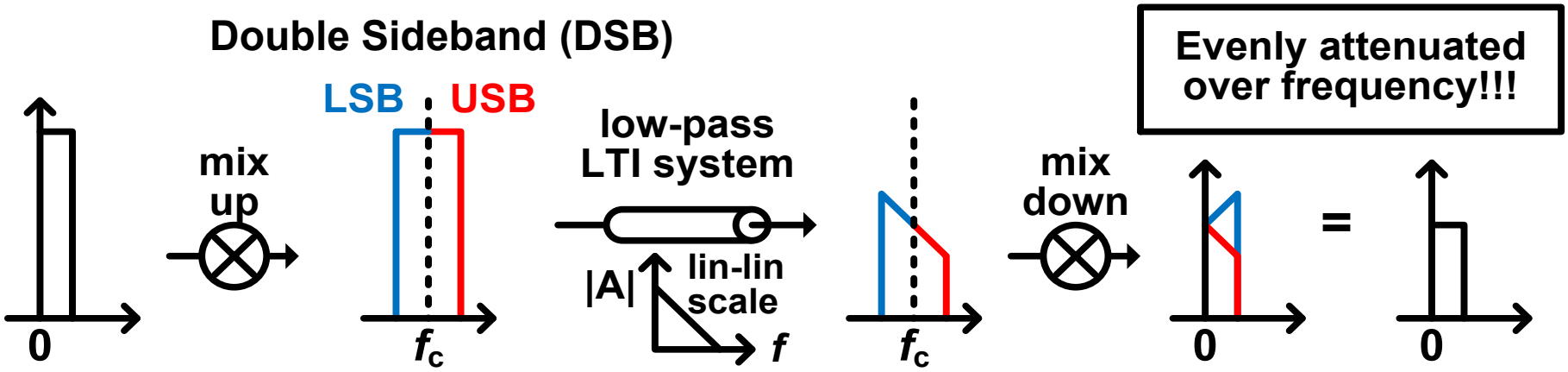
Outline

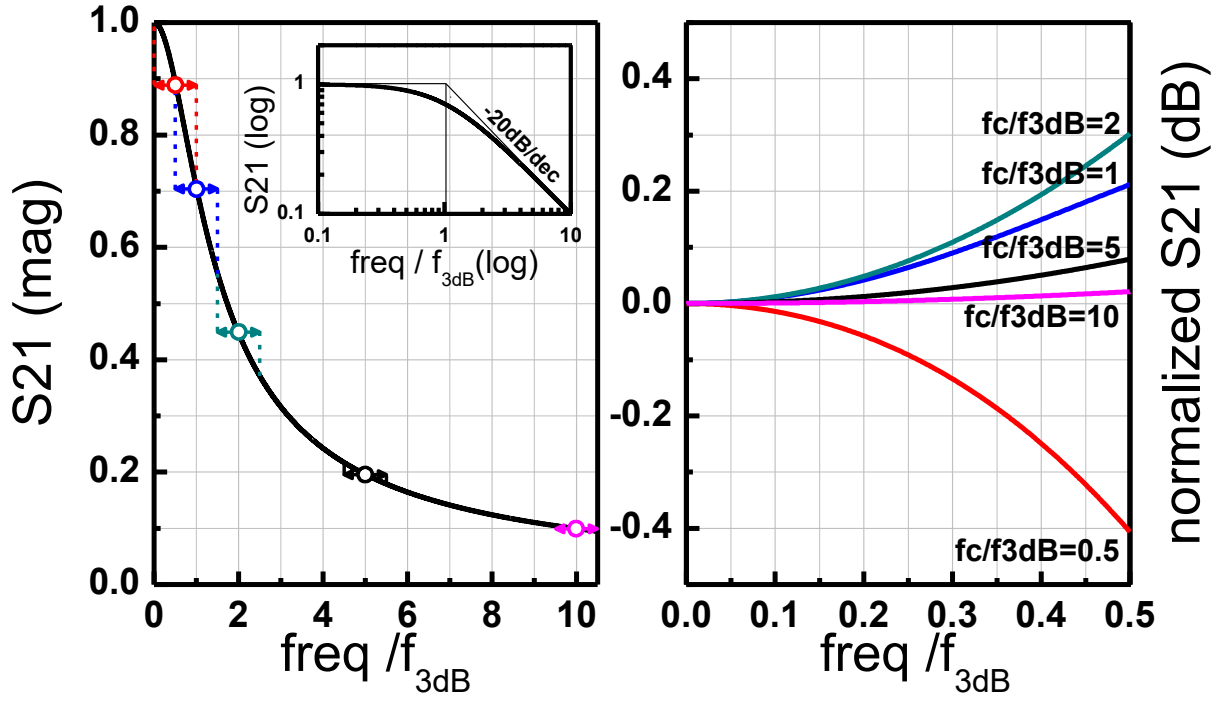
- **FDM Memory Interface**
- 5-Band QPSK Transceiver Design
- Measurement Results
- Conclusion

Self-Equalized DSB Signaling



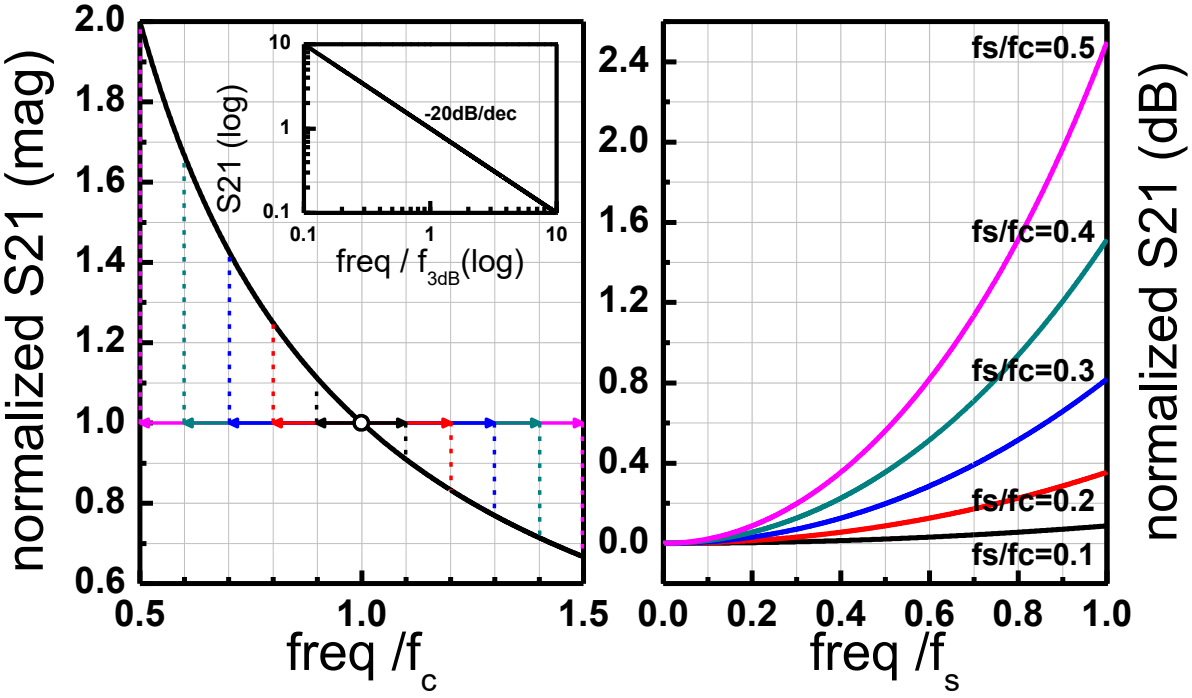
- Two images of original signal (LSB and USB) exist after up-conversion
- LSB with less attenuation compensates for USB with more attenuation
- Reconstructed signal is evenly attenuated over frequency → No ISI
- Too ideal? 10dB/dec (skin effect) or 20dB/dec (RC)

Self-Equalized DSB Signaling (cont.)



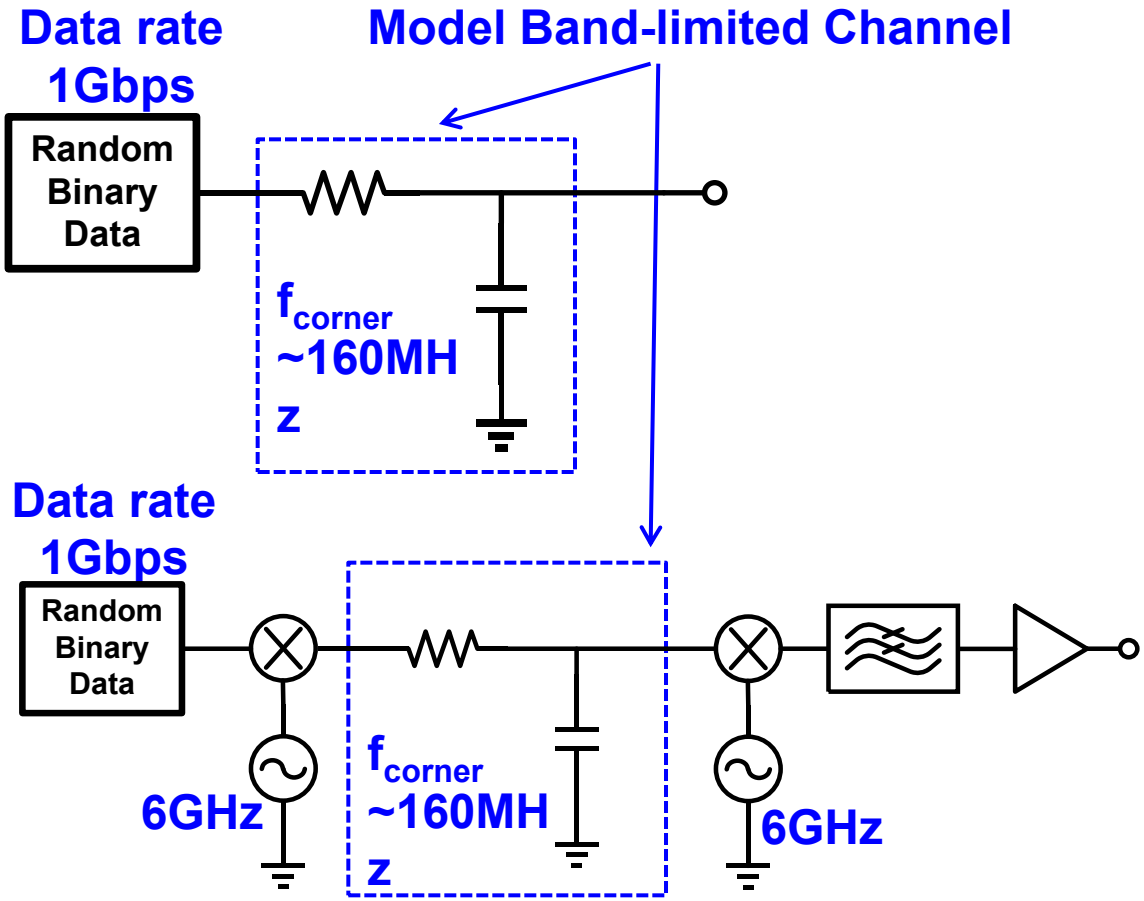
- Assume 1st-order low-pass channel (RC)
- If $f_c < f_{3dB}$, slightly damping
- If $f_c \geq f_{3dB}$, slightly peaking

Self-Equalized DSB Signaling (cont.)

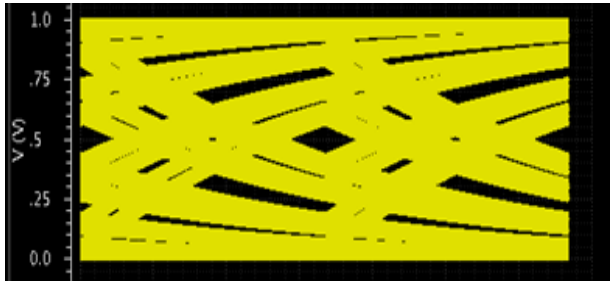


- If $f_s \geq 0.5 f_c$, over-peaking (>2.4 dB)
- How about transient response?

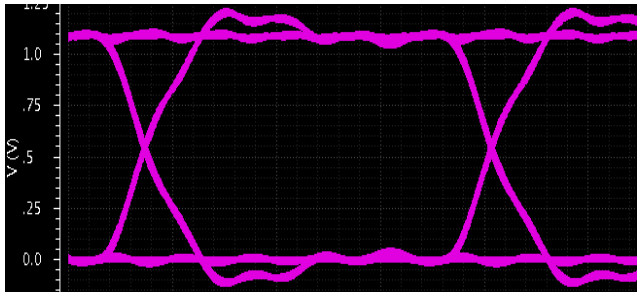
Comparison between NRZ and DSB



Non-Return-to-Zero (NRZ)

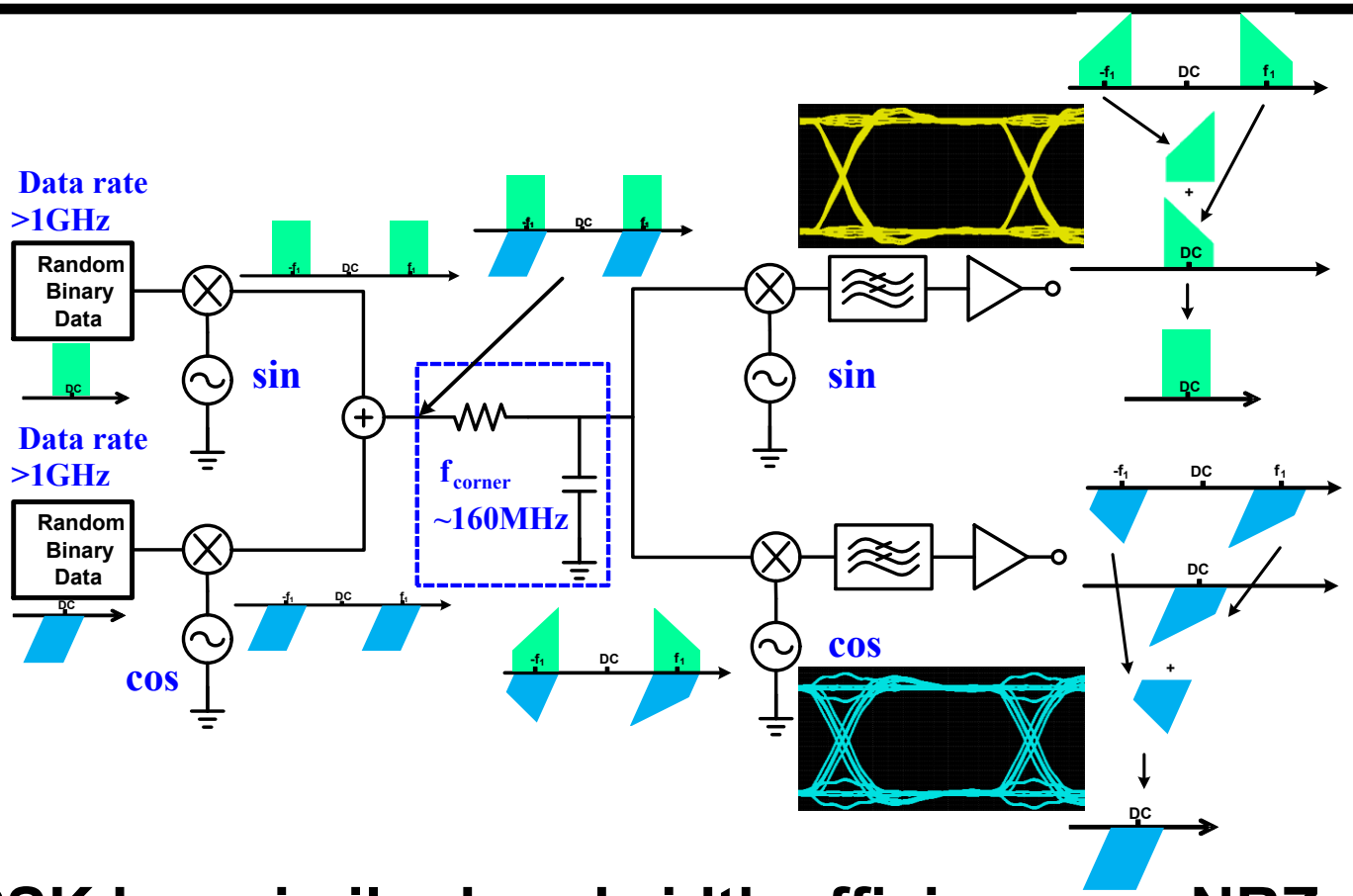


Double Sideband (DSB)



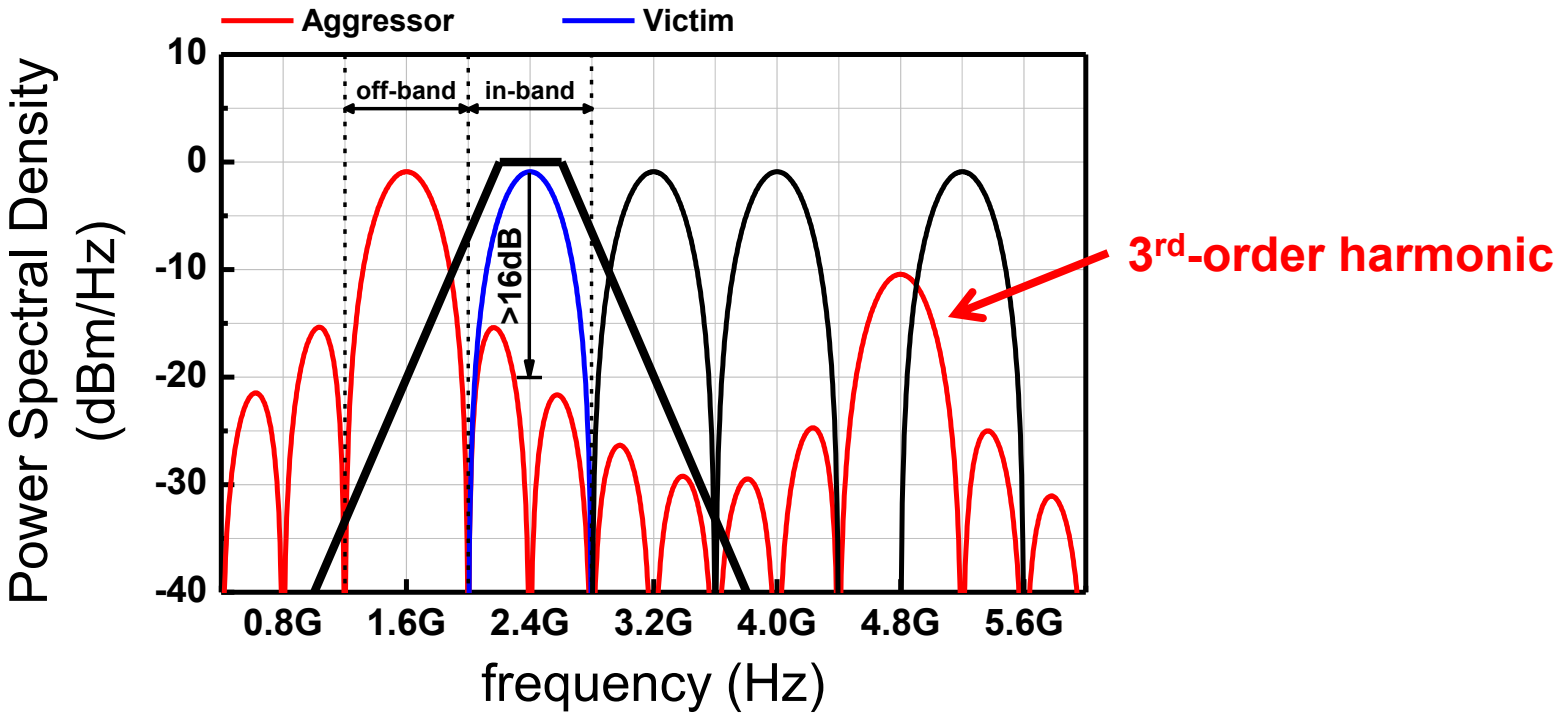
- DSB signaling reduces bandwidth efficiency?

Multi-Band QPSK Modulation



- QPSK has similar bandwidth efficiency as NRZ
- Zero time skew due to sharing the same physical channel → no DLL required
- Skewless 10-bit bundle with 5-band QPSK

Adjacent-Channel Interference (ACI)



- **Off-band ACI can be suppressed by RX LPF**
- **In-band ACI is >20 dB smaller than the desired signal**
- **Fully differential architecture can avoid 2nd-order harmonic**

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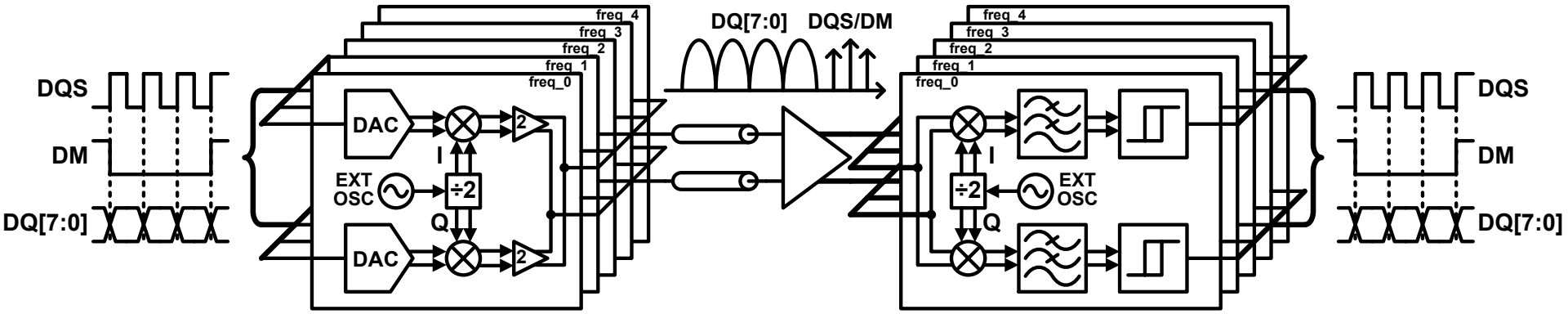
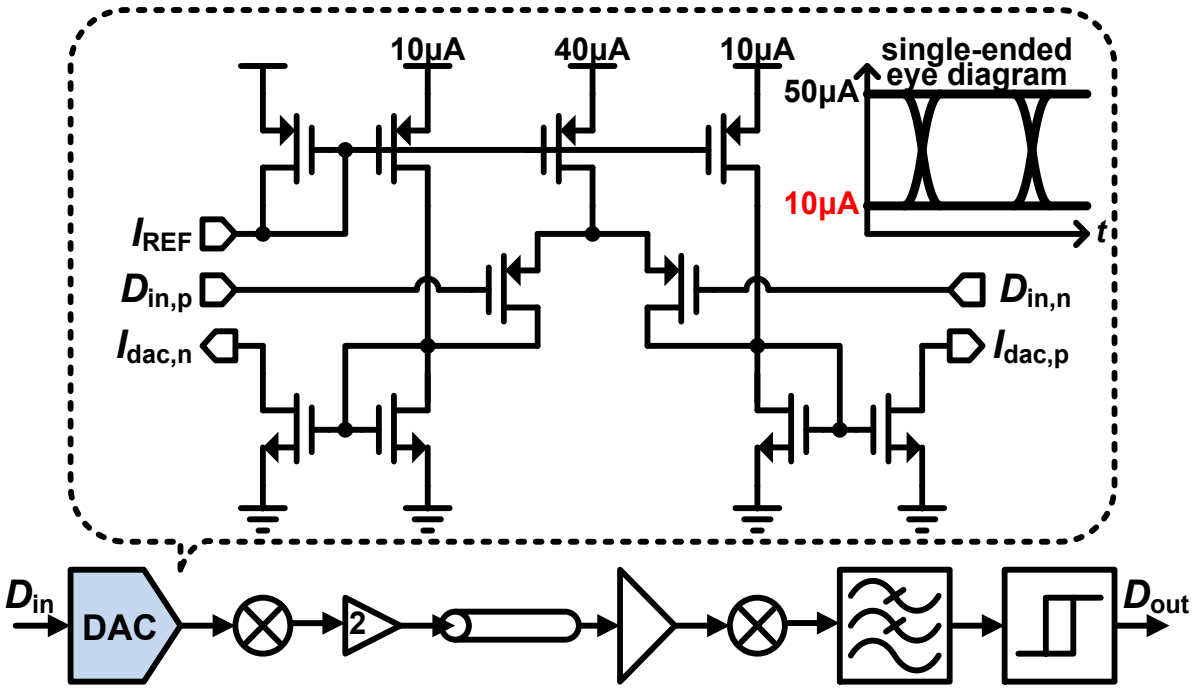
Proposed Transceiver Architecture



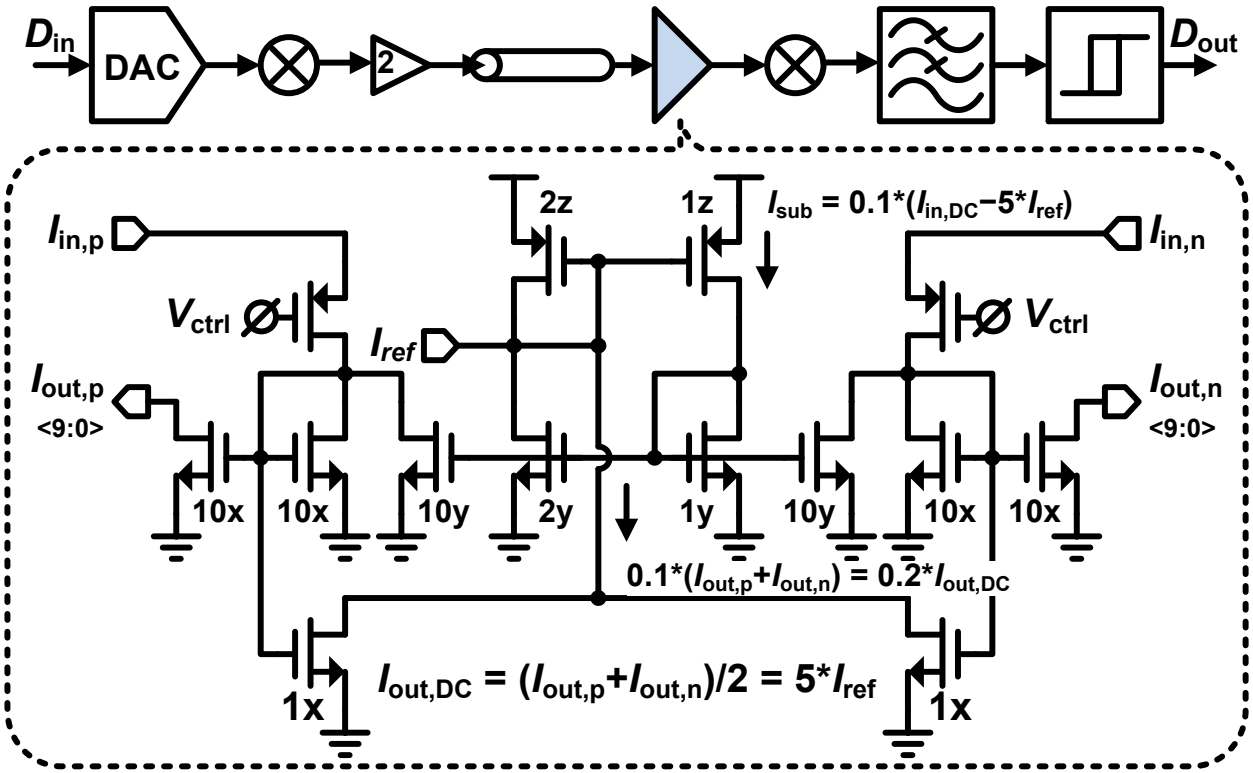
- **5-band QPSK transceiver simultaneously carries 10 parallel bit streams**
- **Fully differential architecture suppresses even-order harmonics**

TX: Current DAC



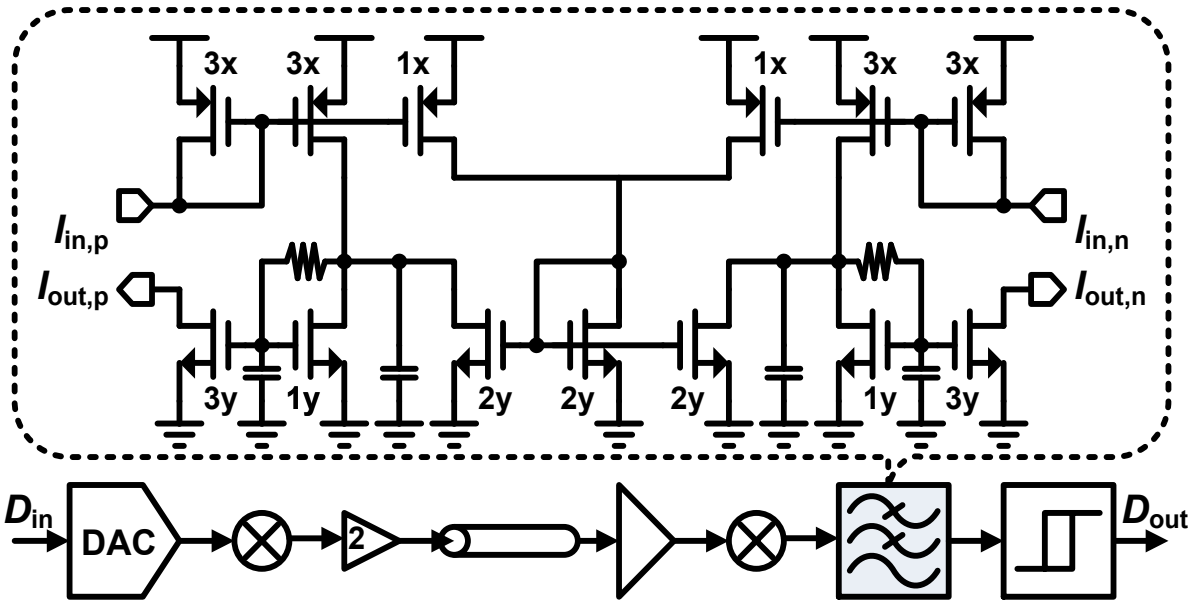
- **10-μA bottom current ensures the TX output buffer speed and RX impedance matching**
- **80-mV_{pp} on 100-Ω differential TML**

RX: Input Current Buffer



- **RX input buffer is directly biased by TX output current**
- **Output common-mode is controlled by I_{ref}**

RX: Low-Pass Filter

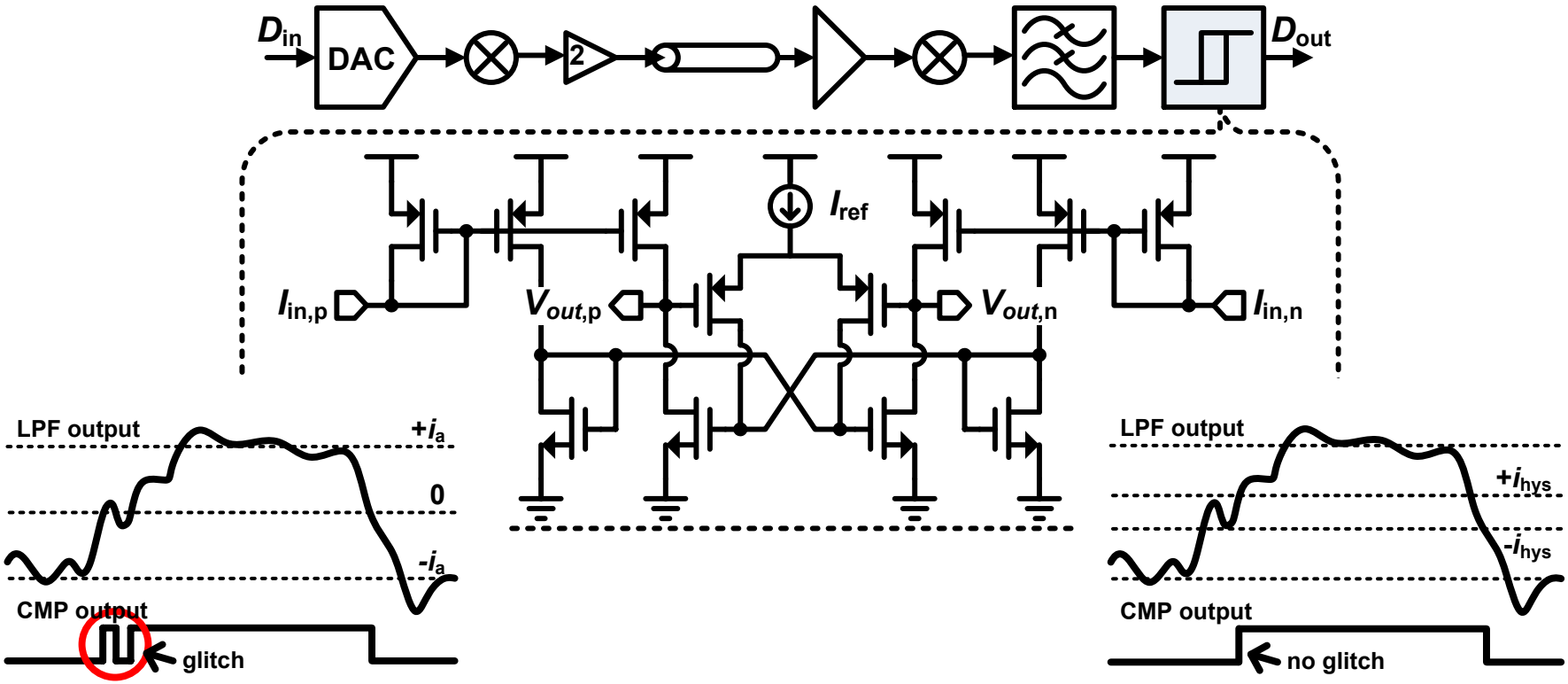


$$\frac{i_{out}}{i_{in}} = \frac{K}{1 + s/\omega_0 Q + s^2/\omega_0^2} = \frac{3}{1 + s\Big/\dfrac{g_m}{C_{gs}+C_{gd}} + s^2\Big/\dfrac{g_m}{RC_{gs}C_{gd}}}$$

$$\Rightarrow \omega_0 = \sqrt{\frac{g_m}{RC_{gs}C_{gd}}},\ Q = \frac{\sqrt{g_m RC_{gs}C_{gd}}}{C_{gs}+C_{gd}}$$

- **Two cascaded 2nd-order LPF with combined f_{3dB} of ~200 MHz → >20-dB off-band ACI suppression**

RX: Schmitt-Trigger Comparator



- **Schmitt-trigger comparator is used to prevent glitch induced by residual ACI**
- **Hysteresis window is set by I_{ref}**

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- **Measurement Results**
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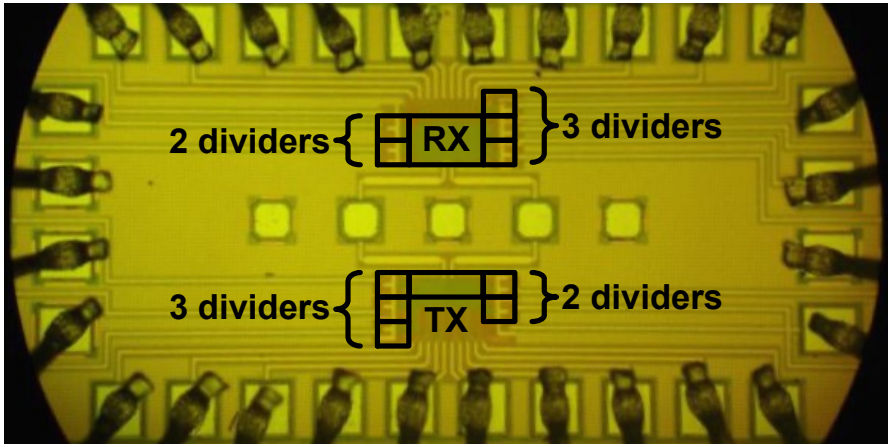
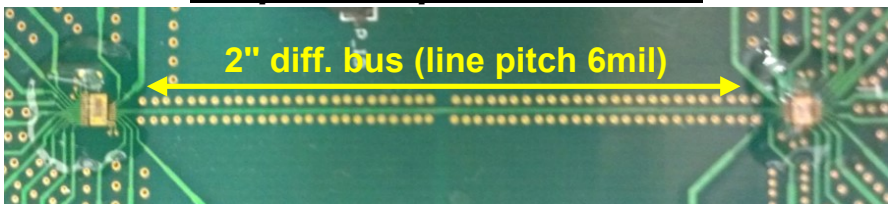
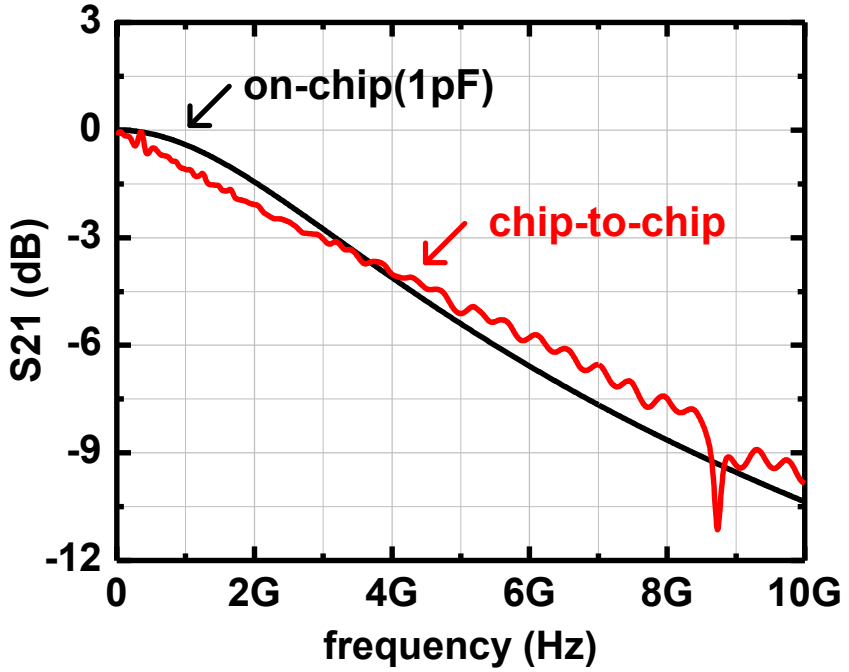
Die Photo & Channel Response

On-Chip Interconnect (1pF)



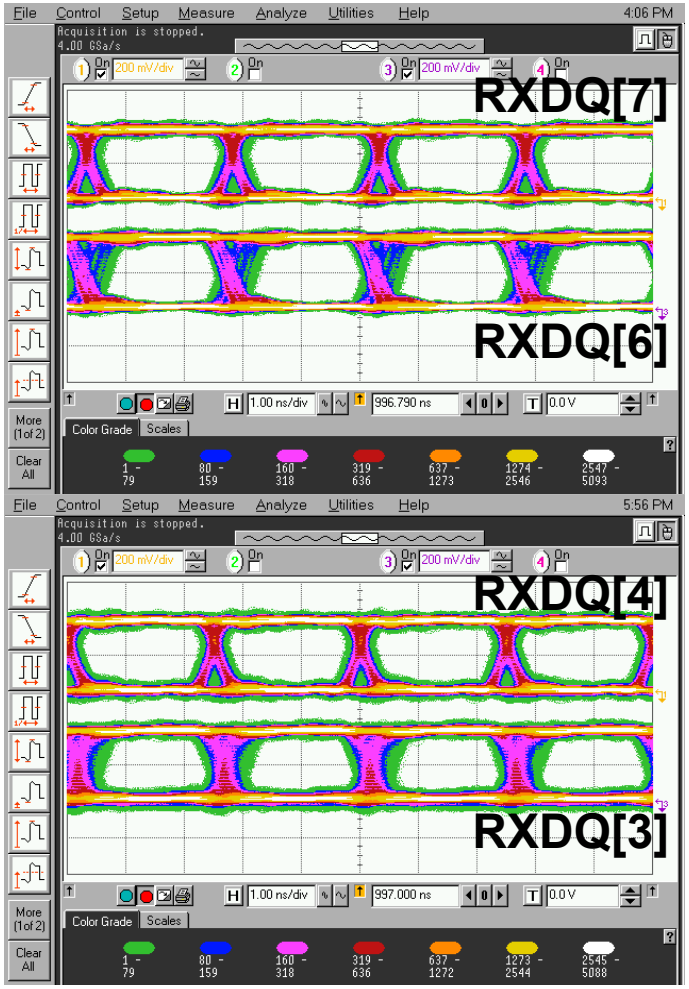
Chip-to-Chip Interconnect

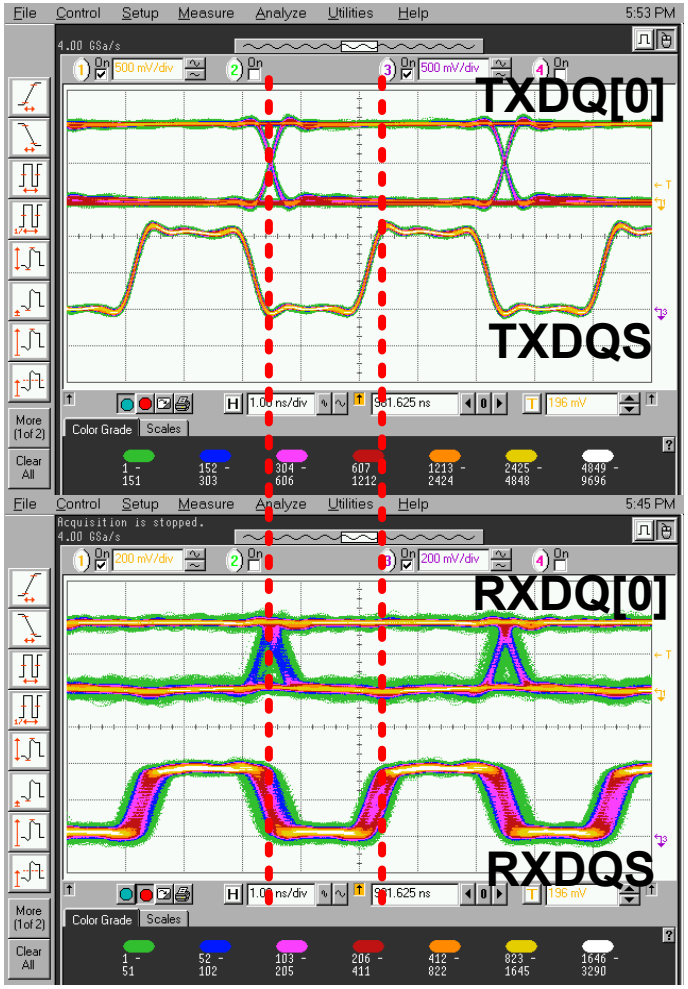




- Compact core area: TX/RX total 80×100 μm^2
- 1-pF loading emulates TSV 3DIC packaging
- Both on-chip and chip-to-chip interconnect experience ~6 dB @6 GHz

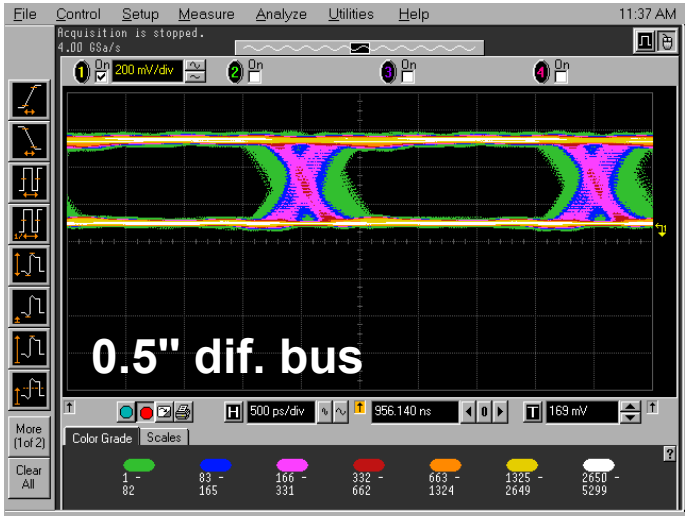
On-Chip Interconnect Measurement

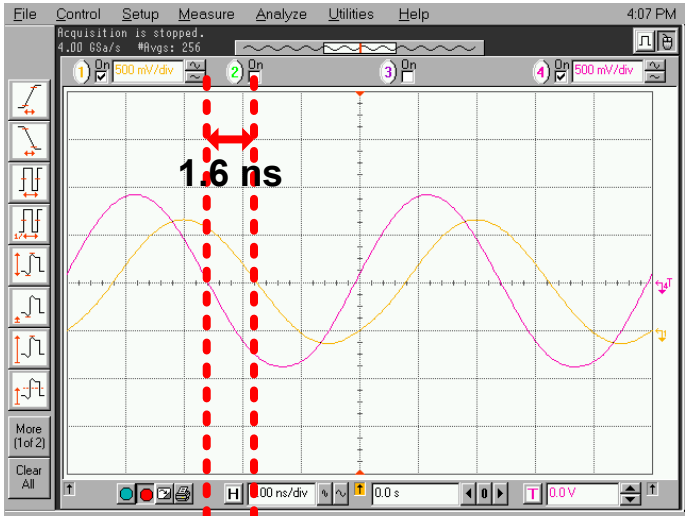


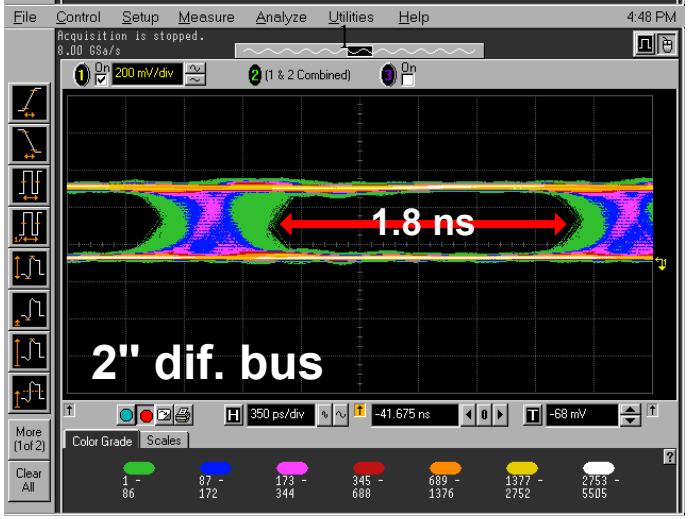


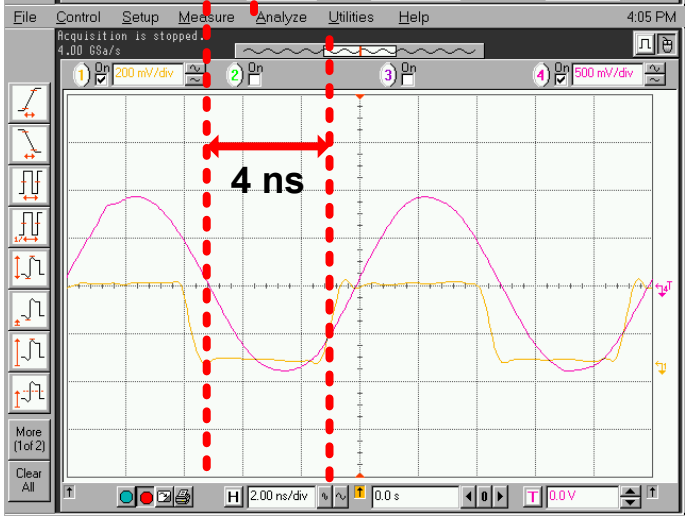
- **Symbol rate: 400 MHz →Total data rate: 4 Gb/s**

Chip-to-Chip Interconnect Measurement



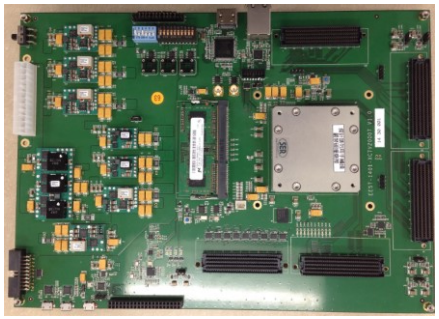






- **2.4 ns delay from SMA to SMA**

Bit Error Rate Testing Platform

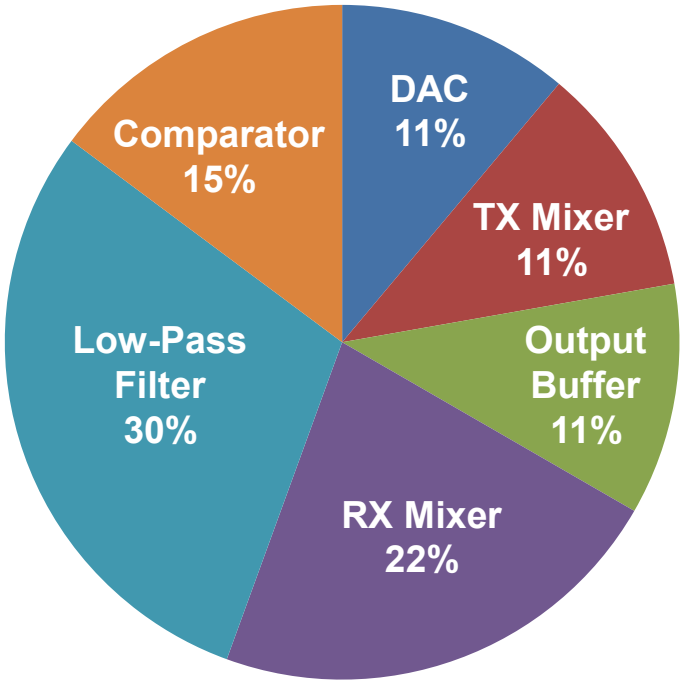


- Xilinx V7-2000T to generate real-time test packets
- Lattice XO3 board is used as the adaptor to SMA
- Measured BER < 10^{-12}

TX/RX Power Breakdown

	Unit Current	Total Current
TX	-	2.4mA
DAC	0.06mA	0.6mA
Mixer	0.06mA	0.6mA
Output Buffer	0.12mA	1.2mA

	Unit Current	Total Current
RX	-	3.6mA
Input Buffer	-	-
Mixer	0.12mA	1.2mA
Low-Pass Filter	0.16mA	1.6mA
Comparator	0.08mA	0.8mA



- Supply Voltage: 0.9 V Total Current: 6 mA
- TX/RX Power Consumption: 5.4 mW
- Dividers can be shared in multi-lane design

Performance Summary and Comparison

	DDR4 [1]	Wide IO [2]	Wide IO [3]	This work
Signaling	NRZ	NRZ	NRZ	5-band QSPK
Technology	22nm CMOS	50nm DRAM	90nm DRAM	40nm CMOS
Data rate	3.2Gb/s/pin	0.2Gb/s/pin	0.2Gb/s/pin	4Gb/s/lane
TX energy efficiency	2.5pJ/b	0.78pJ/b	0.56pJ/b	0.54pJ/b
Cell size (μm^2)	40×135 (TX)	-	-	80×35 (TX) 80×65 (RX)
RX energy efficiency	-	-	-	0.9pJ/b
# of signal pins for 12.8 GB/s	40*	576*	576*	64
# of signal pins for 12.8 GB/s	40*	128*	128*	16
Packaging compatibility	2D/2.5D	TSV 3DIC	TSV 3DIC	2D/2.5D/3DIC

*Estimation based on JEDEC standards

Conclusion

- **Demonstrated a 5-band QSPK transceiver**

- **Self-equalized DSB signaling**
- **Skewless 10-bit bundle**

- **High data rate of 4Gb/s/lane**
- **Low power consumption of 5.4 mW**
- **Compact TX/RX area of 80×100 μm^2**
- **Measured BER < 10^{-12}**

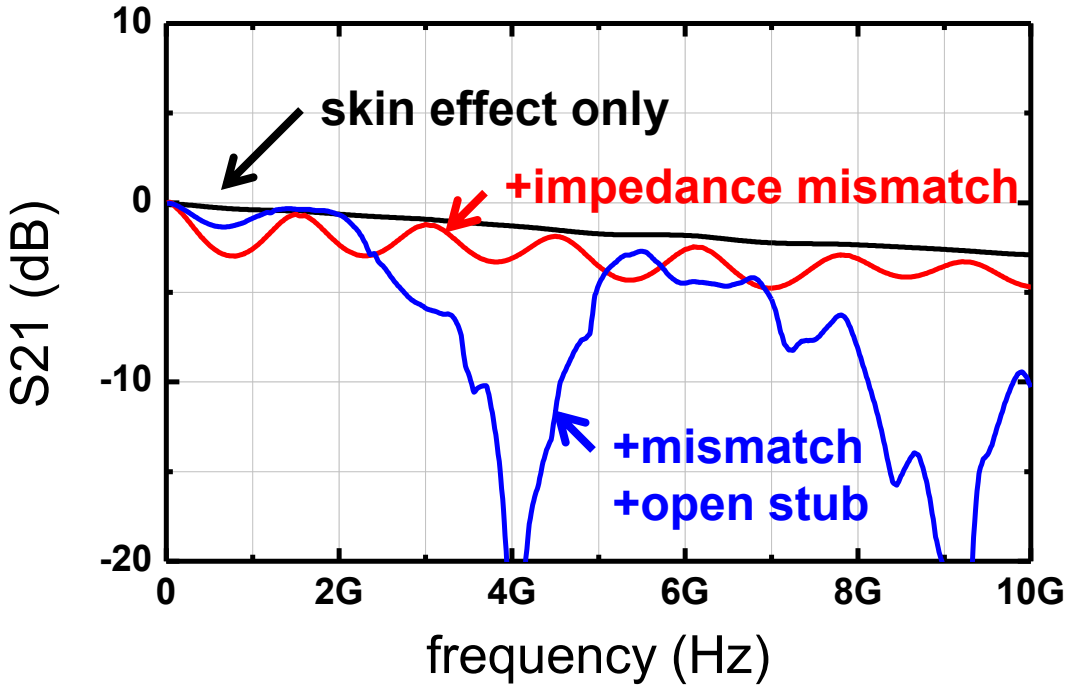
References

[1] T. C. Hsueh, et al.: 'A 25.6Gb/s differential and DDR4/GDDR5 dual-mode transmitter with digital clock calibration in 22nm CMOS', ISSCC Dig. Tech. Papers, pp. 444-445, Feb. 2014.

[2] J.-S. Kim, et al.: 'A 1.2 V 12.8 GB/s 2 Gb Mobile Wide-I/O DRAM With 4 × 128 I/Os Using TSV Based Stacking', IEEE J. Solid-State Circuits, vol. 47, no. 1, pp. 107-116, 2012.

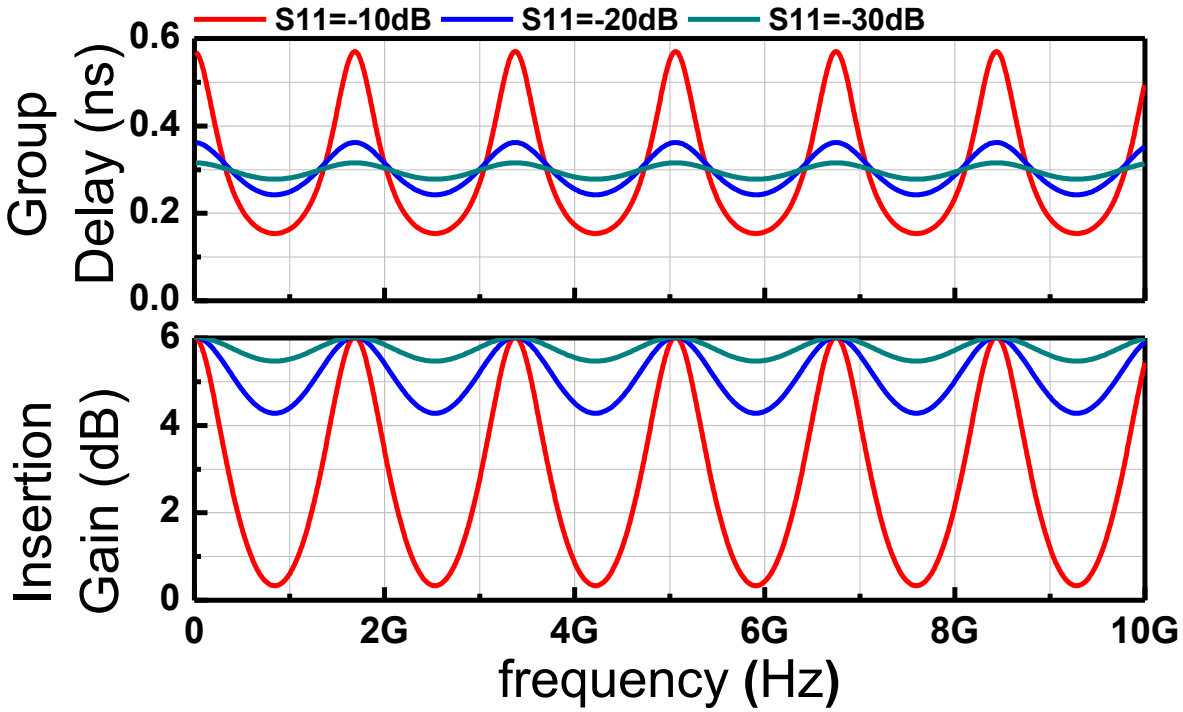
[3] S. Takaya, et al.: 'A 100GB/s wide I/O with 4096b TSVs through an active silicon interposer with in-place waveform capturing', ISSCC Dig. Tech. Papers, pp. 434-435, Feb. 2013.

Other Channel Non-ideality



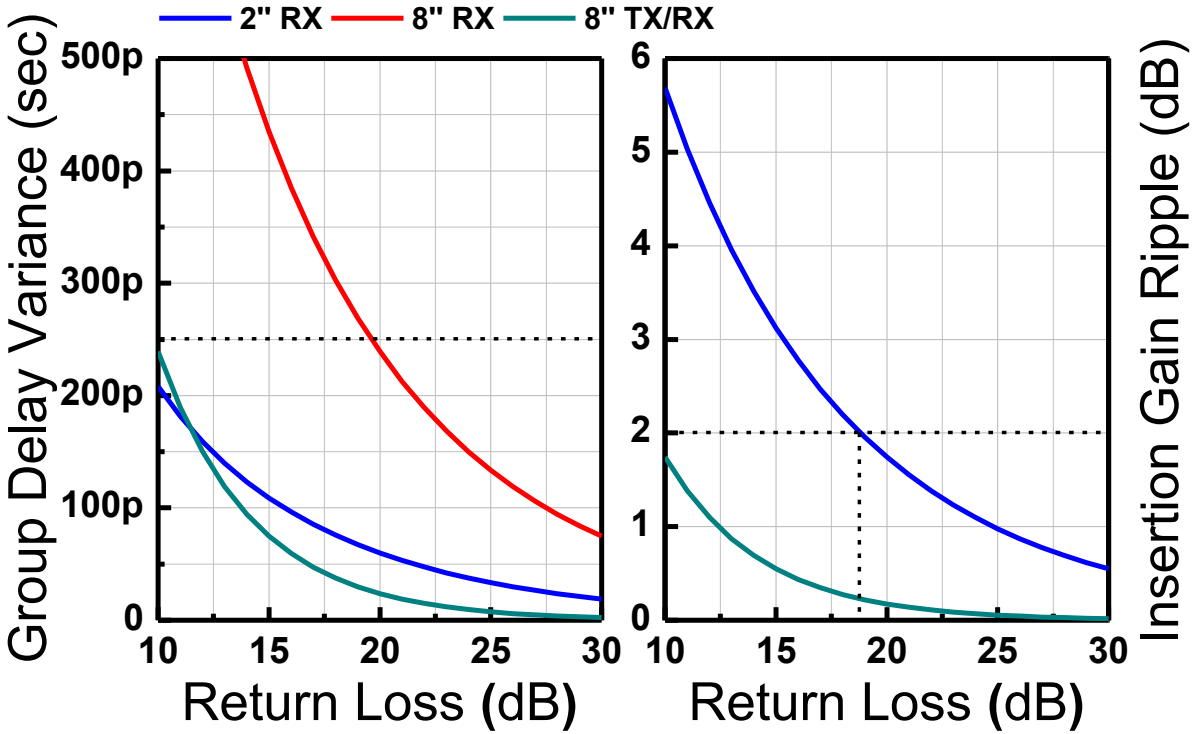
- By proper carrier allocation, we can avoid frequency notches induced by open stubs
- About impedance matching, how good is enough?

Ideal 2” FR-4 with one-end matching



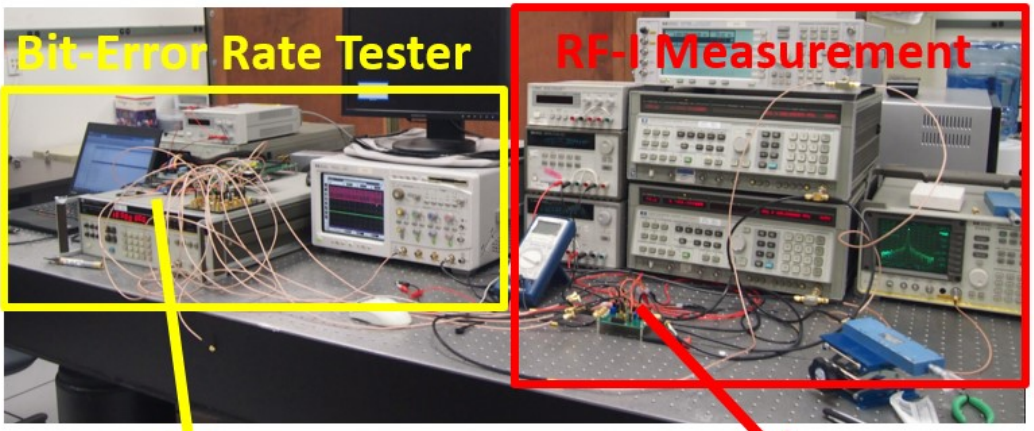
- **Not only amplitude but also phase**
- **Rule of thumb: insertion gain variance < 2 dB**
  group delay variance < 10% UI

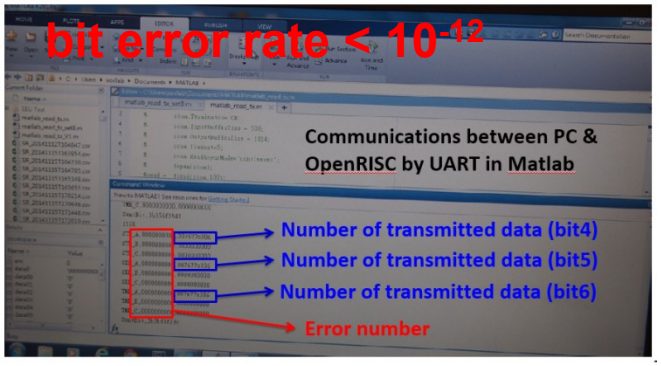
Impedance Matching Specification

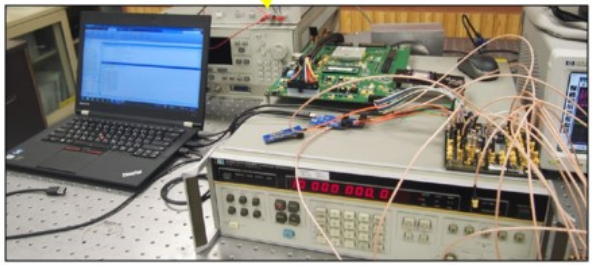


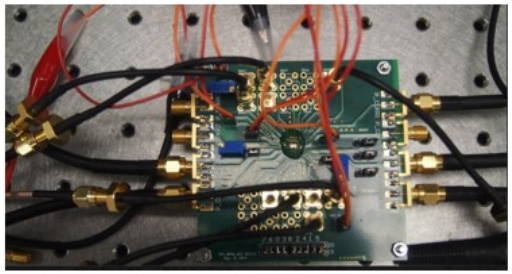
- **Gain variance is independent of channel length**
- **17-dB one-end matching is good enough**

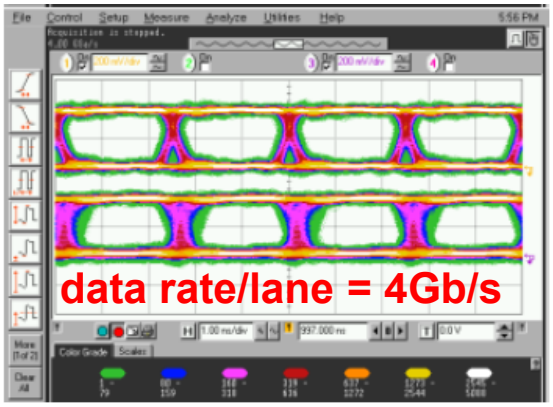
Bit Error Rate Testing











Demo video for MRF-I bit error rate test
https://www.dropbox.com/s/ncsx7kcm77mkxtn/RF-I%20Demo.mp4?dl=0