A power-and-area efficient 10×10 Gb/s bootstrap transceiver in 40 nm CMOS for reference-less and lane-independent operation

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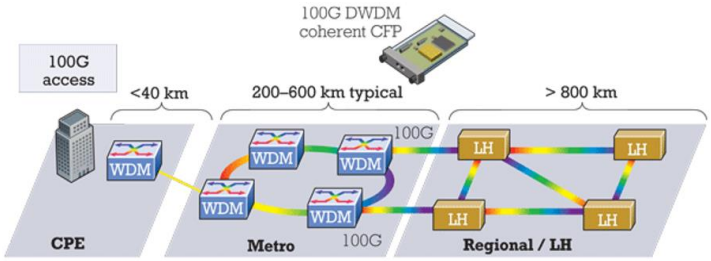
Outline

- **Introduction and Background**
  - Parallel transceivers (TRXs) are becoming mainstream I/O devices.
  - Solution : Reference-less and lane-independent phase interpolator (PI)-based parallel bootstrap TRX
- **Proposed bootstrap CDR**
- **TRX design**
- **Measurement results**
- **Conclusions**

Motivation

- Parallel TRXs are becoming mainstream I/O devices in high-speed serial link applications.



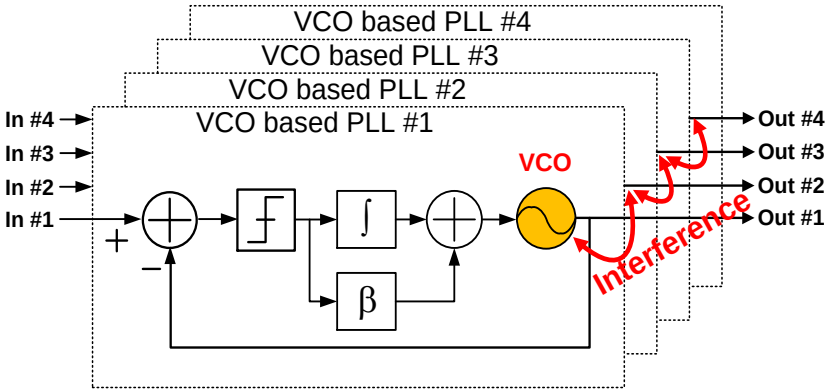
Storage **Networking** **HPC**

- 3 major challenges are
  - Decreasing power consumption
  - Increasing I/O density
  - Reducing the interference among lanes

→ **PI-based clock and data recovery (CDR) architecture** is appropriate.

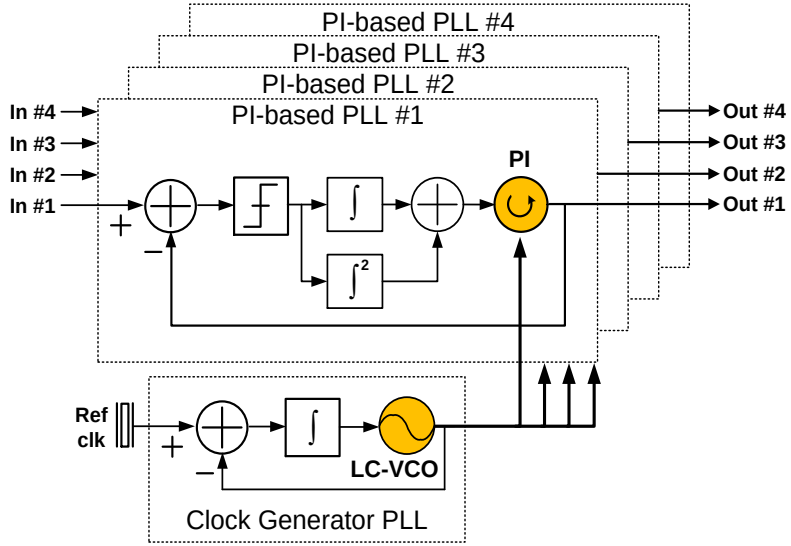
Motivation

- VCO-based PLL



- Ring-VCO
  - ☹ Poor jitter performance
- LC-VCO
  - ☹ Poor area-efficiency

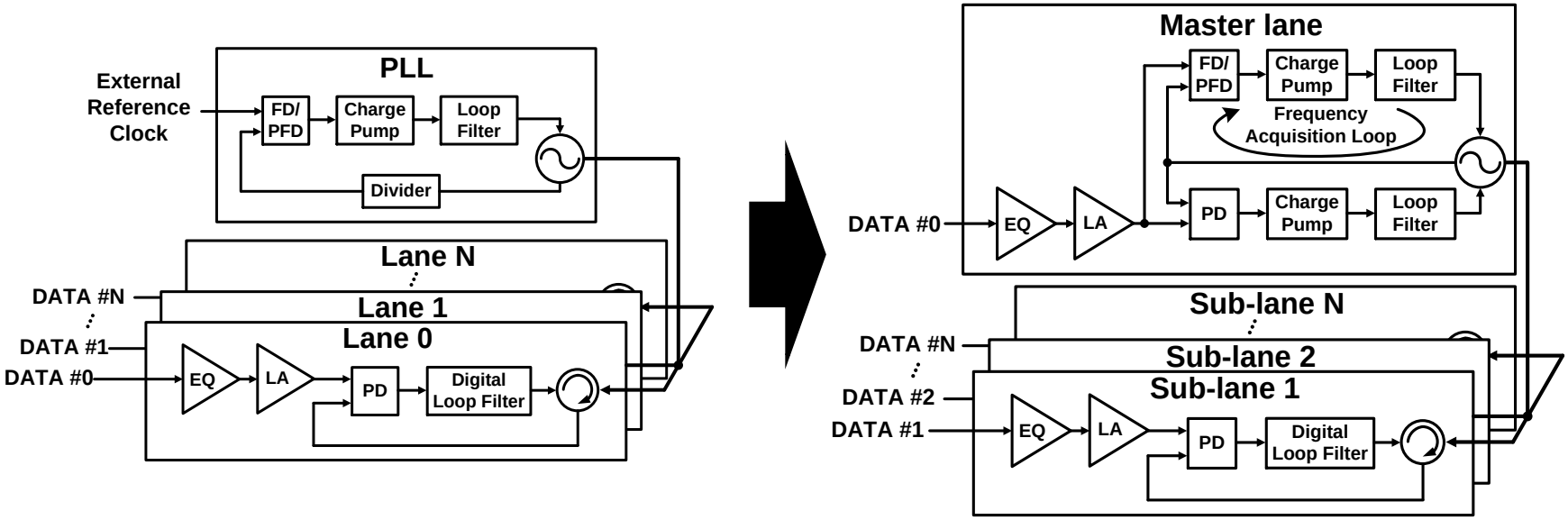
- PI-based PLL



- ☺ Power-and-area efficiency
- ☺ Good jitter performance
- ☺ Robustness to interference

Motivation

- When the reference clock signal is absent,
  - Conventional PI-based CDR designs do not have operational independency between lanes.



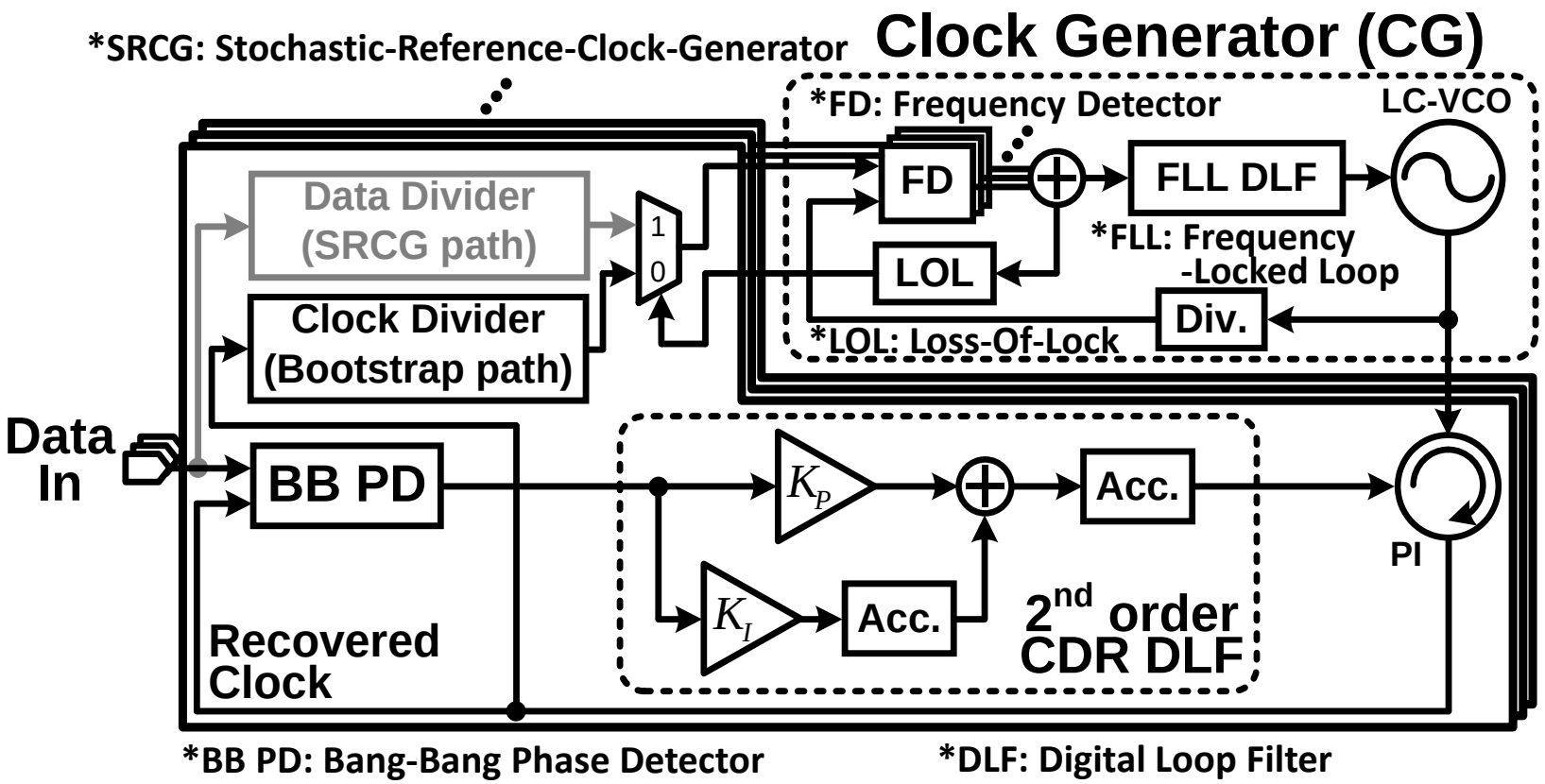
→ **Reference-less and independent lane operations are** required.

Solution

- A low-power small-area 10×10 Gb/s reference-less and lane-independent PI-based parallel TRX
  - Entire lanes operate independently with no reference clock signal or performance penalty by using **a bootstrap technique.**
  - PI output clock signals that are phase locked to the input data are used for the VCO frequency locking.

Reference-less and lane-independent parallel bootstrap CDR

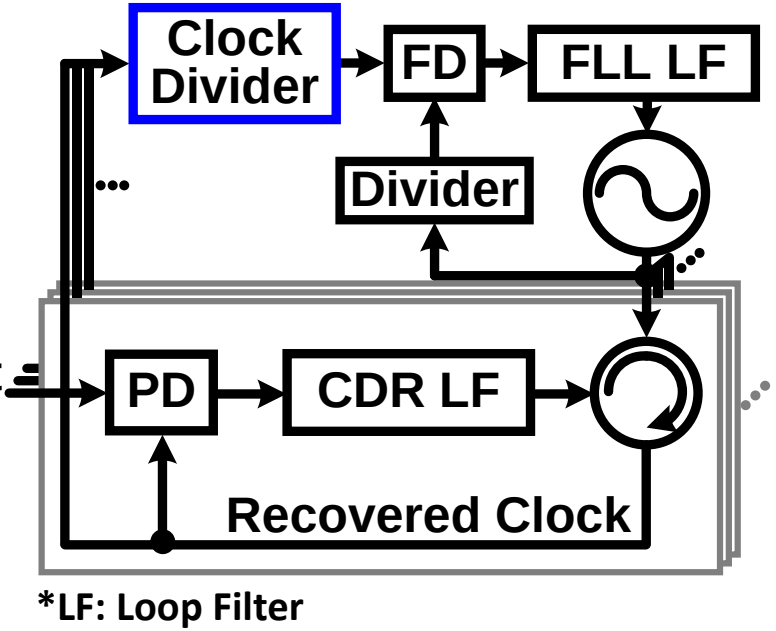
- Entire lanes operate independently as in VCO-based parallel reference-less designs.



Bootstrap CDR

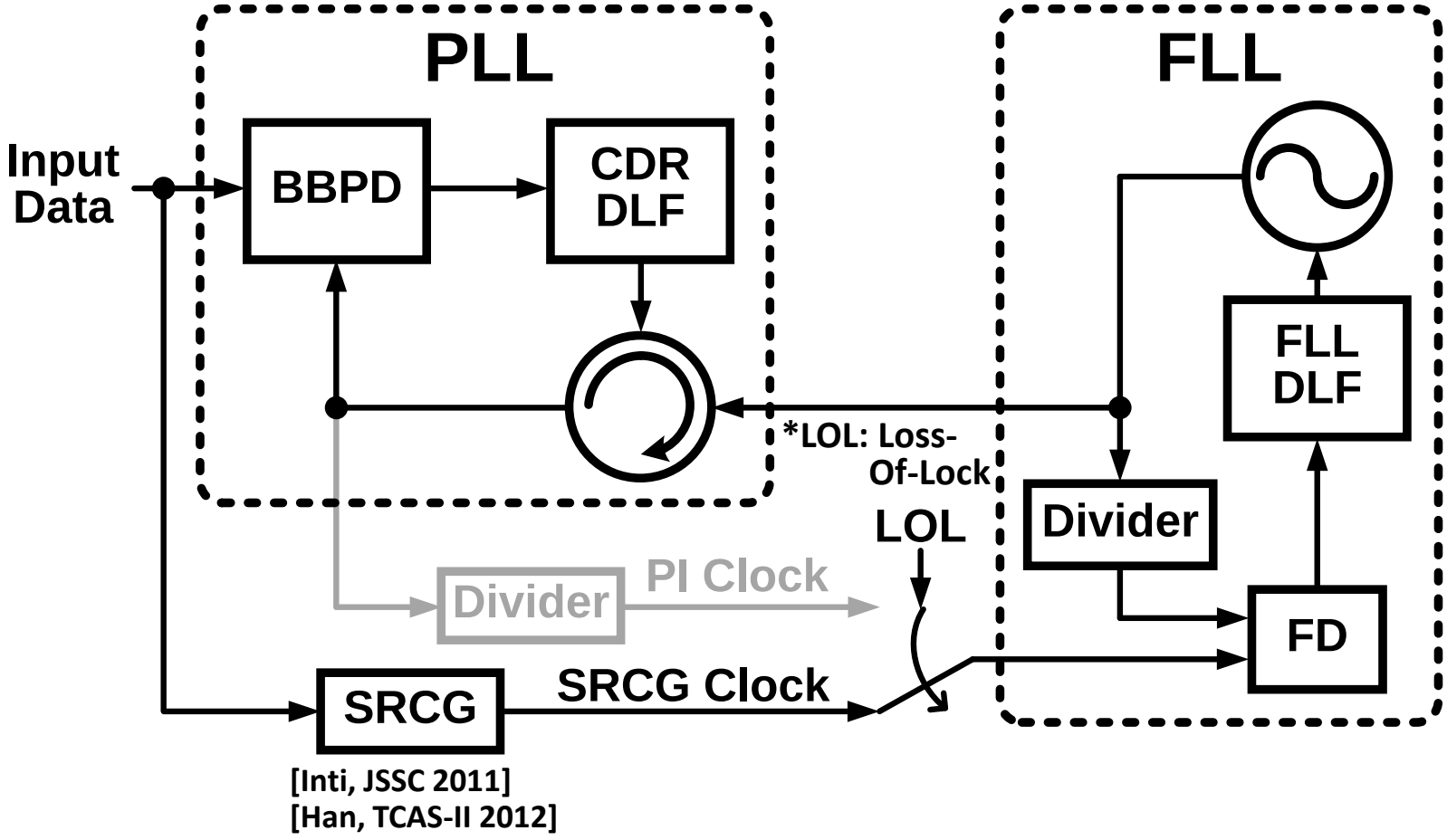
- The frequency information of each lane should be monitored continuously.
  - The VCO should be neither phase nor frequency-locked to a specific lane.
  - A low-power frequency acquisition scheme is critical.

- The bootstrap CDR has negligible power-and-area overhead.
  - The clock divider is the only addition made to the system.



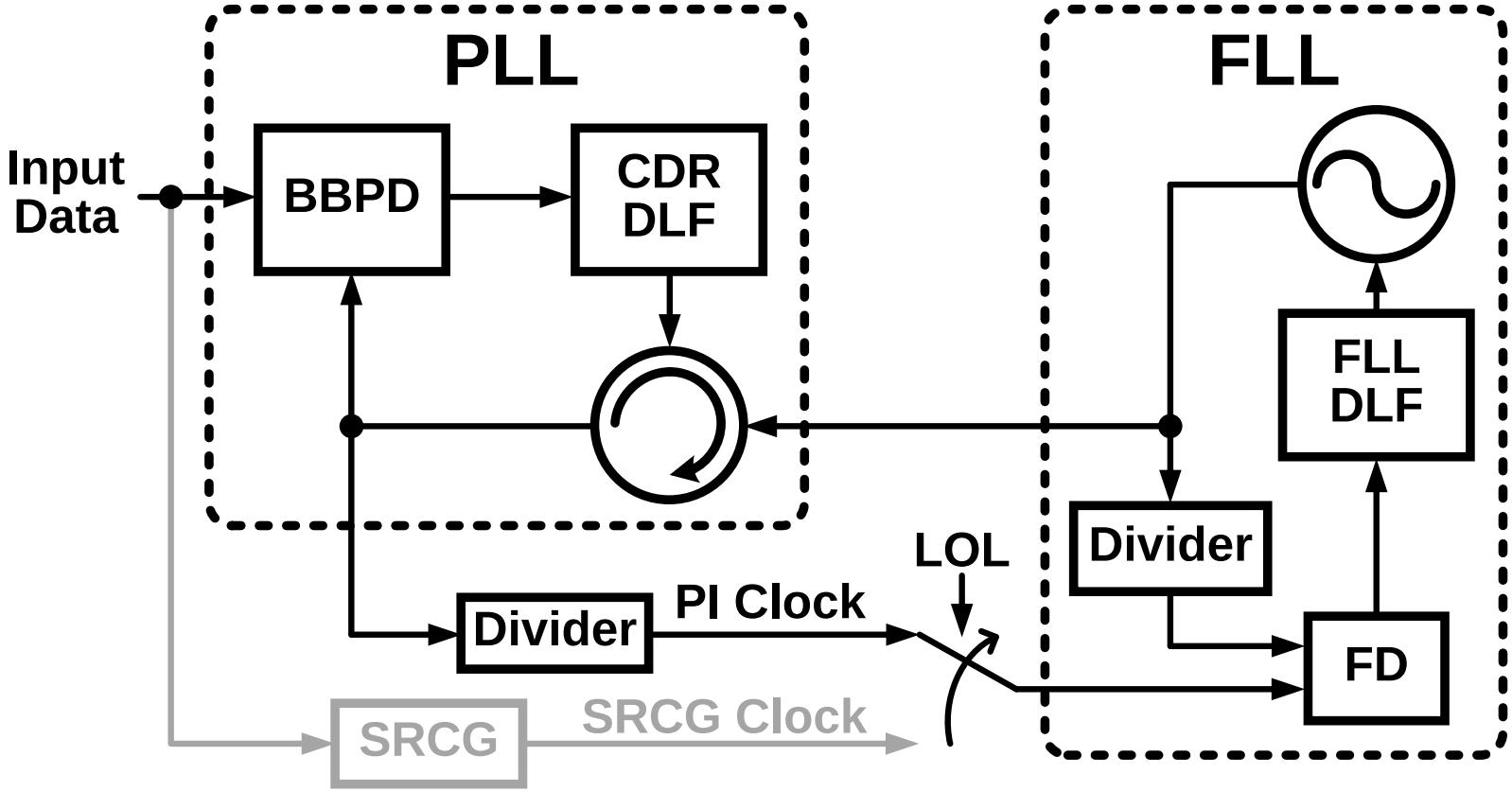
Bootstrap CDR

- Initial frequency acquisition: SRCG mode



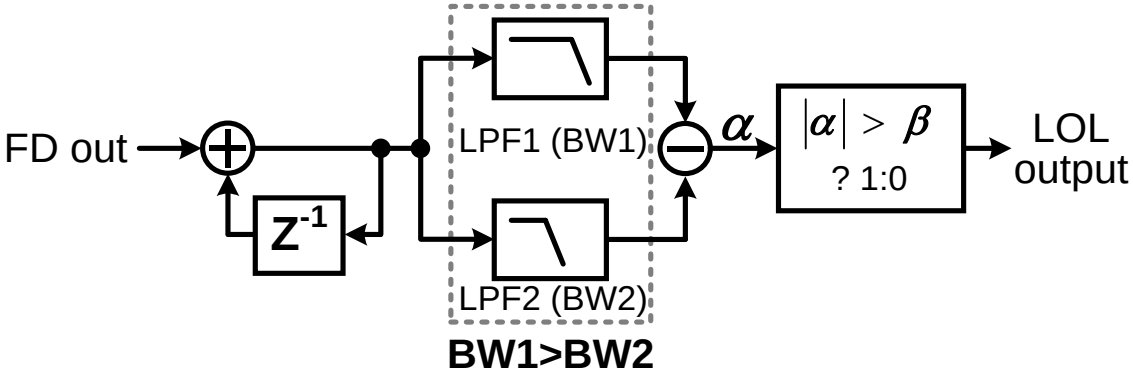
Bootstrap CDR

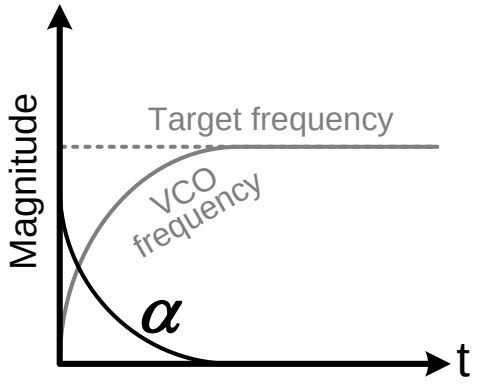
- Bootstrap mode



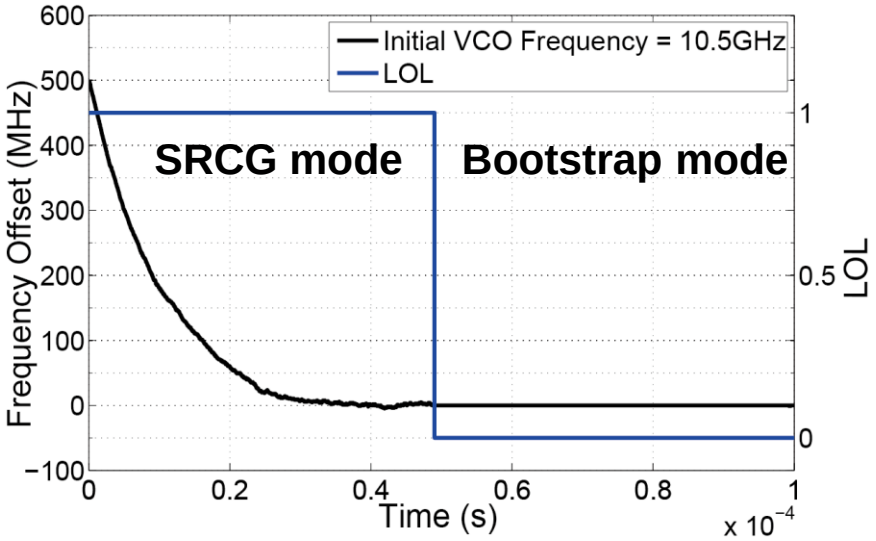
FLL LOL

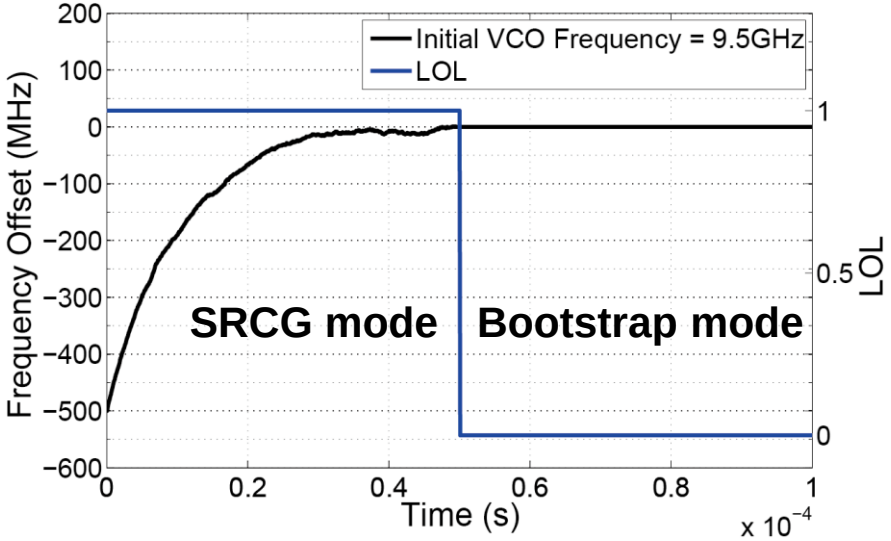
- LOL utilizes frequency errors from FDs





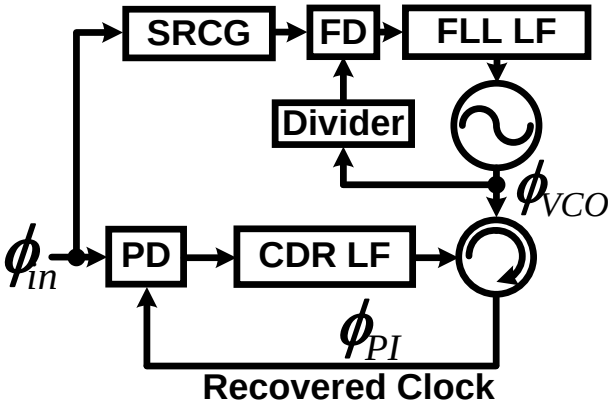
- MATLAB simulation results



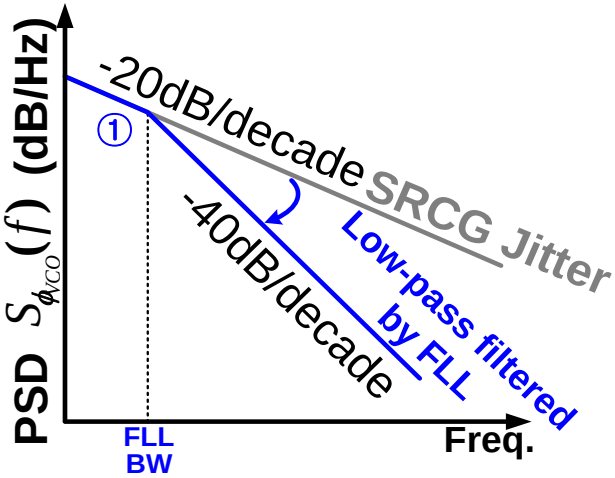


Phase noise progression

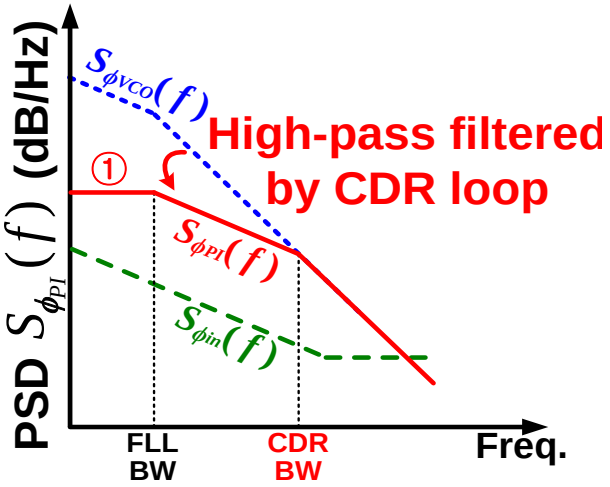
- SRCG mode



- VCO

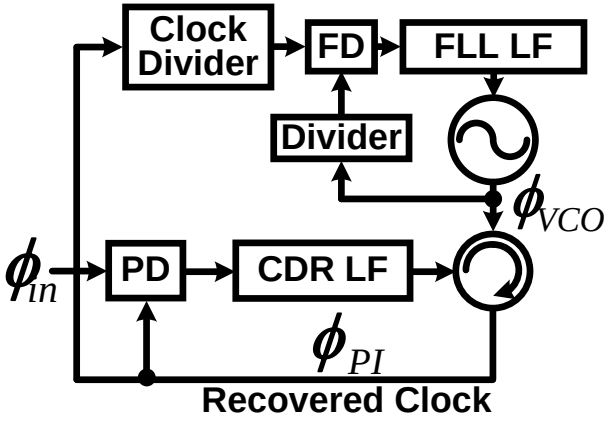


- PI

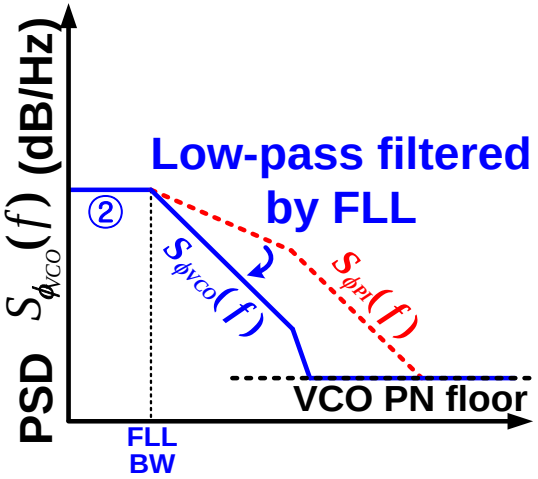


Phase noise progression

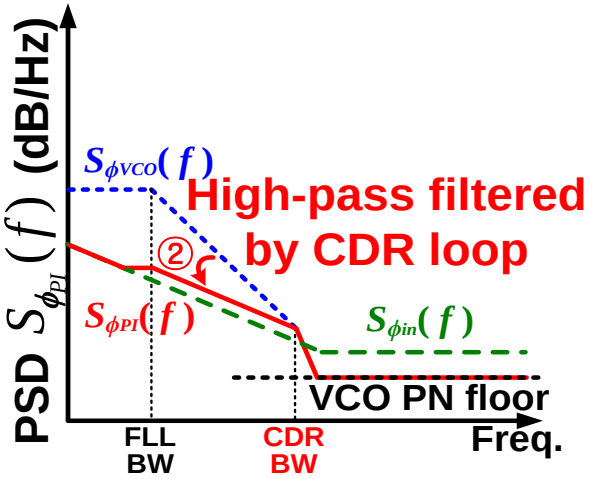
- Bootstrap mode



- VCO



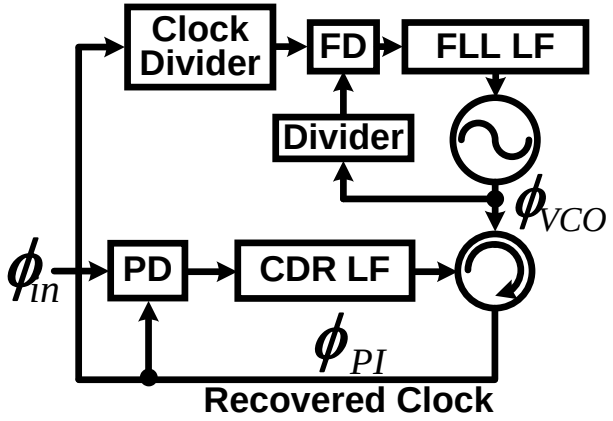
- PI



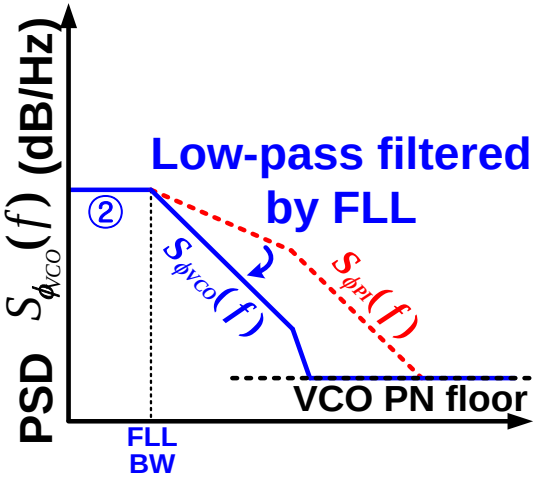
Cleaner VCO ➔ Cleaner Rotator ➔ Cleaner VCO ➔ …

Phase noise progression

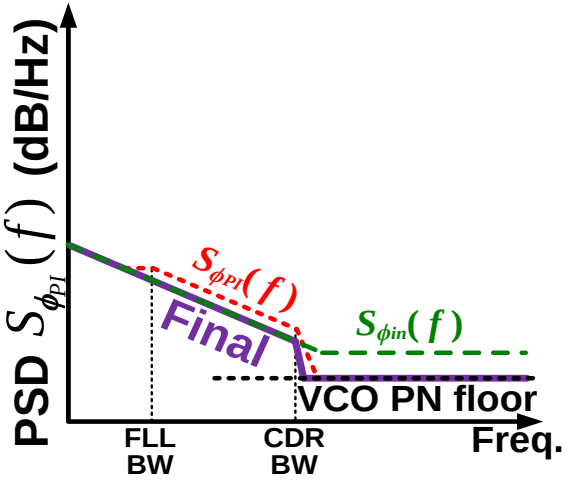
- Bootstrap mode



- VCO



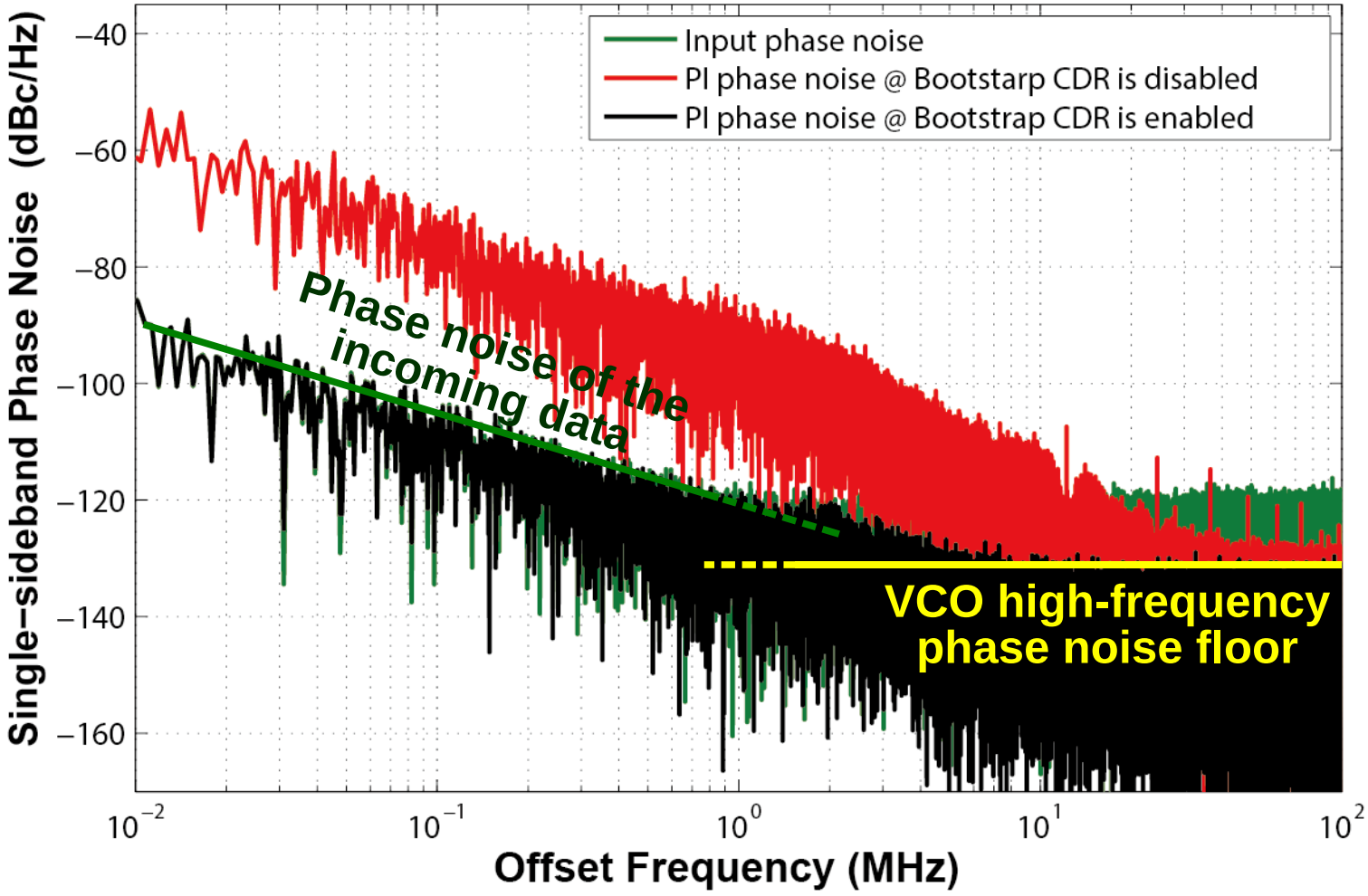
- PI



Cleaner VCO → Cleaner Rotator → Cleaner VCO → … → Bootstrap

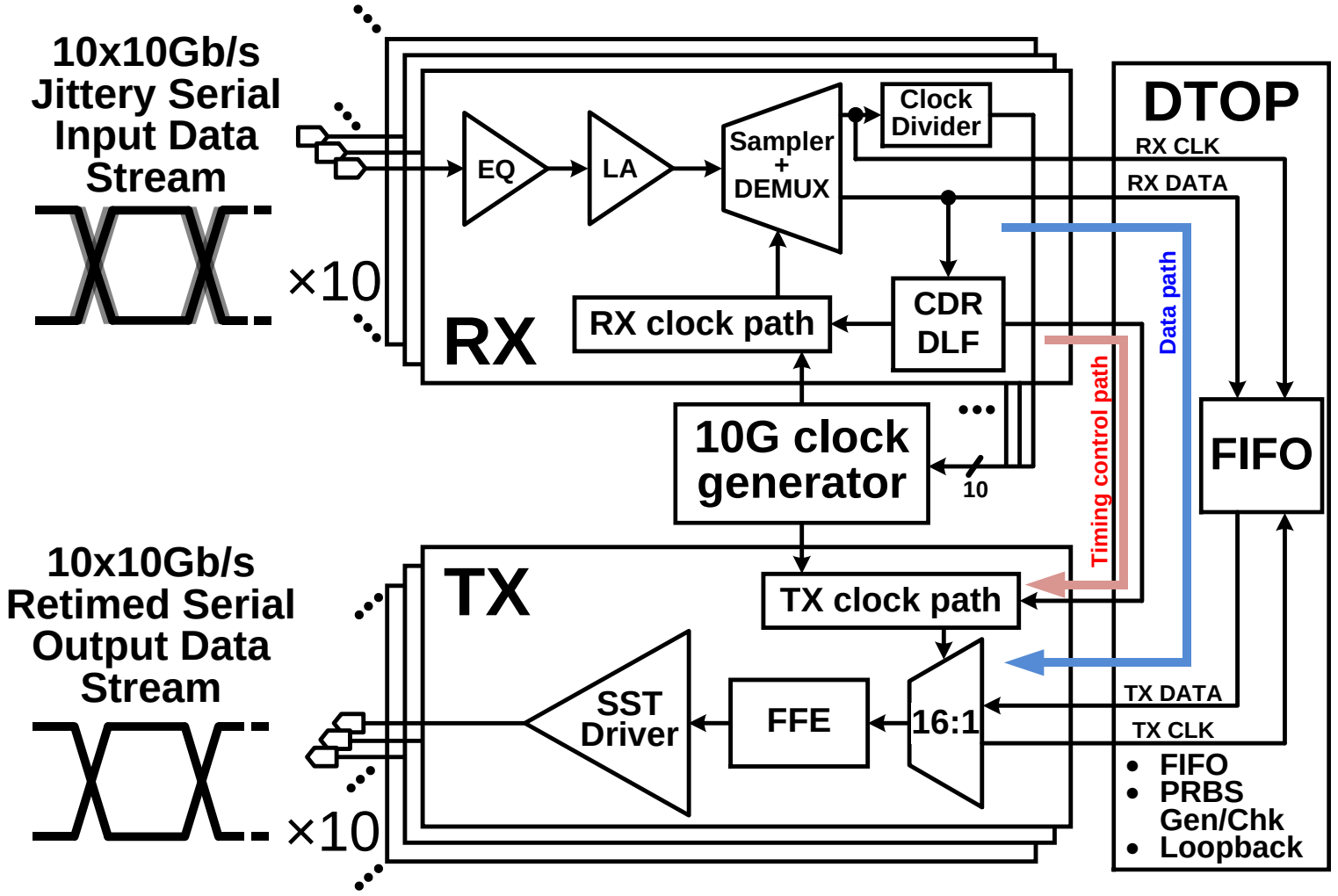
Phase noise progression

- MATLAB simulation result



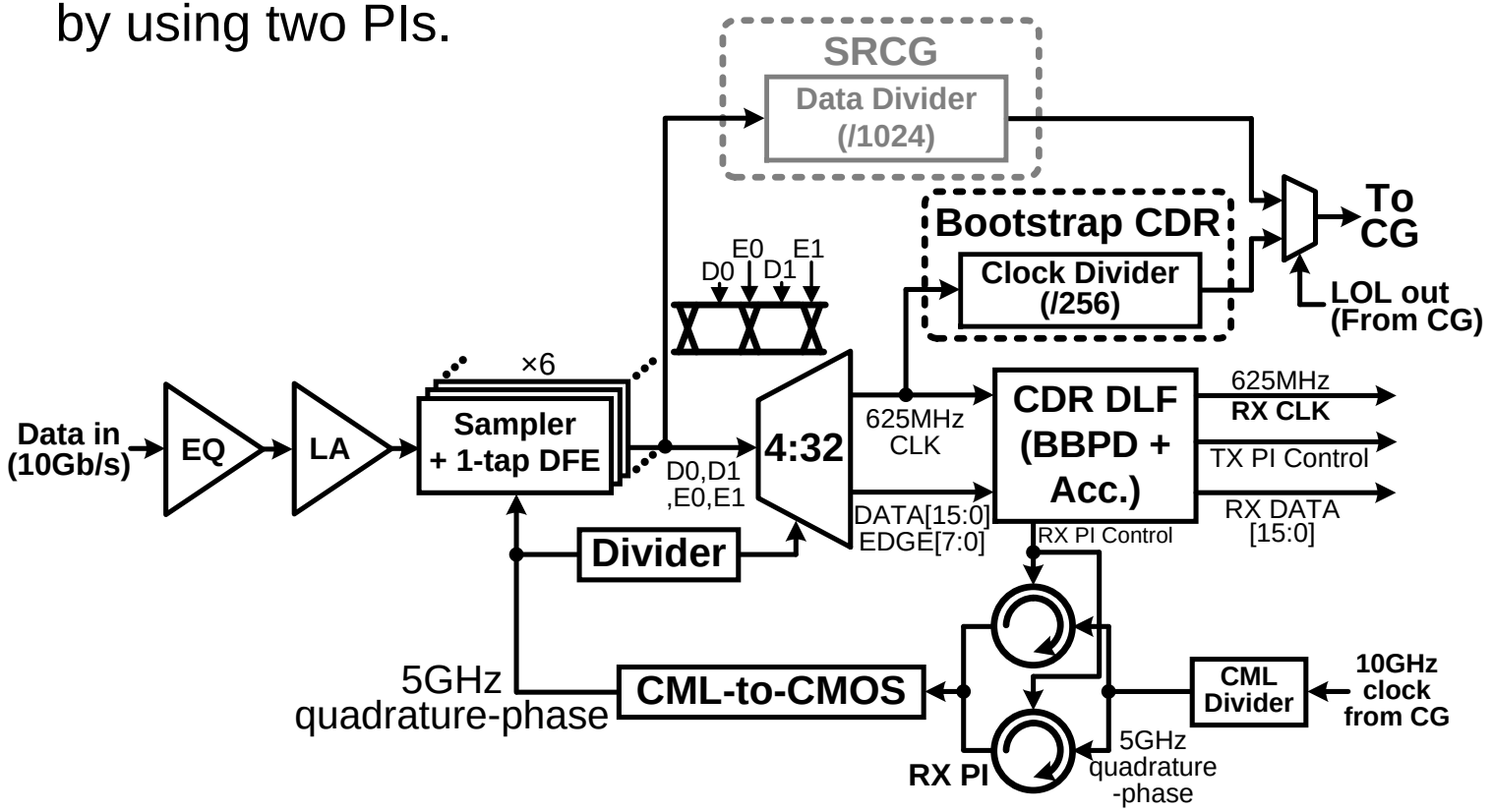
TRX design

- 10×10Gb/s RX, 10×10Gb/s TX, 10GHz CG



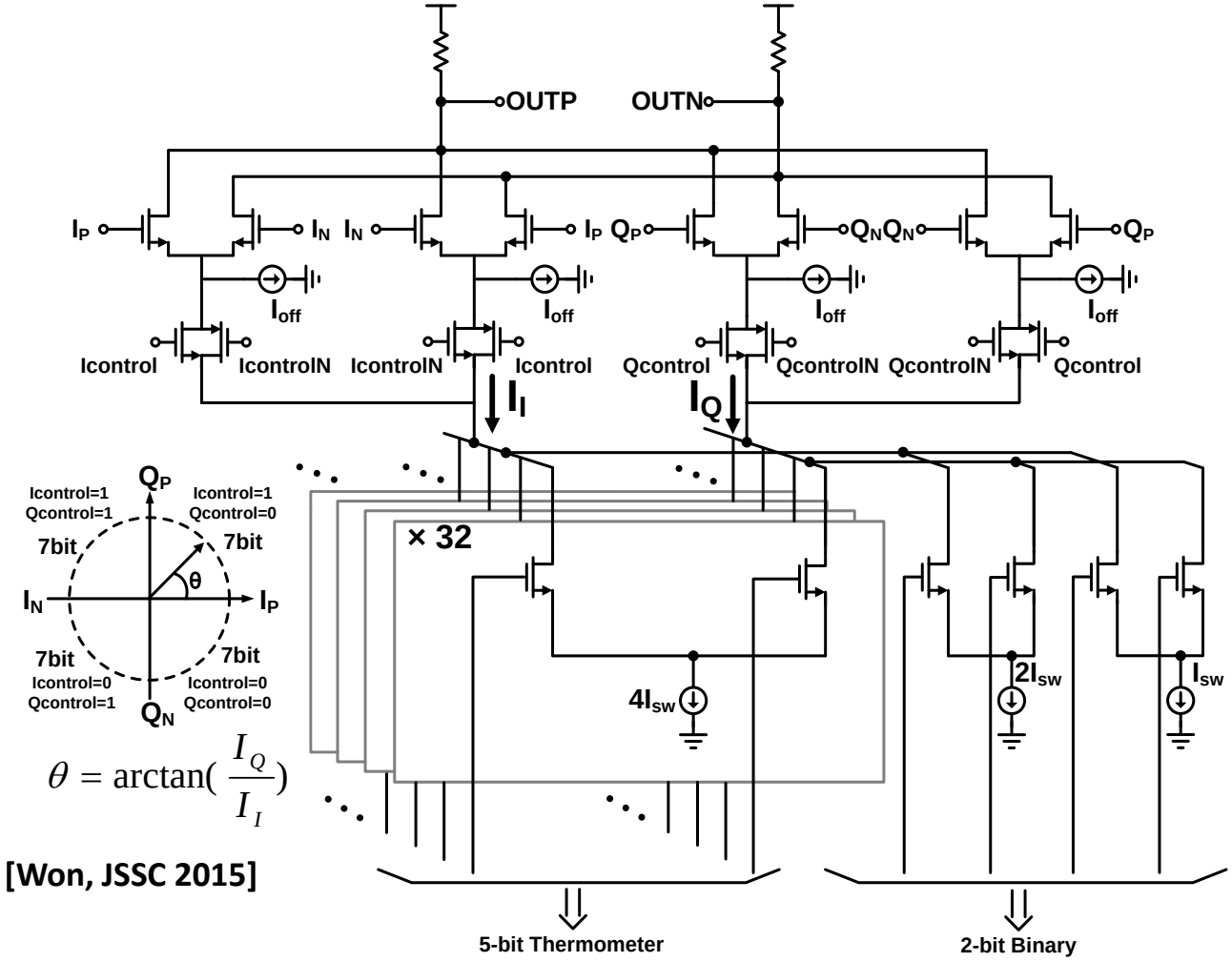
RX design

- Half-rate clocking scheme
- EQ (10dB boosting gain) + LA (25dB gain) + 1-tap loop-unrolled DFE
- The CDR DLF adjusts the phase of the clock signal from the CG by using two PIs.



PI design

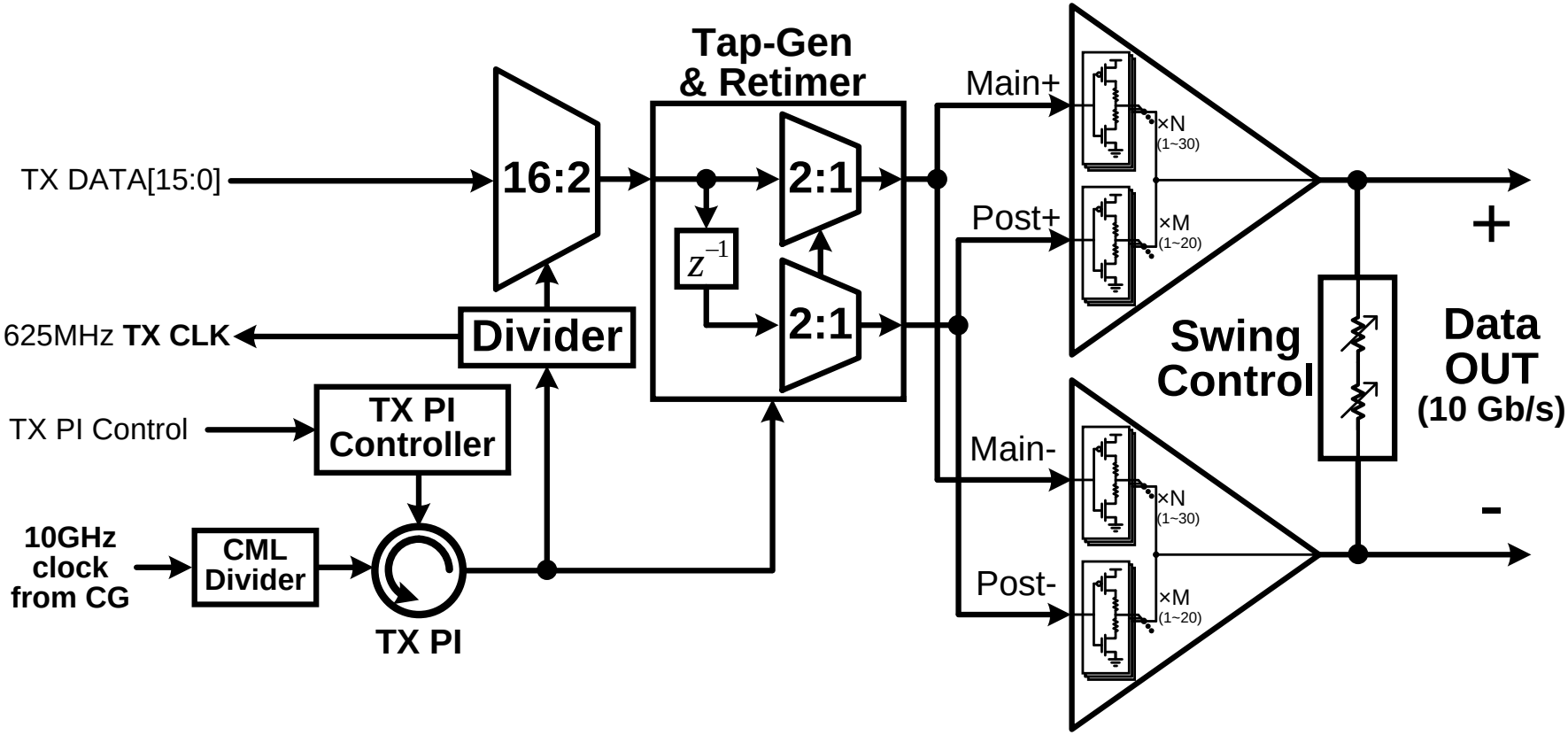
- 9-bit PI operating at half-rate



[Won, JSSC 2015]

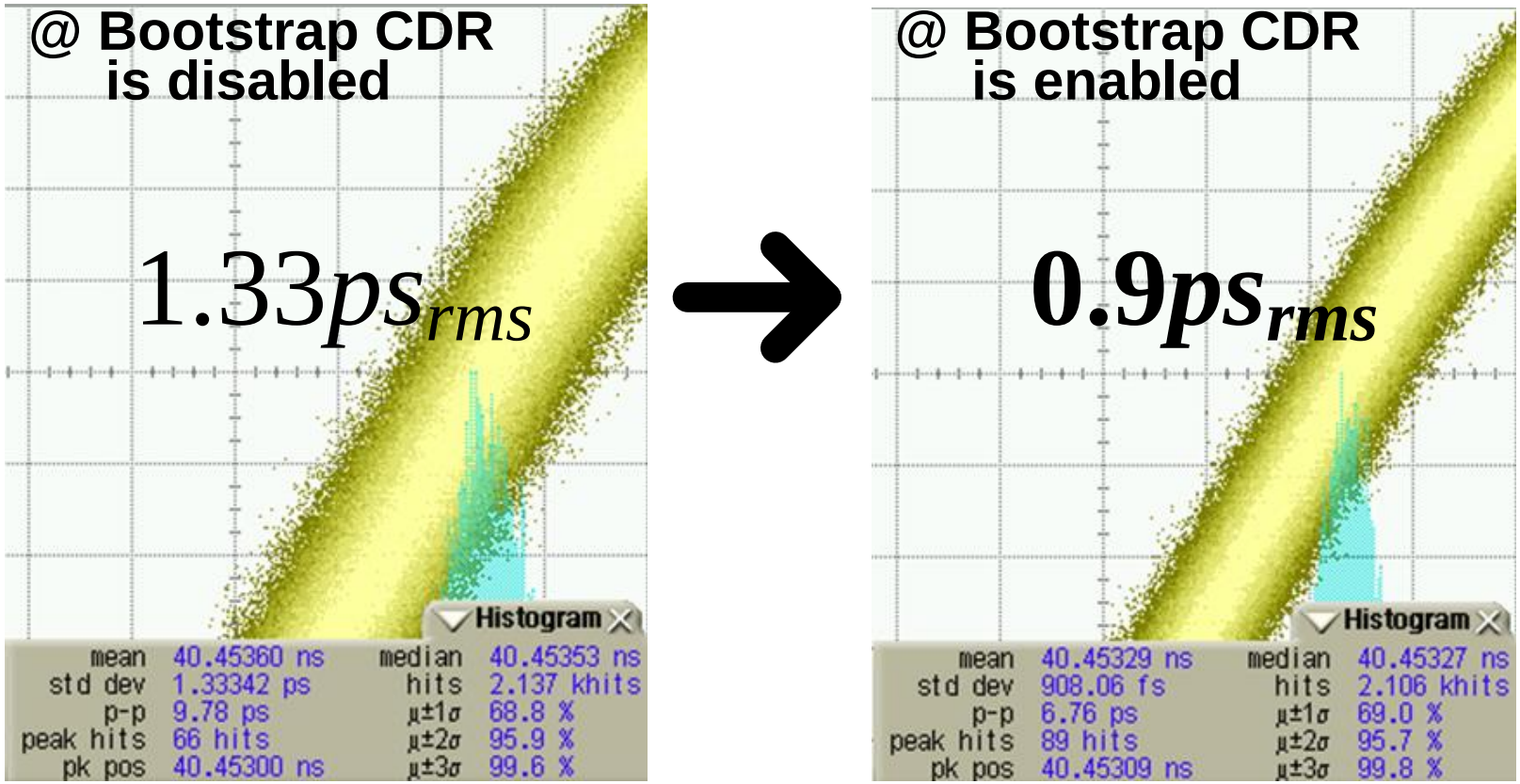
TX design

- Half-rate clocking scheme
- Source-Series-Terminated (SST) output driver
  - Output swing: 0.3 Vppd to 0.9 Vppd
  - Output impedance is made tunable for 50Ω matching.



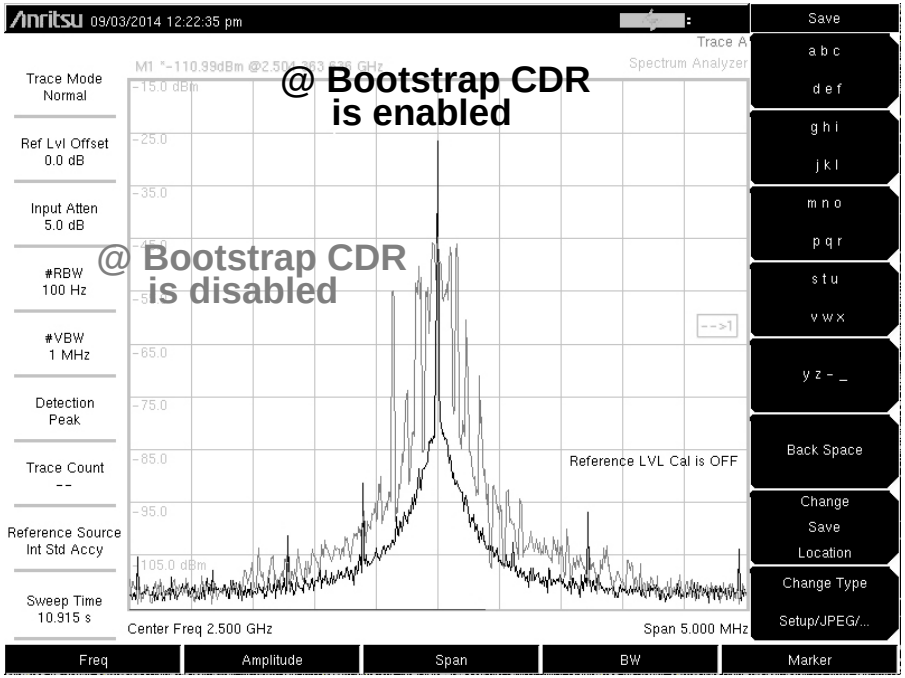
Jitter measurement

- RX clock jitter (2.5 GHz)

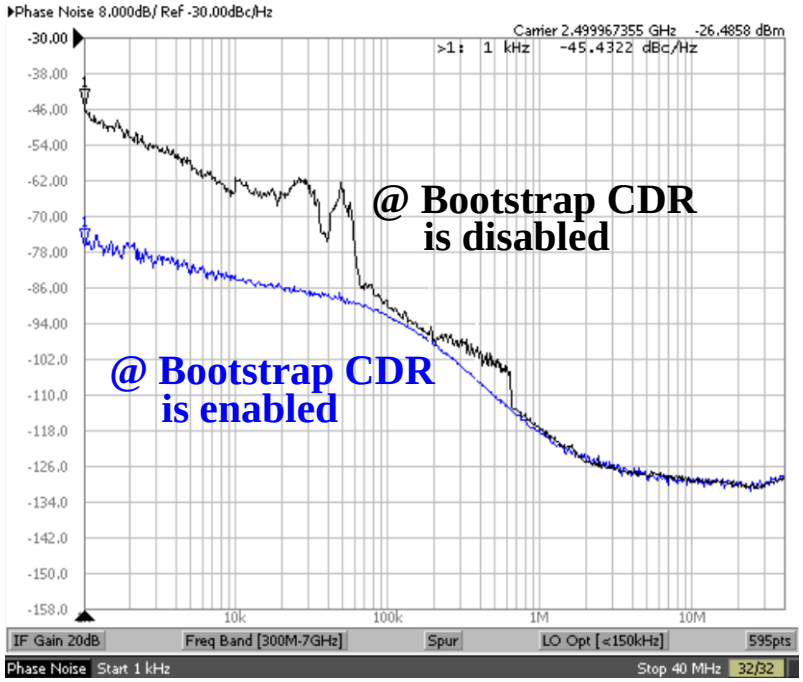


Spectra and phase noise

- VCO divided clock (2.5 GHz)

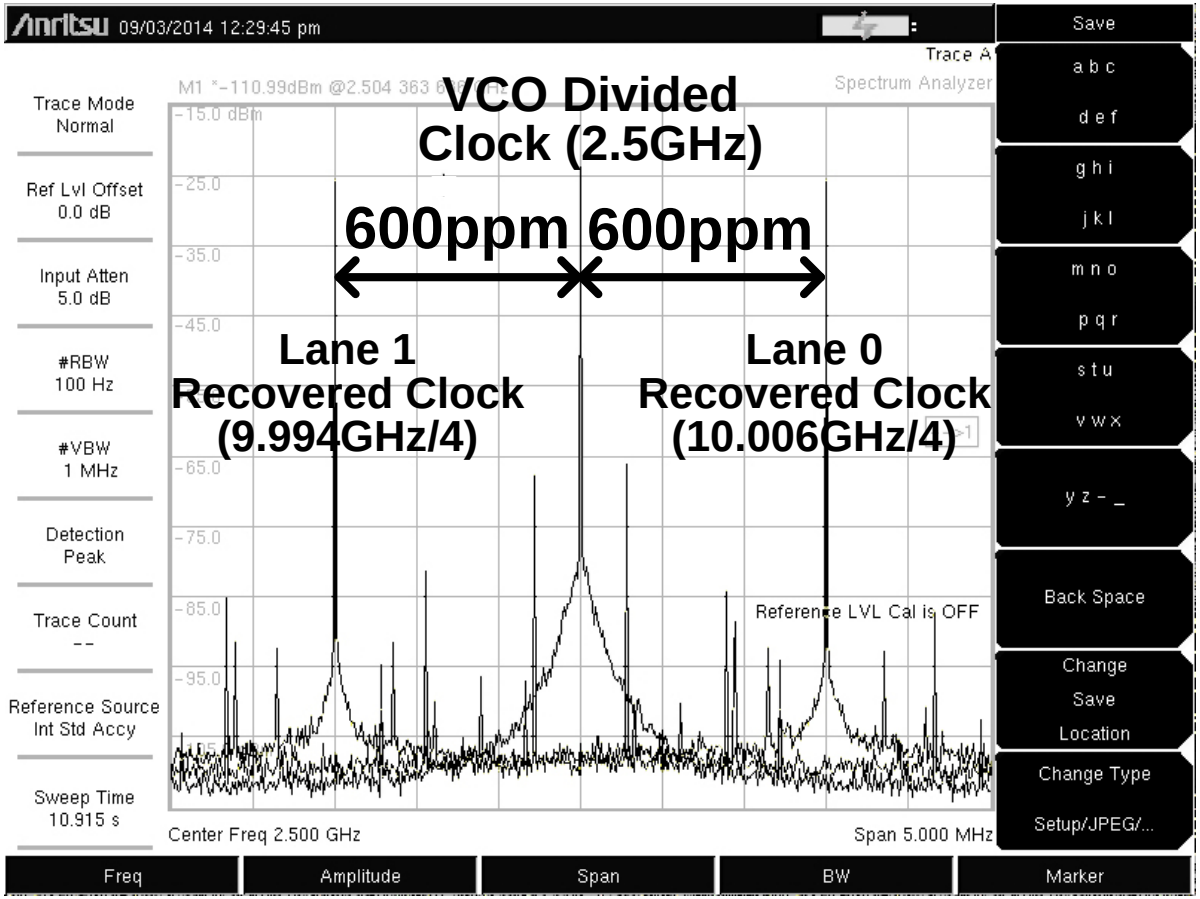


- PI divided clock (2.5 GHz)



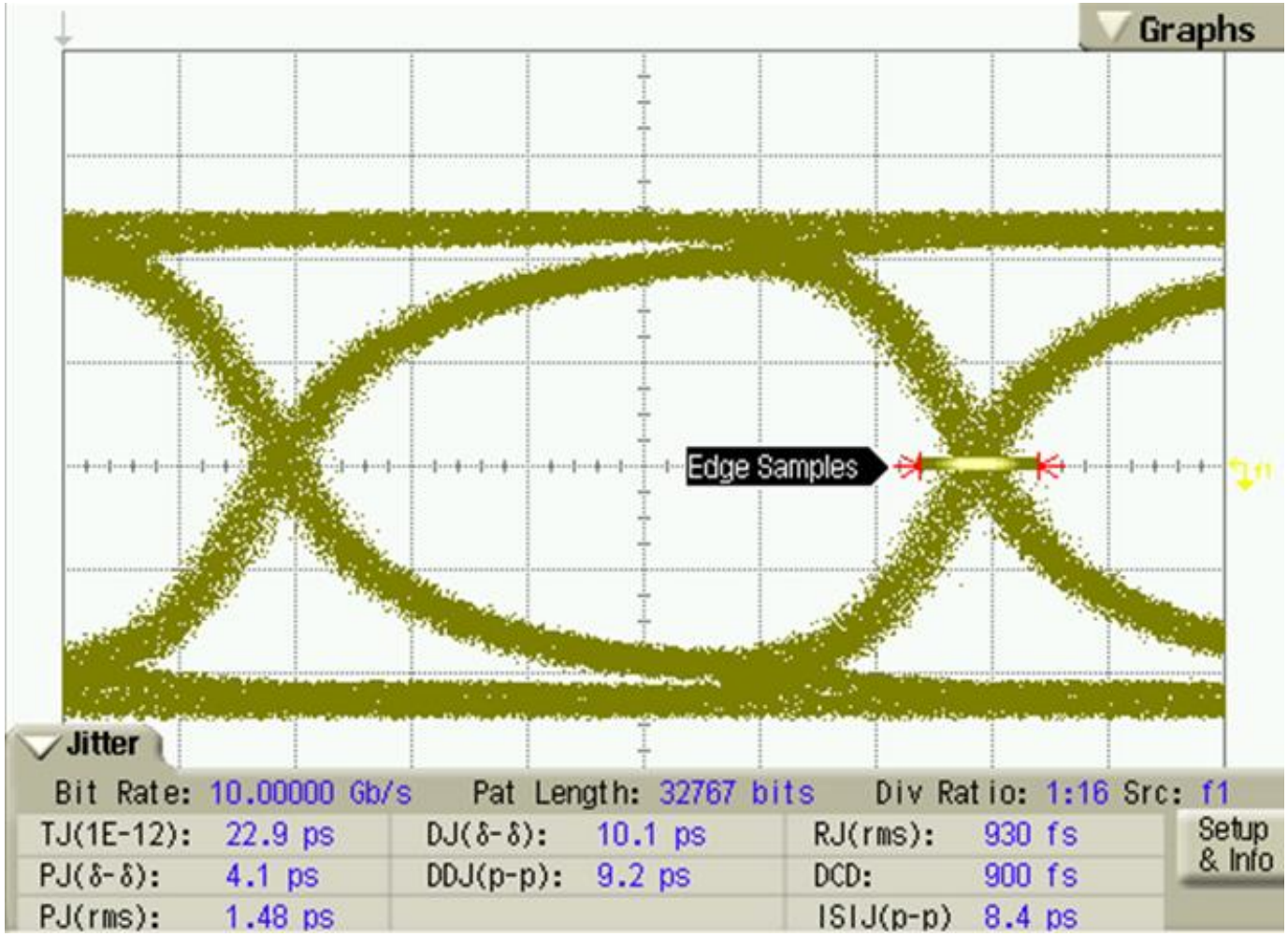
Spectra measurement

- VCO frequency is equal to the average data rate of the input signals.



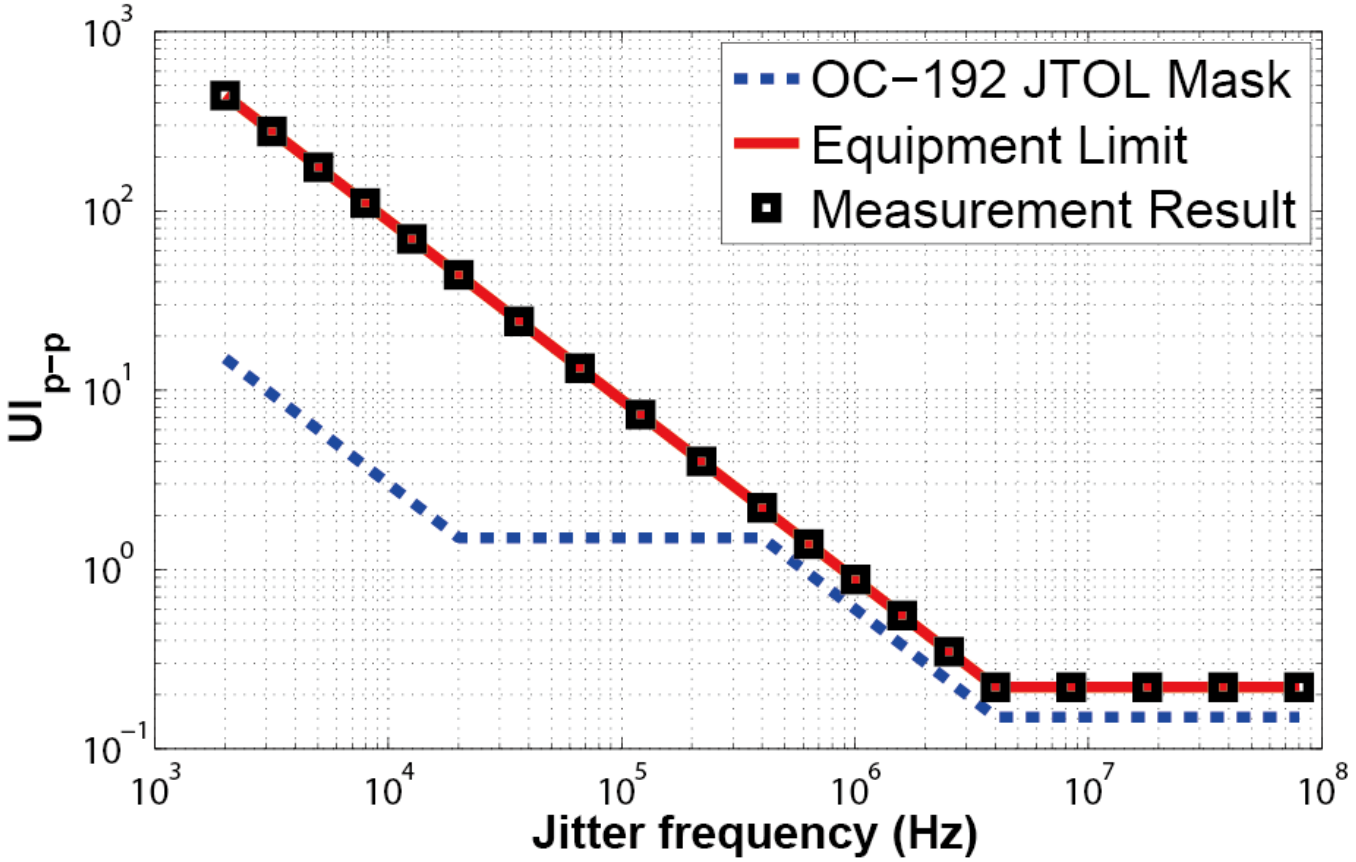
Eye measurement

- TX output jitter is 0.93 ps_{rms}.



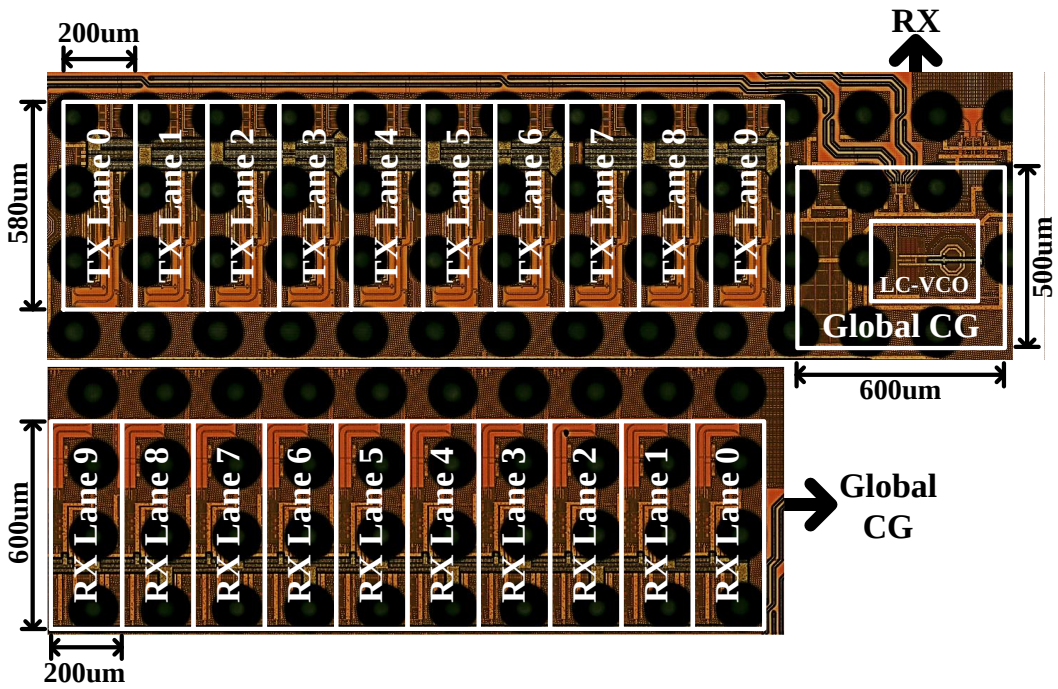
Jitter tolerance measurement

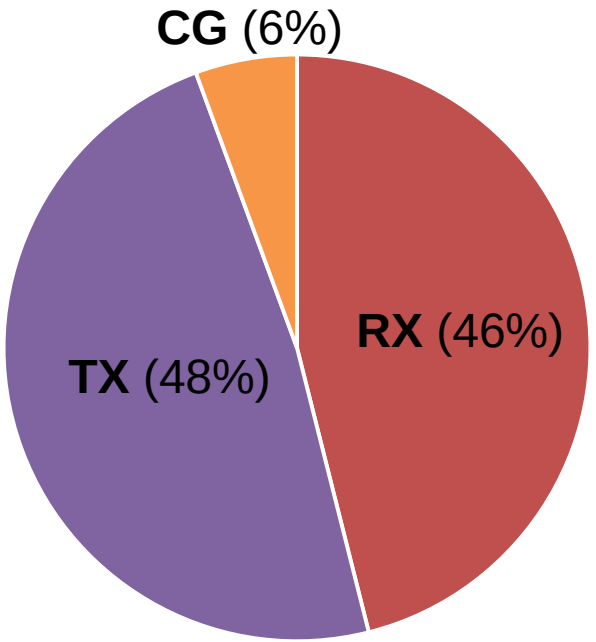
- The transceiver passes OC-192 jitter-tolerance specification.



Chip microphotograph and power breakdown

- 40 nm CMOS, flip-chip packaged
- RX: 0.12mm^2, TX: 0.116mm^2, CG: 0.3mm^2





Total Power: 440.7 mW
Single TRX power: 41.7 mW

Performance summary and comparison

	This work	[1]	[2]	[6]
Process	**40 nm**	90 nm	0.13 um	65 nm
Supply	**0.9 V**	1.5 V	1.2 V	1.0 V
Data rate	**10-parallel 8.9 to 12 Gb/s**	20 Gb/s (950Mb/s operation range)	1.62 to 2.7 Gb/s	8.5 to 11.5 Gb/s
Reference-Less Design	**Bootstrap CDR & SRCG**	Pottbacker FD	Weighted-PFD	Modified Digital Quadricorrelator
Lane-independent Design	**PI-based lane-independent Design**	-	VCO-based lane-independent Design	-
Figure-of-Merit (mW/Gb/s)	**RX: 2.03, TX: 2.13 (@ 10 x 10 Gb/s, TX swing: 839 $mV_{pp-diff}$)**	7.7 (@ 20 Gb/s, without I/O buffers)	8.52 (@ 2.7 Gb/s, RX only)	5.2 (@ 11.5 Gb/s, CDR only)
Area (mm^2)	**RX: 0.12, TX: 0.116, CG: 0.3**	0.85 (CDR only)	0.94	0.97
Data Jitter (rms)	**0.93 ps**	0.48 ps	1.57 ps	0.205 ps
Input Sensitivity	**9.8 $mV_{pp-diff}$ (4.9 $mV_{pp-single}$)**	-	-	10 $mV_{pp-diff}$
Bit error rate	**$<10^{-13}$**	$<10^{-13}$	$<10^{-12}$	$<10^{-12}$

Conclusion

- **The PI-based bootstrap TRX for reference-less and lane-independent operation is presented.**
  - The bootstrapping between the VCO and PIs minimizes the phase noise.
  - Entire lanes operate independently with no reference clock signal or performance penalty.
- **The proposed PI-based architecture is suitable for high-speed parallel interconnections.**
  - Area efficiency
  - Low-power consumption
  - Robustness

Thank You.

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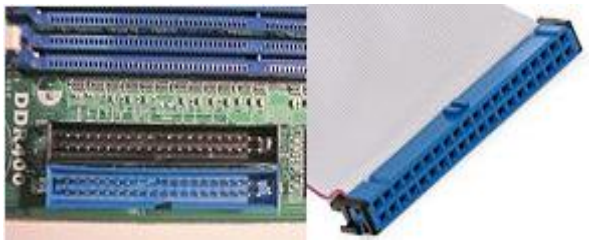
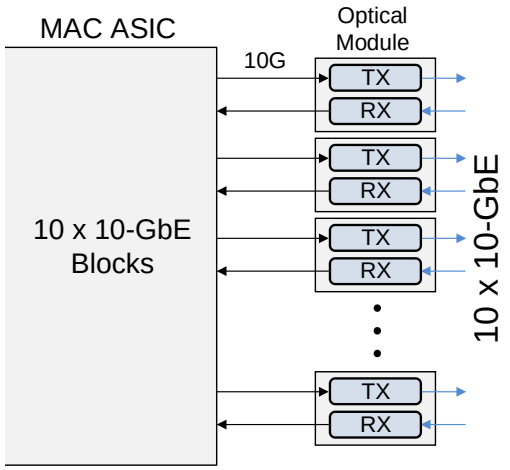
Appendix

History of Data Transmission System





Parallel Bus

- Simple structure
- Ex) PATA, PCI

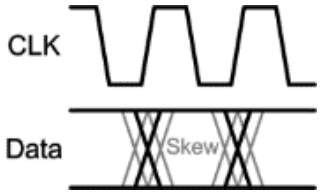
Serial Communication

- Less channel resources
- Ex) SATA, PCIe

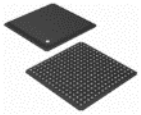
Parallel Communication

- Bunch of serial links
- Ex) 40G,100G Ethernet

Skew problem

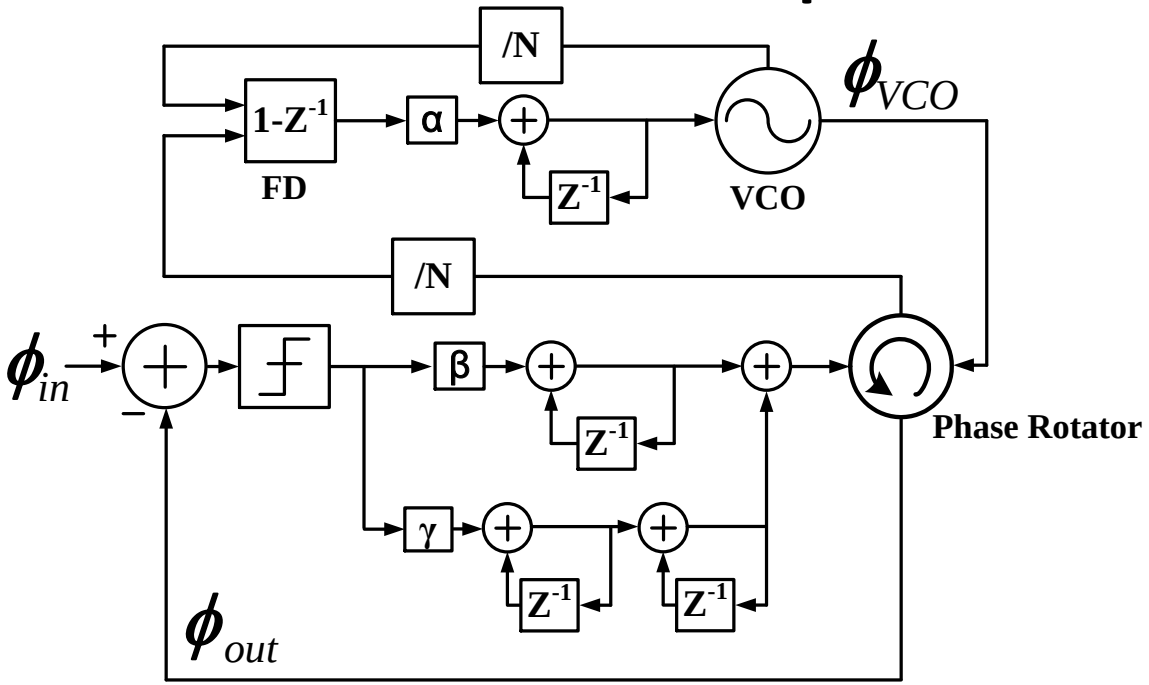


Package limit (BGA <= 28G)



Bootstrap CDR

- **Transfer function of the bootstrap CDR**



By taking the bilinear transformation

$$(\phi_{in}-\phi_{out})K_{bbpd}\theta\left(\frac{\beta(1+sT_0/2)}{sT_0}+\frac{\gamma(1+sT_0/2)^2}{s^2T_0^2}\right)+\phi_{VCO}=\phi_{out}\cdots(1)$$

$$(\phi_{out}-\phi_{VCO})\alpha\frac{K_{VCO}}{Ns}=\phi_{VCO}\cdots(2)$$

Bootstrap CDR

By substituting (2) into (1)

$$\frac{\phi_{out}}{\phi_{in}} = T(s) = \frac{N(s)}{D(s)}$$

$$N(s) = K_{bbpd}\theta\left(\left(\frac{T_0^2\gamma}{4} + \frac{T_0^2\beta}{2}\right)s^2 + T_0(\gamma+\beta)s + \gamma\right)(Ns + \alpha K_{VCO})$$

$$D(s) = NT_0^2\left(K_{bbpd}\theta\left(\frac{\gamma}{4} + \frac{\beta}{2}\right) + 1\right)s^3 + K_{bbpd}\theta T_0\left(N(\gamma+\beta) + \alpha K_{VCO}\left(\frac{T_0\gamma}{4} + \frac{T_0\beta}{2}\right)\right)s^2$$
$$+ K_{bbpd}\theta(N\gamma + \alpha K_{VCO}T_0(\gamma+\beta))s + \alpha K_{bbpd}K_{VCO}\theta\gamma$$

* T_0: Clock period of the digital block = $1/f_S$

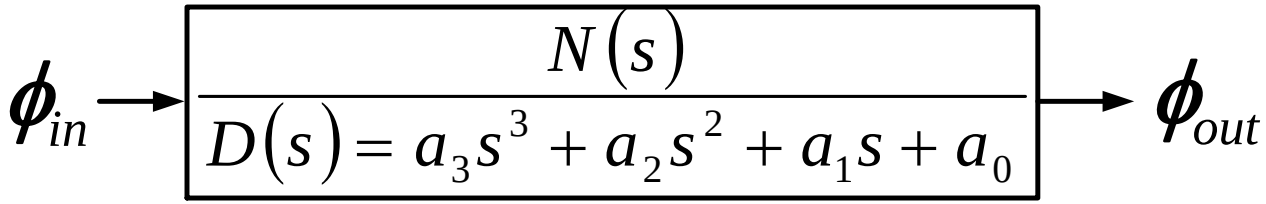
If $\beta >> \alpha, \gamma$

$$\frac{\phi_{out}}{\phi_{in}} \approx \frac{K_{bbpd}\theta\beta}{T_0 s + K_{bbpd}\theta\beta}$$

Bootstrap CDR

- **Stability of the bootstrap CDR**

Routh-Hurwitz criterion for stability

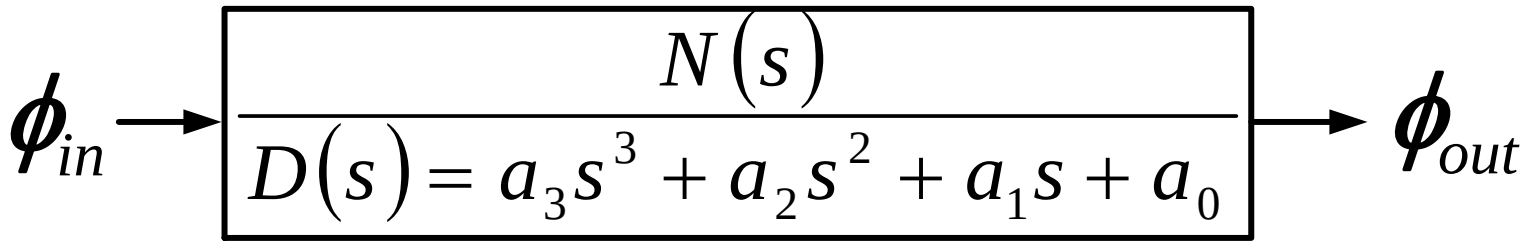


Completed Routh table

s^3	a_3	a_1
s^2	a_2	a_0
s^1	$-\frac{\begin{vmatrix} a_3 & a_1 \\ a_2 & a_0 \end{vmatrix}}{a_2} = b_1$	0
s^0	$-\frac{\begin{vmatrix} a_2 & a_0 \\ b_1 & 0 \end{vmatrix}}{b_1} = c_1$	0

A system is stable if there are no sign changes in the first column of the Routh table

Bootstrap CDR



$$D(s)=NT_0^2\left(K_{bbpd}\theta_{pr}\left(\frac{\gamma}{4}+\frac{\beta}{2}\right)+1\right)s^3+K_{bbpd}\theta_{pr}T_0\left(N(\gamma+\beta)+\alpha K_{VCO}\left(\frac{T_0\gamma}{4}+\frac{T_0\beta}{2}\right)\right)s^2$$
$$+K_{bbpd}\theta_{pr}\left(N\gamma+\gamma K_{VCO}T_0(\gamma+\beta)\right)s+\alpha K_{bbpd}K_{VCO}\theta_{pr}\alpha,$$

The system is stable, when

$$N^2K_{bbpd}\theta_{pr}\alpha\beta+N\gamma K_{bbpd}K_{VCO}\theta_{pr}T_0\beta^2+0.5\gamma^2K_{bbpd}K_{VCO}\theta_{pr}T_0^2\beta^2-N^2\gamma K_{VCO}\alpha T_0>0$$

Therefore, the system is stable under the general condition

$$\beta >> \alpha,\ \beta >> \gamma\,.$$