# *A 4mW Wide Bandwidth Ring-Based Fractional-N DPLL with 1.9ps$_{rms}$ Integrated-Jitter*

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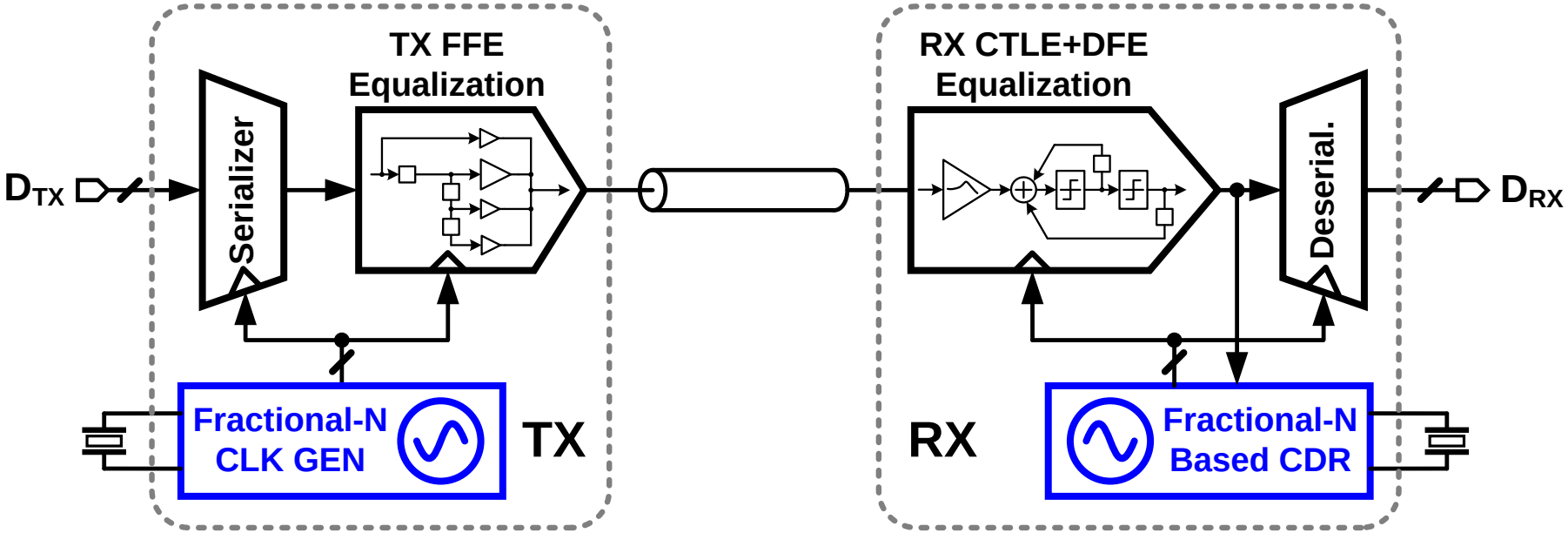
Custom Integrated Circuits Conference (CICC)

# *Outline*

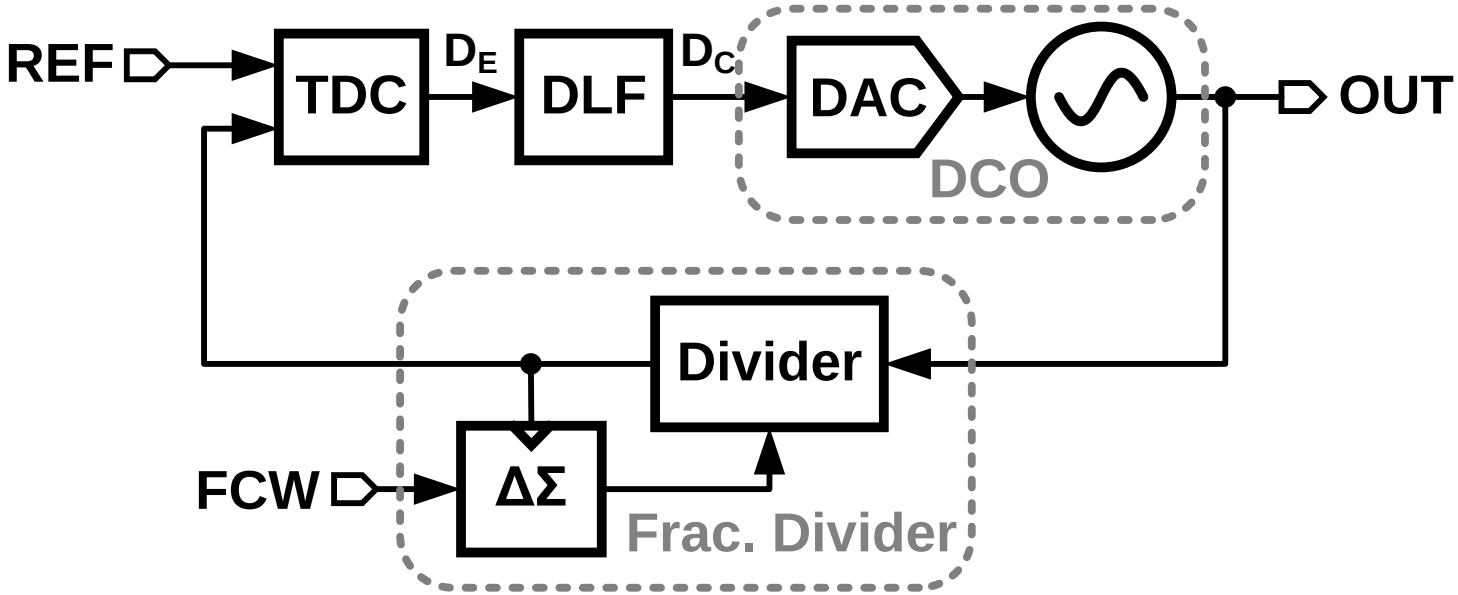
- **Motivation**
- **Proposed Architecture**
- **Circuit Implementation**
- **Measurement Results**
- **Conclusions**

# Motivation




- **Multi-standard/Flexible SERDES**
  - **Wide and continuous range of data-rates**
- **Fractional-N synthesis in TX and RX**
  - **Flexible, low jitter, wide range, multi-phases, …**

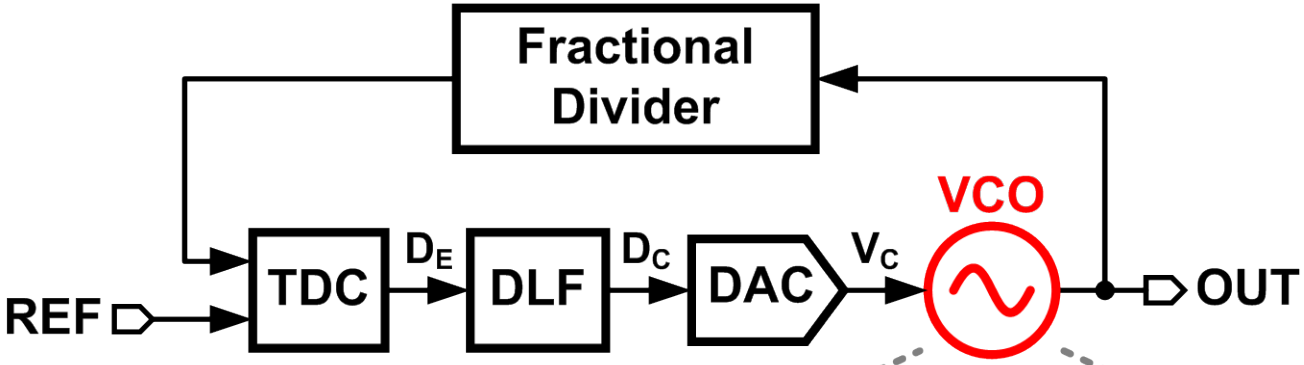
# Digital Fractional-N PLL



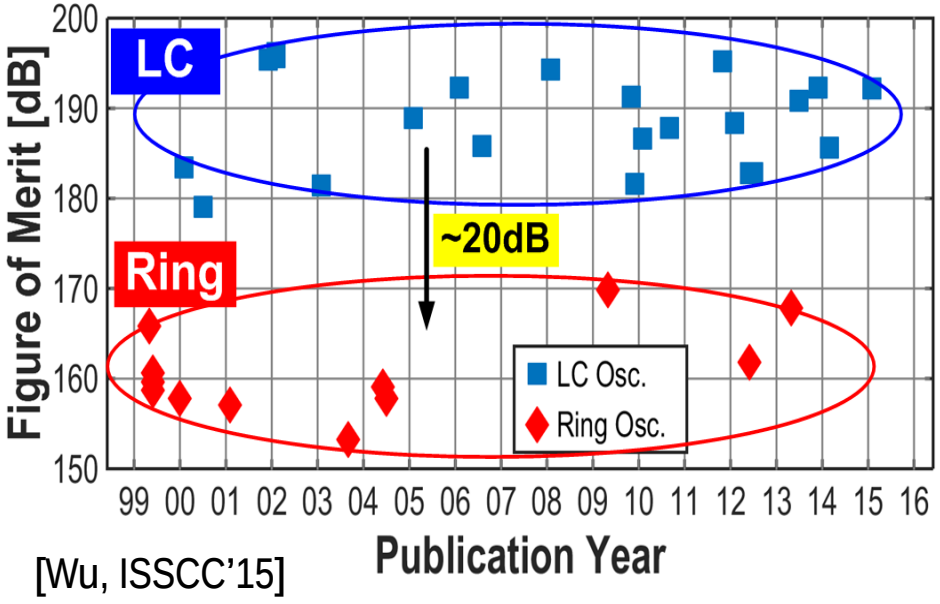

✓ **Digital LF: reconfigurable, scalable, small area**

× **Quantization noise: TDC, DCO, and ΔΣ fractional divider**

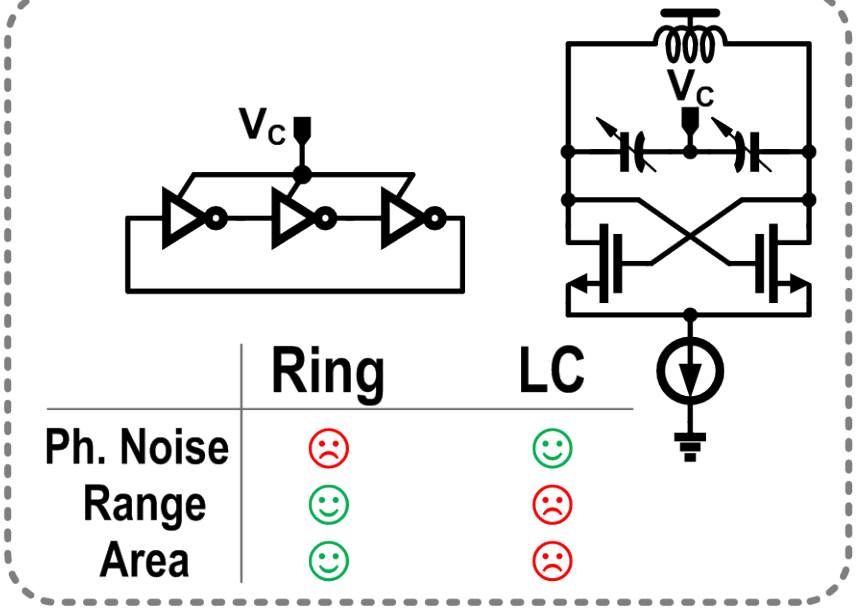
# Trade-off between Jitter and Area




$$FoM_{OSC} = -\mathcal{L}\{\Delta\omega\} + 20\log[\omega_o/\Delta\omega] - 10\log[P_{mW}]$$

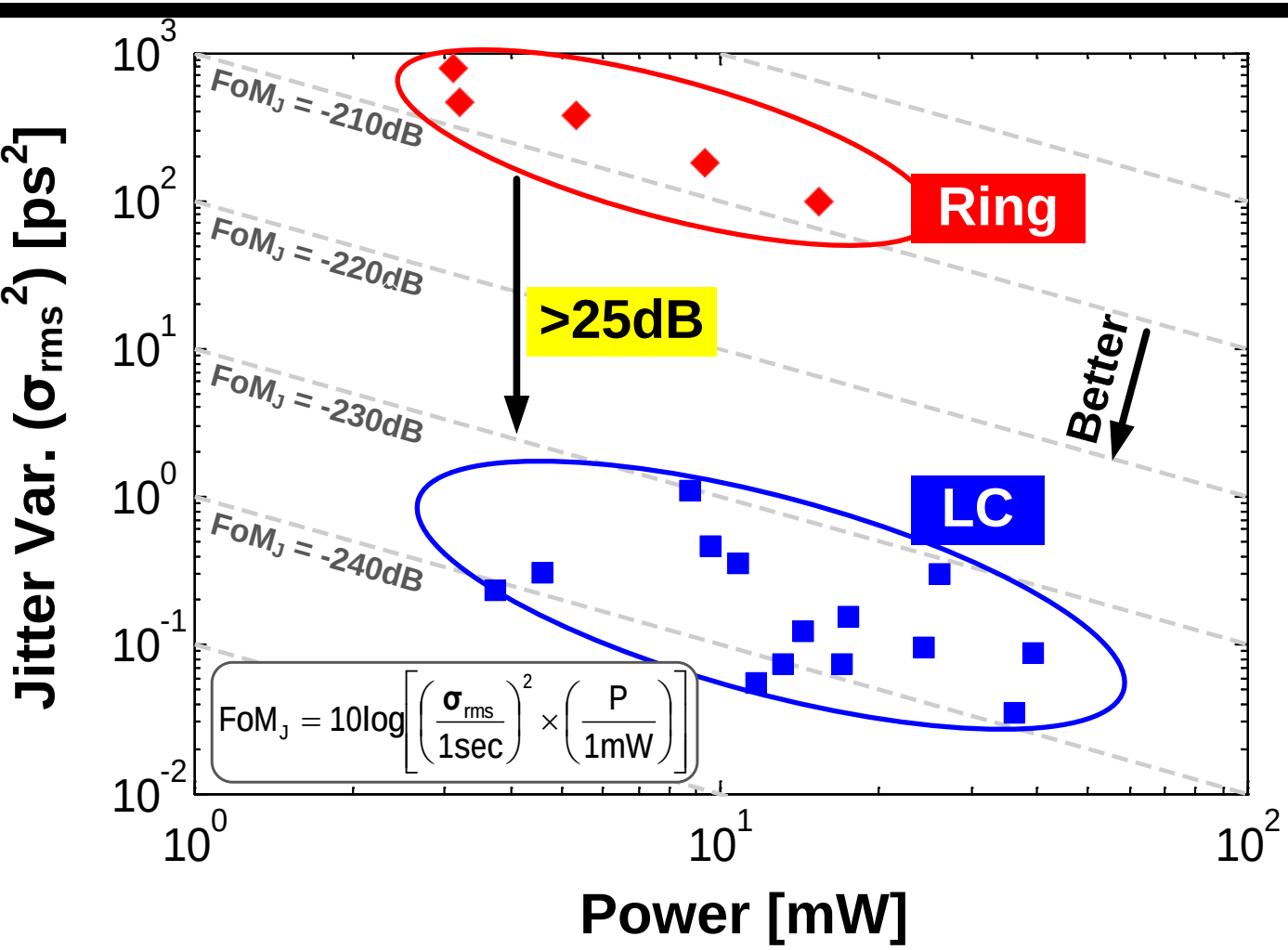



[Wu, ISSCC'15]



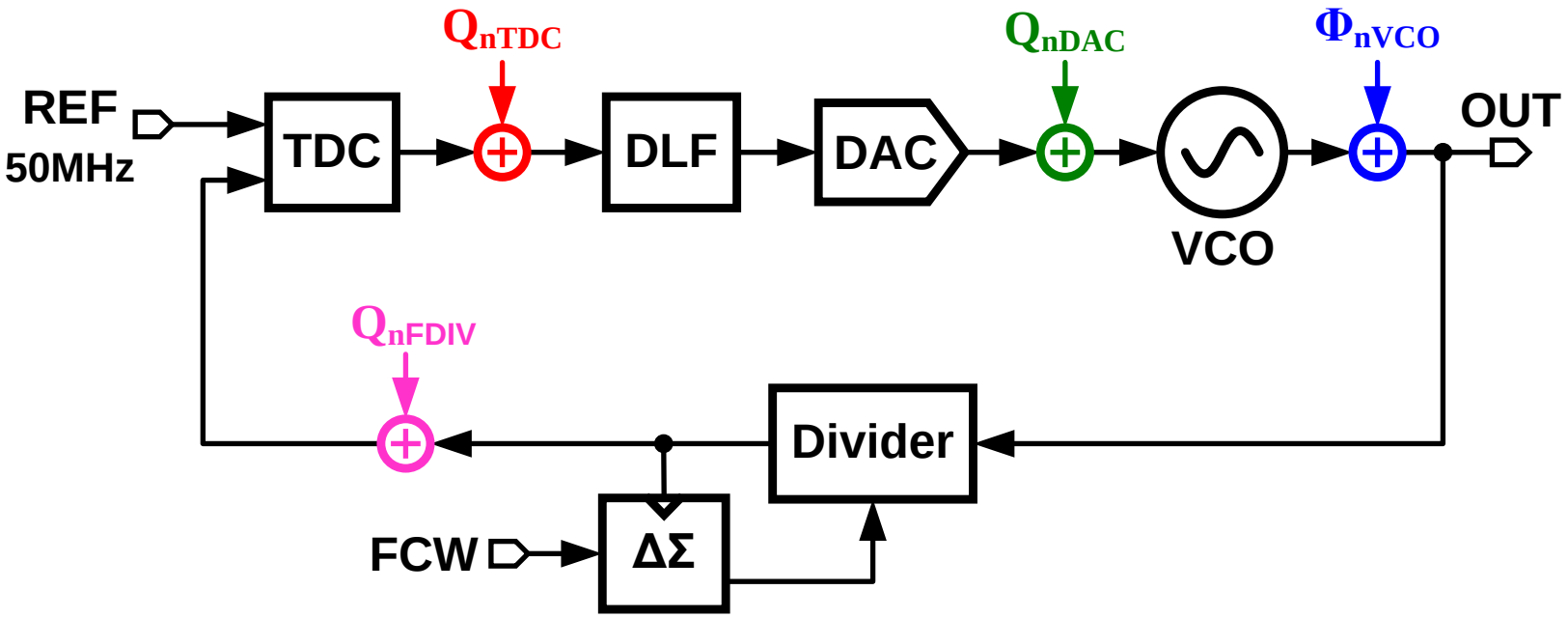

| | Ring | LC |
|---|---|---|
| Ph. Noise | ☹ | ☺ |
| Range | ☺ | ☹ |
| Area | ☺ | ☹ |

# Fractional-N DPLLs FoM



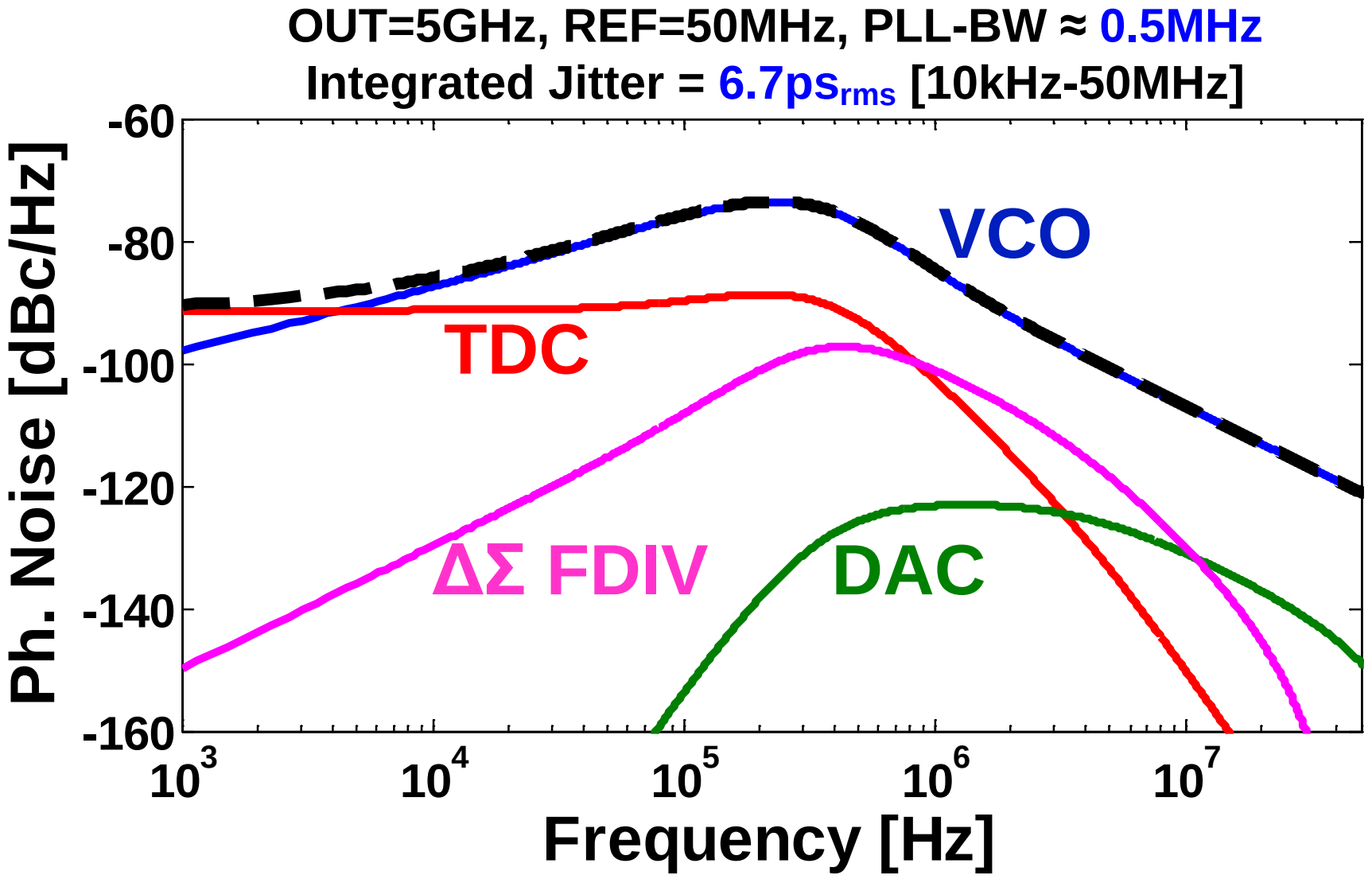

- **Performance gap bet. Ring- and LC-based FN-DPLLs**

# DPLL Phase Noise

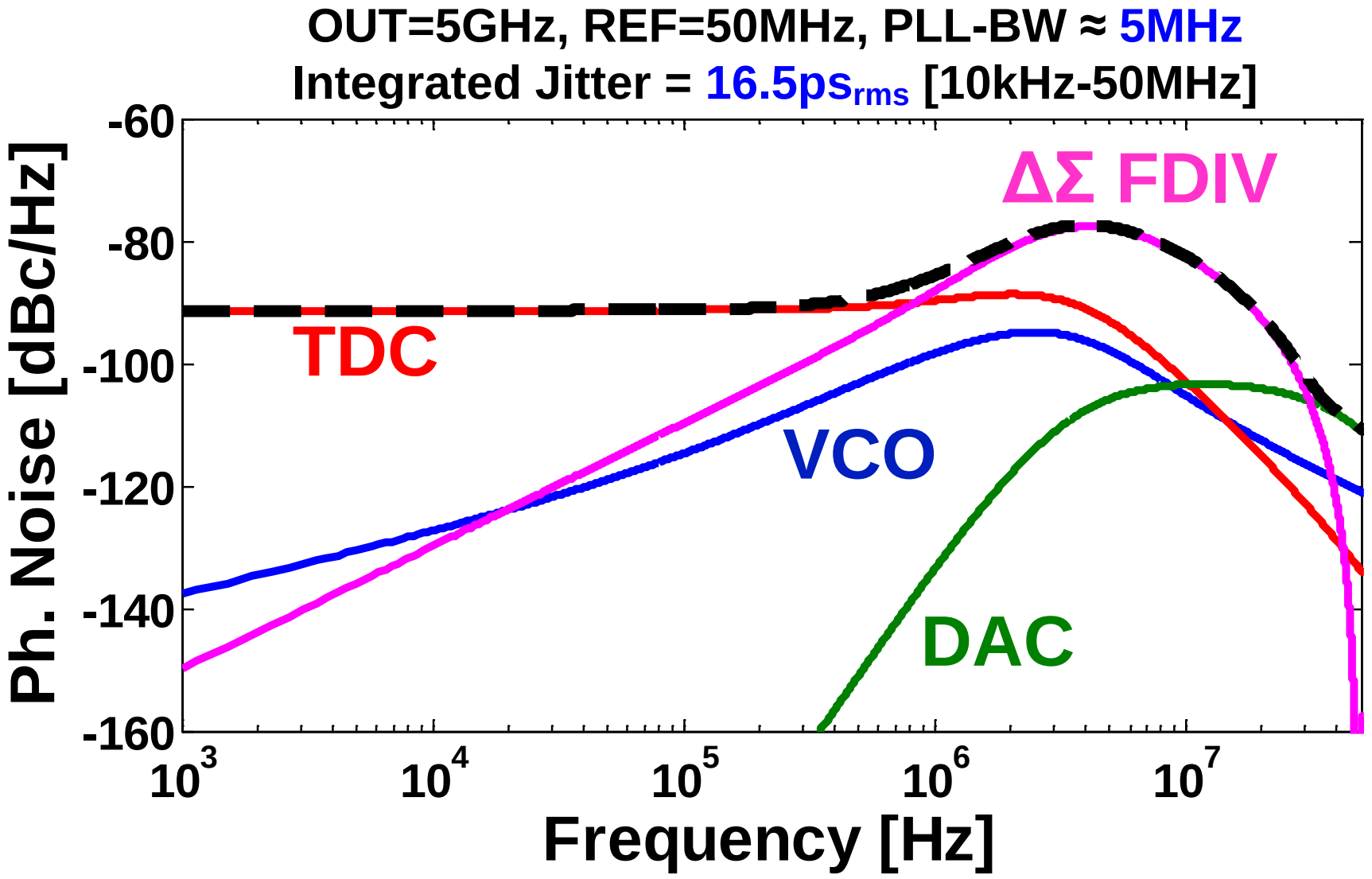



- **Wide BW ⇨ suppress VCO phase noise**
- **Narrow BW ⇨ suppress ΔΣ FDIV, TDC, DAC Q. noise**

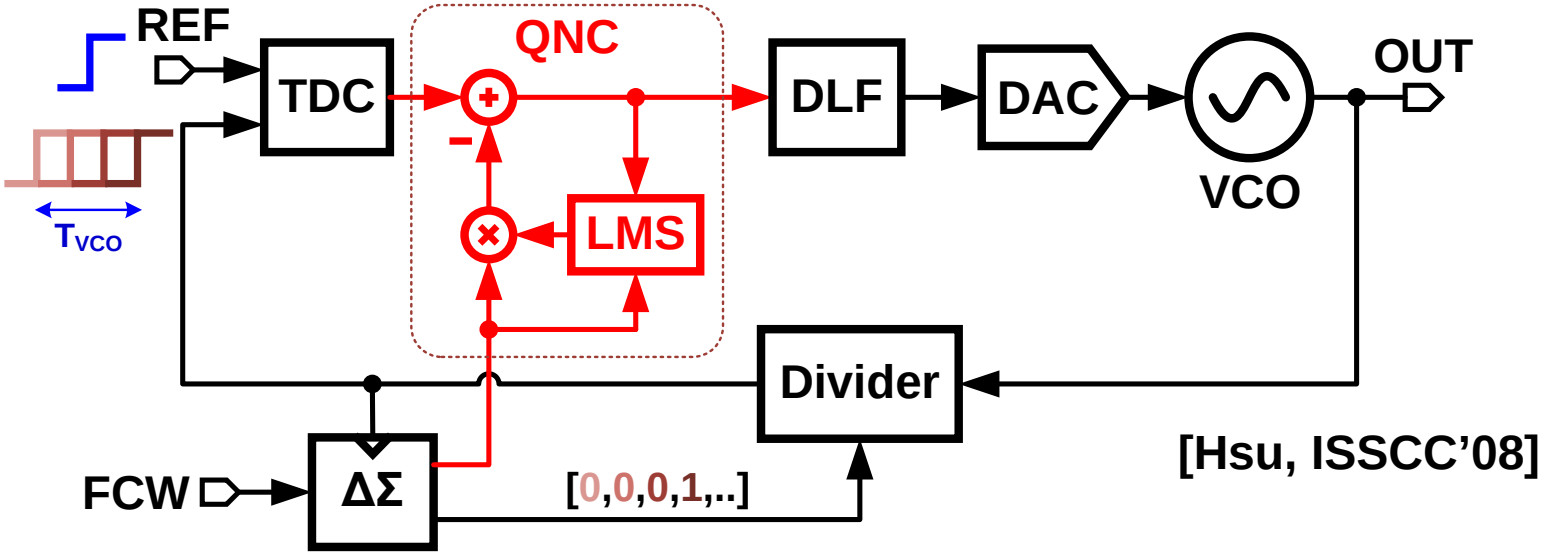
# Fractional-N DPLL with Narrow BW



# Fractional-N DPLL with Wide BW

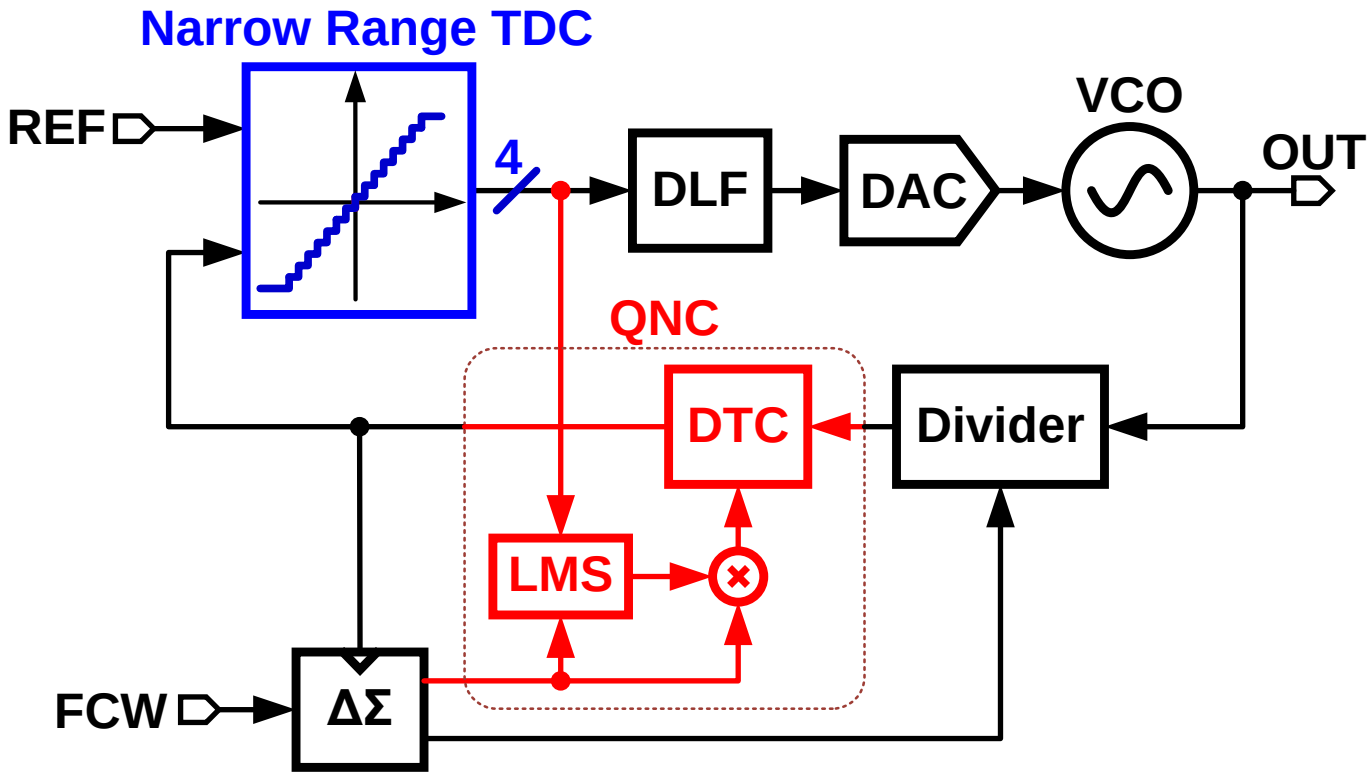


# TDC-based ΔΣ QNC




- Quantization noise cancellation (QNC) at TDC output
- Wide measurement range > $T_{VCO}$
  - Compromises linearity (INL) → large jitter and frac. spurs
- Fine resolution (<3ps) for low in-band noise
- Wide range, high res. and linear TDC → high power

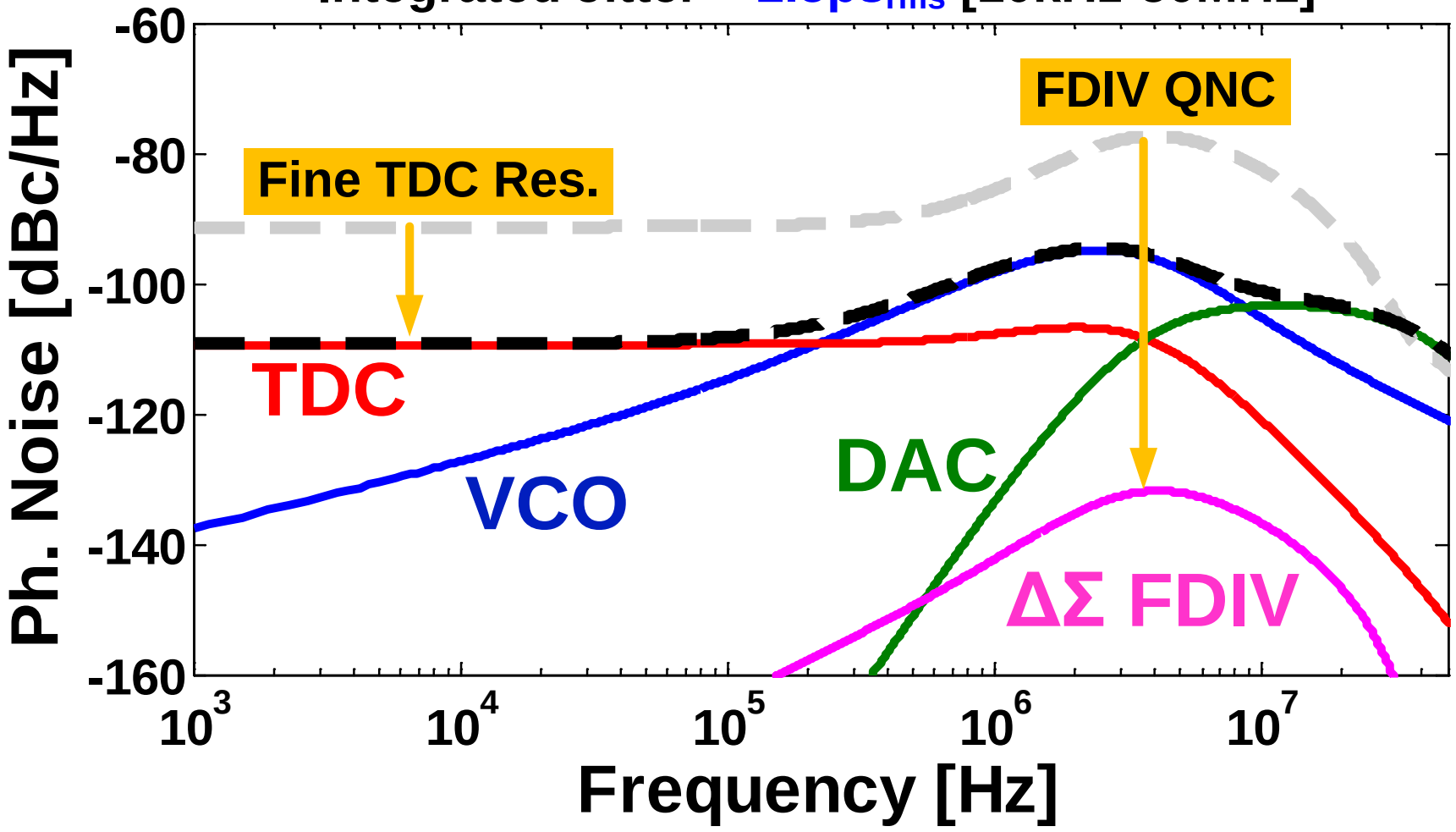
# Proposed DTC-based ΔΣ QNC



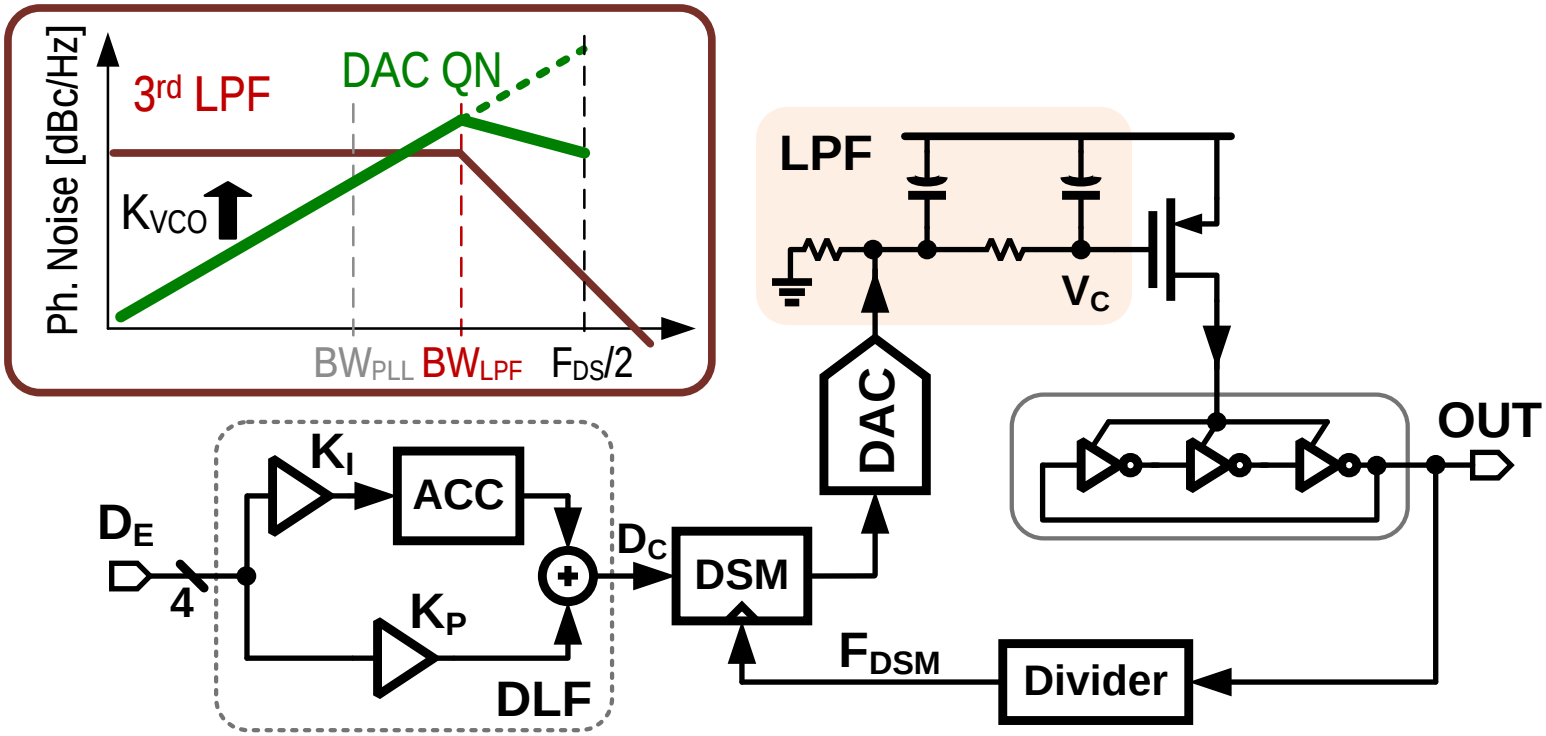

- QNC performed in time domain using a DTC
- TDC range requirement is alleviated
  - Low power, high resolution, narrow range TDC

# Wide PLL BW with ΔΣ QNC

OUT=5GHz, REF=50MHz, PLL-BW ≈ 5MHz
Integrated Jitter = 2.5ps$_{rms}$ [10kHz-50MHz]

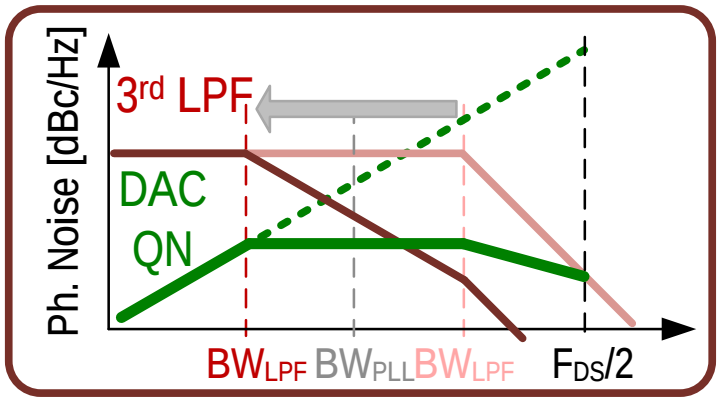


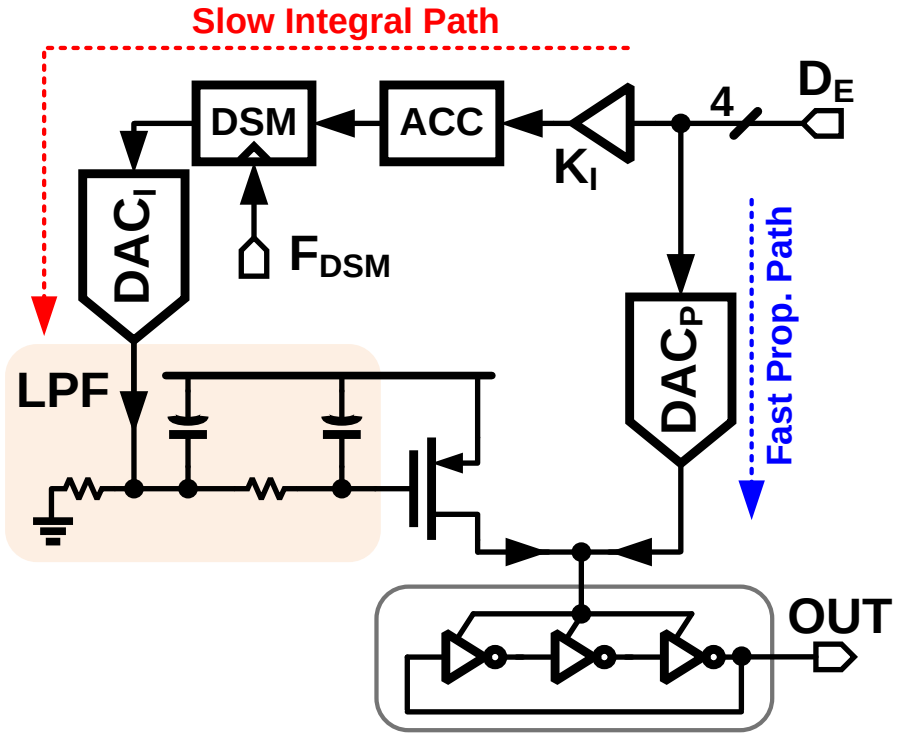
# DAC Quantization Noise Trade-off




- **Ring VCO: large frequency drift across temp.**
  - **Large $K_{VCO}$ → Higher DAC quantization noise**
- **DAC Noise filtering is limited by the wide PLL BW**

# Proposed Dual-Path Control

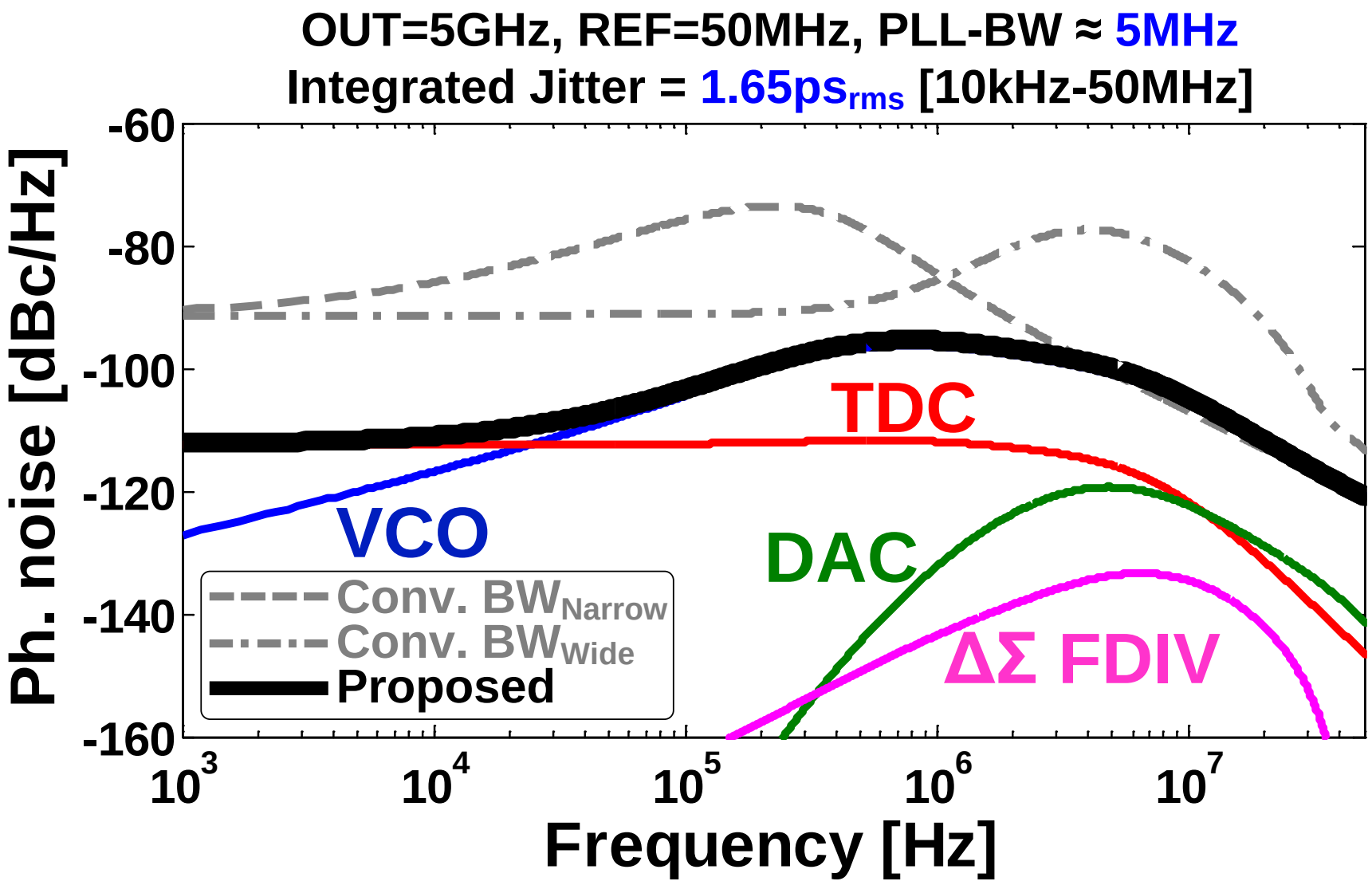


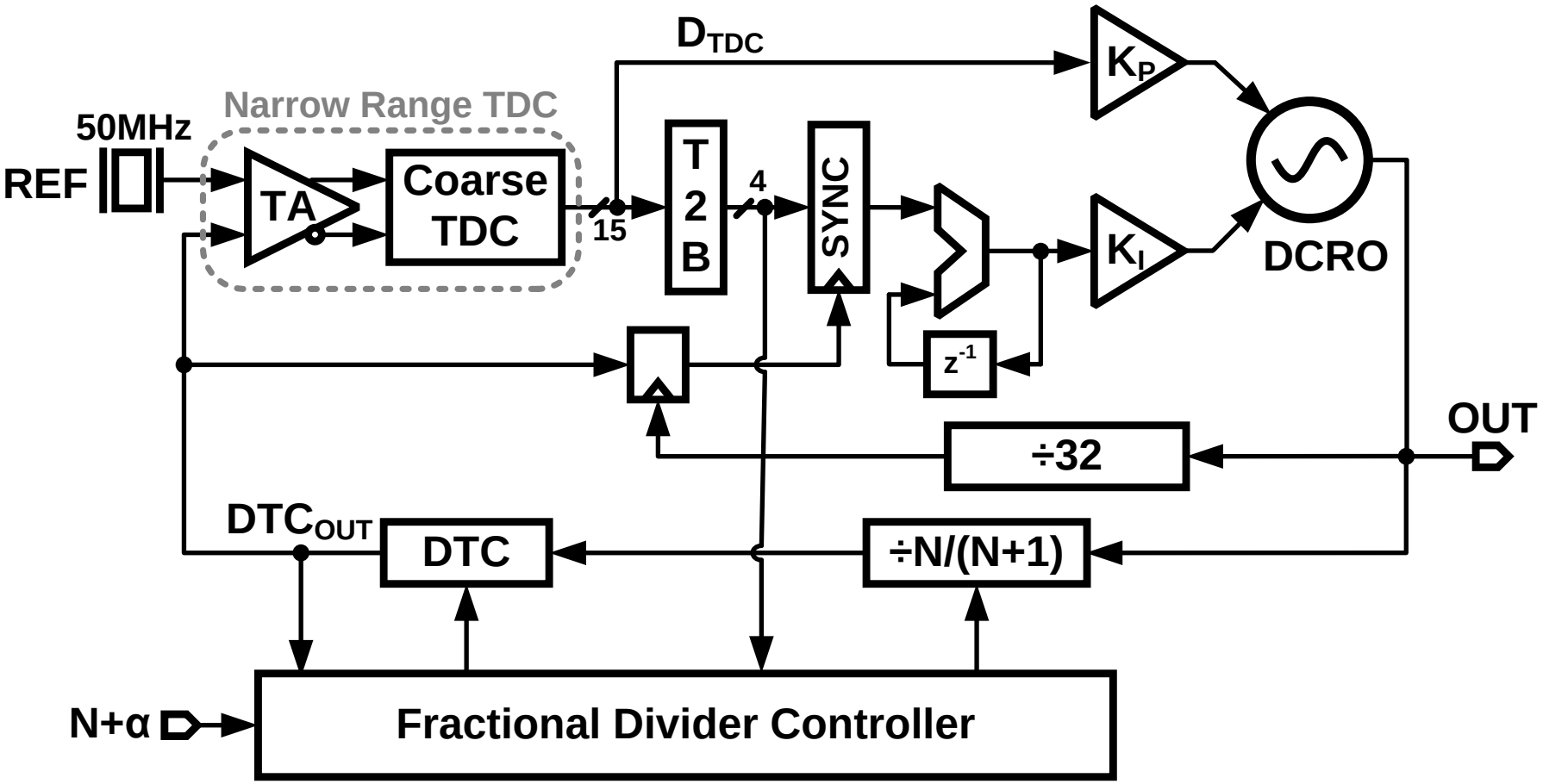

**Filtered DAC noise + Wide PLL BW**

- Decouple DAC filtering BW from loop BW
- Relax ΔΣ oversampling requirement → Low power
- Minimize loop latency → Limit jitter peaking

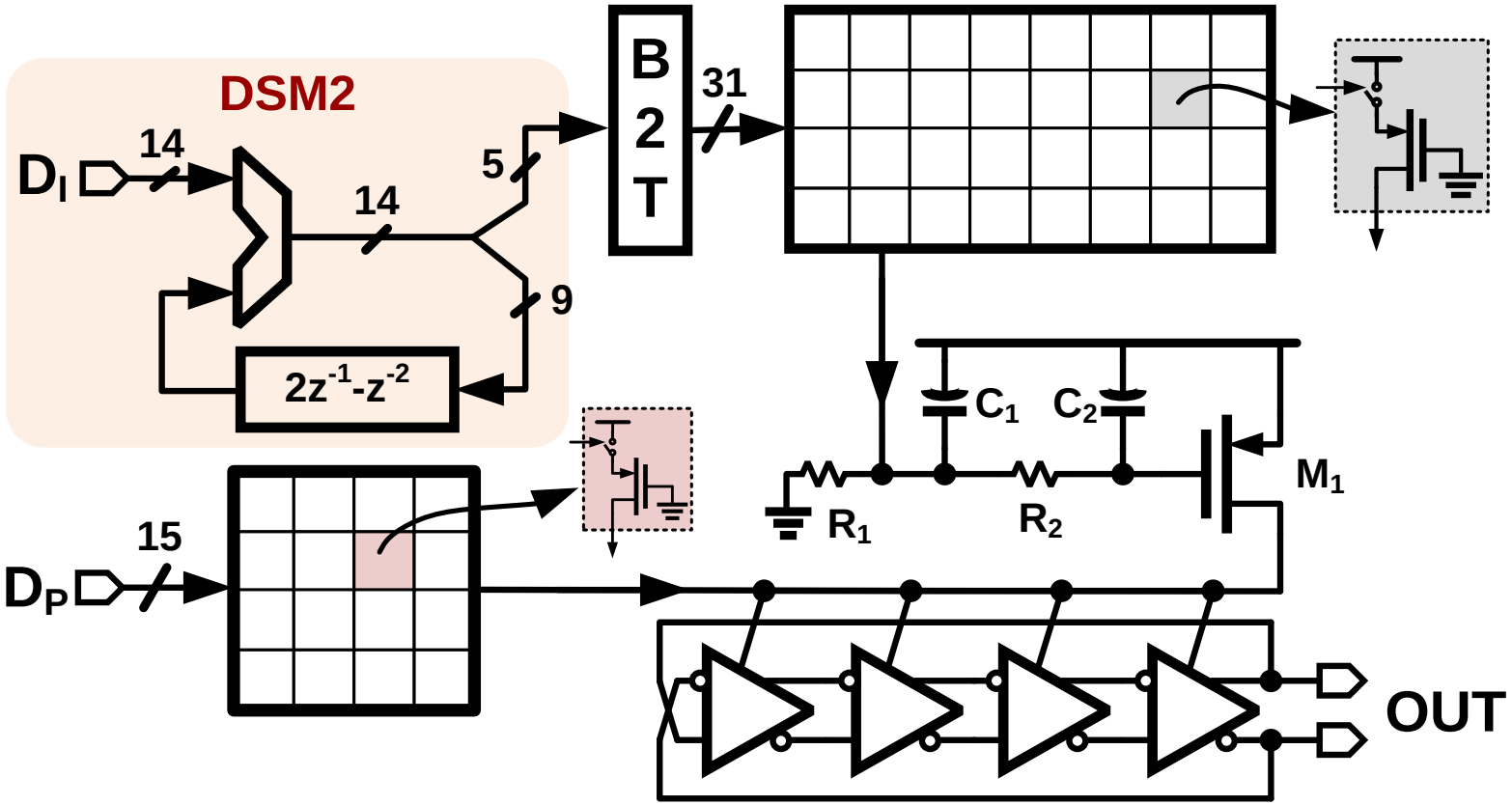
# Proposed DPLL Phase Noise



# Complete DPLL Architecture

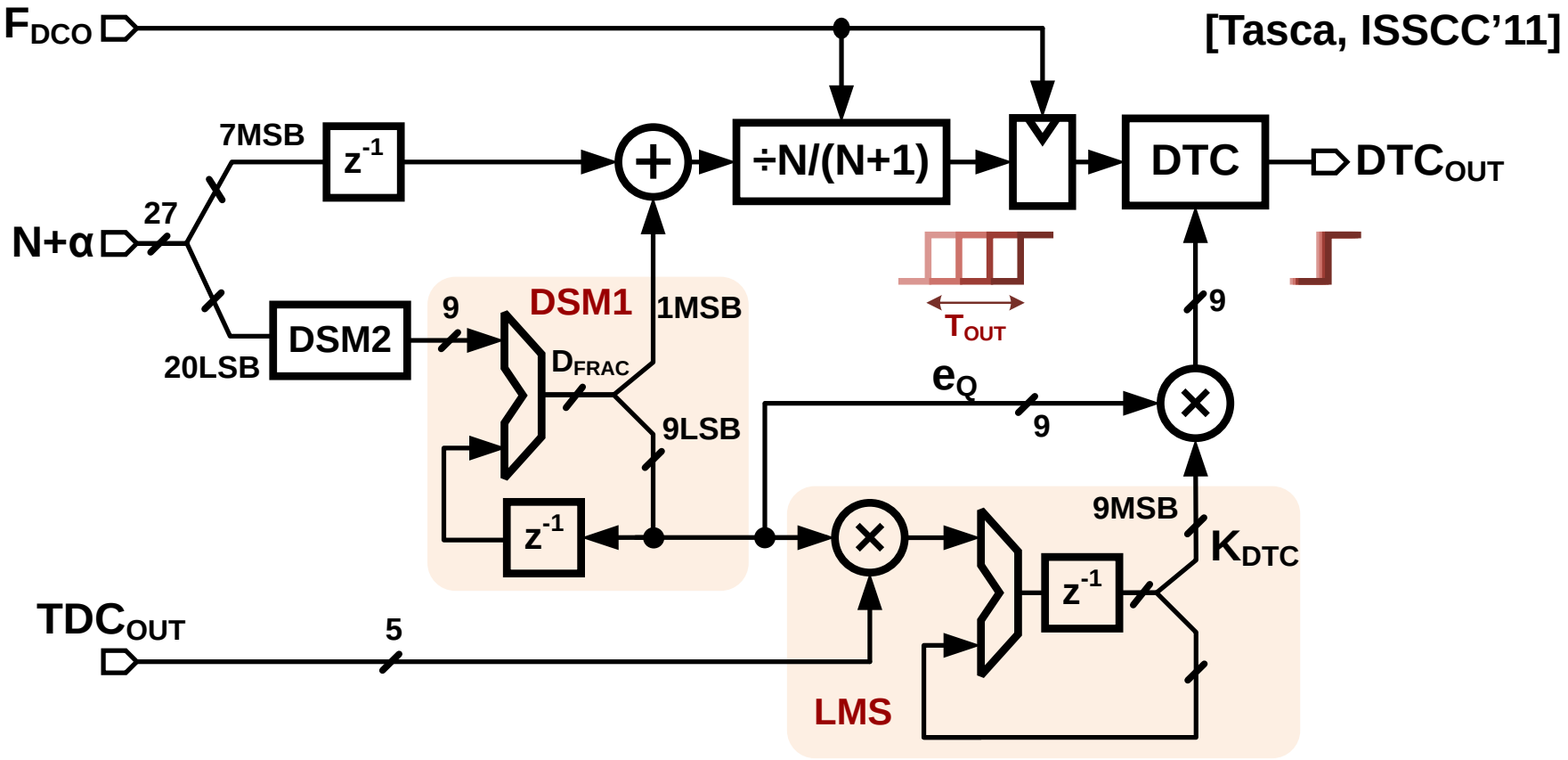


# Digitally Controlled Ring Oscillator




- **Second order ΔΣ + 5-bit current DAC → Integral control**
- **3rd RC filter suppresses shaped quantization noise**
- **Tuning range : 2-6GHz**

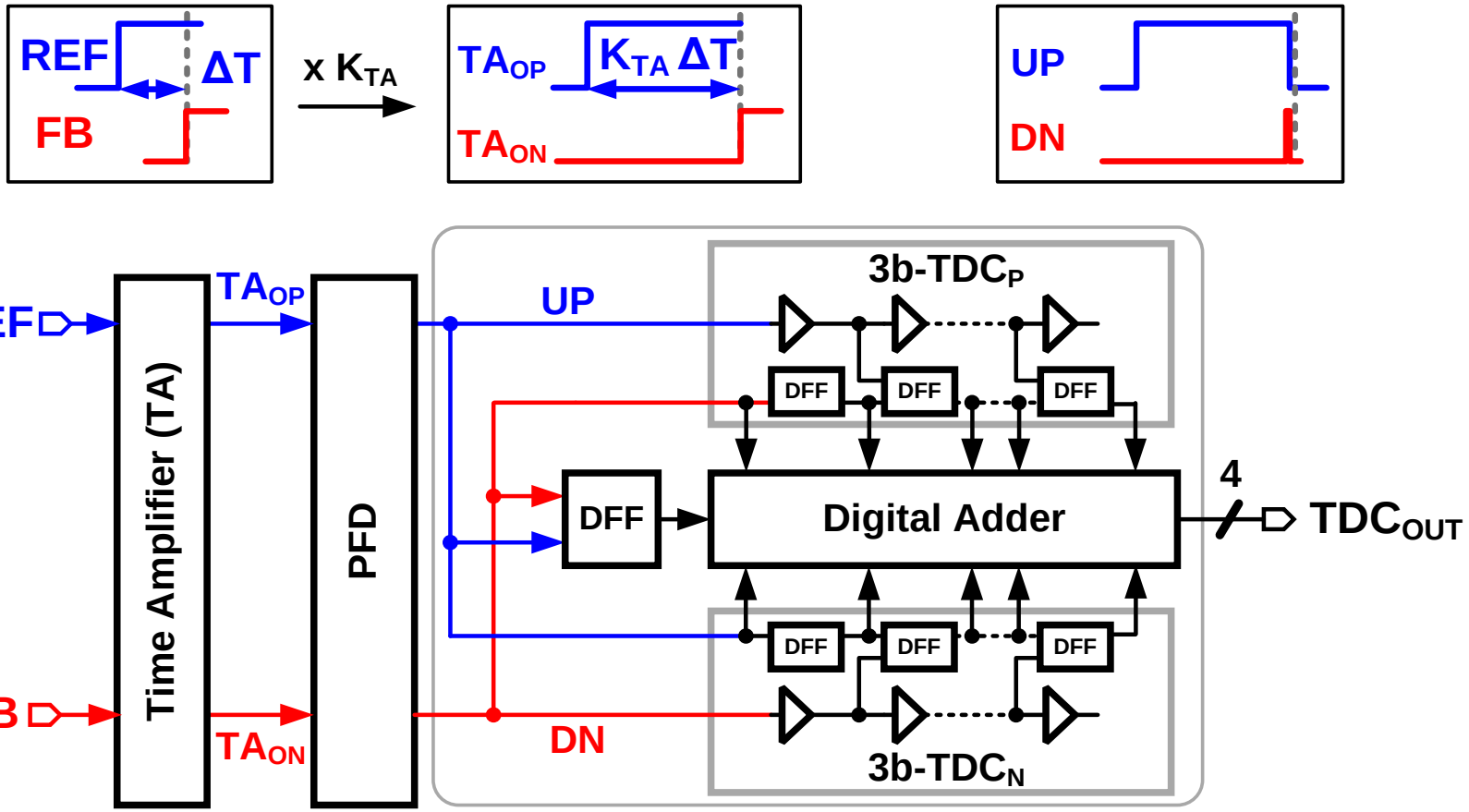
# Fractional Divider




- 27b frequency control word (7b integer + 20b frac.)
- 6-stage multi-modulus divider (MMD) + 9-bits DTC

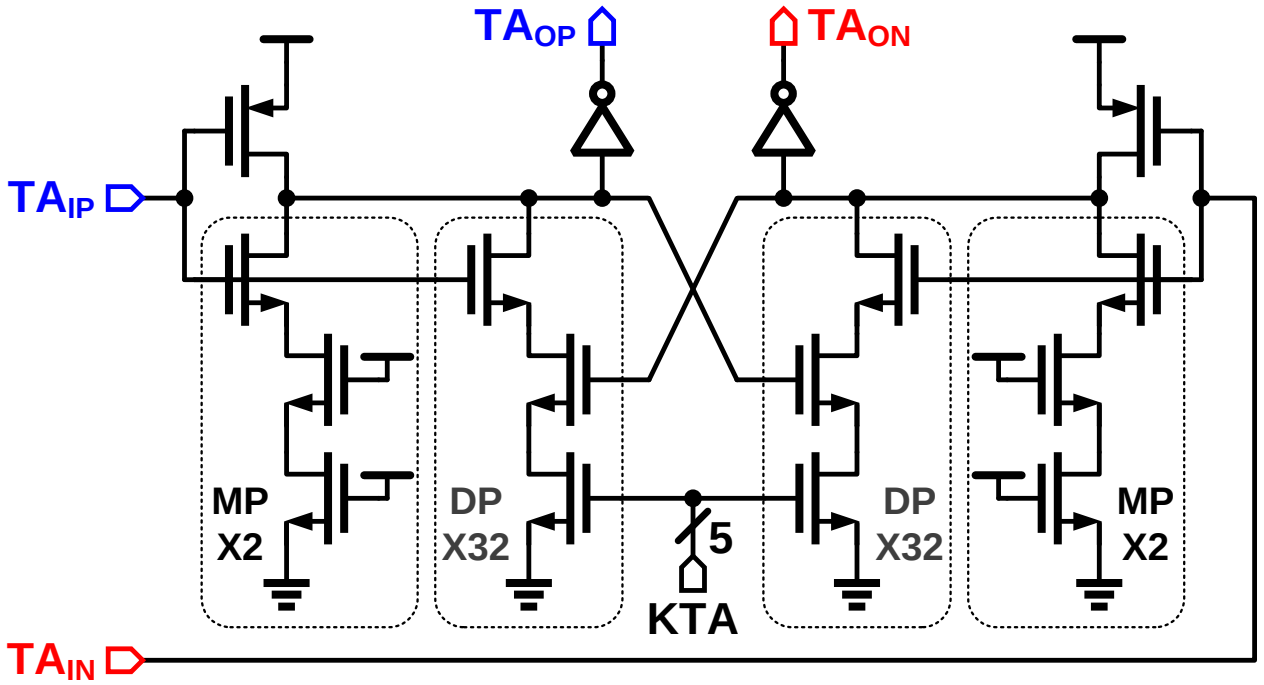
# Narrow Range TA-TDC

[Elkholy, VLSI'14]




- **High gain time amplifier (TA) + Low complexity TDC**

# Time Amplifier (TA)




- High TA gain → Programmable by controlling ratio of main : dependent path from 1-16X
- After QNC in the feedback path, the TA input range is limited to random jitter → Relaxed linearity

# *Outline*

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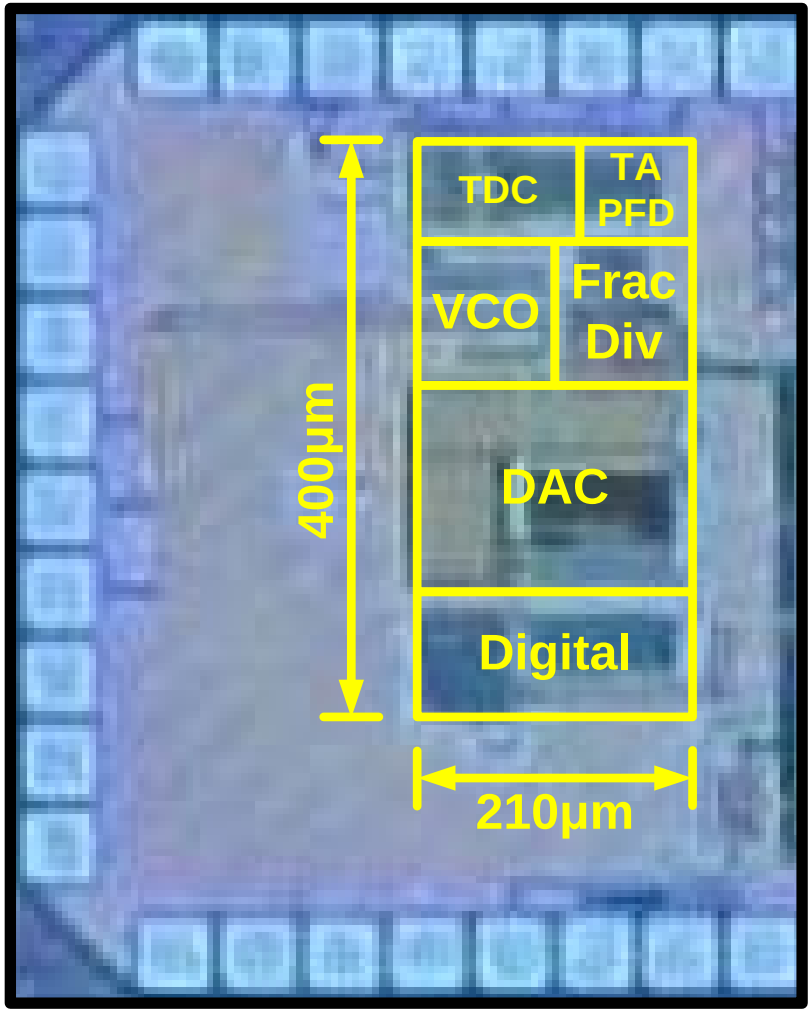
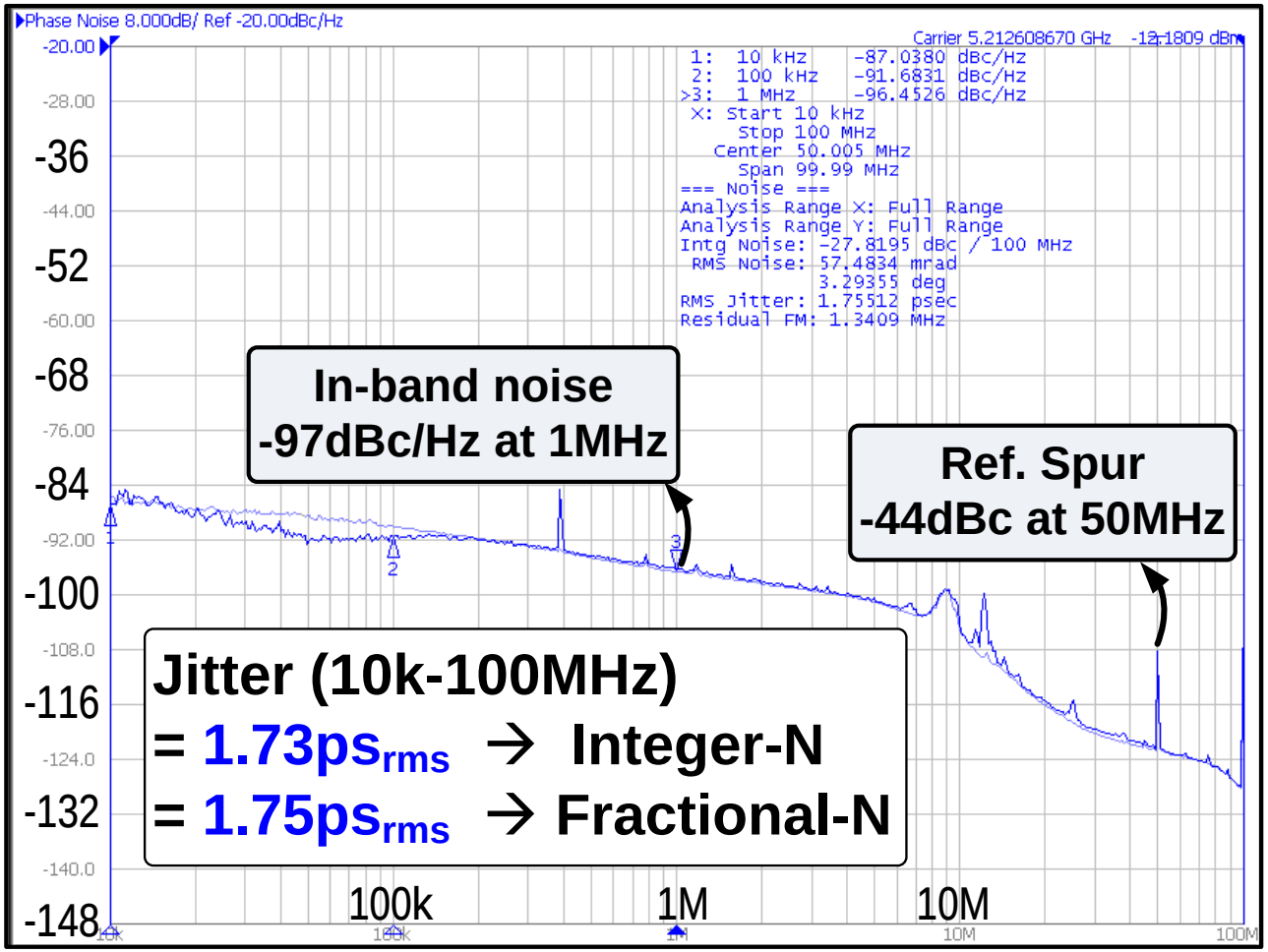
# *Die Photograph*

- 65nm CMOS
- Active area: 0.084mm$^2$
- Power: 4mW
- Supply voltage: 0.9V
- OUT freq: 4-5.5GHz
- REF freq: 50MHz

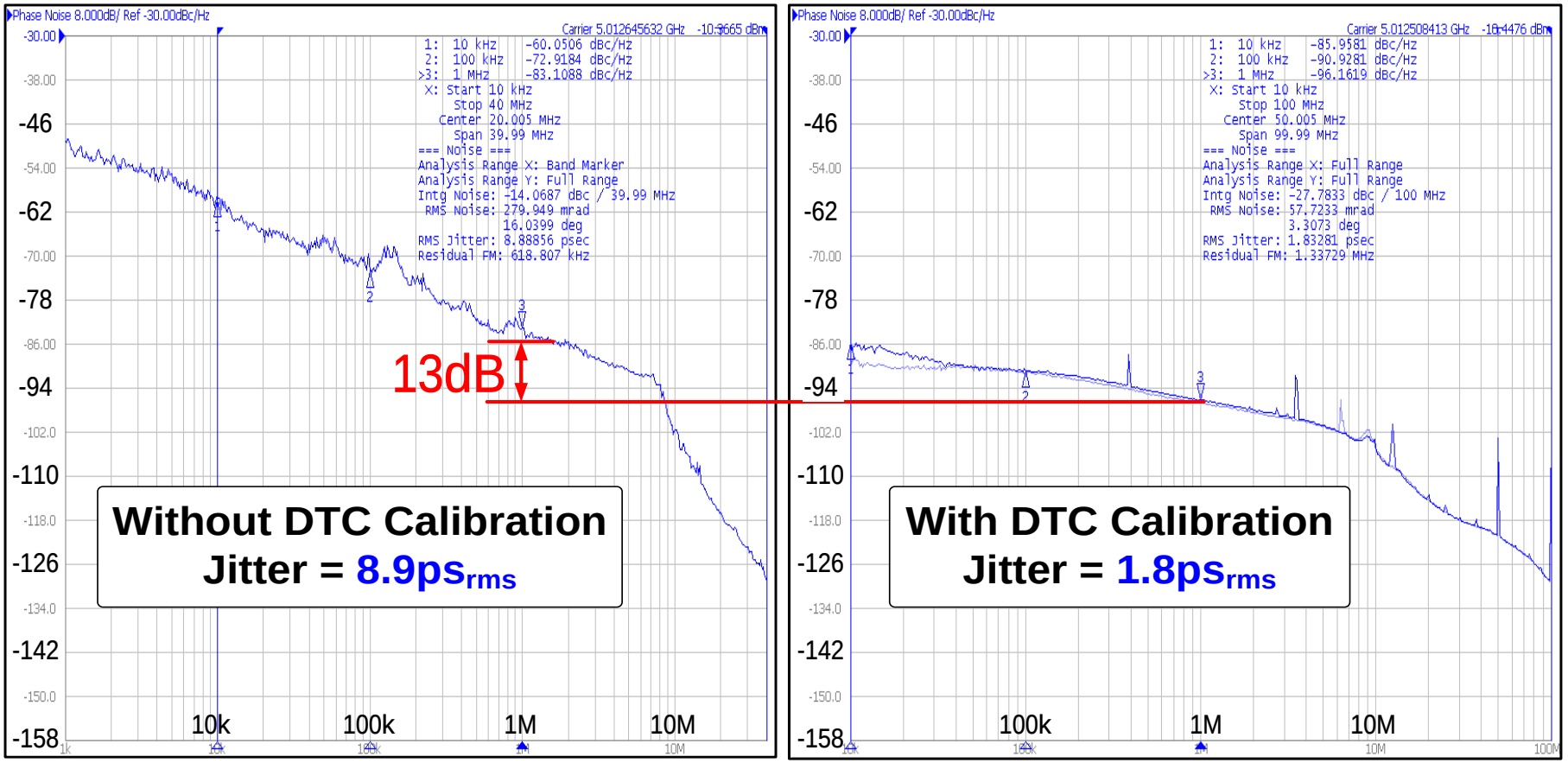


# Phase Noise at 5.2GHz



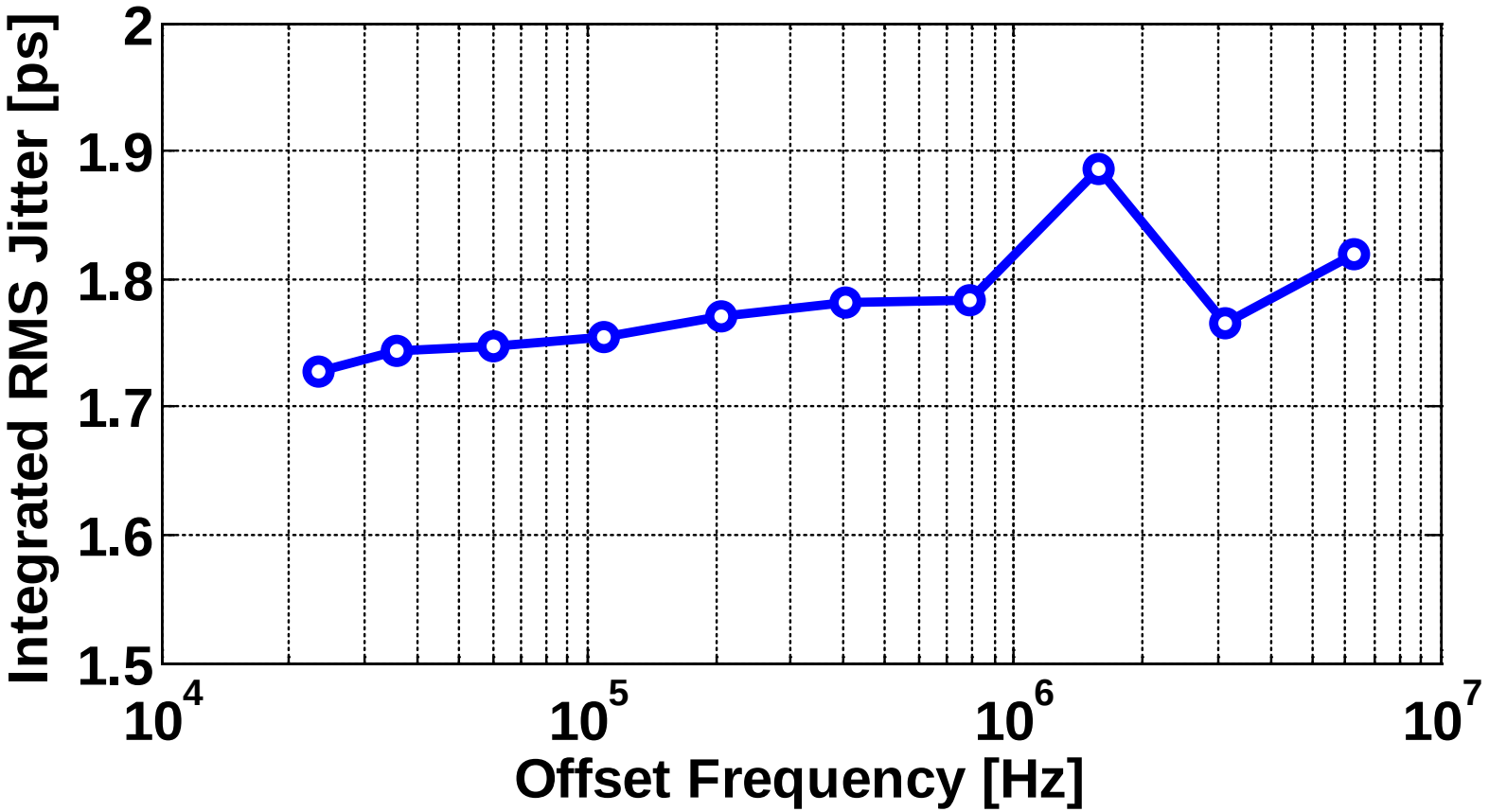

- **Wide BW~ 5MHz, low in-band noise ~ -97dBc/Hz**

# Phase Noise w/wo DTC Calibration



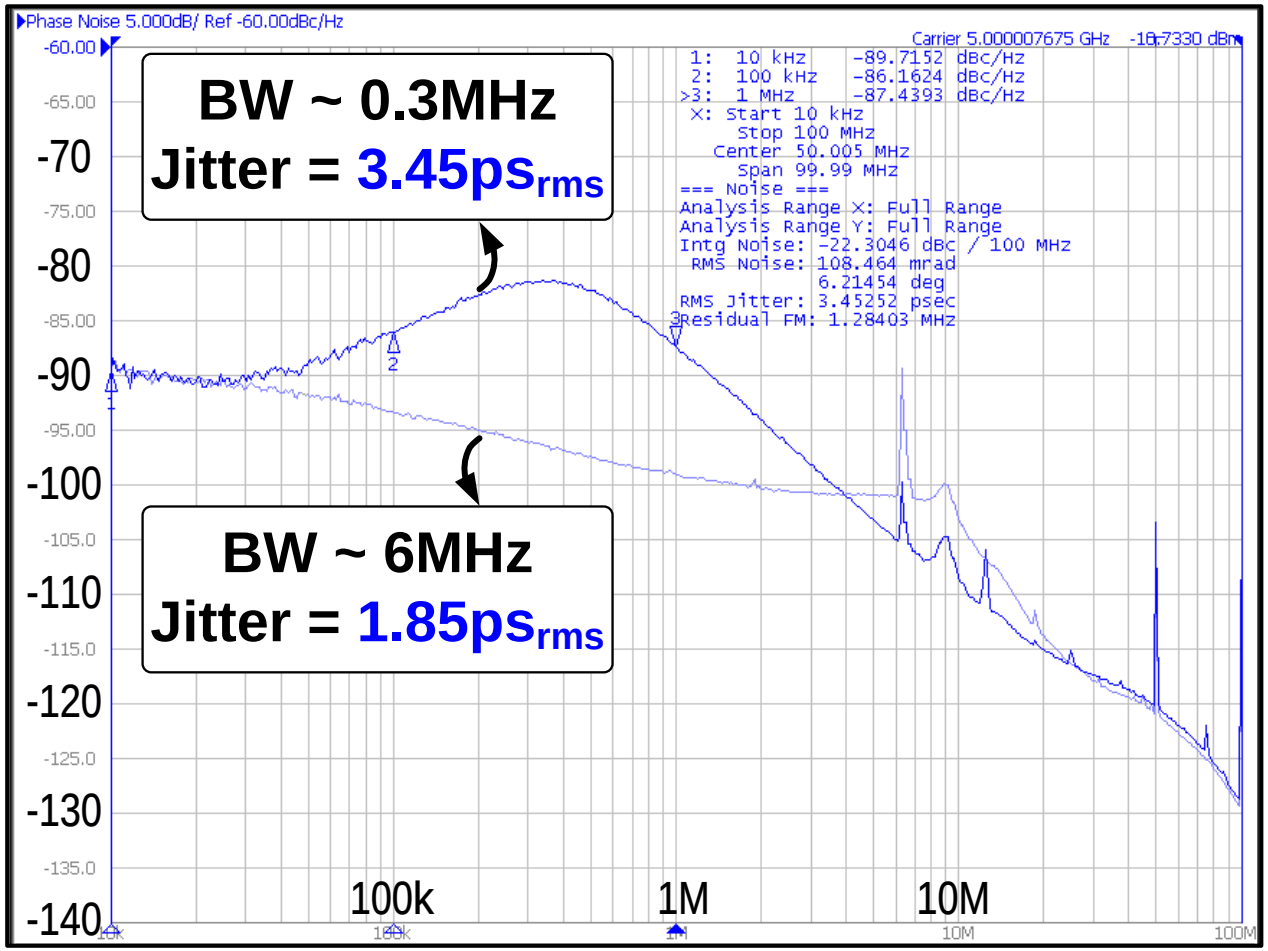

- **Without DTC calibration**
  - **ΔΣ QN is not completely cancelled and saturates TDC**

# Jitter Vs Fractional Output Frequency



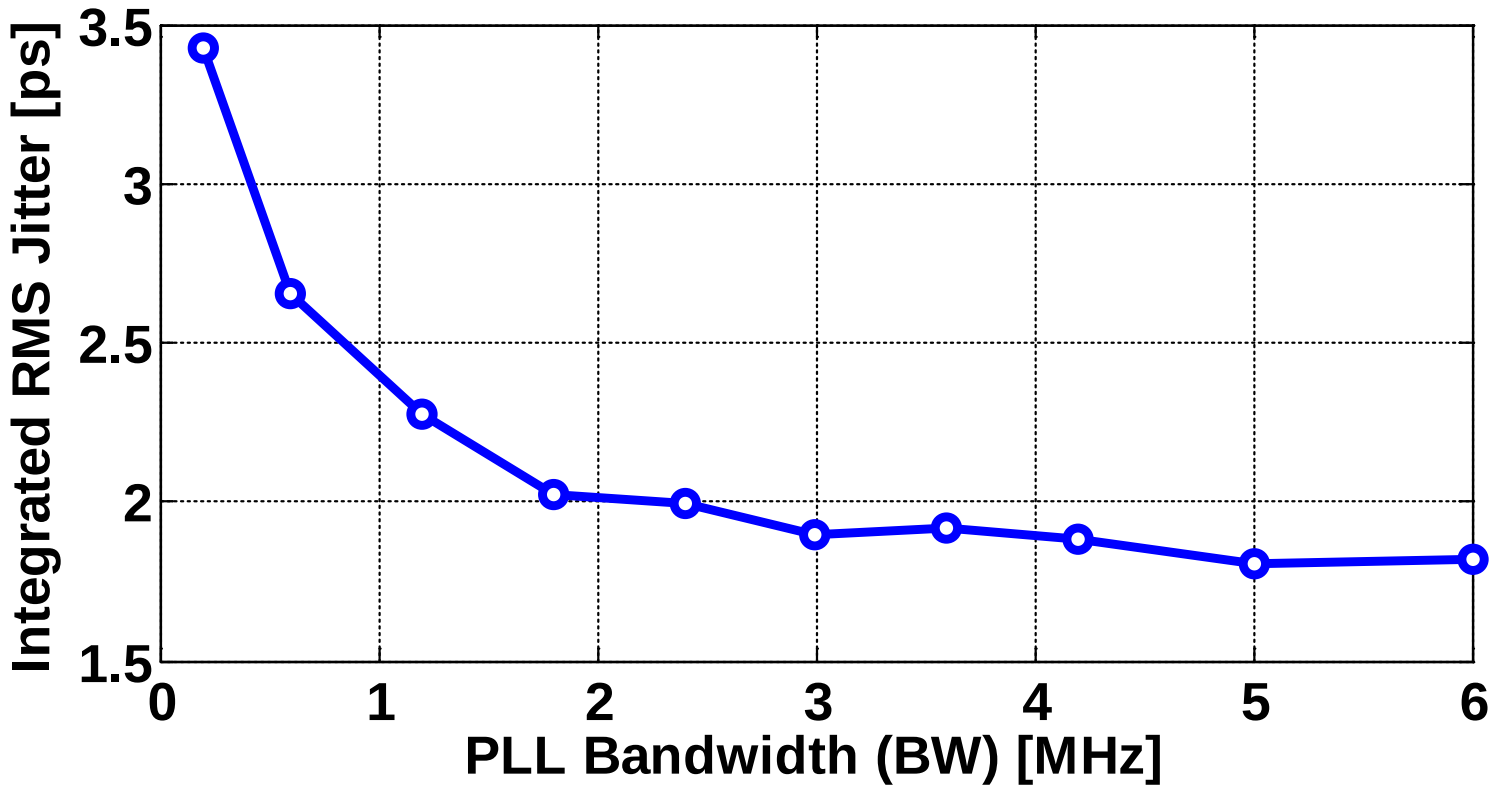

- **Excellent jitter performance (<1.9ps$_{rms}$) is achieved across fractional output frequency**

# PLL BW Impact on Phase Noise




- **Wide BW (~6MHz ≈ $F_{REF}$/8) with no limit cycle**

# *Phase Noise for Different BW at 5.2GHz*




- **Excellent jitter across different BWs (3 to 6MHz)**

# Performance Summary

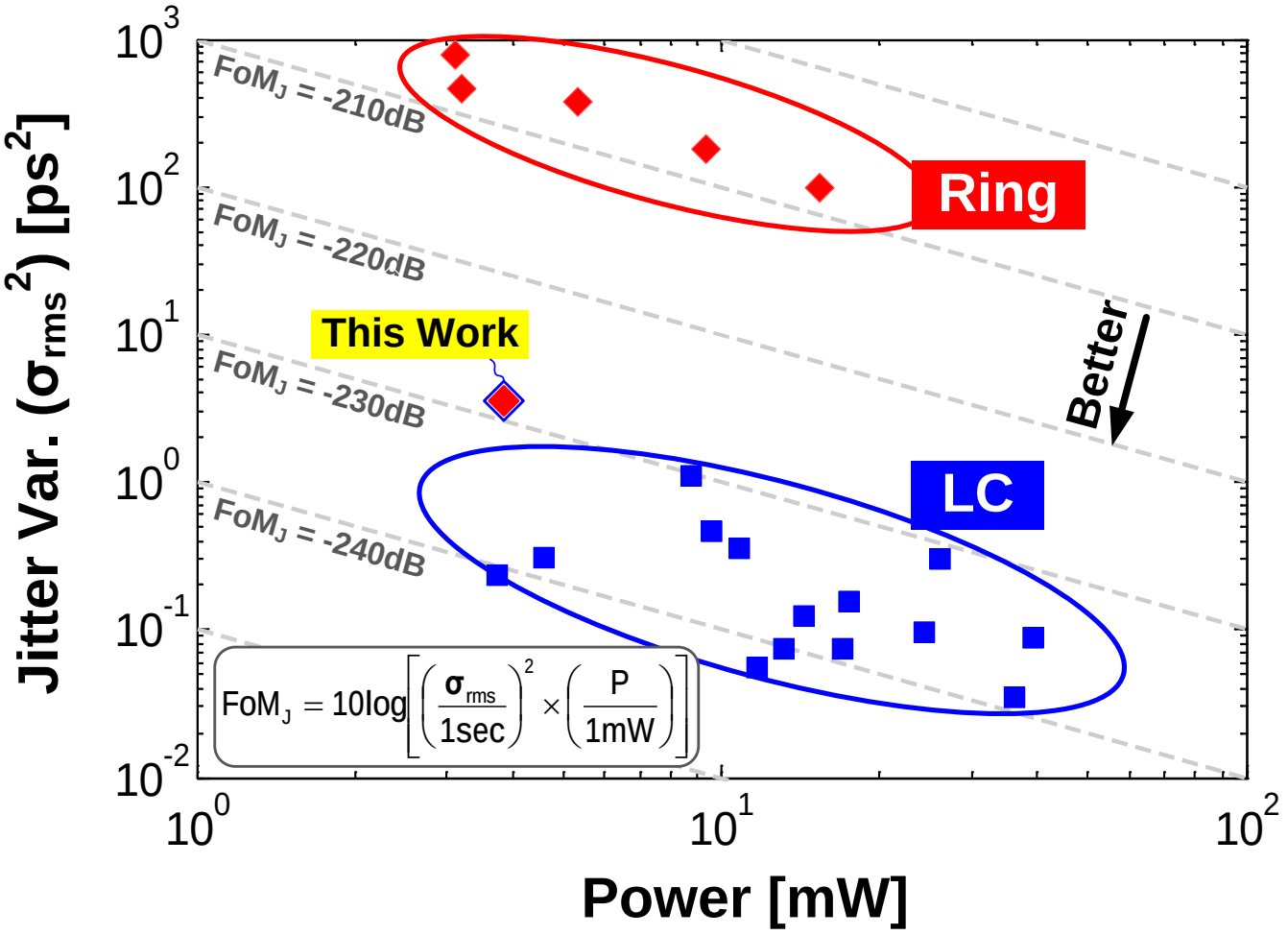
| | M. Chen ISSCC'10 | Grollitsch ISSCC'10 | Y-W. Li ISSCC'12 | T-K. Jang ISSCC'13 | J. Liu ISSCC'14 | This Work |
|---|---|---|---|---|---|---|
| Technology [nm] | 65 | 65 | 22 | 28 | 20 | 65 |
| Supply [V] | 1.1-1.3 | 1.1/1.3 | 1 | 1 | 0.9 | 0.9 |
| Output Freq. [GHz] | 0.6-0.8 | 0.3-3.0 | 0.6-3.6 | 0.032-2.0 | 0.8-1.6 | 4.0-5.5 |
| Ref. Freq. [MHz] | 26 | 25 | 25-200 | 30 | 25 | 50 |
| Power [mW] | 3.2 | 9.3 | 15.4 | 5.3 | 3.1 | 4 |
| BW [MHz] | ~1 | ~0.7 | 0.003-4 | ~4 | ~4 | ~5 |
| In-band PN [dBc/Hz]* | -72.1 | -74.6 | -63.6 | -75.7 | -74.1 | -97 |
| RMS Jitter [ps] | 21.5 [1k-100MHz] | 13.5 [1k-20MHz] | 10 [N/A] | 19.3 [20k-40MHz] | 28 [20k-40MHz] | 1.9 [10k-100MHz] |
| $FoM_J$ [dB] | -208.3 | -207.7 | -208 | -207 | -206.1 | -228.5 |
| Power Eff. [mW/GHz] | 4 | 3.1 | 4.3 | 2.65 | 1.94 | 0.8 |
| Area [$mm^2$] | 0.027 | 0.038 | 0.03 | 0.026 | 0.012 | 0.084 |

* Normalized to 5GHz

$$FoM_J = 10\log\left[\left(\frac{\sigma_{rms}}{1sec}\right)^2 \times \left(\frac{P}{1mW}\right)\right]$$

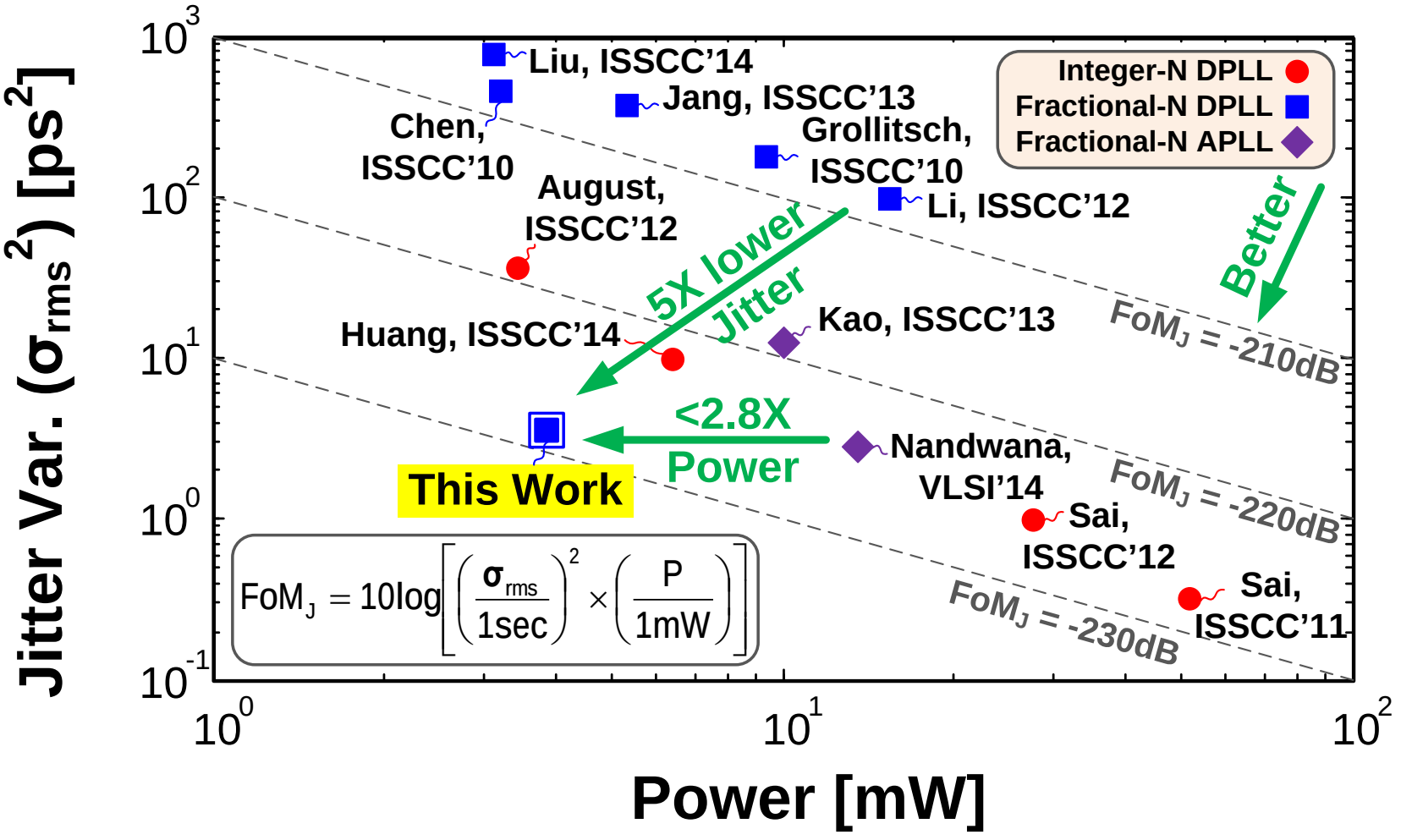
**[Gao, TCAS-II, 2009]**

# Jitter-Power FoM – DPLL




- **Reduce FoM gap between Ring- and LC-based DPLLs**

# Jitter-Power FoM – Ring VCO




- **Best FoM (>20dB better than state-of-the-art)**

# *Conclusions*

- **Low power, low jitter Ring-based fractional-N DPLL is demonstrated with:**
  - **Truly 9b fractional divider that alleviates TDC dynamic range requirements**
  - **Low power, high resolution 4b TDC**
  - **Dual-path loop filter architecture to suppress DAC noise**

- **Measured results indicate:**
  - **Excellent jitter-power FoM (-228.5dB) for Ring-based DPLLs**
  - **Low in-band phase noise (-97dBc/Hz at 5GHz output)**
  - **Wide PLL BW with no limit cycles (~$F_{REF}$/8)**

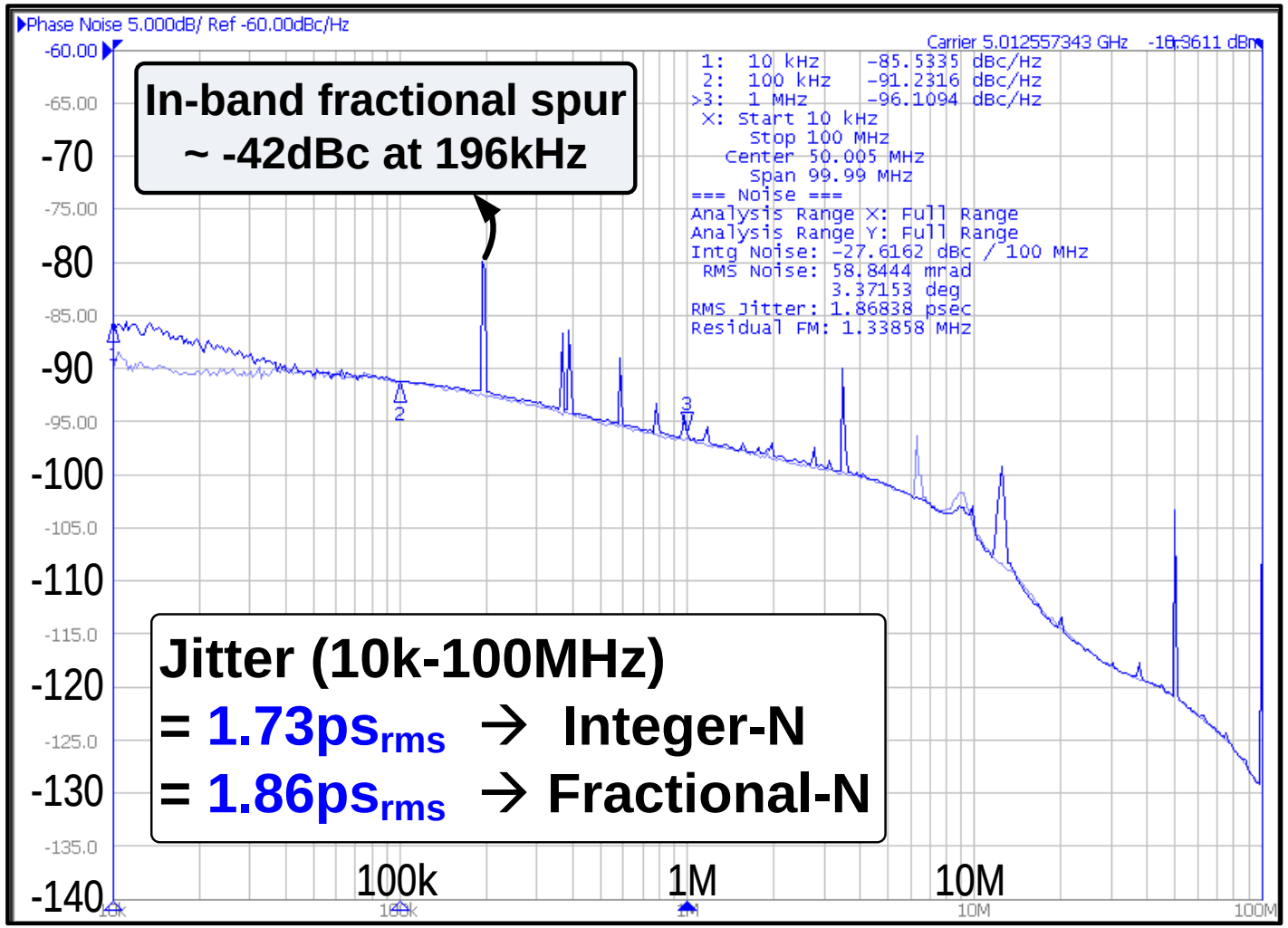
# *Acknowledgements*


- ***National Science Foundation*** **(NSF) under CAREER EECS-0954969**

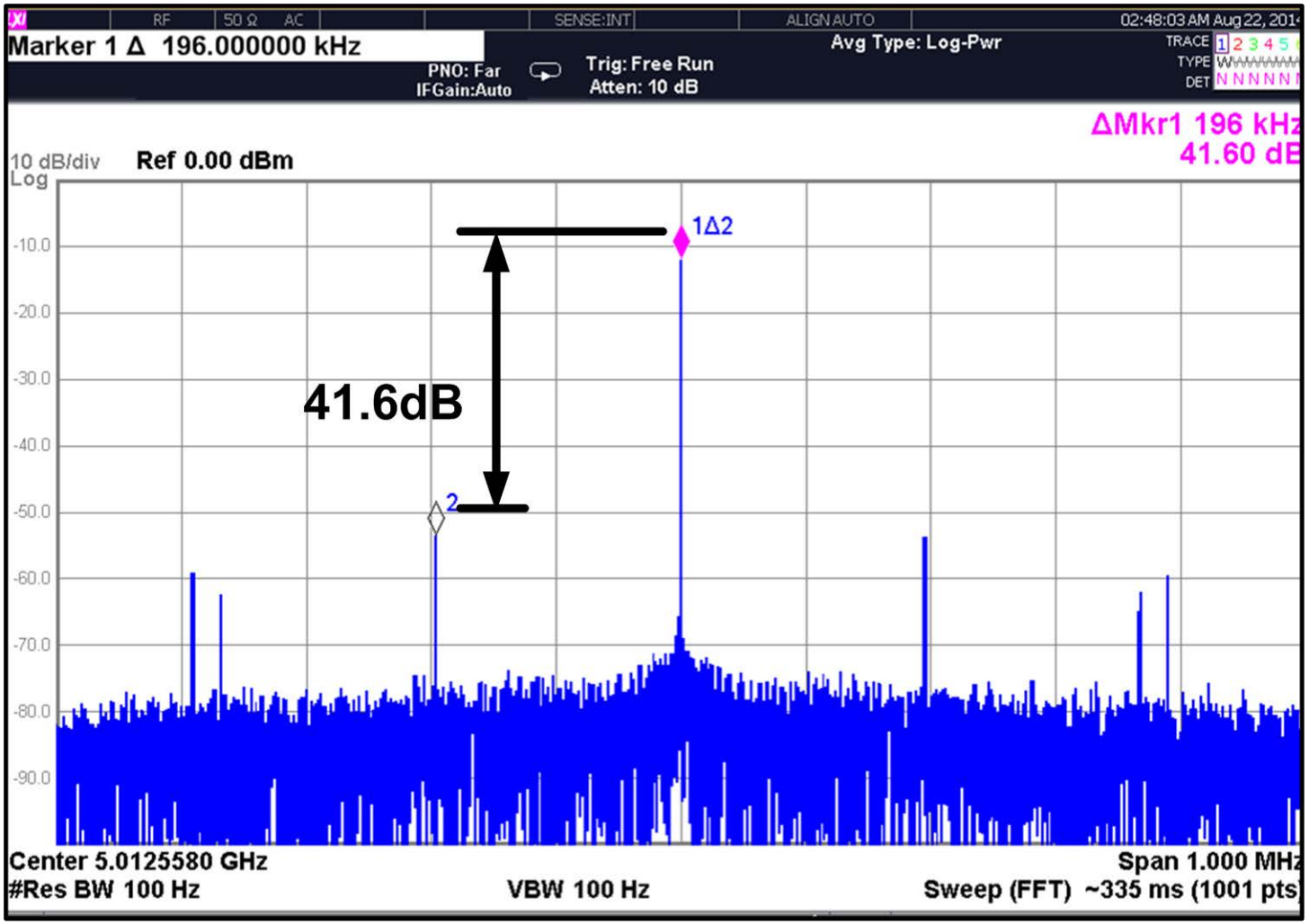
- **Berkeley Design Automation provided Analog Fast Spice (AFS) simulator**

# *Questions*

# Phase Noise w/ in-band Frac. Spurs



# In-band Fractional Spurs



# Reference Spur