Arria® 10 Device Architecture

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Arria® 10 Device Overview

- Device Goals and Overview
- Routing and Core Architecture
- Transceiver and I/O Architecture
- DSP and Floating Point
- Hard Processor System (HPS)
- Security
- Power
- Summary

Arria® 10 Device Goals

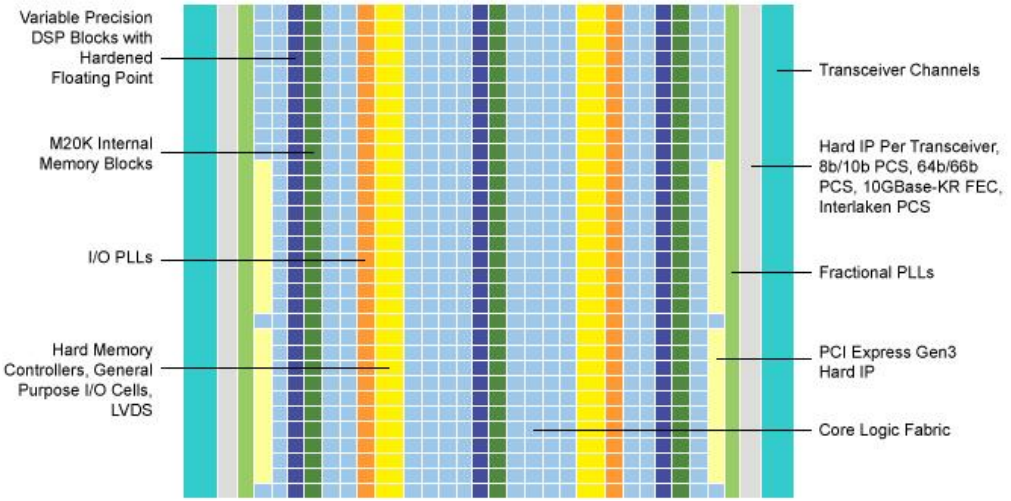
- A mid-range FPGA balancing power, performance and cost targeting key market applications

Wireless Infrastructure	Access, Metro & Core	Transmission	Cloud Servers and Storage	Broadcast
				
Target Applications				
• Remote Radio Head • Mobile Backhaul • Active Antenna • Basestation (BTS) • 4G/LTE Marco eNB • 4G/LTE Micro eNB	• 40G GPON, EPON, FFTH, Switch • 100G / 200G NGPON • 100G Traffic Management	• NX 100G OTU 4 • 2 X OTU 4 • 4 X OTU 4	• Flash Cache • Cloud • Server • Acceleration	• Pro A/V Equipment • Switcher • Server • Transport • Head End • VoD Mux

- Key Targets and Metrics:
  - 491 MHz fixed-point DSP datapath for Wireless Remote Radio Heads
  - Cloud server acceleration – hardened floating-point
  - Dramatic die-size reduction

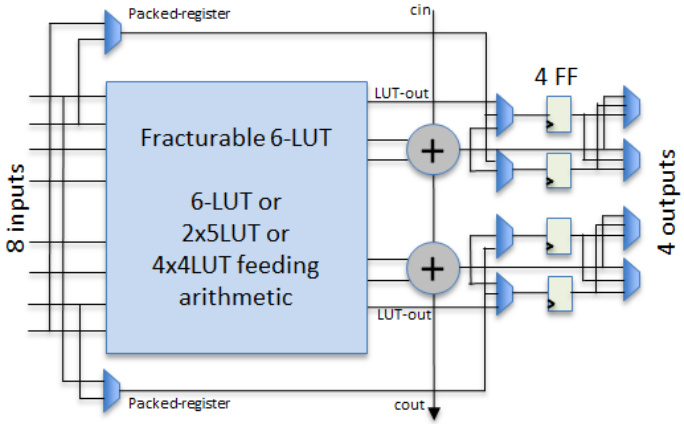
Device Overview and Floorplan

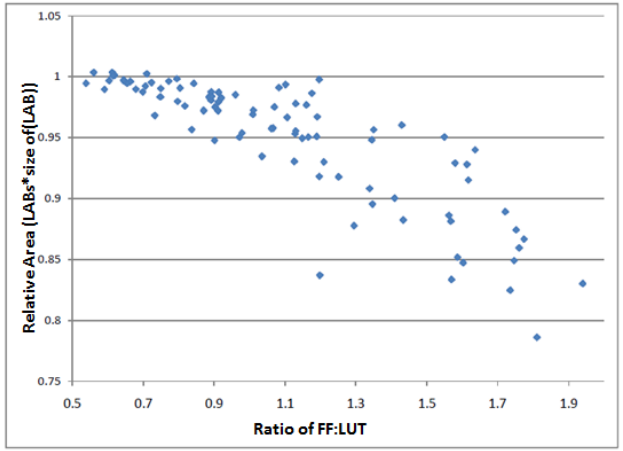
- TSMC 20SoC Process
  - 5.3 Billion transistors, 11 metal layers
- FPGA Resources
  - 1.15M Logic elements
  - 1.7M user flip-flops
  - 64 Mb of embedded memory
  - IEEE 754 floating point with 1.5 TFLOP throughput
  - Dual-core ARM® Cortex®-A9 at 1.5GHz
- FPGA I/O
  - 28G SERDES, over 1.7Tb bandwidth
  - x72 2.667Gbps DDR4 w/ Hard Memory Controller
  - Hardened PCIe, Interlaken, 10GE



Arria® 10 Floorplan

Adaptive Logic Module (ALM) registers and dedicated logic

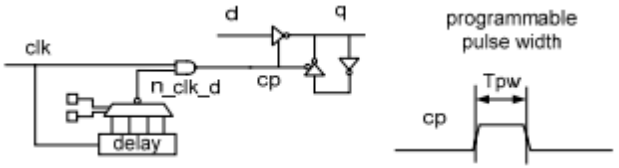




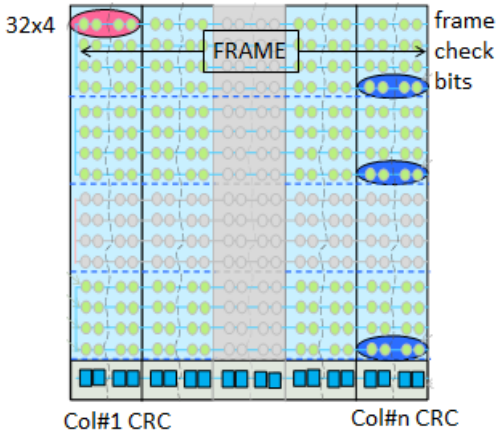
- Adaptive logic module (ALM) based on fracturable 6-LUT (look-up table)
- Many high-performance designs have a Flip-Flop to LUT ratio > 1
- Provided 4 Flip-Flops and 8 LUT inputs to an ALM for more efficient packing

Core Architectural Improvements

- Enhanced range time-borrowing flip-flops (TBFFs) for micro-retiming



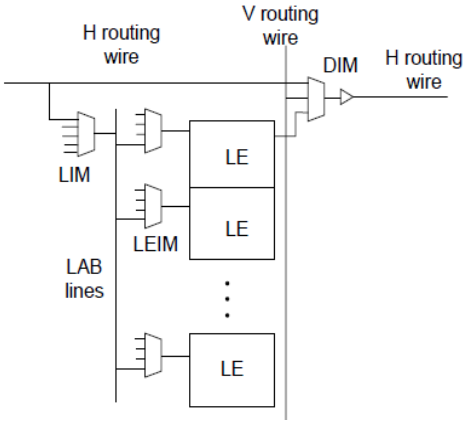
- Column based CRAM CRC in addition to row based CRC
  - Improved SEU detection time from 68ms on Stratix V for 952KLE to 22ms on Arria10 for 1.1M LE

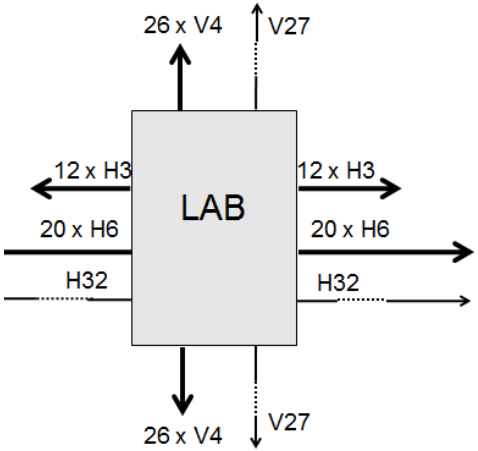


- Improved long-wire utilization for V27, H32 wires using tri-stated wires, replacing the direct drive wires from preceding devices
  - Modest Fmax improvement (0.72%) despite metal scaling challenges

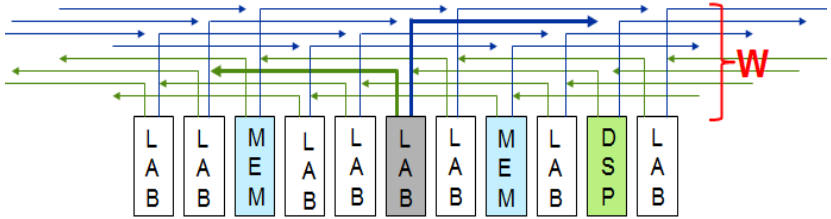
Routing Architecture in Arria® 10

- N/S/E/W wires
  - Direct Drive (uni-directional)
  - Each is a routing mux + driver
- Enter LAB via LIM (60)
- Enter ALM via LEIM (8*10 + 6)
- Exit on DIM routing





- Horizontal Channel Width
  - 12*2*3 + 20*2*6 + 2*32
- Vertical Channel Width
  - 26*2*4 + 2*27

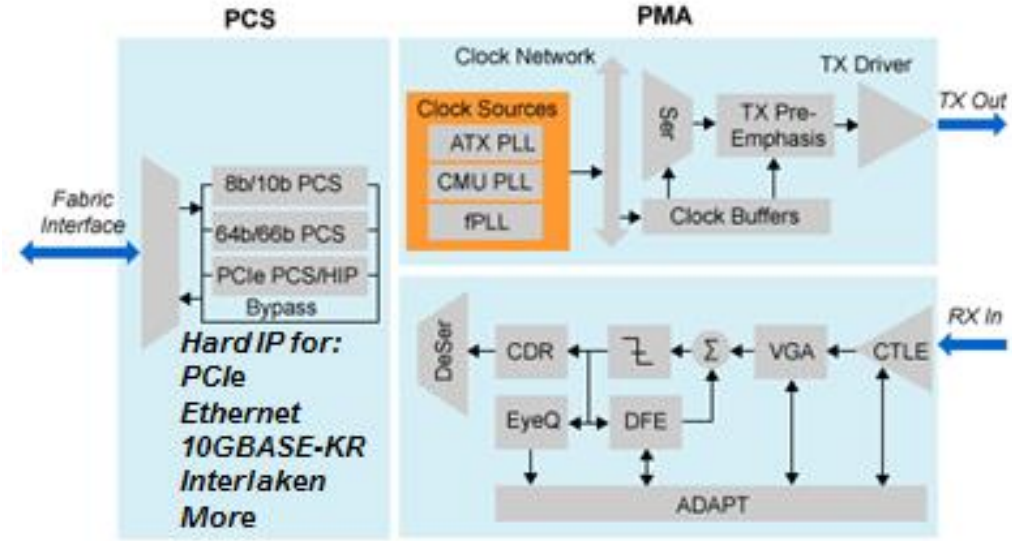


Routing Fabric

Arria® 10 Transceiver Overview

- Architecture supports a wide range of protocols, data rates and applications

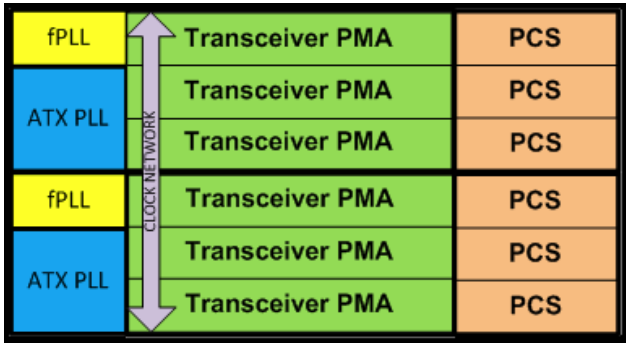
  - Gearbox for configurable interface widths
  - Integrated protocol hard IP blocks
  - Low jitter programmable clock sources
  - Flexible clock distribution networks
  - Advanced adaptive equalization



Arria® 10 Transceiver Overview

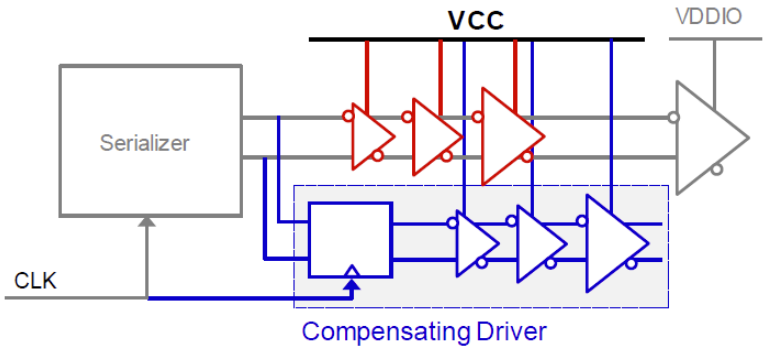
- Wide range of data rates
  - 611 Mbps – 28.1Gbps (Native)
  - Down to 125 Mbps via oversampling
- High Transceiver Density
- Notable improvements
  - 5-tap transmitter pre-emphasis
  - Adaptive Continuous Time Linear Equalization (CTLE)
    - High gain and High data rate modes
  - Adaptive Discrete Feedforward Equalization (DFE)
    - 7 tap fixed, 4 tap floating
  - Hard Forward Error Correction (FEC)
  - Total Equalization Capability > 30db

Feature	Capability
Transceiver count	Up to 96
Max Data Rate (Select Channels)	28.1 Gbps
Max 28G Channels	Up to 16
Max Data Rate (All Ch)	17.4 Gbps
Max Backplane Data Rate	17.4 Gbps

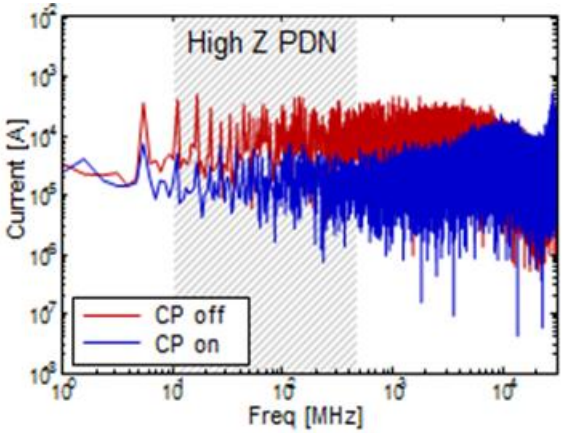


PMA Transmitter Jitter Compensation

- Replicates clock pattern to act as noise compensation
  - Designed to avoid hitting PDN resonance
  - Add switching current using duplicated pre-driver path for identical sequential data bits to eliminate mid frequency noise



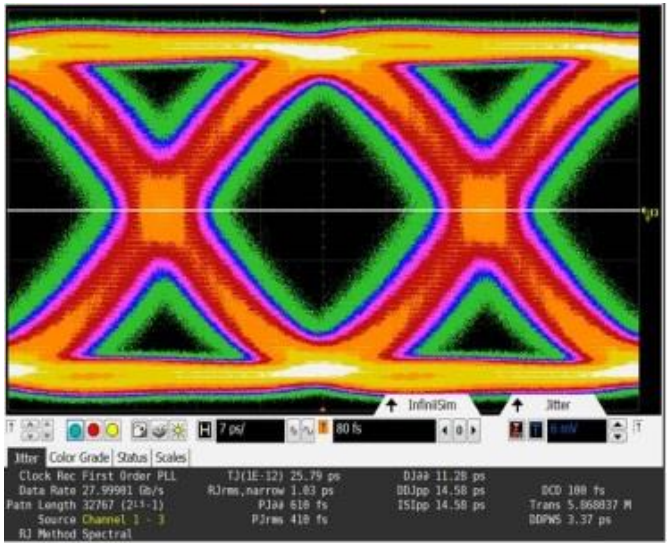
Block diagram



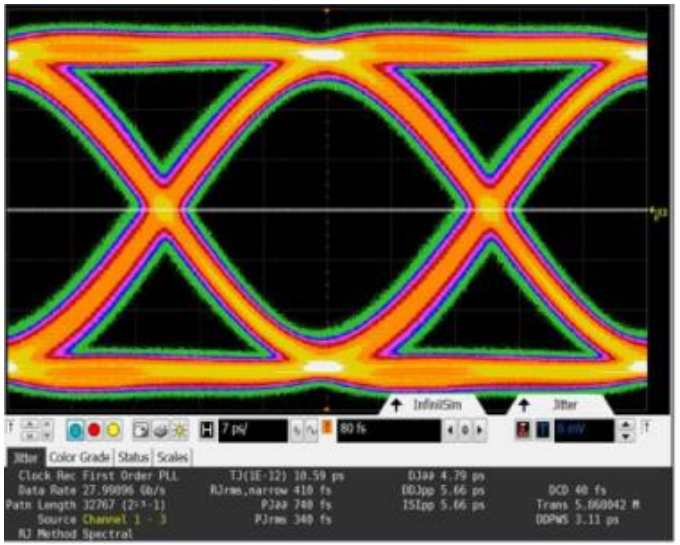
Power supply noise spectrum

PMA Transmitter Jitter Compensation Results

- Reduces PDN induced jitter by 80%
  - Equivalent result from on-die capacitance would increase transceiver area by 50%
  - Average power increases slightly, with no increase in maximum power



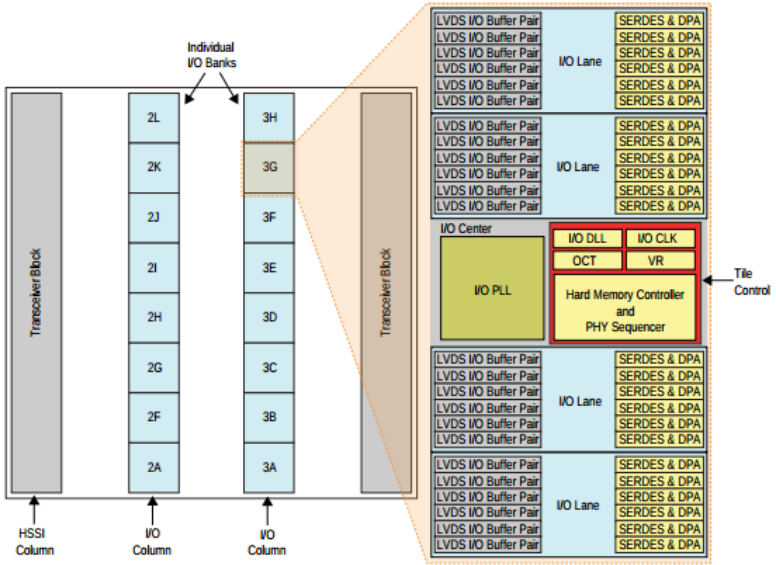
Compensation Off



Compensation On

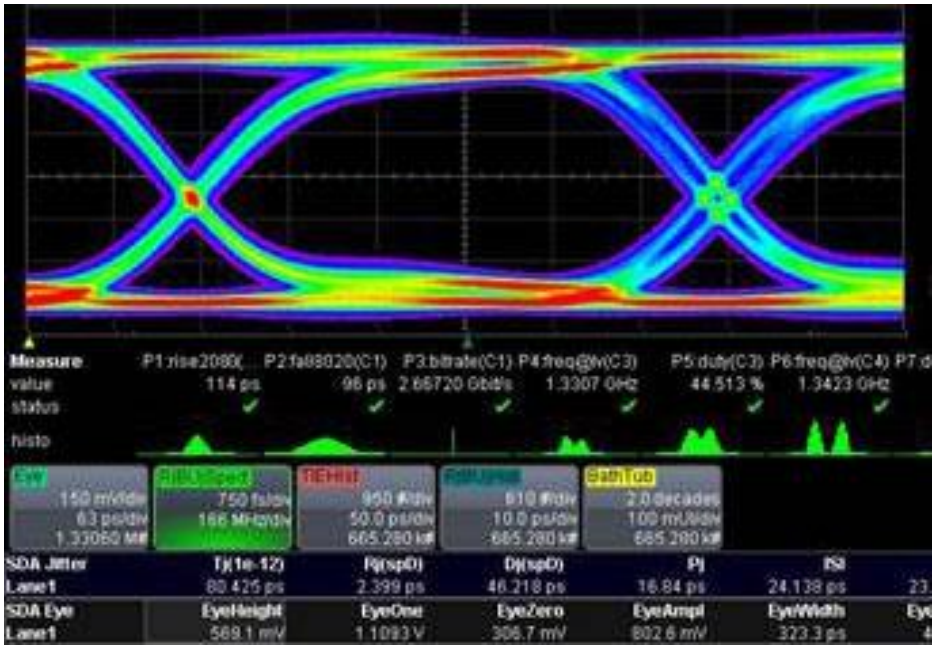
General Purpose IO and External Memory Interface

- Hardened memory controller (HMC) for DDR
  - Programmably mapped to multiple memory interfaces
- Memory subsystem performance
  - 2.667 Gbps DDR4
  - 2.133 Gbps DDR3
  - 1.6Gbps LVDS
- Programmable microcontrollers drive calibration sequences for each IO column



High Performance Memory Results

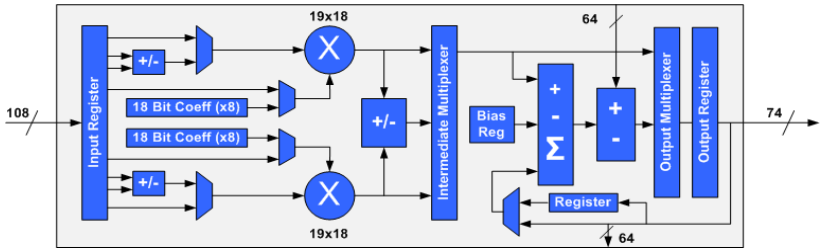
- Flexibility and performance through on-die optimization routines
  - DQS calibration
  - Post-Amble tracking
  - Per-pin read deskew
  - Write leveling
  - Per-pin write deskew
  - Receiver threshold training
  - Command/address calibration
  - FIFO calibration



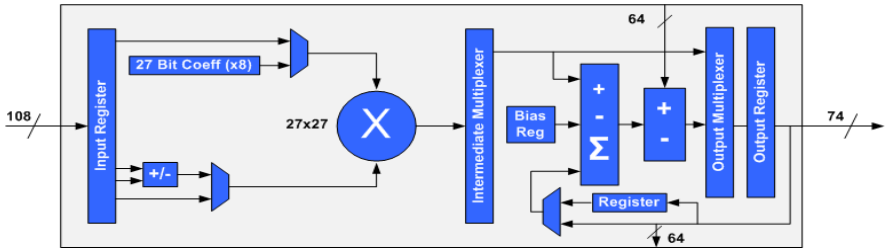
Measured eye diagram for DDR4-1333MHz

Hardened Floating Point DSP

- Included Hardened IEEE 754 Floating point adder and multiplier
  - 12% DSP area increase, <1% die area
- 100% fixed point backwards compatible
  - No performance or power penalty
- Achieved by overlaying floating point algorithms on fixed point circuits
  - Significant architectural advantage



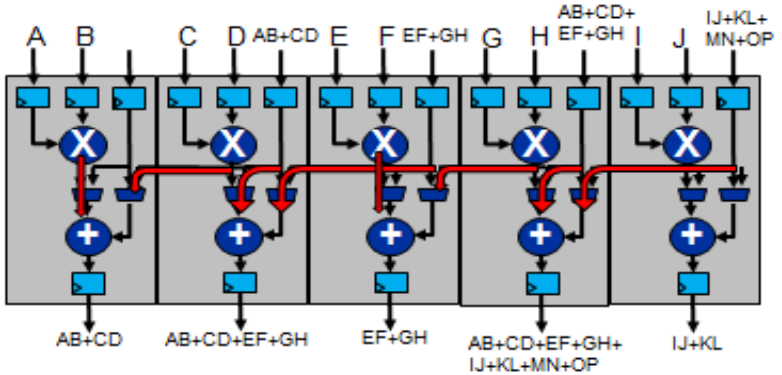
DSP block in dual 19x10 fixed-point mode



DSP block in IEEE 754 floating point mode

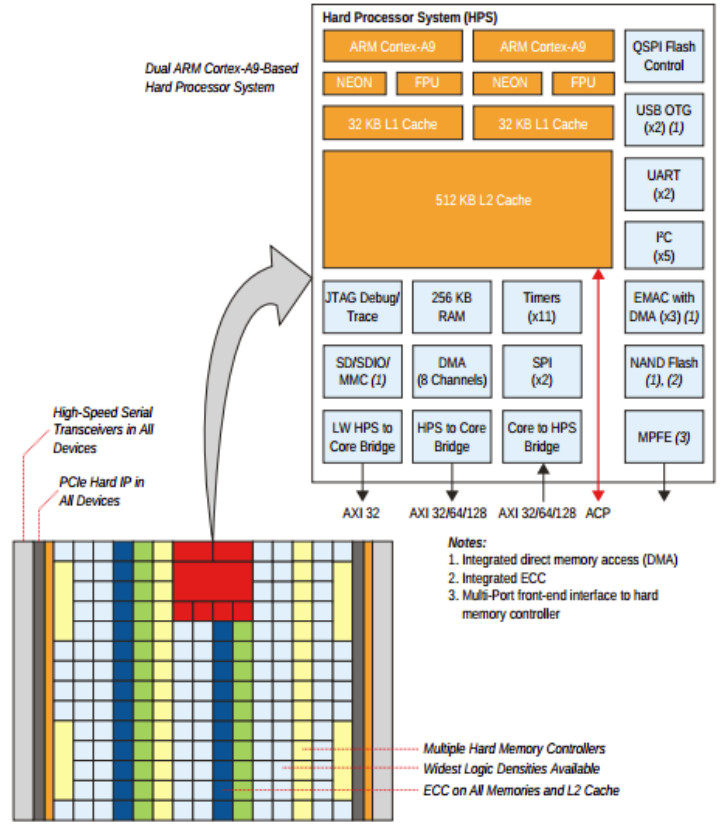
DSP Block – Very Low Latency

- 1.5 TFLOPS of aggregate computation; 50 GFLOPS/W
  - 17678 blocks @ 2 FLOPS/clock @ 450 MHz = 1.52 TFLOPS
  - Can run individually or as a large integrated DSP subsystem
- Hardware recursive structure support (Vector Mode)
  - 10s/100s of DSP blocks can be seamlessly integrated
  - Internal/External pipelining of individual DSP elements
- Floating point used for iterative algorithms – requires small latency
  - Arria® 10 floating point: 256 length dot products ~25 clocks
  - Standard FPGA technology: 256 length systolic FIR filter ~750 clocks



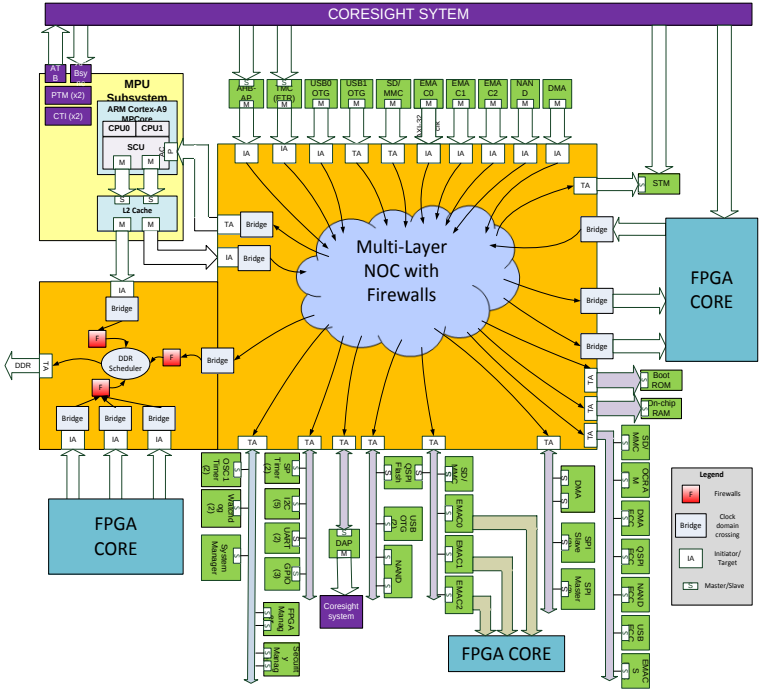
Arria® 10 Hard Processor System

- Arria 10 SoCs feature a dual-core ARM® Cortex®-A9 Processor
  - Up to 1.5GHz, total 7500 MIPS
- Increased security
  - Secure boot with EC DSA Authentication
  - Root of Trust Support (Certificate Authority)
  - Hierarchical Public Key Infrastructure
- Software compatible
  - Extensive reuse of software, OS, Tools reuse from 28nm SoC



Combined SoC and FPGA for HW and SW Co-processing

- High throughput bridge to FPGA
  - Access header/packet data an order of magnitude faster than typical PCIe latency
- Non-blocking, low-latency bridge to FPGA
  - Simple accesses to the fabric
- Shared FPGA/HPS bridge with smart scheduler to DDR interface



Security – Prevention, Detection and Response

Prevention

- AES-256 bitstream encryption
- Key masked prior to storing
- DPA Resistance
- JTAG readback not allowed
- JTAG disable
- Factory Test-mode disable
- Tamper-Protection mode
- On-chip Oscillator

Detection

- JTAG monitoring
- Built-in SEU detection
- On-chip Temperature sensor
- On-chip Oscillator
- Unique Chip ID
- Secure Boot (Code Authentication)
- VBAT Under-voltage detection

Response

- JTAG disable
- Built-in SEU correction
- Chip-core zeroize
- Volatile Key zeroize
- And more!

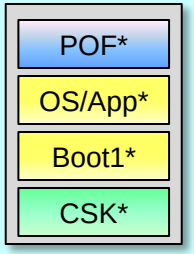
Arria® 10 Secure Key Storage

- Every certification creates 3 keys
  - Private, public, and code signing keys
- Private key storage
  - Remains on source system and is invisible
- Public key storage
  - Hash value of the public key stored in device eFUSE memory
  - In manufacturing, eFUSE is blown by Quartus® II programmer
  - All devices in the field must run authenticated software
- Code signing key
  - Stored in processor boot flash

Private key
- Remains on secure system

Public Key
- Stored in device eFUSE

Code signing key
- Stored in boot flash



Arria® 10 Power Saving Features

Smart VoltageID

- Enables device to run at lower Vcc than nominal level, reducing static and dynamic power while maintaining performance

Programmable Power Technology

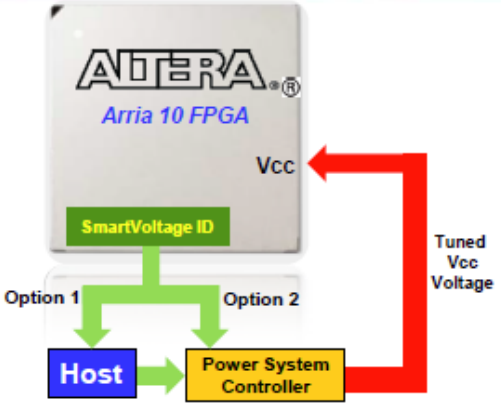
- Utilizes low-power transistors for non-performance critical paths, reducing static power

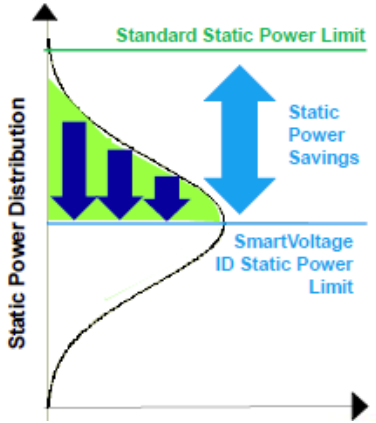
Vcc Power Manager

- Lower operating Vcc level, trading off performance to achieve lower power

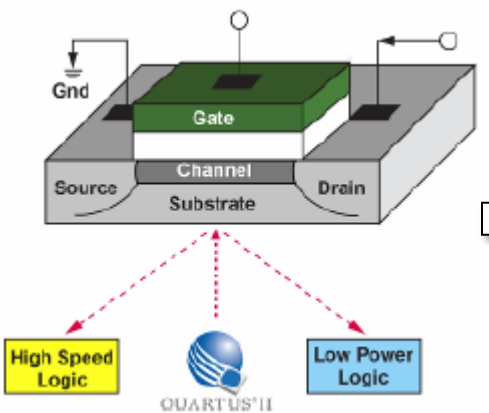
Smart Voltage ID

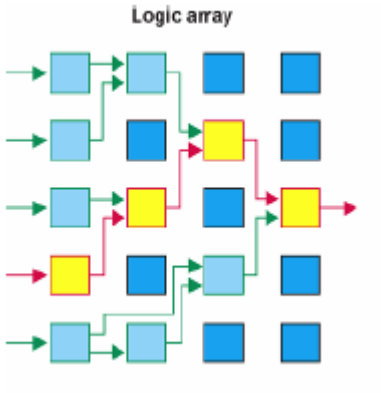
- Allows the FPGA core to run at lower Vcc while maintaining the same performance
- Reduces worst case static power
- Reduces average dynamic power consumption across distribution of devices
  - Lowers customer Operating Expenses
- Requires power system controller that can support tuned voltage
  - Power savings seen near 35%

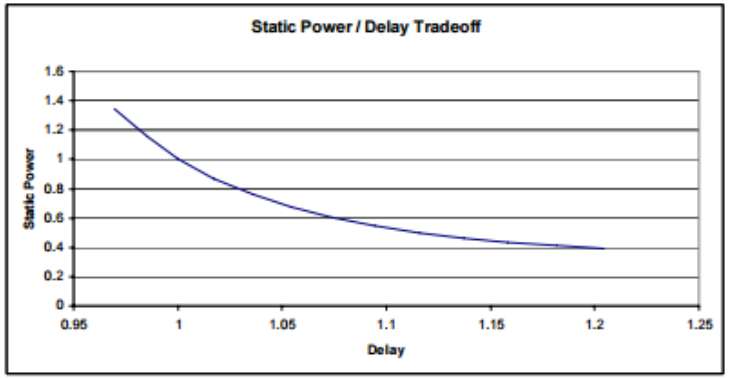




Programmable Power Technology







Static power across bias-range

Dynamic Back-Bias, set in CRAM (bitstream)

Granularity per-block (LAB)

Quartus® II software can choose which blocks to make fast or low-power

Done iteratively until further usage would violate timing

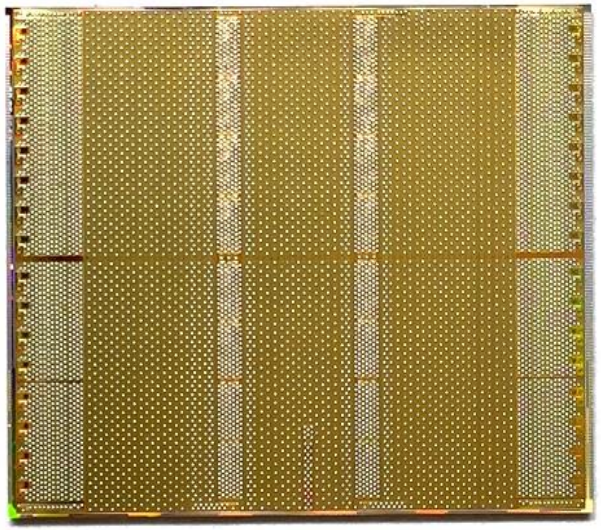
Resulting savings varies, but hits 20% in some designs

Summary – Arria® 10 Device Architecture

- Mid-range FPGA family balancing power, performance and cost

- High density and capabilities
  - 5.3 Billion transistors, 11 metal layers, TSMC 20SoC
  - 1.15M logic elements, 1.7M user flops
  - 64Mb embedded memory

- Innovations and features throughout Arria® 10
  - Dual-core ARM® Cortex®-A9 system at 1.5GHz
  - Hardened floating point DSP at 1.5TFLOP throughput
  - High-speed external memory at 2.667Gbps
  - 28G transceivers
  - Power management techniques
  - SoC and FPGA security



Arria® 10 Die Photo