A Soft-Error Hardened Process Portable Embedded Microprocessor

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Outline

- Motivation
- Highly Efficient Radiation-hardened Microprocessor Enabling Spacecraft (HERMES2) microarchitecture
- Features (added instructions and registers) for software based soft-error recovery and reporting
- Circuits and Physical Design
- Experimental results
- Silicon validation and software based program validation on hardware
- Proton Testing results
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Soft-errors in Logic

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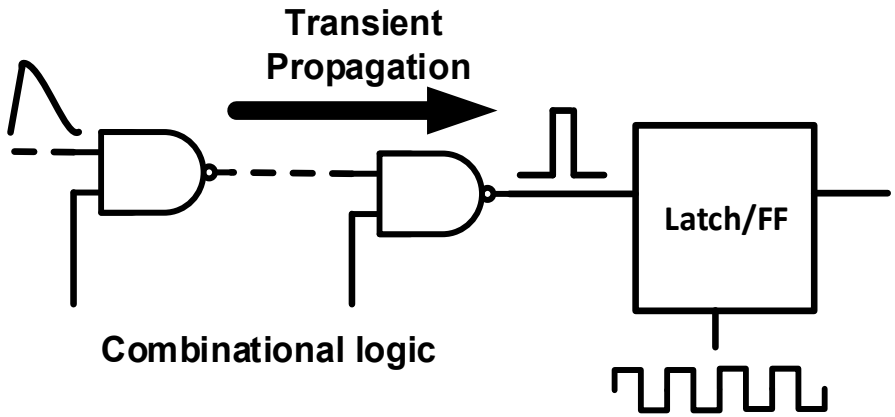
  - **Charge generated by primary or secondary ions**
- **Single Event Transient (SET)**
  - **Temporary voltage glitch at combinational node**



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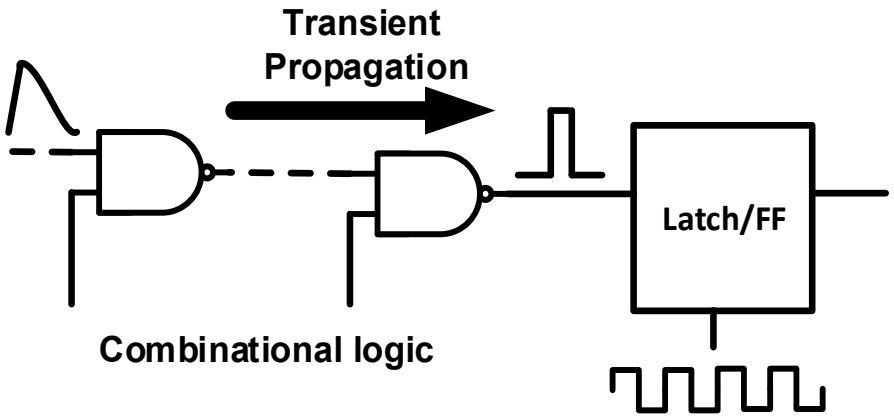

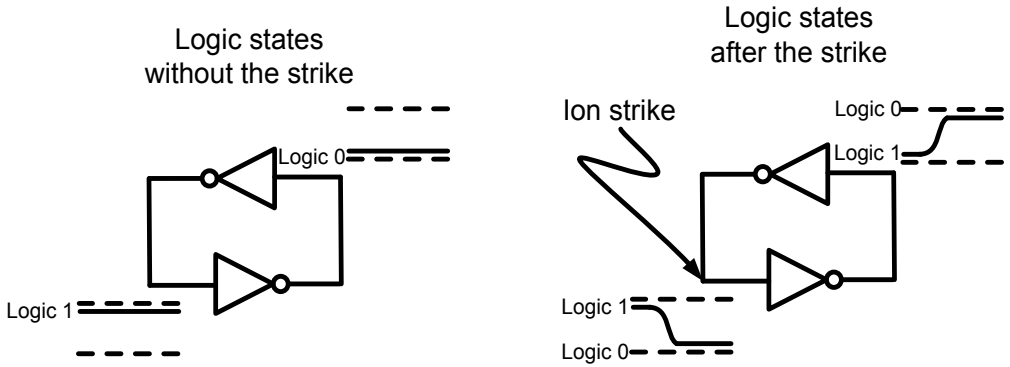

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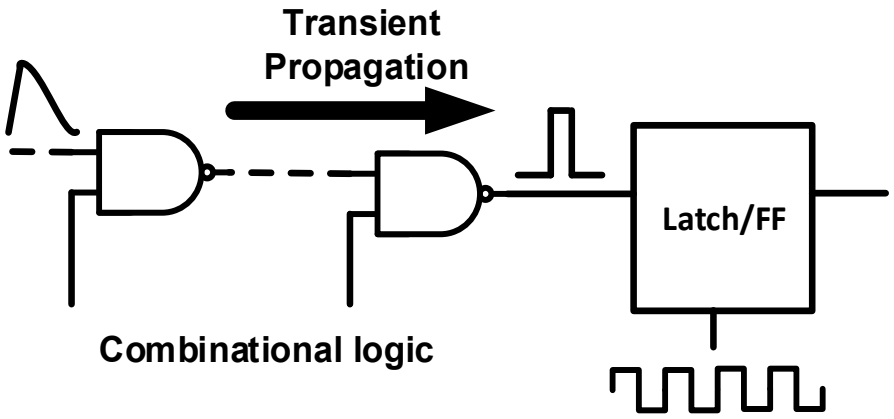
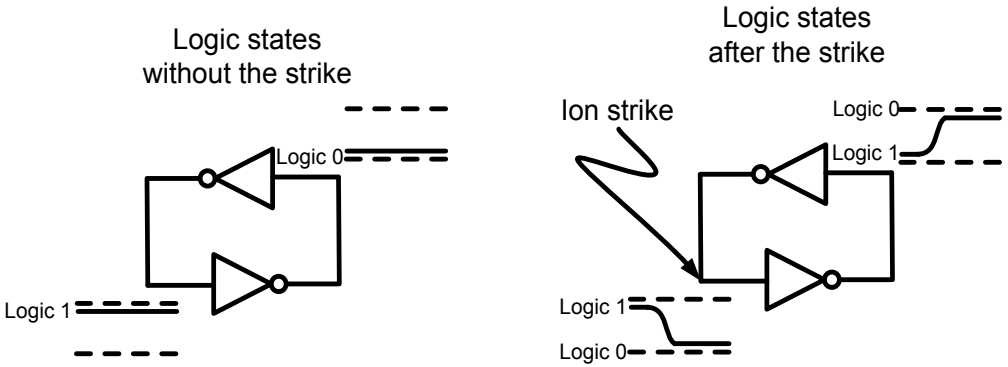
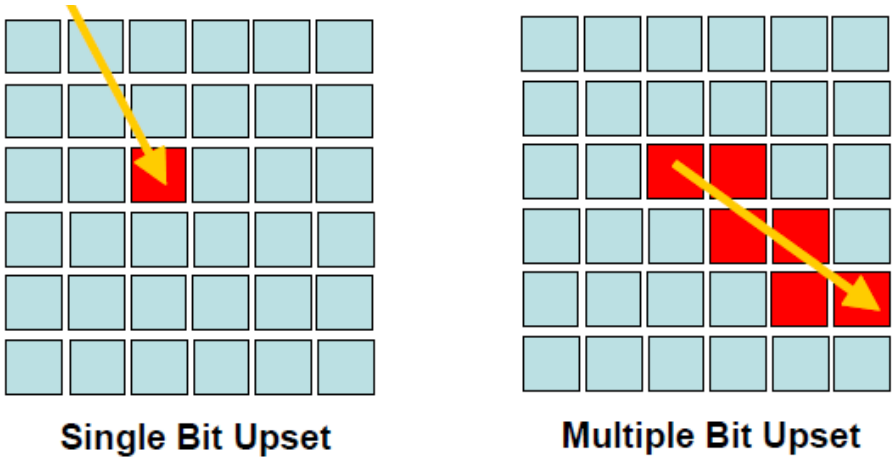
- **Single Event Upset (SEU)**
  - **Directly affects the storage node logic state**
- **Multi-Bit Upset (MBU)**
  - **Caused by multi-node charge collection (MNCC)**
  - **Must be mitigated by separating storage cells**







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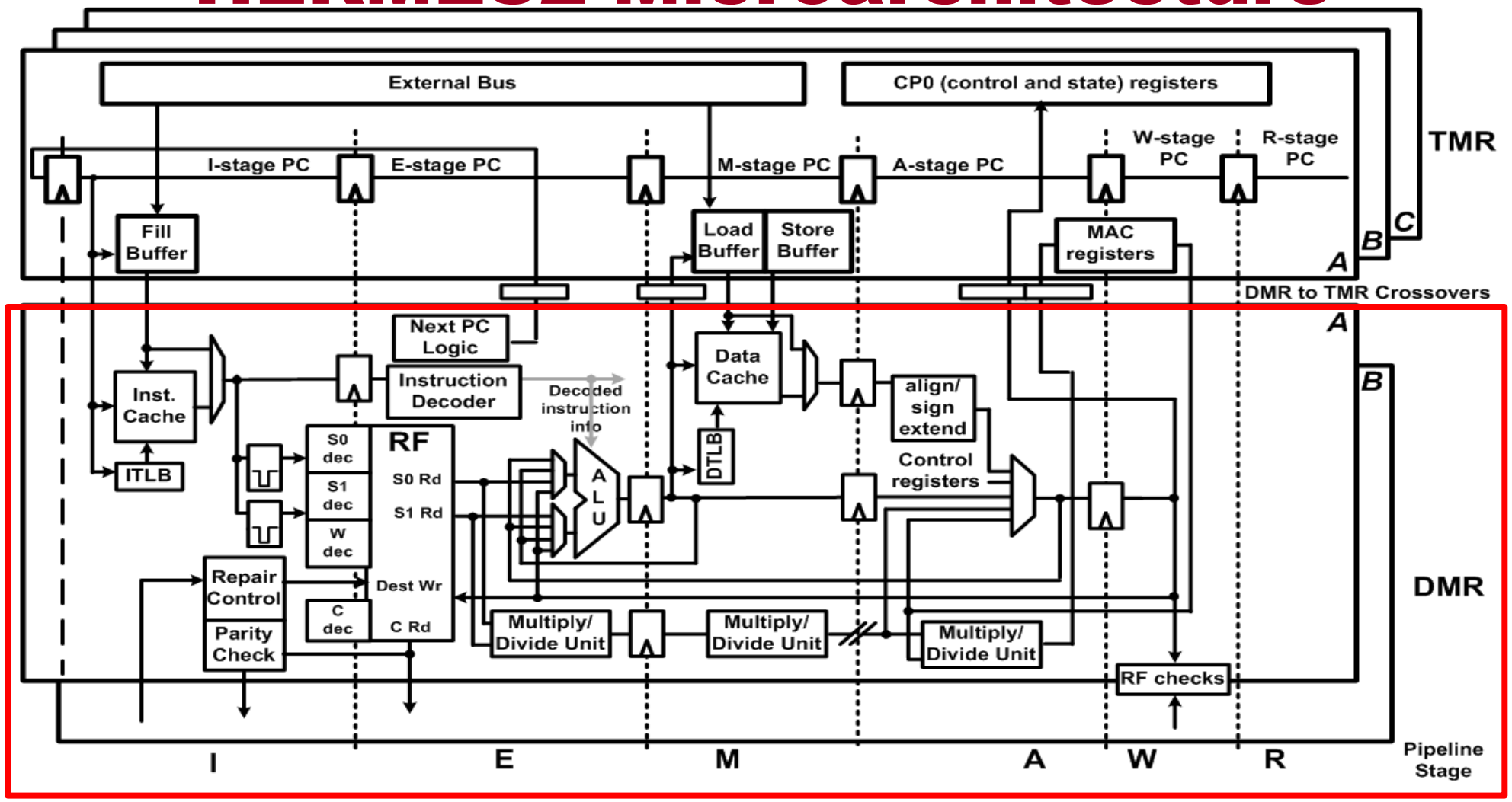
HERMES2 Microarchitecture

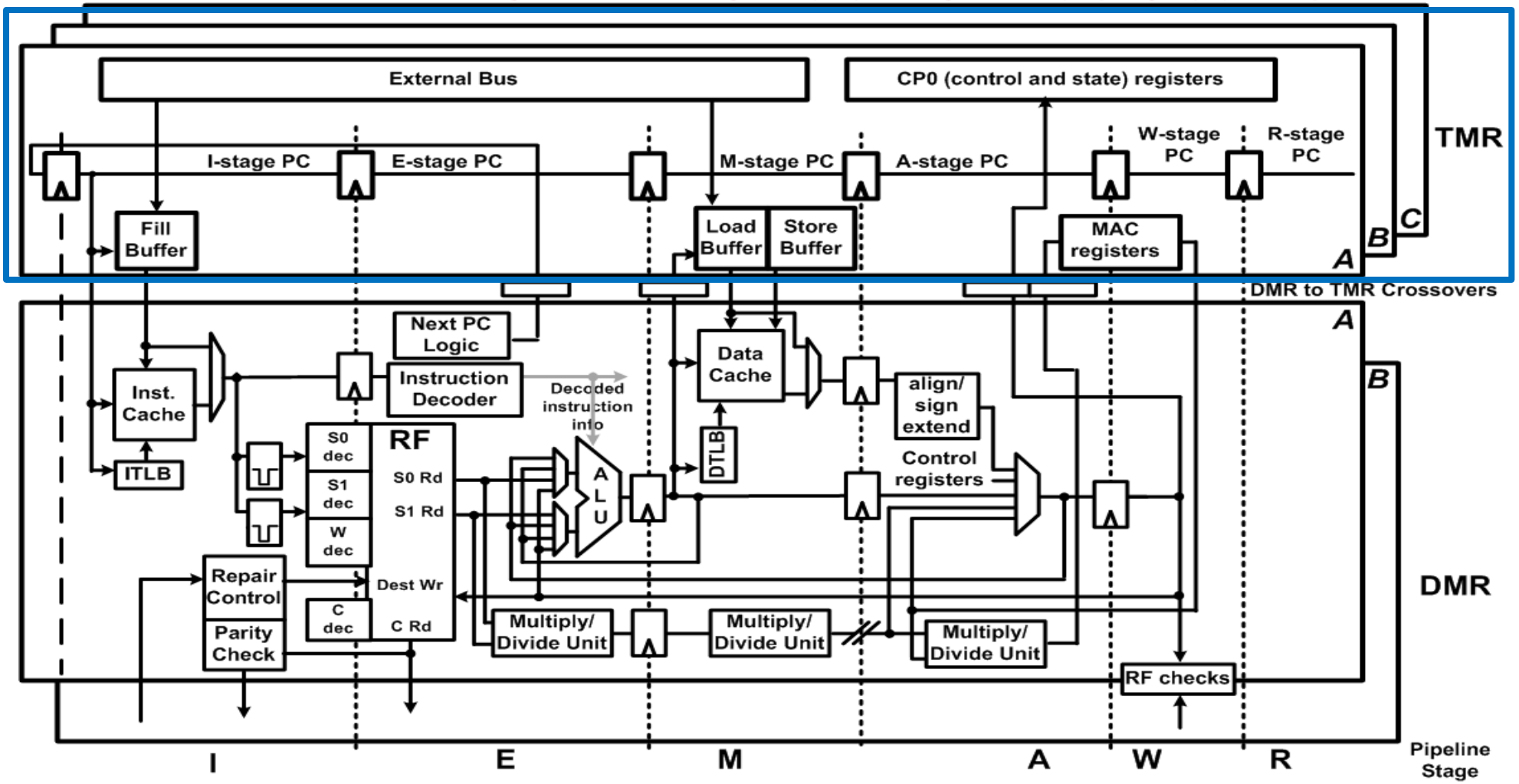
- **MIPS 4Kc clone**
  - **5-stage pipeline**
  - **Full TLB based MMU for operating system support (e.g., Linux)**
- **From scratch (clean-room) microarchitecture for soft-error hardness**
  - **6th pipeline stage added for errors in the branch delay slot**
- **Fully synthesizable**
  - **With considerable help from specialized CAD flows for proper domain separation to avoid MNCC upsets**
  - **Custom circuits for cache arrays and register file**
    - **Based on ultra-low power, fully static readout**
  - **Custom self-correcting triple modular redundant (TMR) flip-flops**
    - **Previously proven hard in heavy ion and proton testing**
- **Software controlled machine repair and reporting on all soft errors**
  - **Any soft-error causes an SE exception (to software handler)**
  - **Excellent for exploring root causes, not just results of errors**

HERMES2 Microarchitecture



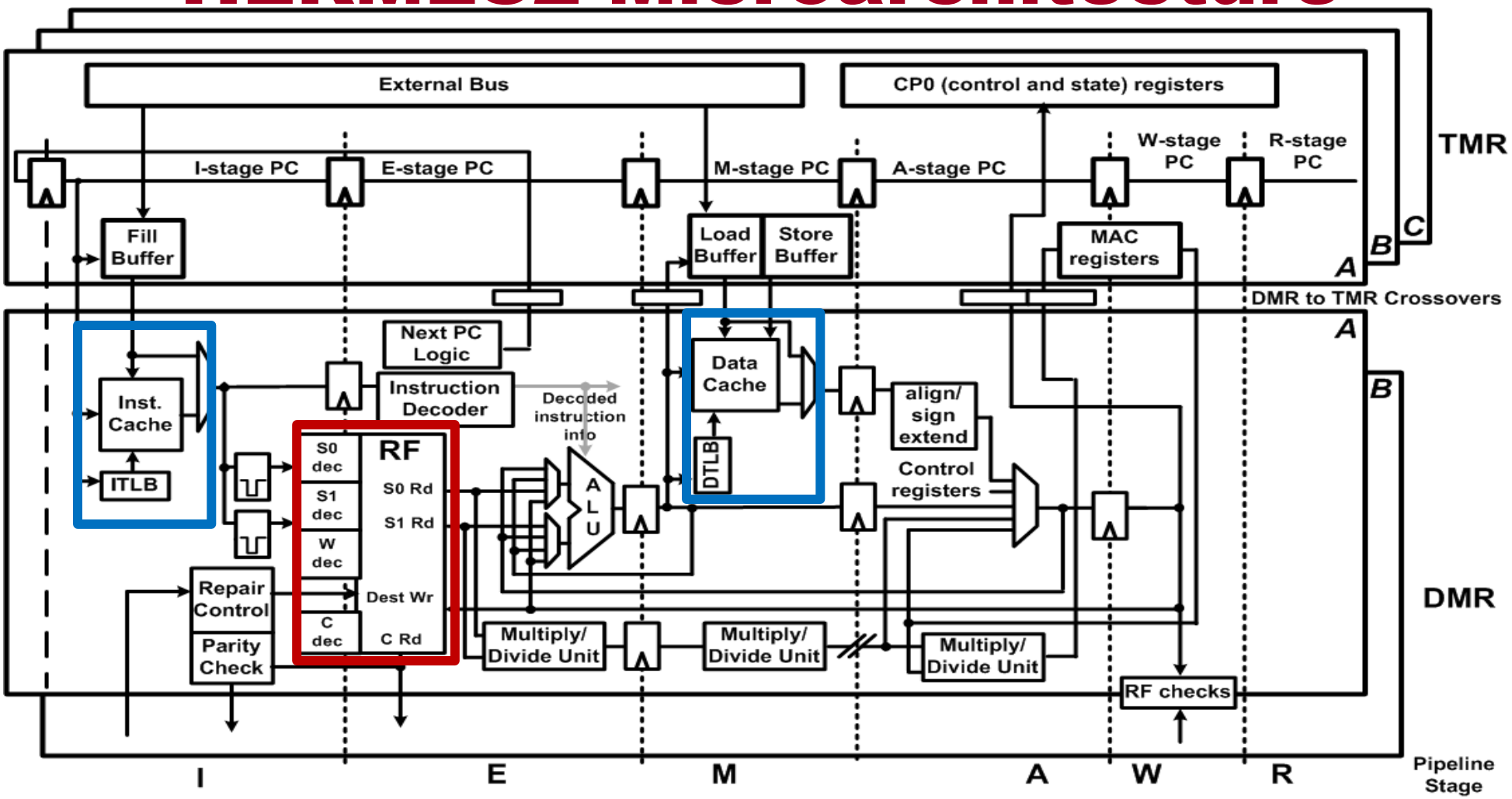
- **Dual modular redundant (DMR) circuits**
  - **For *speculative* state and correctable architectural state**
  - **Two copies allows a mismatch to be detected before committing the speculative machine state to *architectural* state**

HERMES2 Microarchitecture



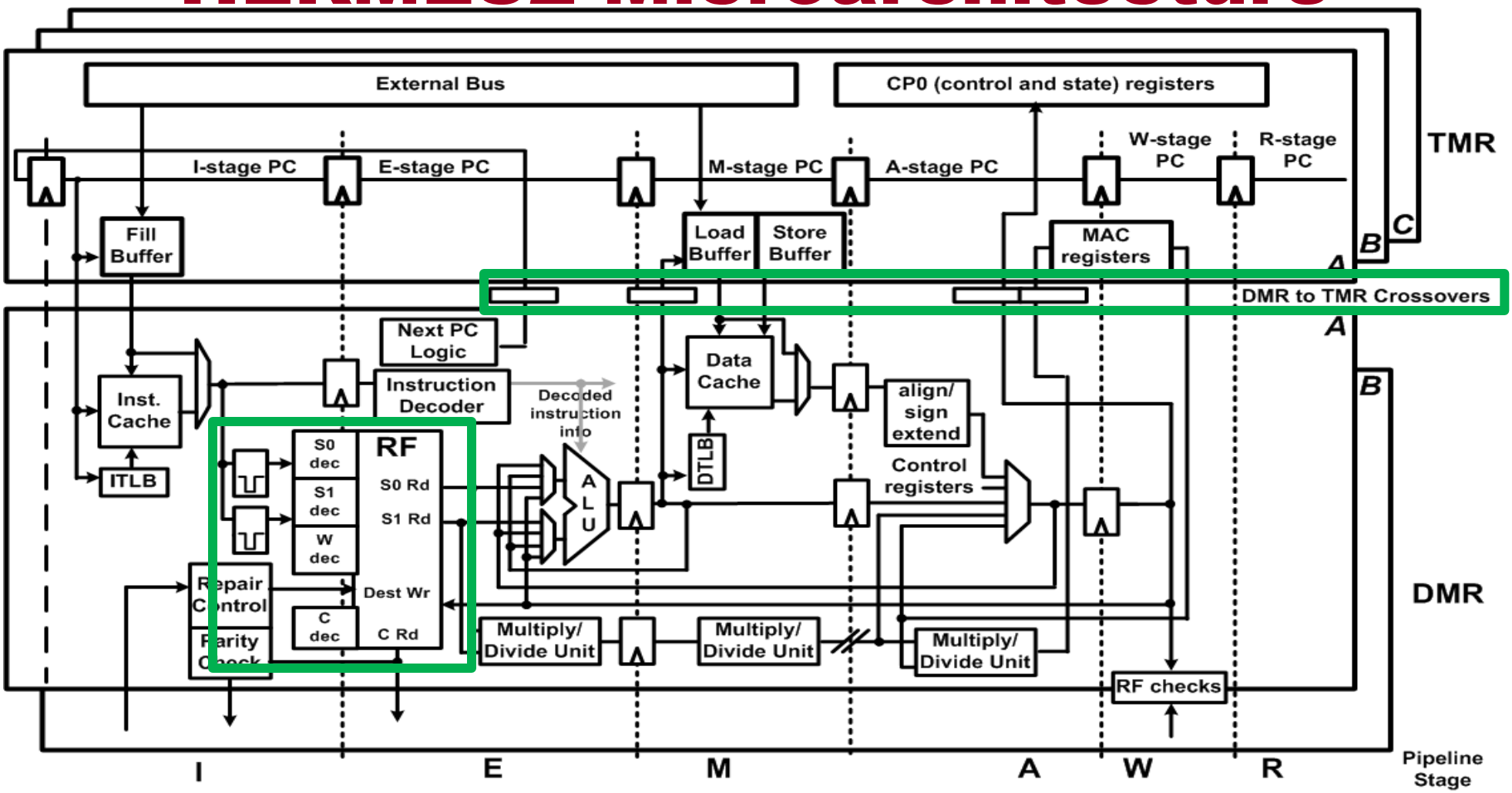
- **Self-correcting TMR circuits**
  - **For key *architectural* state, e.g., program counter (PC)**
  - **This machine state is required for architecturally correct (ACE) operation and cannot be otherwise recovered**
  - **Includes all configuration (e.g., CP0) registers, bus interface**

HERMES2 Microarchitecture



- **Register file (RF) and Caches (and TLBs) are DMR**
  - **RF A and B copies have parity protected 5-bit groups**
  - **Caches are DMR for simplicity—allows rapid porting to new processes**

HERMES2 Microarchitecture



- **7 DMR to architectural state error checkers**
  - **RF parity (from background scrub)**
  - **RF entry select (word-line) mismatch and data mismatch**
  - **DMR to TMR cross-overs for the fill buffer, store buffer, load buffer, and multiply accumulator (MAC)**

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Added Coprocessor Registers

- **The MIPS architecture explicitly allows hardware extensions through the coprocessor registers**
- **Added self-correcting TMR protected registers:**
  - ***SEE EPC*** **that stores the PC to return to after an SE exception**
  - ***RF data and address backup*** **of the next RF entry to be written**
  - ***Error Log 1 and 2:*** **7 specific error checkers prevent DMR data from committing to architectural state**
    - **RF parity error (from background scrub)**
    - **RF word-line (entry) mismatch**
    - **RF write data mismatch**
    - **Data Cache Unit (DCU) load and store buffers**
    - **Instruction fetch unit (IFU) fill buffers**
    - **Multiply divide unit (MDU) buffers to allow recovery of in-flight results—the RF entries may no longer exist when these instructions retire**
    - **Instruction Execution Unit (IEU)**
  - ***Error Mask 1 and 2:*** **To mask error checkers from firing**
    - **Critical to proper error injection based validation**
  - **Registers to control which non-redundant copy for test instructions, etc.**

Added Instructions

- **Instructions added to enable potentially very fast recovery and to control error correction:**
  - ***Back up register file (BURF)*** **restores the register file state to that before the instruction that triggered the error**
  - ***Repair general purpose register (RGPR)*** **repairs RF entry SEUs**
    - **This instruction compares the DMR copies of a given RF location, and 5-bit groups with parity errors are overwritten from the redundant 5-bit group with correct parity**
  - ***TLB invalidate (TLBINV)*** **and extensions to the standard MIPS CACHE instructions provide single-cycle TLB/cache invalidation**
- **Test and recovery instructions to access single instances of the DMR copies**
  - **Extensions to the CACHE instructions**
    - **Read and write for error reporting and validation, respectively**
  - ***RF testability write (RFTW)*** **allows single instance writes**
    - **Can inject errors for processor validation and recovery test checking**
  - ***Read RF data (RDRFDAT)*** **allows data or parity to be examined independently of the check/repair mechanisms**
    - **For error reporting**

Software Based Error Recovery

- Checkers fire when mismatching A and B DMR data tries to commit to architectural state
- A detected SEE error raises an (SE) exception
  - Executes in uncached memory—*the cache may be the cause*
  - Error handler determines the error is SE and not a normal exception—*Soft-errors take priority, since they can cause other exceptions*
    - **Write and read register 0!** If reads back non-zero, it is SE
    - R0 being read/write allows us a spare register to repair the RF using software

1. If the RF was written at the soft error, back it out
   - **BURF** instruction puts the old value back
- (optionally) Report RF errors and the cause (**Error Log**)

2. Repair the register file
   - For each register: **RGPR** R1, **RGPR** R2, … **RGPR** R31
- (optionally) Report cache errors

3. Invalidate the TLBs, I-caches and write-through D-caches
4. Return from the exception
   - The machine is now 'clean'
   - Restart by re-executing the last retired instruction

- SE exception handler can be as few as **86** or as many as **115,328** instructions

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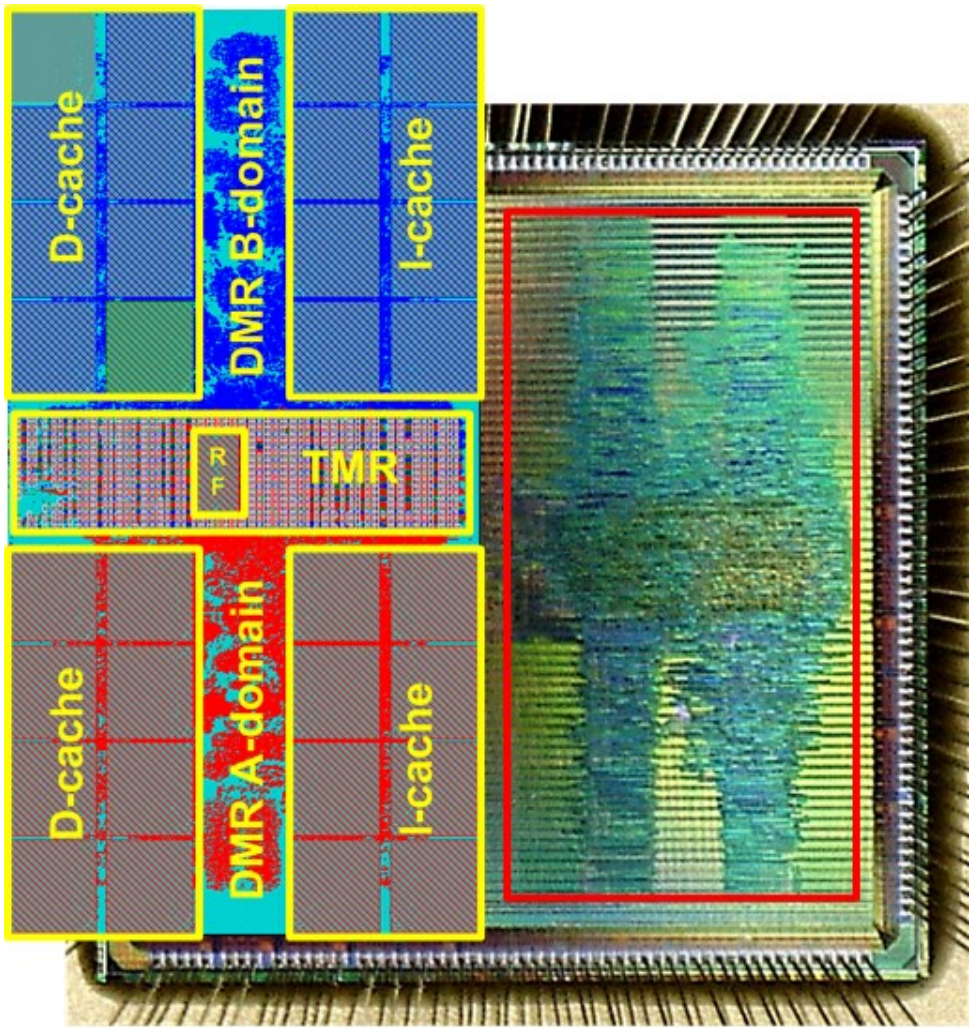
Physical Design

- **Auto-place and route flow keeps DMR and TMR domains separate to avoid MNCC upsetting 2 copies**



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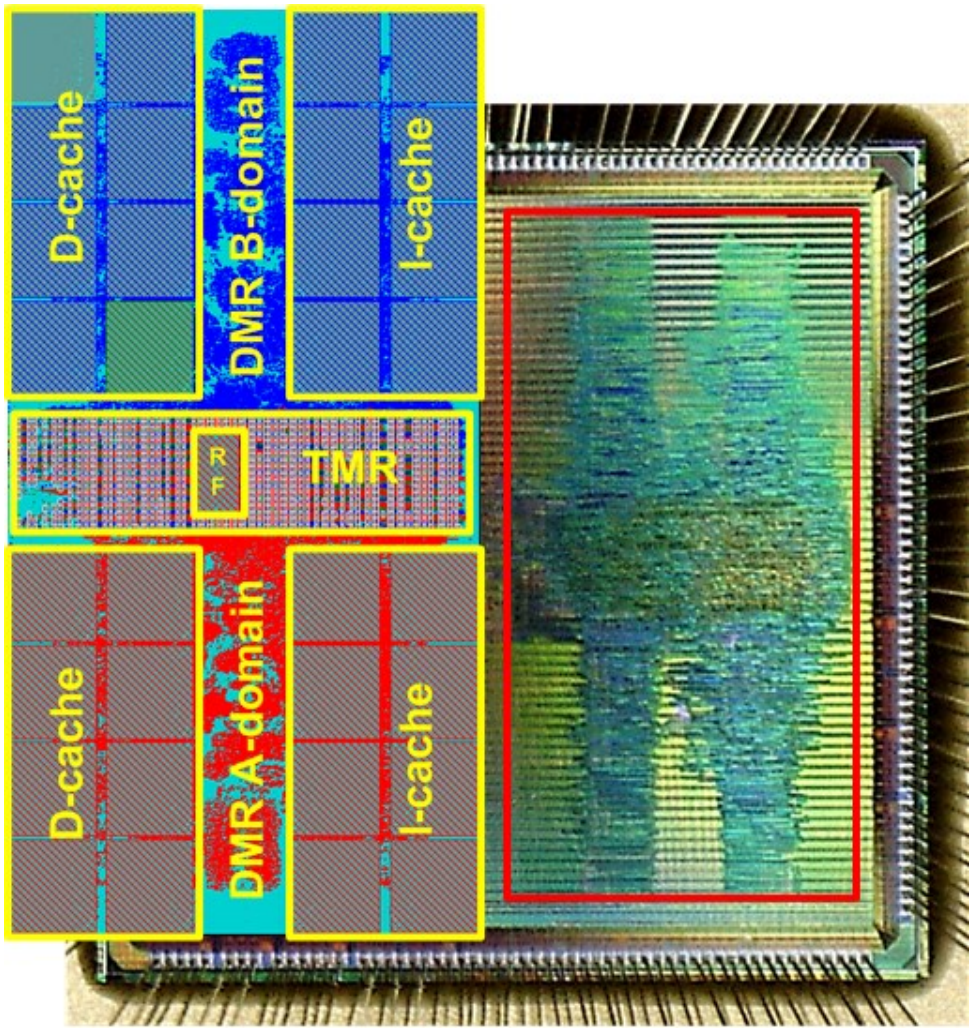
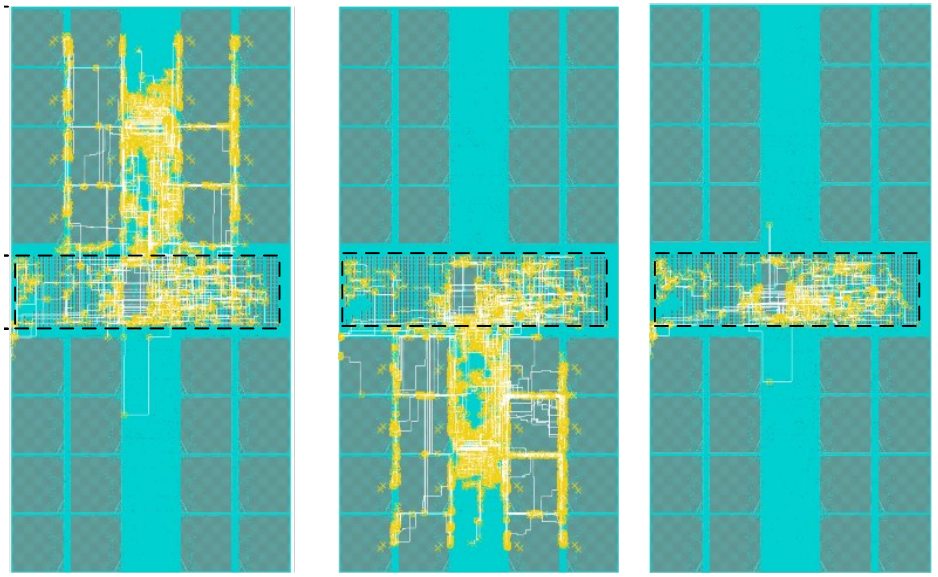
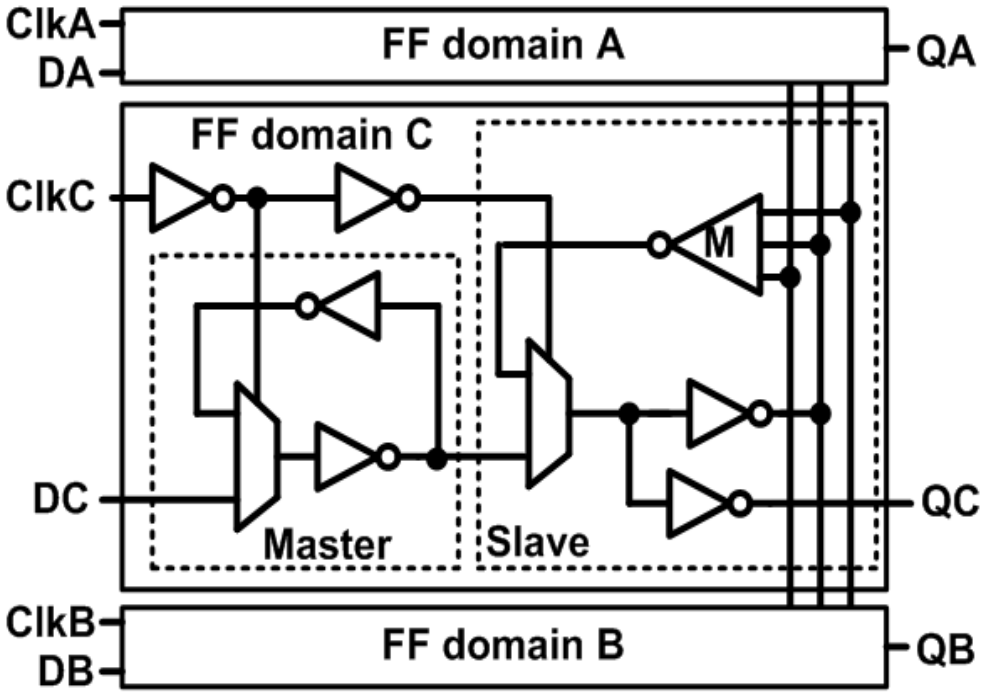


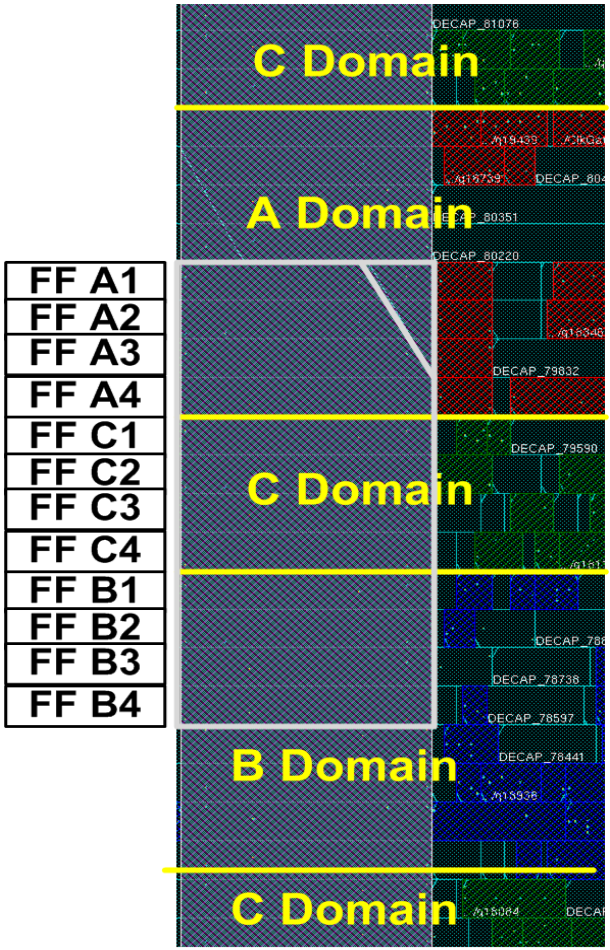


- **Separate clock trees for each of the A, B, C domains**
  - **Clock SET or clock gating enable upset immune**

Circuit Design: Self-correcting FFs

- **Self-correcting TMR flip-flops (FFs) contain key architectural state**
  - **This logic self-corrects and thus does not report errors**
  - **Layout prevents MNCC upsets**
    - **Self-correcting storage bits are separated by 3 rows (and wells)**





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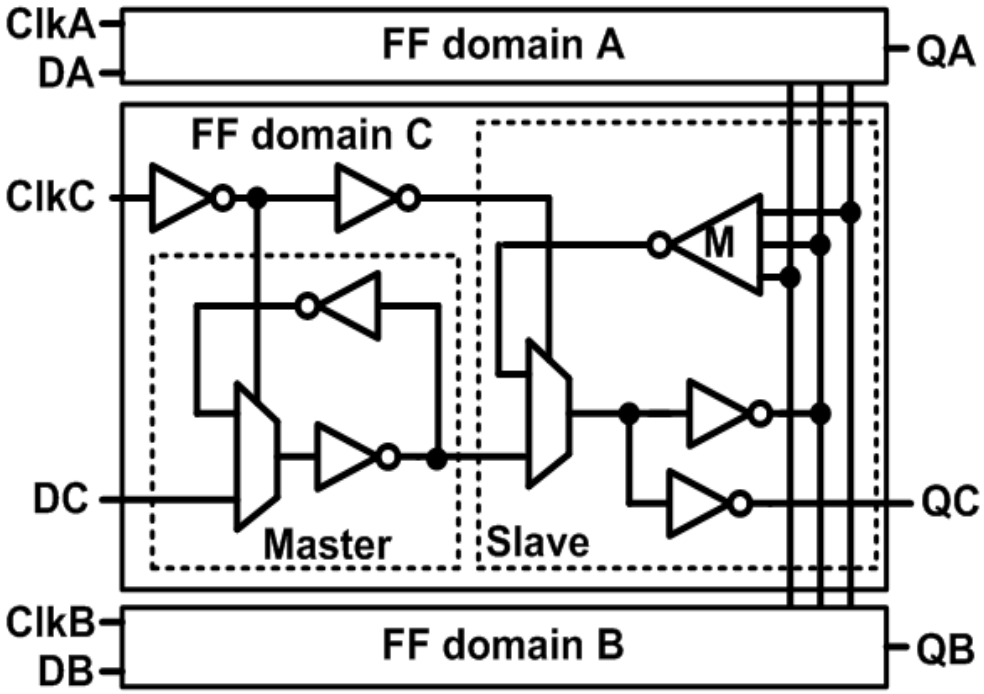
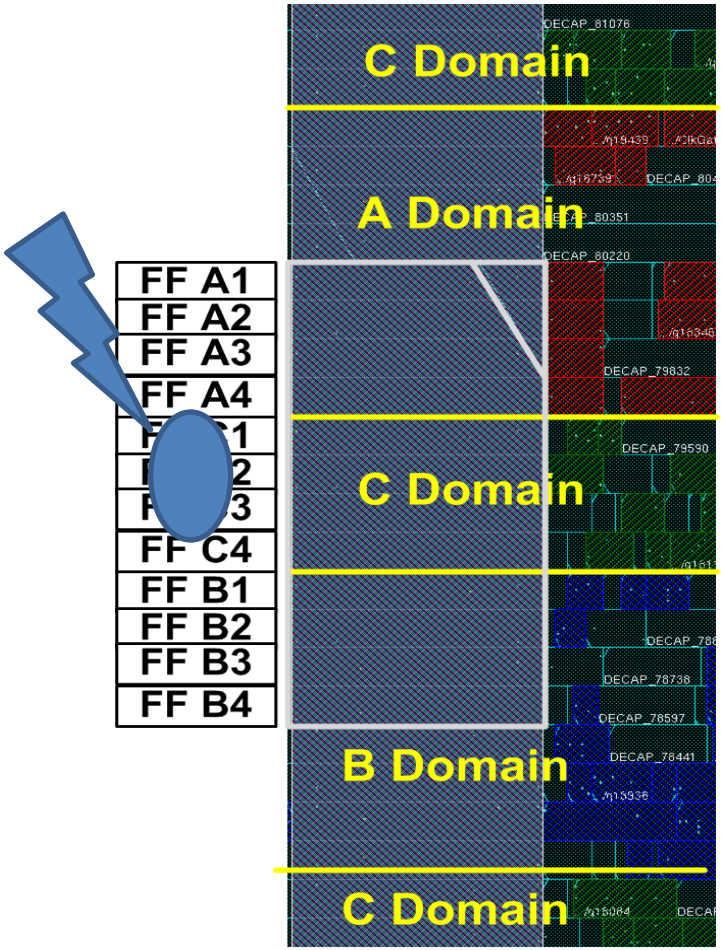
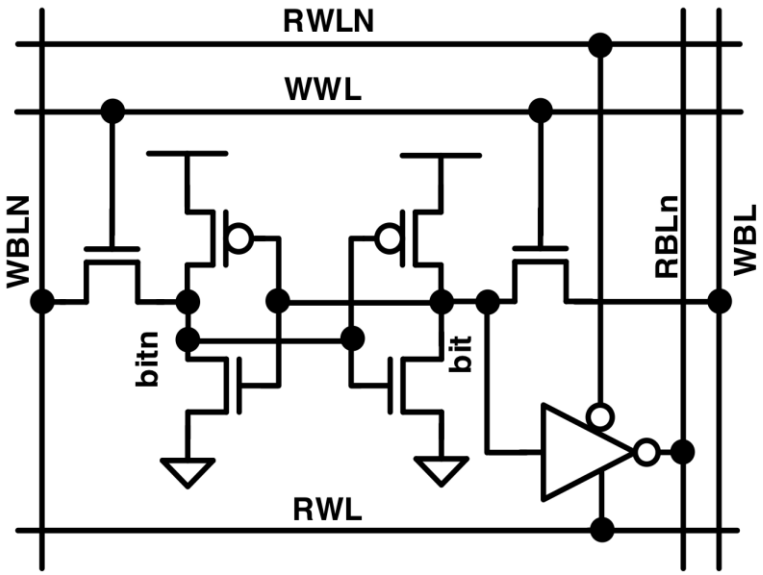
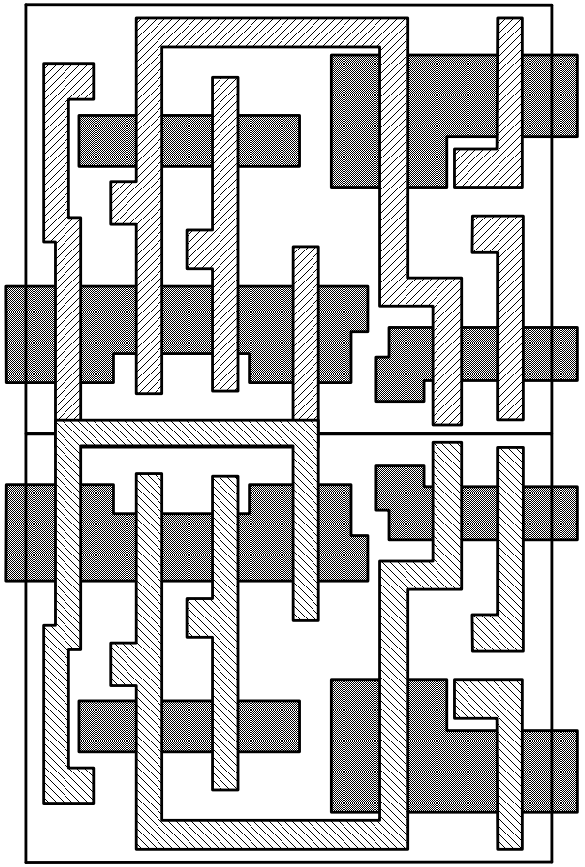


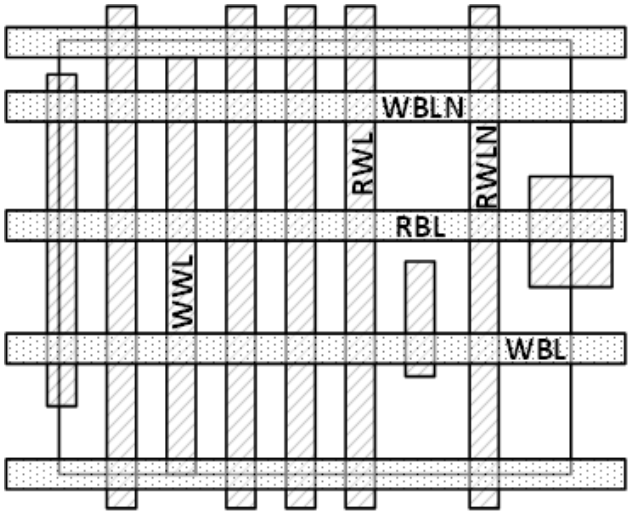


Static RF Cell

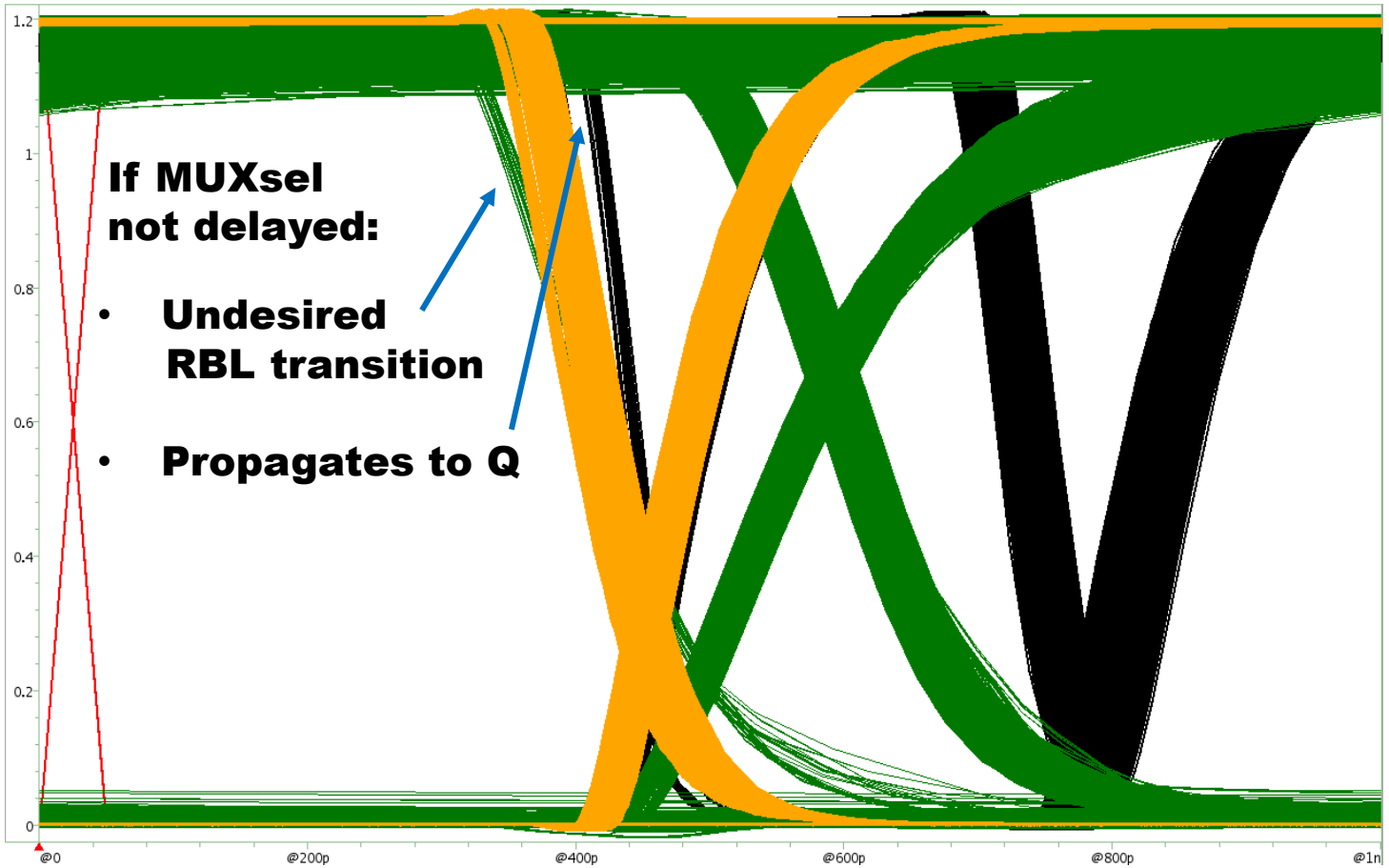




- **1-R 1-W RF Cell features**
  - **Dual-ended clocked write**
  - **Single ended fully static read-out**
    - **Two RWLs required per cell**
- **Layout fits standard cell sizes**
  - **Compatible with 7-track library**
    - **Ability to use library cells in RF array reduces design effort**
  - **Horizontal M3 power and bit-lines**
  - **Vertical M2 word-lines**



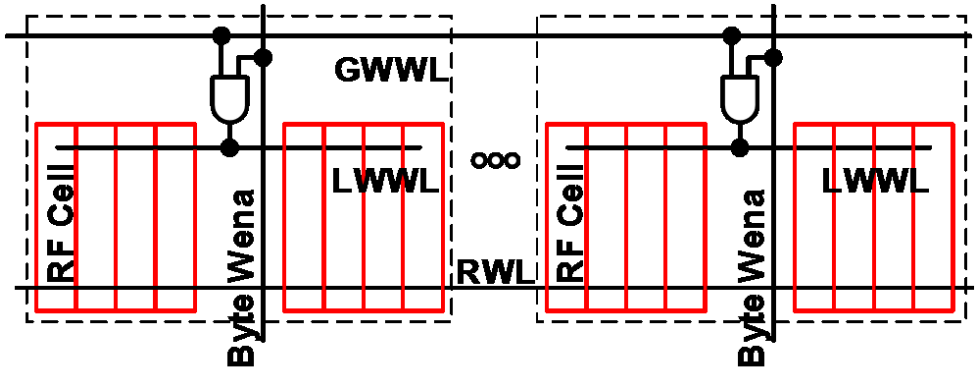
Static RF Read Timing



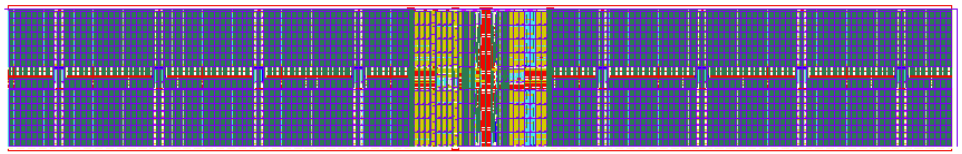
- **No read clocked enable causes RWL contention**
  - **Due to systematic timing variations in the decoder**
- **MUXsel delayed to coincide with the RWL/RWLN pair to avoid output glitching**

Sub-bank and Byte Writes

- **Byte write support required by application**
  - **Cache with byte stores, e.g., SB $1 8($5)**
- **Global WWL qualified by byte write enable to generate local WWL**
  - **This is susceptible to multi-bit soft-errors as storage in one word is adjacent—we don't care because the caches are DMR**

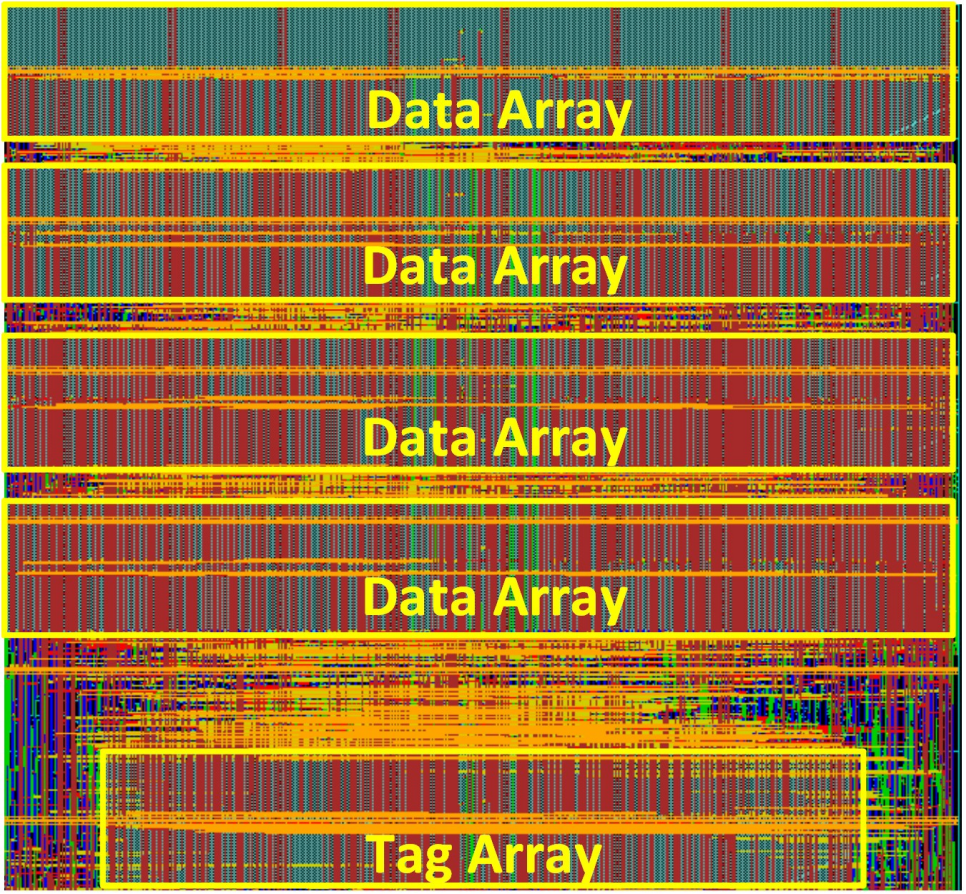


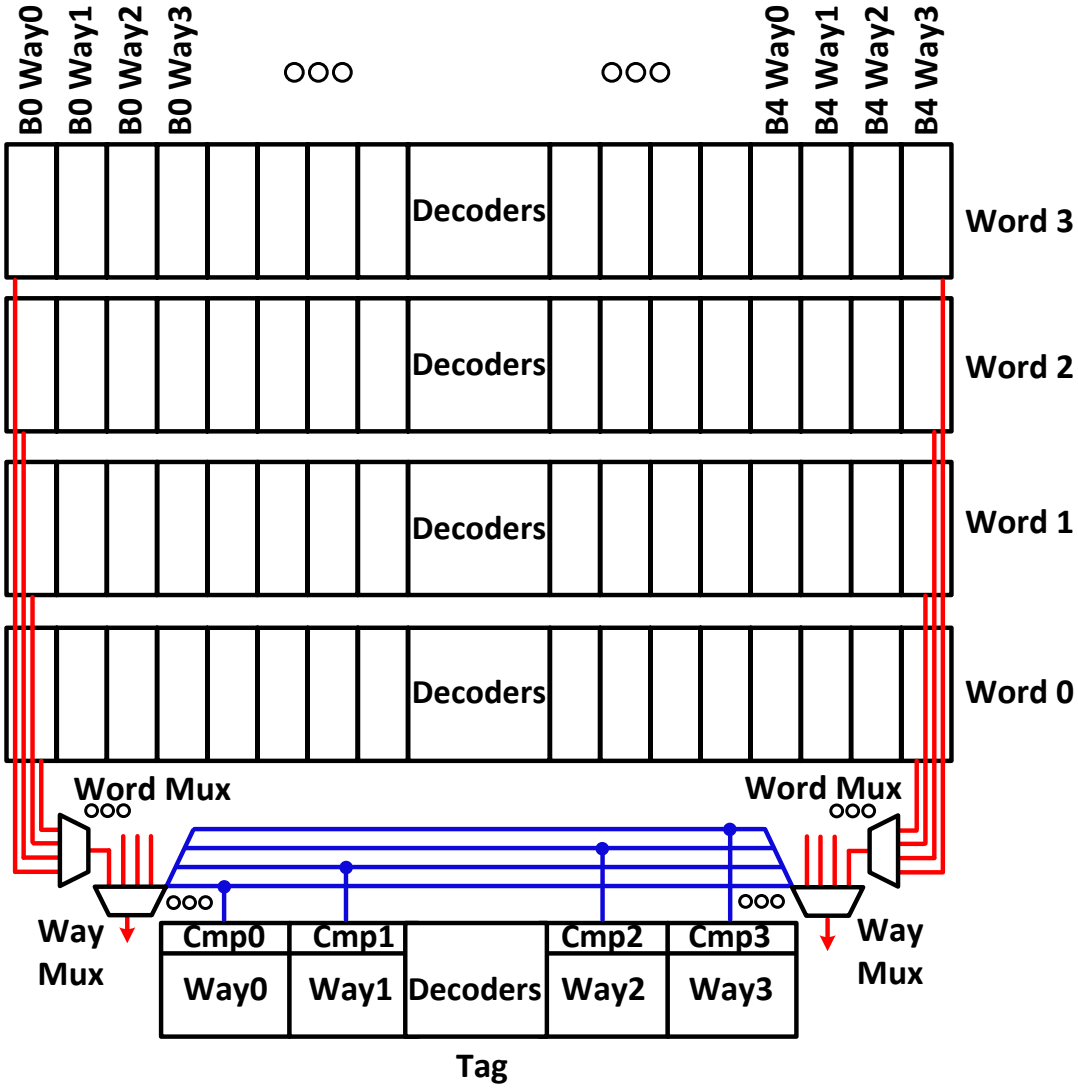
- **The data sub-bank has 16 entries, each 128-bits**
  - **Organized as 32-bits words**
  - **Cache is 4-way set-associative**
  - **Each word belongs to a different set**
  - **Each of the 16 bytes can be written independently and at most 4 bytes are written simultaneously**



Cache Cluster

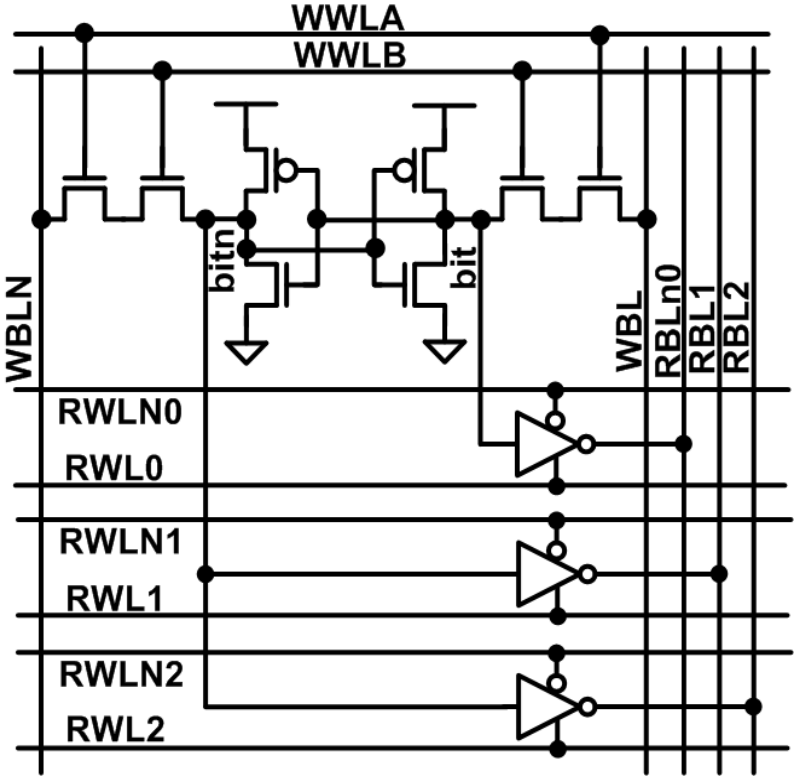
- **Cache cluster has 4 sub-arrays and a tag array**
  - **1k-byte of data and associated tag match, way select and word select circuitry**
  - **Data from each way is interleaved**
    - **Minimizes swizzling in the APR cluster routing for efficiency**

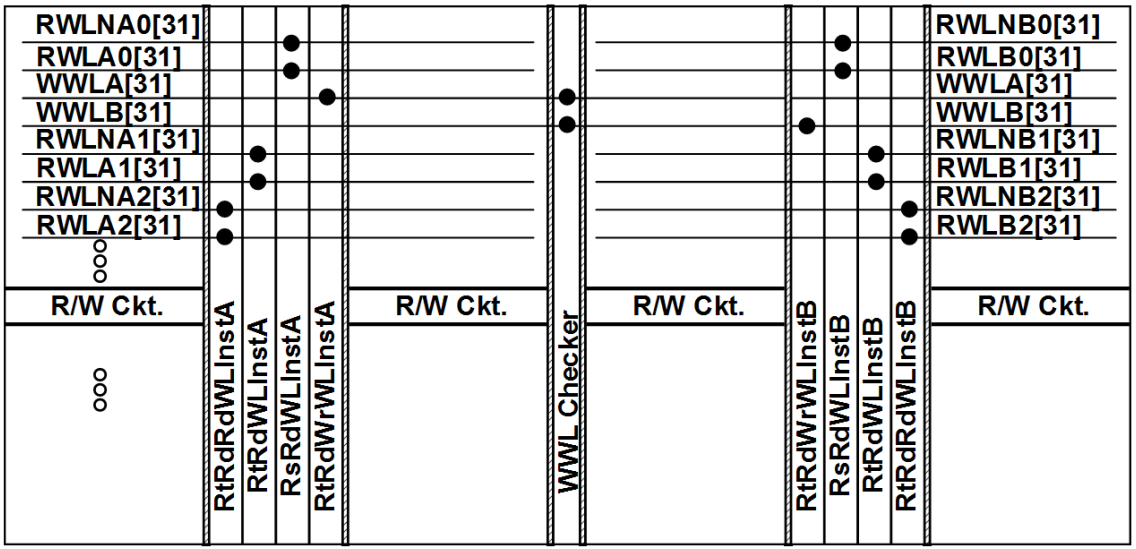


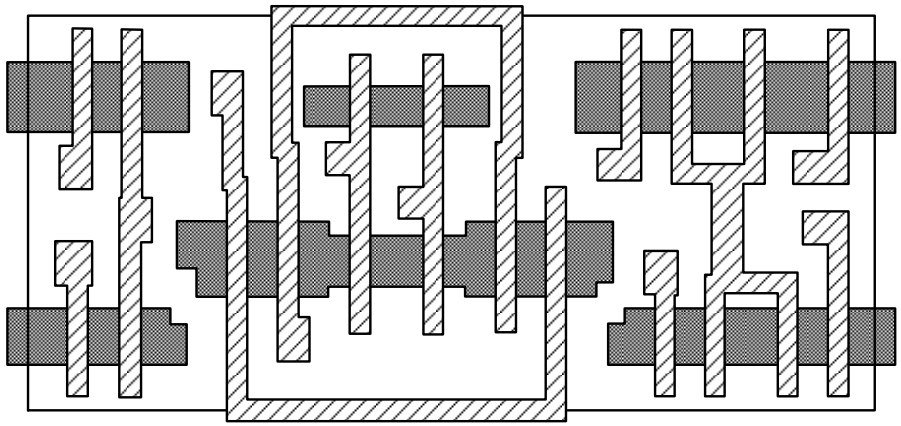


DMR Register File

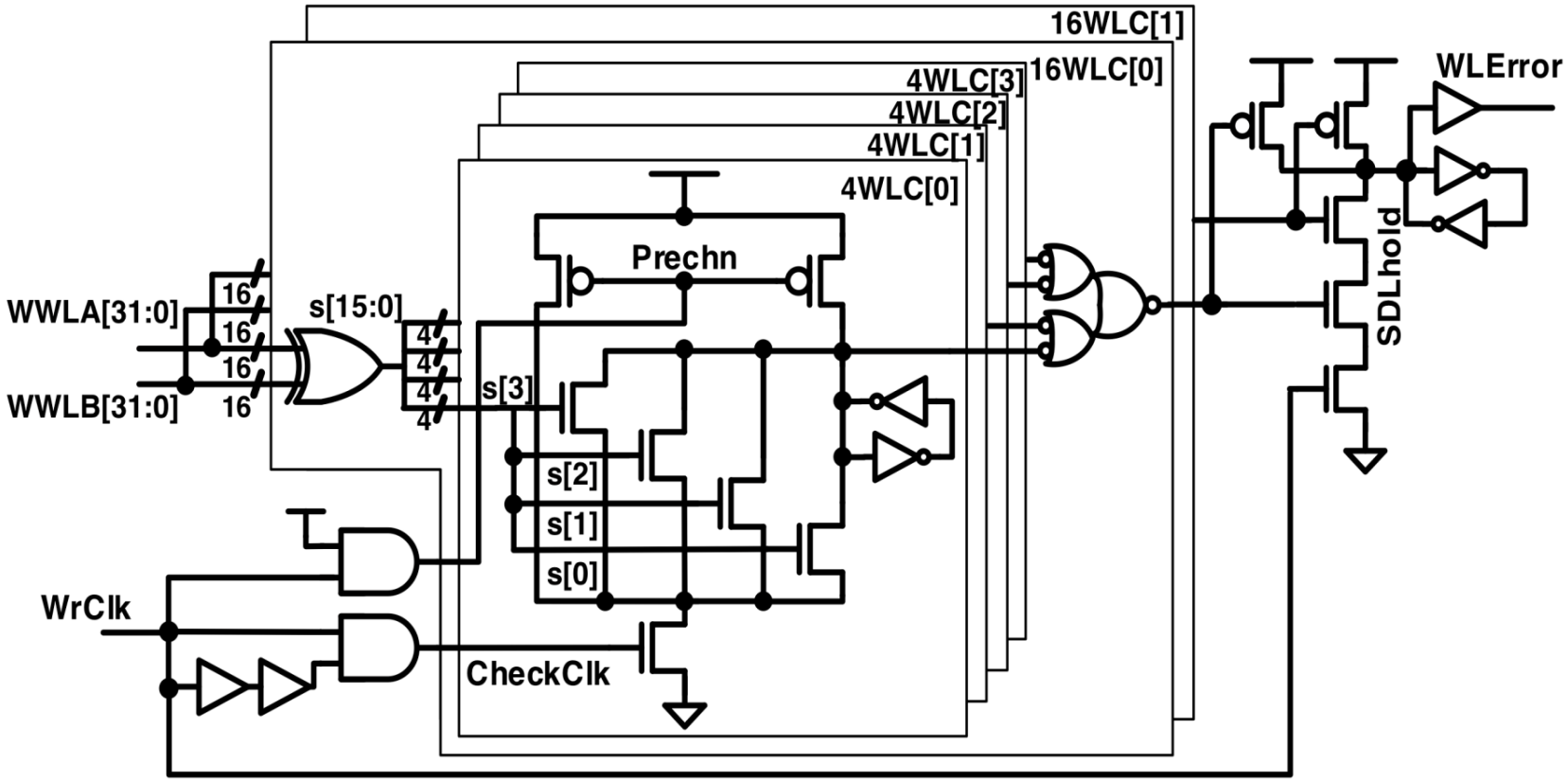
- **Same static RF read for low power and low voltage operation**
  - **Three read ports**
    - **Two for operands**
    - **Third for background scrubbing and saving old value before a store (required for added BURF instruction)**
  - **DMR WWLs prevent erroneous write**







Error Checking Circuits



- **RF WL mismatch checker (example)**
  - **One's catching domino circuits detect even transient mismatches**
  - **DMR WLs are compared in a timing window (CheckClk)**
    - **Delay for them to settle and avoid timing variability issues**
  - **Output latched for pseudo-static operation**

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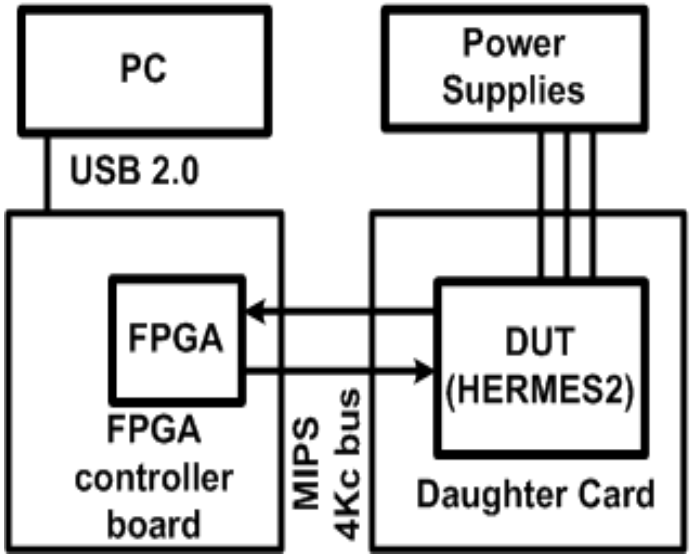
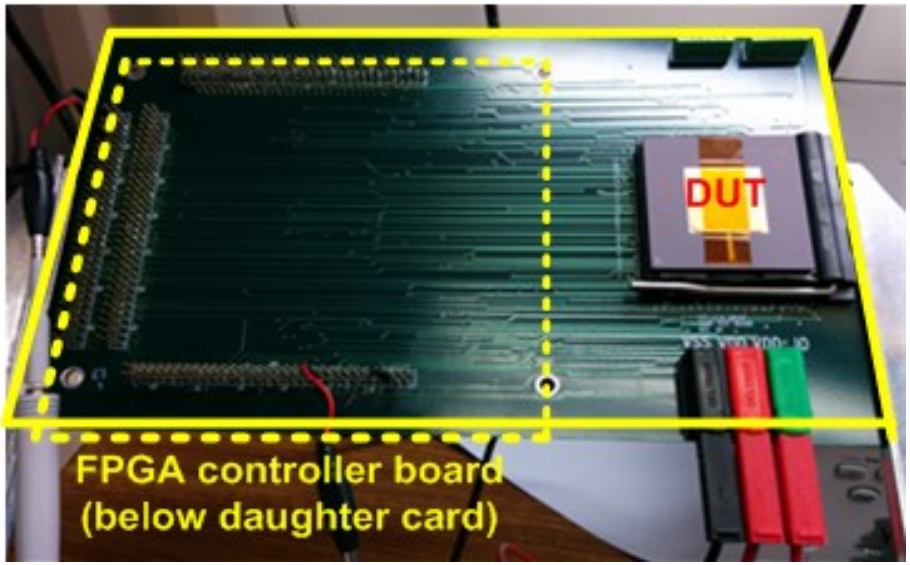
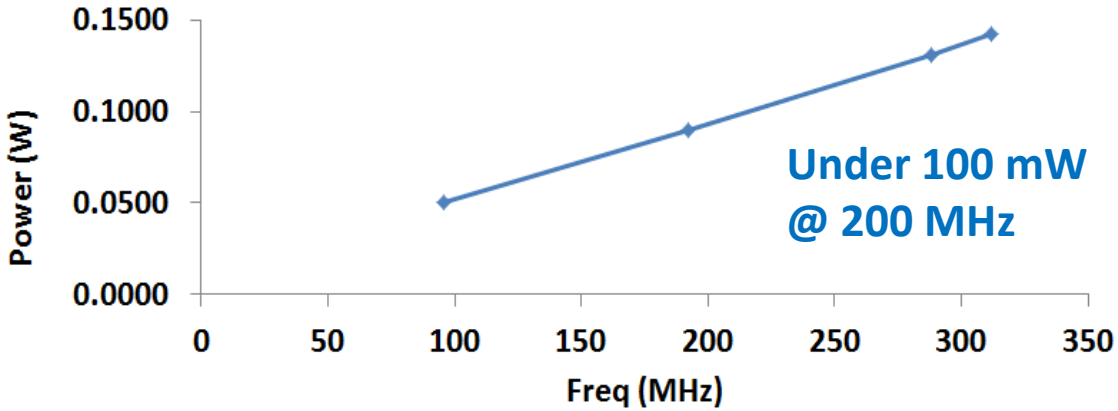
HERMES2 Silicon Results





- **Implemented on a foundry *low standby power* 90-nm process**
- **312 MHz at 1.2 V V_{DD}**
  - **143 mW power dissipation running MAC/cache tests (best RHBD power/performance published)**
    - **Fully cached operation (no I/O) so the machine is at 100% activity**



  - **330 MHz at 1.4 V V_{DD}**
  - **Minimum operating V_{DD} = 650 mV (Lowest RHBD processor V_{DD})**
    - **Limited by standard foundry I/O—should be operable below 300 mV**

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Silicon Validation

- **HERMES instructions allow software error injection**
  - **Allows:**
    - **Validation of the hardware for soft-errors without beam time**
    - **Provably correct software error correction response**

```
  RF Parity checker error injection test:
MTC0 $0, $22 // Turn Error Checkers off
RFTW $5      // Write $5A and $5B with different data
MTC0 $30, $22    // Turn Error Checkers on
// RF Parity checker fires, SEE exception address
// Error log 2 written with RF Parity error
```

CLK	Controls	AValid	Address	Data in	Write	Data out
00000	0000111100000110	1	1fc001a0	00000000	0	00000000
00001	0000111100000110	1	1fc001a0	00000000	0	00000000
00002	0000111100000110	1	1fc001a4	00000000	0	00000000
00014	0000111110000110	1	1fc00000	3c000001	0	00000000
00021	0000111110000110	1	1fc00004	1c000011	0	00000000
00028	0000111110000110	1	1fc00008	00000000	0	00000000
03115	1000111100000110	1	000006c4	4081b007	0	11110000
03116	1000111100000110	1	000006c8	00a52826	0	11110000
03127	0000111100000110	1	1fc00000	3c000001	0	11110000
03134	0000111100000110	1	1fc00004	1c000011	0	11110000
03141	0000111100000110	1	1fc00008	00000000	0	11110000
...						
03701	0000111100000101	1	00000000	00000000	1	ffffffff
03702	0000111100000110	1	1fc00188	ac230004	0	ffffffff
03709	0000111100000101	1	1fc0f000	00000000	1	00000000
03710	0000111100000110	1	1fc0018c	ac230008	0	00000000
03717	0000111100000101	1	1fc0f004	00000000	1	04000000

```
  RF dual redundant wordline error injection test:
RFTW $15, $14
// Write $14B and $15A simultaneously
// RF dual redundant wordline error checker fires
// Error log 1 written with RF wordline error
```

CLK	Controls	AValid	Address	Data in	Write	Data out
...						
00200	1010111100000110	1	000004ac	4084b005	0	bff01000
00204	1100111100000110	1	000004b0	7000000d	0	bff01000
00205	1000111100000110	1	000004b4	0000000f	0	bff01000
00206	1000111100000110	1	000004b8	0000000f	0	bff01000
00210	0000111100000110	1	1fc00000	3c000001	0	bff01000
00214	0000111100000110	1	1fc00004	1c00001b	0	bff01000
...						
01910	0000111100000101	1	1ff0127c	00000000	1	04000000

SE exception goes to general exception address 0x1fc0000

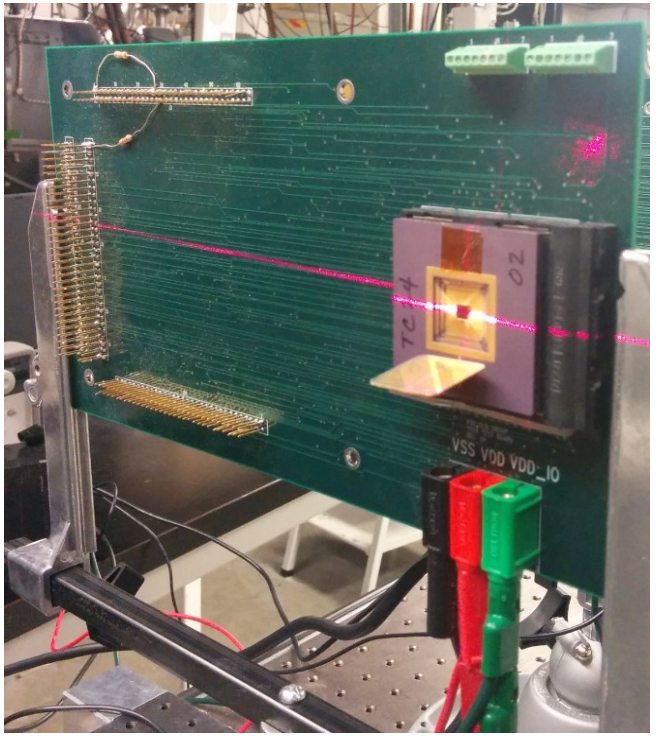
(Note same cause but in different registers)

Outline

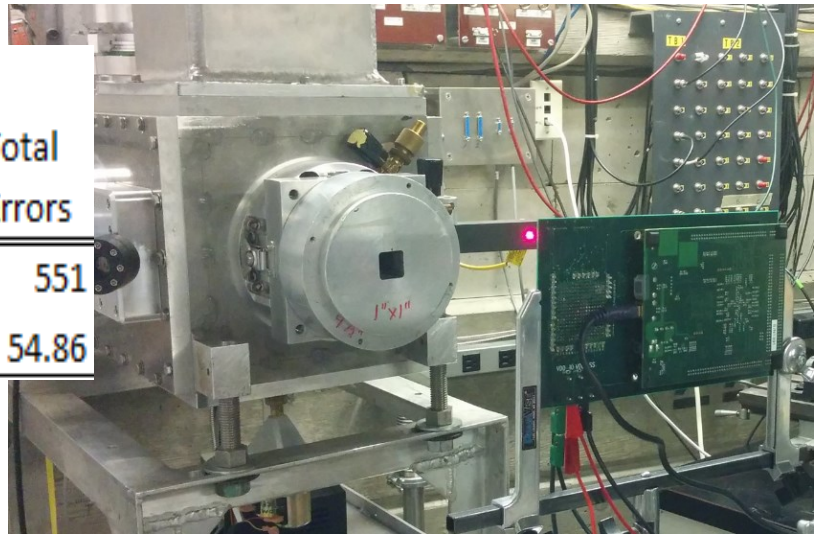
- Motivation
- Highly Efficient Radiation-hardened Microprocessor Enabling Spacecraft (HERMES2) microarchitecture
- Features (added instructions and registers) for software based soft-error recovery and reporting
- Circuits and Physical Design
- Experimental results
- Silicon validation and software based program validation on hardware
- **Proton Testing results**
- Summary

Proton Testing

- **UC Davis Crocker Labs cyclotron**
  - **63 MeV protons**
  - **1.3×10^7 protons/cm^2-sec flux (ave.)**
  - **1.004×10^{11} protons/cm^2 total fluence**
- **MAC/cache and MAC intensive programs**
- **509 SE exceptions taken**
  - **551 checker reported errors**
- **All perfectly corrected by handler with 100% return to program execution**
  - **No anomalous instruction or data fetches**



	MDU	RF Write back	RF Word line	IFU	IEU	RF Parity	DCU	Total Errors
Total by type:	5	104	0	25	180	8	229	551
Cross-section (µm^2)	0.50	10.35	0.00	2.49	17.92	0.80	22.80	54.86



- **Zero measured soft-error cross-section post correction!**

Summary

- **HERMES2 has:**
  - **No uncorrectable soft errors in 500+ events with proton testing to over 10^{11} protons/cm^2 fluence**
  - **312 MHz operation at spec 1.2 V V_{DD} dissipating 143 mW**
  - **Operable down to 650 mV V_{DD} for ultra low power operation**

- **Demonstrated efficacy of software controlled soft-error recovery**
  - **DMR speculative pipelines allow soft-errors to be "caught"**
  - **Errors cause an exception**
    - **Triggering error cleanup and reporting handler**
  - **Software allows detailed reporting to determine *error root causes* (not just the final manifestation of the error)**
  - **New instructions enable state repair and reporting, as well as hardware validation and provably correct software recovery**

- **Automated RHBD design approaches and limited custom circuits allows fast porting to new fabrication processes**

Thank you for your attention

This work was funded by

Questions?