Dynamic and Leakage Power Reduction of ASICs Using Configurable Threshold Logic Gates

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Motivation

- **Nearly three decades of R&D effort into reducing power of digital CMOS logic**

  - **Dynamic Power**
    - **Voltage Scaling**
    - **Activity Reduction**
    - **Logic synthesis**
    - **Technology mapping**
    - **Retiming**
  - **Leakage Power**
    - **Multiple Vdd**
    - **Multiple Vt**
    - **Adaptive Body Bias**
    - **Transistor Stacking**
    - **Power Gating**

- **Everything has been tried, and little left to do**
- **This work explores an alternate way to compute logic functions in order to reduce power**

What Is This About?

1. **A new approach to digital system design**
   - **Significant reduction in dynamic/leakage power**
   - **Reduction in area**
   - **Without performance loss**

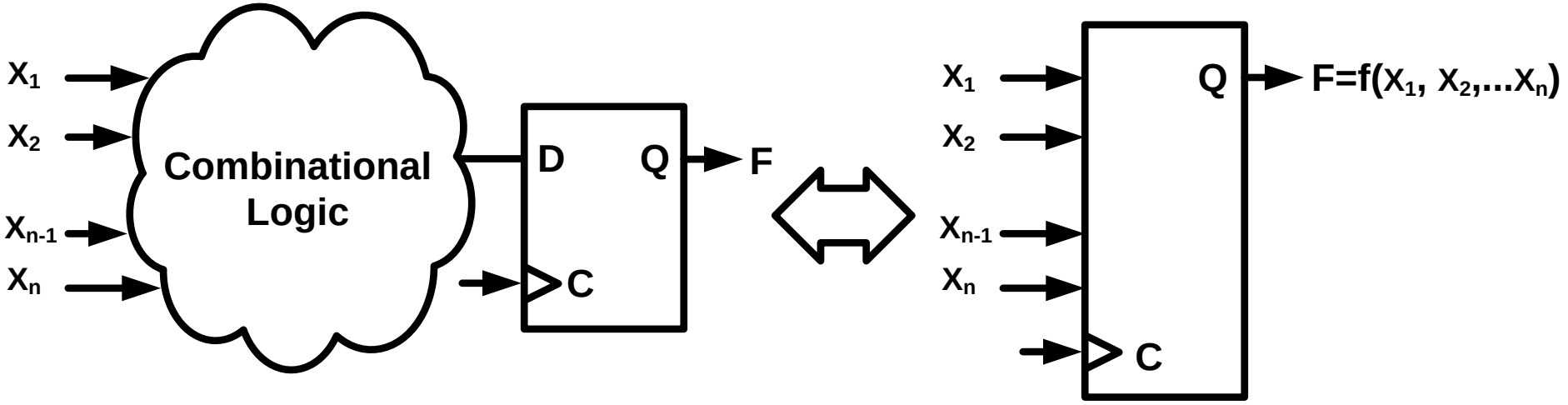
2. **Seamless integration with existing commercial design methodology**

Outline

1. *Motivation*
2. **High level abstract**
3. **Implementation results**
4. **Technical details**
5. **Conclusion**

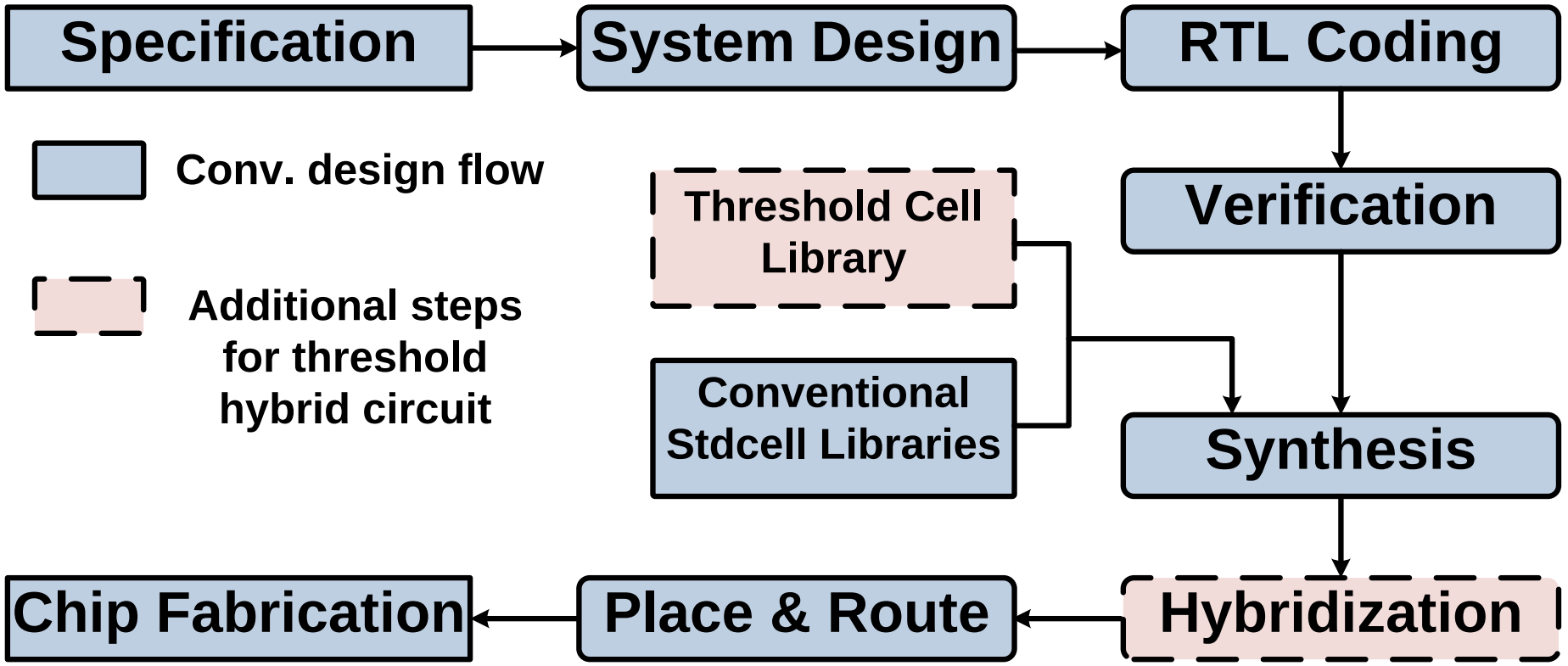
New Approach to Logic Synthesis

- **A new set of logic primitives**
  - **Multi-input edge triggered threshold flipflop**
- **Algorithm that replace logic cones + DFF with threshold flipflops (Hybridization)**
- **Conventional place and route tools support**

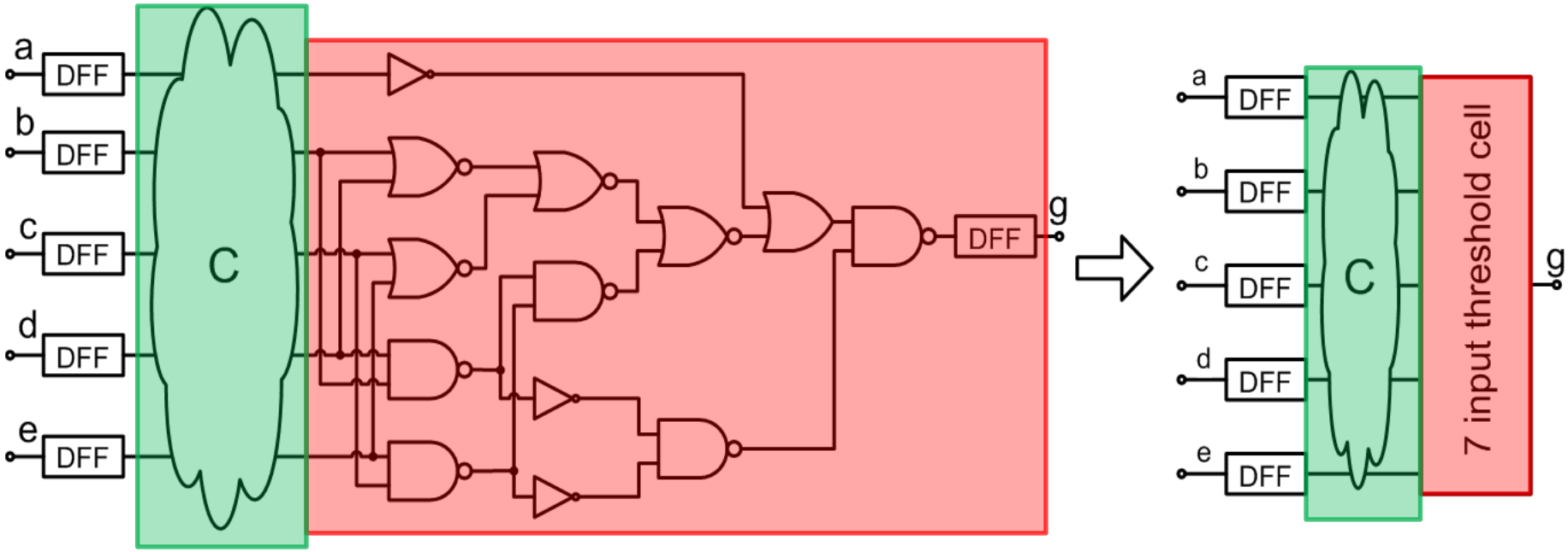


Threshold flipflop

Automated Design Flow



Technology Mapping (Hybridization)



In the absence of C

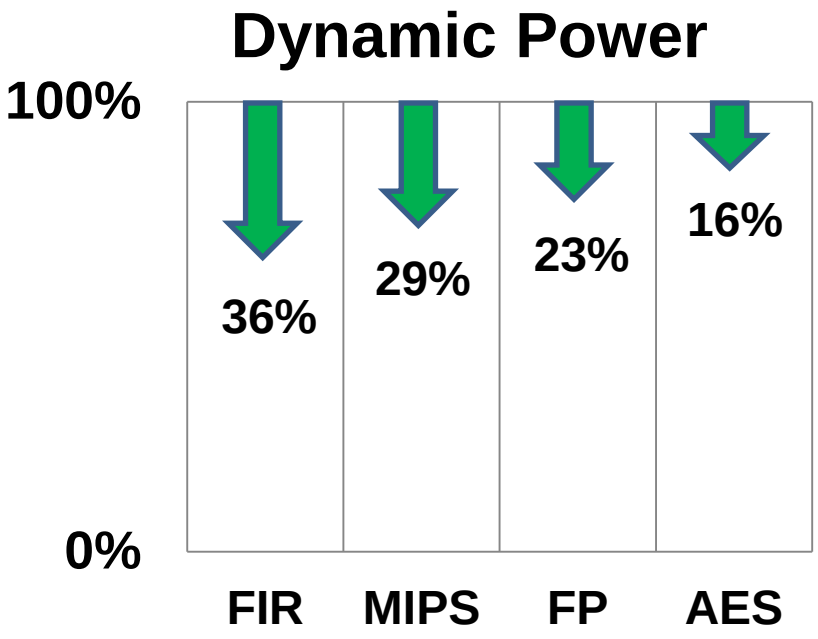
Parameter	Conventional	Hybrid	Improvement
Delay (ps)	515	276	49%
Area (μm^2)	54	33	38%
Energy (fJ)	63	45.6	27%
Leakage (nW)	5.8	1.8	70%
Total input cap (fF)	77.9	56.1	28%

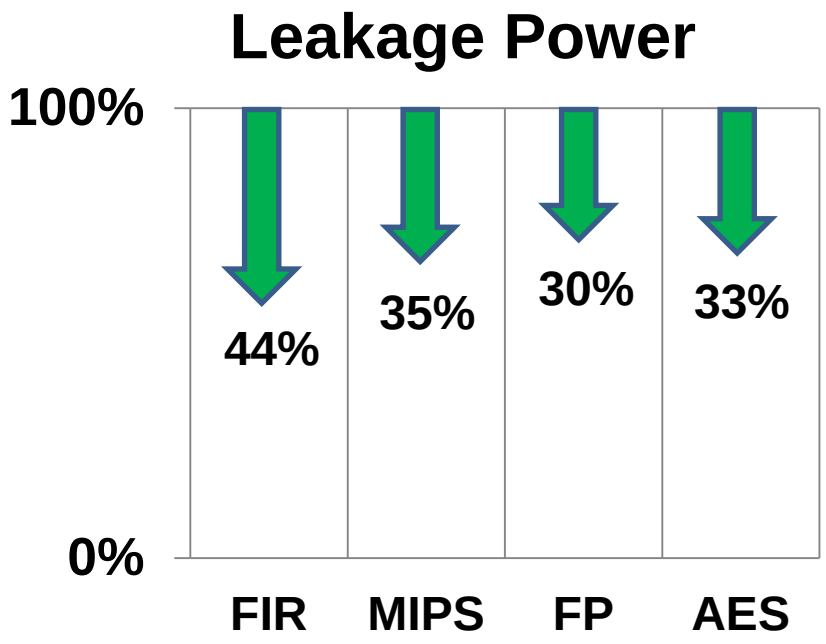
Post Layout Simulations

- 28 bit FIR Filter
- 32-bit MIPS
- 64-bit Float Point Multiplier
- 128-bit AES crypto-chip

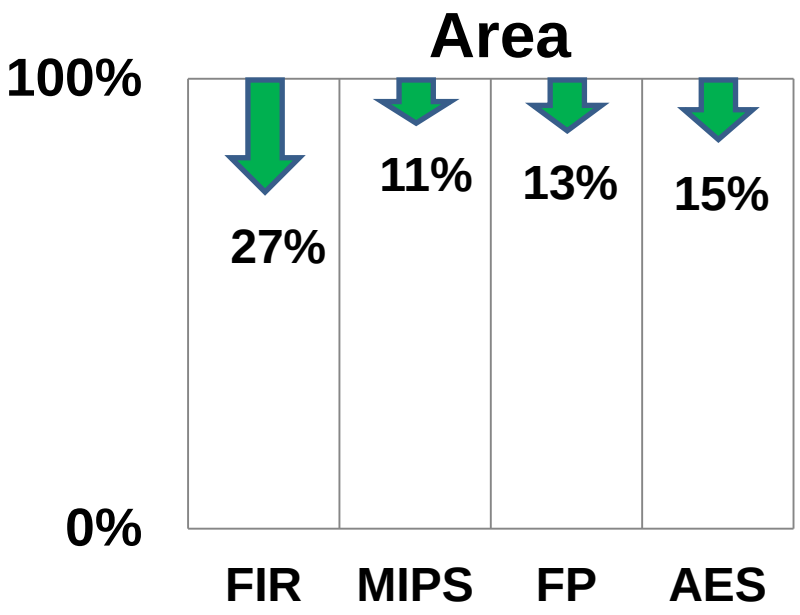
Identical Function
Same CLK Frequency

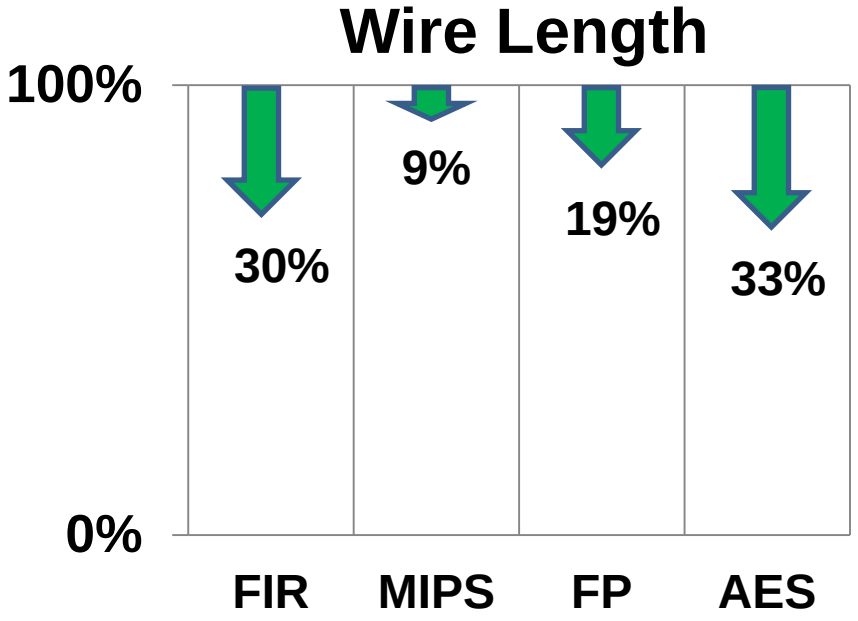
Normalized to conventional design

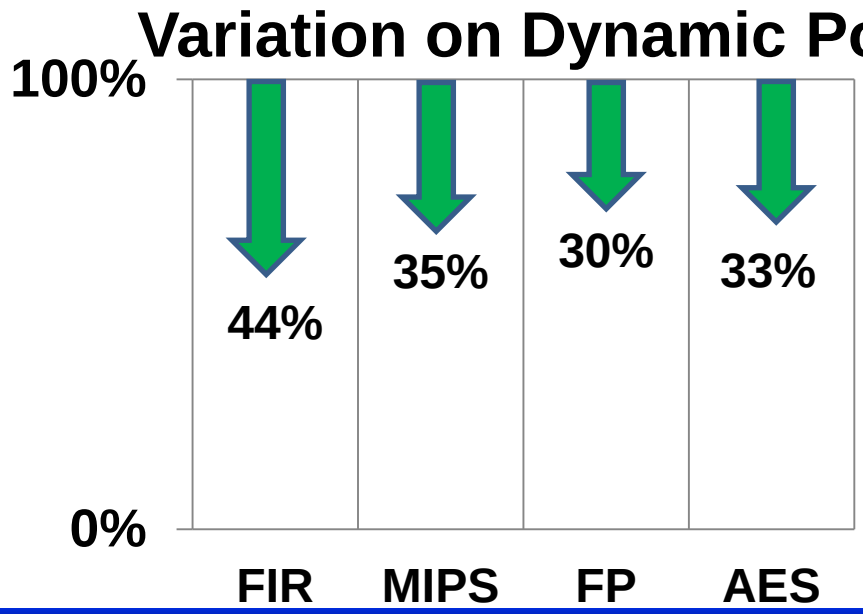




Post Layout Simulations

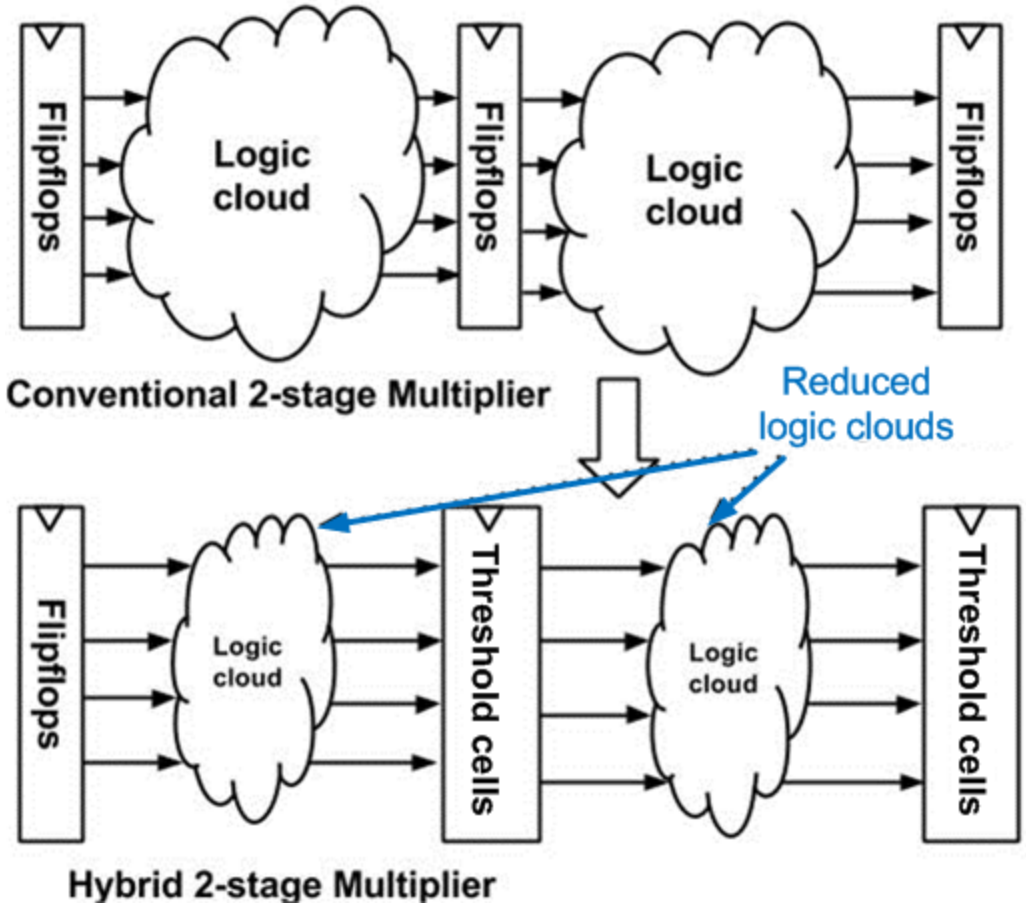






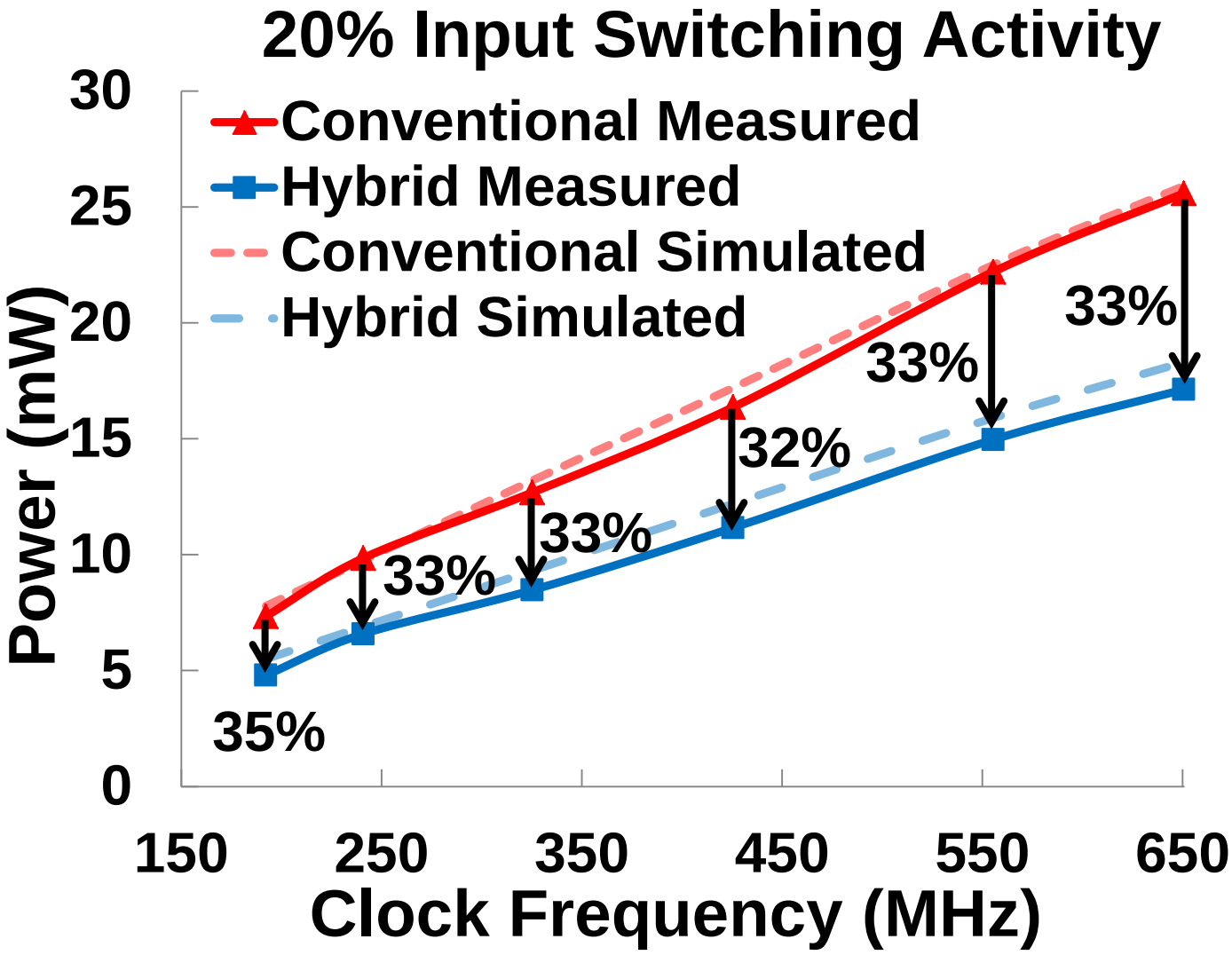
Prototype Circuit Fabrication

- **32-bit Two stage Wallace Tree multiplier**
  - **Fabricated in 65nm LP technology**

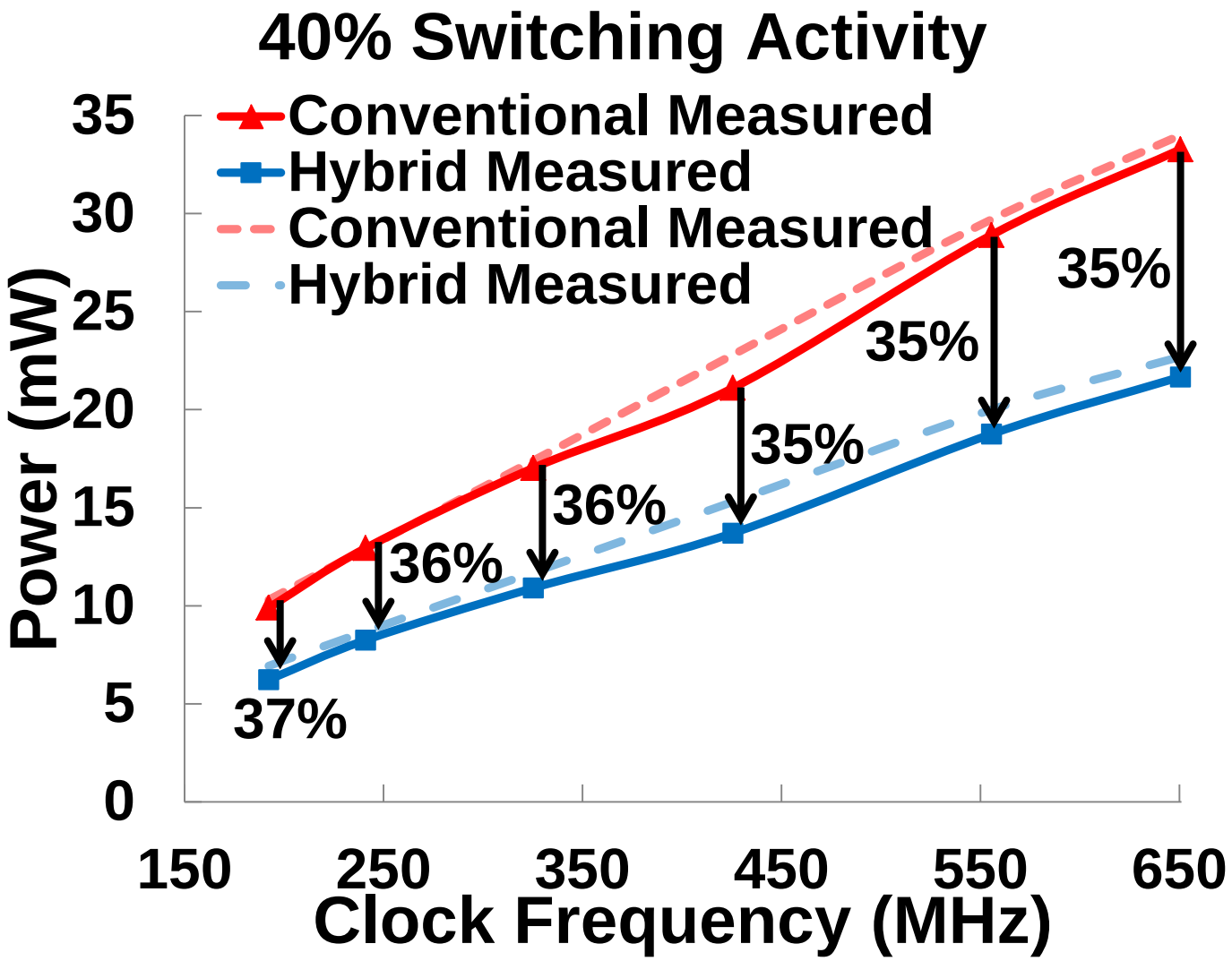


Threshold flipflop type	Count
1 input	55
3 input	69
5 input	114
7 input	20
9 input	9

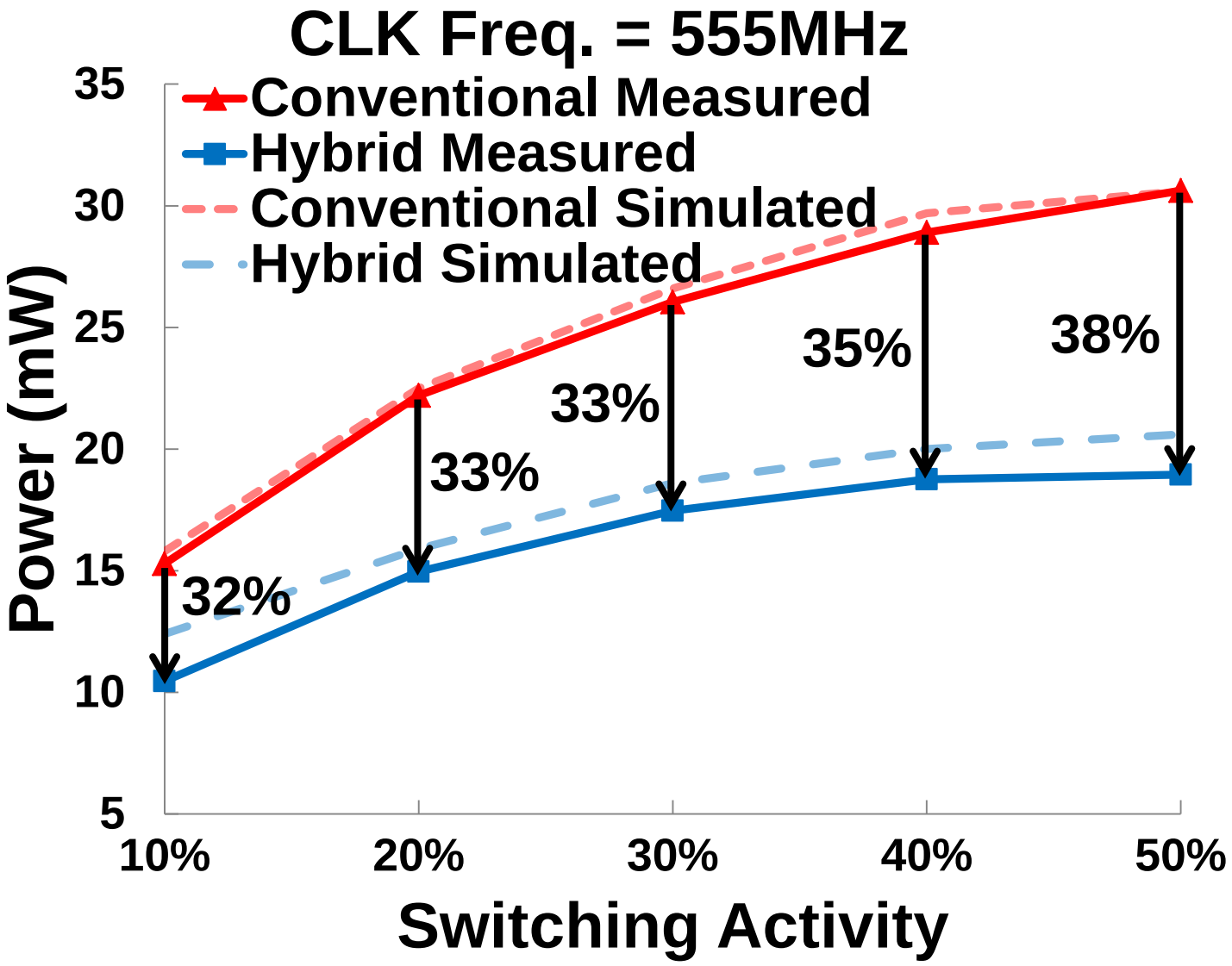
Dynamic Power vs Frequency



Dynamic Power vs Frequency

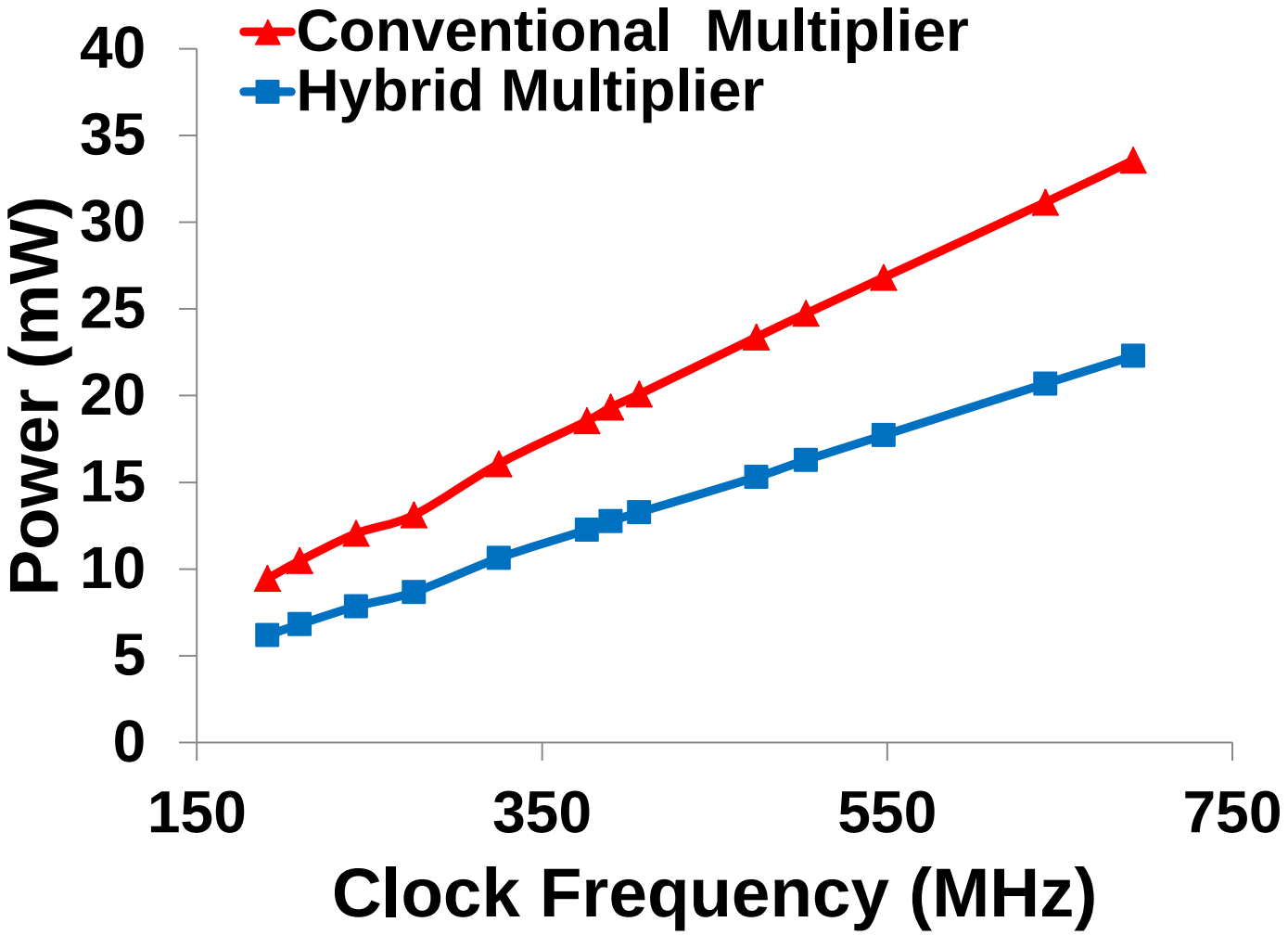


Power vs Switching Activity



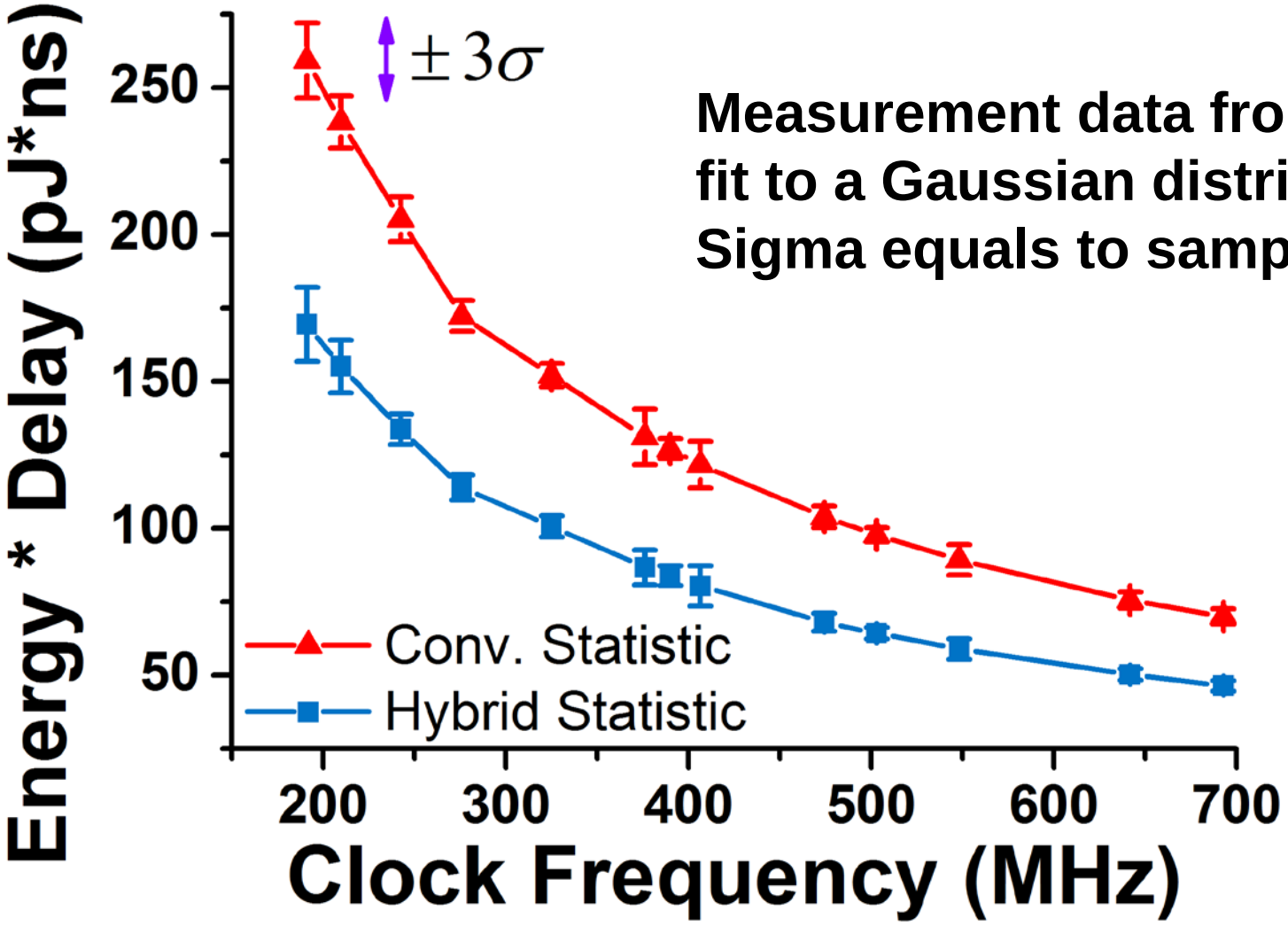
Average Power (cross 19 dies)

- **30% input Switching Activity. Consistent power improvement across all dies at different frequencies**



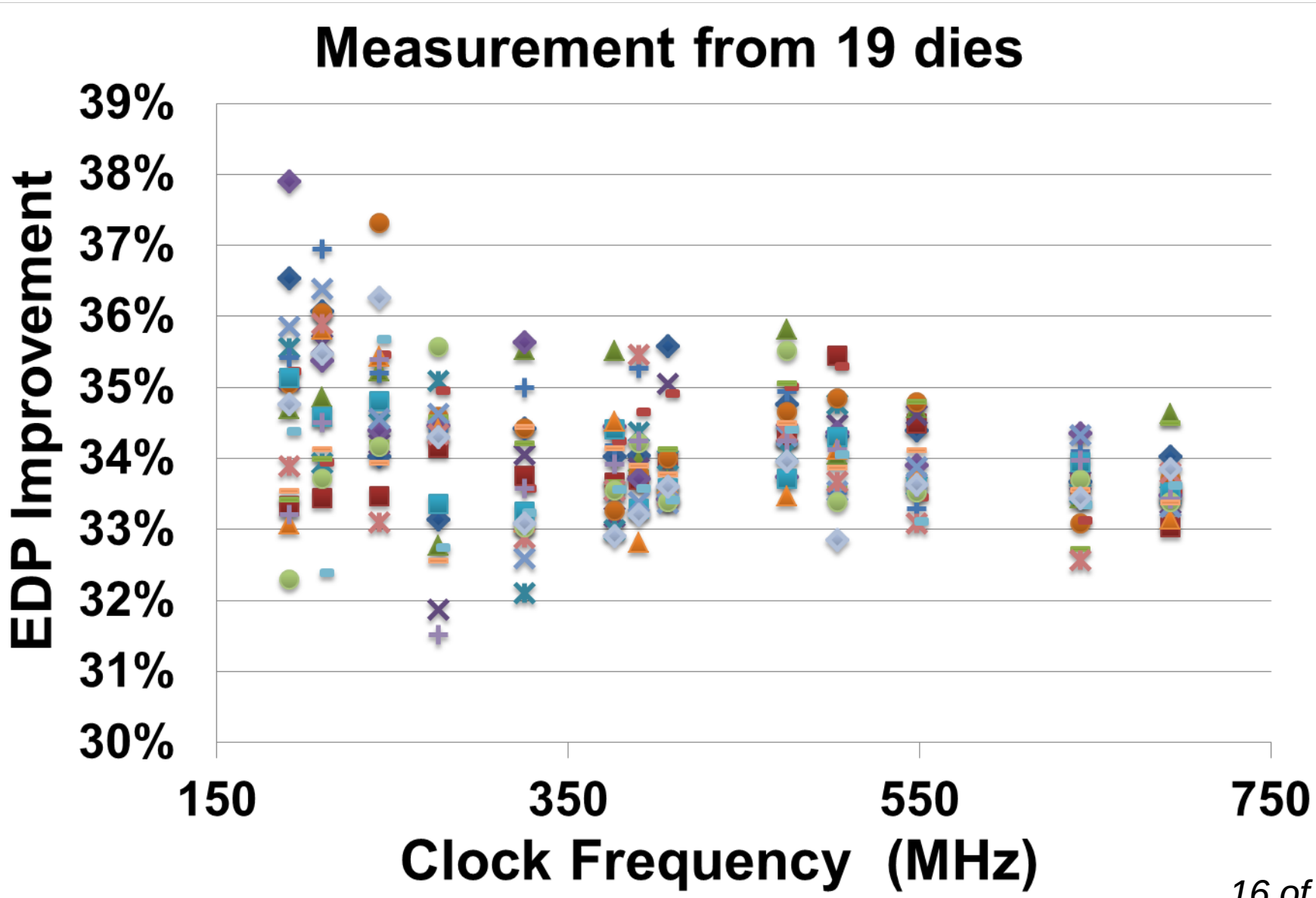
Energy Delay Product

- **The energy delay product improvement is larger than 6 sigma**



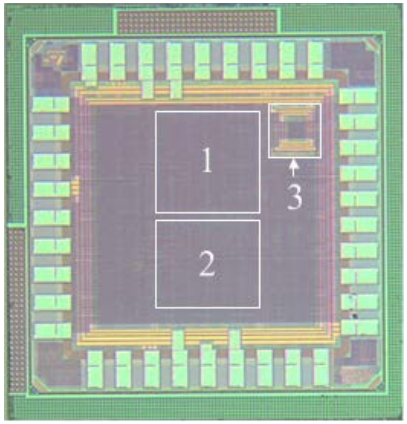
Measurement data from 19 dies fit to a Gaussian distribution. Sigma equals to sample variance

EDP Improvement Distribution



Chip Measurement Summary

Specification	Conv.	Hybrid	Improvement
Supply (V)	1.2		-
Area (μm²)	41814	31680	24%
Leakage (μW)	8.1	4.1	49%
Wirelength (μm)	160160	87243	45%
# Std. Cells	5546	4003	28%
Clock Frequency	642MHz, 30% switching activity		
Power (mW)	31.1	20.7	34%
Average EDP (pJ·ns)	75.6	50.2	34%



1 Conventional CMOS multiplier

2 Fully automated hybrid multiplier

3 Clock generator

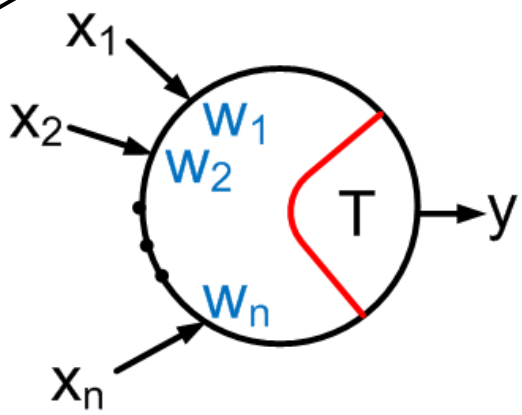
Technical Details -- Function

- **Threshold function**
  - **A subset of Boolean function**
  - **Computes by comparing sum weighted inputs with threshold**

Integer weights **Boolean variables** **Integer Threshold**

$$y = \begin{cases} 1 & \text{if } \sum_{i=1}^{n} w_i x_i \geq T \\ 0 & \text{otherwise} \end{cases}$$

$$y = [w_1, w_2, \ldots, w_n; T]$$

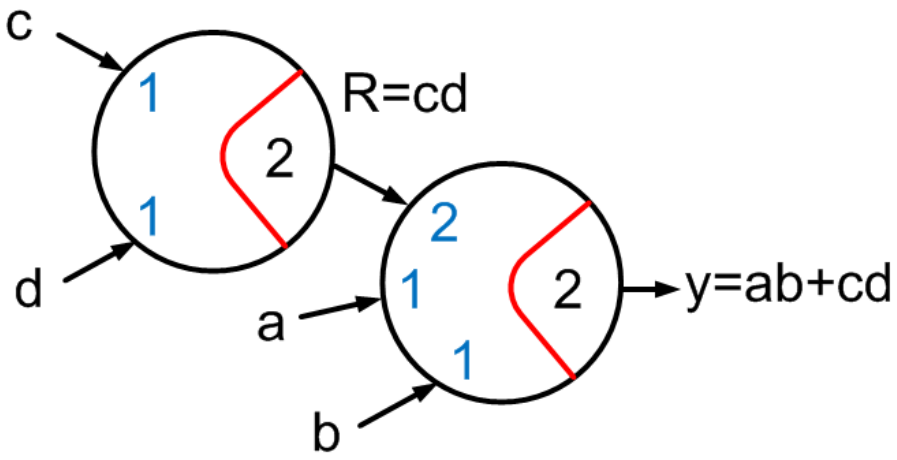


Technical Details -- Examples

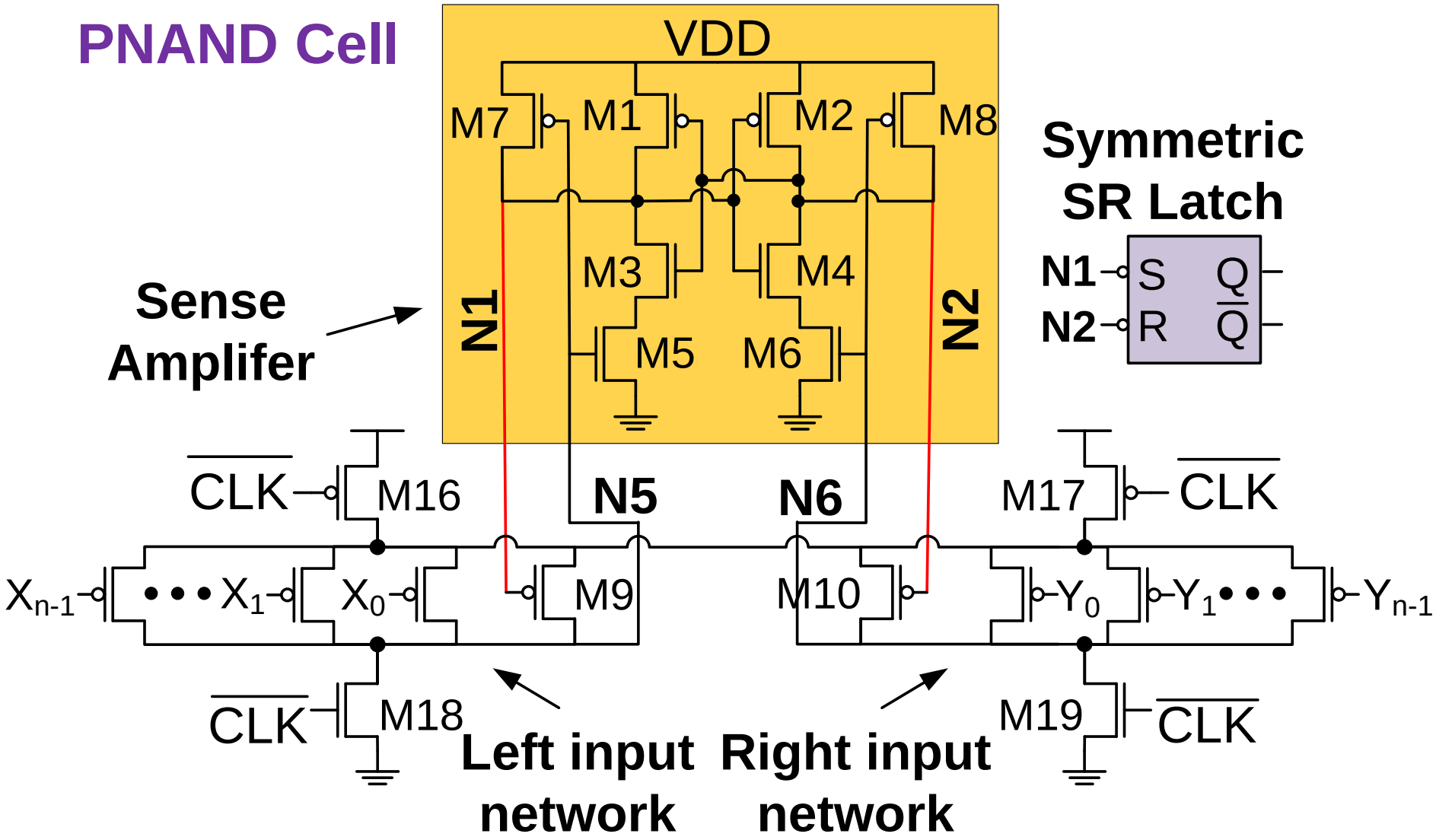
- $y = a + bc \Leftrightarrow y = \begin{cases} 1 & 2a+b+c \geq 2 \\ 0 & 2a+b+c < 2 \end{cases}$

y is a threshold function: $y = [2, 1, 1; 2]$

- **$y = ab + cd$ is not a threshold function**



Technical Details -- Circuit



Technical Details -- Library

- **Characterize the PNAND-n library for n=1, 3, 5, 7, 9**
  - **Clocked sequential element**
  - **Setup/hold times, C to Q delay, power**
  - **72 base functions + all NPN equivalents**

PNAND cell	# of functions	Boolean function example
PNAND-1	1	a
PNAND-3	3	ab+ac+bc
PNAND-5	8	abc+abd+acd+bcd
PNAND-7	18	…
PNAND-9	42	…

Technical Details -- Mapping

- $\mathbf{y = a + bc \Leftrightarrow y = [2, 1, 1; 2]}$
- $2a + b + c \geq 2$ **Equality is not allowed**

1. $\Rightarrow 4a + 2b + 2c > 3$ ***PNAND-8***

2. $\Rightarrow \quad a + 2b + 2c > 3(1 - a)$ ***PNAND-5***

3. $\Rightarrow \quad 3a + b + c > (1 - a) + (1 - b) + (1 - c)$

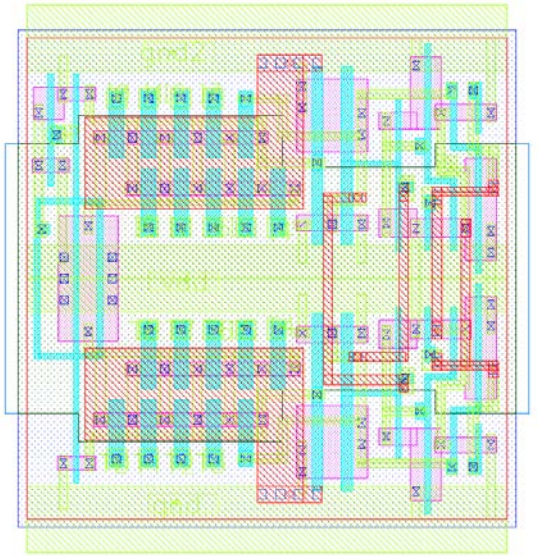
PNAND-5

There is a optimal function mapping that:

- ✓ **Minimum # of inputs**
- ✓ **Eliminate race condition**
- ✓ **Minimum delay & power**

Technical Details -- Robustness

- **Optimal Signal Mapping**
  - **Eliminates contention**
  - **Maximize performance**
- **Analog layout techniques**
  - **Parasitic matching**
  - **Noise shielding**



- **Monte Carlo simulation -- cell yield**
  - **Global and local variations in Vt and β**
  - **PVT corners (global)**
  - **Foundry data (local)**
  - **100,000 simulations (1.2V, -40C)**
    - **Zero error**

Conclusion

1. New approach to reducing power of digital CMOS without sacrificing performance or area
2. Seamlessly integrated into existing design flow
3. Simulation and measurement on 65nm test chip demonstrated
    1. ~ 35% less dynamic power
    2. ~ 50% less leakage
    3. ~ 25% smaller area

All at same clock frequency

On-going Work:

1. Integration with emerging devices for low power, high performance, and nonvolatile computing
2. New clocking strategy
3. Asynchronous design