A Highly Linear Dual-Band Mixed-Mode Polar Power Amplifier in CMOS with An Ultra-Compact Output Network

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Outline

- Introduction
- Circuit Schematic and Simulation Results
- Measurement Results
- Conclusion

Introduction

Modern wireless systems often need ***multi-band*** operations to simultaneously support different communication standards.

Spectrum-efficient modulations (e.g., 16 QAM and 64 QAM) in modern wireless systems often result in large peak-to-average power ratios (PAPRs) for the transmitted signals, which requires ***highly linear power amplifier***.

IEEE 802.11

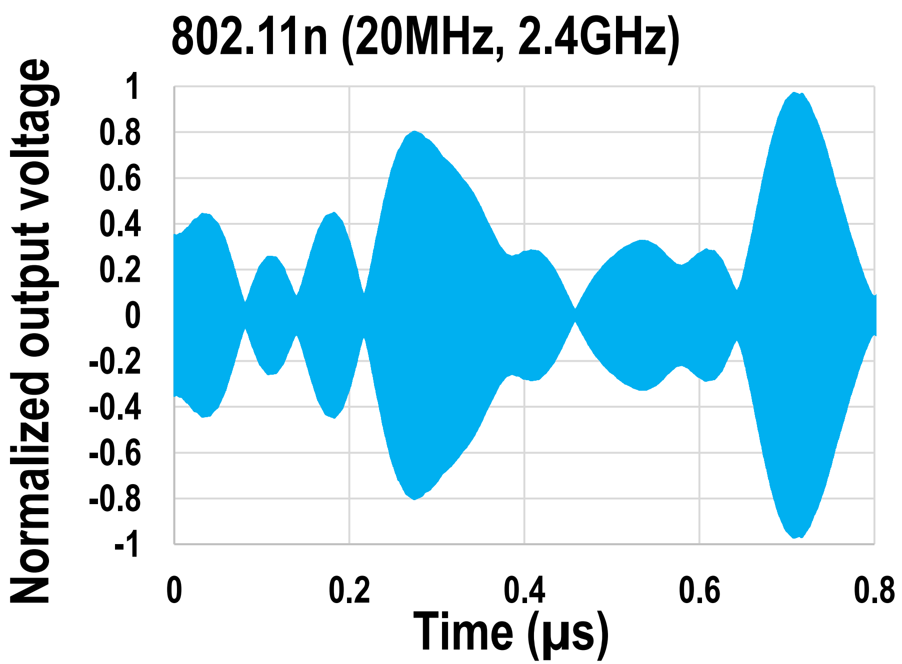
2.4GHz (802.11b/g/n)

3.65GHz (802.11y)

4.9GHz (802.11y)

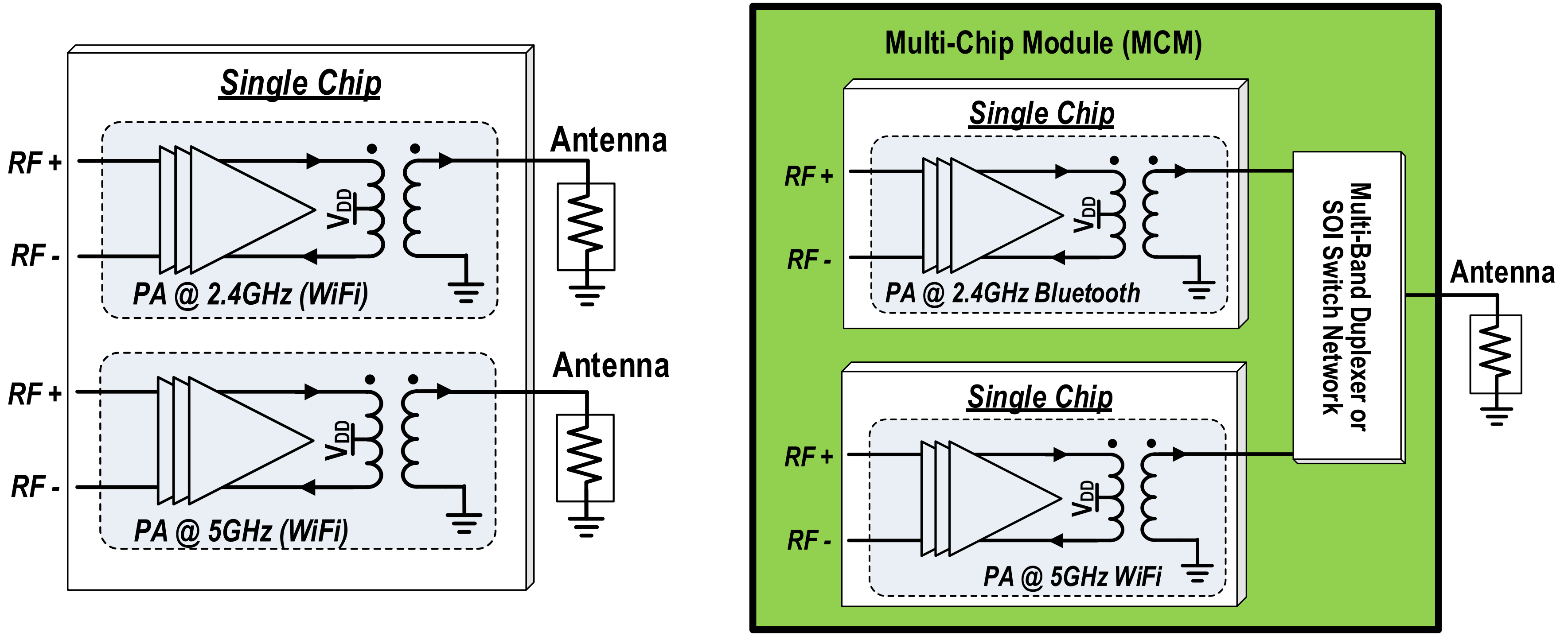
5GHz (802.11a/h/j/n/ac)

5.9GHz (802.11p)



Introduction

A common multi-band PA solution is to directly assemble several single-band PAs either in a single chip or on a multi-chip module (MCM)

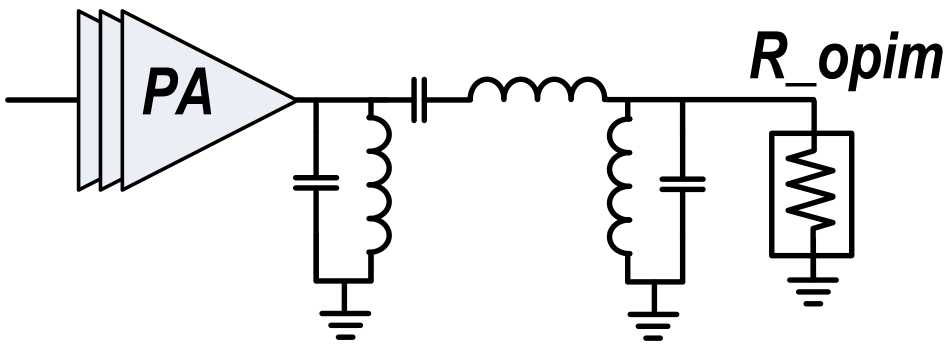


• Large chip/module area, dedicated antenna interface, and complicated packaging

→ **increased cost, reliability, and nonlinearity concerns.**

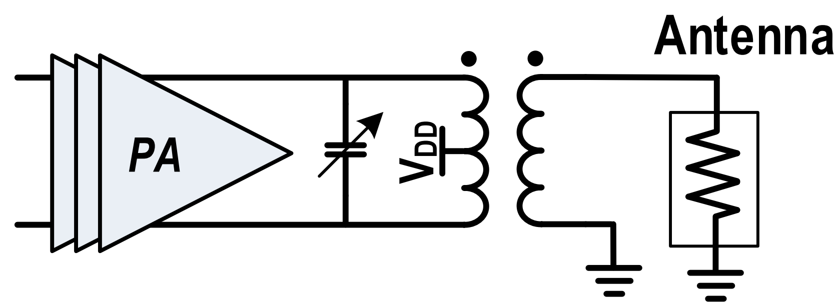
Introduction

On the other hand, high-order passive networks and/or tunable passives can be utilized to achieve multi-band impedance matching and power combining for RF PAs



6th order passive network
3rd order band-pass filter

[H. Wang ISSCC 2010]



Tunable element

[W. Neo JSSC 2006]

• High-order network requires **multiple inductors → large chip area and high passive loss.**

• Tunable elements such as varactor and switch capacitor bank → **nonlinearity and reliability concerns as well as extra passive loss.**

• 2nd or 3rd harmonics are often located in-band and cannot be suppressed using off-chip filters → **on-chip harmonic leakage cancellations are required.**

Introduction

In order to address these challenges, we propose digital polar power amplifier in CMOS with an ultra-compact output passive network and mixed-mode linearization techniques.

- The class D^{-1} digital polar PA architecture is employed for high power >26dBm and simple output passive network.

- Output passive network is implemented within one transformer foot print and provides optimum load pull impedance matching at two different frequencies without tunable elements.

- On-chip 2^{nd} harmonic leakage cancellation is achieved at the output passive network.

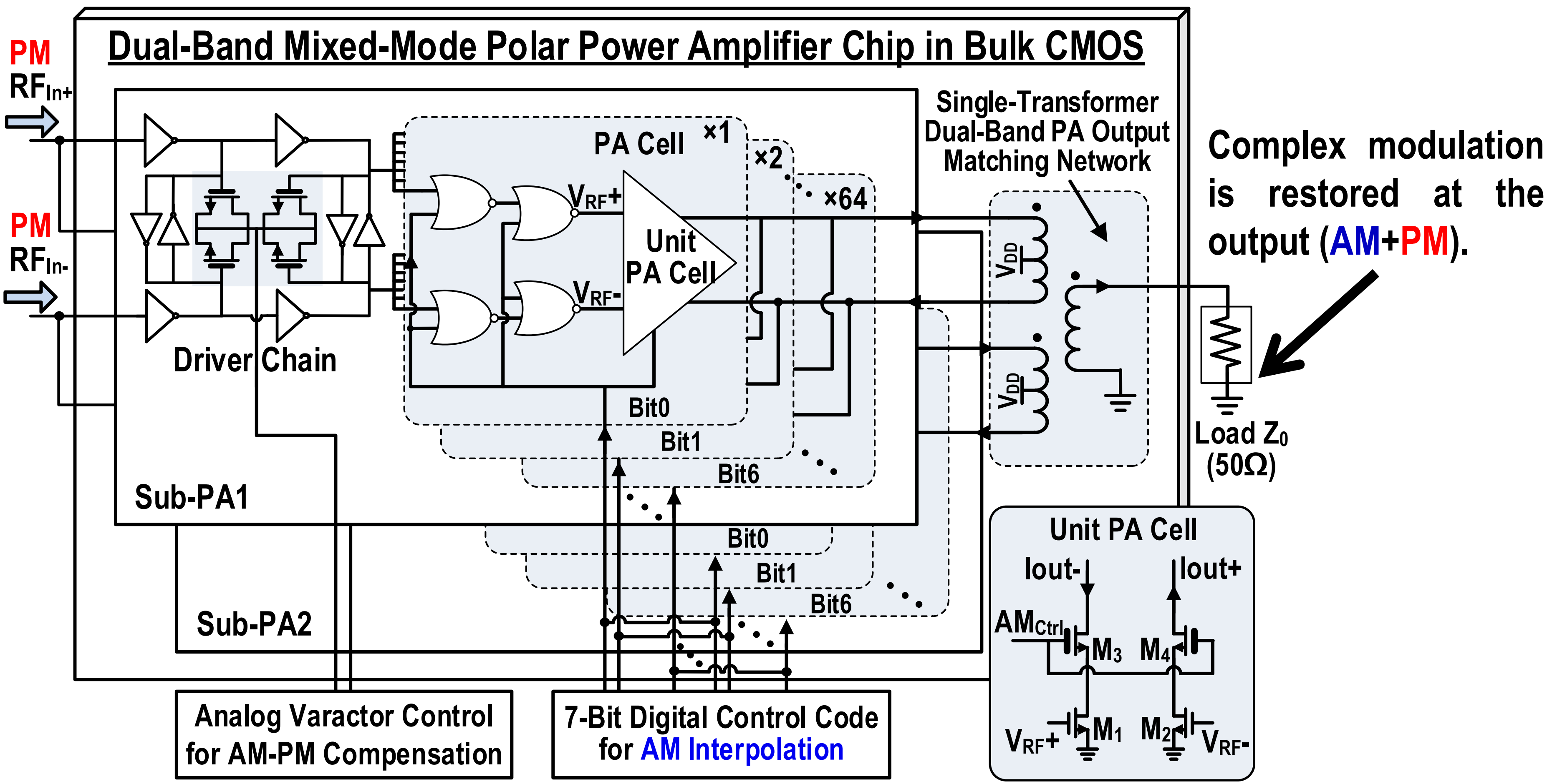
- The AM-AM and AM-PM distortions are compensated by mixed-mode linearization techniques.

Outline

- Introduction
- **Circuit Schematic and Simulation Results**
- Measurement Results
- Conclusion

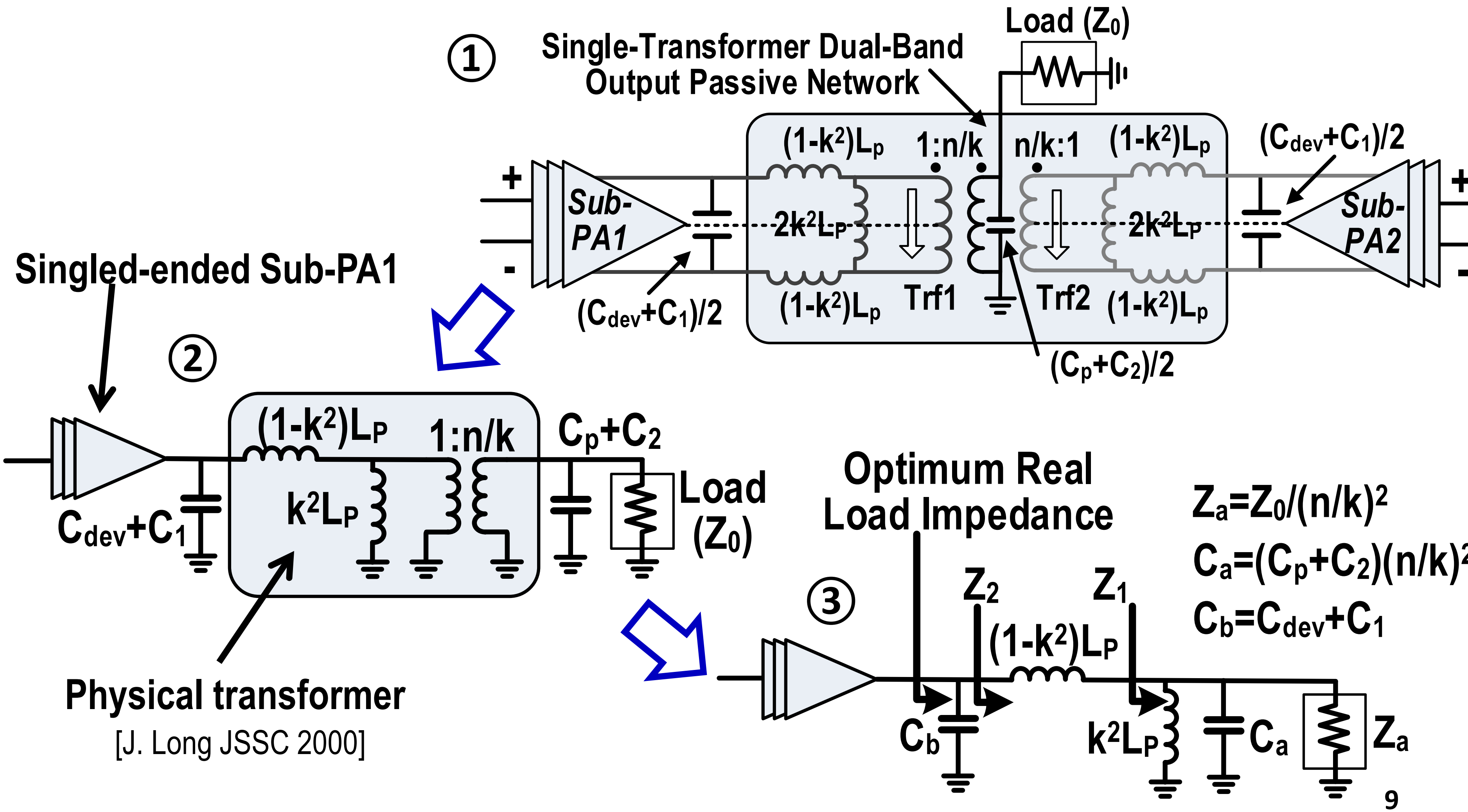
Circuit Schematic

A Highly Linear Dual-Band Mixed-Mode Polar Power Amplifier: top schematic



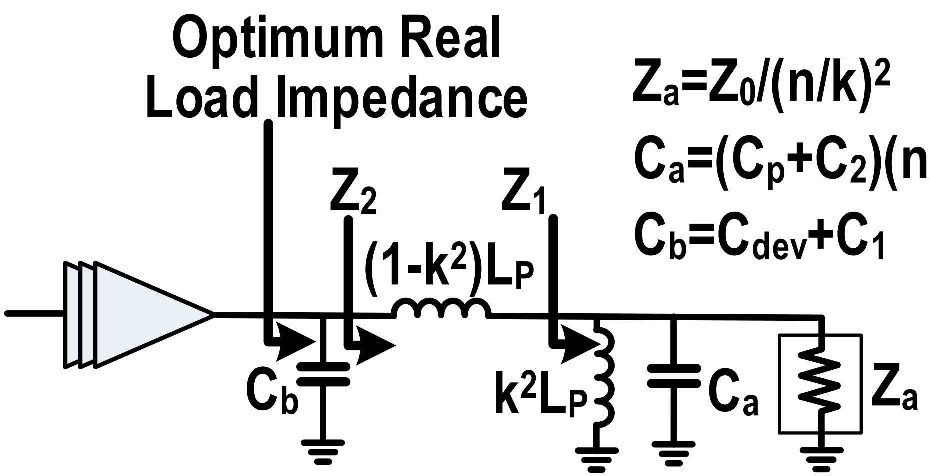
Circuit Schematic

Output passive network: dual band optimum load pull impedance matching



Circuit Schematic

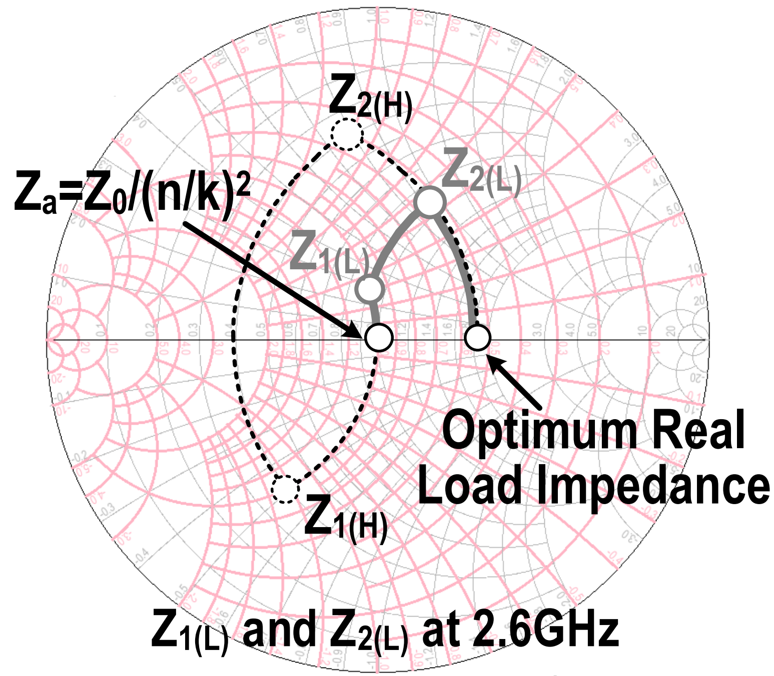
Output passive network: dual band optimum load pull impedance matching



$Z_a = Z_0/(n/k)^2$

$C_a = (C_p + C_2)(n/k)^2$

$C_b = C_{dev} + C_1$



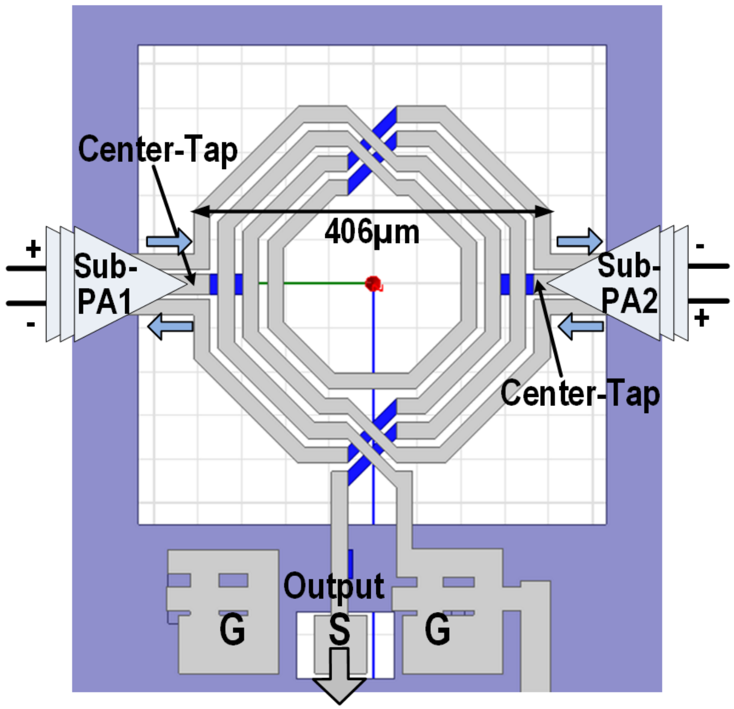
$Z_{1(L)}$ and $Z_{2(L)}$ at 2.6GHz

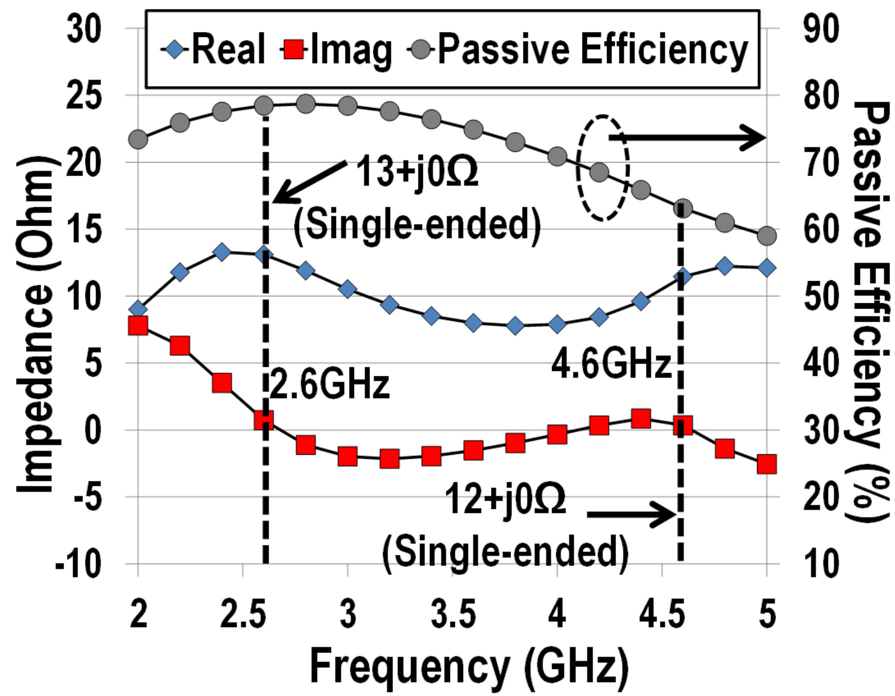
$Z_{1(H)}$ and $Z_{2(H)}$ at 4.6GHz

- Dual band optimum load impedance matching within one transformer foot print.
- PA device parasitic capacitance is absorbed into the output passive network design.

Circuit Schematic

Output passive network: full 3D EM model and EM simulation results





- The desired optimum real load impedance 13Ω (>+28dBm) is achieved at 2.6GHz and 4.6GHz (note that PA device capacitance is absorbed into output passive network).
- The Passive efficiencies for the desired odd-mode (fundamental tone) are 78.5% and 62% for 2.6GHz and 4.6GHz, respectively.

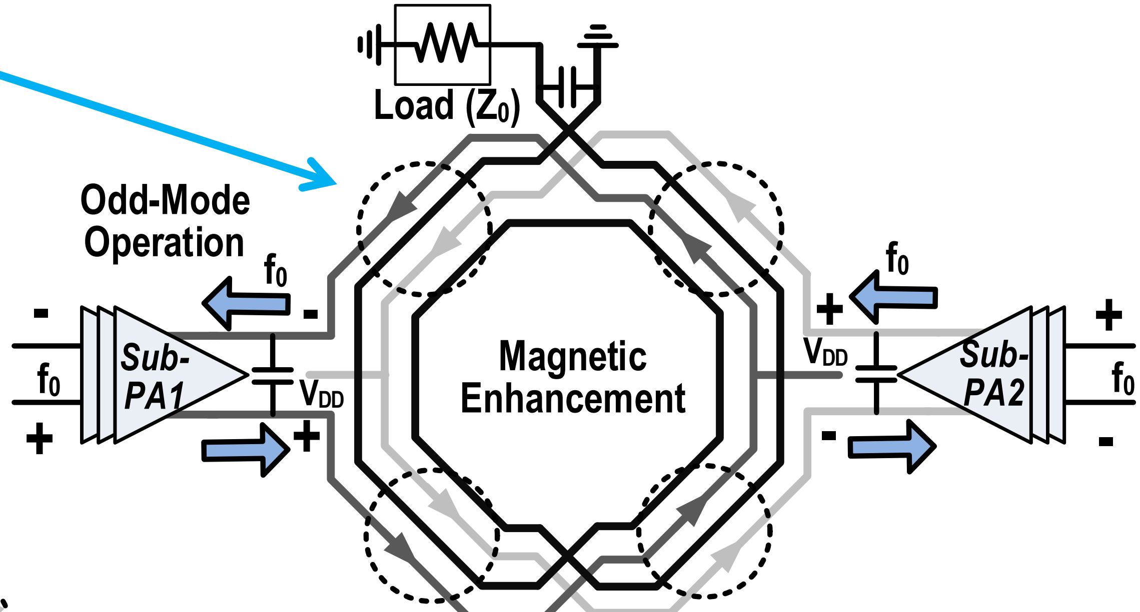
Circuit Schematic

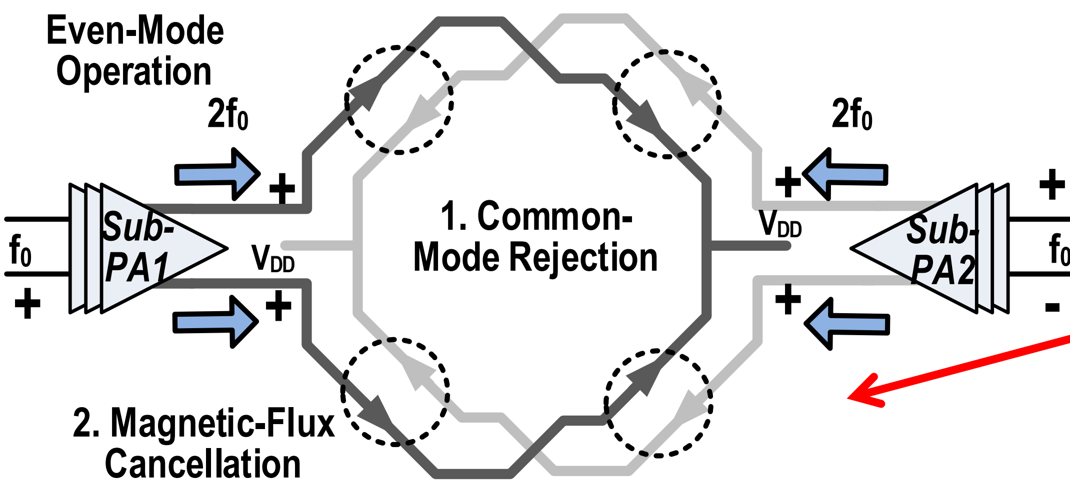
GEMS CICC

Output passive network: 2nd harmonic leakage cancellation

① <u>Desired fundamental current</u>

- Low loss
- Size reduction ($L_{eff}=L_{self}+M$)
- 4× net current for secondary coil



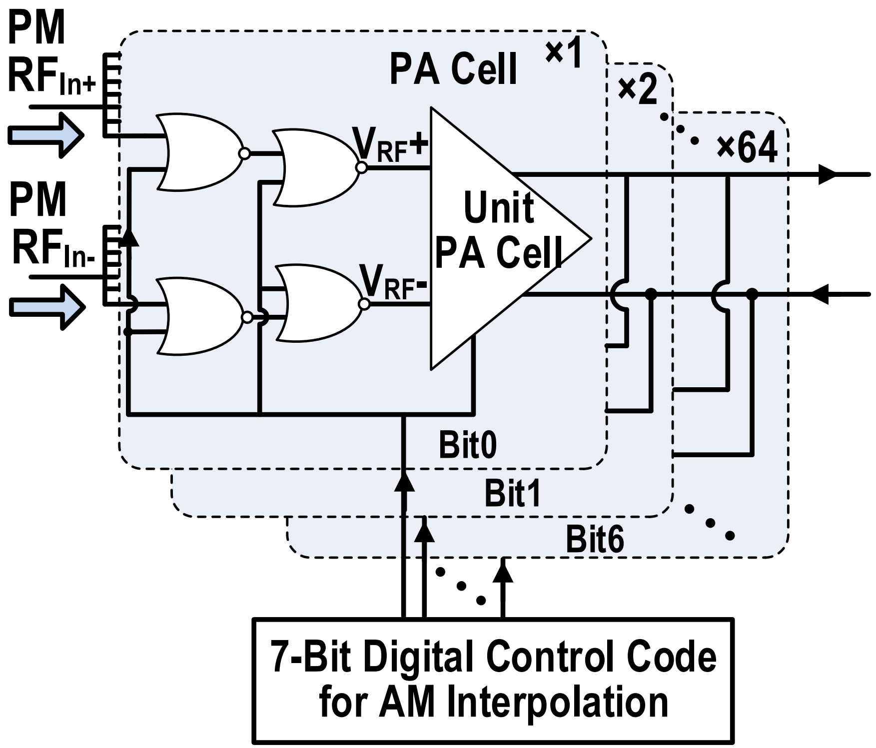


② <u>Undesired 2nd harmonic current</u>

- Zero net current for secondary coil

Circuit Schematic

Mixed-mode PA linearization techniques: digital AM-AM distortion compensation

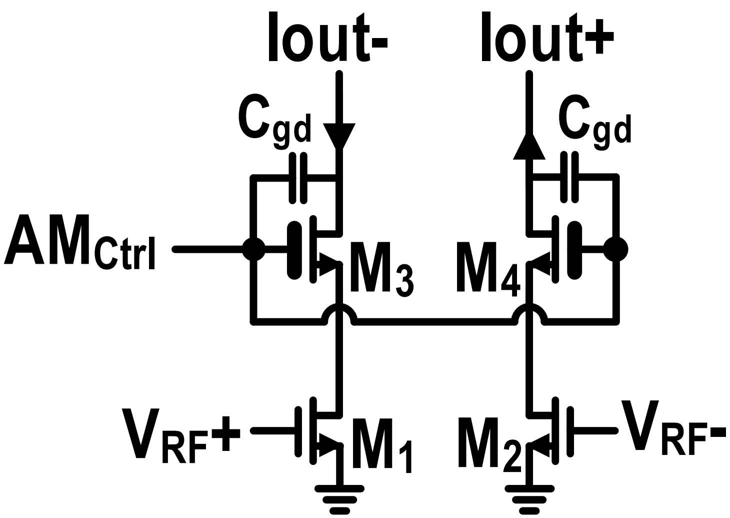


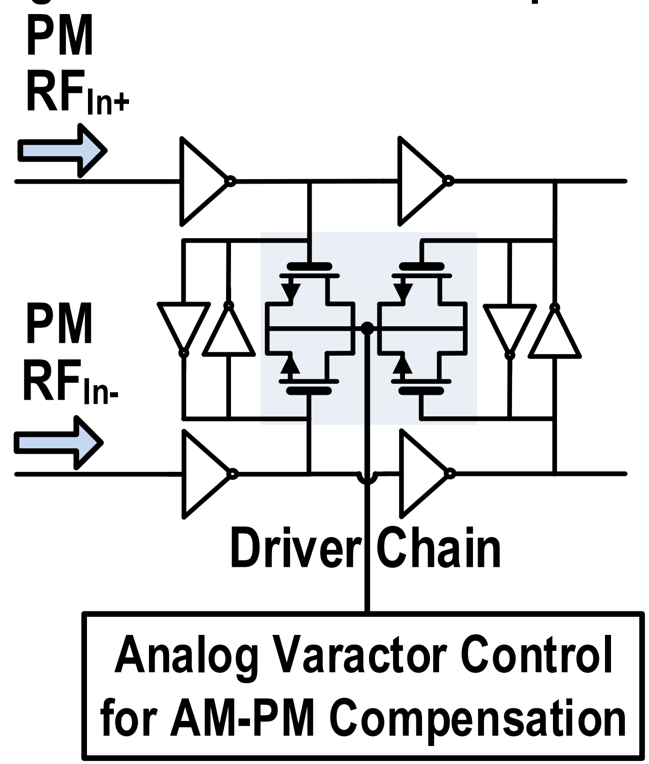
• 7-bit digital amplitude control codes to synthesize the desired amplitude → precise interpolation of the transient envelope and direct pre-distortion.

• The RF phase modulated input signals restore complex modulation at the output.

Circuit Schematic

Mixed-mode PA linearization techniques: analog AM-PM distortion compensation





- Non-linear capacitance C_{gd} of CG transistor (M3 and M4) is one of the main reasons for AM-PM distortion for digital class D^{-1} PA architecture.

- In order to compensate AM-PM distortion, we employ varactors in the driver chain.

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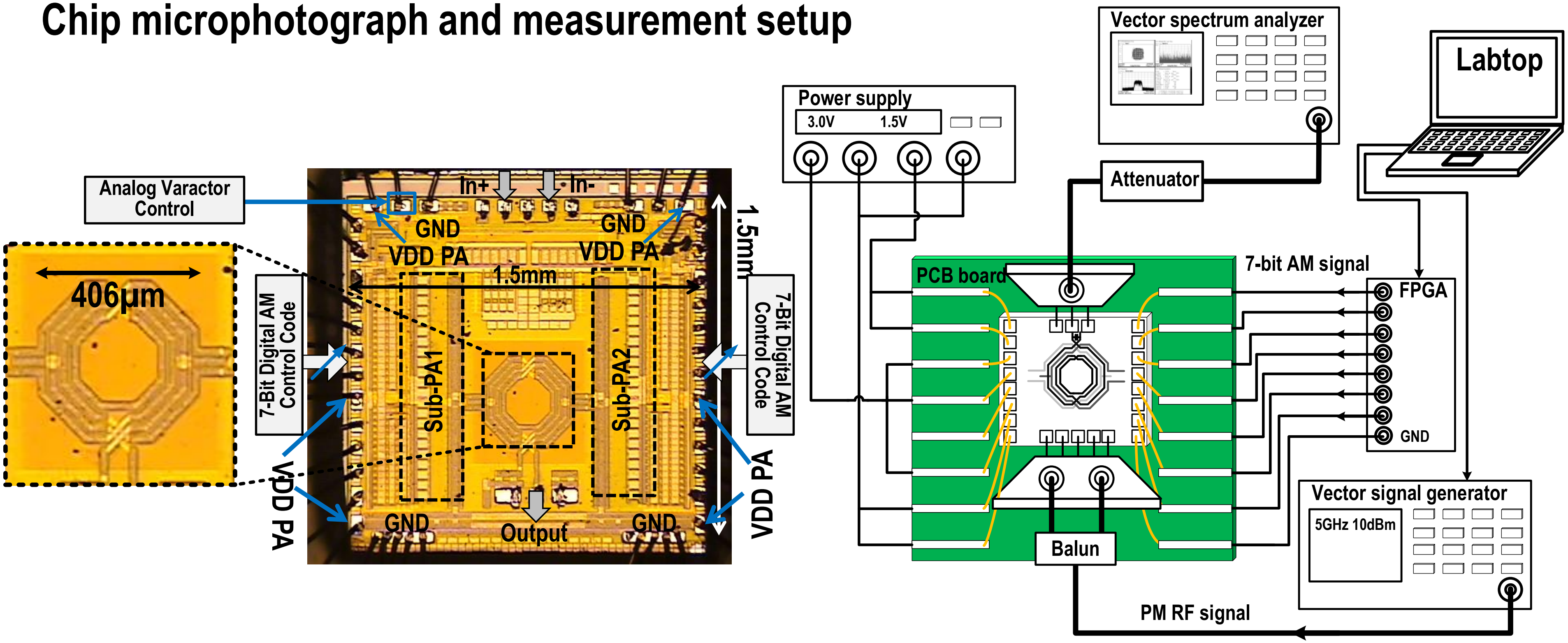
Measurement Results

Chip microphotograph and measurement setup



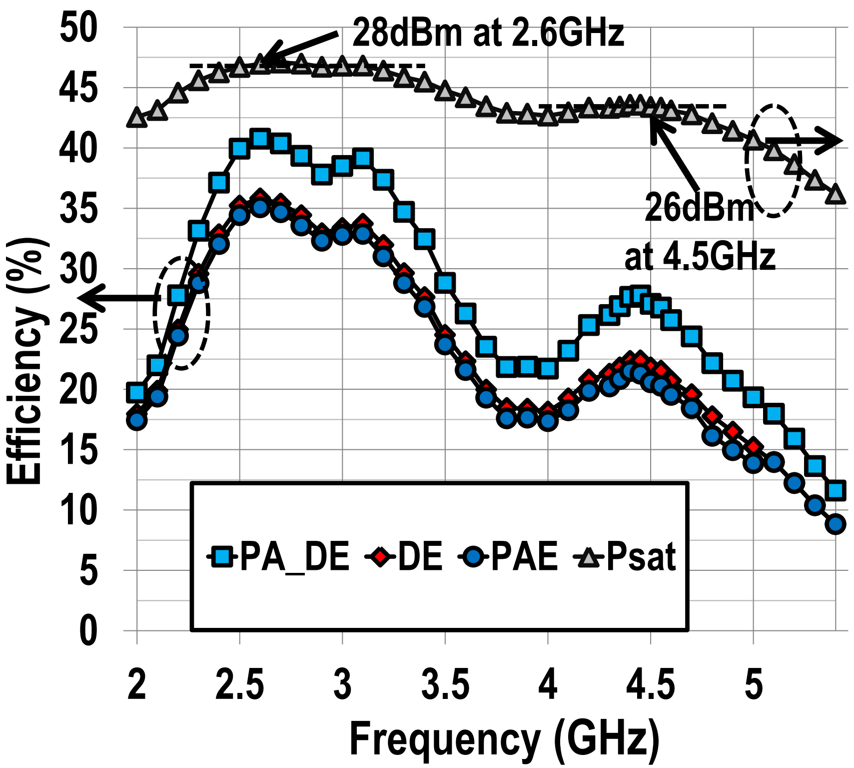
• Standard 65nm CMOS process with low resistive substrate 100S/m.

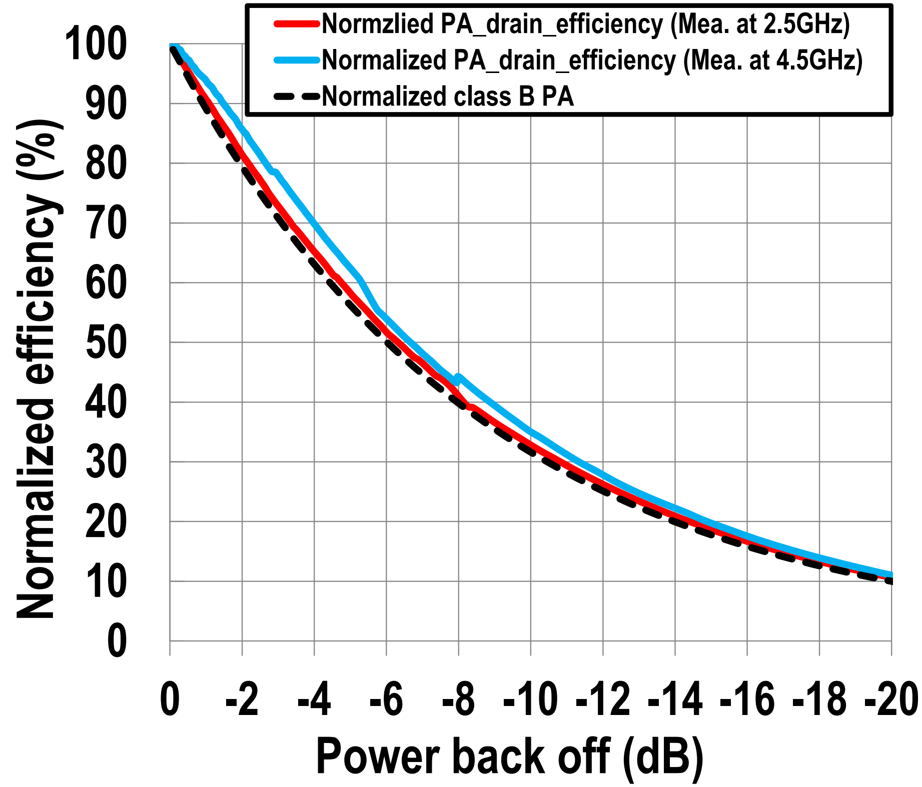
• The proposed PA is implemented within 1.5mm×1.5mm chip area and the diameter of the ultra-compact output network is 406μm.

• The supply for PA cores and digital drivers are 3V and 1.5V, respectively.

Measurement Results

Continuous-Wave (CW) measurement results

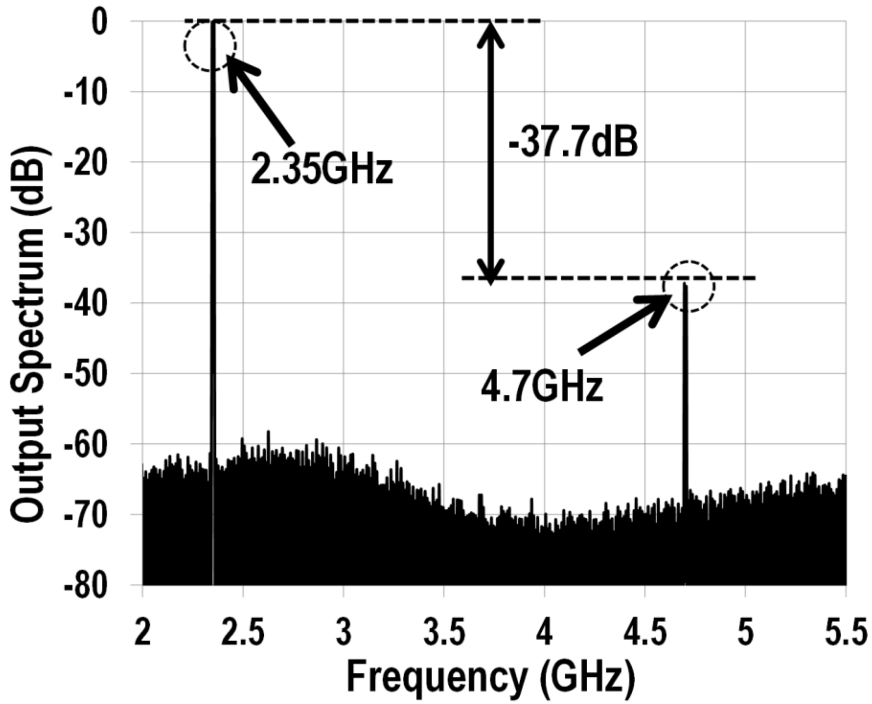


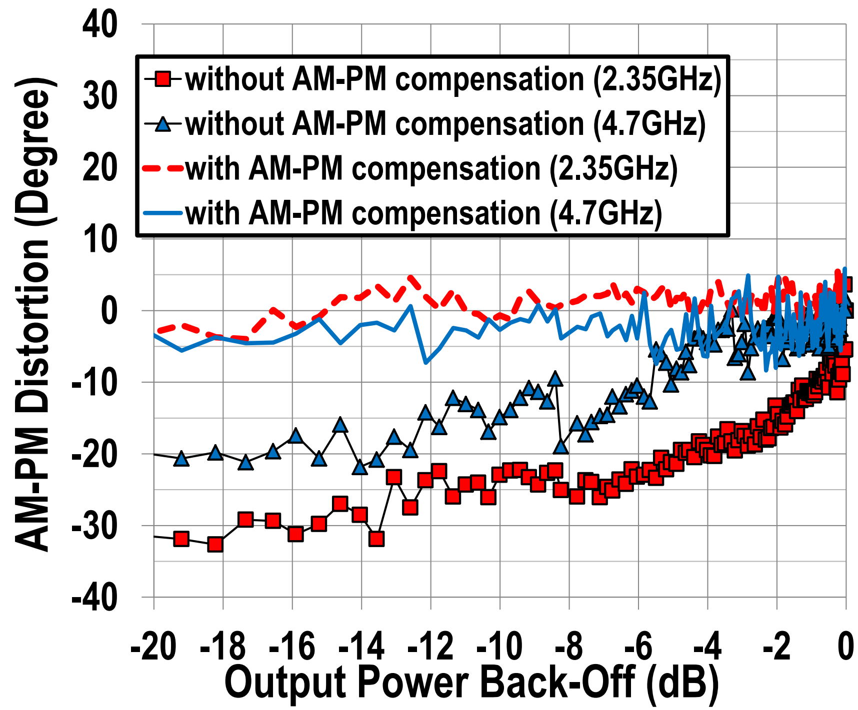


- The measured peak PA Drain Efficiency (PA_DE) and power added efficiency (PAE) are 40.7%/27.0% and 35%/21.2% with +28.1dBm/+26.0dBm output power at 2.6GHz/4.5GHz.
- The measured back-off efficiency curves closely follow the class-B PA.

Measurement Results

Continuous-Wave (CW) measurement results

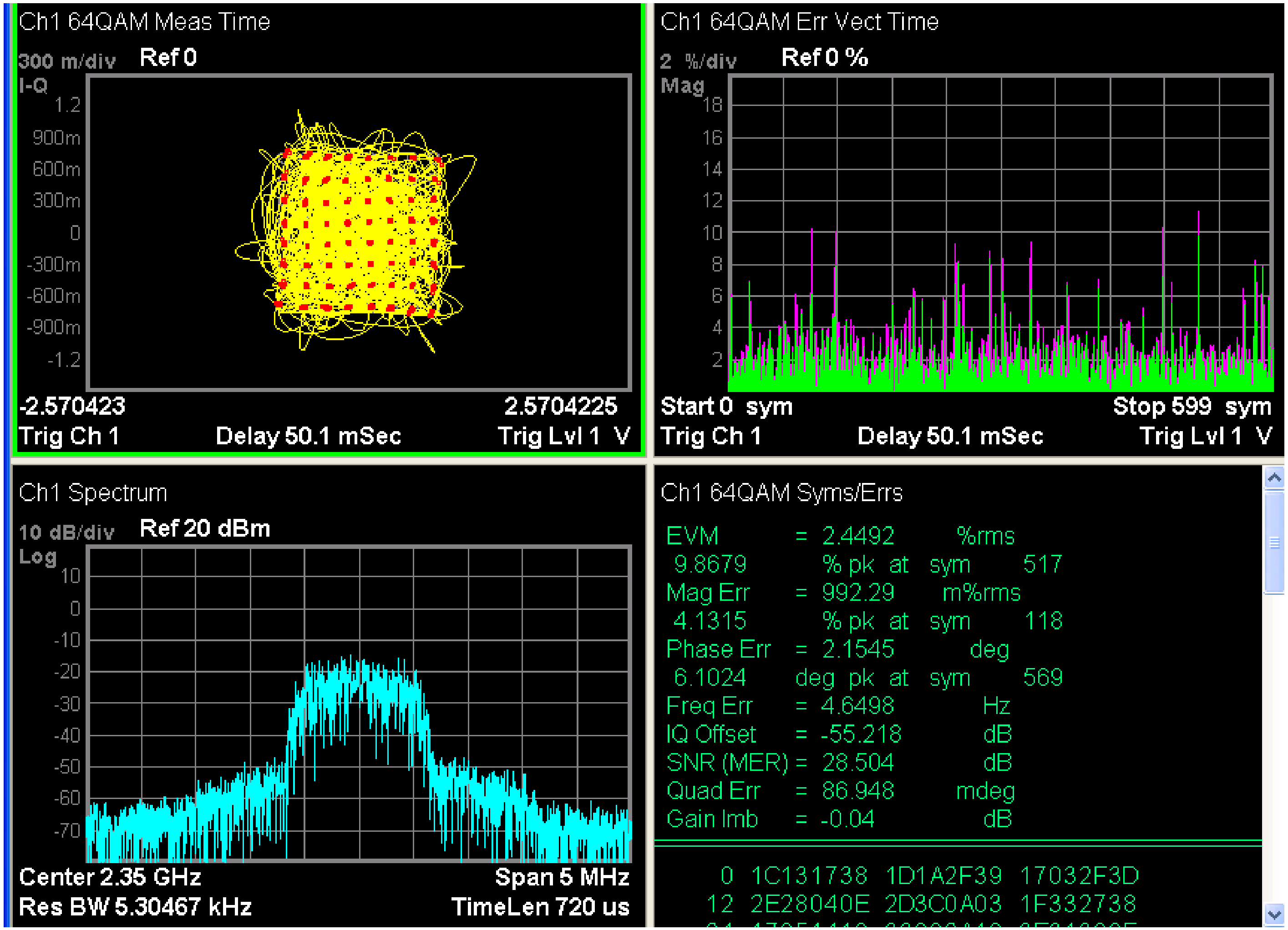




- The measured 2nd harmonic suppression is 37.7dB at 2.35GHz (2nd harmonic at 4.7GHz).
- The analog varactor control voltage is adjusted to compensate AM-PM distortion.

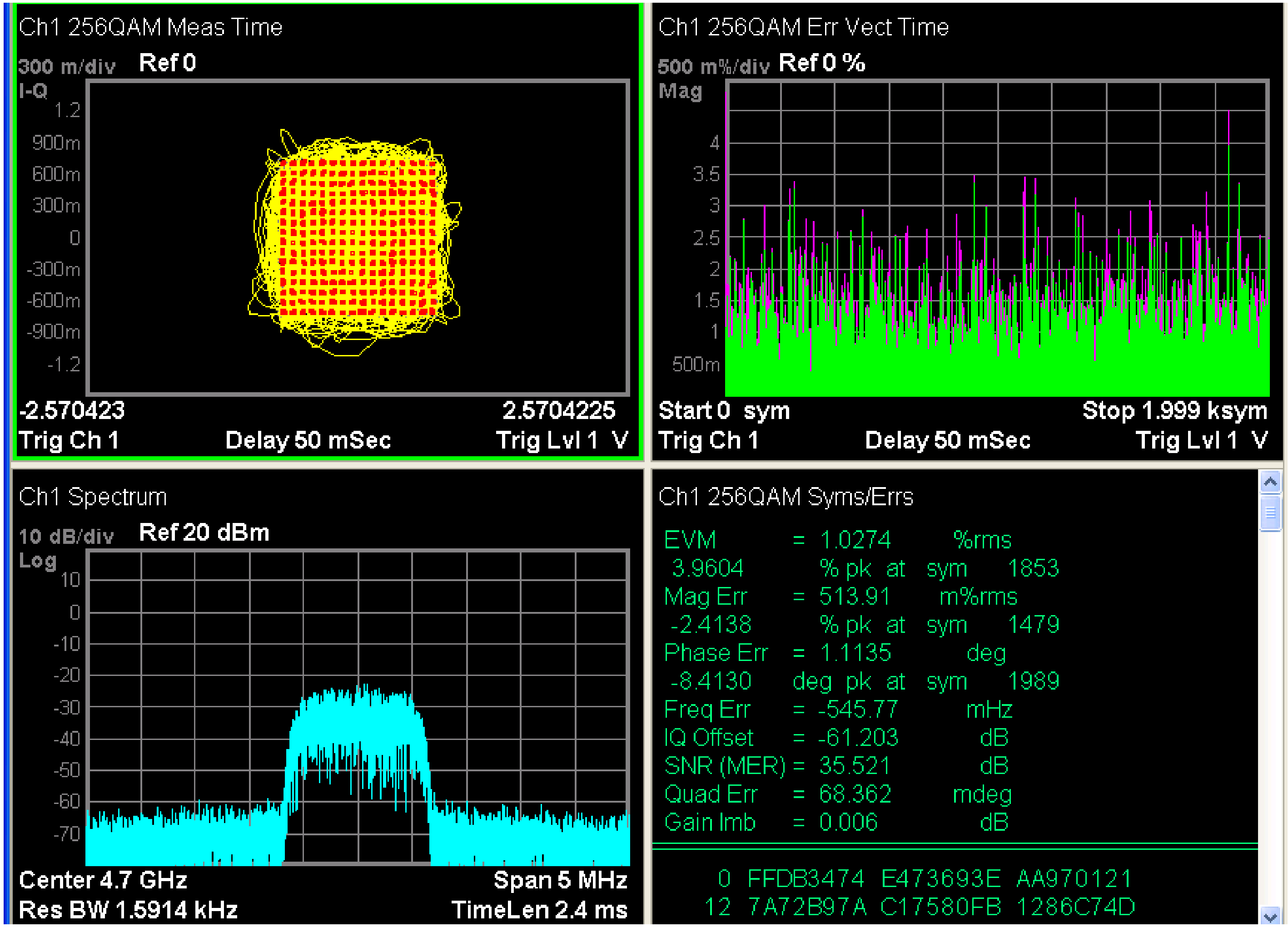
Measurement Results

Modulation test 64QAM 1MSym/s with Pout=22.28dBm at 2.35GHz PA DE 19.1%



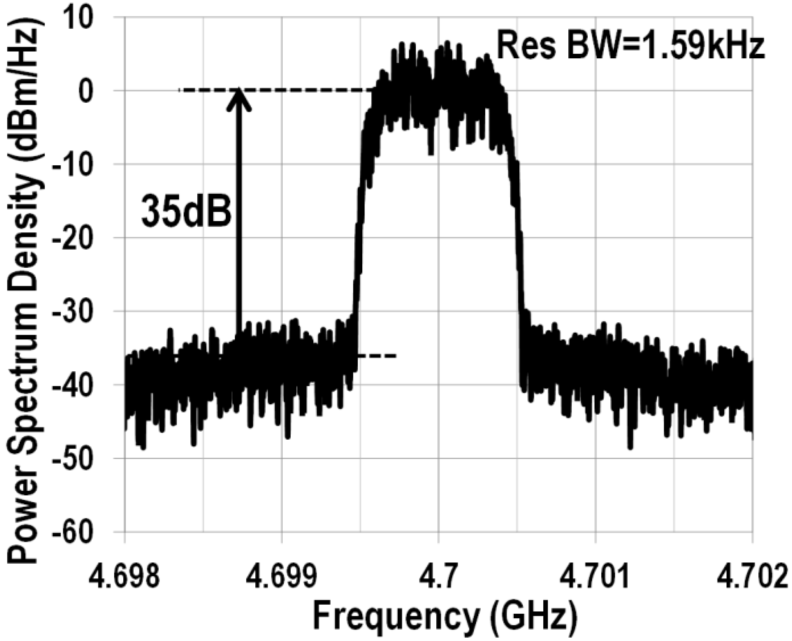
Measurement Results

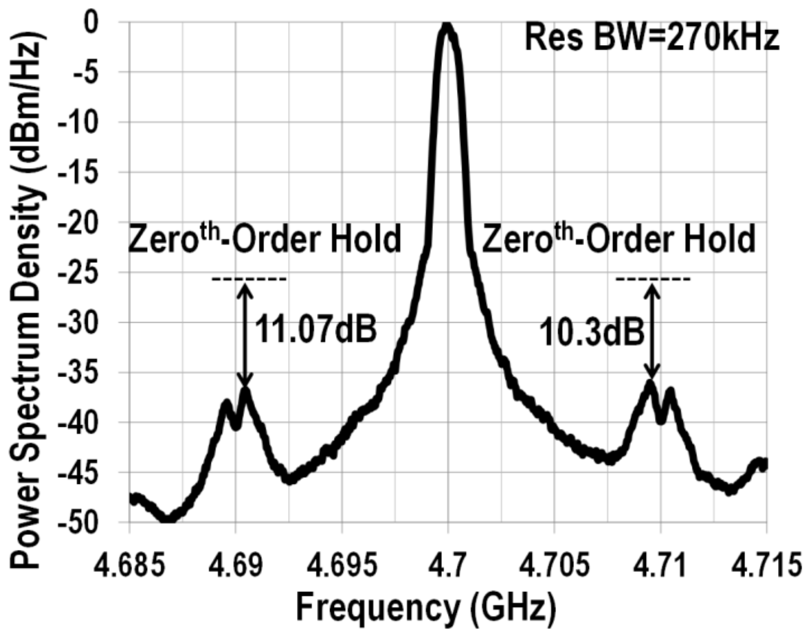
Modulation test 256QAM 1MSym/s with Pout=19.27dBm at 4.7GHz PA DE 13.6%



Measurement Results

Modulation test 256QAM 1MSym/s with Pout=19.27dBm at 4.7GHz PA DE 13.6%



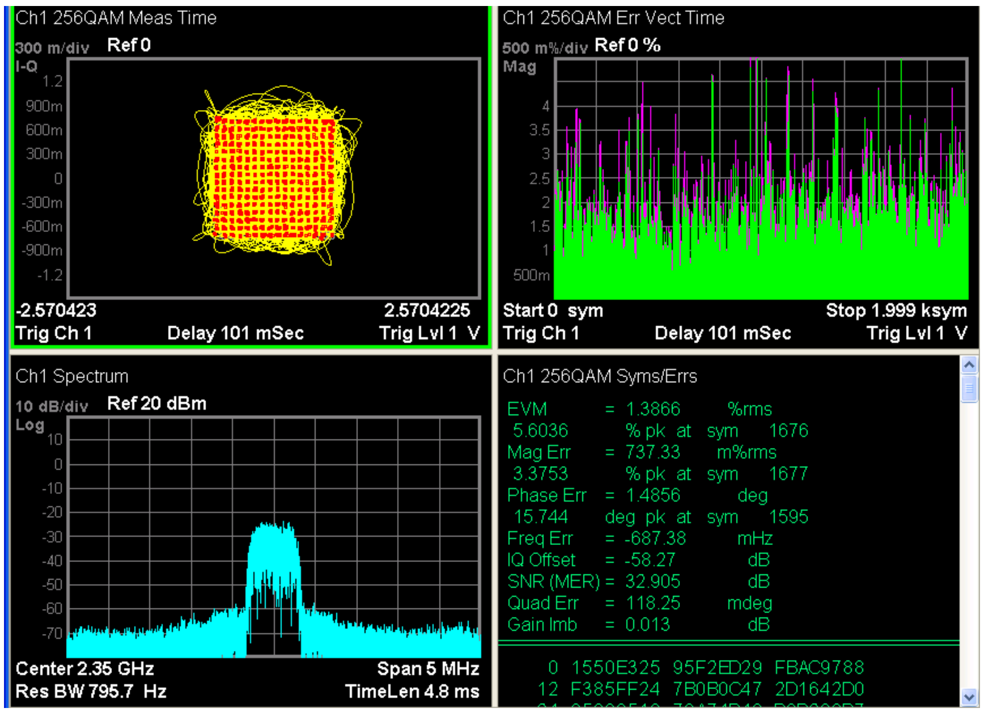


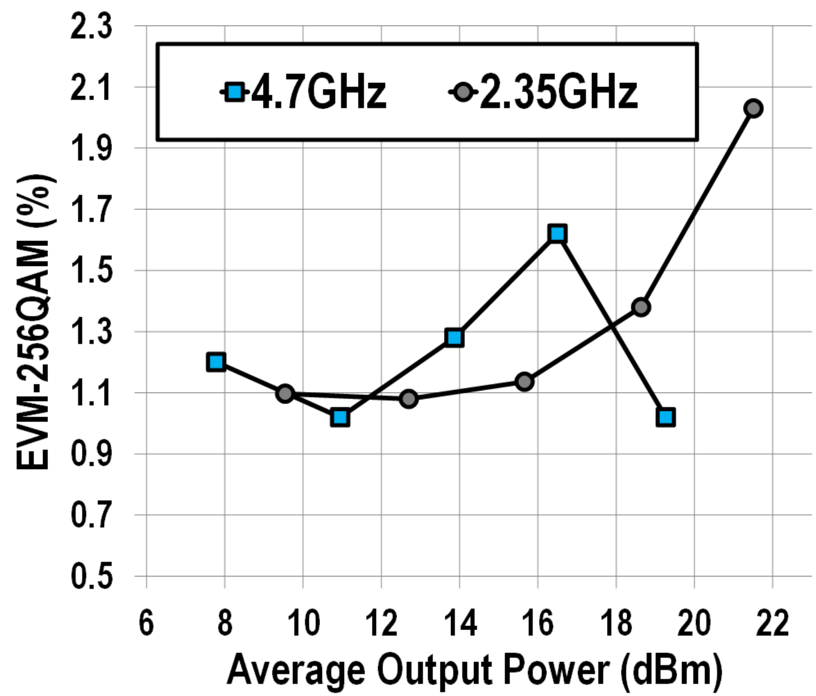
- The close-in out-of-band spectrum is kept below -35dBc with no additional filtering.
- For 1MSym/s modulation with ×10 over sampling, the sampling images appear at 4.71GHz and 4.69GHz with 36.7dB suppression, which is 11dB better than the zeroth-order hold sampling images.

Measurement Results

Modulation test with power back-off.

256QAM, 0.5MSym/s, Pout=18.64dBm at 2.35GHz (3dB PBO)





• The measured rms EVMs for 0.5MSym/s 256-QAM signals (PAPR=6.62dB) versus P_{out} back-off up to 12 dB, showing EVM below 2.1% at both 2.35GHz and 4.7GHz.

Comparison table

This work is compared to the recently published multi-band power amplifier in CMOS

	Freq. (GHz)	Configuration	Output Network Configuration	Peak P_{out} (dBm)	Peak Efficiency (%)	Modulation Test (rms EVM/P_{out}/Efficiency)	Technology
This Work	**2.6/4.5**	**Single PA**	**1 transformer (no switch or tunable element)**	**28.1/26.0**	**35/21.2 (PAE) 40.7/27.0 (PA DE)**	**2.05% (256QAM)/21.51dBm/18.5% (PA DE) at 2.35GHz 1.03% (256QAM)/19.27dBm/13.6% (PA DE) at 4.7GHz**	**65 (nm)**
Ref [1]	2.4/5	Multiple PAs	2 transformers	28.3/26.7	35.3/25.3 (DE)	3.98% (OFDM)/19.5dBm/14.1% (DE)	65 (nm)
Ref [2]	2.4/5	Multiple PAs	2 transformers	29/26	33.9/32.1 (DE)	5.6% (64QAM)/18.7dBm/N.A.	45 (nm)
Ref [7]	1.95/2.4	Single PA	4 transformers	31.8/32	28.8/32.4 (PAE)	2.8% (OFDM)/23.8dBm/N.A.	65 (nm)
Ref [8]	2.4/5	Multiple PAs	N.A.	26.8/26.6	N.A.	3.9% (OFDM)/17dBm/17.5% (PA_DE)	90 (nm)
Ref [9]	2/6	Single PA	1 transformer+3 inductors	22.4/20.1	28.4/19 (PAE)	2.5% (256QAM)/11.3dBm/N.A.	65 (nm)

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Conclusion

- A highly linear dual-band mixed-mode polar PA fully integrated in a standard 65nm CMOS is demonstrated.
- The output passive network occupies only one-inductor footprint and achieves dual-band optimum load matching, parallel power combining, double even-mode rejection, and differential to single-ended conversion.
- Mixed-mode techniques are employed to largely suppress the AM-AM and AM-PM distortions.
- The PA achieves +28.1dBm/ +26.0dBm peak Pout with 40.7%/27.0% peak PA drain efficiency at 2.6/4.5GHz with 37.7dB 2nd-harmonic suppression.
- The PA supports high-fidelity amplification of high-order QAM modulations and demonstrates 2.05% and 1.03% rms EVMs for 1MSym/s 256-QAM signal at 2.35GHz and 4.7GHz.