A Dual-Band 802.11abgn/ac Transceiver with Integrated PA and T/R Switch in a Digital Noise Controlled SoC

Che-Hung Liao[1]

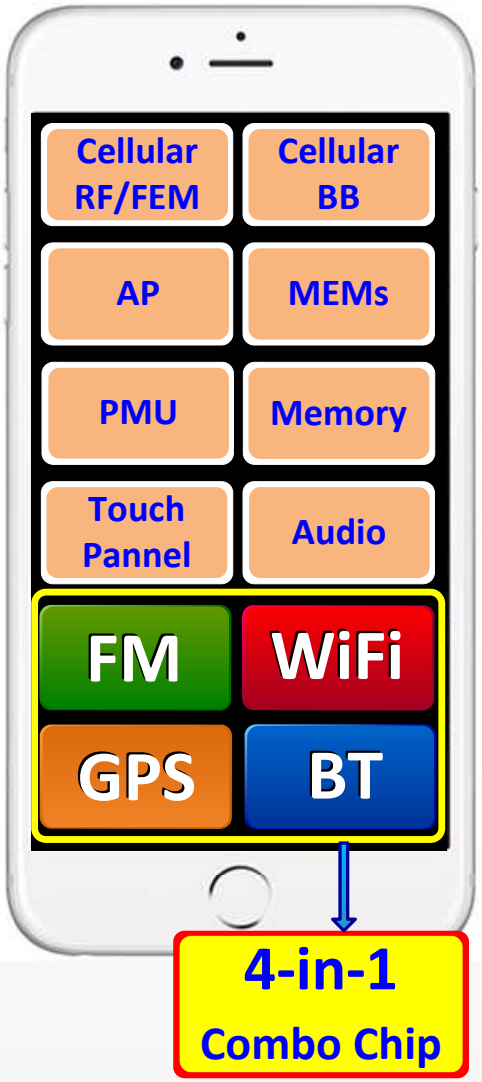
Yuan-Hung Chung[1], Che-Hung Liao[1], Chun-Wei Lin[1], Yi-Shing Shih[1], Chin-Fu Li[1], Meng-Hsiung Hung[1], Ming-Chung Liu[1], Pi-An Wu[1], Jui-Lin Hsu[1], Ming-Yeh Hsu[1], Sheng-Hao Chen[1], Po-Yu Chang[1], Chih-Hao Chen[1], Yu-Hsien Chang[1], Jun-Yu Chen[1], Tao-Yao Chang[1], George Chien[2].

[1] MEDIATEK INC., HSINCHU, TAIWAN, 30078, R.O.C., [2] MEDIATEK INC., SAN JOSE, CA

Outline

- Introduction and Motivation
- Block diagram of SoC
- Transceiver architecture and Circuit Design
- Coupling and De-sensitization
- Experimental Results
- Conclusion

Introduction

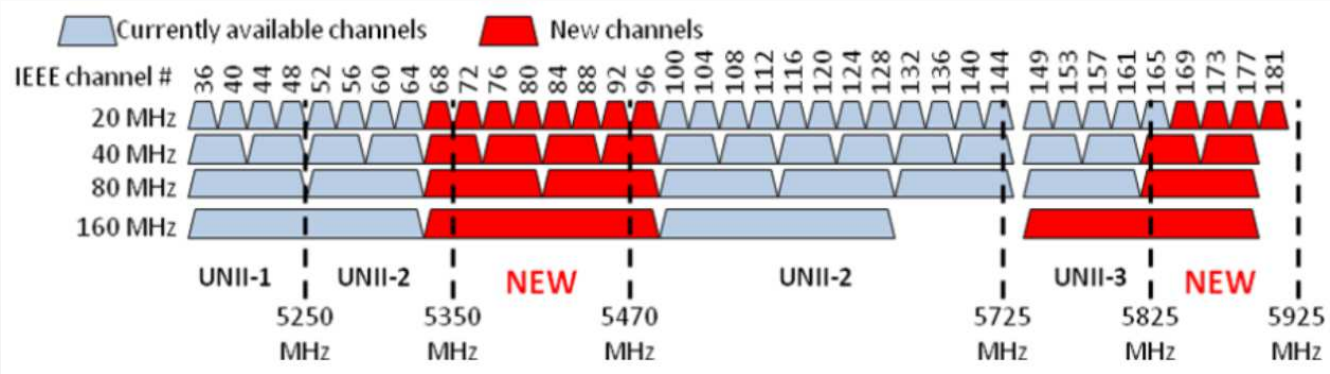


Motivation :

- A dual-band WiFi transceiver design for high data rate requirement in multi-radio connectivity SoC

Challenge :

- RF architecture selection for wide frequency range (~1GHz), and wide signal BW circuit design



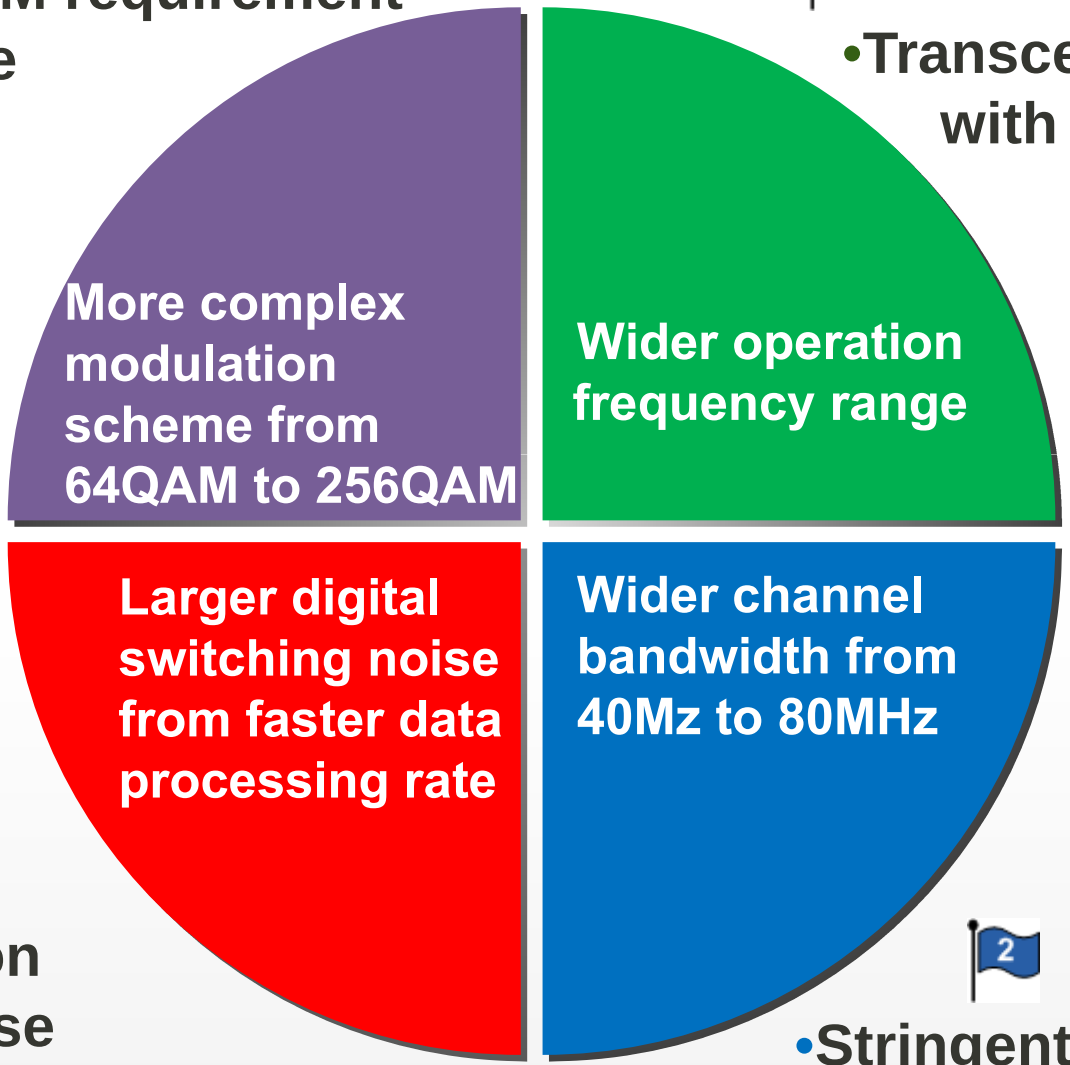
Challenges to Circuit Design

3

•Stringent EVM requirement
1.Phase noise
2.TX linearity

1

•Transceiver design with broadband matching



4

•Digital to RF de-sensitization
1.switching noise
2.clock harmonics

2

•Stringent IQ imbalance requirement(FD-IQ)

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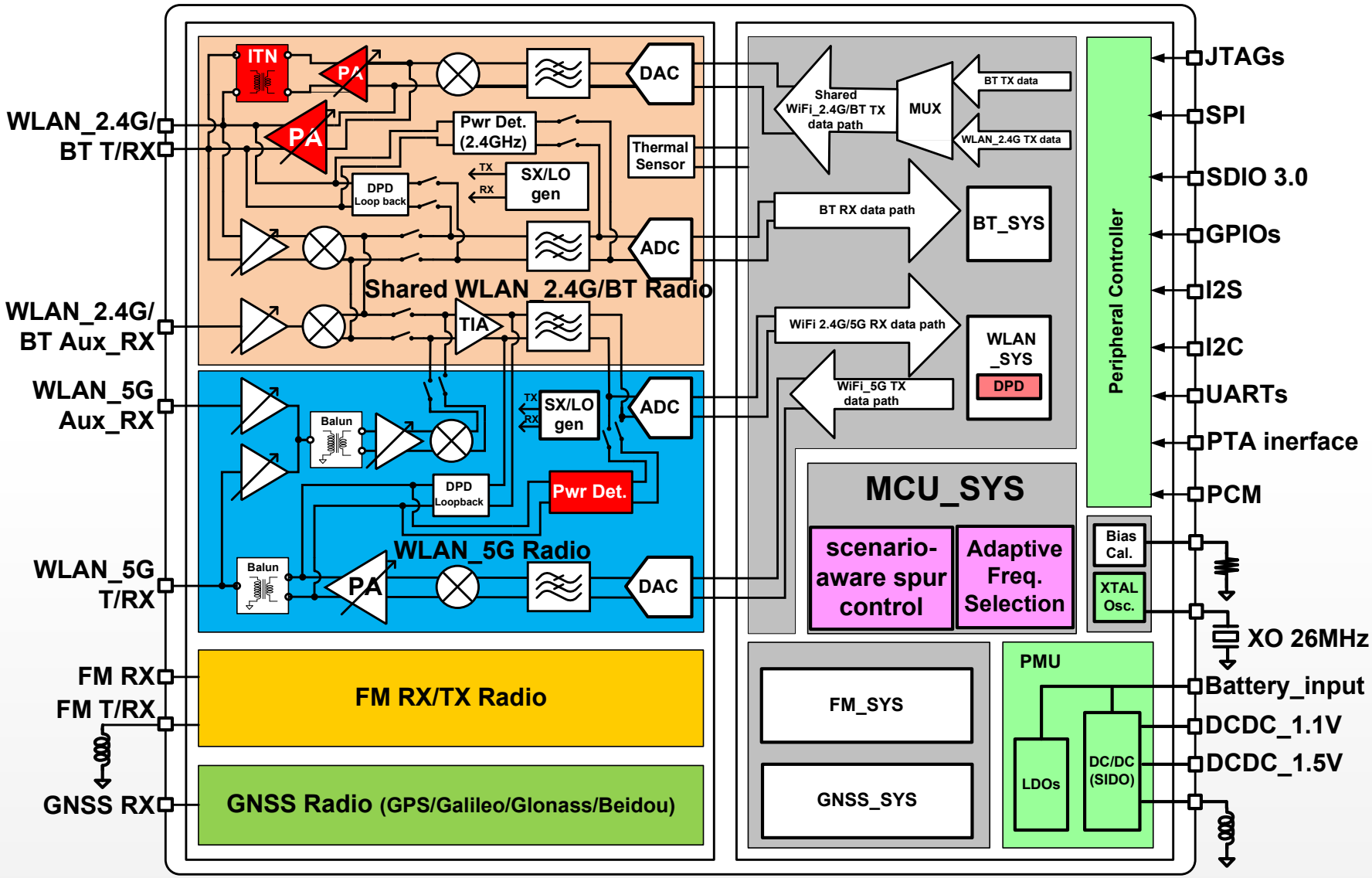
4-in-1 Connectivity Combo Block Diagram of SoC



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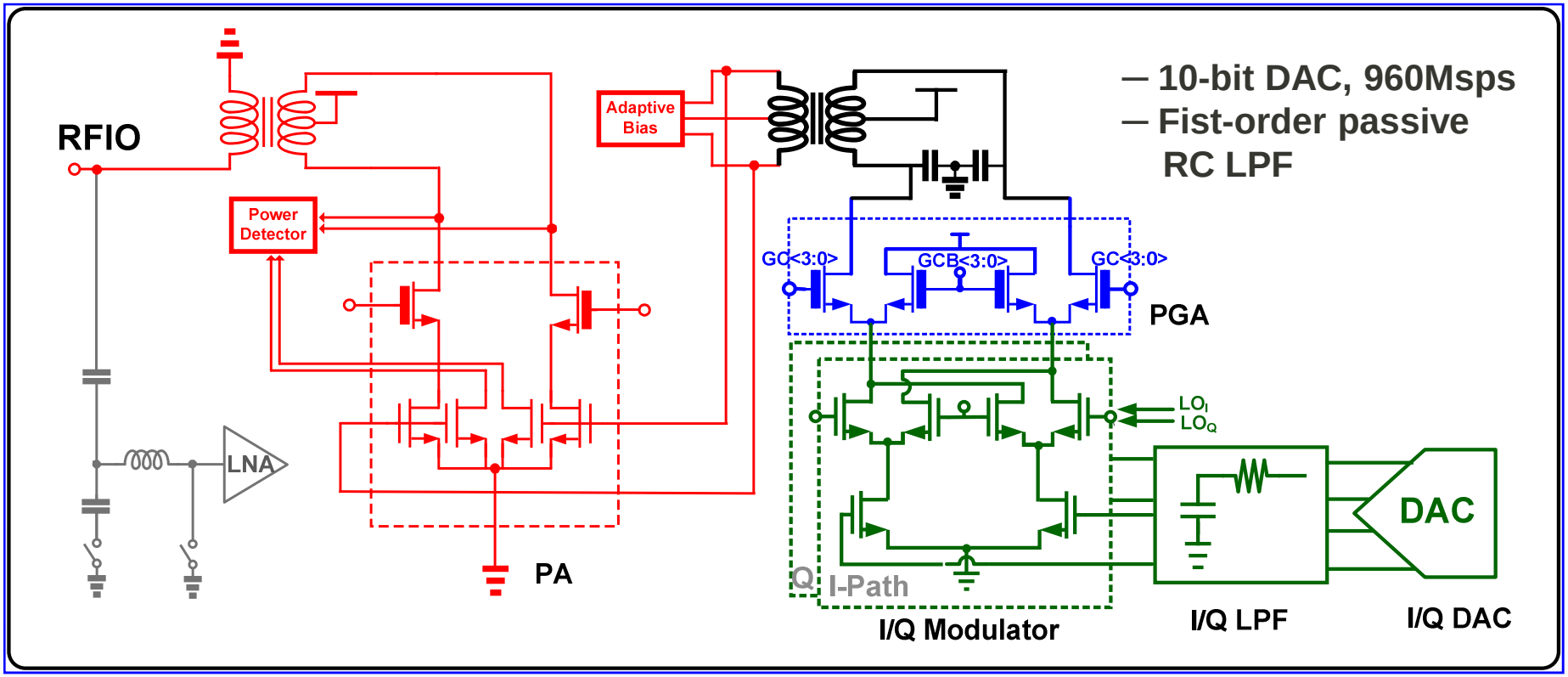
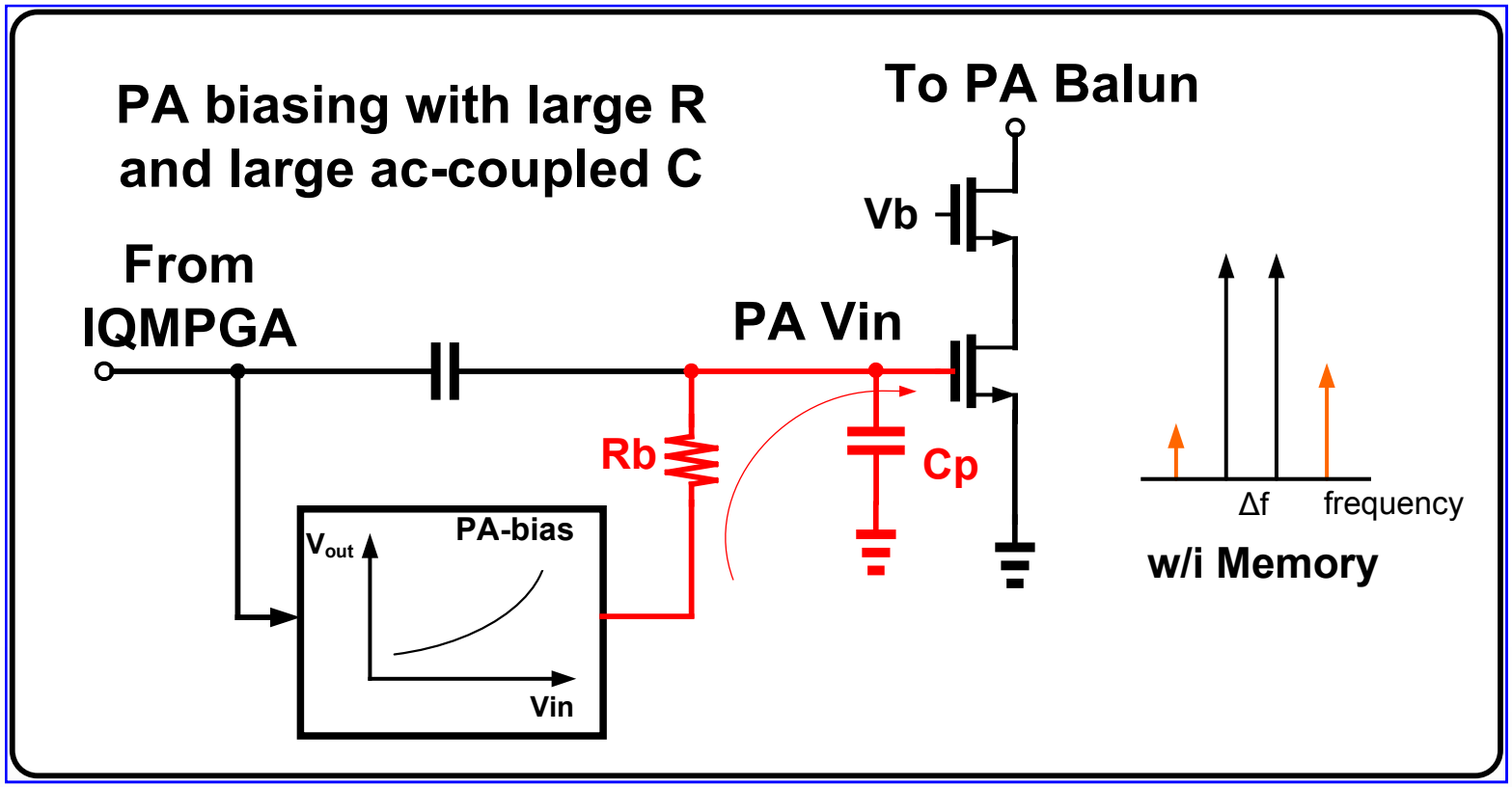
5GHz WiFi TX Architecture



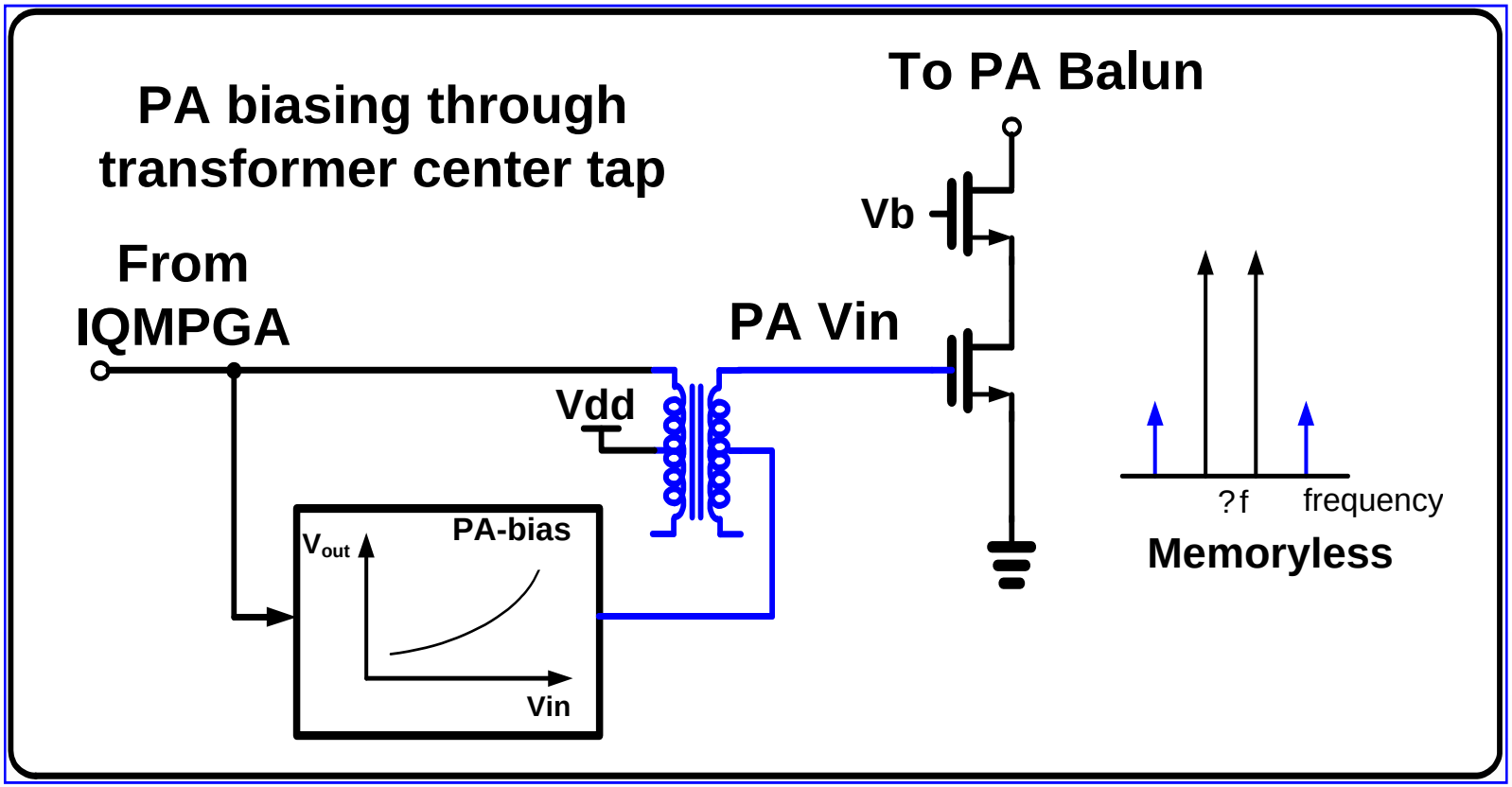
- First-order passive RC LPF 3dB BW can be designed around 100MHz. It reduces the FD-IQ mismatch caused by LPF.
- Adaptive PA bias circuit track input signal to boost bias voltage to improve linearity

PA biasing limitation



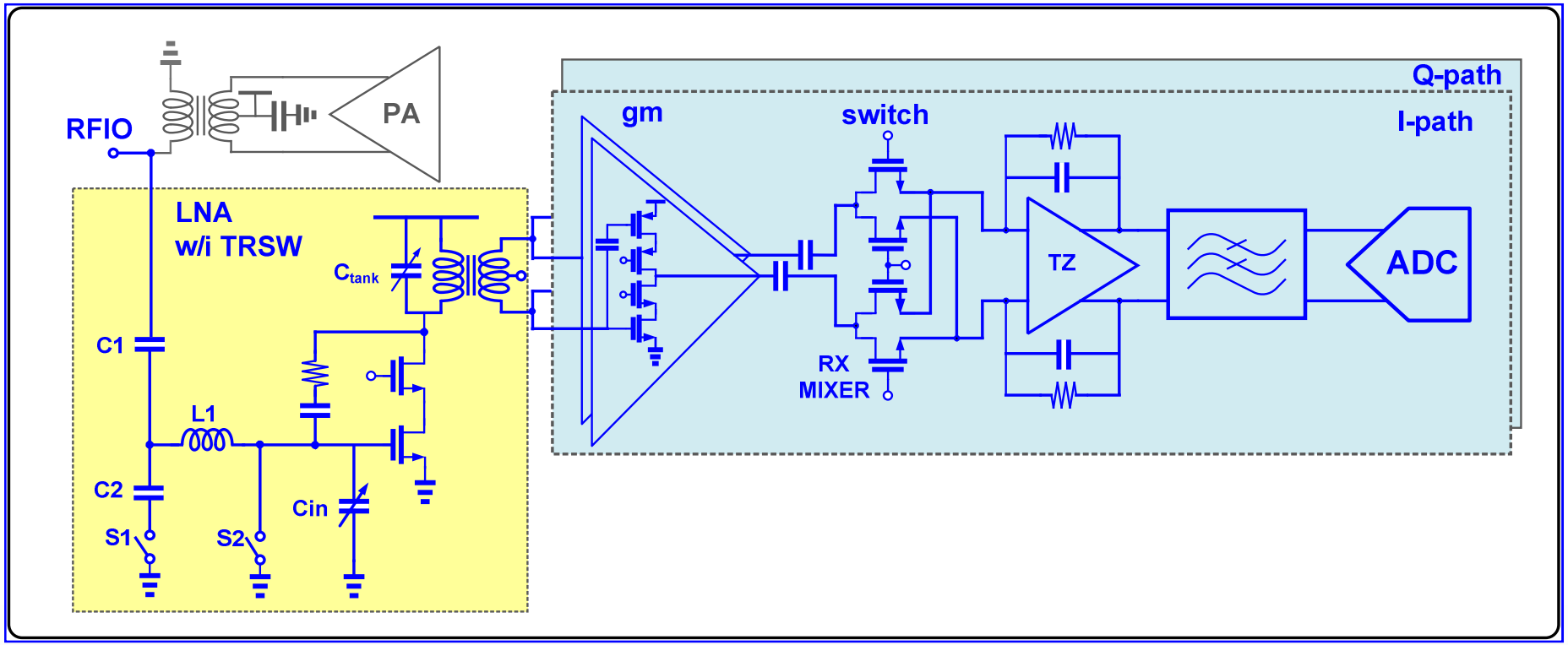
- Rb and Cp forms a LPF, limit the BW of tracking PA bias signal significantly, cause memory effects
  - Asymmetric spectrum
  - IM3 degradation with larger frequency spacing of 2-tone

Wide bandwidth PA biasing



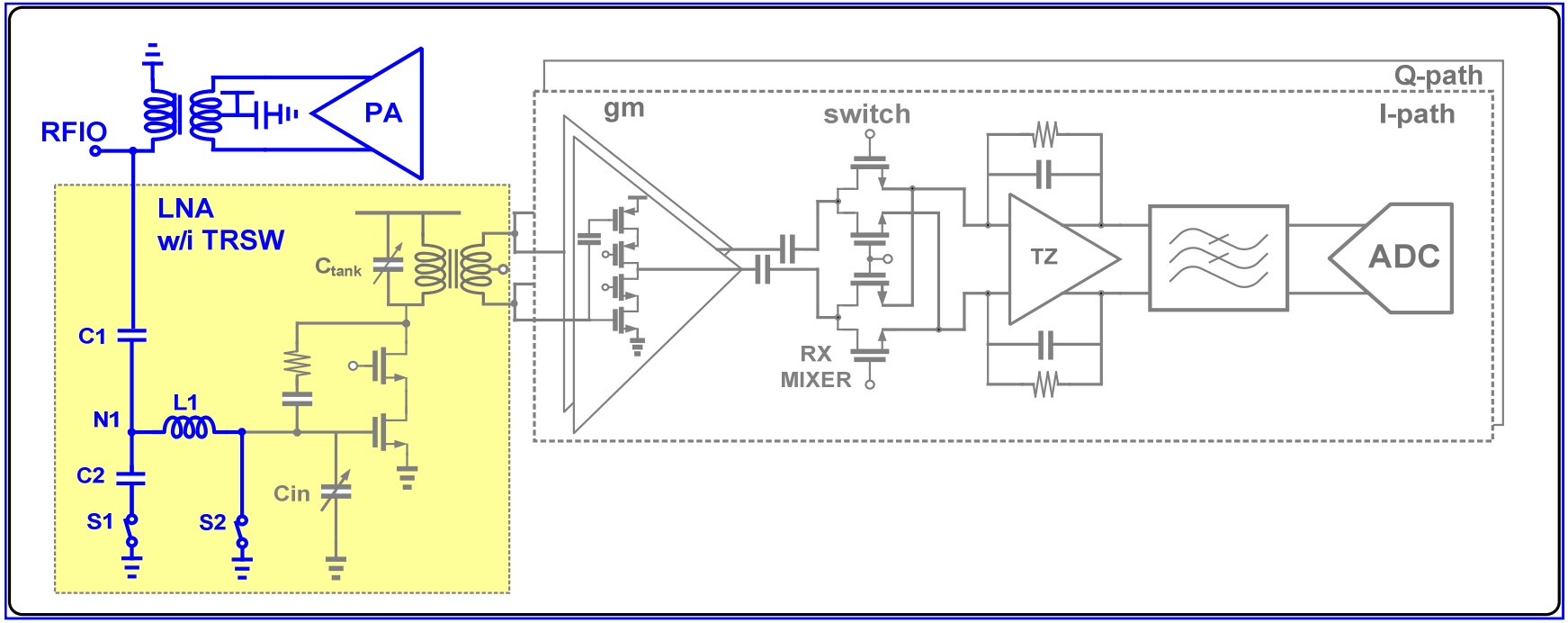
- Adaptive tracking bias is connected to the center-tap of transformer secondary coil to increase the BW of the tracking circuit

T/R SW and RX Chain



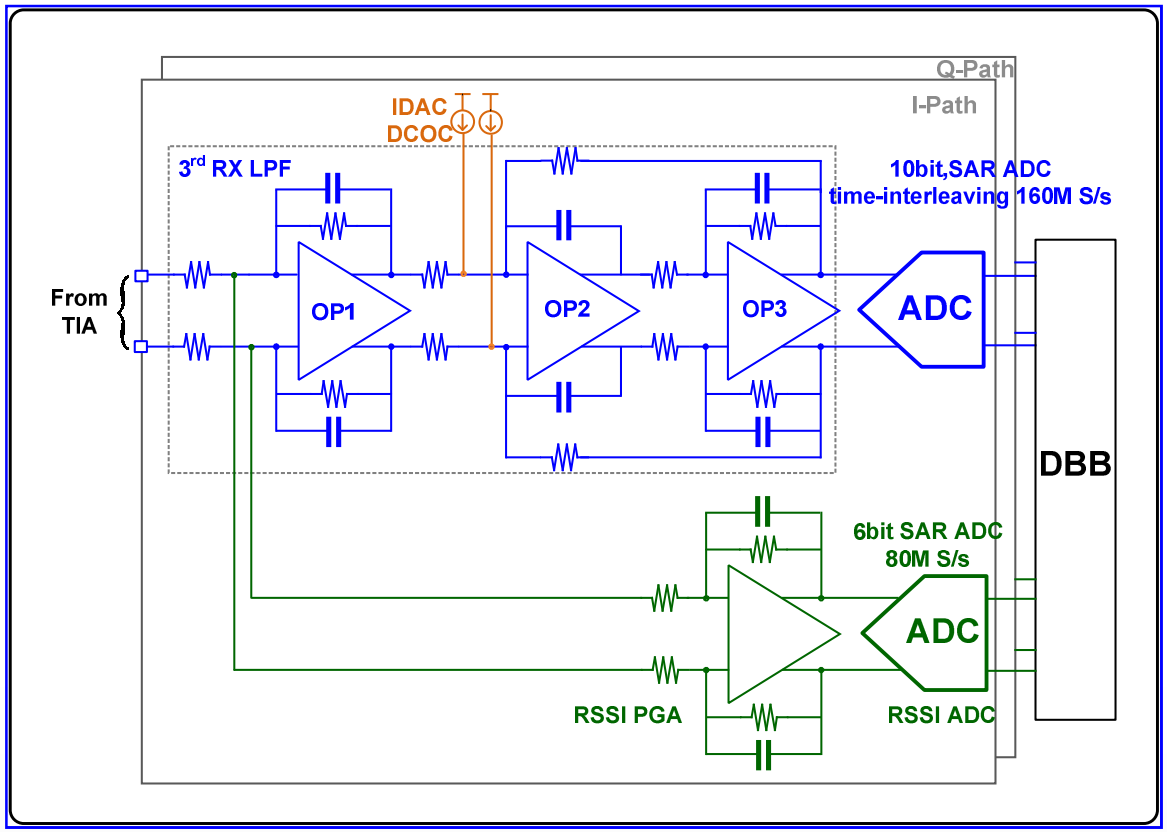
- RX mode: S1,S2 = open
- Wideband RX design: Single-ended LNA with resistor shunt-shunt feedback

T/R SW Configuration in TX



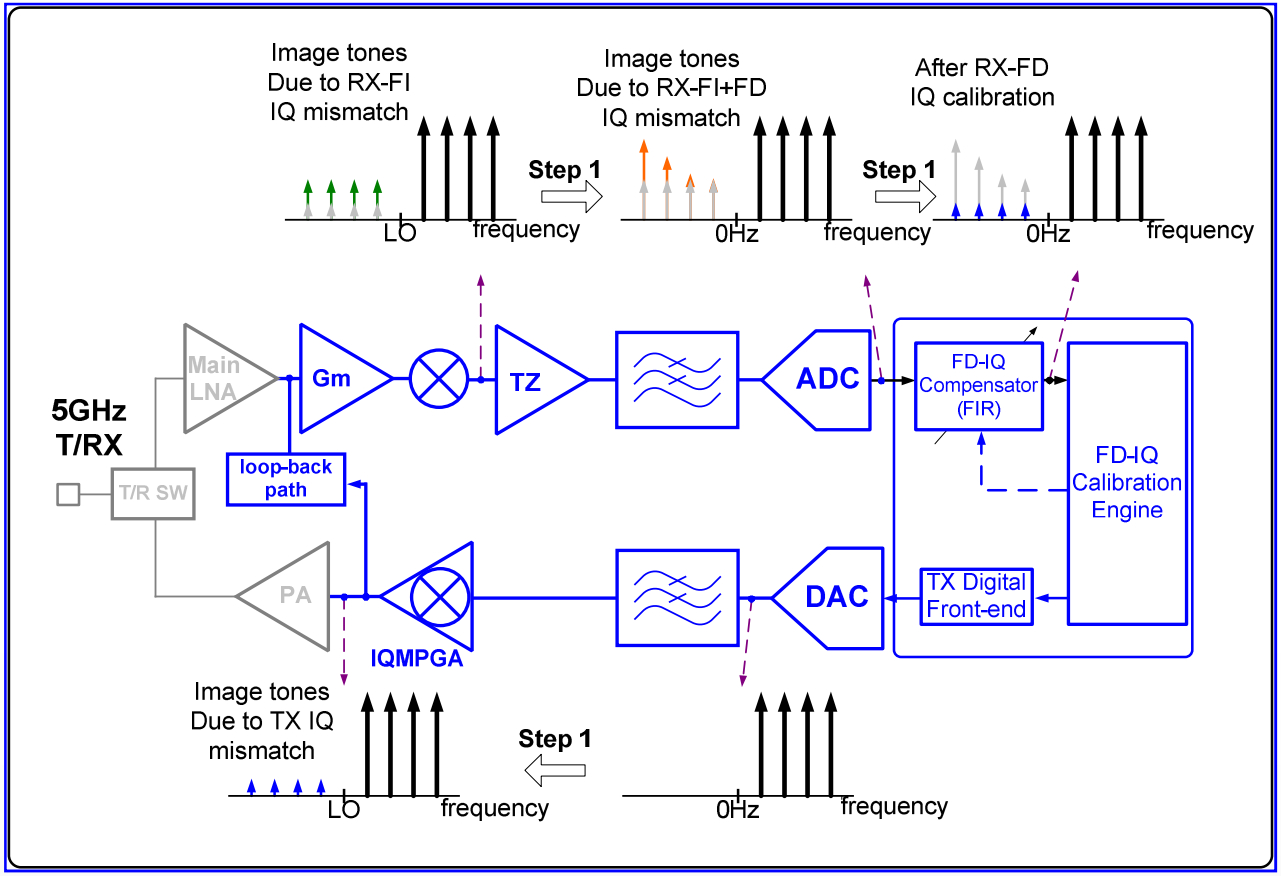
- TX mode: S1, S2 = short
- C2 and L1 form a parallel resonance to mitigate TX loading effect
- C2 over C1 ratio is chosen for attenuation at node N1 and attenuation by switch S2 to protect the LNA transistor

RX Analog Baseband



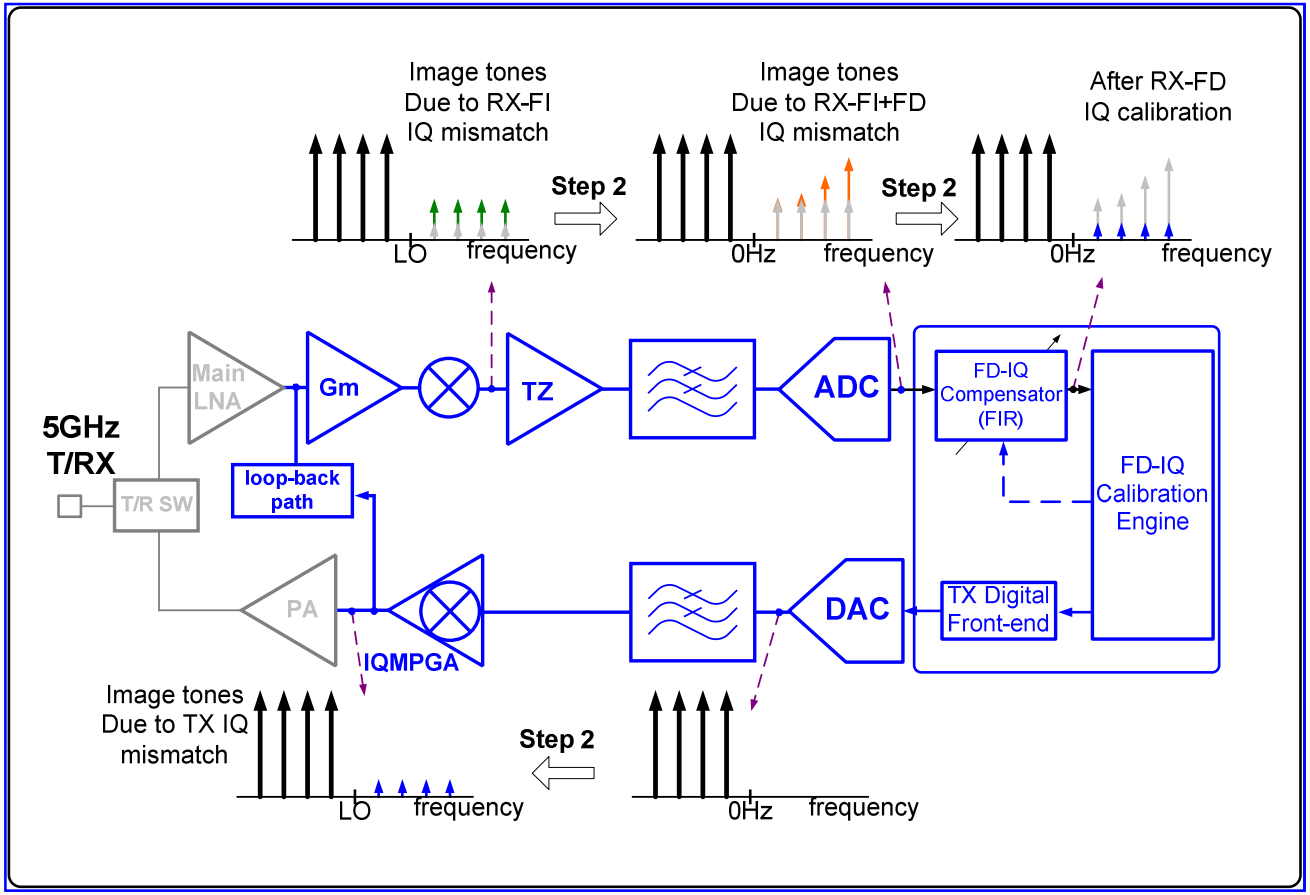
- 3rd order Chebyshev low-pass filter for adjacent and alternative-adjacent channel rejection
- Residue DC offset of LPF output is less than 50mV after IDAC compensation
- A RSSI is used for wide-band blocker power level detection

RX FD-IQ Calibration (Step 1)



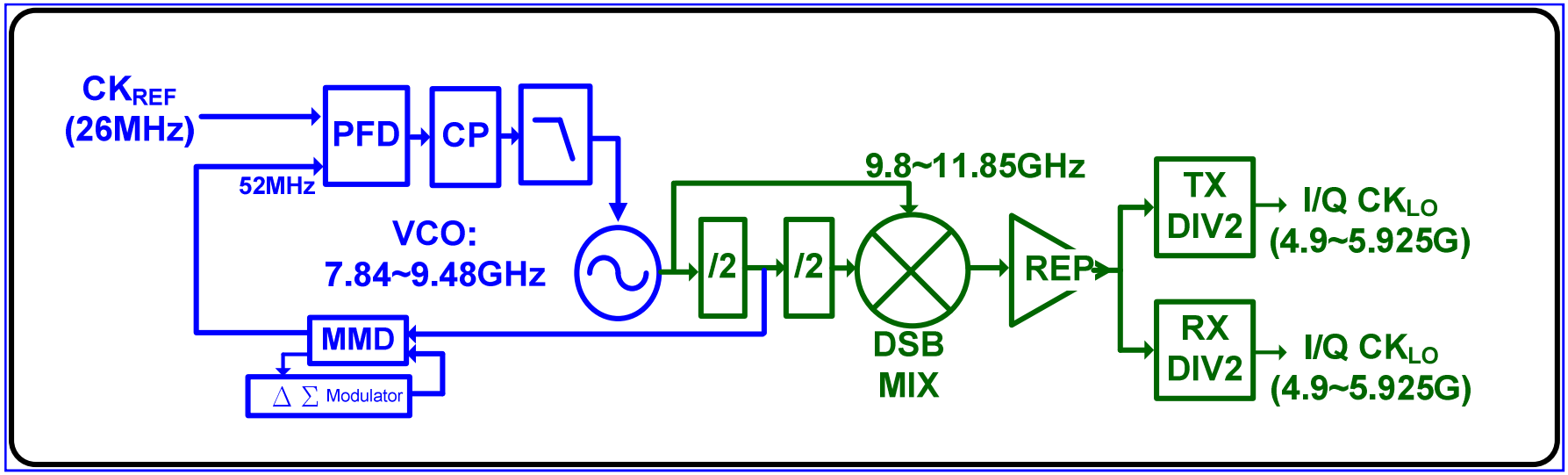
- The TX sends the multi-tone signals and loop-back to the RX.
- The frequency domain IQ imbalance compensation coefficients of each tone are derived by calculating the magnitude and phase error of their corresponding image tones.

RX FD-IQ Calibration (Step 2)



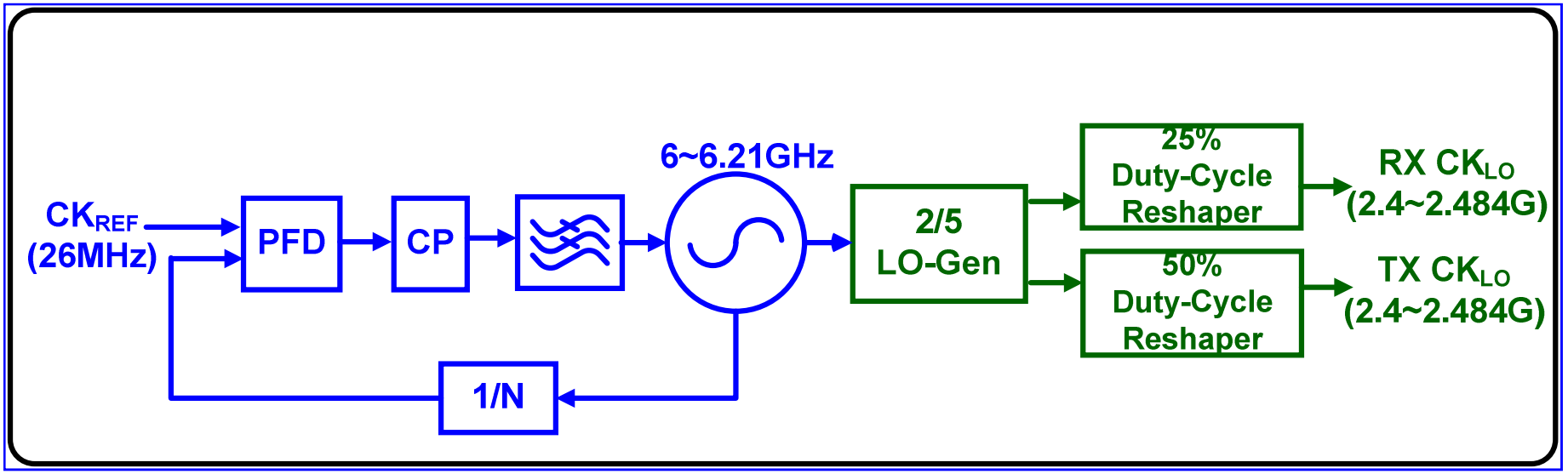
- TX sends the multi-tone signals " below" the LO frequency in step 2 and also loop back to RX to complete whole signal BW FD-IQ calibration.

LO Generator in 5GHz



- FVCO=(8/5)*Flo, 2*LO frequency is synthesized by DSB MIXER
- Offset LO generator architecture is adopted to avoid PA harmonic pulling on VCO
- Integrated SX phase noise <0.4 degree from system analysis to achieve overall TX EVM performance better than -32dB

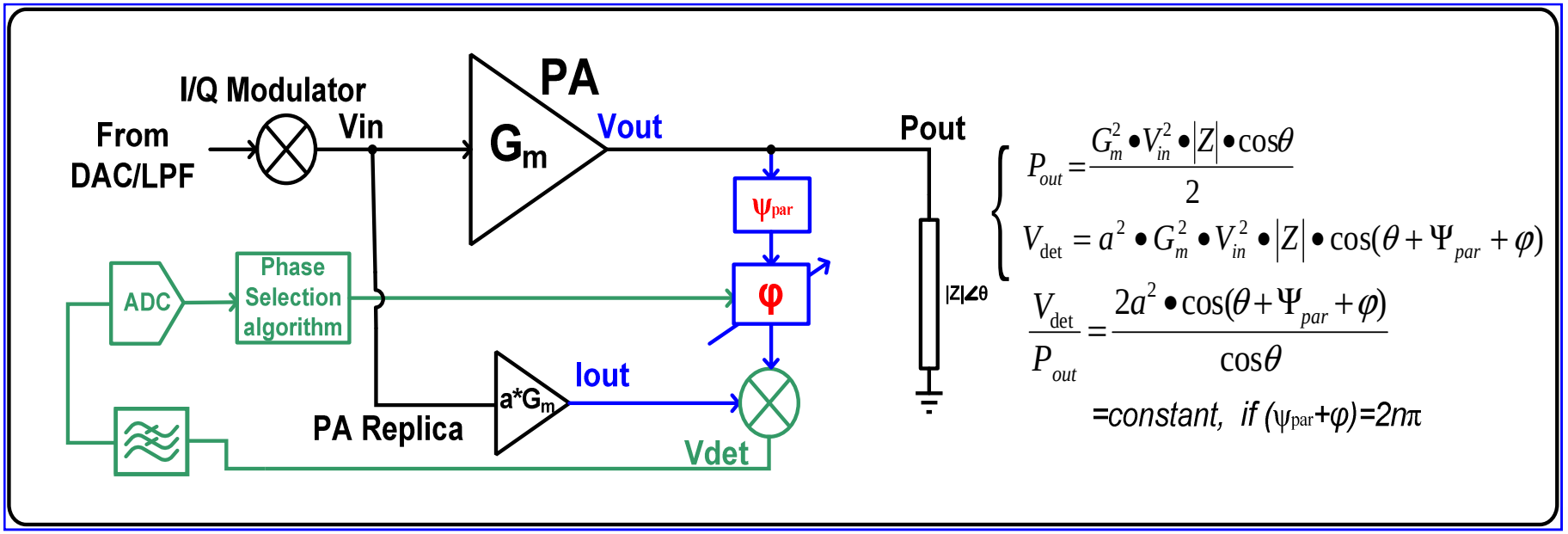
LO Generator in 2.4GHz



- FVCO=(5/2)*Flo, LO IQ signals are directly produced by 2/5 divider
- Inductor-less LO generator circuit design saves both current and die area

[8]Y-L Hsueh et al., "A 0.29mm^2 Frequency Synthesizer in 40nm CMOS with 0.19psrms Jitter and <-100dBc Reference Spur for 802.11ac" *ISSCC Dig. Tech. Papers*, pp. 472-473, Feb. 2014.

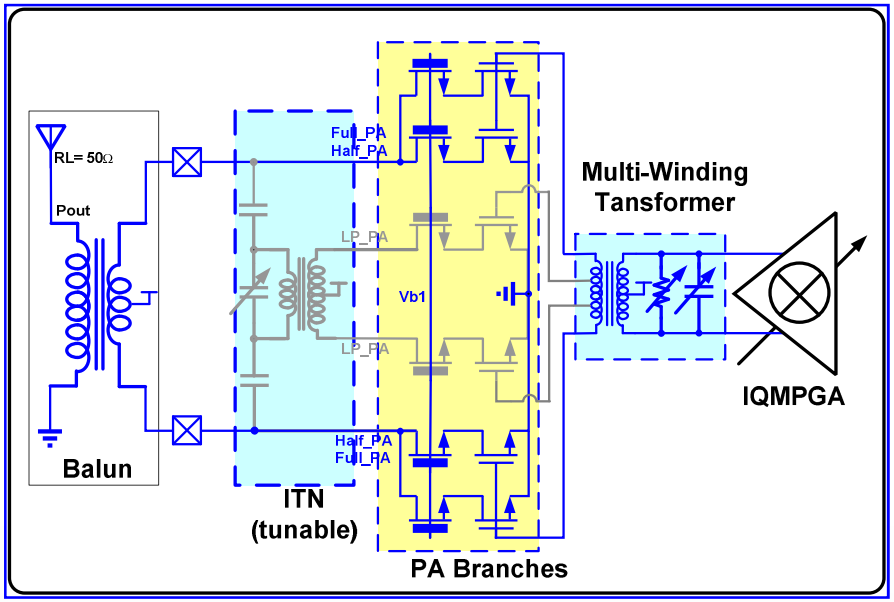
Phase Compensated Power Detector



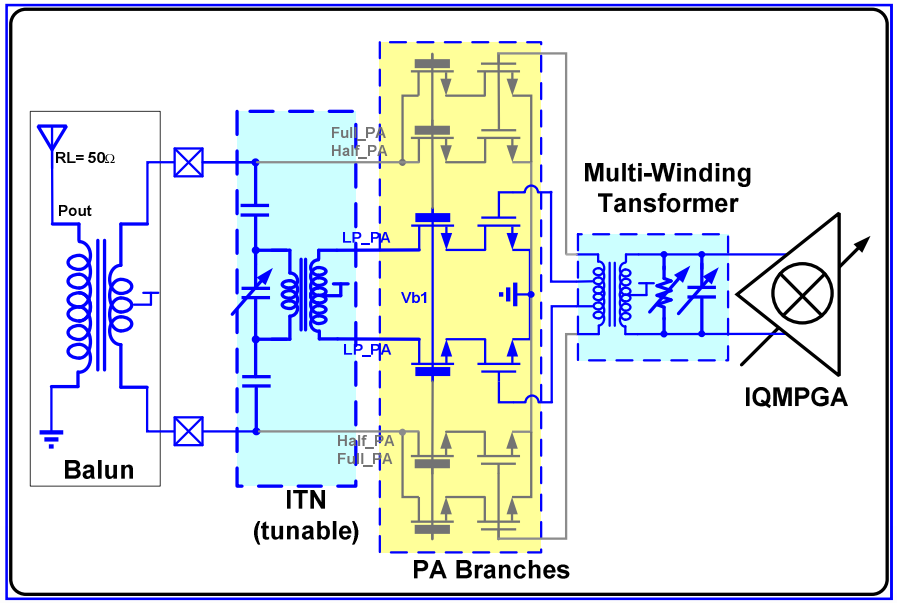
- True power detector by multiplying current (Iout) and voltage (Vout) to against antenna VSWR variation.
- Extra phase (ψ_{par})caused by the implementation parasitic can be compensated by proper phase (φ) insertion.

2.4GHz WiFi PA with Load-Line Adjustment

Full/Half-Power Mode



Low-Power Mode



- Full/Half-Power Modes with different PA branches, sharing the same PA output impedance (~35ohm) transformed from Balun. Psat of Full-Power PA is 28dBm.
- ITN(impedance tuning network) transforms the Balun output impedance to higher impedance (~200ohm) for Low-Power Mode. Psat of Low-Power PA is 15dBm.

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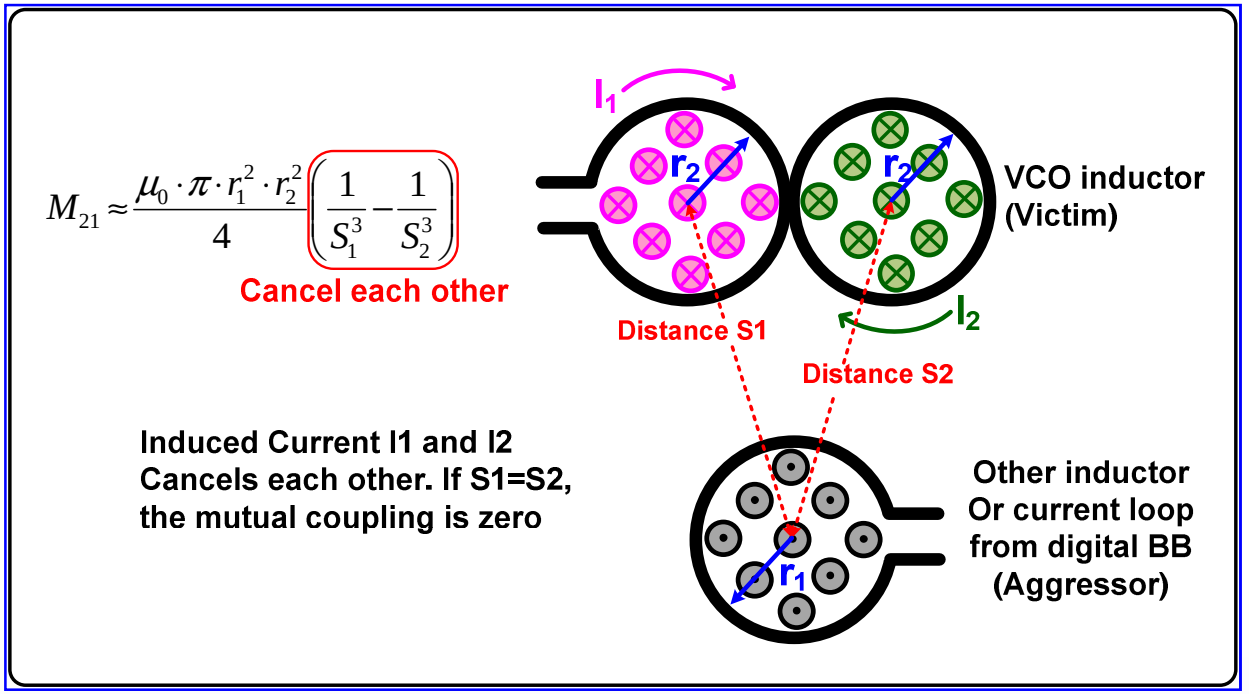
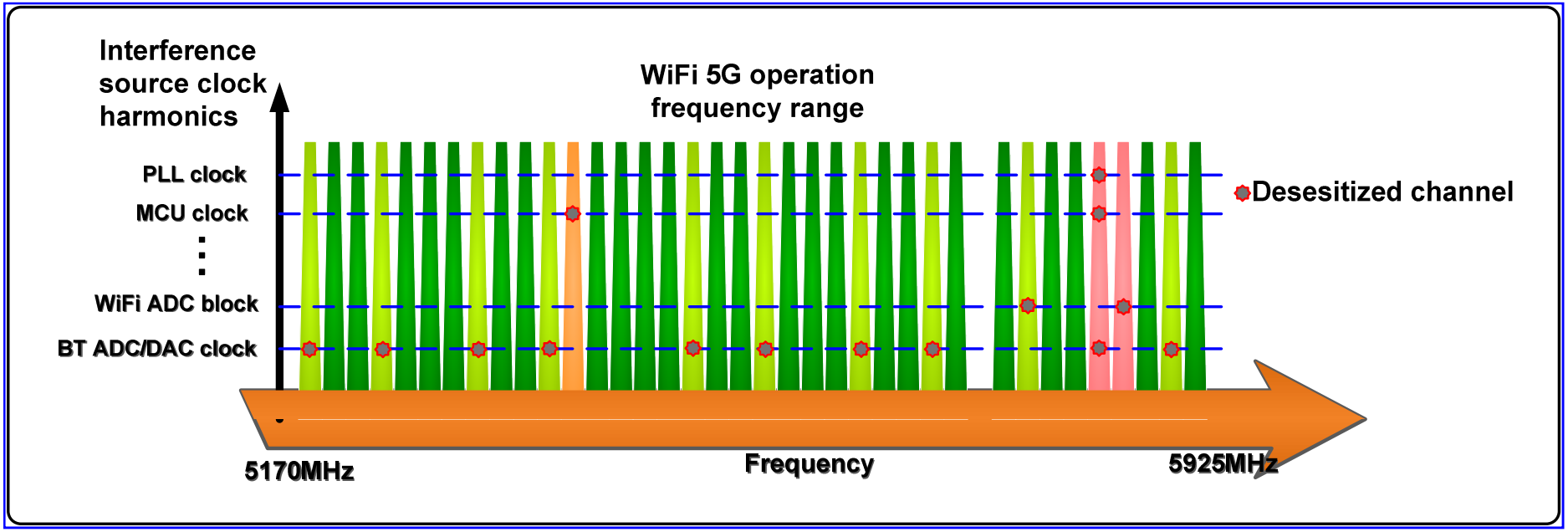
Field-cancelling Layout Topology for VCO inductor



- Field-cancelling layout topology is adopted in VCOs to mitigate mutual magnetic coupling among inductors.
- Assuming the distance S1、S2 are sufficiently larger than r1 、r2 radius, the mutual coupling to VCO inductor can be mitigated.

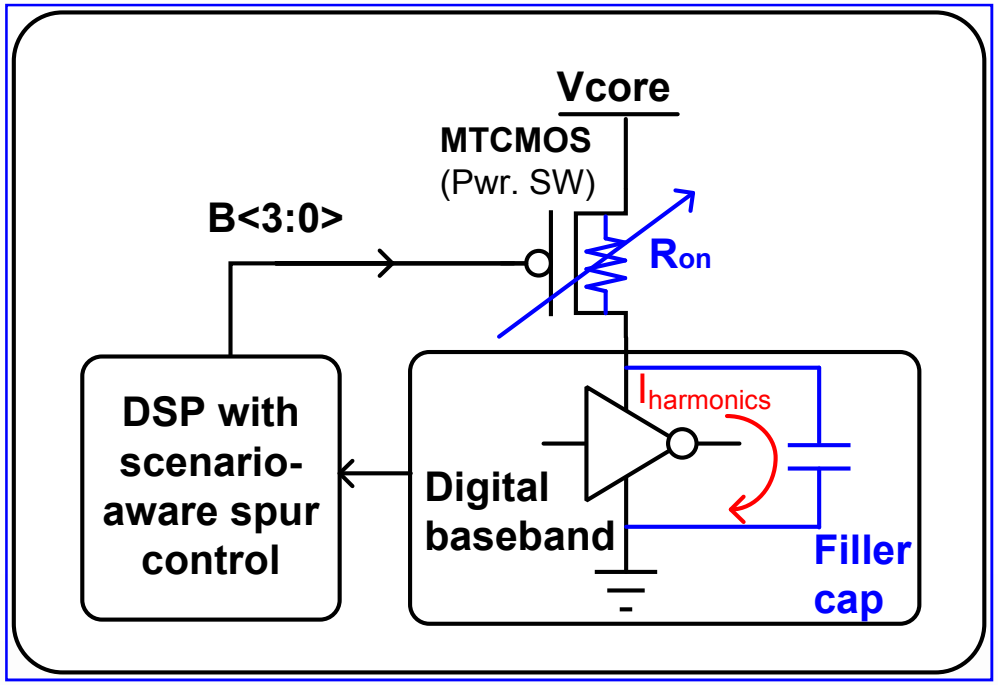
[8]Y-L Hsueh et al., "A 0.29mm^2 Frequency Synthesizer in 40nm CMOS with 0.19psrms Jitter and <-100dBc Reference Spur for 802.11ac" *ISSCC Dig. Tech. Papers*, pp. 472-473, Feb. 2014.

RX Desensitization



- Adaptive frequency selection in ADC/DAC, MCU, and PLL clock to avoid clock harmonics falling into desired channels
- Spread-spectrum clock (SSC) technique is used to reduce clock harmonics level around 20dB

Spurious Tone Reduction in Digital Baseband

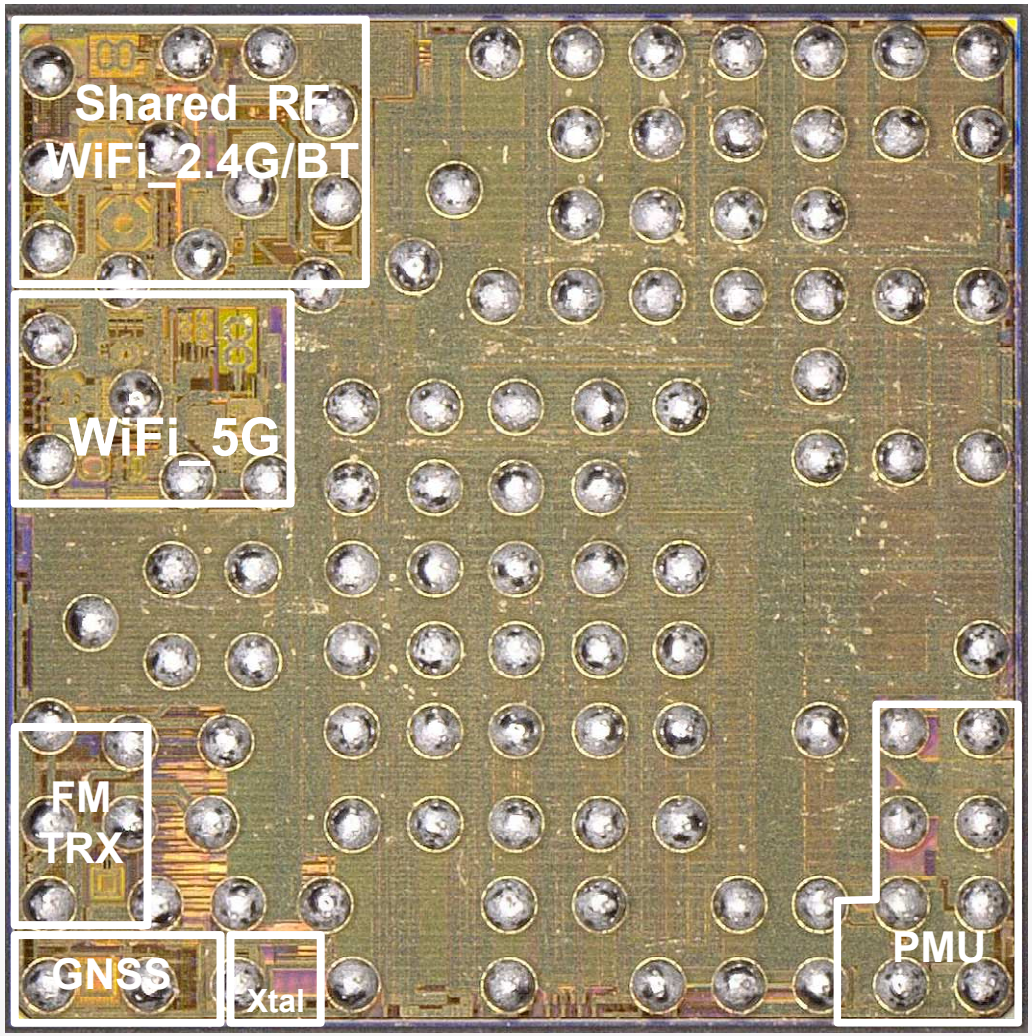


- An equivalent current-mode RC filter can be formed to localize the high-frequency spurious signals near the digital circuit itself

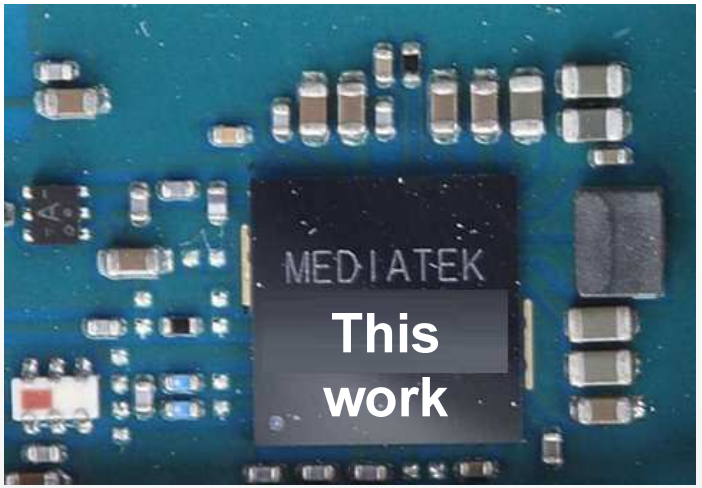
  where R → turn-on resistor of power switch.

  C → filler capacitor

Die Photo



- 1P6M 55nm CMOS process
- Whole chip : 24.9mm^2
  - 2.4G transceiver : 2.1mm^2
  - 5G transceiver : 1.3mm^2
- WLCSP:
  - 0.25mm bump diameter
  - 0.4mm bump pitch



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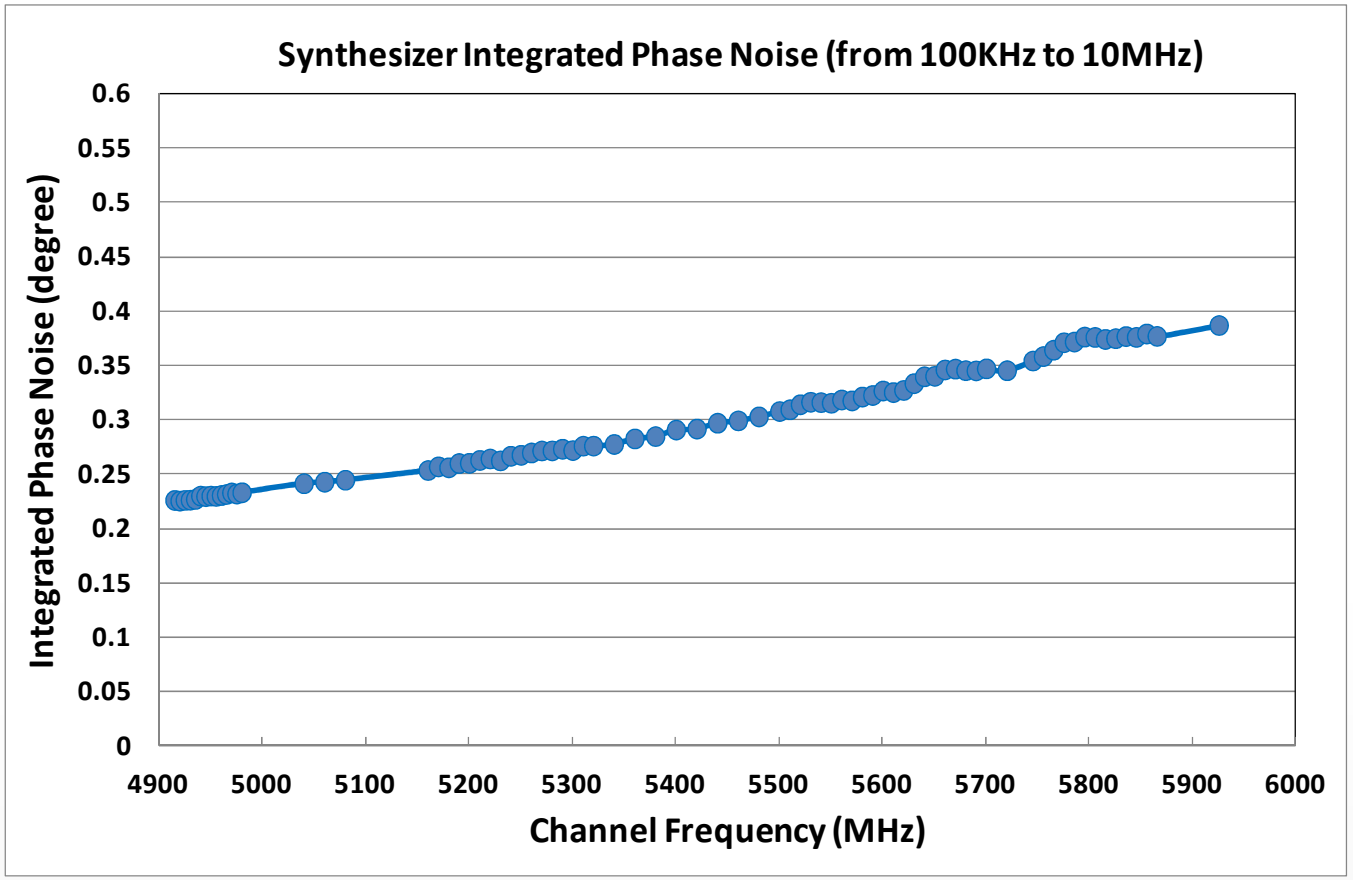
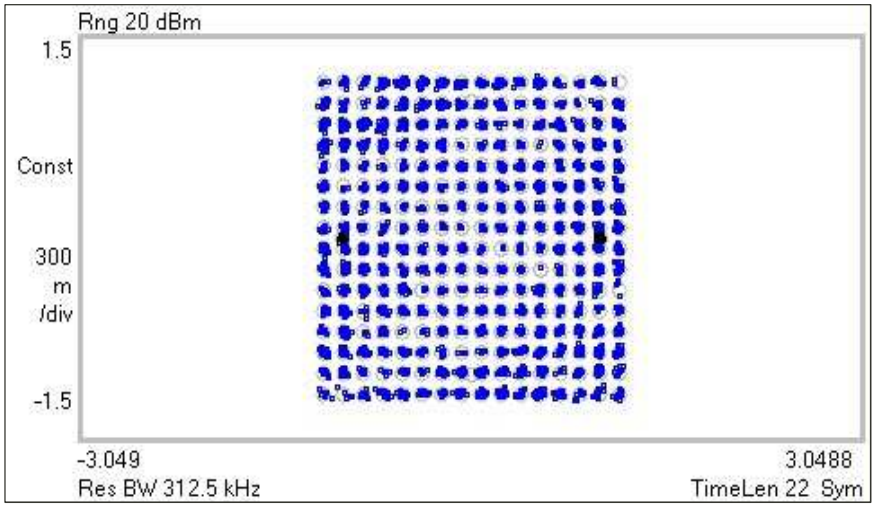
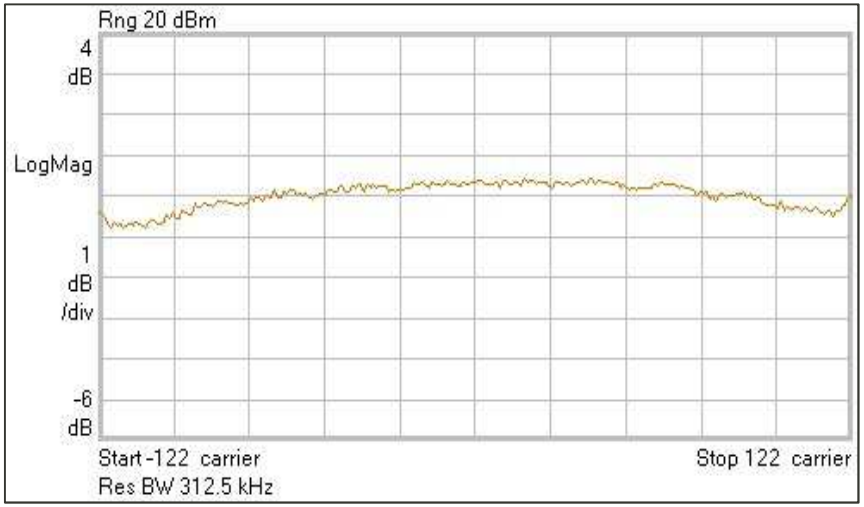
Measured SX Integrated Phase Noise

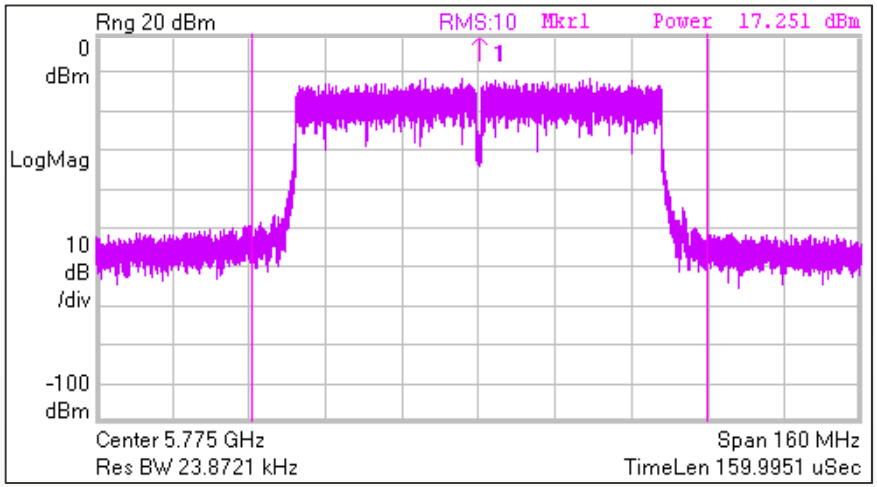


- 5GHz Wi-Fi SX Integrated PN from 100kHz to 10MHz is smaller than 0.4 degree.

Measured 256QAM TX Performance





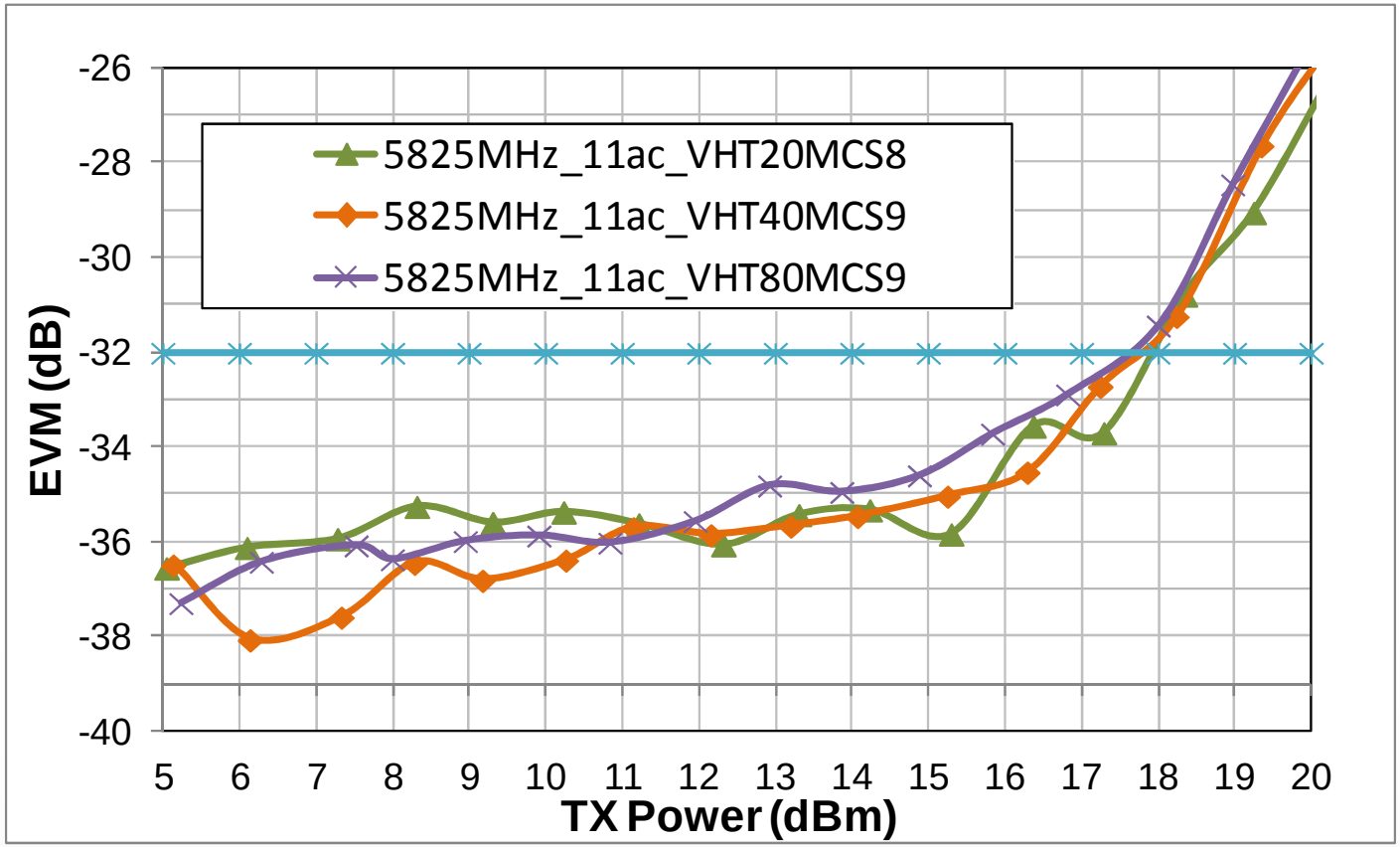


RMS:10

	Ch1	Ch2	Ch3	Ch4	Avg	
EVM	-32.719	***	***	***	-32.719	dB
EVMPeak	-22.143	***	***	***	-22.143	dB
PilotEVM	-34.38	***	***	***	-34.38	dB
DataEVM	-32.672	***	***	***	-32.672	dB
FreqErr	***	***	***	***	-6.2038	kHz
SymClkErr	***	***	***	***	-1.0921	ppm
CPE	***	***	***	***	1.1546	%rms
IQOffset	-46.384	***	***	***	-46.384	dB
IQQuadErr	-0.3102	***	***	***	-0.3102	deg
IQGainImb	-0.0137	***	***	***	-0.01372	dB
IQTimeSkew	-0.0206	***	***	***	-0.02068	ns
CrossPwr	***	***	***	***	***	
SyncCorr	0.95847	***	***	***	0.95847	

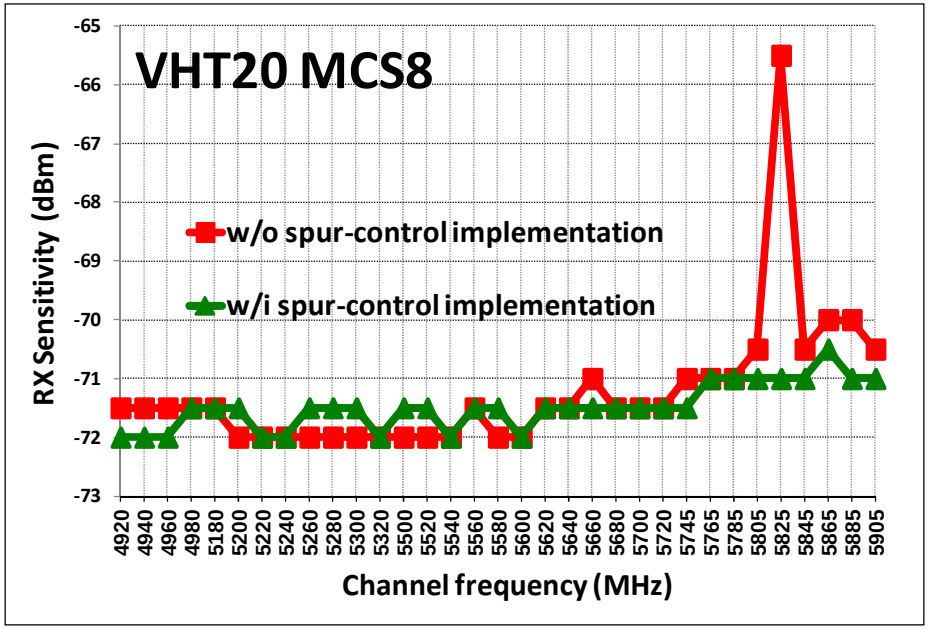
- EVM=-32.7dB@17.2dBm Pout, Channel=5.775GHz

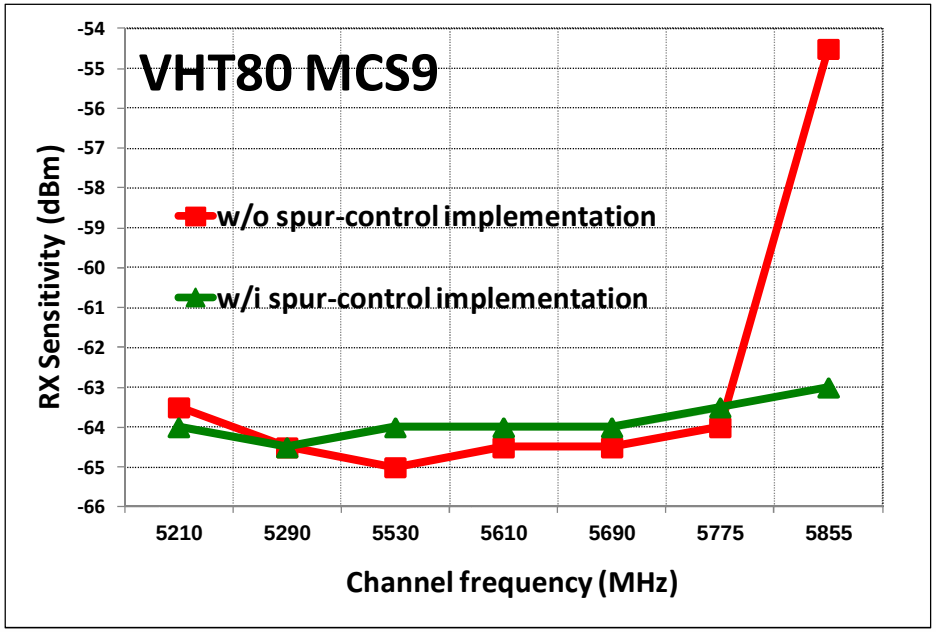
Wi-Fi 5G TX Performance



- The same EVM performances for different modulation scheme

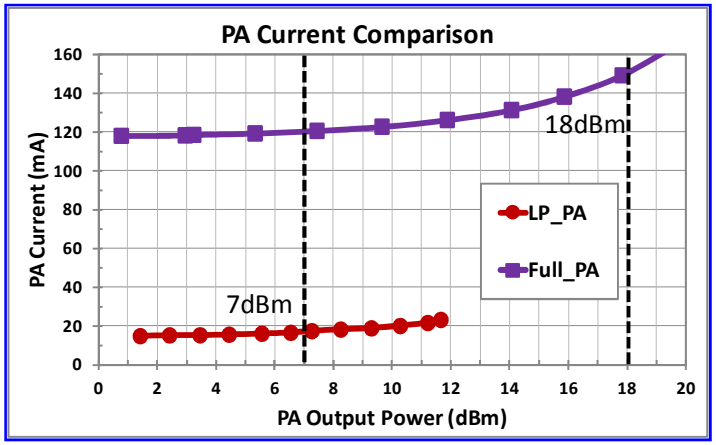
Wi-Fi 5GHz Measured RX Sensitivity

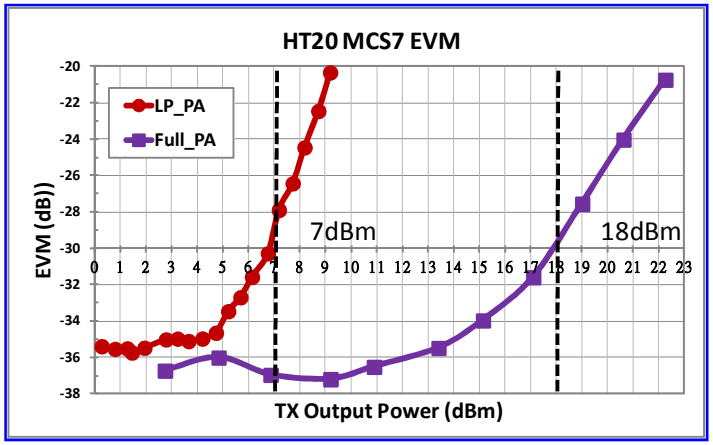


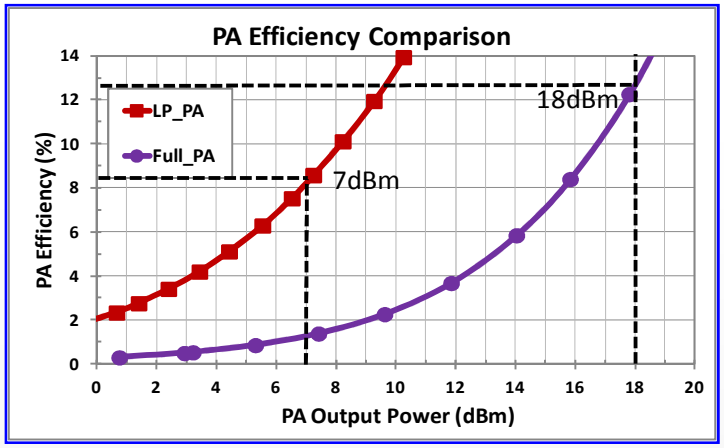


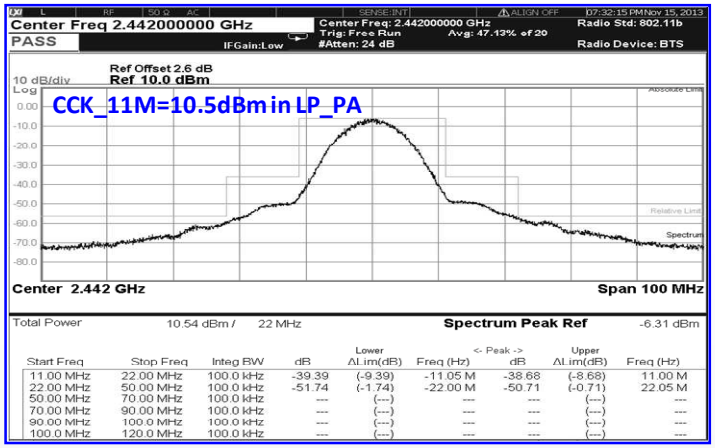
- 5GHz RX sensitivity is seriously degraded due to a spurious tone which is the 7th order harmonics of digital 832MHz clock.
- 5GHz VHT20 MCS8 and VHT80 MCS9 sensitivity can be improved 5.5dB and 8.5dB with spurious tone-control algorithm implementation

2.4GHz TX Performance Comparison in Full /Low-Power Modes









- 100mA current saving can be achieved at 7dBm by changing Full_PA mode to LP_PA mode under HT20 MCS7, EVM=-30dB.
- Efficiency degraded from 12.5% to 8.3% due to implementation loss

Comparison

		This work	ISSCC 2013 [10]	ISSCC 2014 [11]
Support WLAN standards		**1X1 11bgn +1X1 11ac**	2X2 11bgn +1X1 11a	4X4MIMO 11abgn/ac
Integrate PA, T/Rswitch,Balun	2.4GHz 5GHz	**Yes/Yes/No** **Yes/Yes/Yes**	Yes/Yes/Yes Yes/No/Yes	No/No/No No/No/No
Int. LO PN (deg.)	2.4GHz 5GHz	**0.3** **0.37**	N/A 0.42	0.19 0.37
Chip-in RX NF (dB)	2.4GHz 5GHz	**4.2 (w/i SW)** **4.7 (w/i SW)**	4.2 (w/i SW) 4.2 (w/o SW)	3.0 (w/o SW) 4.3 (w/o SW)
Chip-in RX sensitivity (dBm)	2.4GHz,54Mbps 5GHz,54Mbps 5GHz,11ac VHT80MCS9	**-77.5** **-77** **-63.5**	-78 -78 N/A	N/A N/A N/A
TX Pout(dBm) @EVM=-25/-32dB For 54Mbps/11ac	2.4GHz,54Mbps 5GHz,54Mbps 5GHz,11ac VHT80MCS9	**20.5** **20.0** **17.8**	20.5 17.3 N/A	-5 N/A -5
Technology		**55 nm**	45nm	40nm
WiFi RF+Analog Die Area(mm^2)		**3.4**(1x1) (*1)	3.8(1x2 in 5GHz)	21.5(4x4)

[10] R. Kumar, et al. ISSCC, 2013.
[11] Ming He, et al. ISSCC, 2014.
(*1)Including BT RF area

Conclusion

- The FD-IQ compensation scheme is adopted in RX chain to compensate the FD-IQ mismatch in RXLPF
- The TX achieves 17.8dBm in VHT80 256QAM with the proposed TX architecture and wide BW adaptive bias for the PA.
- Proposed Wi-Fi PA with load-line adjustment to maintain power efficiency, covering 7dBm~21dBm wide output power range.
- Proposed spurious tone reduction method is implemented in SoC for improving de-sensitization.

Acknowledgement

Thanks to all Mediatek teams who supported this work

Special thanks to RF, WCN and CSD.