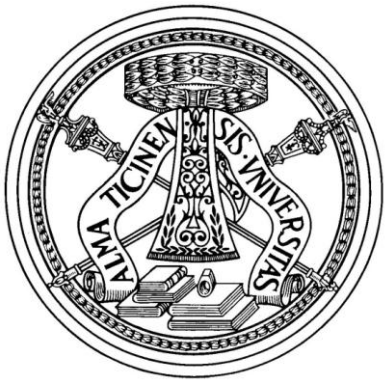
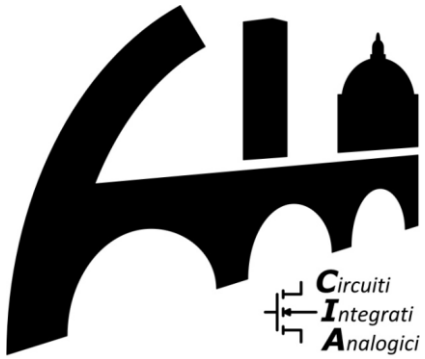
# A 15 GHz Bandwidth 20 dBm $P_{SAT}$ Power Amplifier with 22% PAE in 65 nm CMOS

Junlei Zhao, Matteo Bassi, Andrea Mazzanti and Francesco Svelto



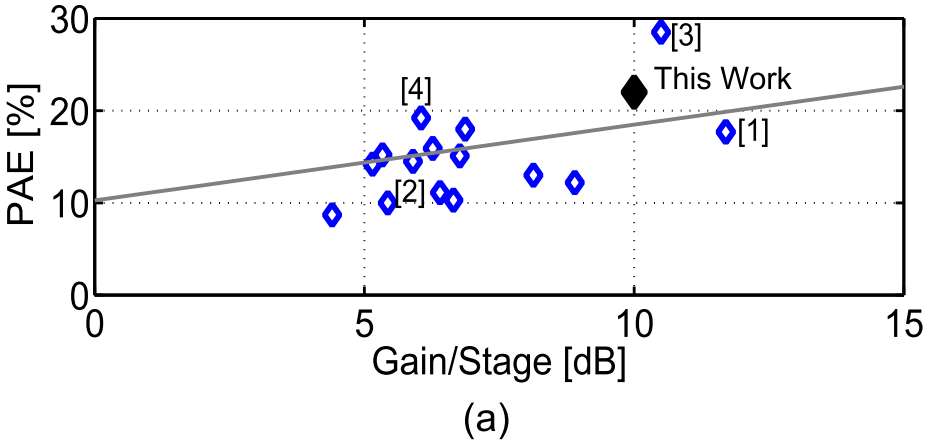

University of Pavia, Italy

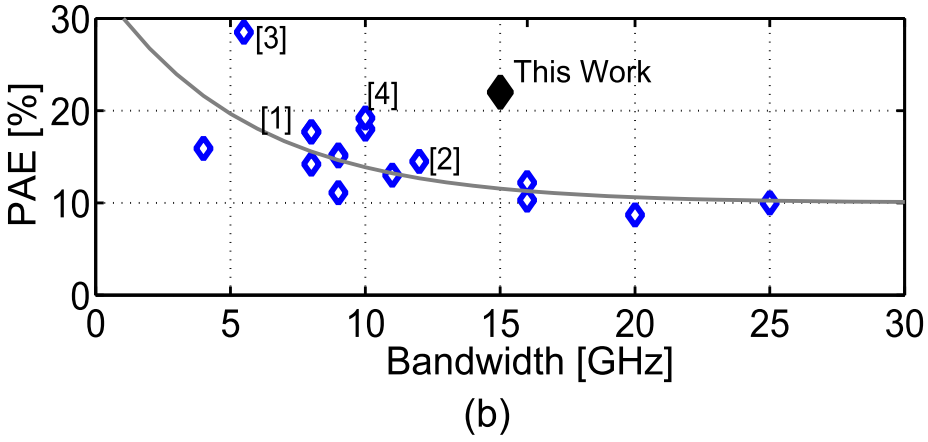


# Outline

- Wideband Power Amplifier Design Challenges
- Coupled Resonators to Improve GBW
- Wideband Power Combining/Splitting
- Circuit Design and Measurement
- Conclusions

# Wideband Power Amplifier Design Challenges



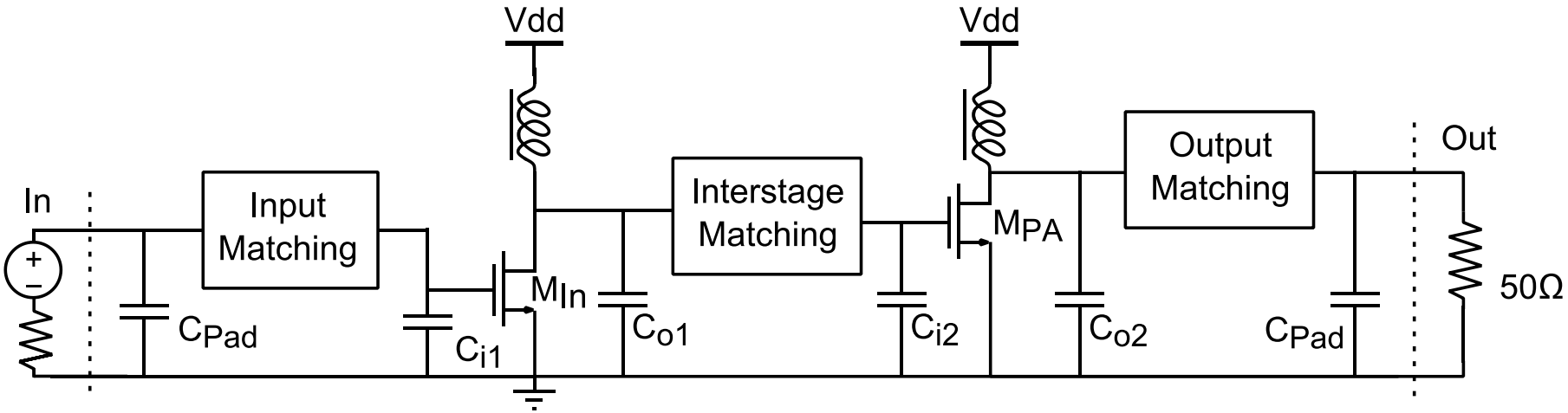




- High efficiency requires high gain

$$PAE = \frac{P_{Out} - P_{In}}{P_{DC}} = \frac{P_{Out}}{P_{DC}}\left(1 - \frac{1}{G}\right)$$

- Bandwidth trades with gain and efficiency
- Improving GBW is the key to achieve high efficiency over large bandwidth

# GBW of Power Amplifiers

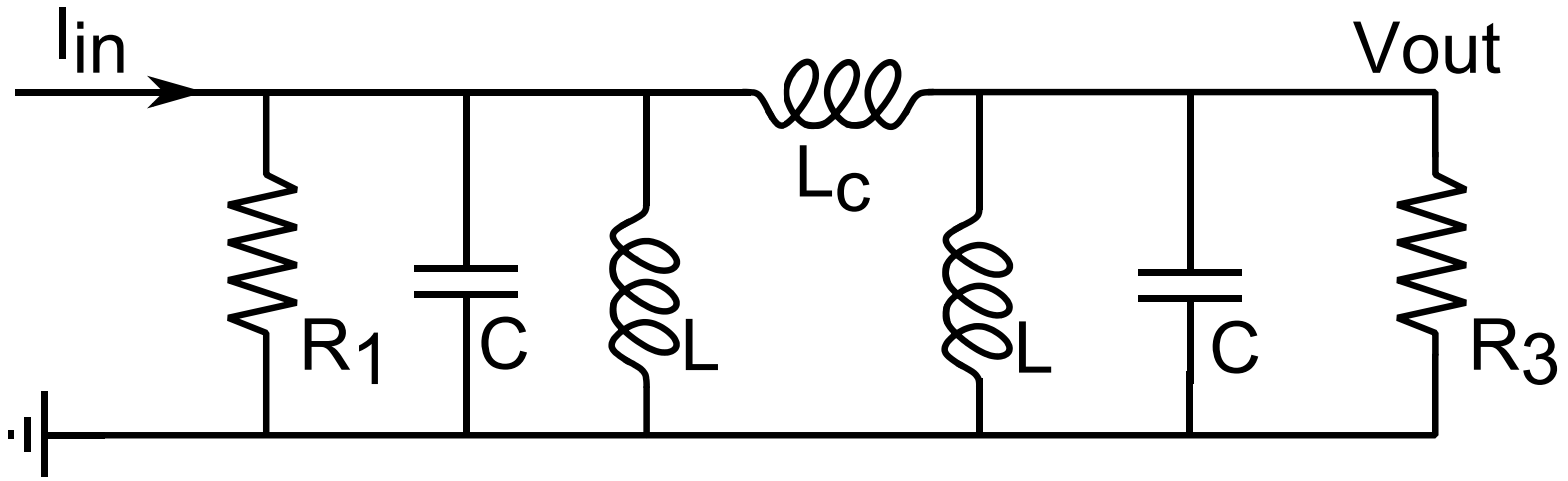



- Active devices
  - Maximum gain is limited by technology
  - Class AB biasing further reduces gain
  - Large layouts determine significant parasitics
- Passive matching networks
  - High-order networks can enhance GBW
  - Compact layout to minimize loss

# Outline

- Wideband Power Amplifier Design Challenges
- Coupled Resonators to Improve GBW
- Wideband Power Combining/Splitting
- Circuit Design and Measurement
- Conclusions

# Coupled Resonators

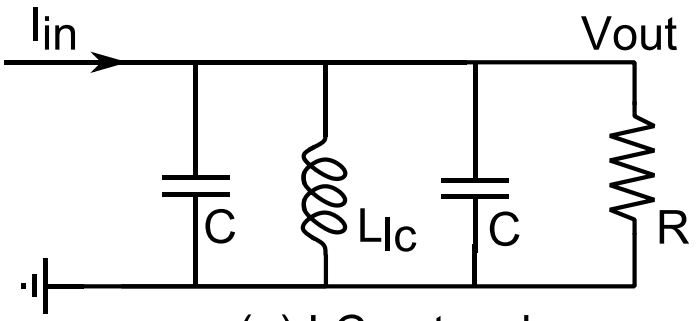



- Simple topology and low loss
- Two peaking frequencies:

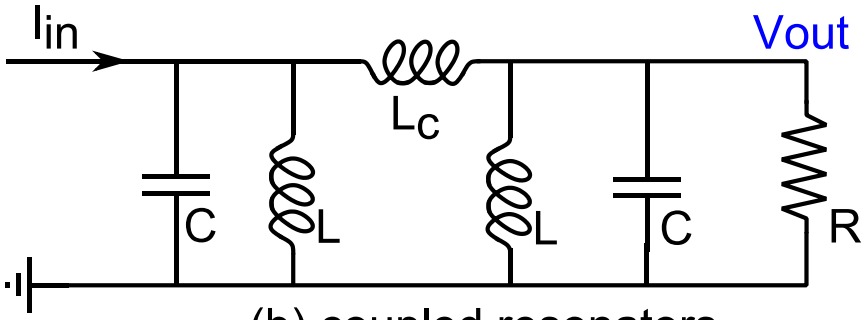
$$\omega_L \approx \frac{1}{\sqrt{LC}}, \quad \omega_H \approx \sqrt{1+2\frac{L}{L_C}}\ \omega_L$$

- $L_C$ used to control the bandwidth

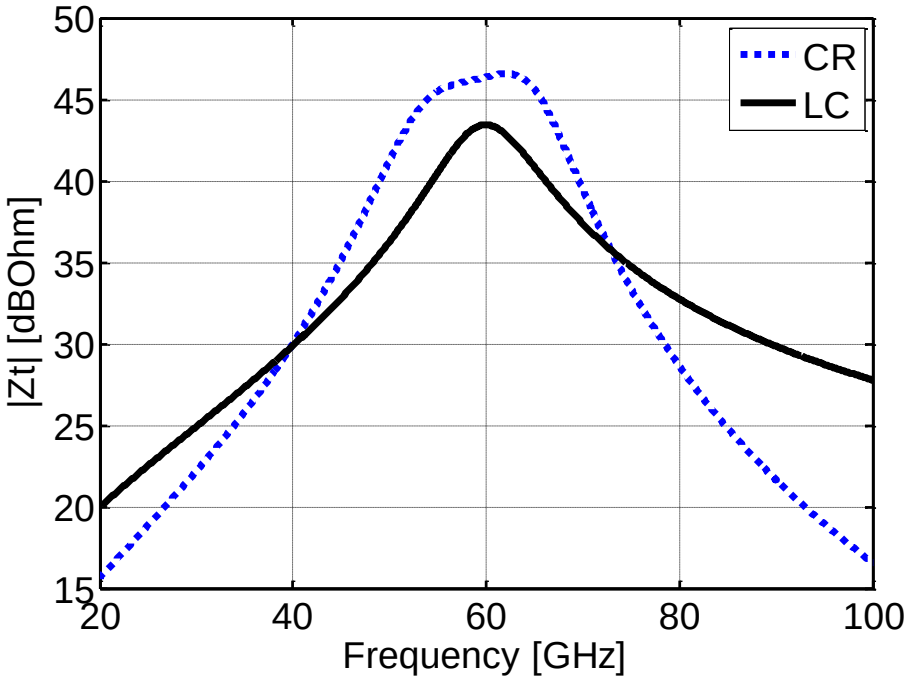
# GBW Enhancement




(a) LC network



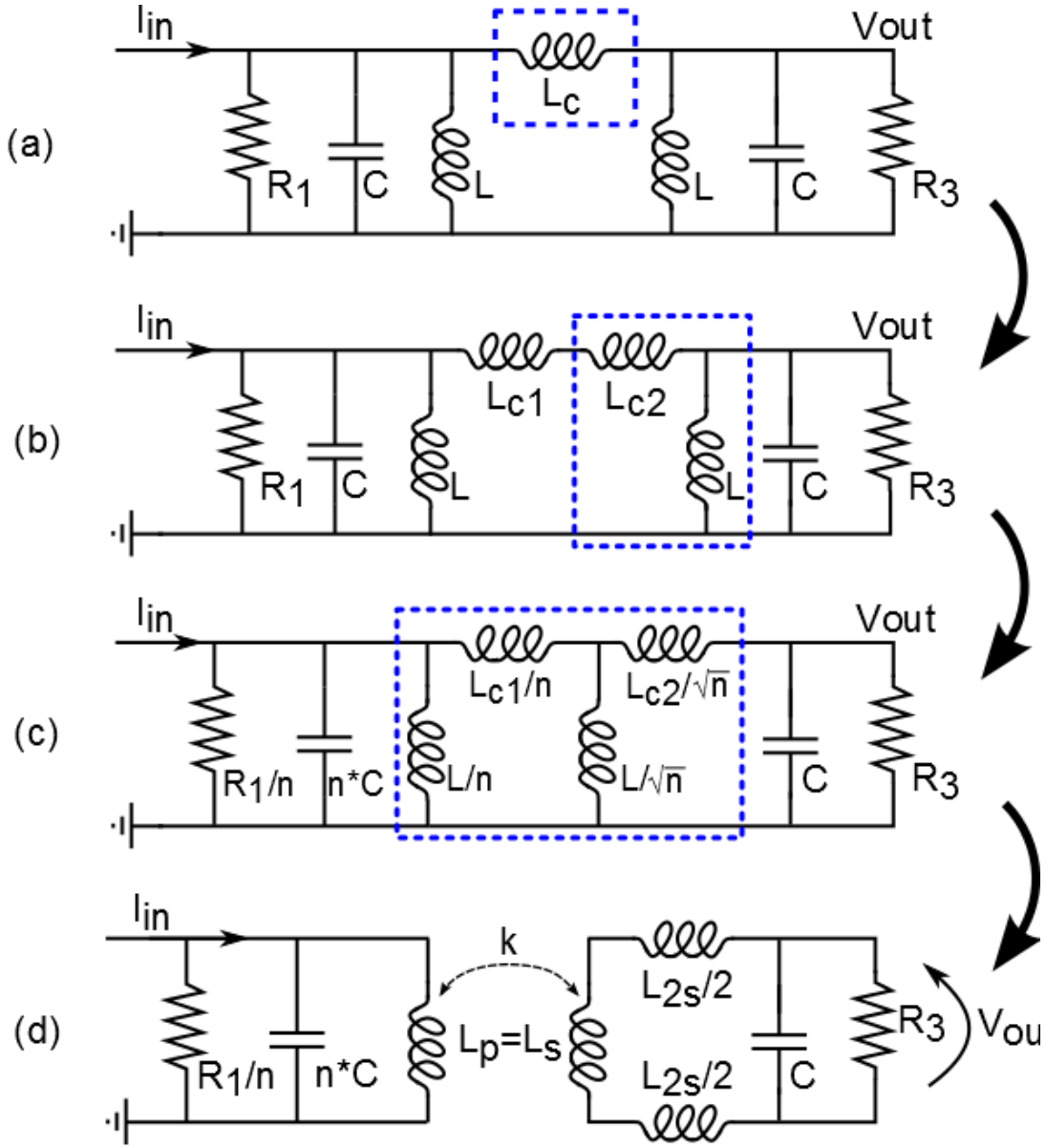

(b) coupled resonators




$$\left|Zt_{CR}\right| \approx \sqrt{2}\left|Zt_{LC}\right|, \quad BW_{CR} \approx \sqrt{2}BW_{LC}$$

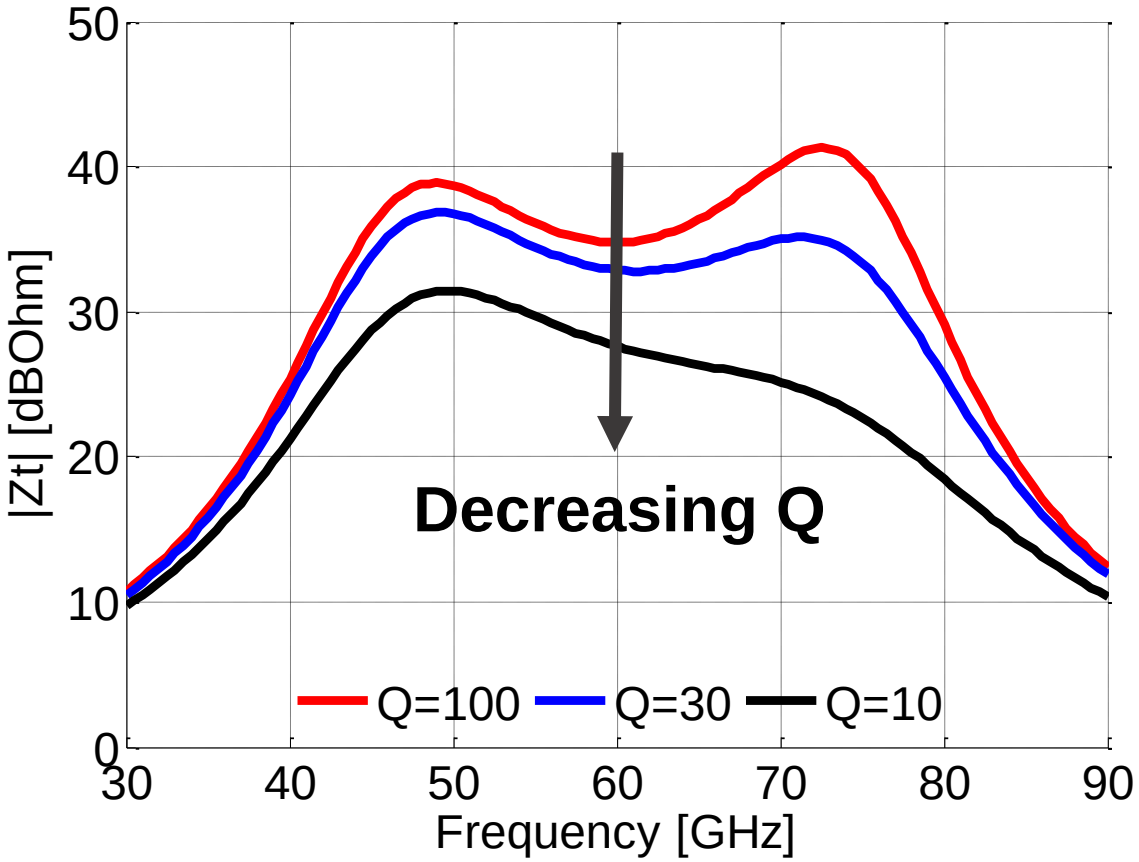
Coupled resonators allow 2x GBW enhancement (GBWEN)

# Transformation of Coupled Resonators



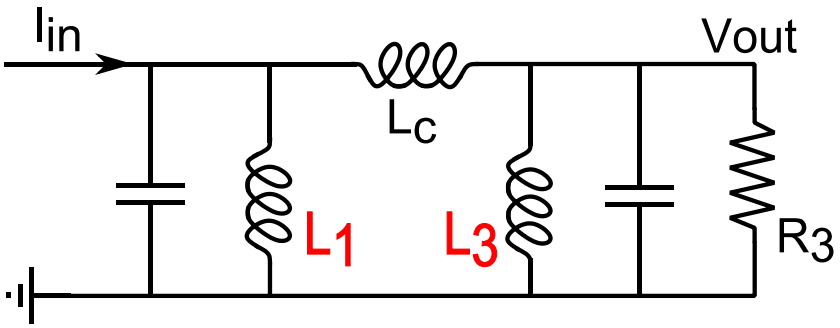

$$GBWEN = \frac{n+1}{\sqrt{n}} \geq 2$$

# Effect of Layout Parasitics

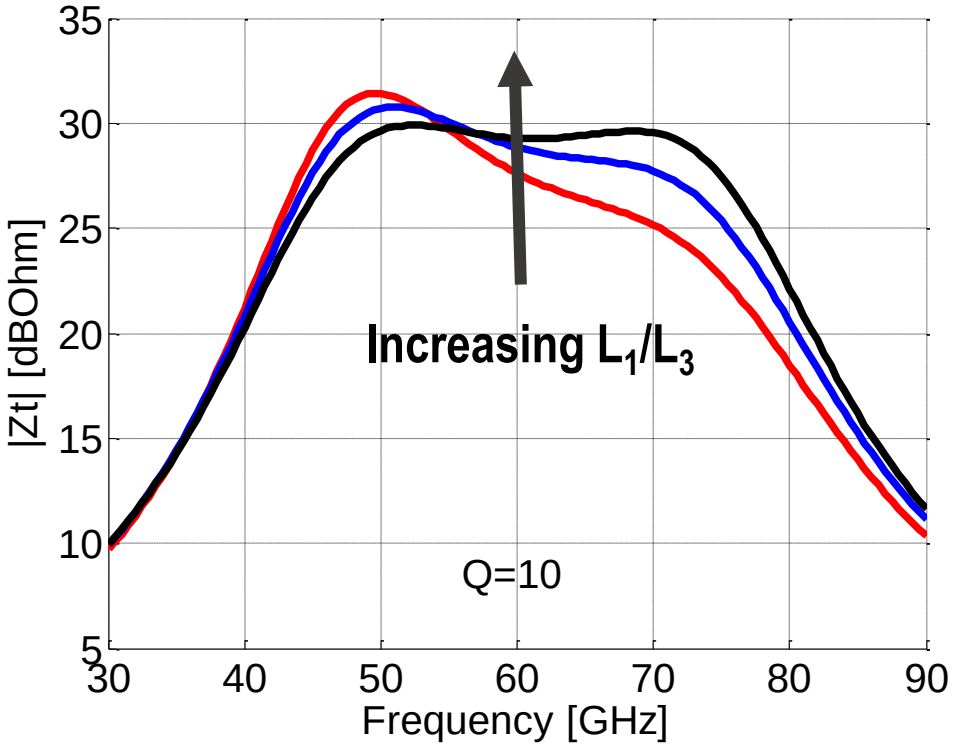



- Limited inductor Q leads to asymmetric response
- Network needs to be smart to accommodate parasitics

# Restoring Flat Response




$$\left|\frac{Z_T(\omega_H)}{Z_T(\omega_L)}\right| \approx \frac{L_1}{L_3}$$



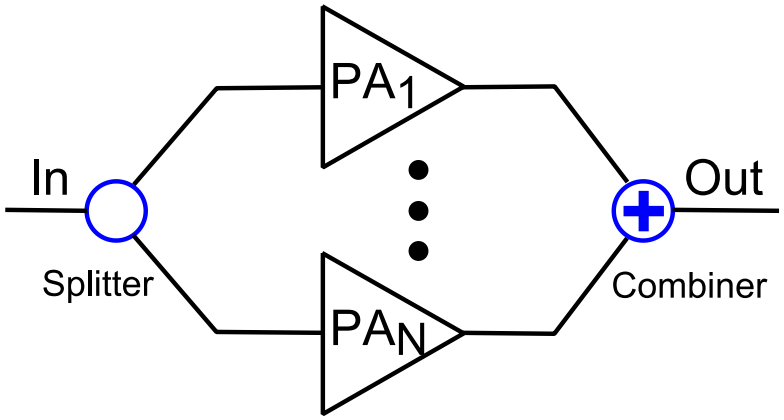

- Coupled resonator can be conveniently tuned to achieve flat response

# Outline

- Wideband Power Amplifier Design Challenges
- Coupled Resonators to Improve GBW
- Wideband Power Combining/Splitting
- Circuit Design and Measurement
- Conclusions

# Power Combing

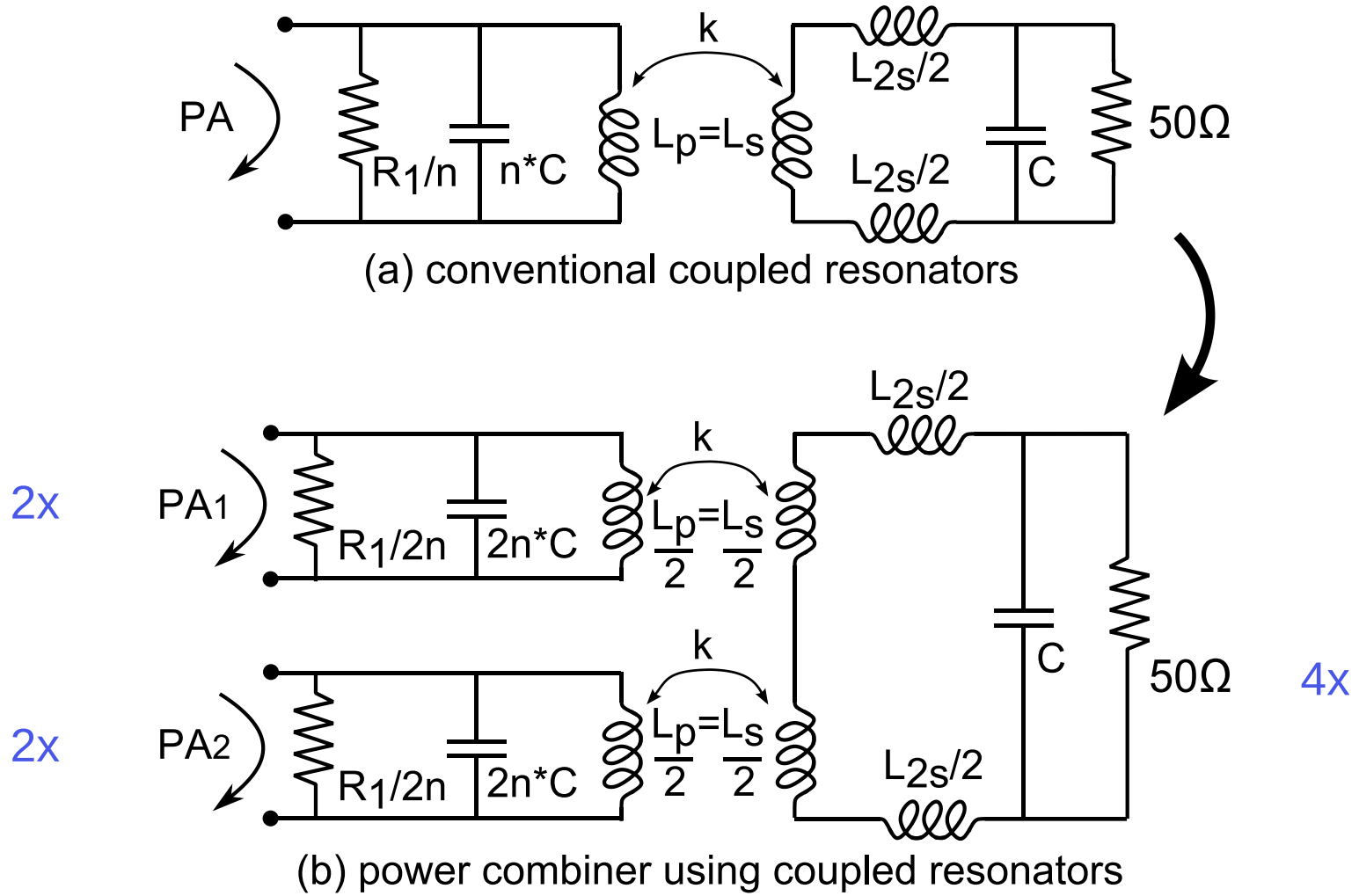
- Power combining is mandatory to achieve high Pout for CMOS PAs




- Transformer based combiner/splitter is popular
  - Compact size
  - Low insertion loss
  - Generally narrow bandwidth

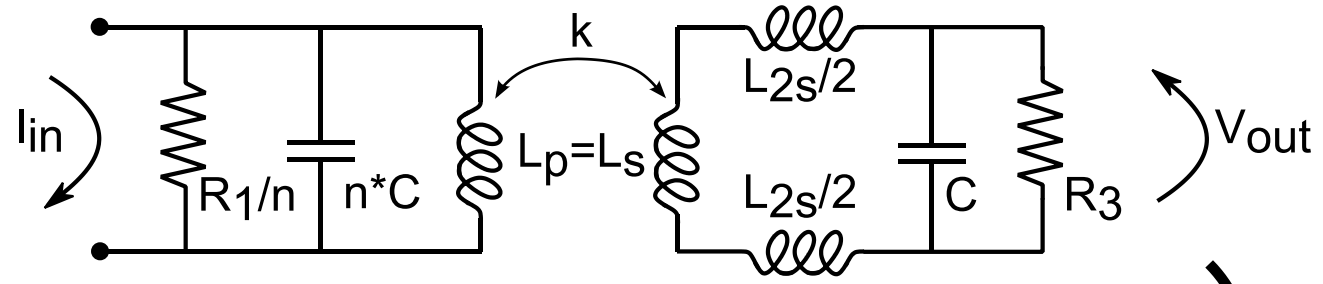
Wideband combining through coupled resonators

# Wideband Combiner

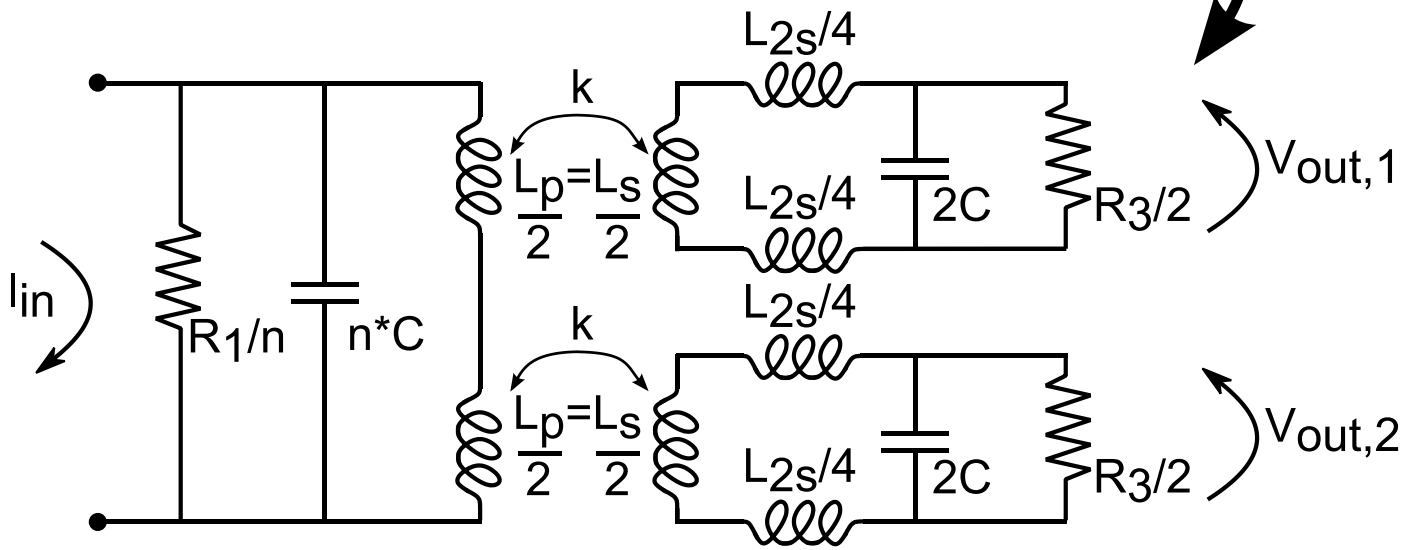



- Easy to transform
  - Divide the left network into two equal portions

# Wideband Splitter



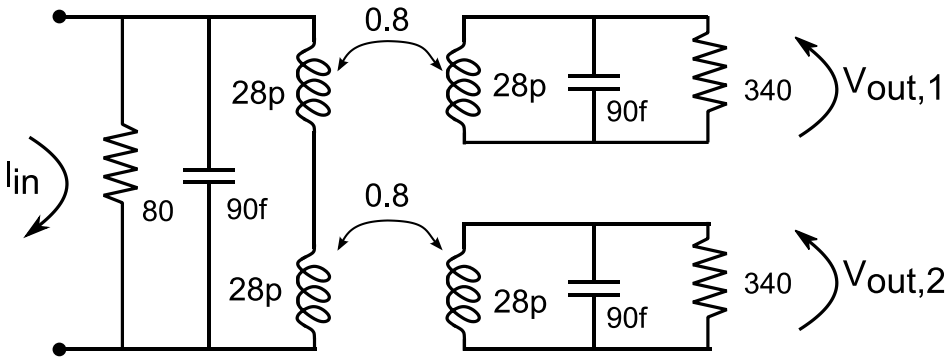

(a) conventional coupled resonators



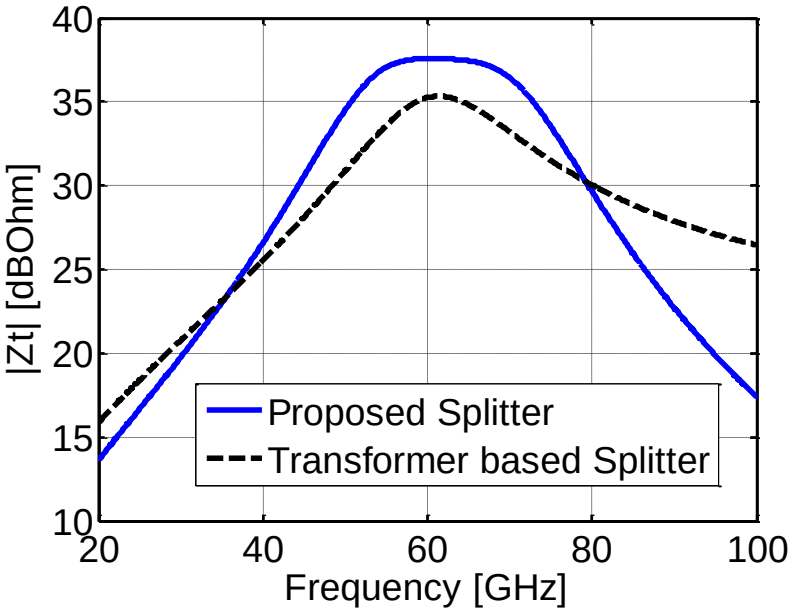

(b) power splitter using coupled resonators

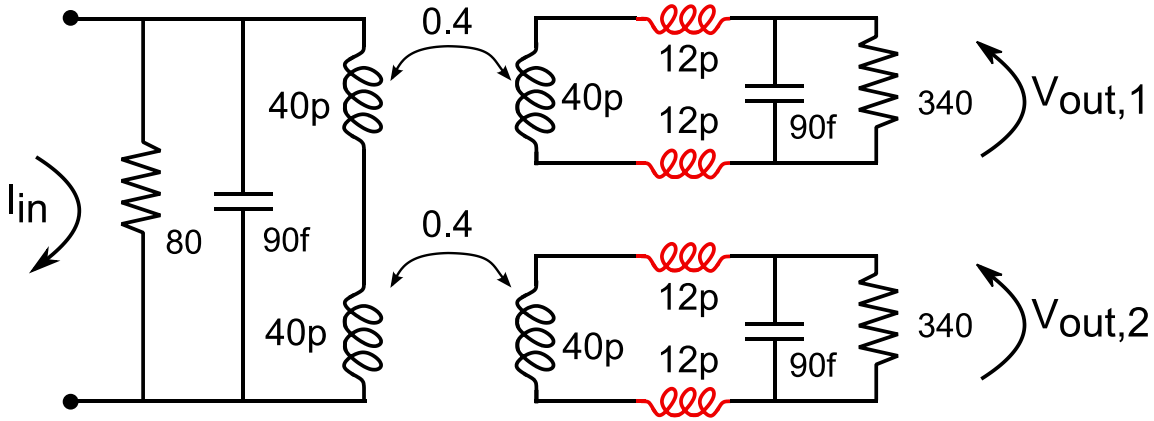
- Easy to transform
  - Divide the right network into two equal portions

# Comparison with Transformer Splitter




(a) transformer based splitter




(b) proposed splitter

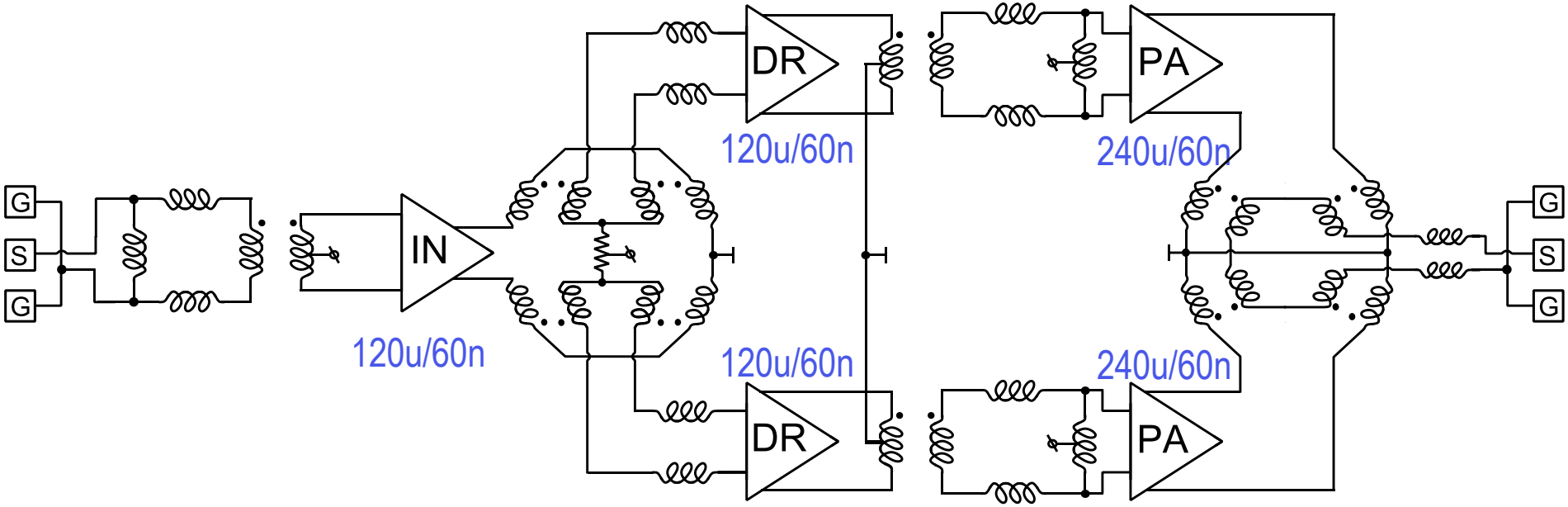
More than two times GBW enhancement.

# Outline

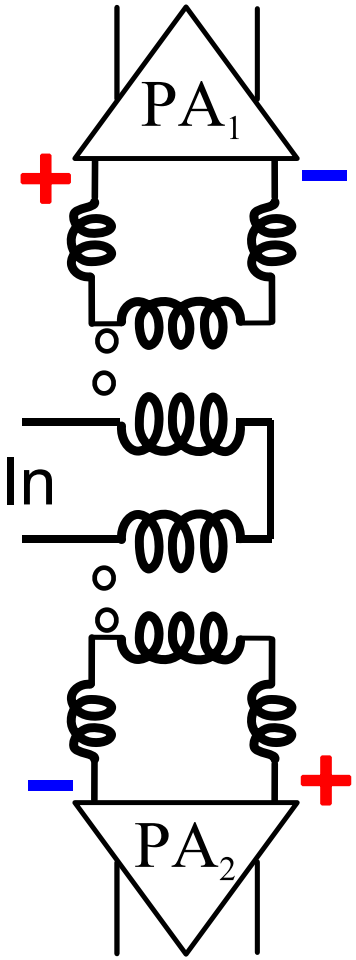
- Wideband Power Amplifier Design Challenges
- Coupled Resonators to Improve GBW
- Wideband Power Combining/Splitting
- Circuit Design and Measurement
- Conclusions

# PA Design

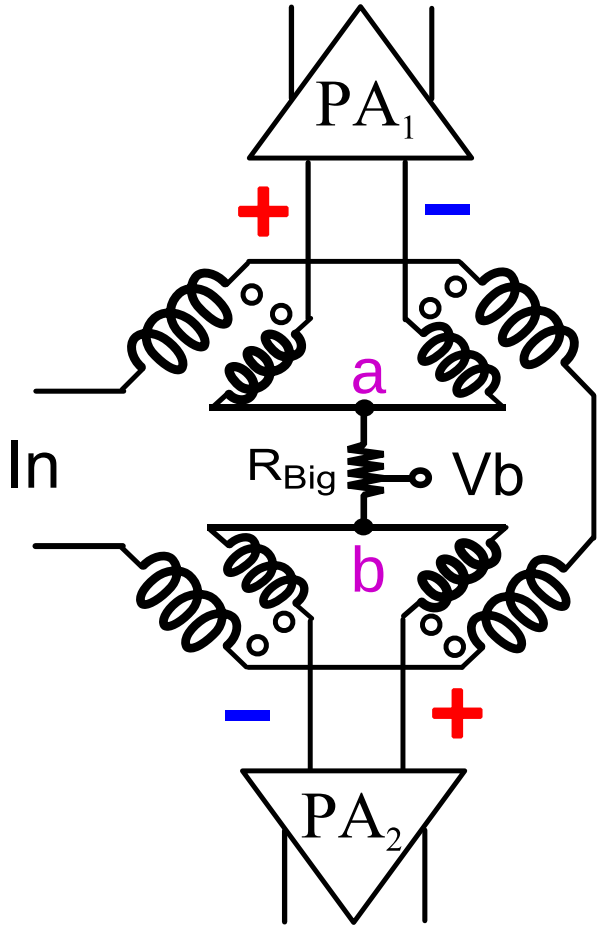
- A prototype has been designed in ST 65nm CMOS
  - Bandwidth >13 GHz
  - Gain > 25dB
  - P1dB > 15dBm
  - PAE > 20%



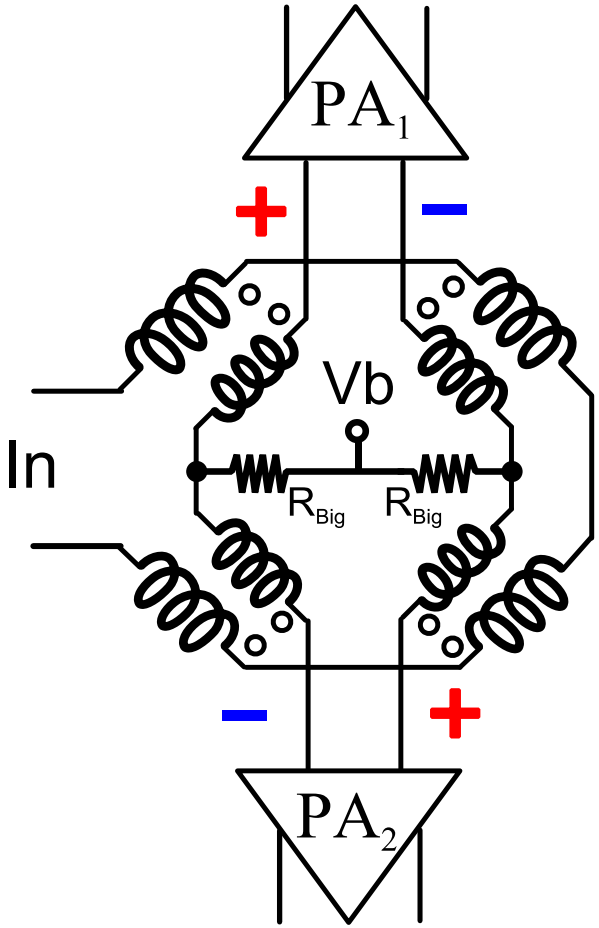
# Layout of Splitter




(a) splitter network



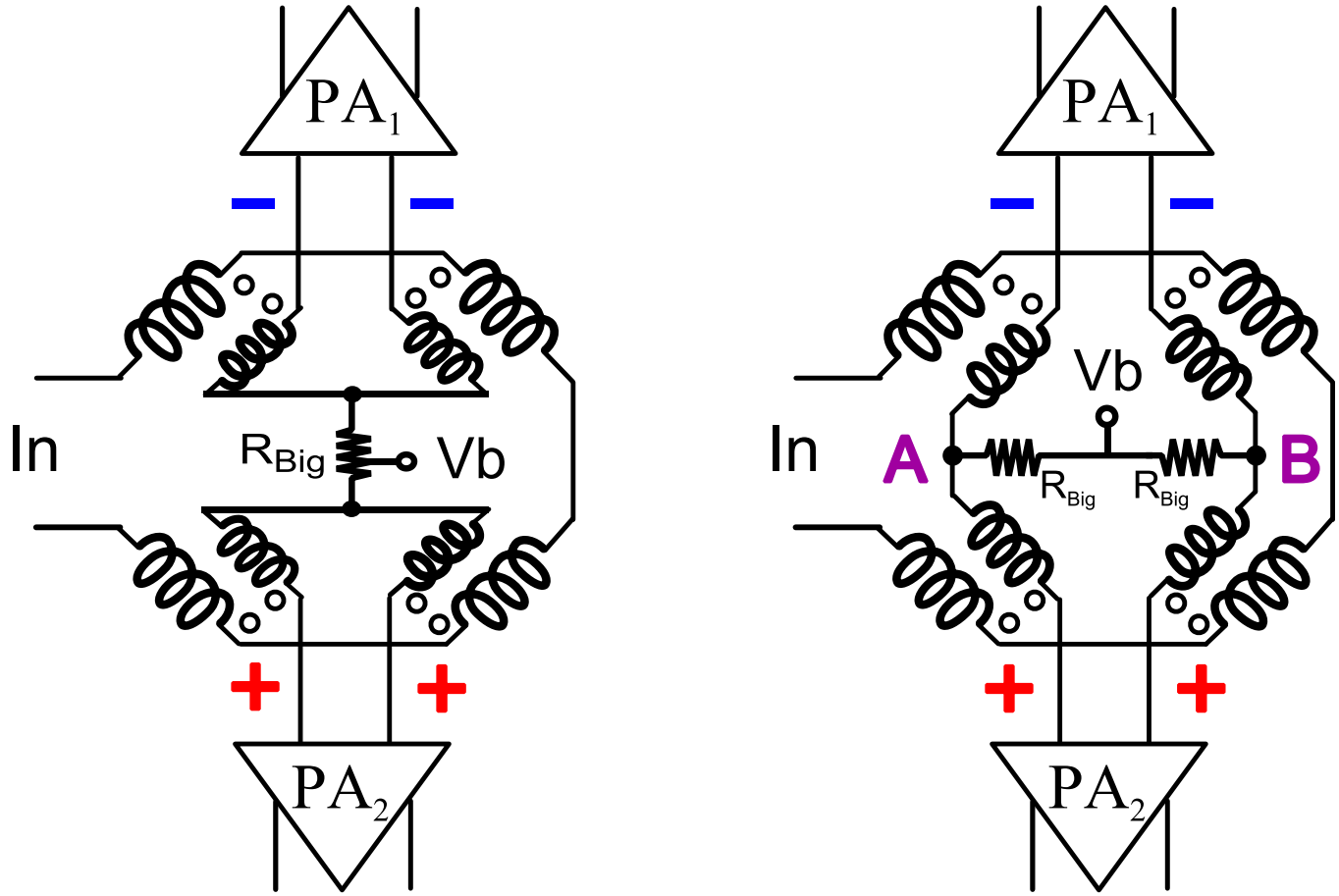

(b) 1st topology




(c) 2nd topology

- Two different layout topologies for splitter

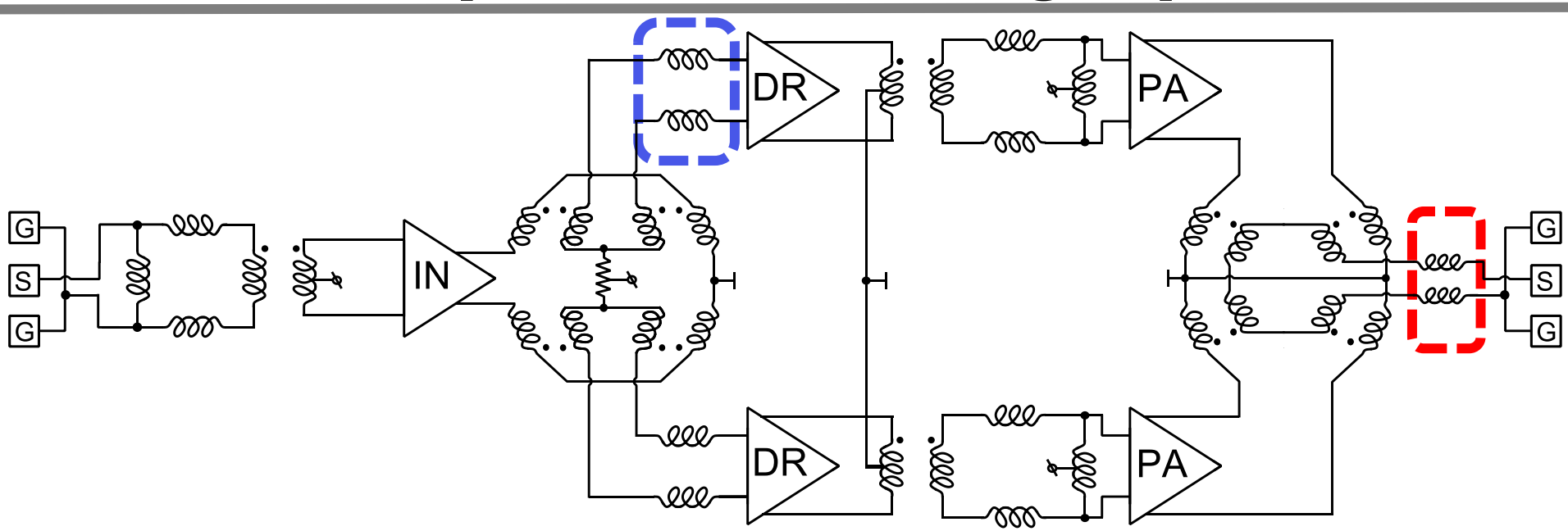
# Stability Analysis

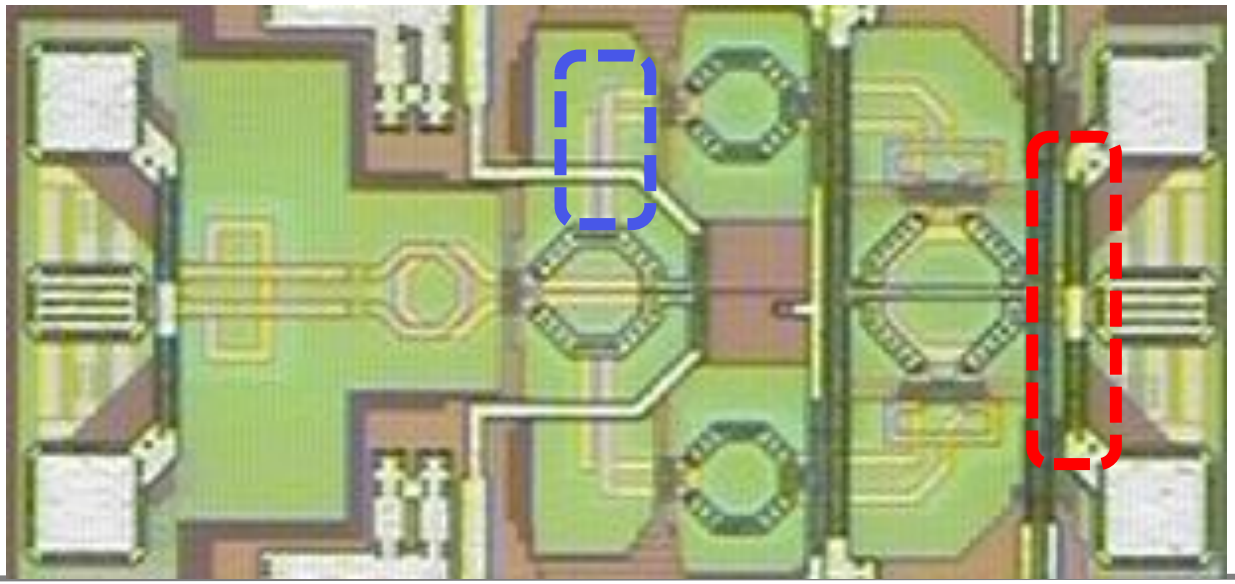



(a) 1st topology (b) 2nd topology

- Proposed splitter can suppress differential-mode common-mode oscillation

# Chip Photomicrograph



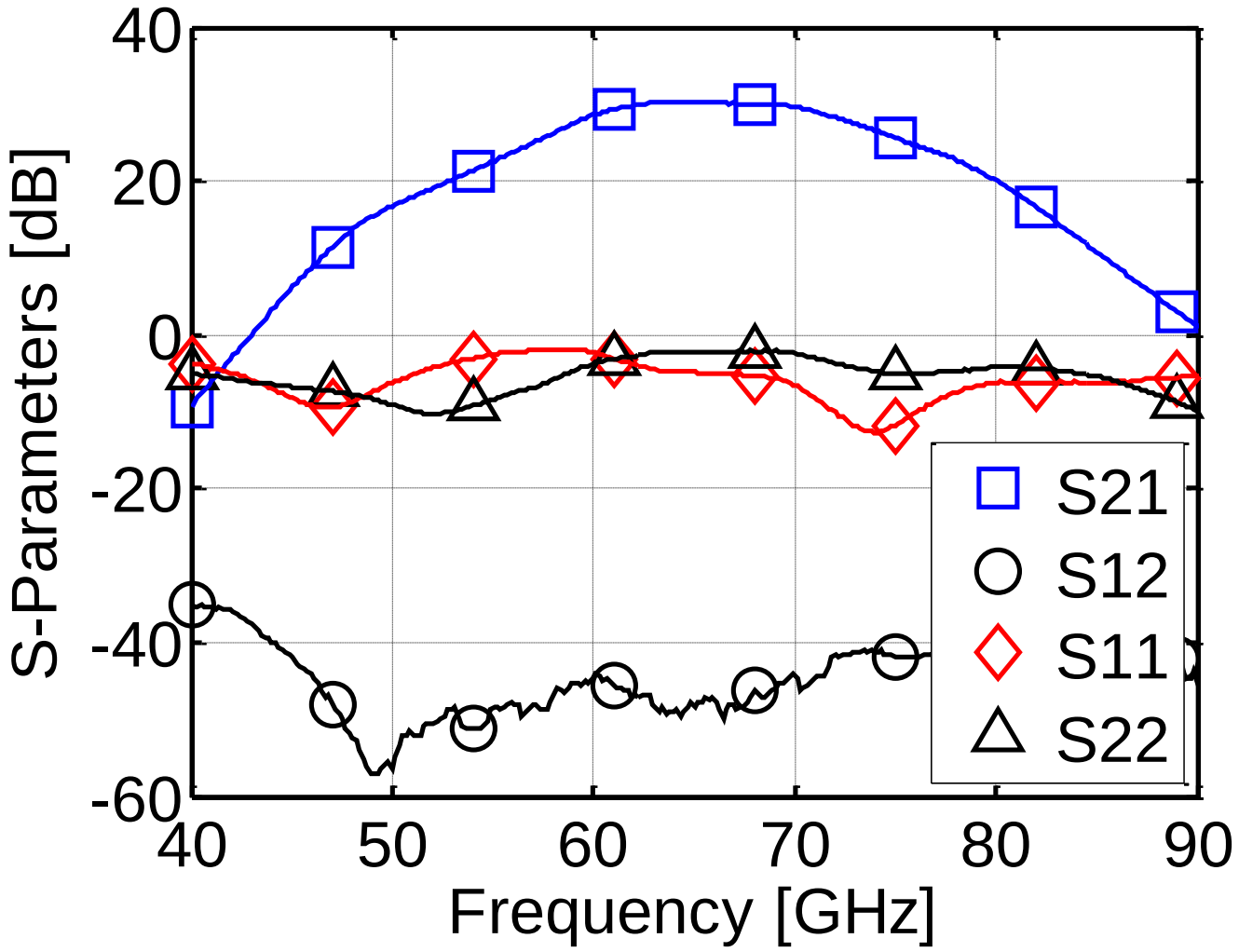



ST 65nm CMOS

Chip area: 0.57 $mm^2$

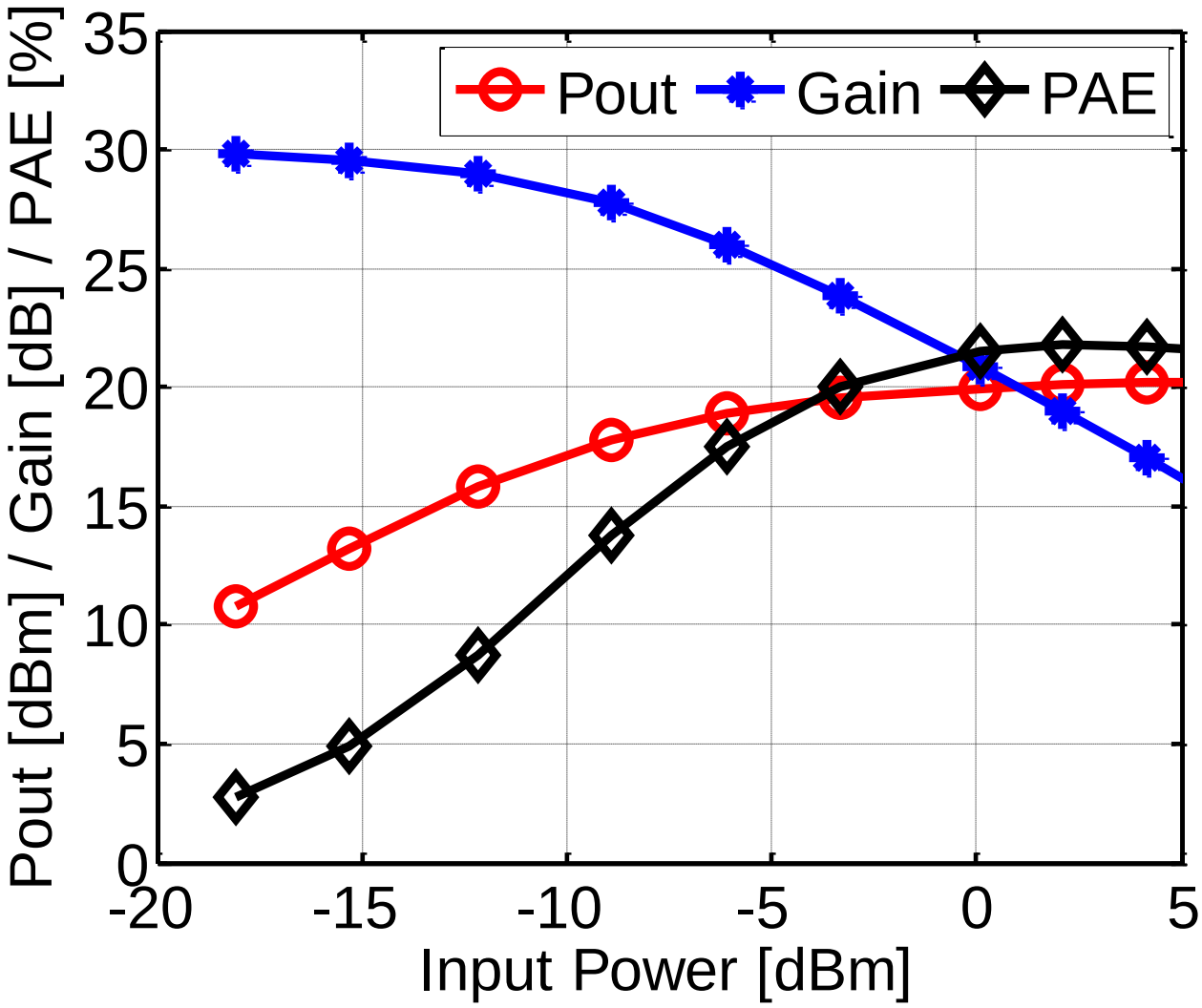
Core area: 0.11 $mm^2$

# Measured S-Parameters



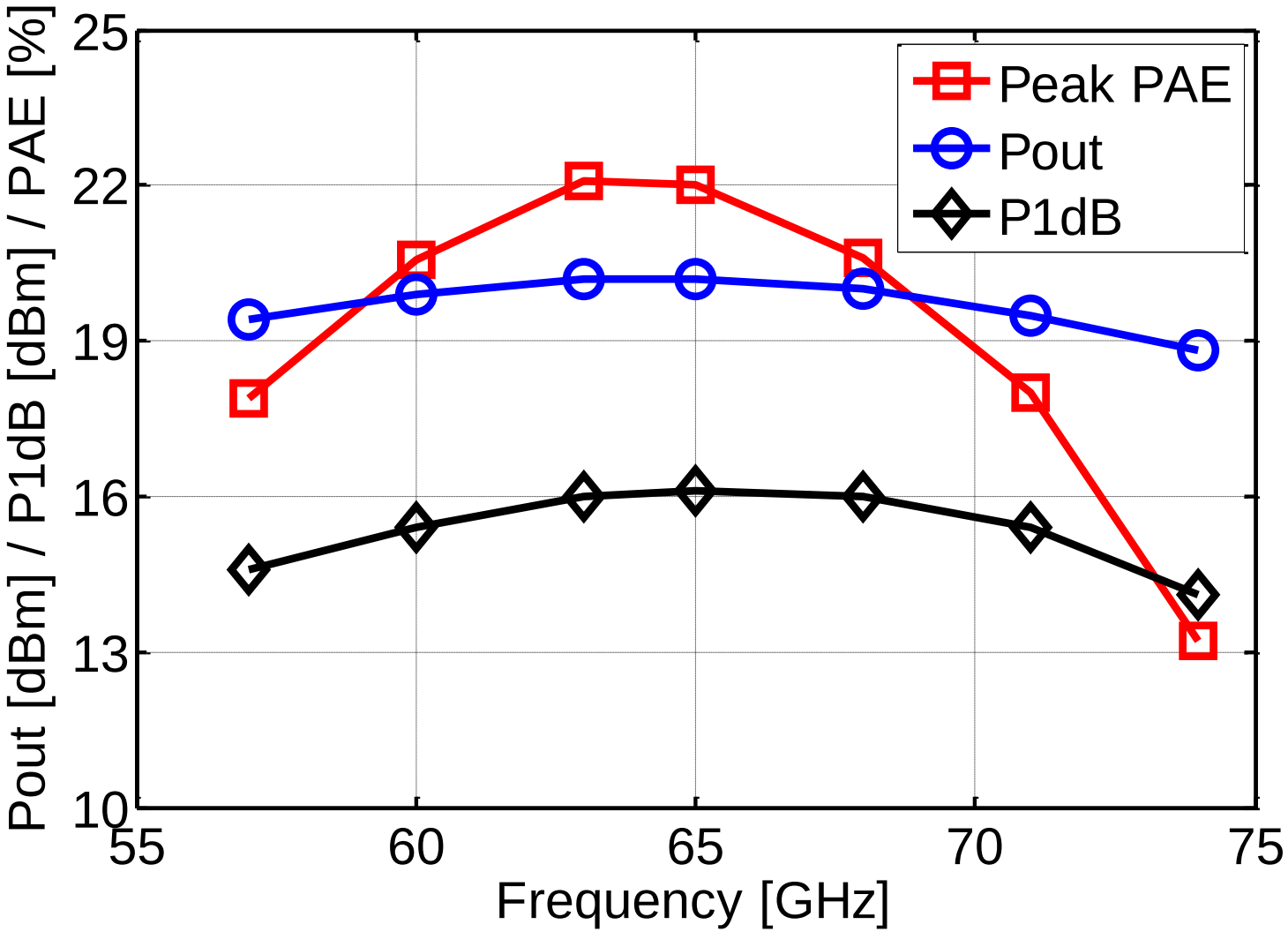

Gain≈30dB, $BW_{3dB}$: 58.5-73.5GHz

# Large Signal Performances at 65GHz




$P_{SAT}$≈20dBm, $P_{1dB}$≈16dBm, PAE≈22%

# Large Signal Performances over Frequency




$P_{Sat}$>19dBm, $P_{1dB}$>15dBm, PAE>15% over the bandwidth

# Performance Summary and Comparison

| Reference | Tech. & Vdd | Gain (dB) | BW (GHz) | GBW (GHz) | $P_{SAT}$ (dBm) | $P_{1dB}$ (dBm) | PAE (%) |
|---|---|---|---|---|---|---|---|
| CICC13 [5] | 28nm / 1V | 24 | 11 | 174 | 16.5 | 11.7 | 13 |
| JSSC13 [3] | 40nm / 1V | 17 | 6 | 42 | 17 | 13.8 | 30 |
| RFIC14 [2] | 65nm / 1.2V | 17.7 | 12 | 92 | 16.8 | 15.5 | 15 |
| ISSCC14 [8] | 40nm / 1.8V | 22.4 | *n/a* | *n/a* | 16.4 | 13.9 | 19 |
| ISSCC15 [1] | 28nm SOI/ 1V | 35 | *8* | *450* | 18.9 | 15 | 18 |
| **This Work** | **65nm / 1V** | **30** | **15** | **474** | **20** | **16** | **22** |

State-of-the-art $P_{SAT}$ and PAE with the largest GBW

# Conclusions

- High GBW is critical for high efficient, wideband PAs
- Coupled resonators can improve PA GBW while keeping compact layout
- A methodology has been proposed to design wideband combiner/splitter using coupled resonators
- A three-stage two-path PA with 20dBm $P_{SAT}$, 22% PAE, and 15GHz bandwidth in 65nm CMOS was demonstrated

# Acknowledgements



- Studio di Microelecttronica, Pavia, Italy


- Prof. Yann Deval and Magali de Matos, University of Bordeaux

***Thank You!***

# References


[1] A. Larie et al., “A 60 GHz 28 nm UTBB FD-SOI CMOS reconfigurable power amplifier with 21% PAE, 18.2 dBm P1dB and 74mW PDC,” in ISSCC15

[2] P. Farahabadi and K. Moez, “A dual-mode highly efficient 60 GHz power amplifier in 65 nm CMOS,” in RFIC14

[3] D. Zhao and P. Reynaert, “A 60-GHz dual-mode class AB power amplifier in 40-nm CMOS,” in JSSC13

[4] K.-Y. Wang, T.-Y. Chang, and C.-K. Wang, “A 1V 19.3dbm 79GHz power amplifier in 65nm CMOS,” in ISSCC12

[5] S. Thyagarajan, A. Niknejad, and C. Hull, “A 60 GHz linear wideband power amplifier using cascode neutralization in 28 nm CMOS,” in CICC13

[8] S. Kulkarni and P. Reynaert, “A Push-Pull mm-Wave Power Amplifier with <0.8° AM-PM Distortion in 40nm CMOS,” in ISSCC14