Non-Resistance Metric based Read Scheme for Multi-level PCRAM in 25nm Technology

Junho Cheon, Insoo Lee, Changyong Ahn, Milos Stanisavljevic, Aravinthan Athmanathan, Nikolaos Papandreou, Haris Pozidis, Evangelos Eleftheriou, Minchul Shin, Taekseung Kim, Jong Ho Kang and Jun Hyun Chun

SK hynix
Icheon, Korea

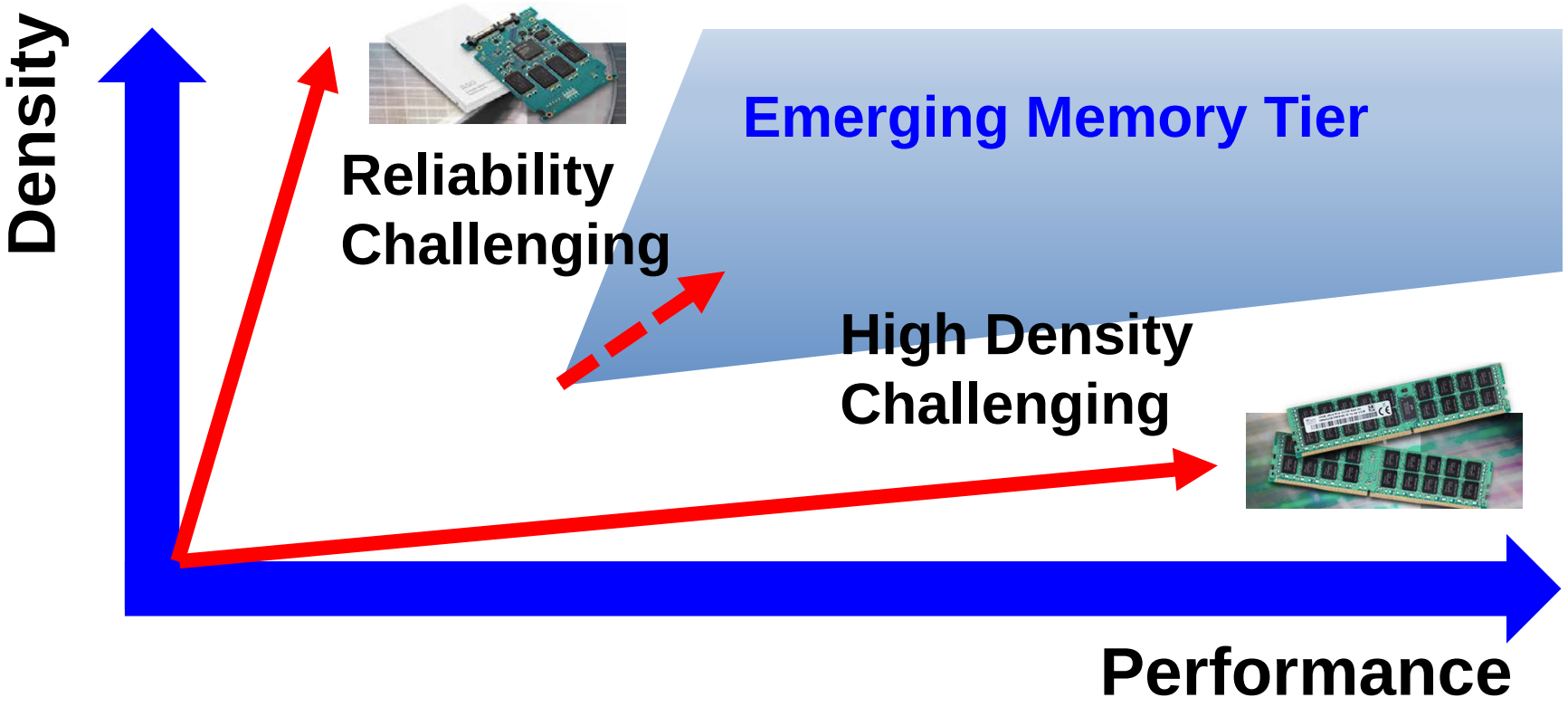
IBM Research
Zurich, Switzerland

OUTLINE

- Motivation
- Main feature of this work
  - Drift Resilient Read Metric & Circuit for Large Density Cell Array
- Implementations
  - Brief Architecture
  - Read Circuitry
- Measurement Results
- Summary

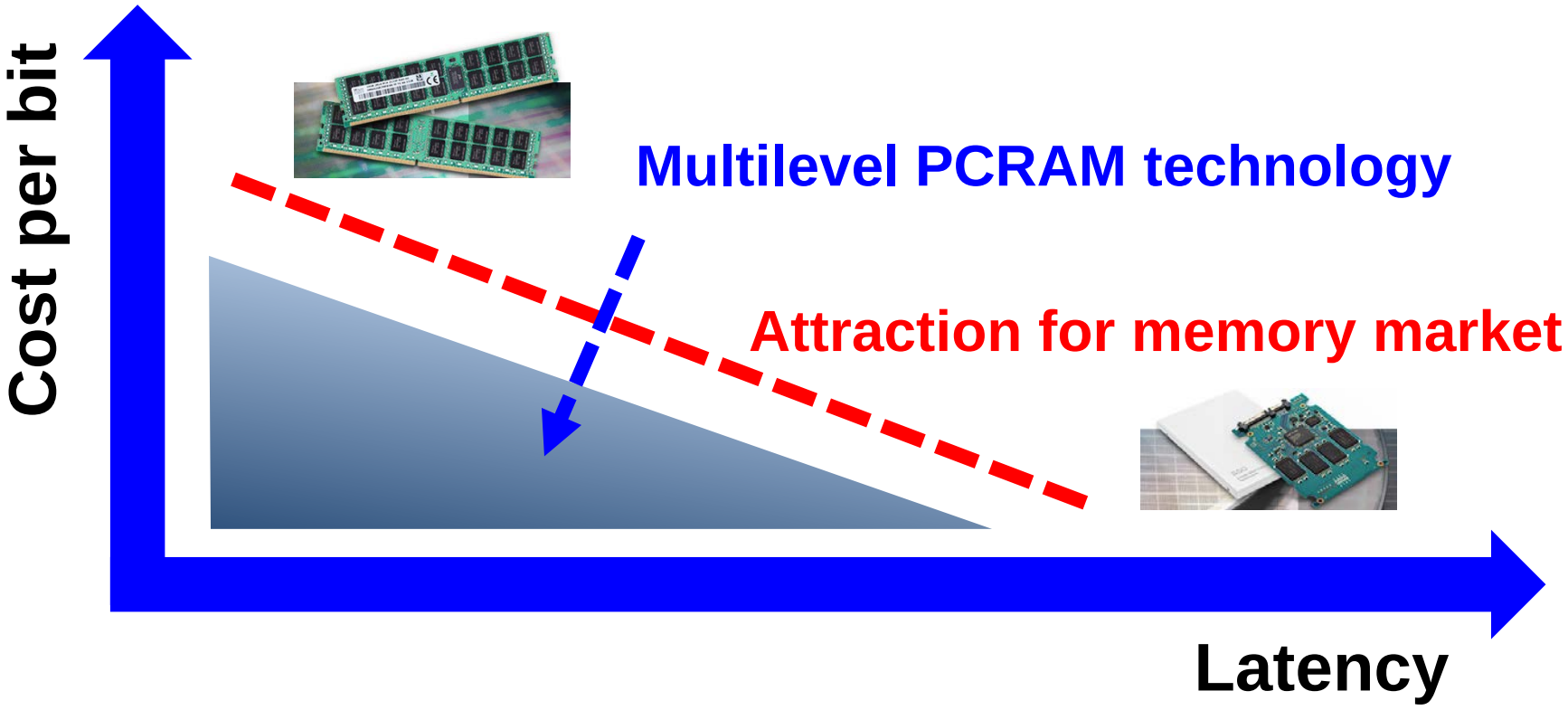
Motivation

- **The phase change memory targets an additional memory tier between DRAM and Flash storage.**



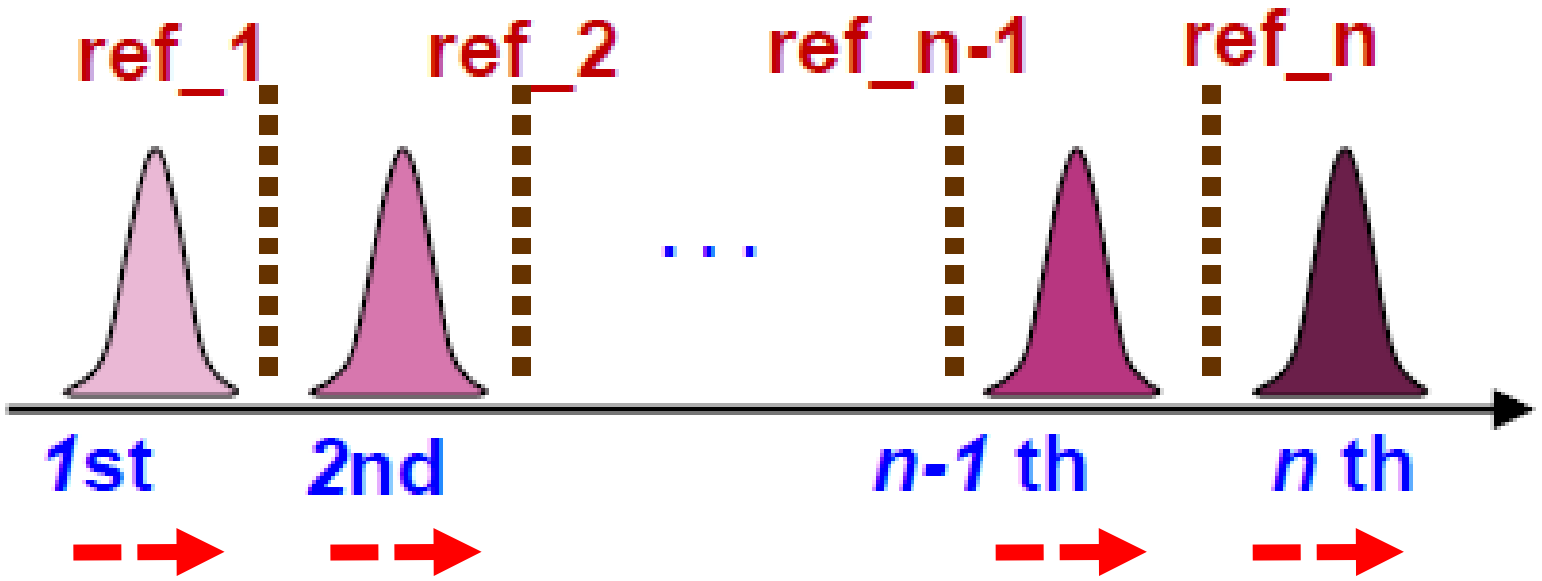
Motivation

- **Low “cost per bit” is the most key-requirement.**



Motivation

- **Important challenges for multilevel PCRAM**
  - **Temporal drift**
  - **Temperature dependency**



Main Feature of This Work

Bank size	➢ **1Gcells (2K by 4K tile)**
Architecture	➢ **Hierarchical BL structure**
Virtues	➢ **Drift mitigation** ➢ **Temperature compensation**
Latency	➢ **450ns random access latency**

Temporal Drift

- **Poole-Frankel conduction.**

$$I_R = 2q\frac{\pi r_E^2}{\tau_0} N_T \Delta z exp\left(\frac{-E_A}{kT}\right) \sinh\left(\frac{q\Delta z V_{READ}}{2kTu_A}\right)$$

Defect density, physical compressive/tensile stress influence activation energy with time.

- **Temporal drift power law.**

$\frac{R(t)}{R(t_0)} = \left(\frac{t}{t_0}\right)^{\nu}$ **, where the exponent v is drift coefficient.**

Drift Resilient Nature

- **Poole-Frankel conduction for constant electric field method.**

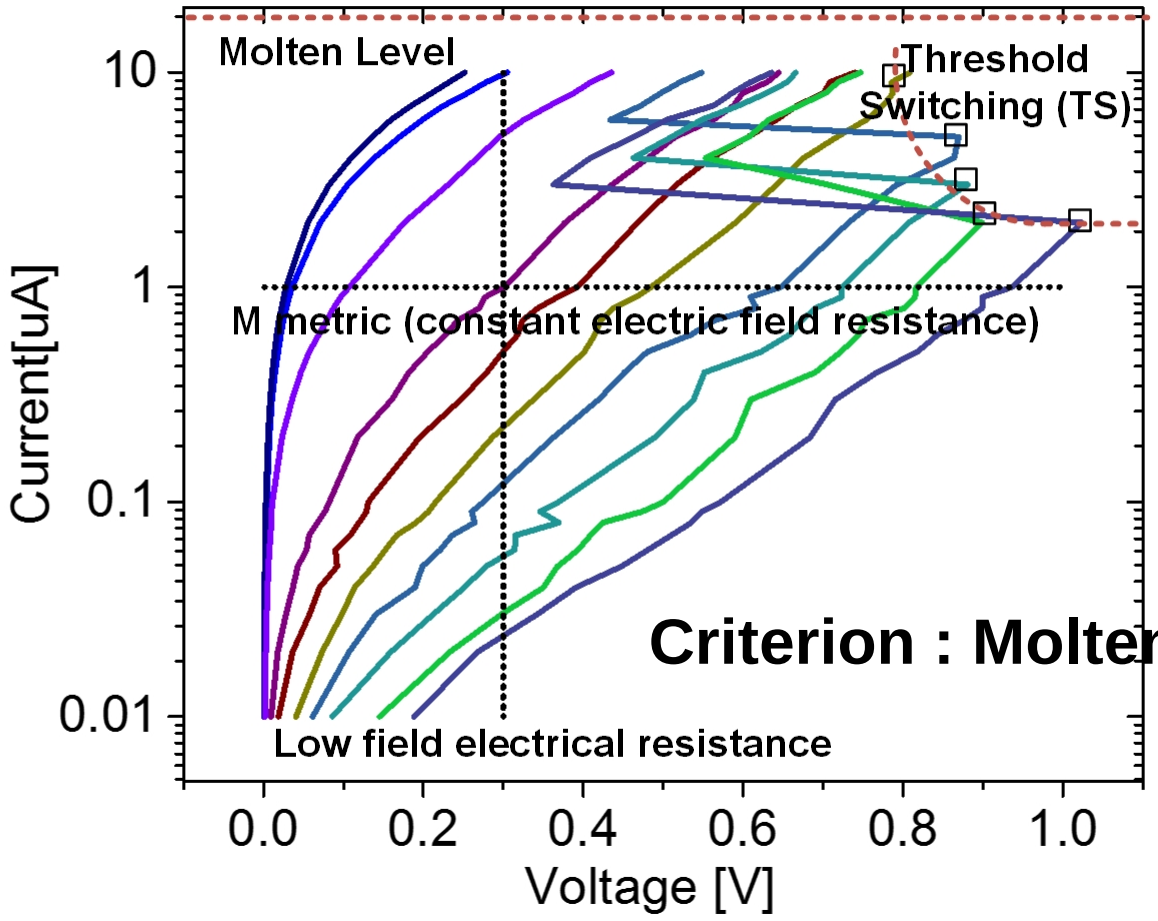
$$V_M = \frac{2kTu_A}{q\Delta z} sinh^{-1}\left[\frac{I_{DET}\tau_0}{2q\pi r_E^2 N_T \Delta z} \exp\left(\frac{E_A}{kT}\right)\right]$$

- **Not strong function of activation energy.**

- **Drift depends programmed state and material as well as “READ metric”**

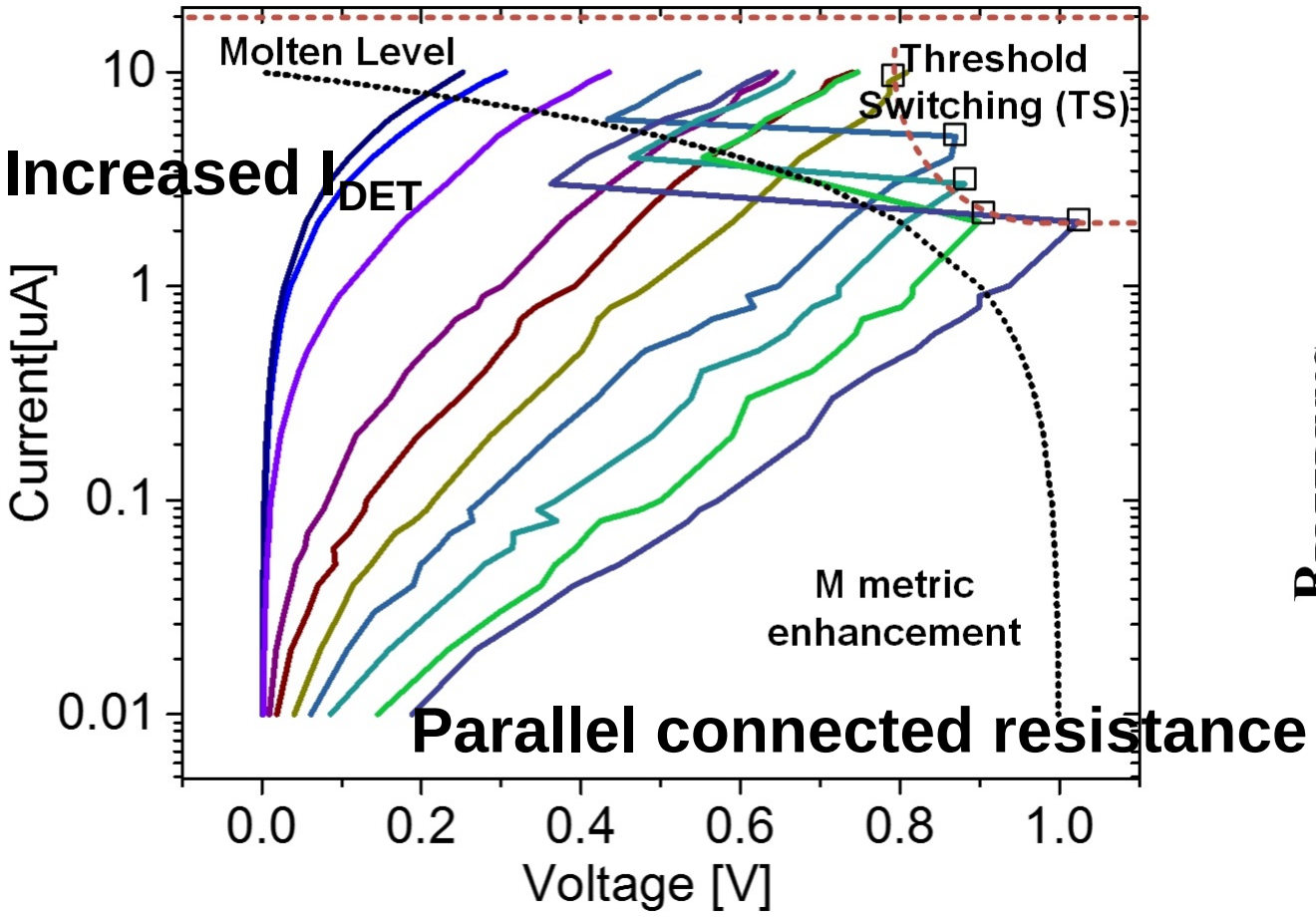
Drift Resilient Read Metric

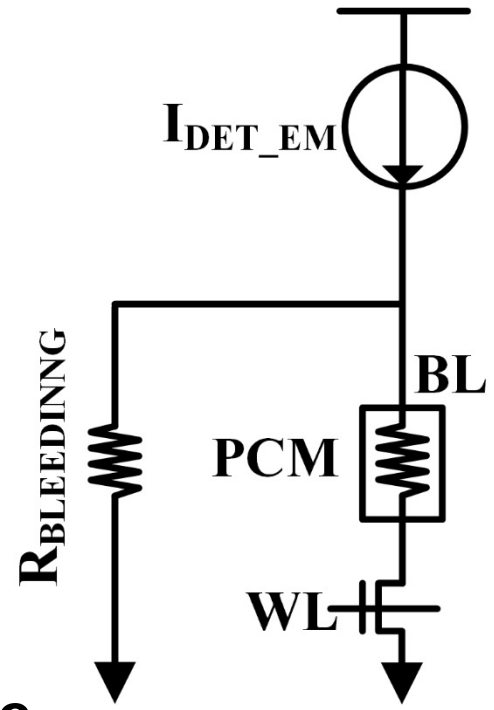
- **How can we read phase change material?**



M metric Enhancement

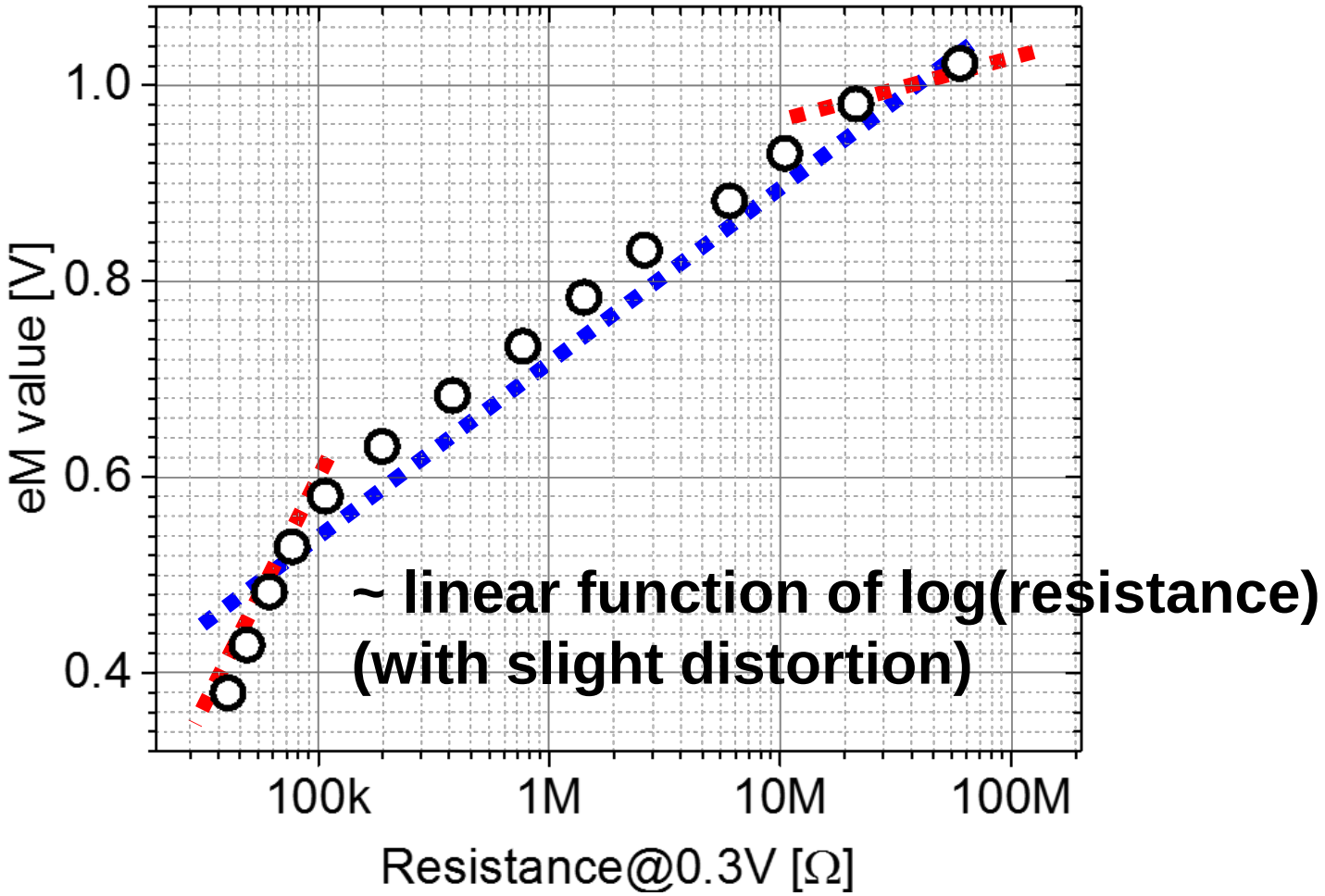
- **M metric enhancement**





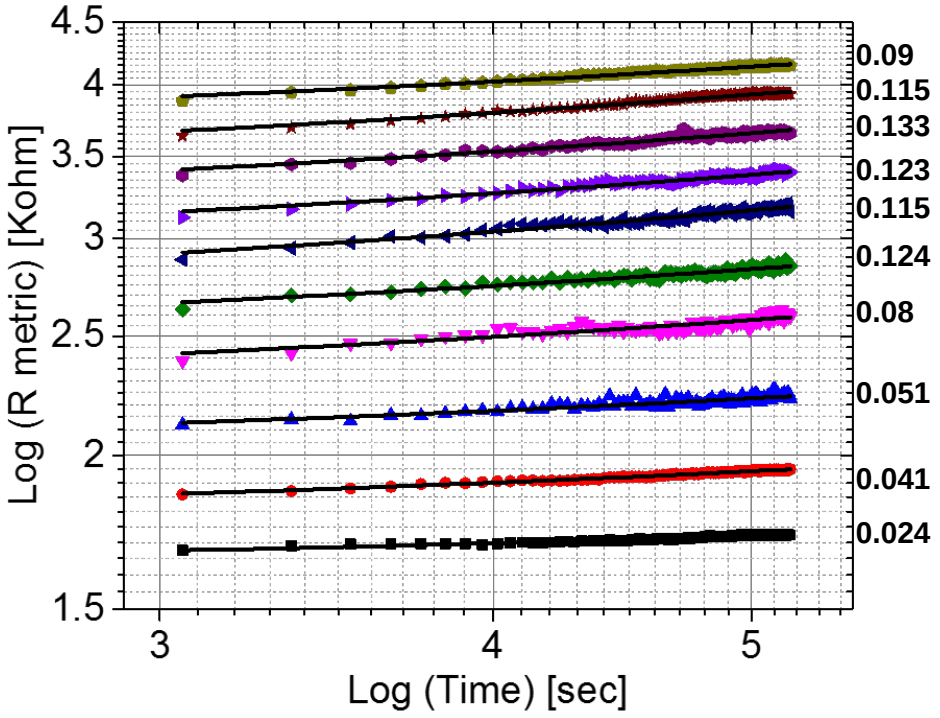
Conv. metric vs. eM metric

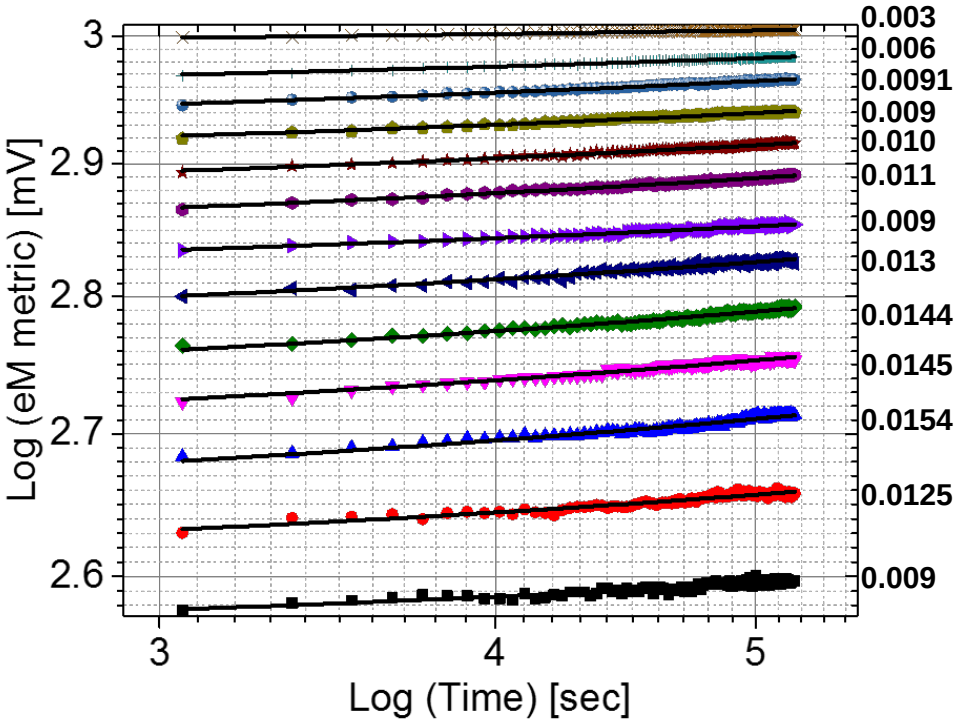
- **Exponential to linear projection.**



Temporal Drift

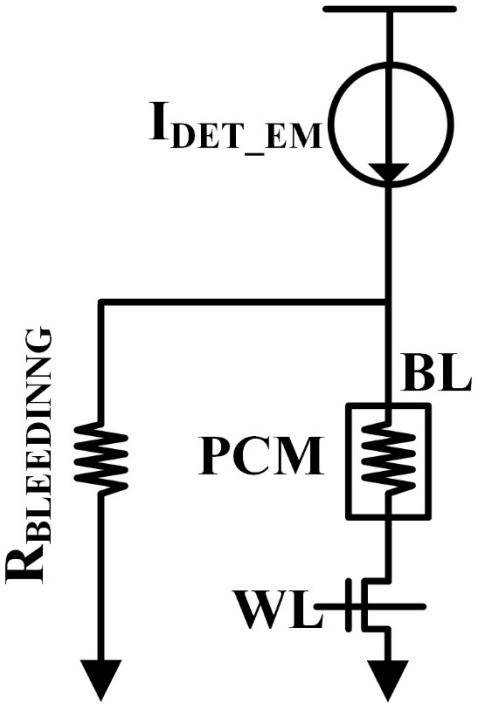
- **Bi-logarithmic scale**
- **Drift exponents are 10 times smaller.**

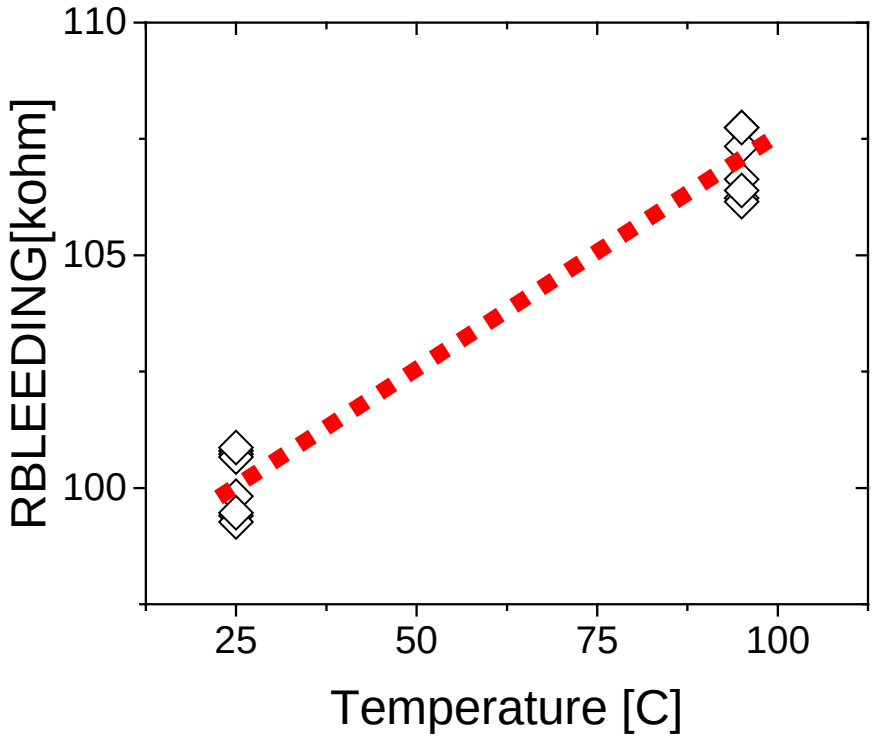




Temperature Dependency

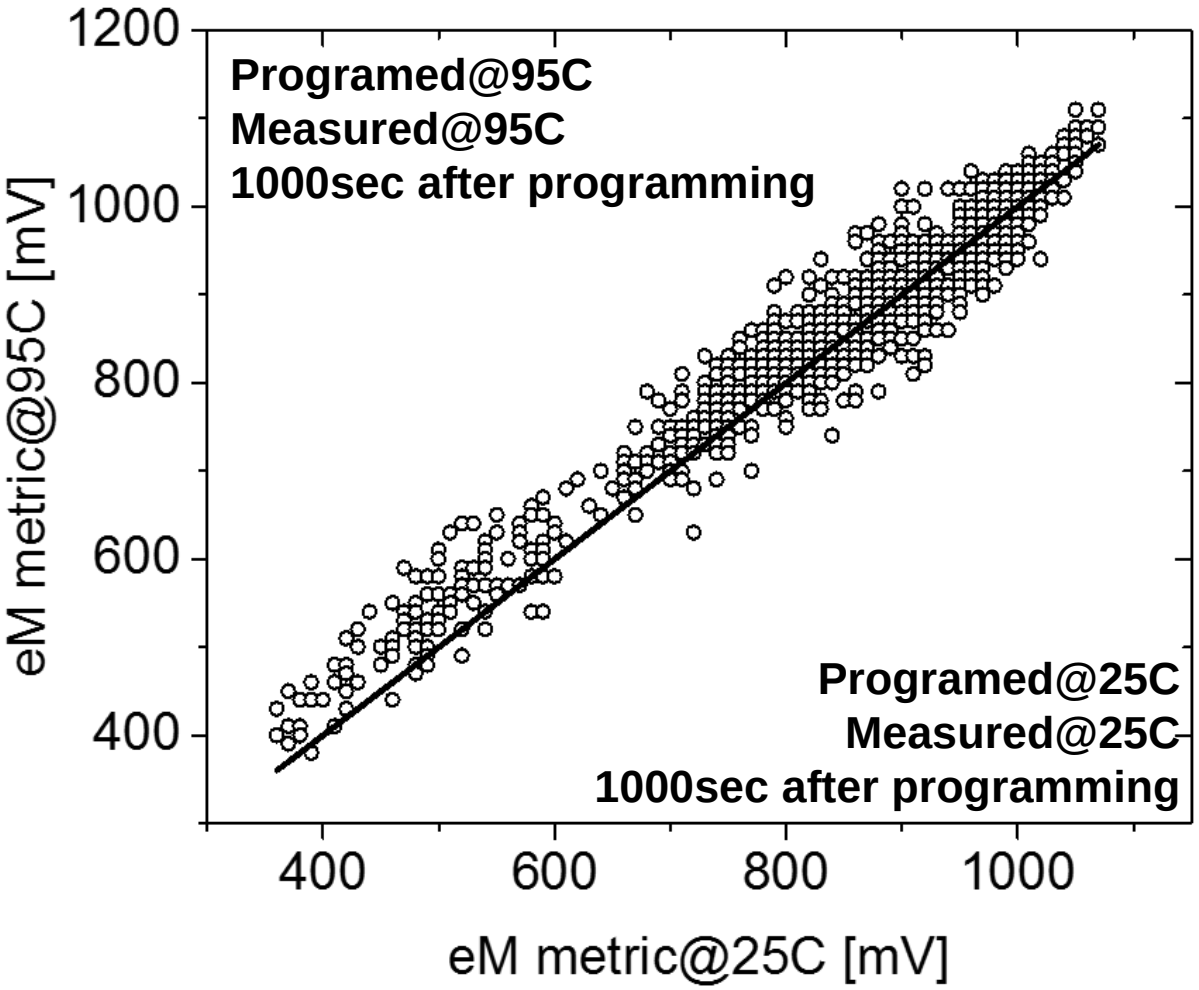
- **Proportional : phase change material**
- **Complementary : doped silicon resistor**





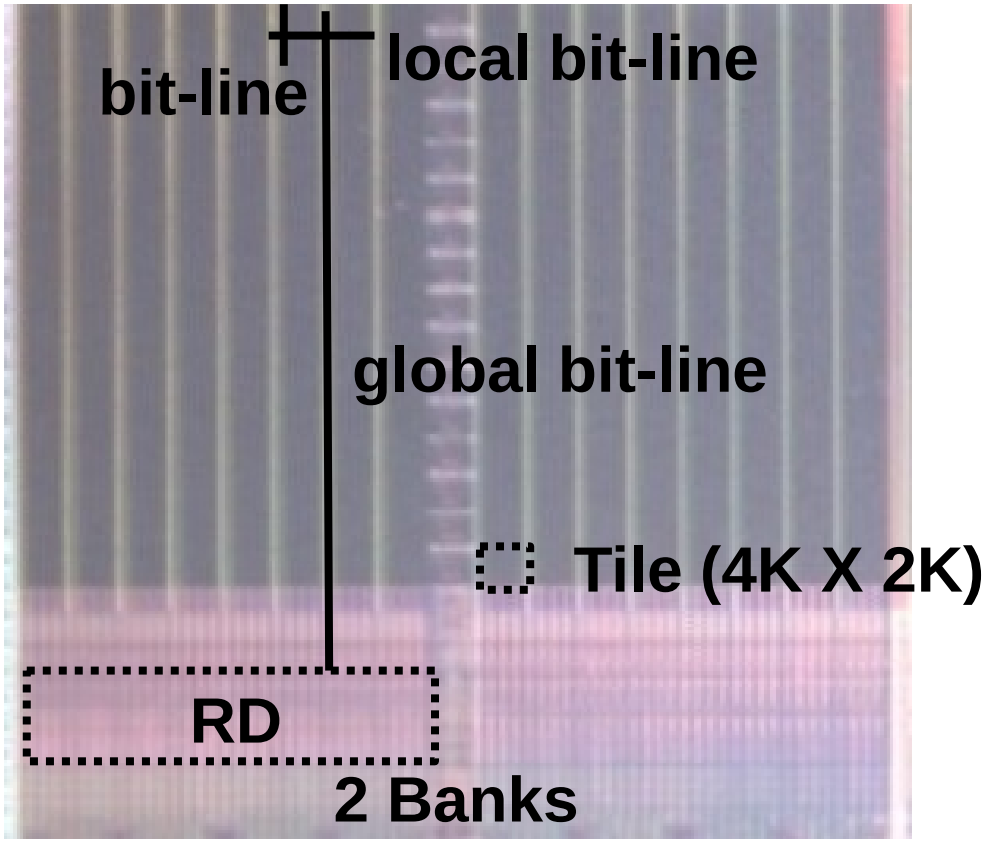
Temperature Dependency

- **Effectively Compensated.**

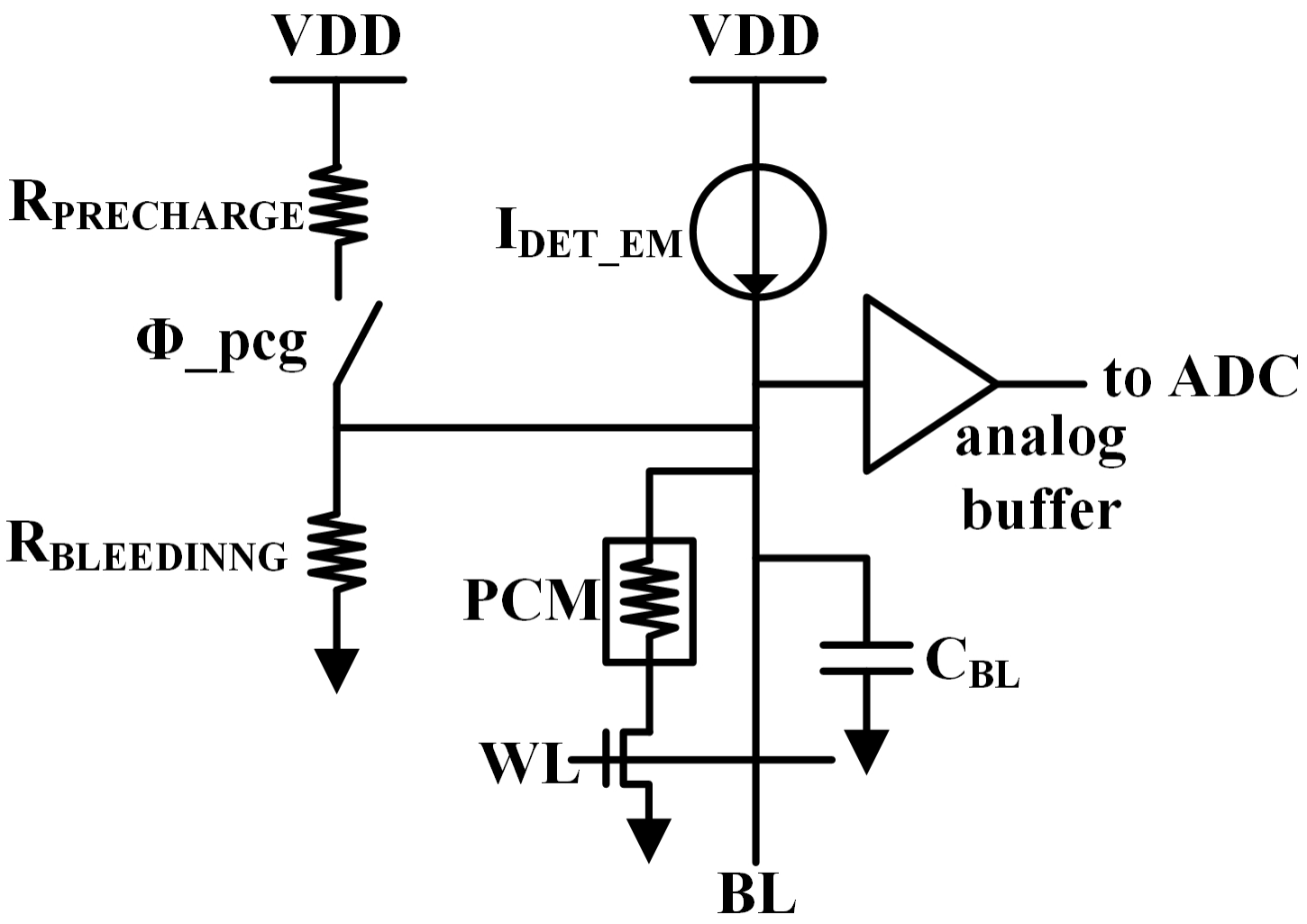


Hierarchical Bit-line Structure

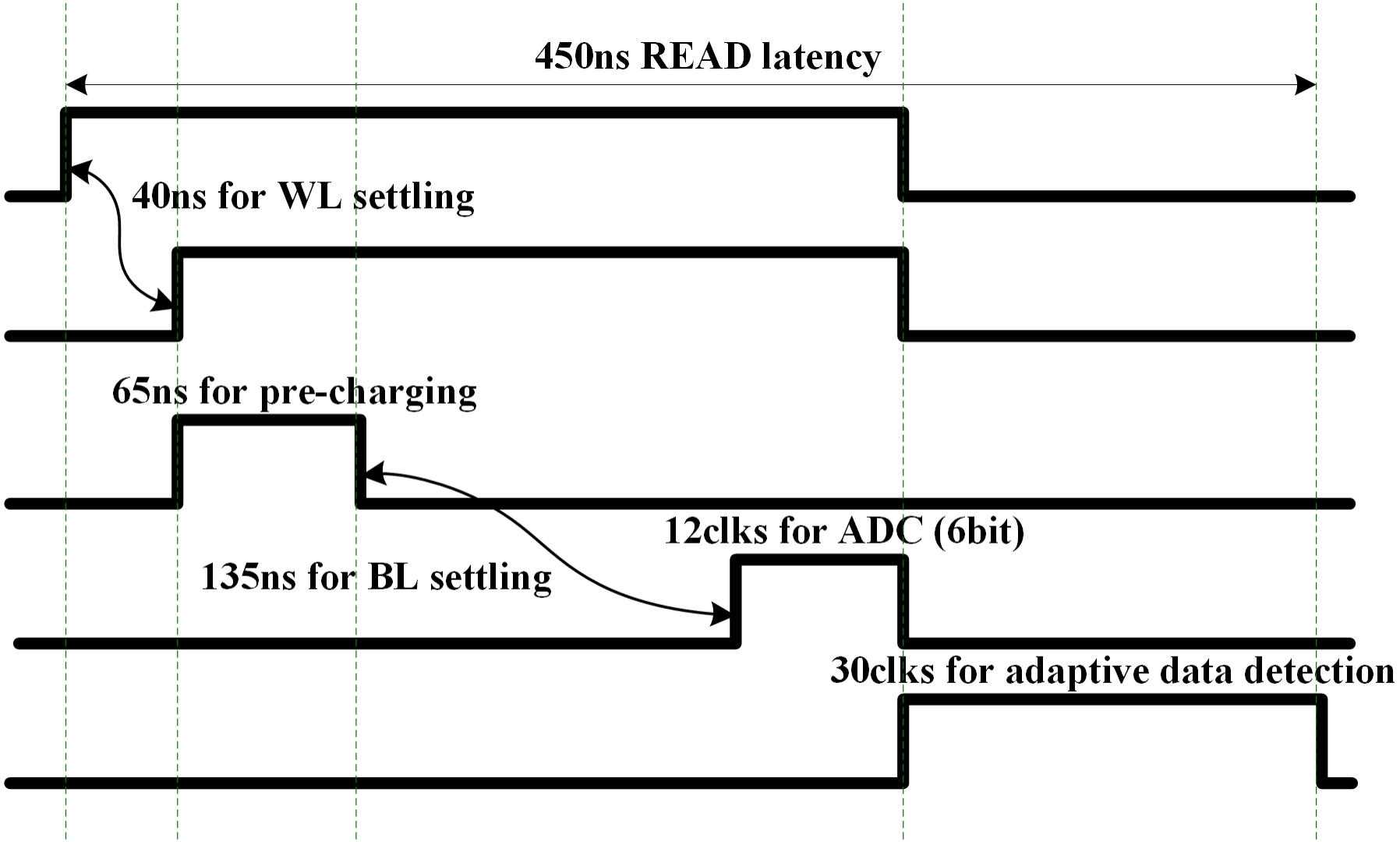
- **Suitable for cost-effective large array**



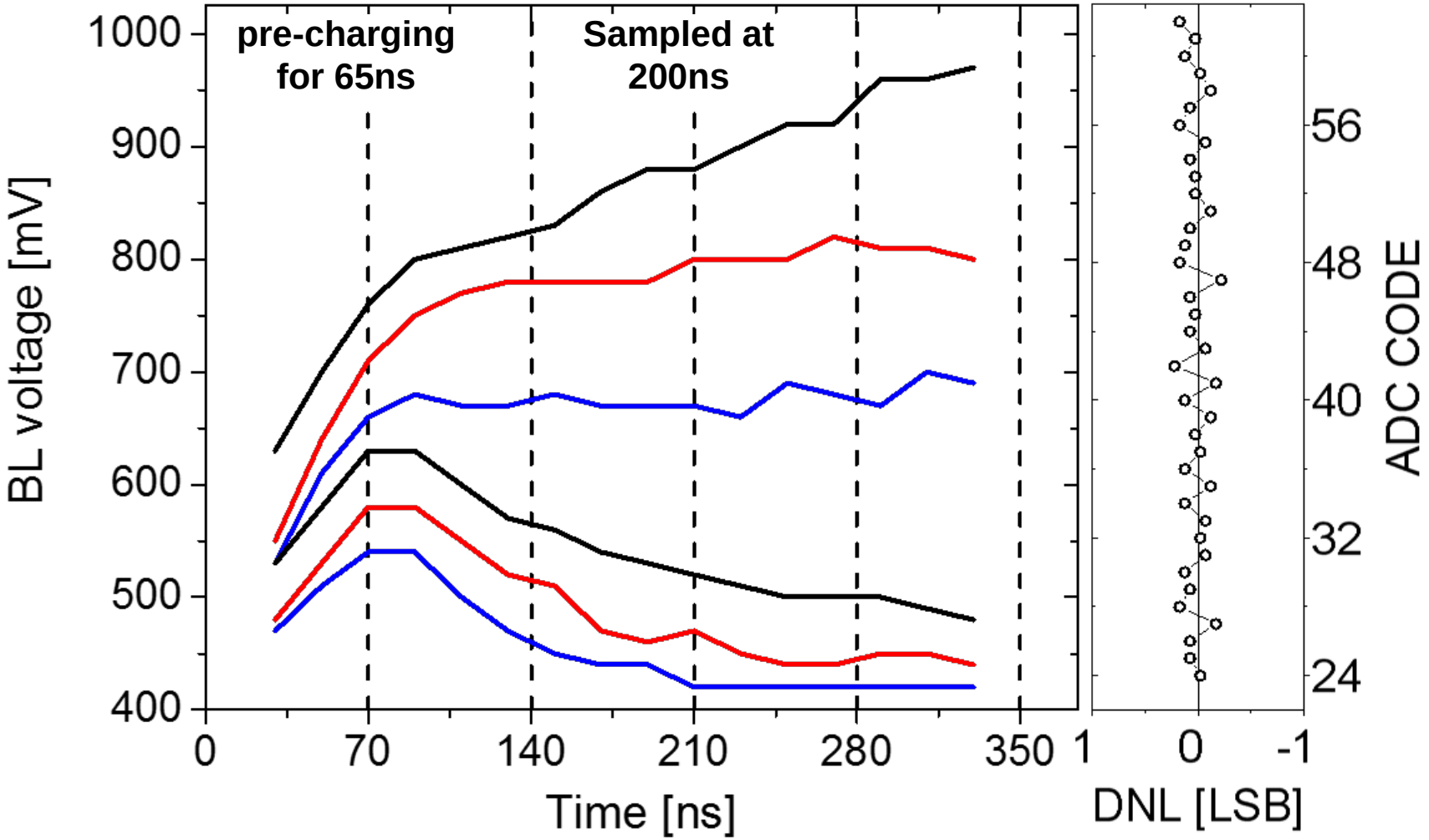
Read Circuitry



Read Timing

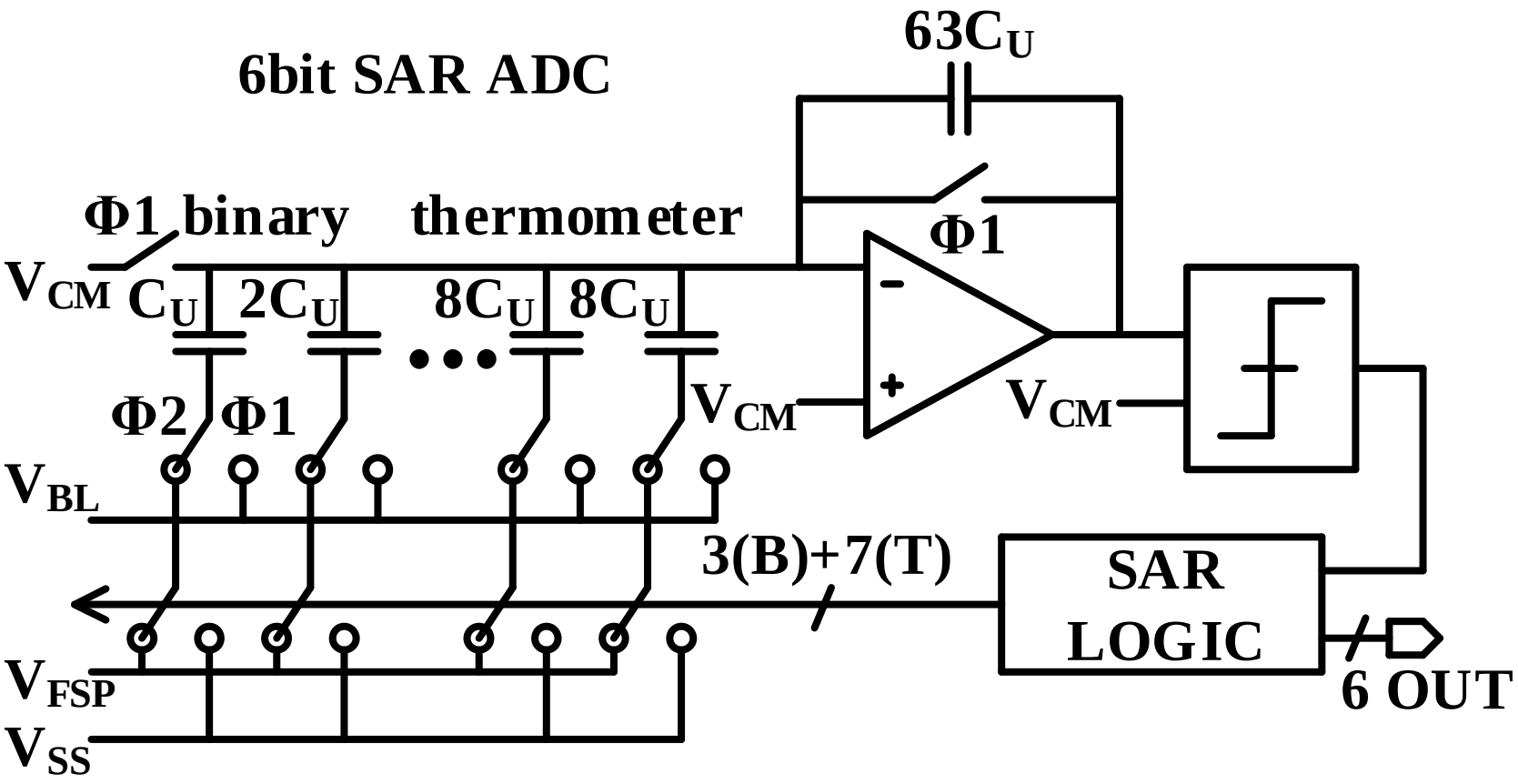

450ns READ latency
40ns for WL settling
65ns for pre-charging
12clks for ADC (6bit)
135ns for BL settling
30clks for adaptive data detection

Bit-line Voltage Trajectory



6bit SAR ADC

- **ADC as an sense amplifier**

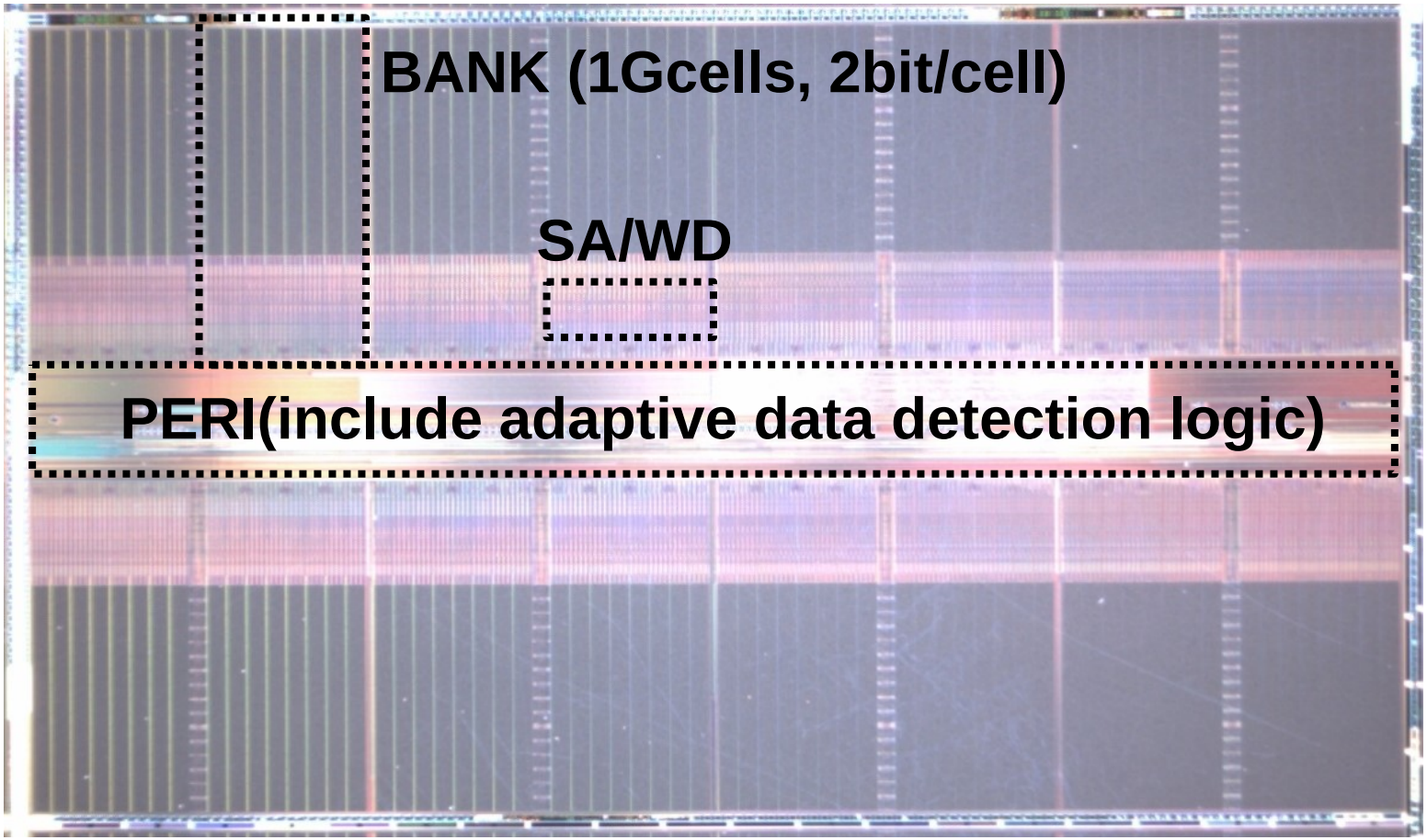


Adaptive Data Detection

- **The cells in a single frame are read/programmed simultaneously.**

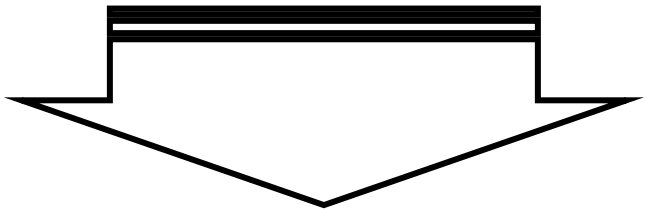
- **Based on statistics of temporal drift, the cells in a single frame are separated in 4 distinguished states.**

Die Photo


BANK (1Gcells, 2bit/cell)
SA/WD
PERI(include adaptive data detection logic)

Summary

- ✓ ~10 times smaller drift exponent
- ✓ Effective temperature compensation
- ✓ 450ns random access READ latency



✓Reliable Multilevel PCRAM Read Scheme