# A 298-fJ/writecycle 650-fJ/readcycle 8T Three-Port SRAM in 28-nm FD-SOI Process Technology for Image Processor

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**[1] Kobe University**

**[2] Renesas Electronics Corporation**

# Outline

- **Background**
- **Proposed 8T Three-Port SRAM**
- **Majority Logic**
- **Chip Implementation**
- **Measurement Result**
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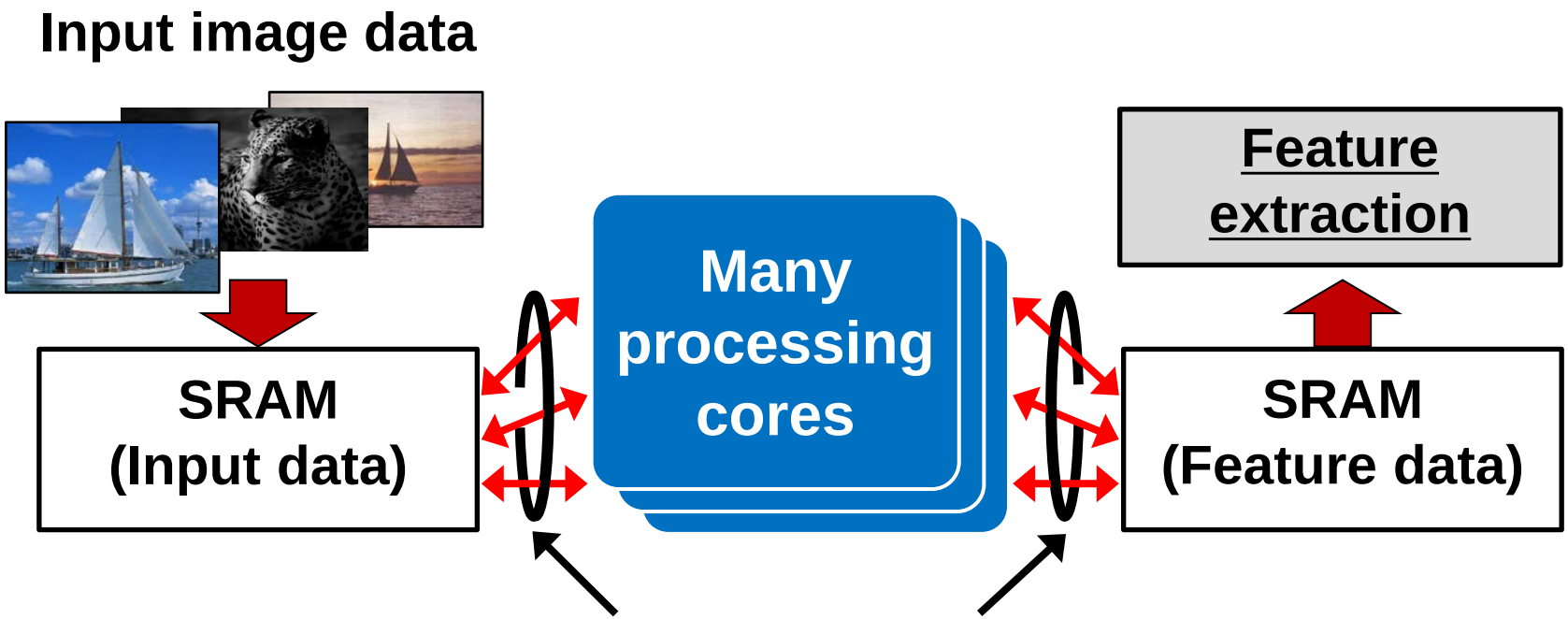
# Multiport SRAM in image processor

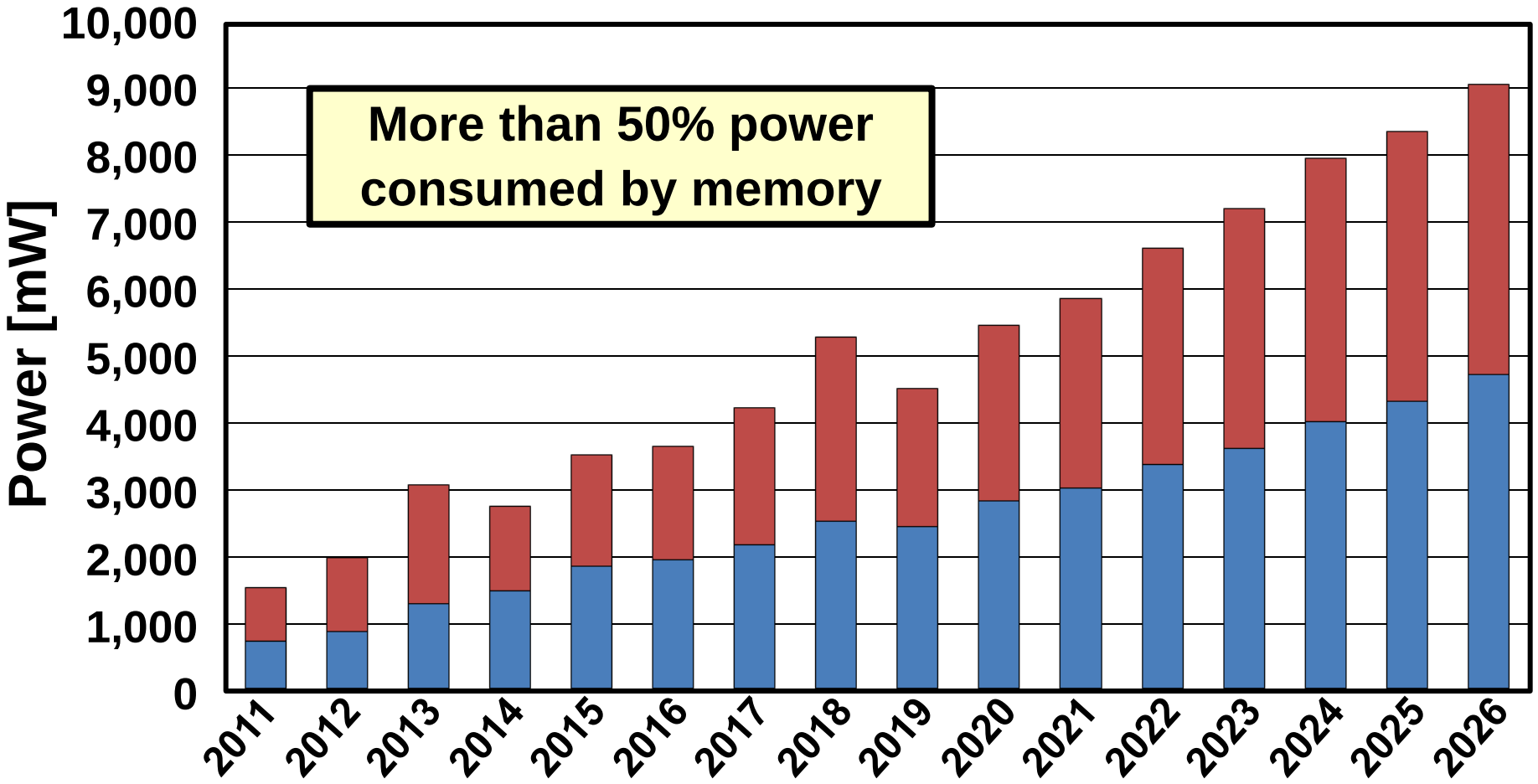
- **Multi-processing:** Image processor requires the many cores for high-resolution real-time graphics [1].




**Multiport SRAM is expected for image processor.**

*[1] S. W. Keckler, et al, IEEE Micro, 2011.*

# Trend of power consumption in portable SoC



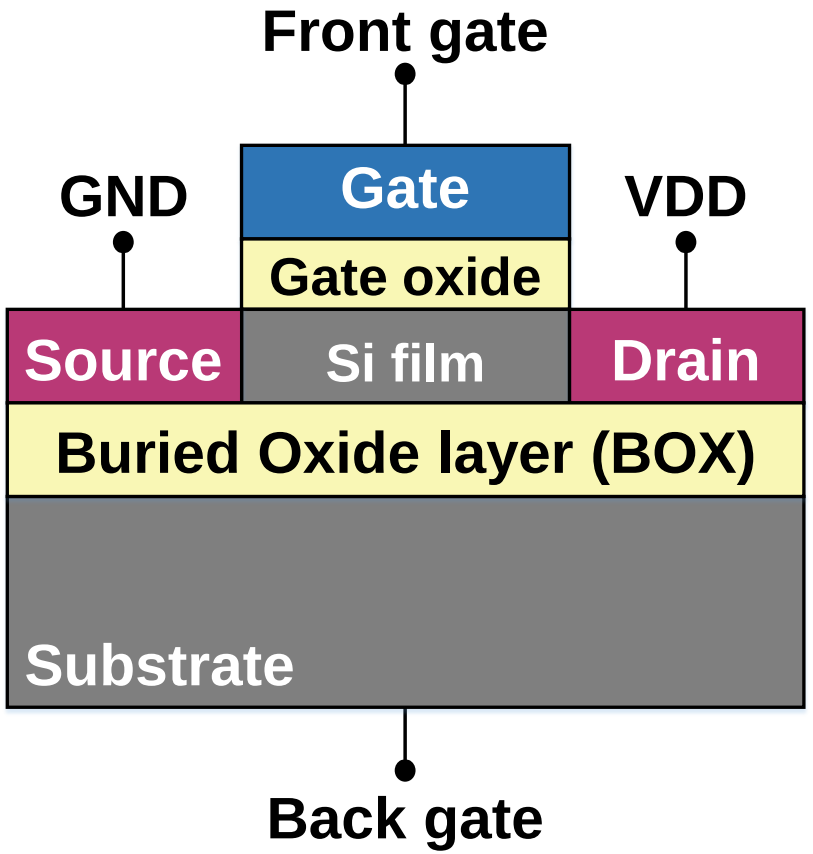

**More energy efficient SRAM will be expected**

*[1] ITRS 2011 Edition (System Drivers)*

# 28-nm UTBB FD-SOI : Advantages

**UTBB FD-SOI: Ultra Thin Body&BOX Fully-Depleted Silicon on Insulator**

- **FD-SOI has been adopted in the 28nm node [2].**
  - Improving transistor behavior, especially at low supply voltage.
- **28nm FD-SOI enables an ultra-low power SRAM design [2].**
  - Thicker gate dielectric reduced gate leakage




*[2] P. Flatresse et al., ISSCC 2013.*

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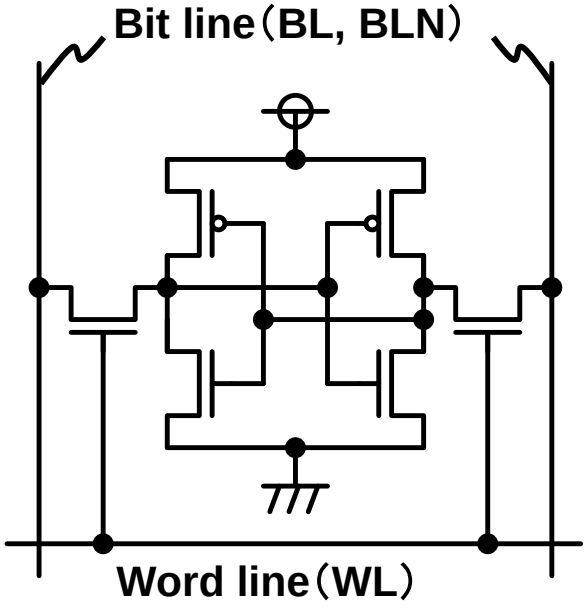
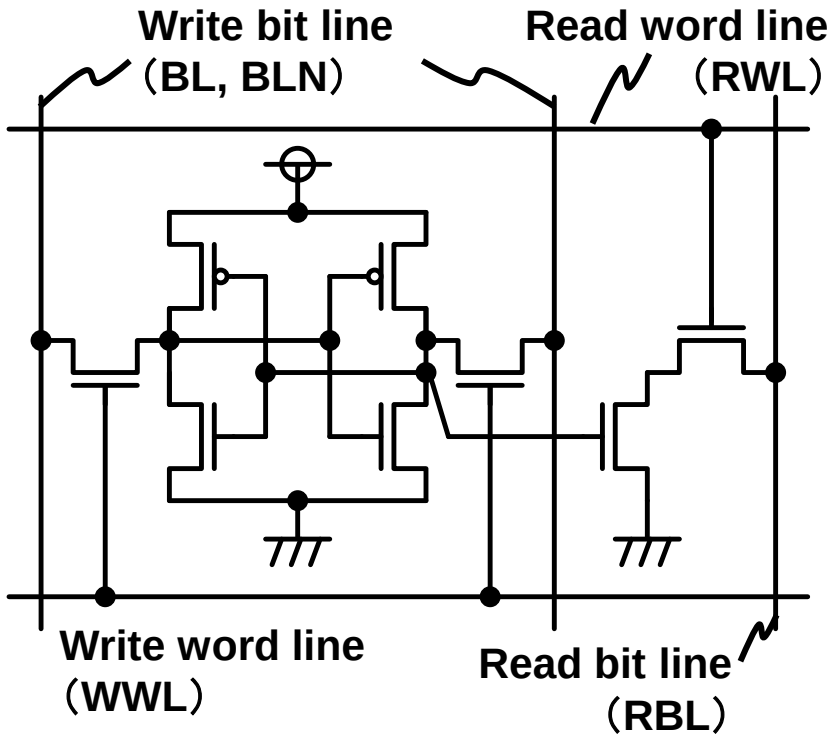
# Static random access memory (SRAM)



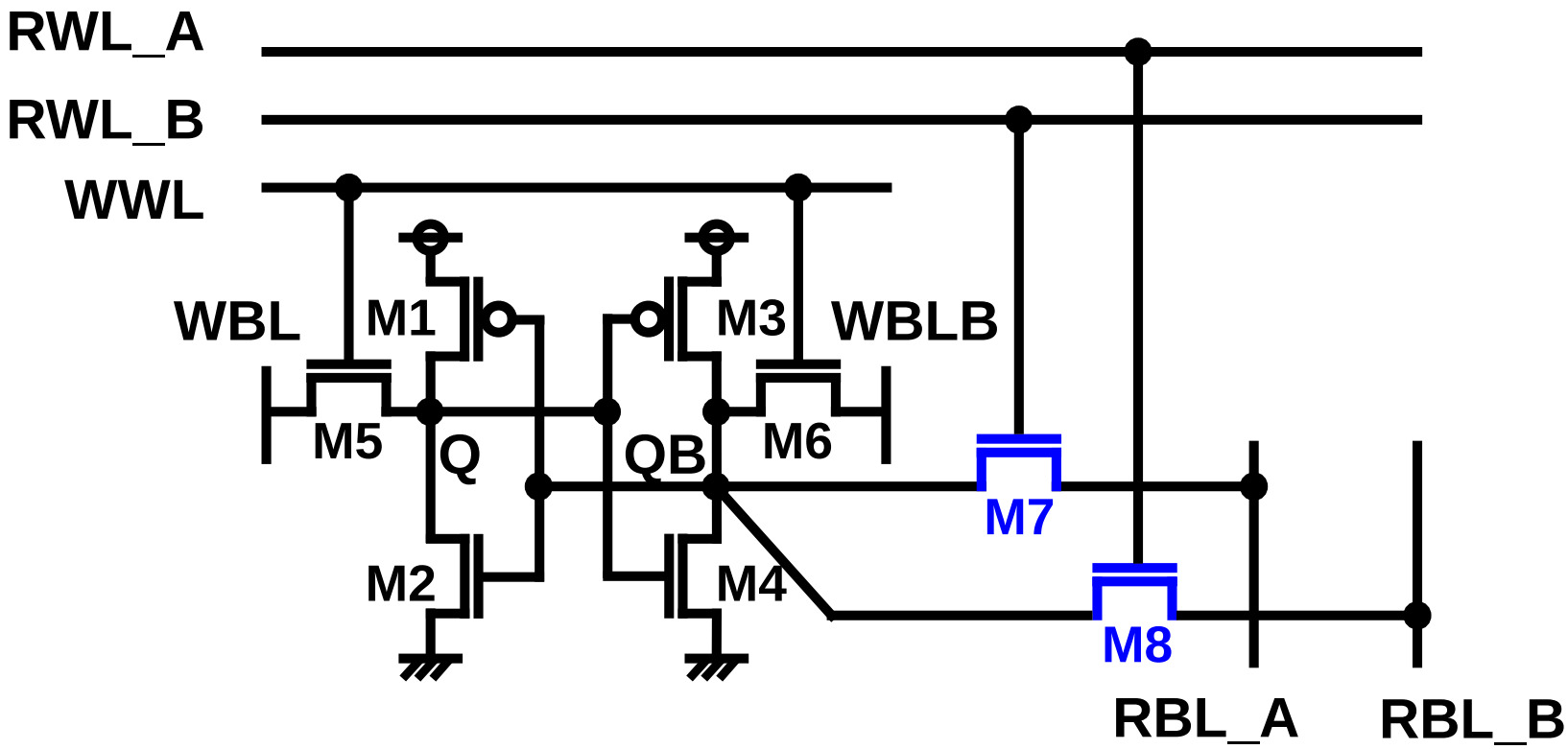




【6T SRAM cell】
- High density
- Bit line pair
 (Common write/read port)

【8T dual port SRAM cell】
- Area: 6T cell + 30%
- 1write/1read port structure

**Area becomes large according to the port number increases**
**→Multi port SRAM is expected to be a smaller layout**

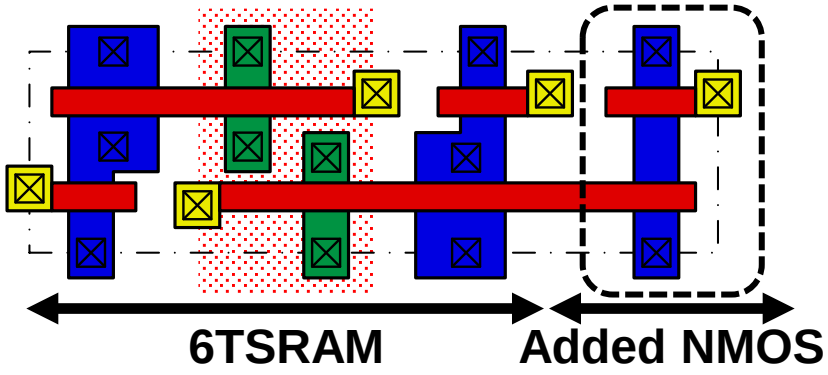
# Proposed 8T three-port SRAM



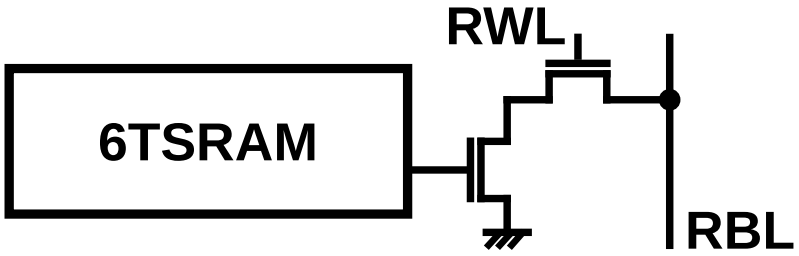

**M7 and M8 transistors are used as single end read ports**

**Asymmetrical 8T three-port cell achieves high density & low power operation.**

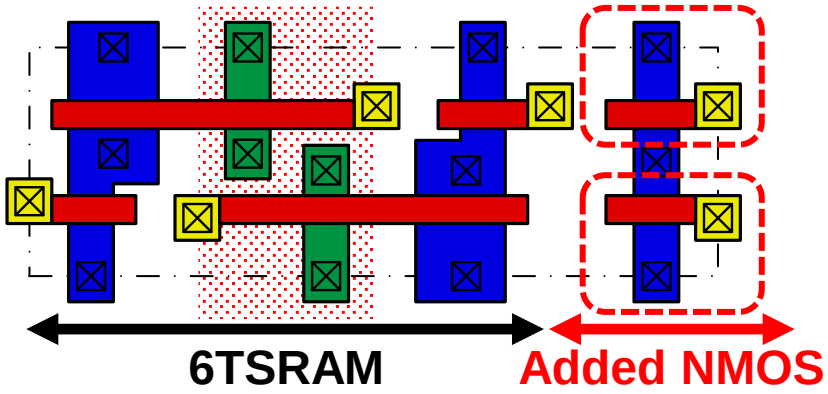
# Memory cell layout (2-p vs. 3-p)



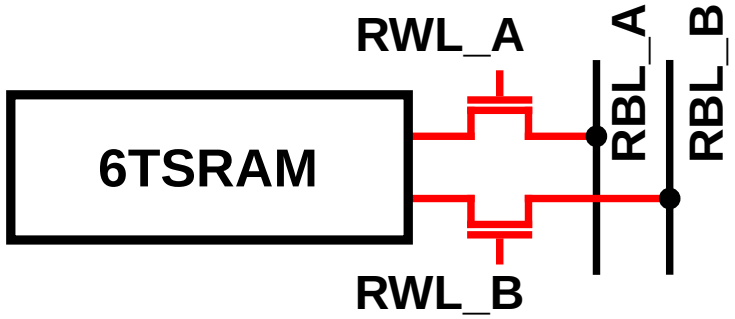

Conv. 28nm 8T 2-port cell




2-port: Two NMOS transistors are used as read port.



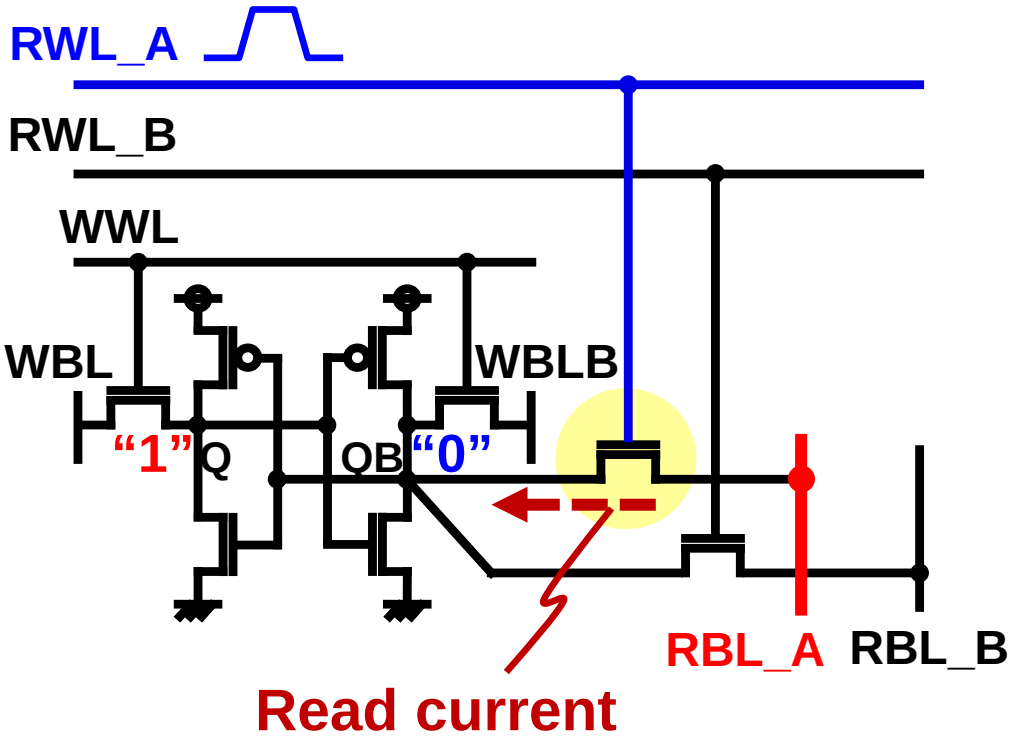

Prop. 28nm 8T 3-port cell

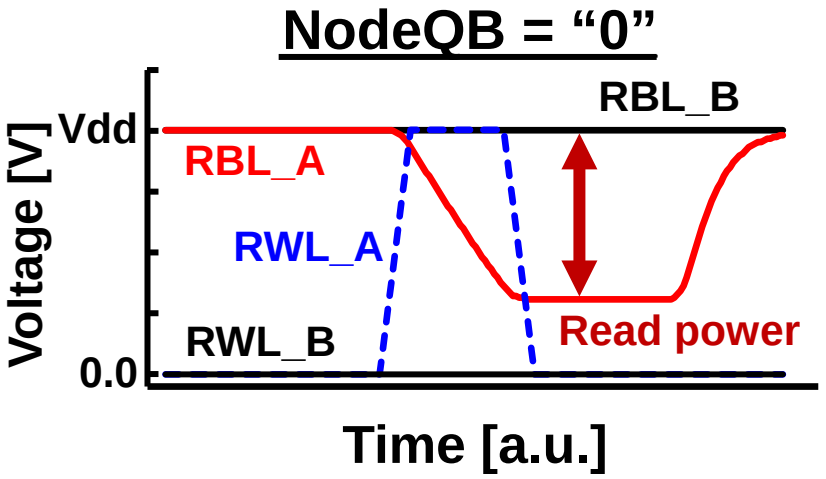


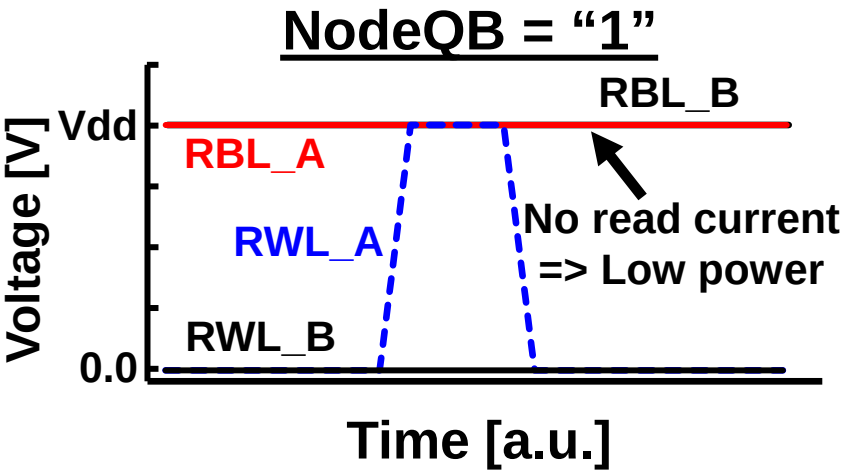

3-port: Single NMOS transistor is used as read port.

**Three-port SRAM is realized in the same cell area and at the same number of transistors as 2-p SRAM**

# Read operation waveforms

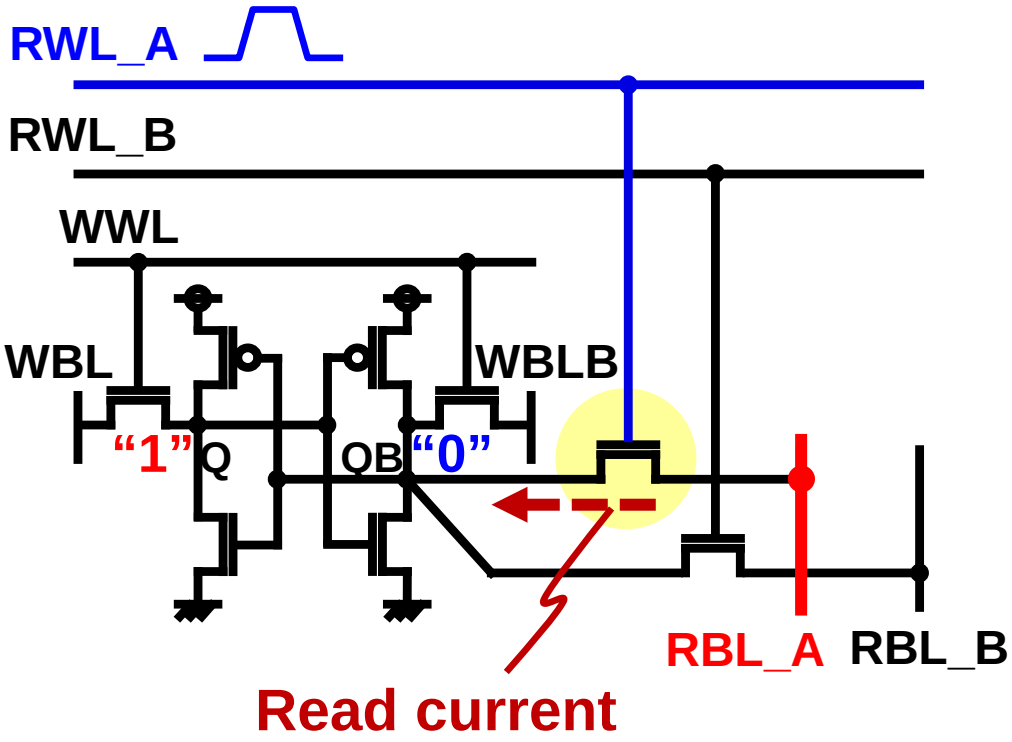


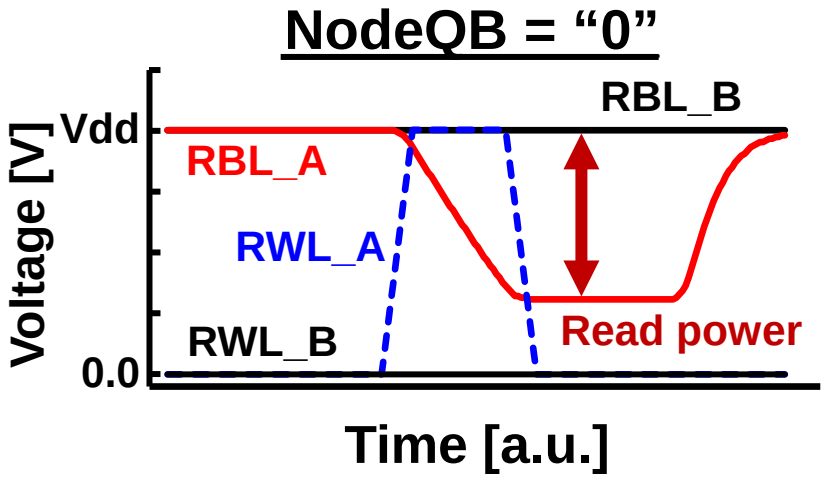




**Read power is reduced when "1" data is stored.**

# Read operation waveforms



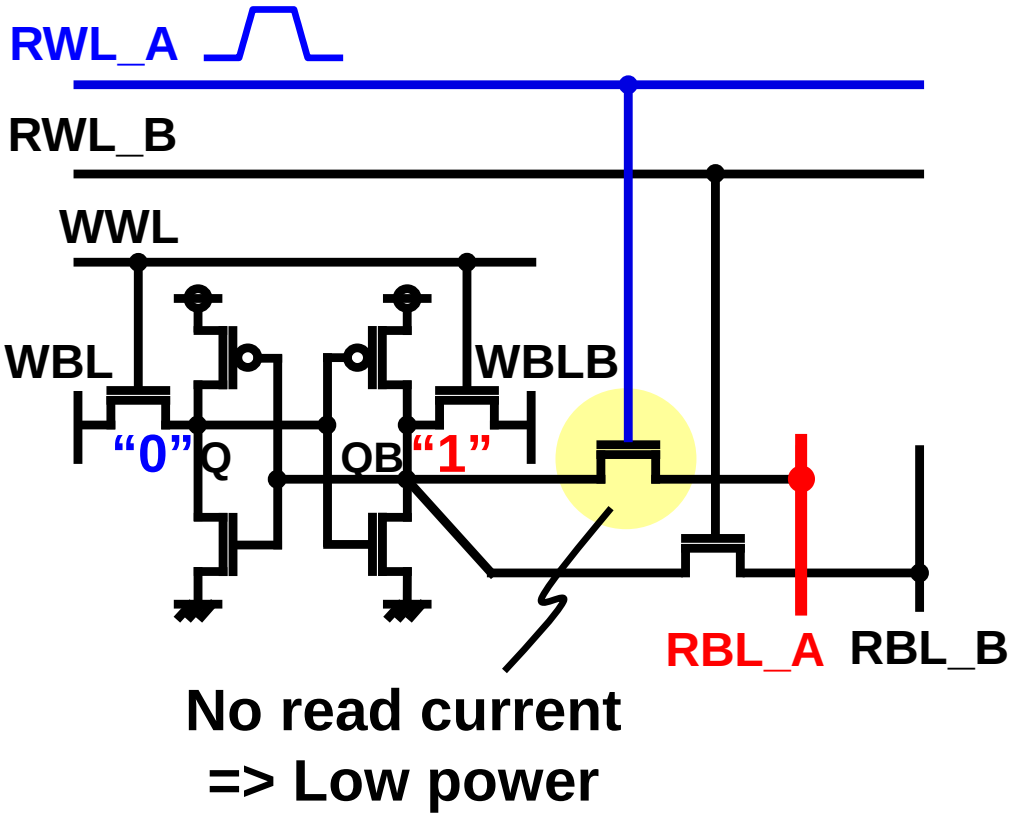







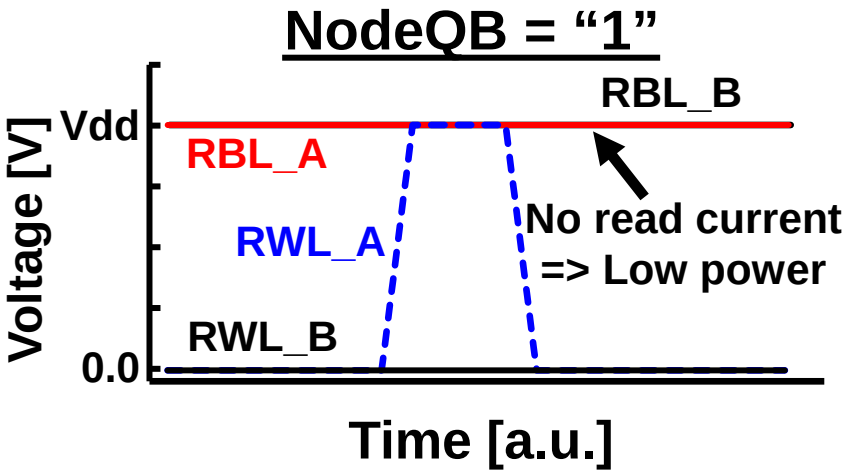
**Read power is reduced when "1" data is stored.**

# Read operation waveforms





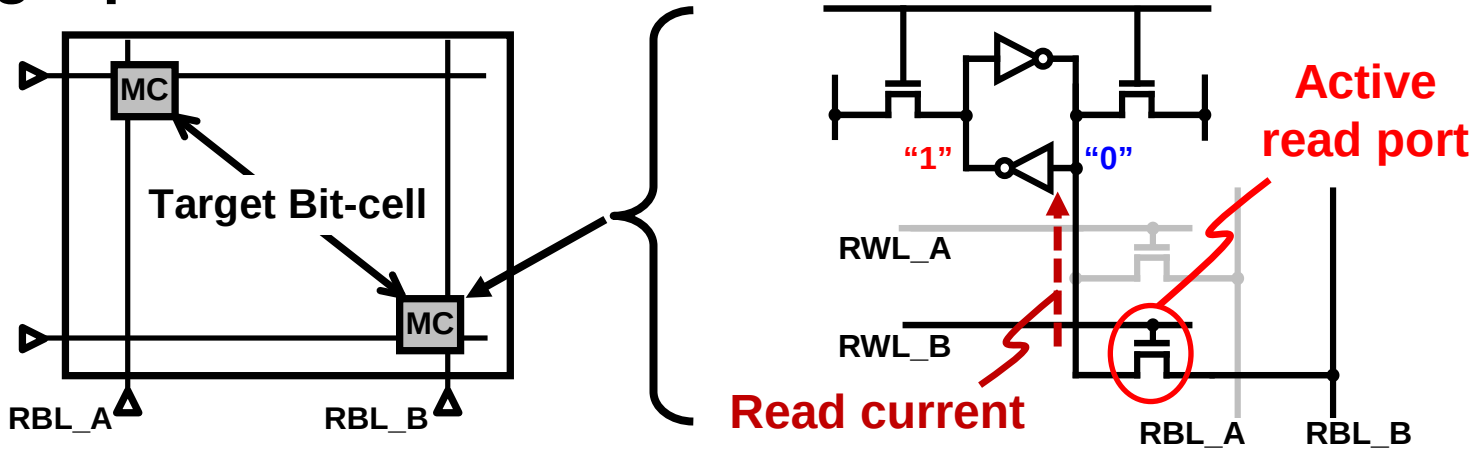




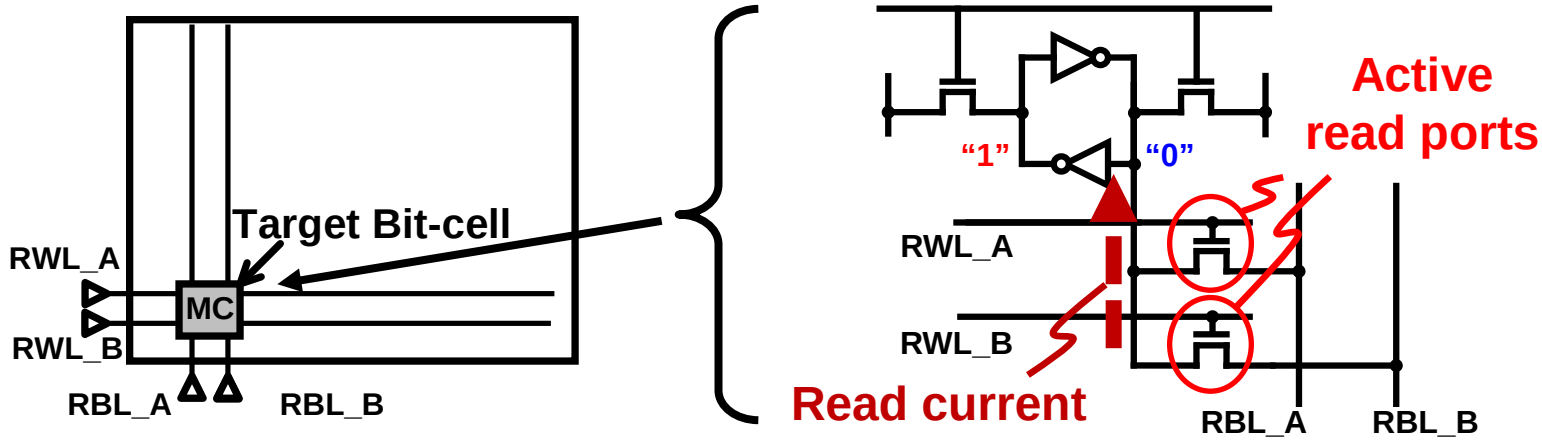

**Read power is reduced when "1" data is stored.**

# Variety of access conditions

- Single port condition

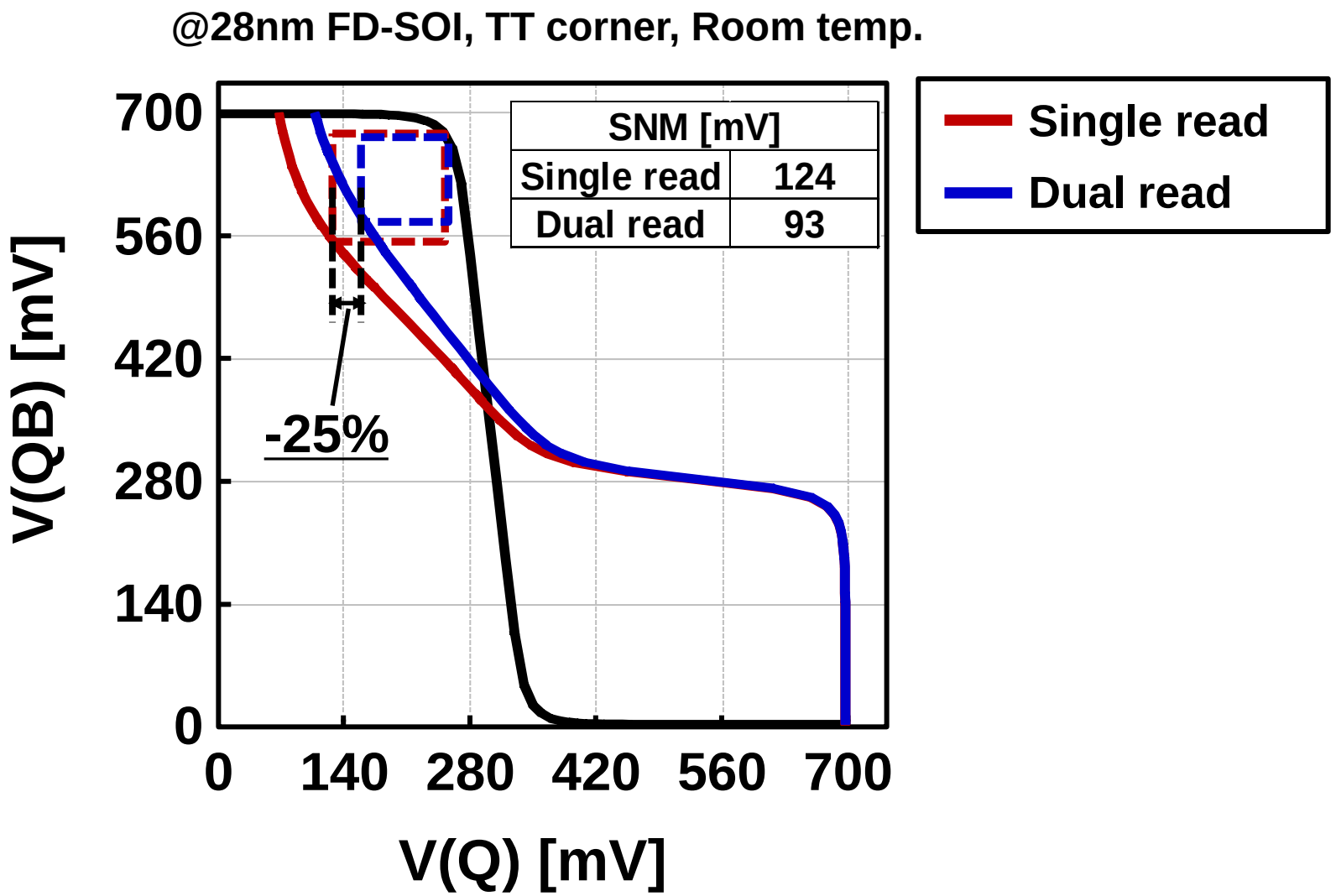



- Dual port condition

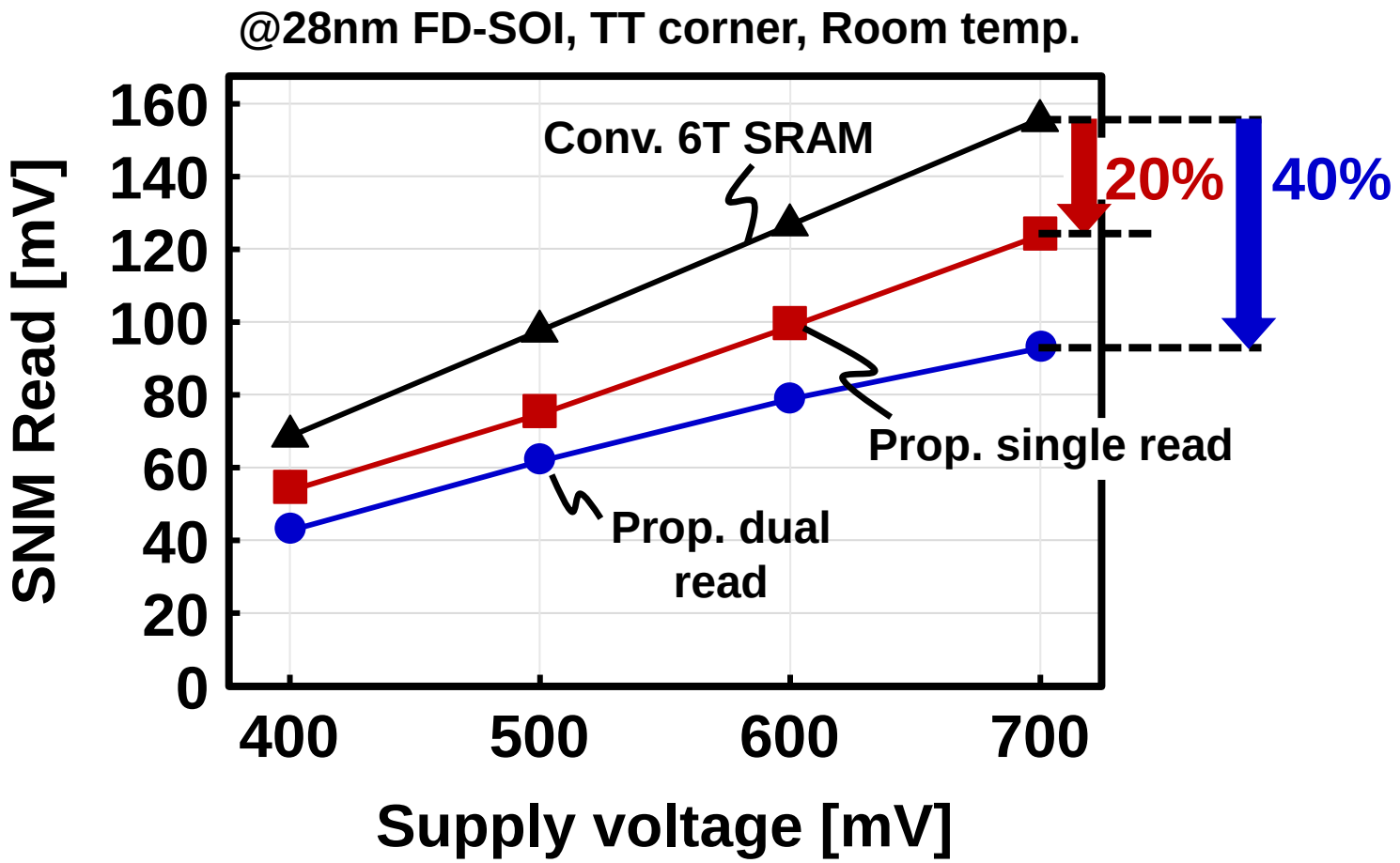



**Dual port condition cause read margin deterioration!**

# Read margin (Static Noise Margin)

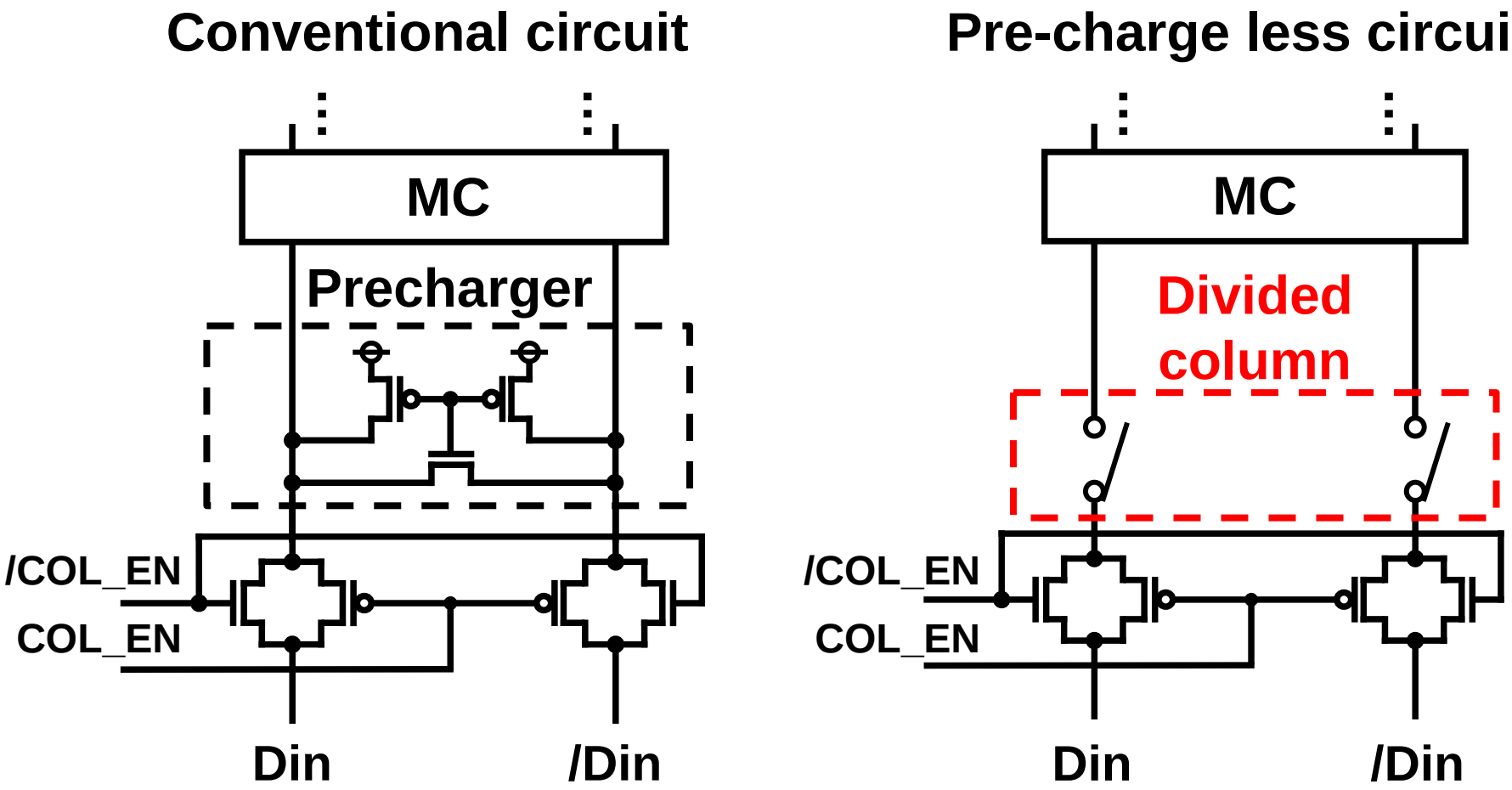


# Read margin (Static Noise Margin)




**Sufficient SNM remain for stable operation even under the dual read condition.**

# Pre-charge less write operation




**Pre-charge less write circuit and divided column structure effectively reduce the write energy.**

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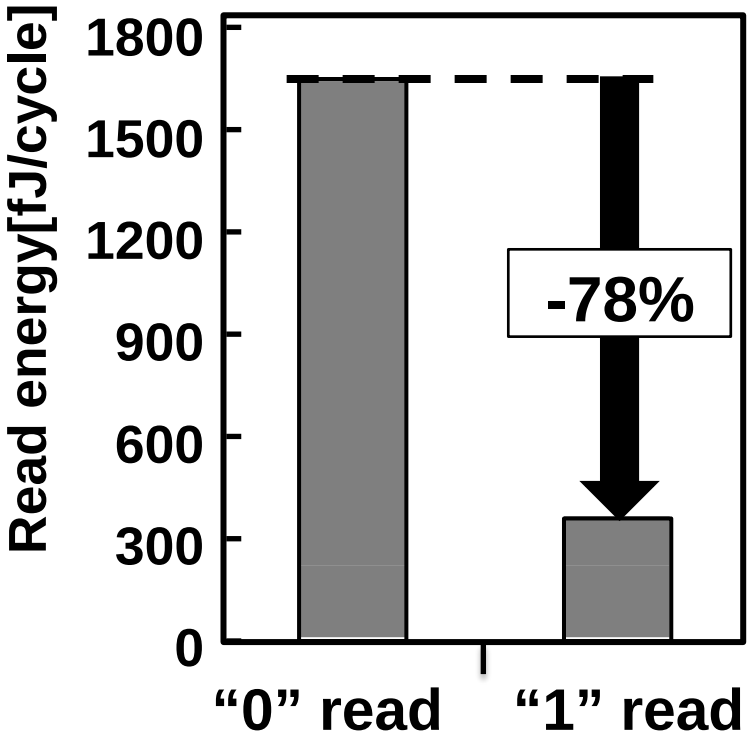
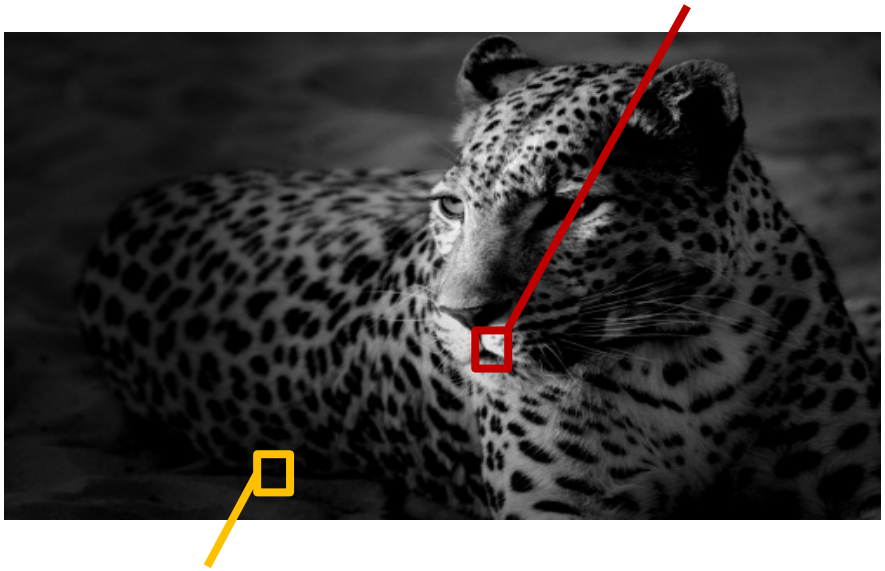
# Concept of majority logic(1/2)

**Read energy comparison**
**“0” read vs “1” read**



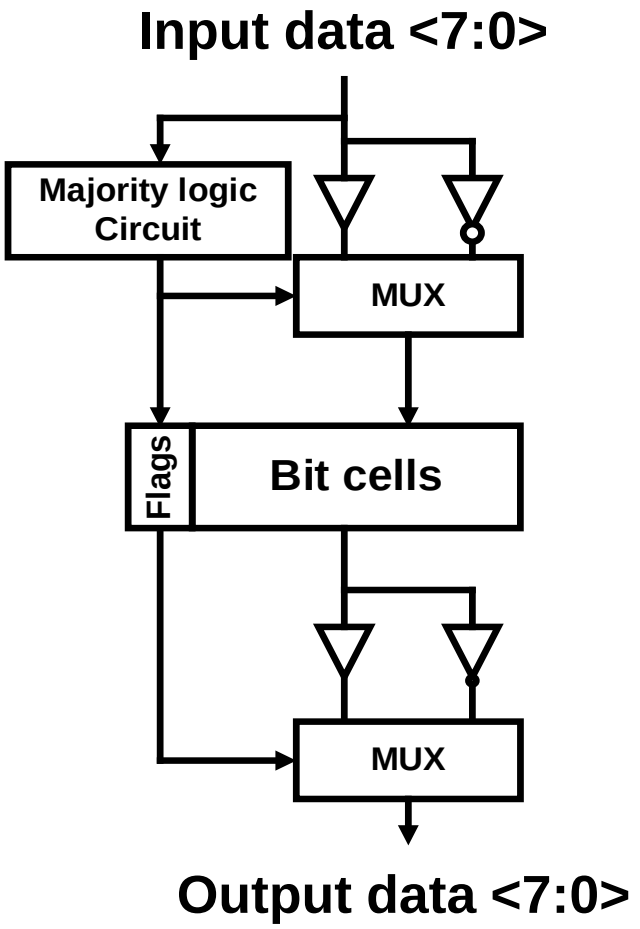

**Bright pixels:**
**Many “1” data stored as they are**

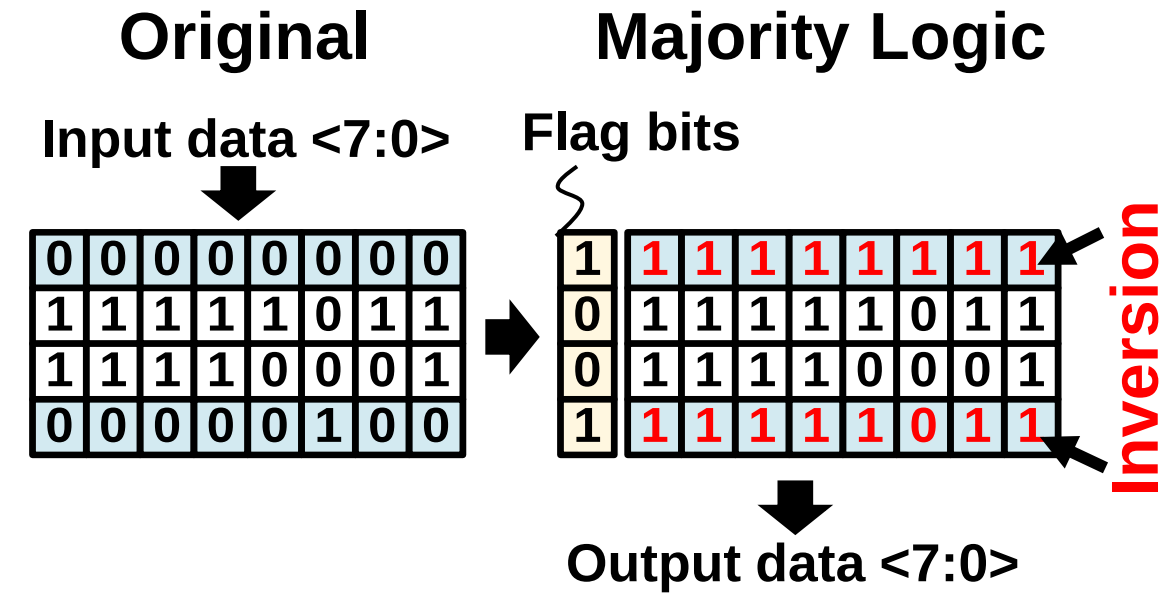


**Dark pixels:**
**Many “0” data inverted**

**Many “0”s are inverted by majority logic.**

# Concept of majority logic(2/2)

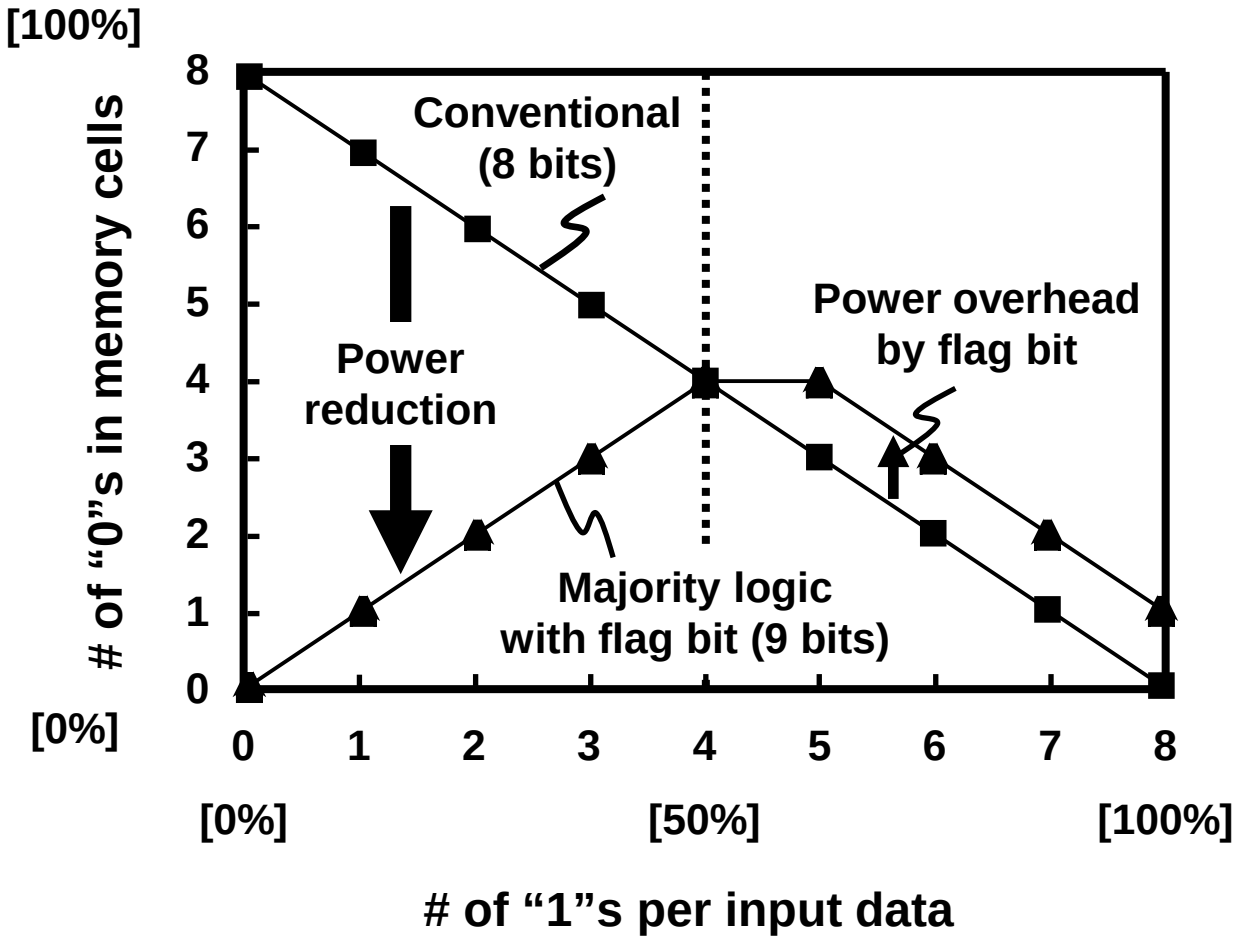



19 “0”s > 13 “1”s ➡ 7 “0”s > 29 “1”s

**Increase number of “1”s by “0”s inversion.**

# Power overhead of majority logic




**Majority logic statistically saves 18% of an RBL power even if the data are random.**

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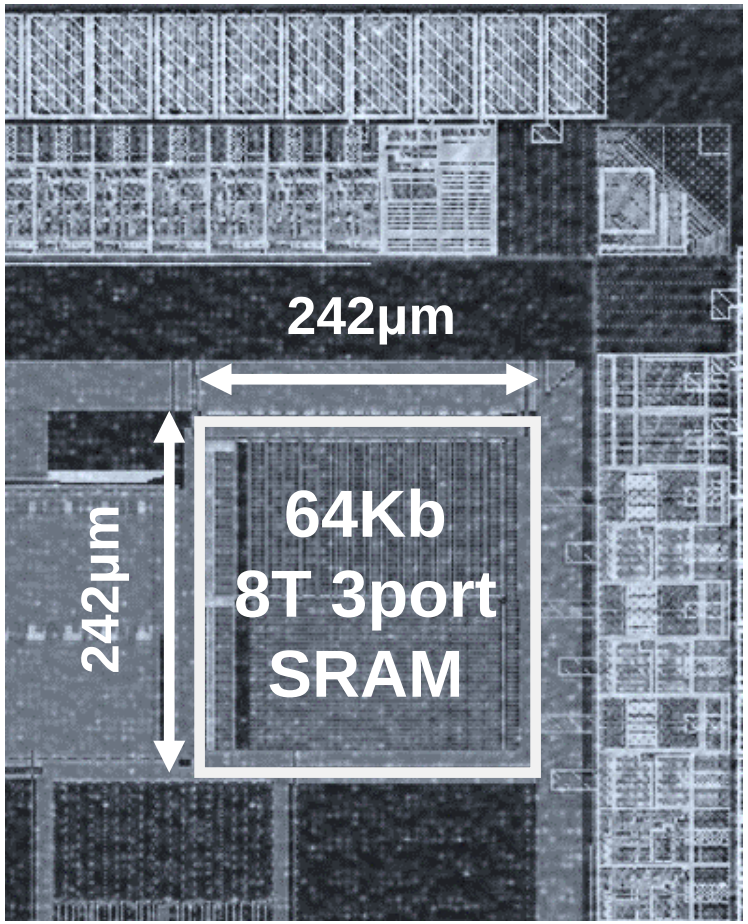
# Chip implementation




Chip photograph

| | |
|---|---|
| Technology | 28nm FD-SOI |
| Supply voltage | 0.4-0.7V (Memory macro) |
| | 1.8V (I/O) |
| Chip area | 1.0mm$^2$ |
| Macro size | 242x242um$^2$ |
| Macro configulation | 64Kb (32Kb X 2), 16bits/word |
| Cell size | 0.384x1.457um$^2$ |
| Frequency | 7.14MHz@0.46V, 50MHz@0.7V |

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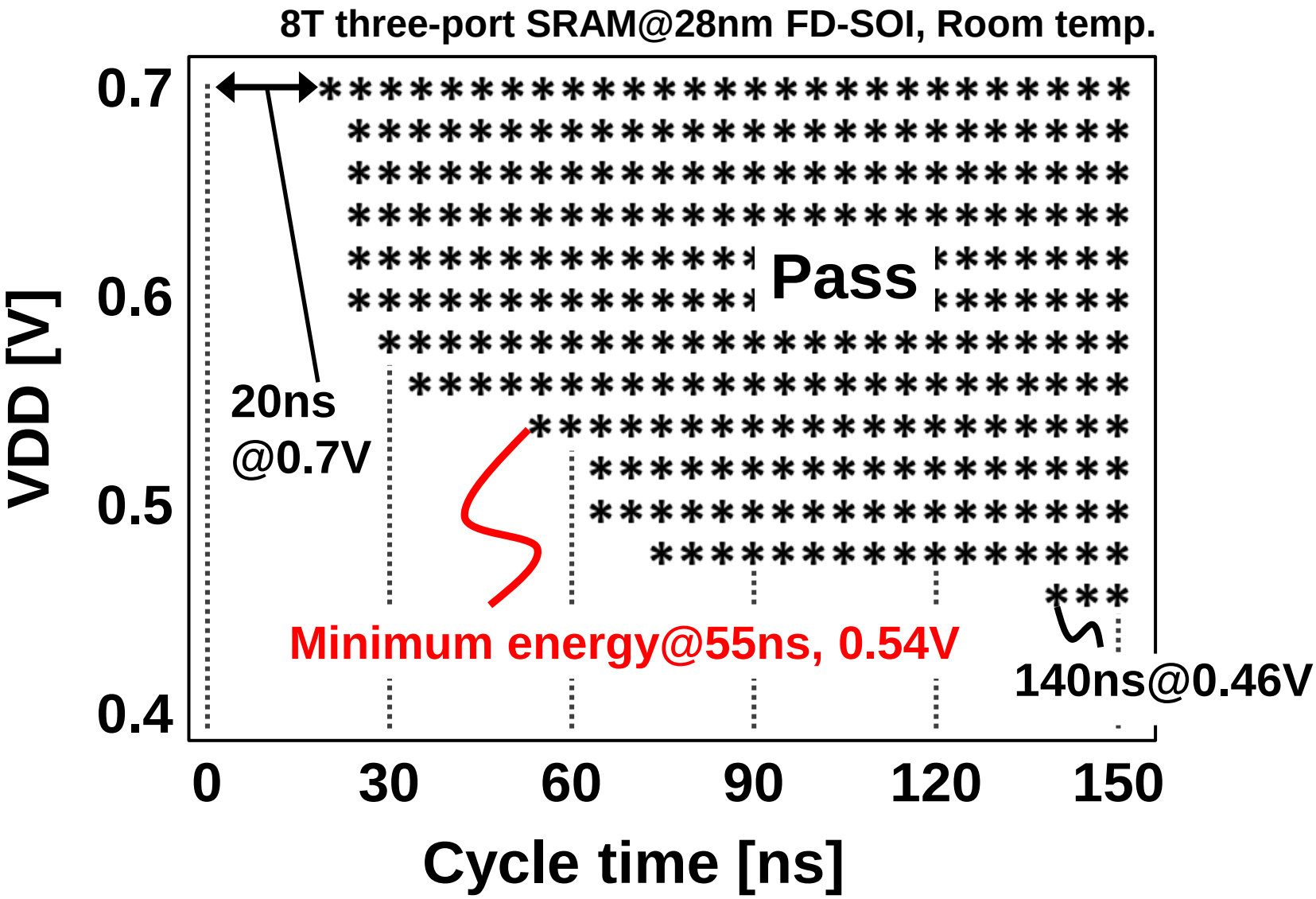
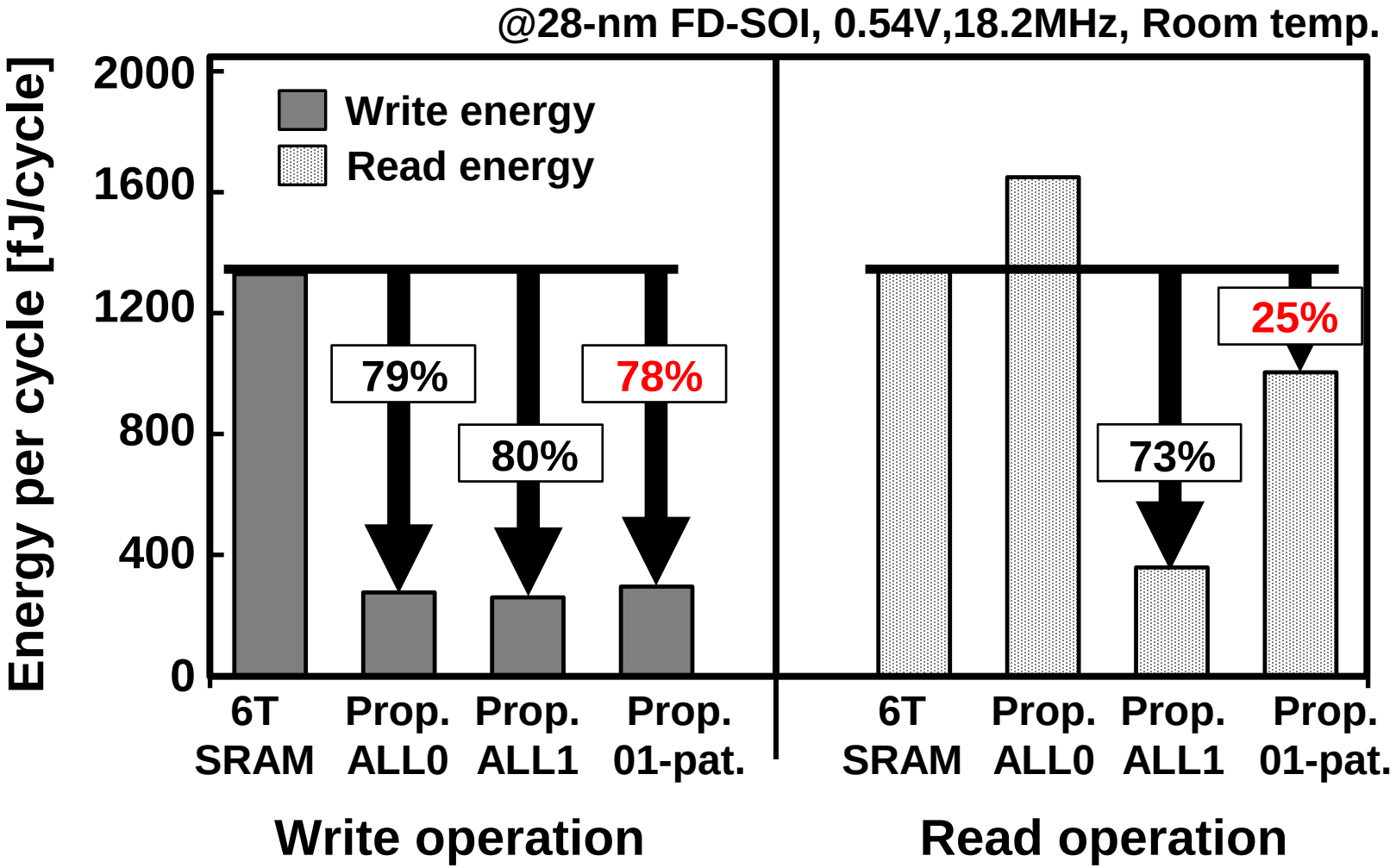
# Shmoo plot


8T three-port SRAM@28nm FD-SOI, Room temp.
VDD [V]
0.7
0.6
0.5
0.4
Pass
20ns
@0.7V
Minimum energy@55ns, 0.54V
140ns@0.46V
0
30
60
90
120
150
Cycle time [ns]

# Measured energy consumption




**298fJ/cycle at 01-pat. writing, 1000fJ/cycle at 01-pat. reading**

# Application for image processor

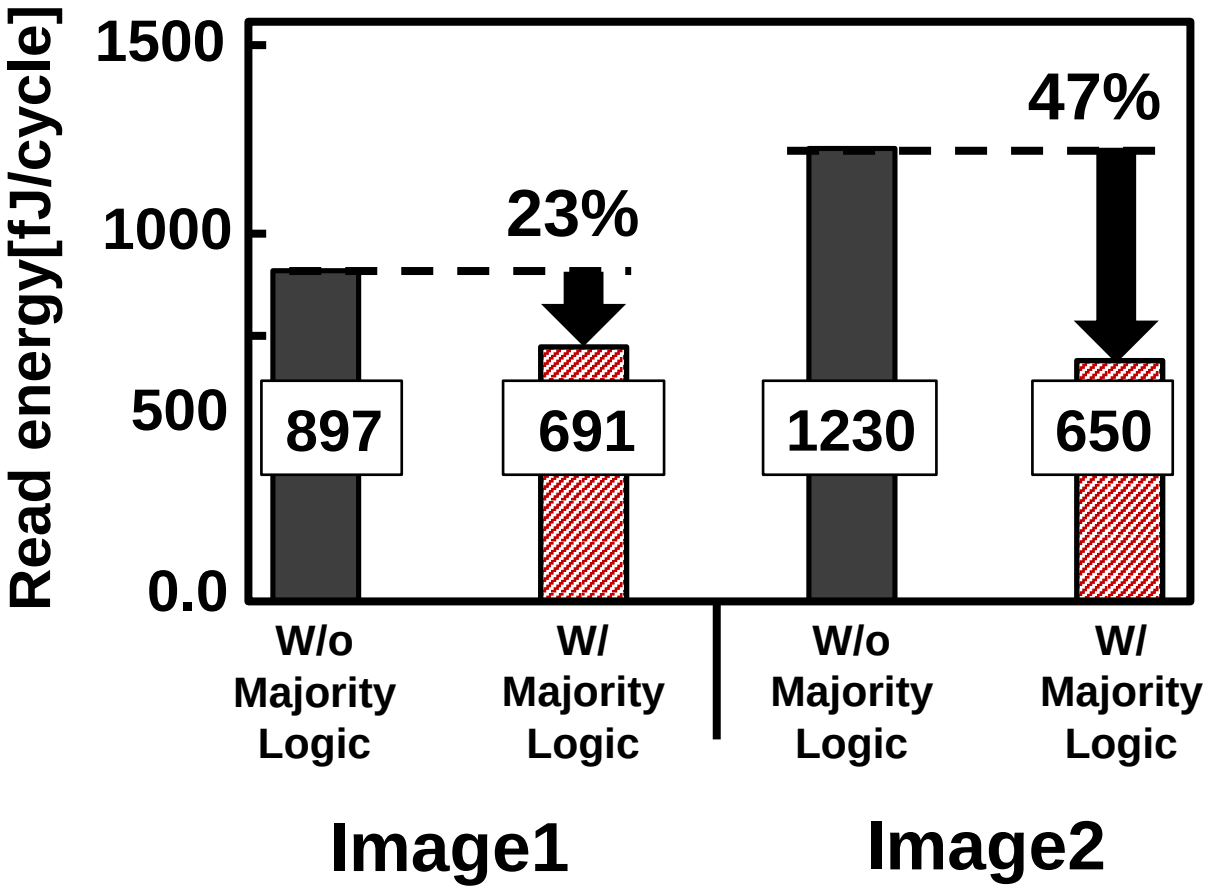



Image1

Image2

**Read energy is reduced by 47% in a dark image**

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# Summary

- I presented 8T three-port SRAM for Image processor.
- The proposed SRAM is comprising 1-write/2-read ports and the majority logic to save active energy.
- Test chip achieves 298-fJ in the write cycle and 650-fJ in the read cycle with the help of the majority logic.

# Acknowledgment

**We would like to thank STMicroelectronics for chip implementation.**

**This work was supported by STARC,
VLSI Design and Education Center (VDEC),
The University of Tokyo with the collaboration with Cadence Corporation,
Mentor Graphics Corporation, Synopsys Inc.,
CMP Inc., and Renesus Electronics Corporation.**

# Appendix

# Appendix: write shmoo plot