A Novel Switched-Capacitor-Filter Based Low-Area and Fast-Locking PLL

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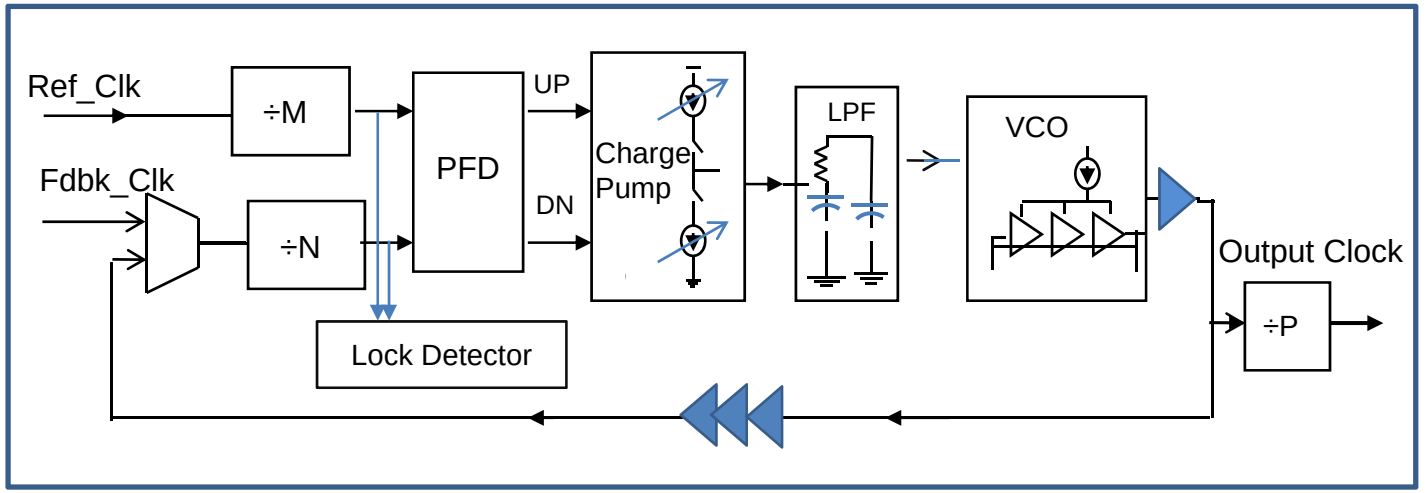
Outline

- Introduction
- Motivation
- Previous Work
- Proposed Technique
- Simulation Results
- Measurements
- Comparisons
- Conclusion

Introduction "General PLL Block Diagram"

Modern products use phase locked loops (PLLs) to satisfy clocking requirements.

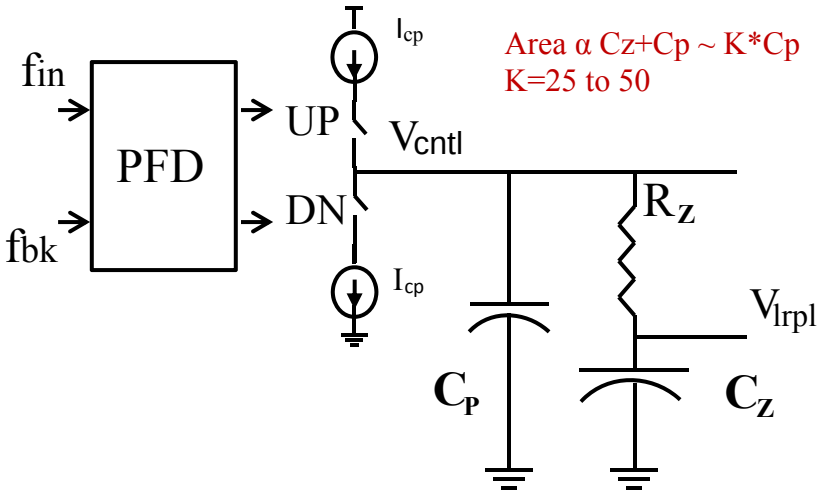
System silicon area is impacted by PLL silicon area.
System performance is impacted by PLL lock-time and noise performance.



General Analog PLL block diagram

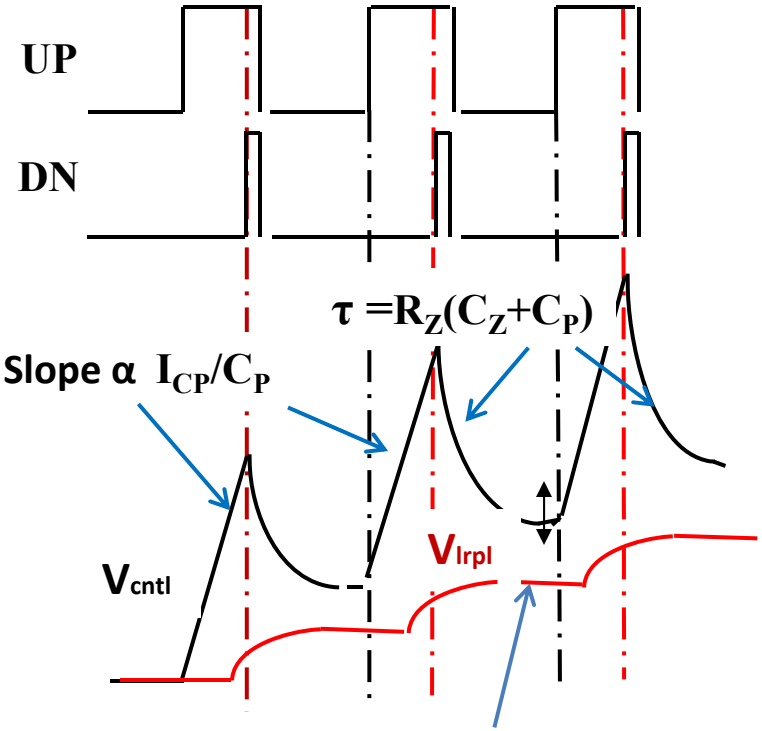
PLL silicon area is mainly impacted by PLL-LPF capacitors sizes.
PLL Lock time is impacted by PLL-LPF capacitors sizes, charge-pump current, and VCO gain "system natural frequency ω_N".

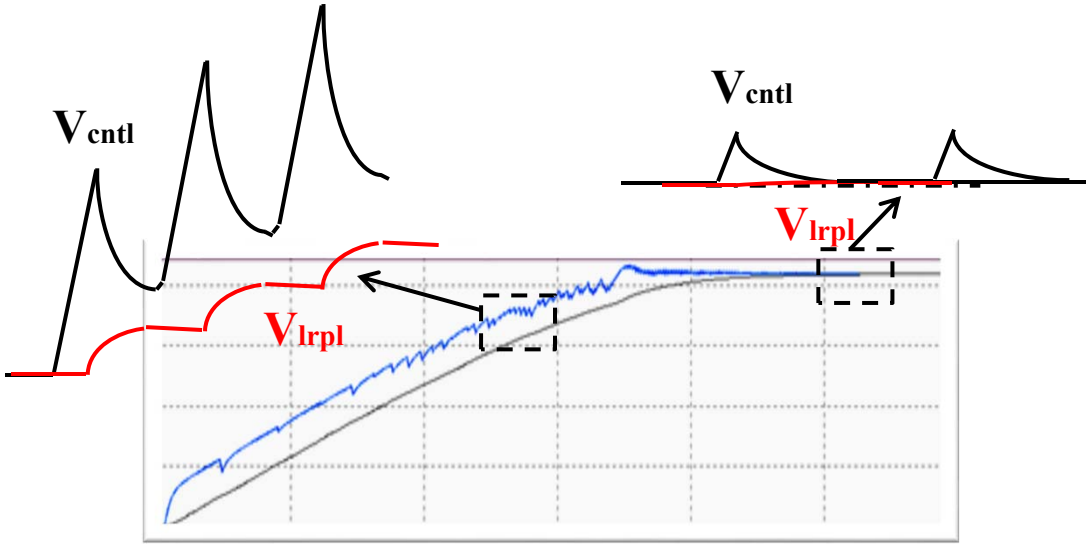
Introduction "(RC) LPF Time Domain Response"



Area α Cz+Cp ~ K*Cp
K=25 to 50

General PLL passive LPF





PLL control voltage (V_{cntl}) and low ripple internal voltage (V_{lrpl}) relationship.

Motivation

1- **Reduce analog PLL silicon area while keeping analog PLL benefits:**

- **Fast locking**
- **Simple architecture**
- **Excellent Noise performance.**

2- **Achieve faster PLL locking without affecting**

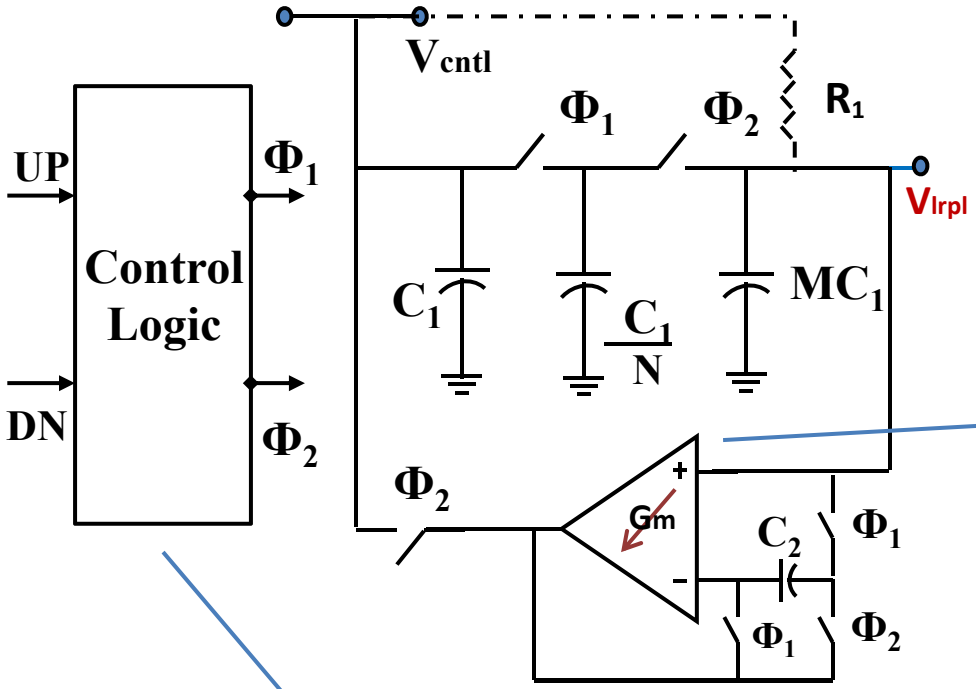
- **PLL stability, phase margin.**
- **Almost no area or power penalty.**

3- **Architecture that is Immune to device gate leakage**

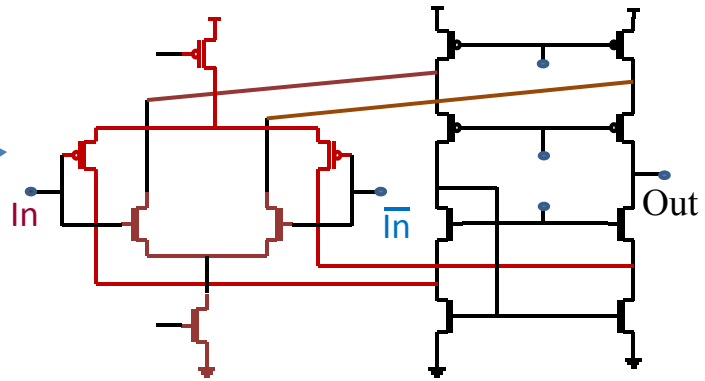
- **Allow using device gate capacitance as well as metal capacitance in the LPF.**

Proposed Architecture

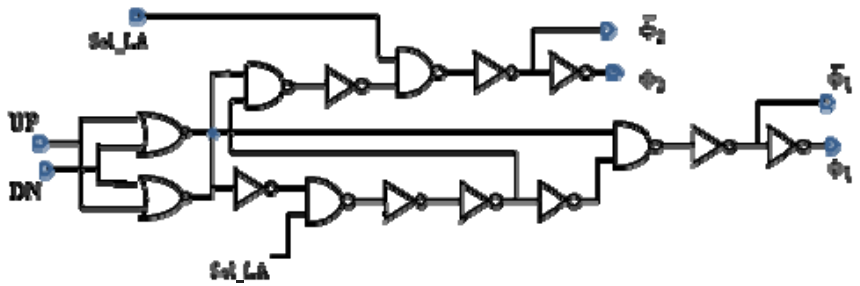
Switched-Capacitor-based **LPF** Architecture



(SC) Based LPF



Rail-to-Rail OpAmp for the SC LPF



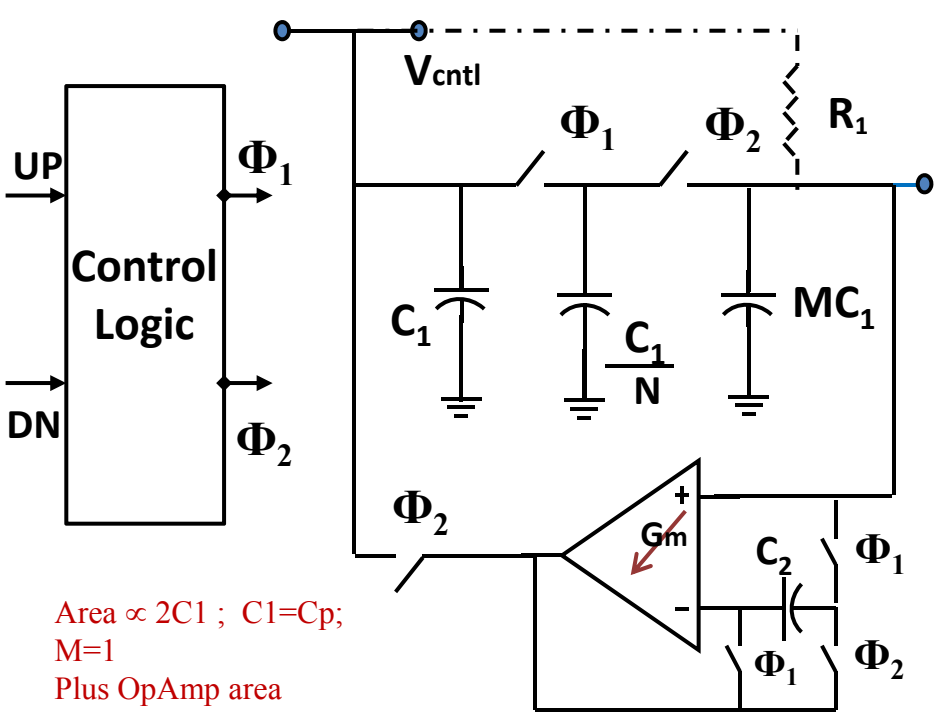
A non overlapping control signals generator

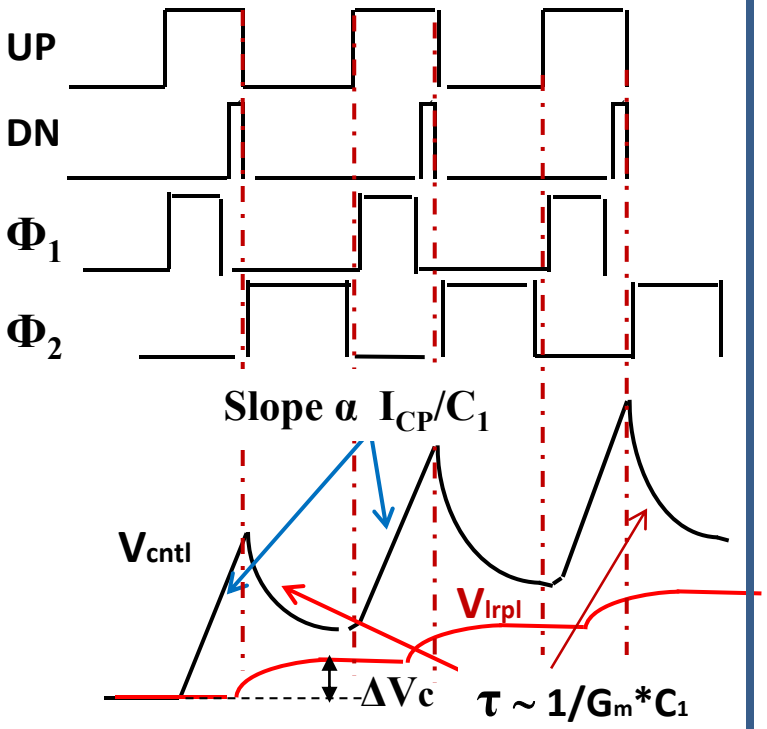
Proposed Architecture

Switched-Capacitor-based **LPF** Time Domain Response

- Operation:

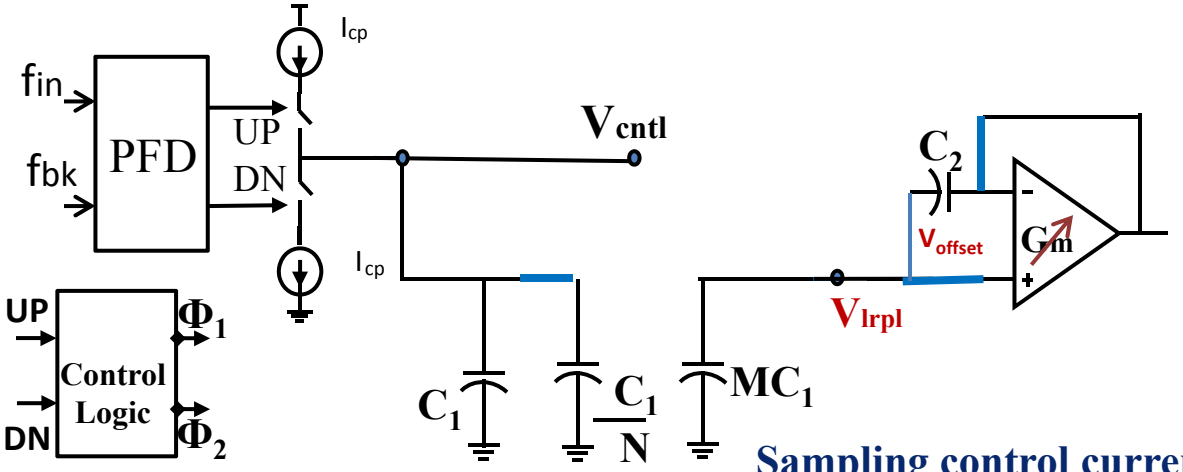
Generate UP/DN sampling current pulses, just like the traditional (RC) LPF, then redistribute, integrate, a fraction of (1/N+1) of this control charge to a fraction-sized capacitor to generate similar control voltage level and behavior to traditional (RC) LPF.

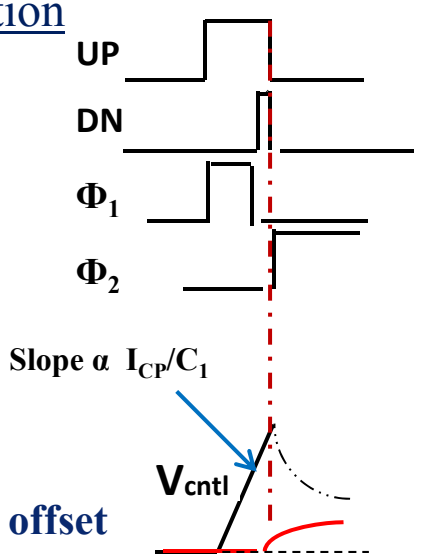




Proposed Architecture

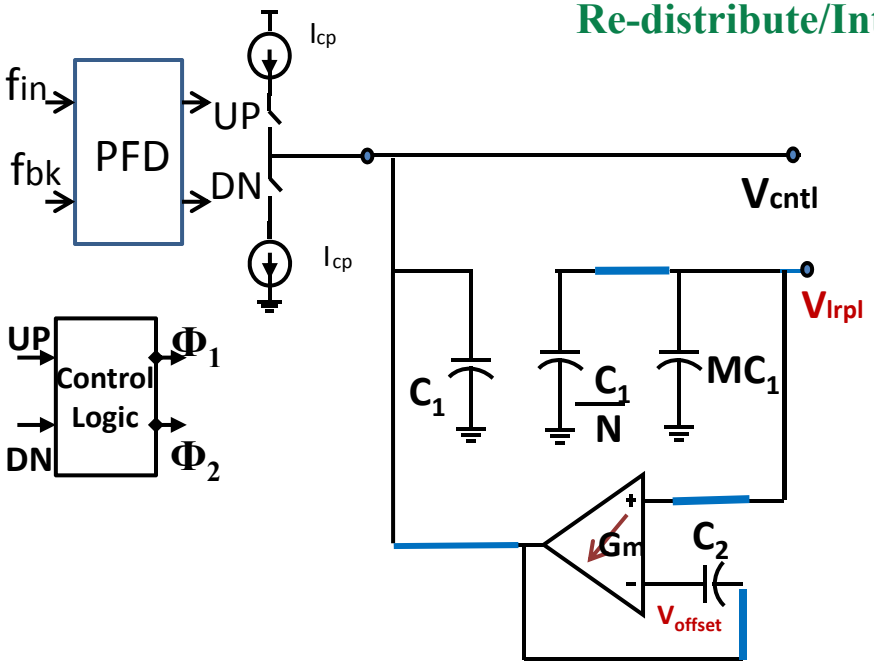
Switched-Capacitor-based **LPF** Discrete time Operation

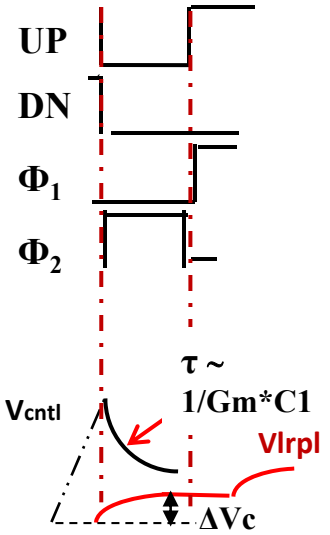




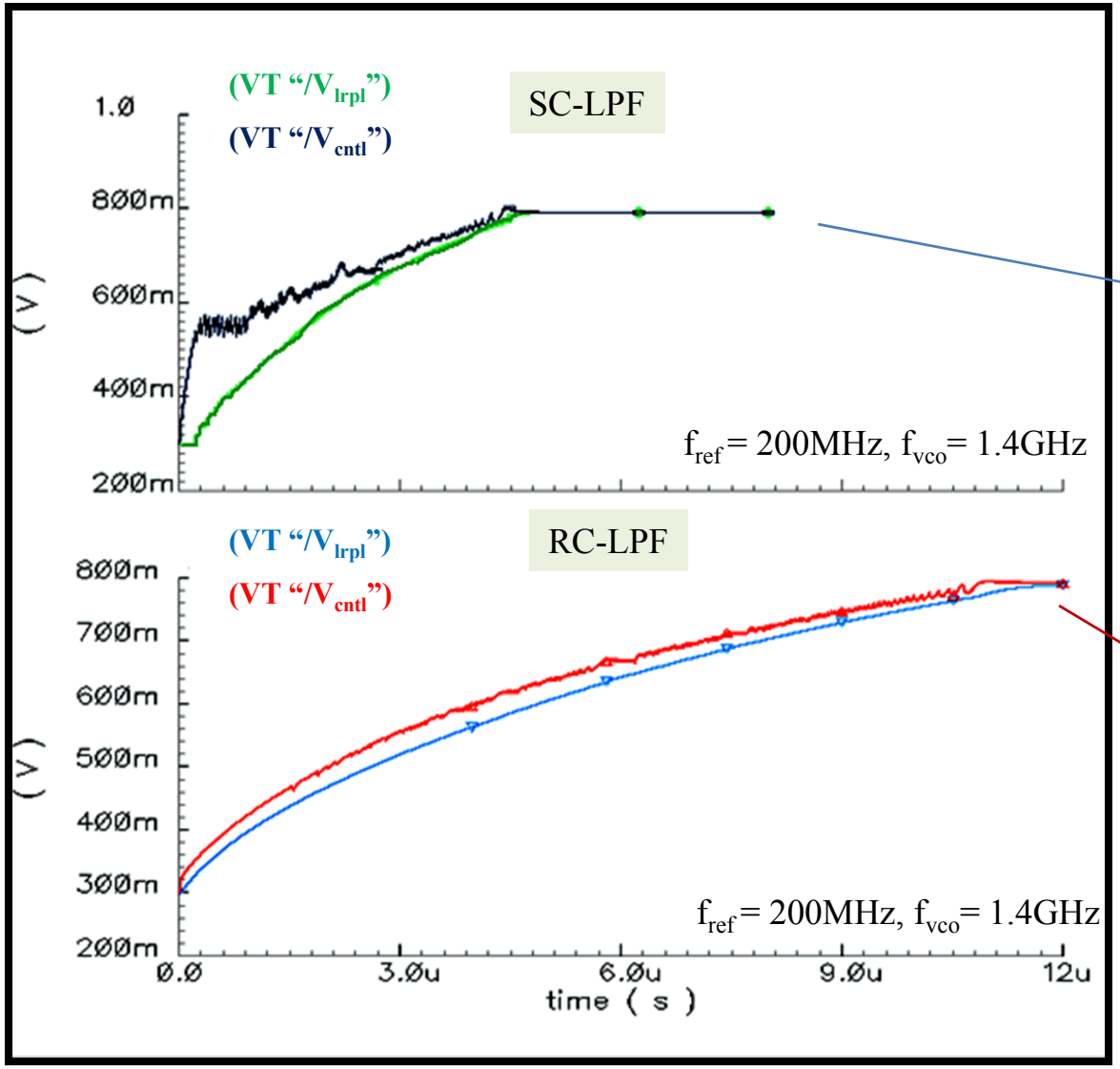
Sampling control current/Amp offset

Re-distribute/Integrate sampled charge





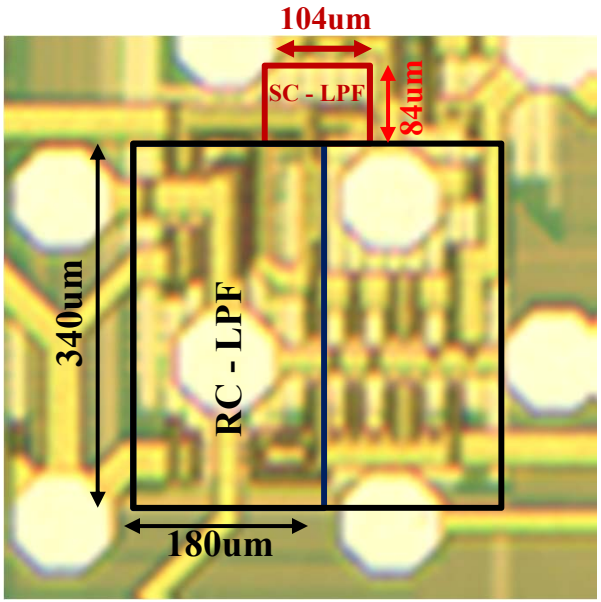
Simulations Results



Relationship between V_{cntl} and V_{lrpl} for both traditional (RC) LPF and (SC) LPF case.

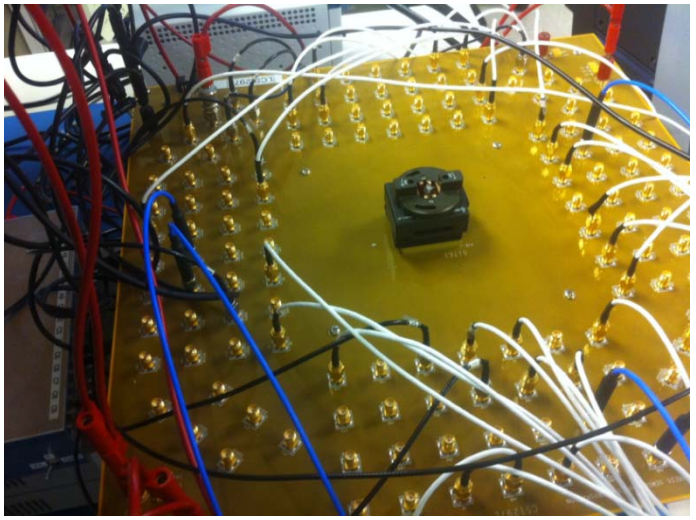
Measurements

The (SC) LPF scheme was implemented into a BIST mode PLL in a multi-port SRAM chip and fabricated using 65nm CMOS process.



Die Photo of a PLL with both (SC) and traditional LPFs

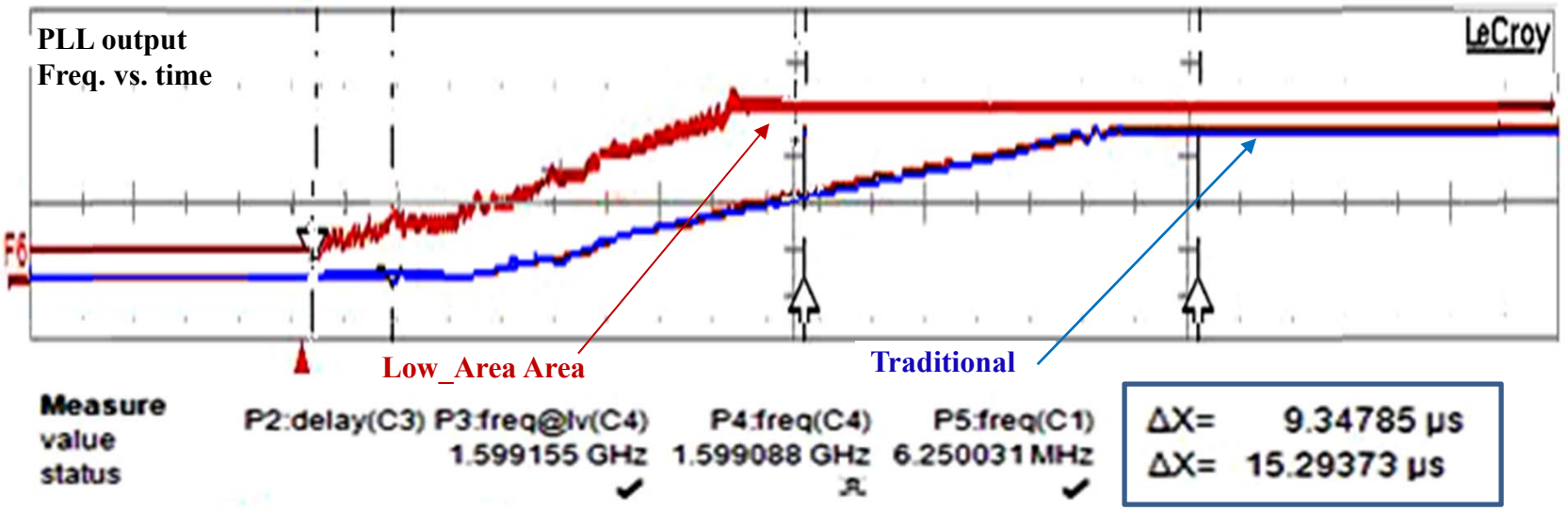
RC LPF area is 0.0612 mm^2 while the (SC) LPF area is only 0.0087mm^2,



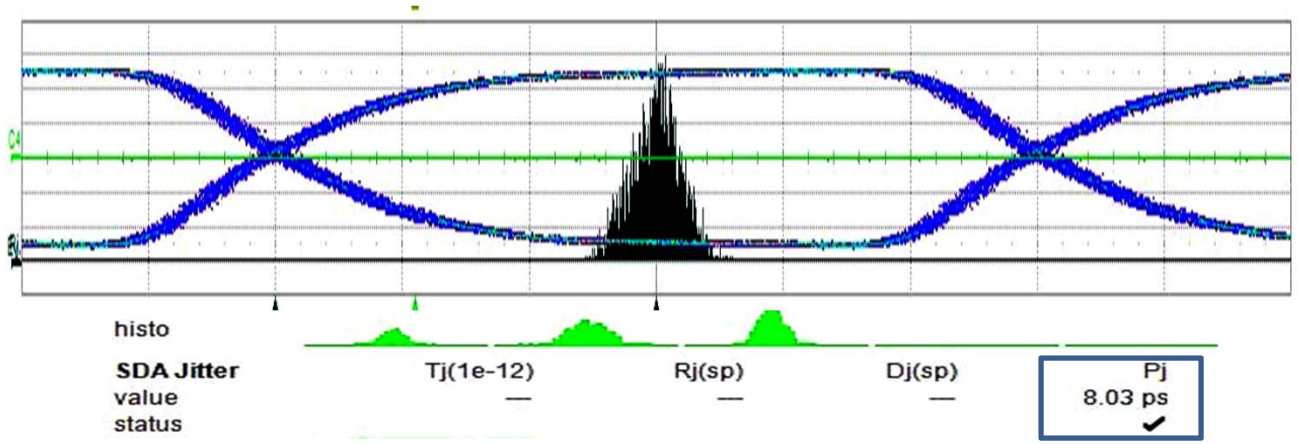
Testing board photo.

	RC-LPF	SC-LPF
Area	340μ×180μm	84μm×104μm
Cap sizes	C_Z=260pfF, C_P=16pF	C_1=8pF, C_1/N=250fF, C_2=150fF

Measurements



Measured PLL acquisition time with (SC) LPF vs. with (RC) LPF for f_{ref}= 200MHz, f_{vco}= 1.6GHz



Measured Period jitter with (SC) filter, f_{ref}= 100MHz, f_{vco}= 1.6GHz.

8.03pS pk-pk or 0.9pS RMS

Comparisons

COMPARISON OF PLL parameters between (RC) LPF and (SC) LPF

Parameter	Description	Traditional Filter	New Filter
Natural Frequency squared	T.F. peaking frequency	$\omega_N^2 = \frac{K_{cp} \cdot K_{VCO}}{2\pi (C_Z + C_P)}$	$\omega_N^2 = \frac{K_{cp} \cdot K_{VCO}}{2\pi (N+2) C_P}$
PLL O.L. BW.	PLL open loop BandWidth	$OLBW = \frac{K_{cp} \cdot K_{VCO}}{2\pi L} \frac{R_Z \cdot C_P}{(C_Z + C_P)}$	$OLBW = \frac{K_{cp} \cdot K_{VCO}}{2\pi L \cdot G_m} \frac{1}{N+2}$
ξ Damping Factor	T.F. damping/stability	$\xi = \frac{R_Z}{2} \sqrt{K_{cp} \cdot K_{VCO} \frac{C_Z}{L}}$	$\xi = \frac{1}{2 G_m} \sqrt{K_{cp} \cdot K_{VCO} \frac{(N+1) C_P}{L}}$

For : Ron | switch << 1/Gm , M=1, Cp=C1, Gm : OTA transconductance, and L: feedback divider Value

COMPARISON OF PERFORMANCE WITH PRIOR WORK

Refs	This work	Song [6]	Cath [5]	Musa [1]	PU [7]
f_{out} (GHz)	0.2-2.0	2.5	8-10	0.5-1.6	0.1-0.4
f_{in} (MHz)	40-800	10	NA	40-300	NA
Tech.	65nm	0.18µm	28nm	65nm	0.18µm
Power	9mW	16mW	15.5mW	0.97mW	12.2mW
Area mm^2	0.049	0.36	0.093	0.022	0.36
Jitter pS (rms/pp)	0.9/8.03	NA	NA	1.81/19.4	NA

Conclusion

- **A new low-area fast-locking PLL was successfully built, simulated, and tested using a new switched-capacitor (SC) LPF.**
- **The new technique has successfully lowered PLL LPF area by a large factor of "7X", and reduced lock time by a factor of "1.5X"**
- **Simulations and test results show that the new technique successfully reduces analog PLL area and lock time with small penalty in noise performance.**
- **The new technique has no impact on PLL stability or power consumption and has no effect on any other PLL sub-block design/requirements.**
- **The new (SC) LPF design provides immunity to device gate leakage in the LPF.**

References

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