A 10 mW 60GHz 65nm CMOS DCO with 24% Tuning Range and 40 kHz Frequency Granularity

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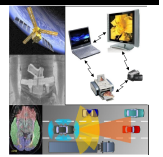
Motivation

- **Why millimeter-wave bands?**
  - Large available bandwidth → Higher data rates
  - Many emerging applications including:
    - LTE backhaul, automotive radar, medical imaging.
- **Frequency Synthesizers**
  - LO generation in transceivers
  - Constant envelope modulation in transmitters
- **Why All-Digital Frequency Synthesizers?**
  - Digital loop filter → compact and reconfigurable.
- **DCO is a crucial part of All Digital Frequency Synthesizer.**
  - Wide tuning range (15%) → to cover the whole 60GHz ISM band (57GHz-66GHz).
  - Fine resolution → to minimize quantization noise which degrades out of band phase noise.



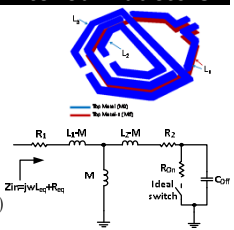
Wide Tuning Range: Switched Inductors

- Changing the effective inductance (L_{eq}) seen from the primary side
- When the secondary side switch is turned off:

$$L_{eq} \approx L_1 - \frac{\omega M^2}{\omega L_2 - (wC_{off})^{-1}} \qquad R_{eq} \approx R_1$$

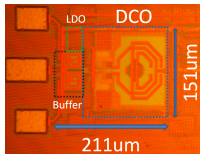
- When the secondary side switch is turned on:

$$L_{eq} \approx L_1 - \frac{M^2}{L_2} \qquad R_{eq} \approx R_1 + \left(\frac{M}{L_2}\right)^2 (R_2 + R_{on})$$

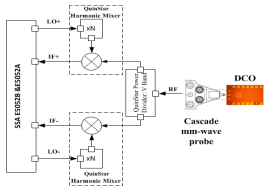


- T-Model of a transformer with non ideal switch

Measurement Setup



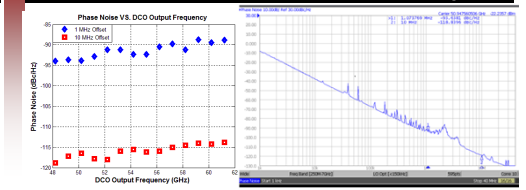
- Die photo of proposed DCO with output buffer



- Measurement setup of proposed DCO.

- Power divider, and two V-band harmonic mixers were used to down convert the DCO outputs to 1GHz IF signals.

Phase Noise Results & Performance Summary



- Phase noise measurement at output frequency of 50.95GHz

- The highest frequency band, when both switched inductors on shows the highest phase noise.
- The proposed DCO has the smallest active area and highest reported FOM, in mm-wave band, due to the wide tuning range.

Table I Performance summary and comparison of DCOs

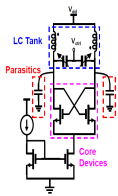
Ref.	[2]	[3]	[5]	[4]	This Work
Tech.	CMOS 90nm	CMOS 90nm	CMOS 90nm	CMOS 65nm	**CMOS 65nm**
F_{out}(GHz)	56.33~ 62.16	51.3~ 53.3	37.6~ 43.4	56.4~ 63.4	**48.1~ 61.3**
TR(%)	10	4	14	11.6	**24.13**
Resolution(Hz)	160K	1.8M	24K	1.64M	**39K**
PN @1MHz (dBc/Hz)	-92.5~ -95.5	-116.5 @10MHz	-109 @10MHz	-92	**-95.1~ -88.8**
Power(mW)	12	2.34	19	11	**10**
Area (mm^2)	0.16	0.09	0.075	-	**0.032**
FOM_T(dB)	-177.4 ~ -179	-179.2	-180.6	-178.42	**-186.4 ~-182**

$$FOM_T = PN(\Delta f) - 20\log\left(\frac{F_{out} * TR}{\Delta f * 10\%}\right) + 10\log\left(\frac{Power(mW)}{1mW}\right)$$

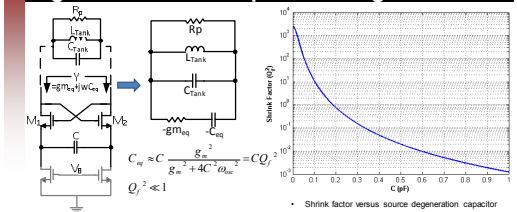
*: Using 12-bit dithering controlled by 2nd $\sum\Delta$ modulator.

Design Challenges of 60GHz DCO

- **Require greater than 20% tuning range of 60GHz DCO including margin for PVT variation**
  - Trade-off between tuning range and quality factor.
- **Achieving 100KHz resolution, to not introduce high quantization noise, requires a capacitor <0.5aF!**
  - Sigma delta dithering[1]: frequency of dithering should be very high.
  - Capacitive divider network: sensitivity to mismatches and parasitics.
- **60GHz DCO have other challenging aspects**
  - Transistors have small gain closed to f_T.
  - Poor phase noise.
  - Limited tuning range due to significant parasitics.



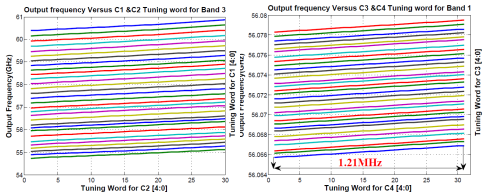
High Resolution: Capacitive degeneration



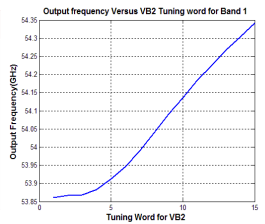
$$C_{eq} \approx C\frac{g_m^2}{g_m^2 + 4C^2\omega_{osc}^2} = CQ_f^2 \qquad Q_f^2 \ll 1$$

- Shrink factor versus source degeneration capacitor

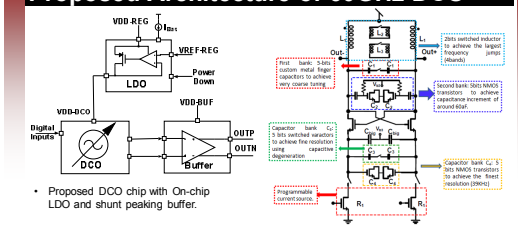
Measurement Results



Parameter	Tuning Range
$L_{2,3}$ (2bits)	48.1GHz-60.8GHz
C_1 (5bits)	175MHz
C_2 (5bits)	12.25MHz
C_3 (6bits)	450 KHz
C_4 (5bits)	39 KHz
V_{B2} (4bits)	500 MHz



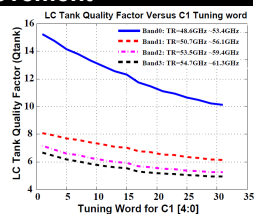
Proposed Architecture of 60GHz DCO



- Proposed DCO chip with On-chip LDO and shunt peaking buffer.

Quality Factor Improvement

- Capacitor bank C_1
  - Custom designed
  - 4 metal layers with wide metal traces.
- Capacitor bank C_2
  - ac-coupled to the inductor
  - Biased at external voltage (V_{B2}) controlled by a 4-bit DAC.



References

[1] R. B. Staszewski, *et al.*, "ADPLL and transmitter for mobile phones", *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2469-2482, Dec. 2005.

[2] Wu Wanghua, *et al.*, "High-Resolution Millimeter-Wave Digitally Controlled Oscillators With Reconfigurable Passive Resonators,", *IEEE J. Solid-State Circuits*, vol. 48, no. 11, pp. 2785-2794, Nov. 2013.

[3] R. Genesi, *et al.*, "A 53 GHz DCO for mm-wave WPAN", *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 571-574, Sept. 2008.

[4] Wu Wanghua, *et al.*, "A 56.4-to-63.4 GHz Multi-Rate All-Digital Fractional-N PLL for FMCW Radar Applications in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1081-1096, May. 2014.

[5] Tai-You Lu, *et al.*, "Wide Tunning Range 60 GHz VCO and 40 GHz DCO Using Single Variable Inductor," *IEEE Transactions on Circuits and Systems I*, vol.60, no.2, pp.257-267, Feb. 2013.