Efficiency Improvement Techniques for RF Power Amplifiers in Deep Submicron CMOS (INVITED)

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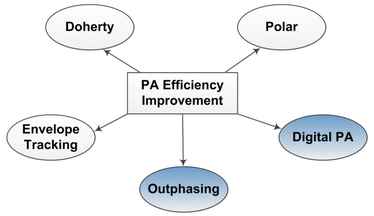
ABSTRACT

Integration of RF power amplifier (PA) in CMOS technology can help to reduce total solution cost and achieve small form factor in modern communication systems. To improve overall efficiency of the power amplifier supporting modulated signals with very high peak-to-average power ratio (PAPR), new transmitter and PA architectures are being explored by researchers. This paper reviews some of our recent developments in Texas Instruments in CMOS based PA architectures including PWM based digital transmitter, outphasing power amplifier and multi-mode outphasing PA designed in 45 nm CMOS.

INTRODUCTION

- Key requirements of modern communication systems: high efficiency, low cost and small form factor
- Cost and size reduction => integration of RF transceiver including PA in CMOS
- Issues in CMOS PA: reduced supply voltage, nonlinearity, low gain and low break-down voltage
- Advantages of CMOS PA: performance can be improved using DSP such as built-in self-test (BIST), self-calibration, digital pre-distortion (DPD)
- Efficiency: Modern modulation techniques have very high PAPR and traditional PAs show poor efficiency at large power back-off => reduced battery lifetime in handheld devices and higher heat sinking cost in base stations
- New PA architectures required for back-off efficiency improvement

PA EFFICIENCY IMPROVEMENT TECHNIQUES

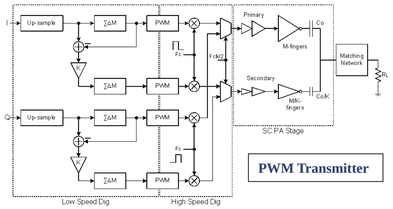


Transmitter architectures for efficiency improvement

- Switch-mode PAs (class-D, class-E etc.) have very high efficiency but a switch-mode PA alone can not handle amplitude modulation
- Outphasing and PWM based digital PA architectures have been chosen that incorporate switch-mode PAs and can support amplitude and phase modulated signals
- Efficiency is improved due to inherent switching nature of these architectures
- **PWM Digital PA:** Switch-mode class-D PAs generate RF pulses and number of pulses are changed to create amplitude modulation with time interleaved I-Q data
- Less switching activity for smaller amplitudes => back-off efficiency improvement
- **Outphasing:** Two high efficiency switch-mode PAs are driven by constant envelope phase modulated signal and their outputs are combined to obtain amplitude and phase modulation
- Efficiency Enhancement Circuit is used and auxiliary branches are turned OFF for improving back-off efficiency

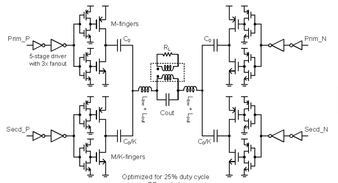
PWM DIGITAL TRANSMITTER AND PA

- Transmitter architecture is based on cascaded sigma-delta modulator and pulse width modulation (PWM) with switched-capacitor power amplifier
- Up-sampled baseband I/Q signals are noise shaped using ΣΔ and time windows (quantized) are created using digital PWM. PWM windows are multiplied by RF carrier which then drive switched-cap PAs. I and Q data are time interleaved.
- Cascaded ΣΔ increases resolution and reduces out of band noise
- Large output amplitude => wide PWM window, more RF pulses. Small amplitude => narrow PWM window, less RF pulses. Back-off efficiency improves.

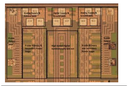


PWM Transmitter

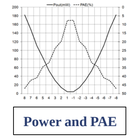
- Each ΣΔ produces $M=16$ level digital output at F_s rate
- Scaling factor K=8 => effectively 128 level resolution at RF output
- High efficiency class-D PAs are used in switched-capacitor output stage
- Digital PWM runs at $F_{clk} = 16*F_s = 4*F_c$
- Matching network transforms 50 ohm load to a much smaller impedance
- On resistance of class-D should be much smaller than transformed load



Class-D switched-capacitor PA

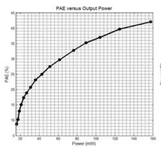


Chip photograph

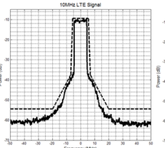


Power and PAE

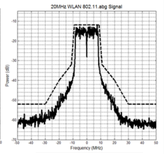
- Test chip is designed in 45nm CMOS process
- 23 dBm peak output power with 47% peak PAE at 2.4GHz
- 23% average PAE for modulated LTE signal with 8.2dB PAPR



Back-off efficiency



Spectrum with 10MHz LTE

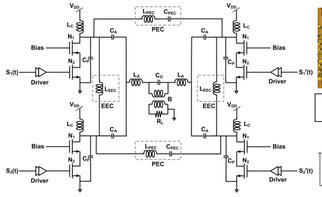


Spectrum with 20MHz WLAN

OUTPHASING POWER AMPLIFIER

- Challenges in outphasing: quarter wavelength transmission line combiner bulky in nature and efficiency reduction at low output power

Class-E outphasing PA:



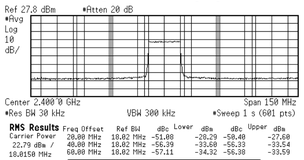
Class-E Outphasing PA

Test chip

PCB

Measurement setup

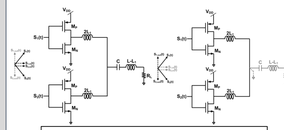
- Cascode class-E outphasing PA with non-isolated LC combiner with *Power Enhancement Circuit (PEC)* and *Efficiency Enhancement Circuit (EEC)*
- EEC does not affect in-phase components but reduces out-of-phase current by creating parallel resonance with C_p and C_A => improves back-off efficiency
- PEC is tuned to 3rd harmonic of carrier and reduces peak drain voltage => supply is increased to get increased output power without violating reliability limits



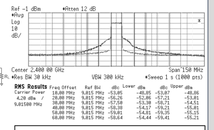
Spectrum with 20MHz LTE

- Test chip designed in 45nm CMOS for 2.4GHz carrier frequency
- 29.5 dBm peak output power with 46.76% drain efficiency
- ACPR - 10MHz and 20MHz LTE: -50dBc and 2-carrier 20MHz LTE: -44dBc

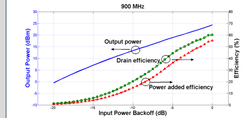
Class-D outphasing PA:

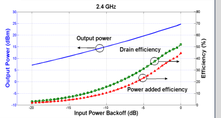


In-phase & out-of-phase operation



Spectrum with 10MHz LTE



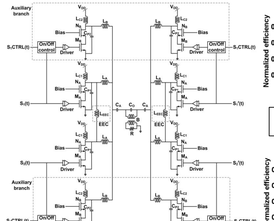


Power, DE and PAE

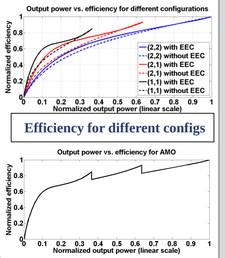
- 900 MHz implementation: 24.4 dBm peak power with 55% PAE, 2.4 GHz implementation: 24.9 dBm peak power with 45% PAE
- Class-E outphasing PA achieves higher output power than class-D as high voltage I/O NMOS (cascode) allows higher RF stress at the drain.

MULTI-MODE OUTPHASING PA

- Auxiliary PA branches are added in S_1 side and S_2 side and they can be turned ON or OFF by CTRL signals and 'On/Off control' blocks
- Auxiliary branch turned off => no power consumption in that PA and drivers => efficiency improves at lower power levels



Multi-mode class-E outphasing PA



Efficiency for different configs

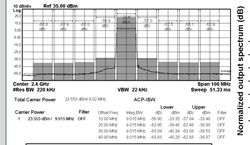
AMO Efficiency

- PA config: *(m,n)* => *m* branches in S_1 side and *n* branches in S_2 side are 'ON'
- Modes of operation: (i) Single level outphasing (ii) Symmetric multilevel outphasing (SMO) and Asymmetric multilevel outphasing (AMO)
- Benefits of proposed AMO: (i) single supply rail, (ii) no efficiency reduction due to supply switching, (iii) avoids nonlinearity, (iv) higher peak power

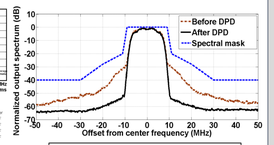
Test chip

PCB

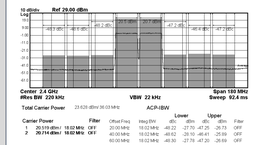
Power levels		Peak power	3 dB back-off	6 dB back-off	9 dB back-off
SLO (high power)	η_d	49.2%	34.8%	25.3%	14.1%
	η_s	43.7%	29.6%	20.1%	11.0%
AMO	η_d	49.2%	39.1%	32.9%	25.2%
	η_s	43.7%	33.9%	27.9%	19.8%



Spectrum with 10 MHz LTE



Spectrum with 20 MHz WLAN



Spectrum with 2-carrier 20 MHz LTE

- Test chip in 45nm CMOS for 2.4GHz carrier
- 31.6 dBm peak power with 49.2% drain efficiency and 43.7% system efficiency
- ACPR – 10MHz LTE: -57dBc (SLO) and -42dBc (AMO), 20MHz LTE: -53 dBc (SLO) and 2 carrier 20MHz LTE: -47dBc (SLO) after DPD

COMPARISON TABLE

PA	Peak output Power	Eff @ Peak power	Eff @ 6-dB back-off	Freq.	Power supply	Process
[1]	26.3 dBm	33% (PAE)	25.1% (PAE)	2.4 GHz	2 volts	90 nm
[2]	26.7 dBm	40.2 % (DE)	37% (DE)	3.71 GHz	-	65 nm
[3]	30.1 dBm	36% (DE)	19% (DE)	2.4 GHz	3.3 volts	90 nm
[4]	28.1 dBm	19.7% (Total)	8% (Total)	2.25 GHz	2.4 volts	45 nm
PWM PA [5]	**23 dBm**	**47% (PAE)**	**29% (PAE)**	**2.4 GHz**	**1.7 volts**	**45 nm**
Class-E Outphasing [6]	**29.5 dBm**	**46.76% (DE)**	**21.16% (DE)**	**2.4 GHz**	**2.4 volts**	**45 nm**
Class-D Outphasing [7]	**24.9 dBm**	**52% (DE)**	**28% (DE)**	**2.4 GHz**	**1.7 volts**	**45 nm**
Multi-mode Outphasing [8]	**31.6 dBm**	**49.2 % (DE)**	**25.3%, 32.9% (DE)**	**2.4 GHz**	**2.4 volts**	**45 nm**

CONCLUSION

- Recent innovations at Texas Instruments in CMOS based transmitter and power amplifier architectures targeting back-off efficiency improvement are reviewed
- Digital PWM transmitter, outphasing power amplifier and multi-mode outphasing PA techniques are presented

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