390-640MHz Tunable Oscillator Based on Phase Interpolation with -120dBc/Hz In-Band Noise

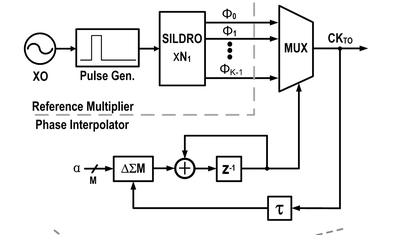
Xu Meng[1, 2], Lianhong Zhou[1], Fujiang Lin[2], Chun-Huat Heng[1]

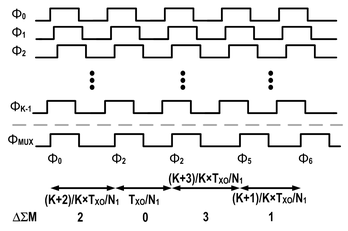
[1] ECE, National University of Singapore [2] DEST, University of Science and Technology of China

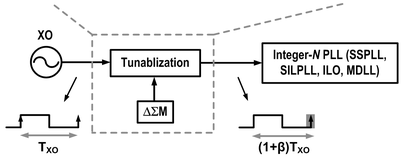
Abstract

This presentation proposes a high frequency tunable oscillator (TO). It first employs sub-harmonic injection-locked digitally controlled ring oscillator (SILDRO) to obtain low phase noise high frequency fixed reference. Delta-sigma modulator (ΔΣM) is then applied to obtain phase interpolation between the multi-phase outputs of the SILDRO to achieve fine frequency tuning. This method enables the creation of low phase noise tunable high frequency reference. Cascade the designed TO with subsequent integer-*N* PLL can form a high performance fractional-*N* synthesizer.

System Architecture

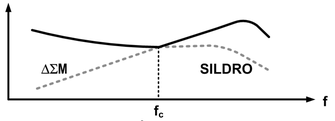






$$f_{TO} = \frac{1}{T_{TO}} = \frac{N_1}{1+\alpha/(K\times 2^M)} f_{XO}$$

$$\Delta f_{LSB} = \frac{N_1}{K\times 2^M} f_{XO}$$

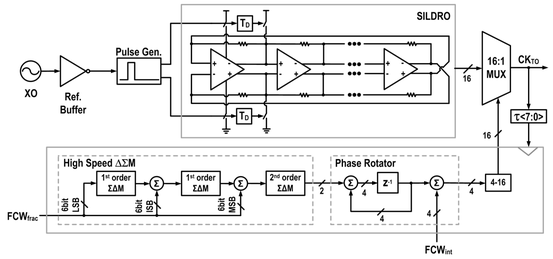


$$Q_{noise}(f) = \frac{\Delta_\phi^2}{12 f_{\Delta\Sigma M}} [2\sin\left(\frac{\pi f}{f_{\Delta\Sigma M}}\right)]^{2n-2}$$

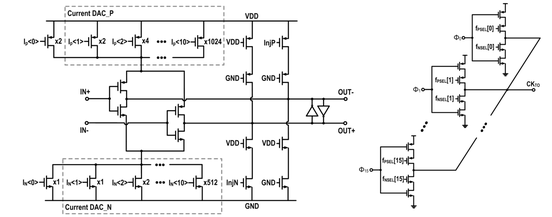
$$\Delta_\phi = \frac{\Delta_t}{T_{\Delta\Sigma M}} \times 2\pi = \frac{T_{XO}/(N_1\times K)}{T_{\Delta\Sigma M}} \times 2\pi = \frac{2\pi}{K+\alpha/2^M}$$

- Phase interpolation to achieve frequency tuning ability
- Sub-harmonic injection locking provides low in-band noise
- High frequency ΔΣM generates low quantization noise

Circuit Implementation

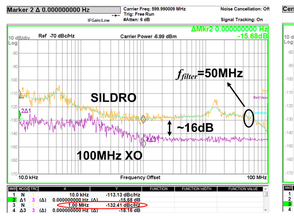


- Fully phase re-alignment achieved in SILDRO
- 1st order noise shaping with 2nd order ΔΣM
- Phase rotator provides inherent dynamic element matching
- Additional delay to prove correct interpolation

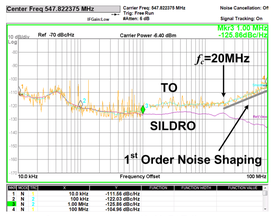


- Digitally controlled ring oscillator
- Mismatch filter resistor applied
- Tri-state inverter based multiplexer

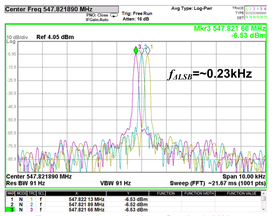
Measurement Results



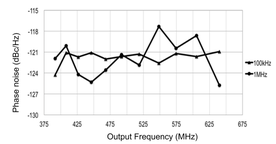
Phase noise of XO and SILDRO



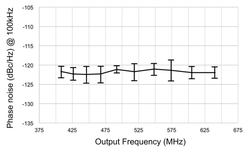
Phase noise of TO @ 547.8 MHz



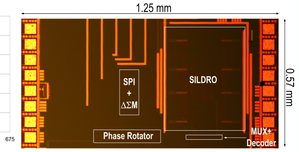
Frequency resolution @ 547.8 MHz



Phase noise Versus Output frequency @ different offsets



Phase noise @ 100kHz Versus Output frequency for 7 chips



Die Photo

Benchmarking

	D. Jee JSSC Nov. 2013	Blank ESSCIRC 2012	P. Park ISSCC 2012	This work
Technology (nm)	130	180	65	65
Architecture	Fractional-N	Fractional-N	Fractional ILO	Phase Interpolation
Reference Frequency (MHz)	32	32~40	32	100
Output Frequency Range (GHz)	0.86~1.26	0.133~0.96	0.58	0.39~0.64
Frequency Resolution	~0.12kHz	30Hz	1MHz	~0.2kHz
Oscillator Type	Ring	LC	Ring	Ring
In-band Phase Noise (dBc/Hz)	<-100	-100	-100	<-120
Area (mm^2)	0.31	2.08	0.1575	0.257
Power (mW)	16.8	15	10.5	6.3
FOM_1 (dB)	147.8	169	159.1	172.6
FOM_2 (dB)	-220.70	-226	-217.3	-234.2+

+Integrate till 1MHz assuming phase noise suppression beyond 1MHz by subsequent PLL

$$FOM_1 = 10\log_{10}\left[\left(\frac{f_{osc}}{\Delta f}\right)^2 \left(\frac{1mW}{Power}\right)\right] - \text{Phase Noise(dBc/Hz)} \quad FOM_2 = 10\log_{10}\left[\left(\frac{Jitter}{1s}\right)^2 \left(\frac{Power}{1mW}\right)\right]$$

Acknowledgement

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References

[1] S.-J. Cheng, Y. Gao, W.-D. Toh, Y. Zheng, M. Je, and C.-H. Heng, "A 110pJ/b multichannel FSK/GMSK/QPSK/p/4-DQPSK transmitter with phase-interpolated dual-injection DLL-based synthesizer employing hybrid FIR," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2013, pp. 450–451.

[2] D. Park and S. Cho, "A 14.2mW 2.55-to-3GHz cascaded PLL with reference injection, 800MHz delta-sigma modulator and 255frms integrated jitter in 0.13um CMOS," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2012, pp. 344–345.

Contact: mengxu@mail.ustc.edu.cn