

# A Seizure-detection IC Employing Machine Learning to Overcome Data-conversion and Analog-processing Non-idealities

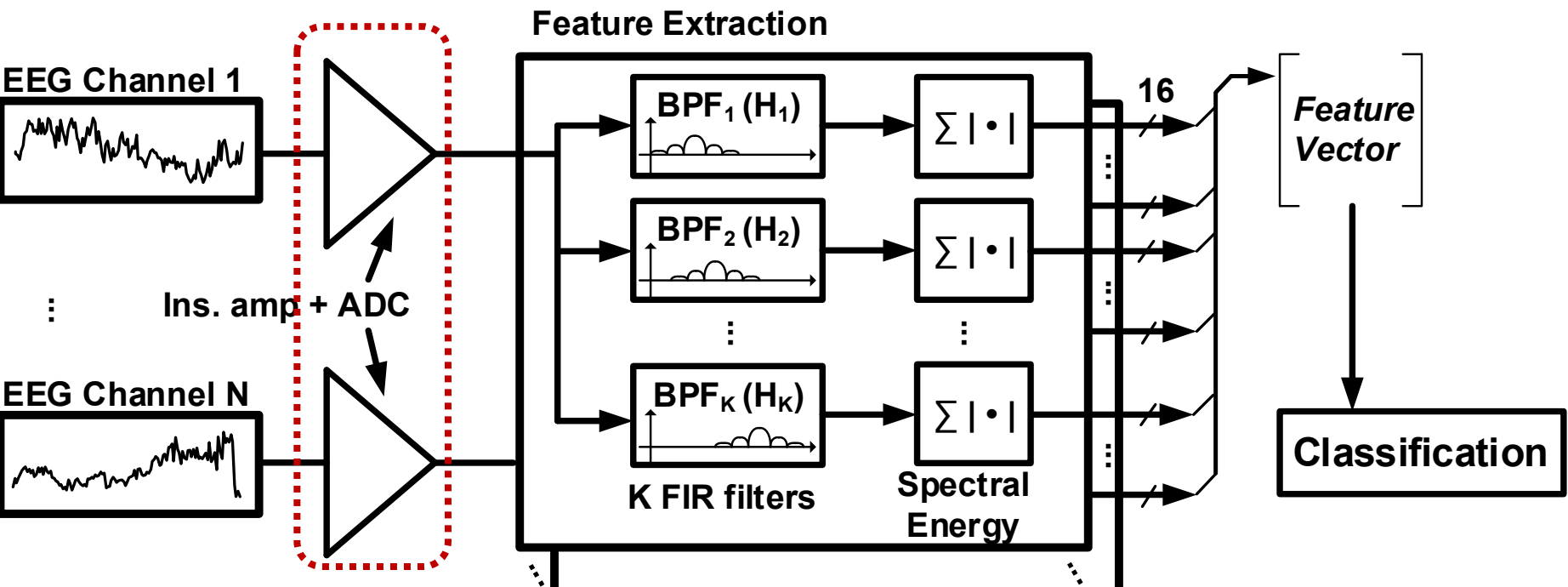
J. Zhang, L. Huang, Z. Wang and N. Verma, Princeton University



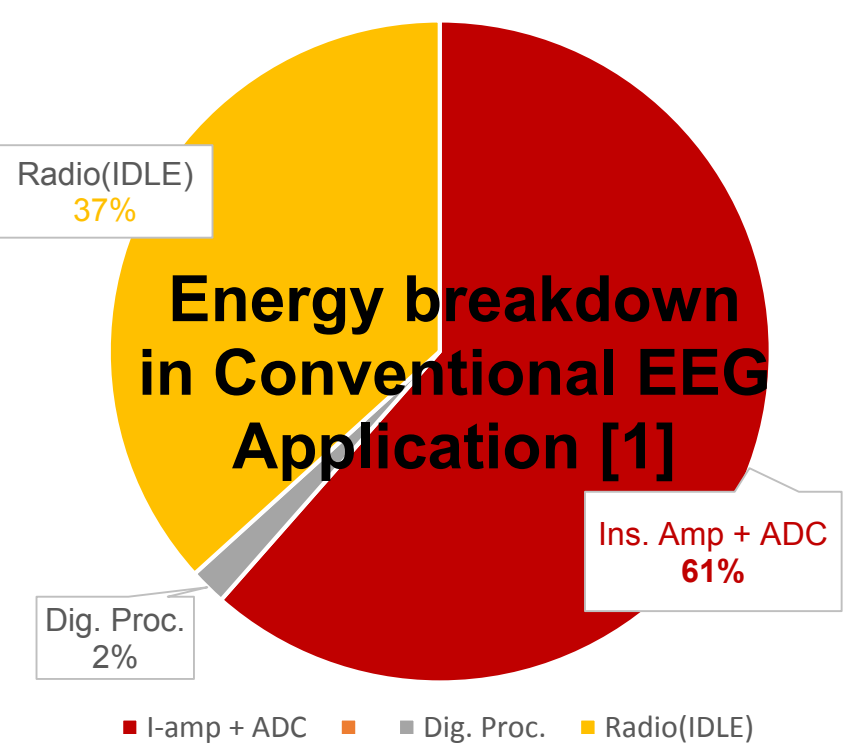
PRINCETON  
UNIVERSITY



## CONVENTIONAL SEIZURE –DETECTOR [1]

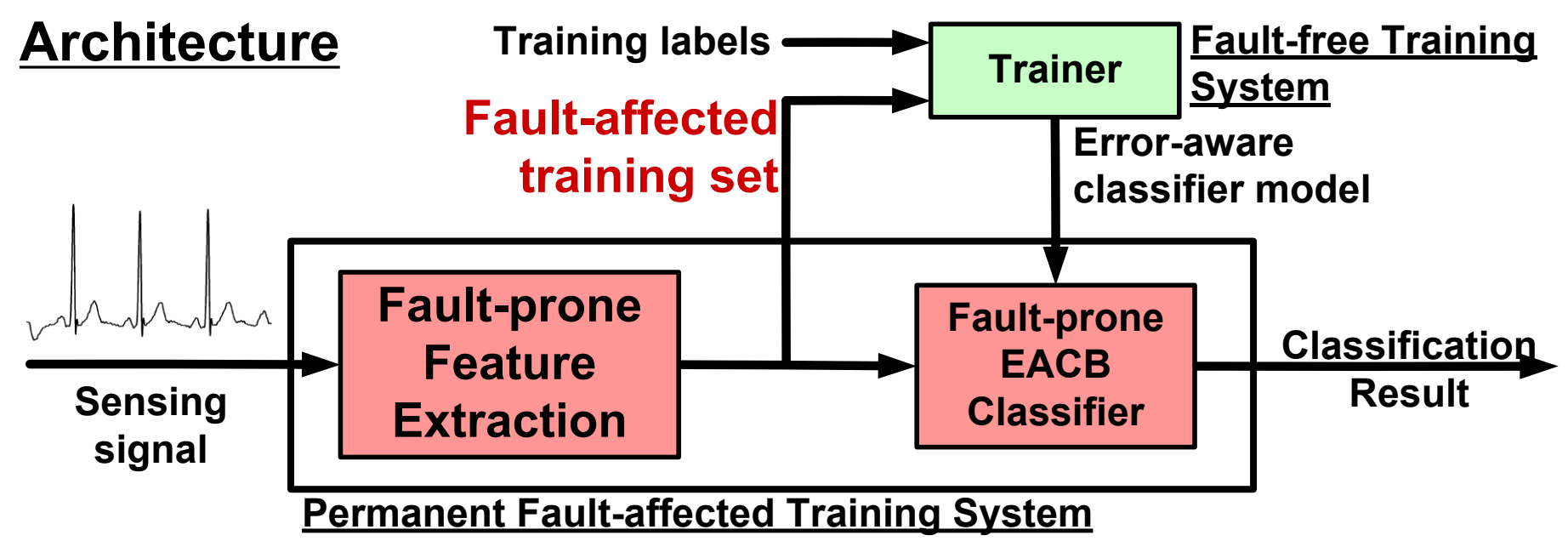


In Seizure detection, and other biomedical applications, high quality signal analysis first requires sensor outputs to be acquired with high accuracy. Given the low amplitude of signals, high impedance of electrodes, and prominence of artifacts (stray coupling, electrode interfacing/movement), the analog front end (instrumentations amplifiers and ADCs) often dominate energy.

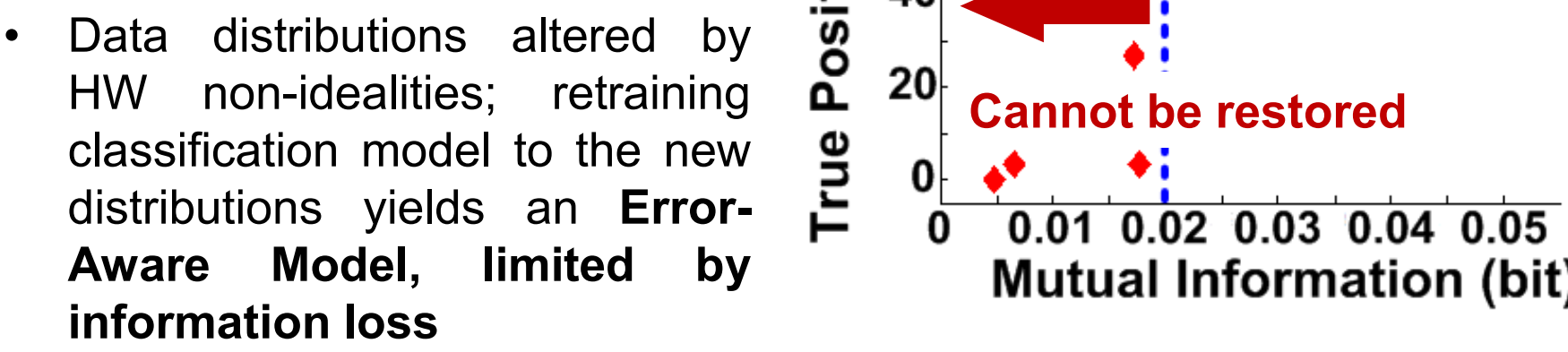
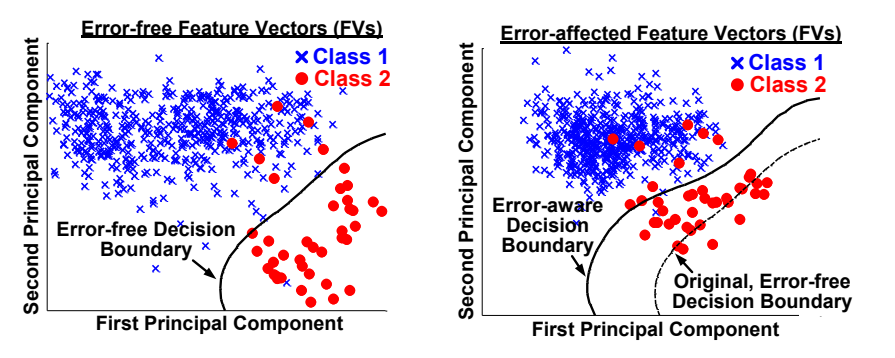


Use machine-learning algorithms to relax analog front-end

## Data-Driven Hardware Resilience (DDHR) [2]

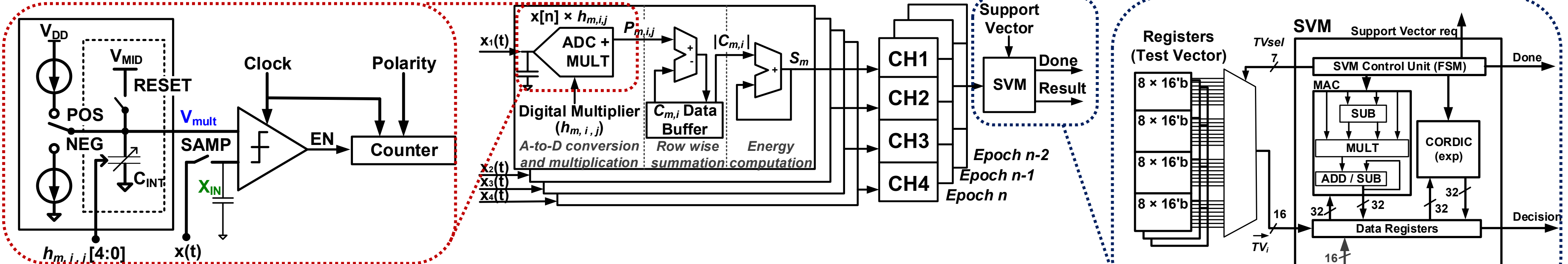


## Error-aware Modelling

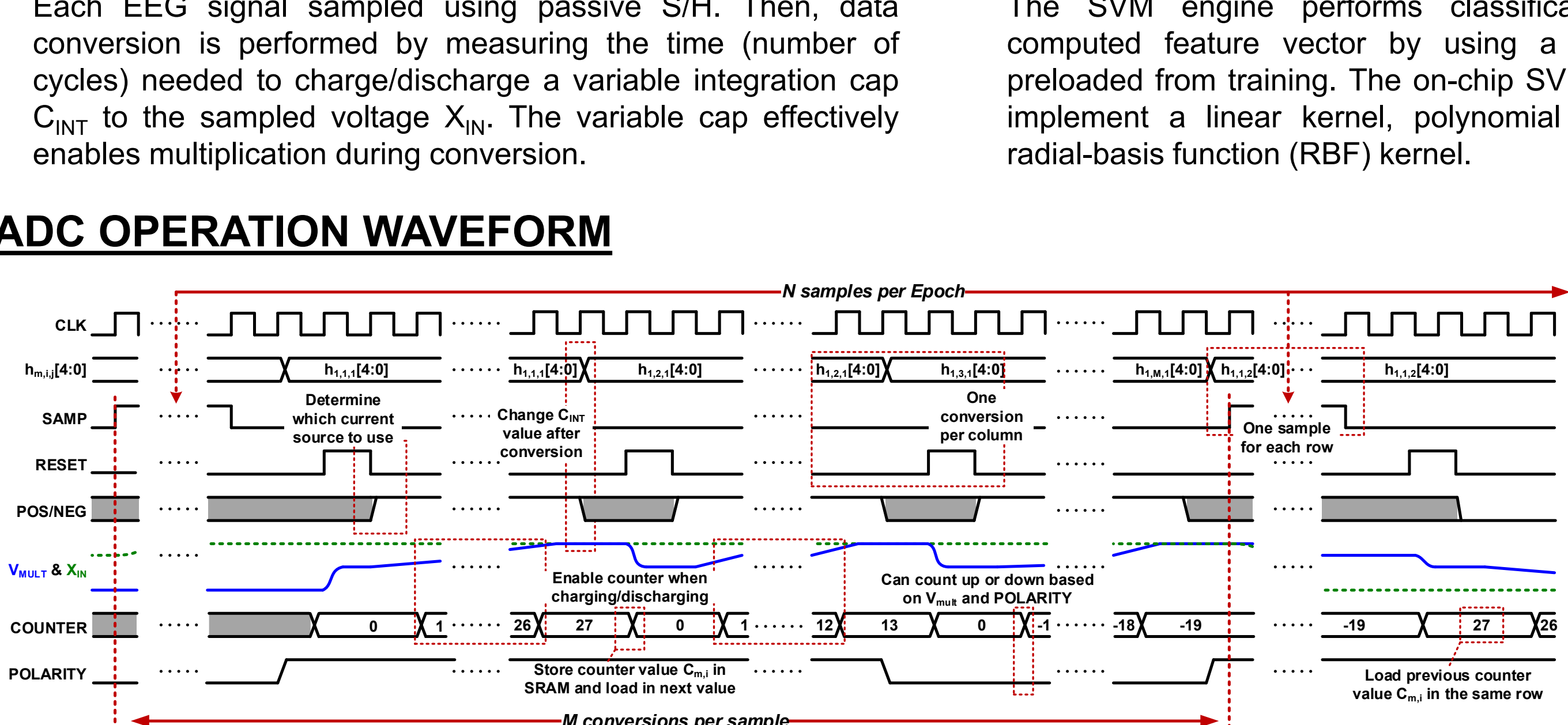


[1] N. Verma, A. Shoenb, J. Bohorquez, J. Dawson, J. Guttg, and A. P. Chandrakasan, "A micropower EEG acquisition SoC with integrated feature extraction processor for a chronic seizure detection system," IEEE J. Solid-State Circuits, vol. 45, no. 4, pp. 804–816, Apr. 2010.  
[2] Z. Wang, K. H. Lee, and N. Verma, "Overcoming computational errors in sensing platforms through embedded machine-learning kernels," IEEE Trans. VLSI Syst., DOI: 10.1109/TVLSI.2014.2342153.

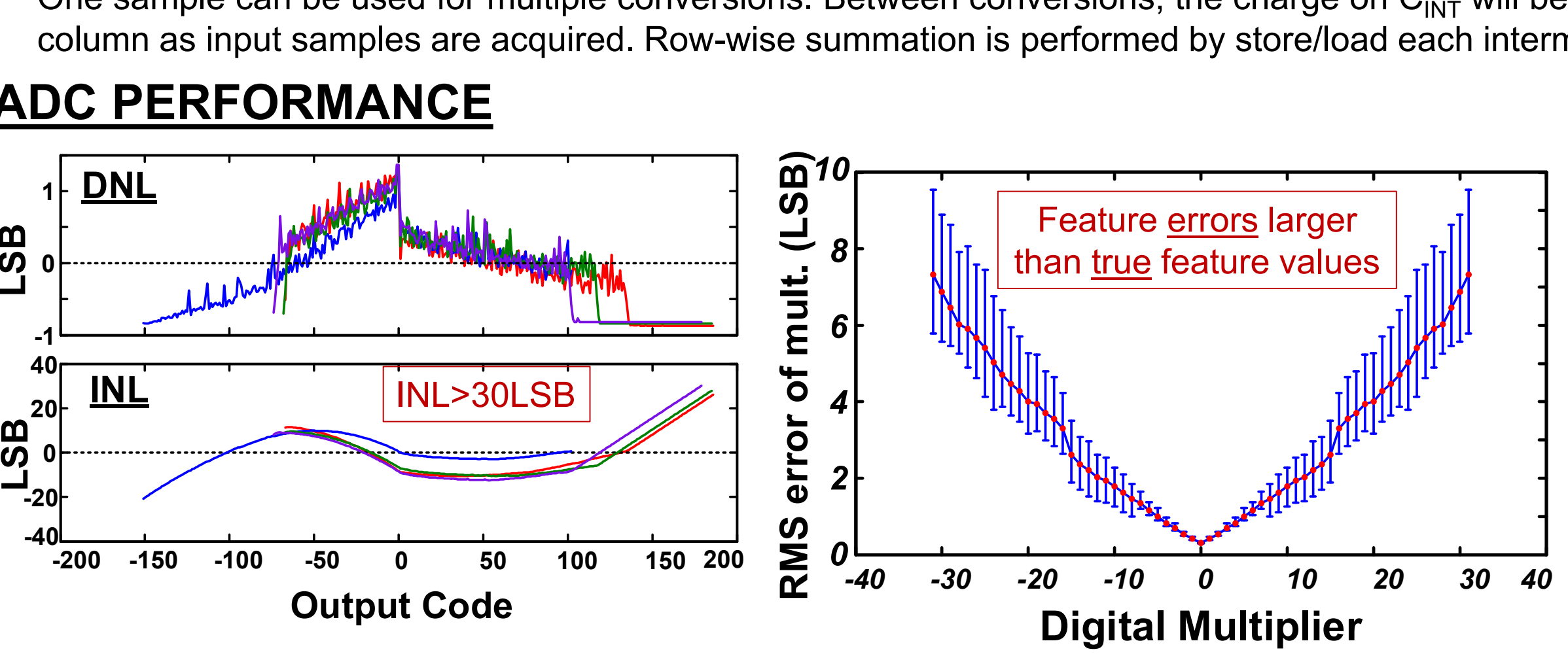
## SYSTEM PROTOTYPE



## ADC OPERATION WAVEFORM



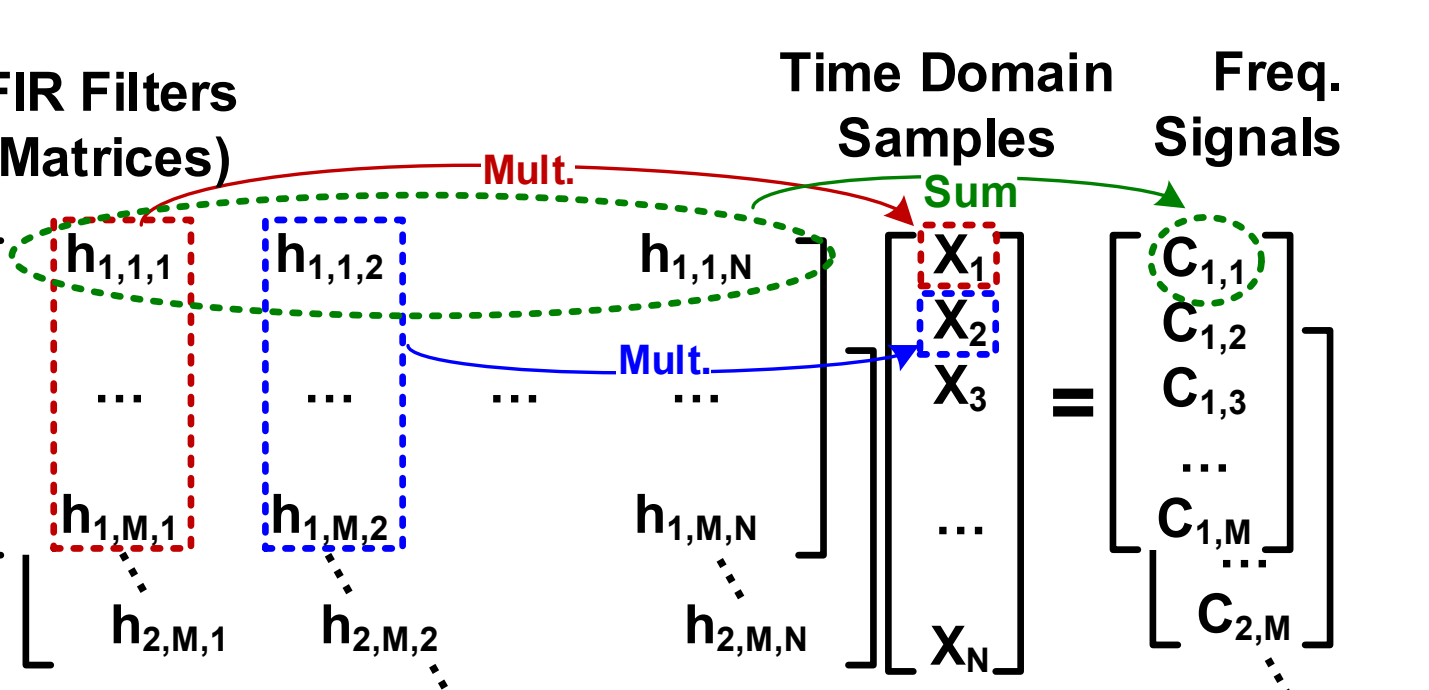
## ADC PERFORMANCE



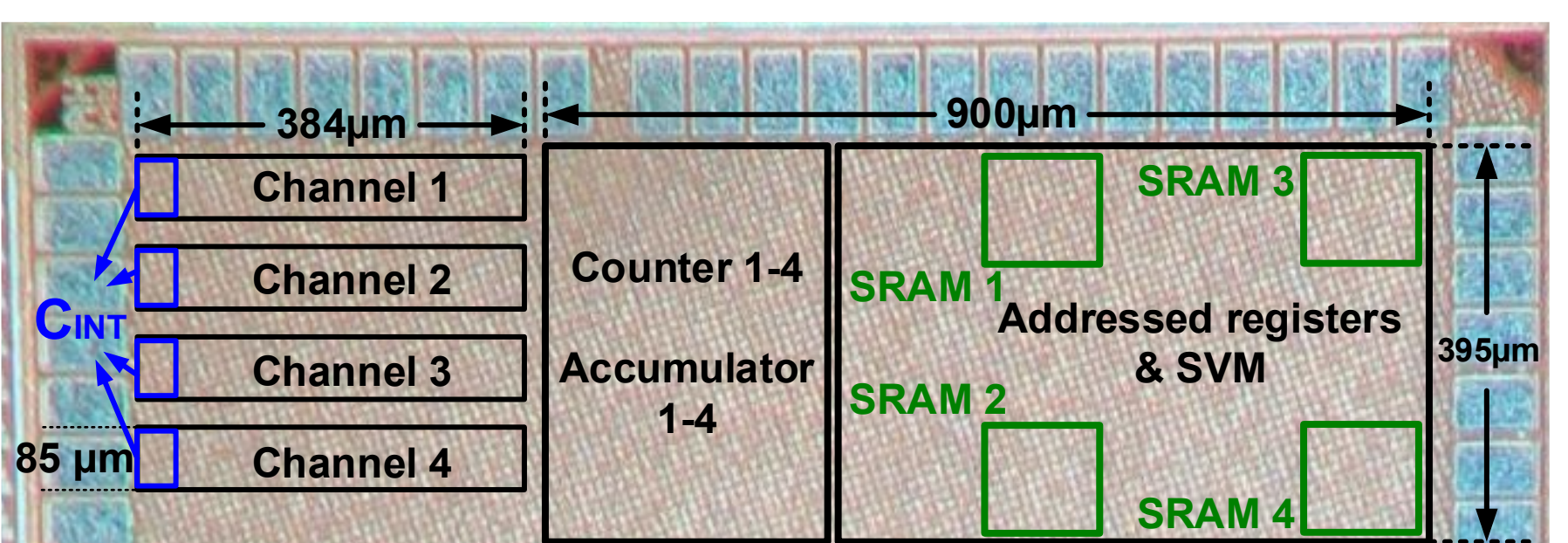
• **Severe Non-linearity**  
Such implementation of ADC in 32nm technology suffers from severe nonlinearity. DNL is 1.5 LSB and INL is >30 LSB at 8-b level

• **High RMS Error**  
The nonlinearity leads to large RMS error of the features; when normalized to the ideal feature values, the RMS error is measured to be 1.16, indicating errors larger than the feature values themselves.

## MATRIX MULTIPLICATION



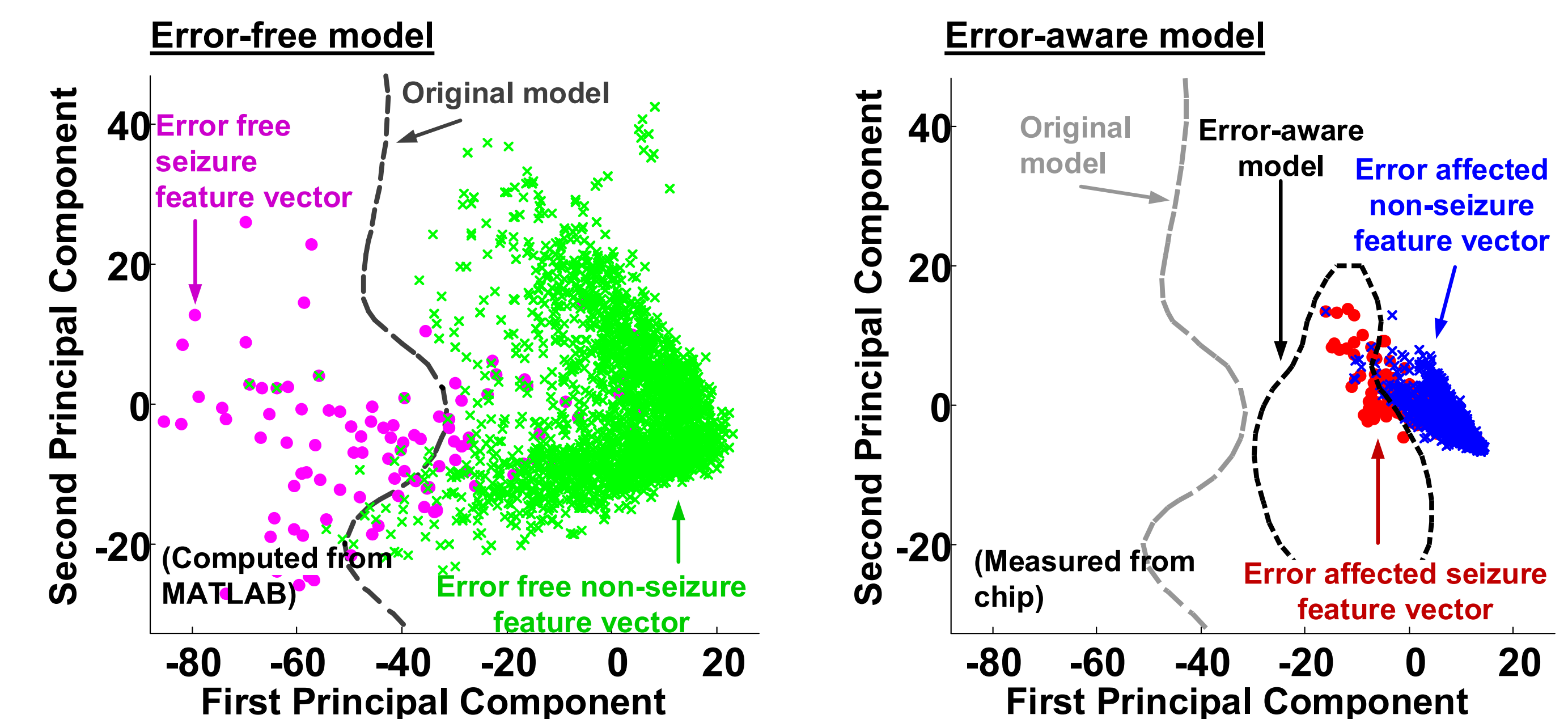
## DIE PHOTO



## CHIP SUMMARY

Technology	32nm CMOS SOI	Sample Rate	Up to 5kHz (typ. 64Hz)
Supply Voltage	Analog: 0.9 V Digital: 0.9 V SRAM: 0.9 V	ADC ENOB	2.8-3.6 ( $f_{in} = 100 \text{ Hz}$ ) / 2.1-2.6 ( $f_{in} = 1 \text{ kHz}$ )
ADC Resolution	8 bits	ADC INL/DNL	20.8-30.1/1.2-1.4 (LSB)
Input Range	200 mV - 700 mV	Energy / Feature Vector	12.04 uJ / Feature Vector
		Energy / class.	1.35 uJ / class.

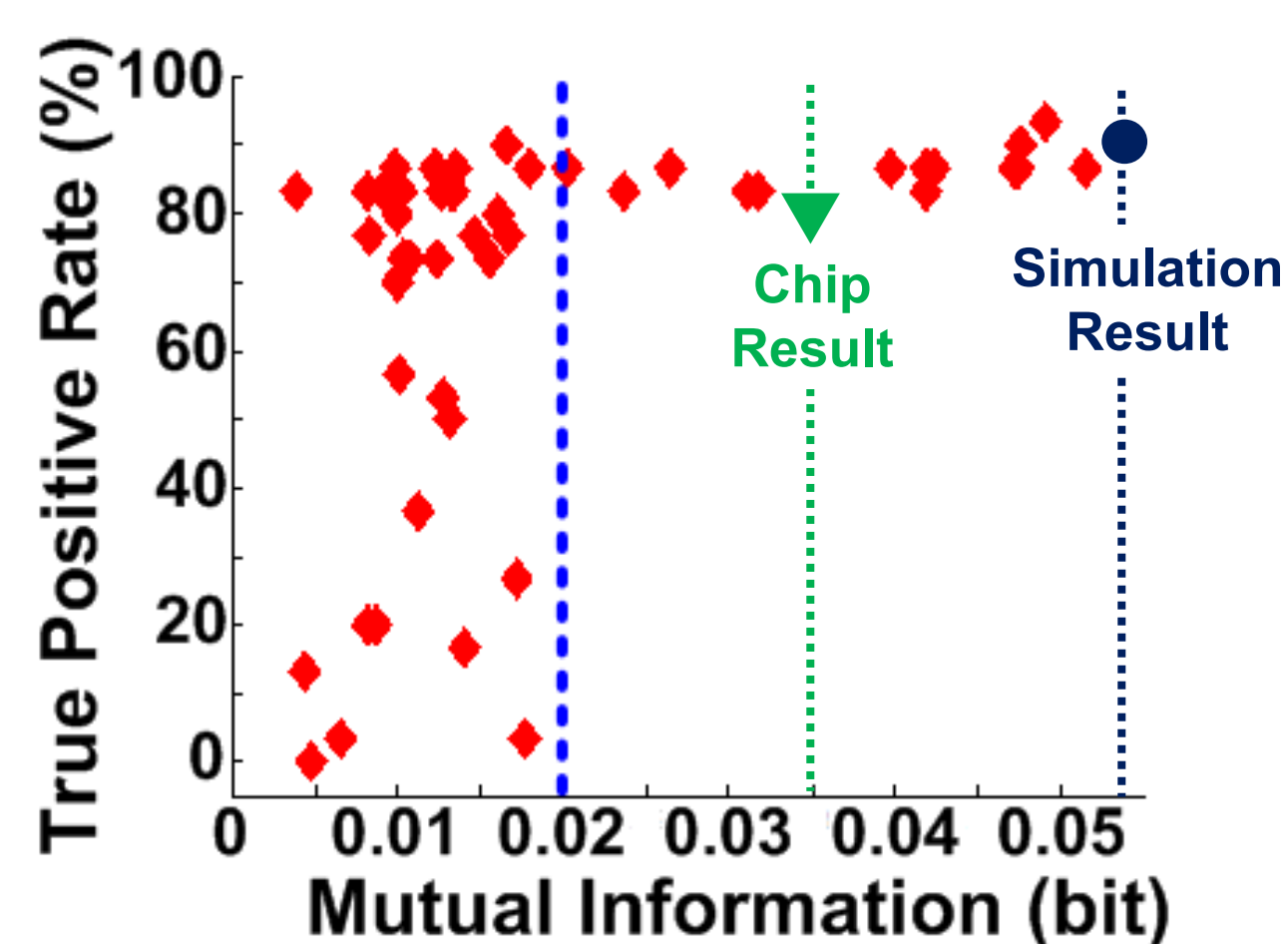
## CHIP RESULT



Performance Summary	Ideal Performance	Chip w/ baseline model	Chip w/ error-aware model
Sensitivity	5/5	5/5	5/5
Latency	2.0 sec.	3.6 sec.	3.4 sec.
Specificity*	8	443	4

• **Restored performance**  
Using baseline model to classify error affected data will cause high false alarm rate. Despite the feature errors, the error-aware model restores the system performance to nearly the ideal level.

## CONCLUSION



• **Mutual Information Preservation**  
The analog frontend downgrade the mutual information from ~0.055 bits to 0.035 bits. However the mutual information still remains in the range where effective classification can be performed.

• **Limitation of error resilience**  
The performance is limited fundamentally by how well the error affected data retains information for distinguishing class membership [2]. Mutual Information (MI), uses Shannon entropy to calculate the difference between the overall uncertainty of a class label and the conditional uncertainty of the label-DDHR systems are shown to be limited by MI.

This project explores the possibility of greatly relaxing the precision requirements of analog frontend circuits by taking advantage of algorithmic capabilities to model how information is represented in the resulting outputs. The performance can be successfully restored in the presence of severe errors.

## ACKNOWLEDGEMENT

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The mutual information calculation is done by J. Alexander Bae.