A Compact, High Linearity 40GS/s Track and Hold Amplifier in 90nm SiGe Technology

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Motivation

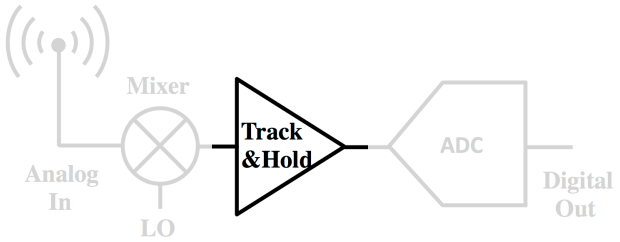
Growing wireless devices

http://www.nydailynews.com/news/world/check-contrasting-pics-st-peter-square-article-1.1288700

mm-wave radios for 5G[2]

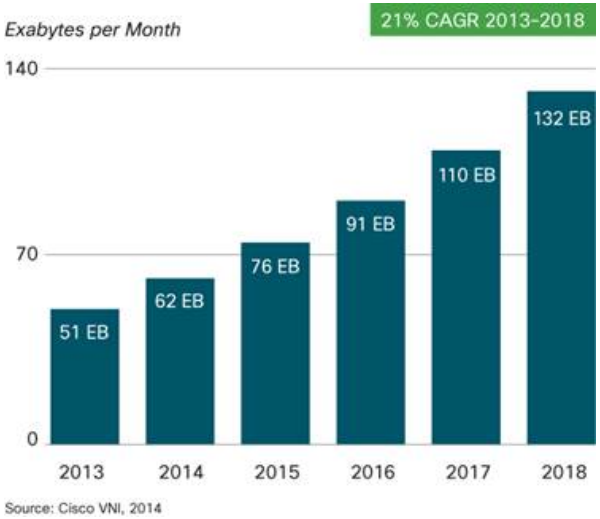
http://pixgood.com/cloud-computing-png.html

High-speed
Digital Receivers



-Low Distortion
-High BW
-Low Power
-High Sensitivity
-High Sampling Speeds

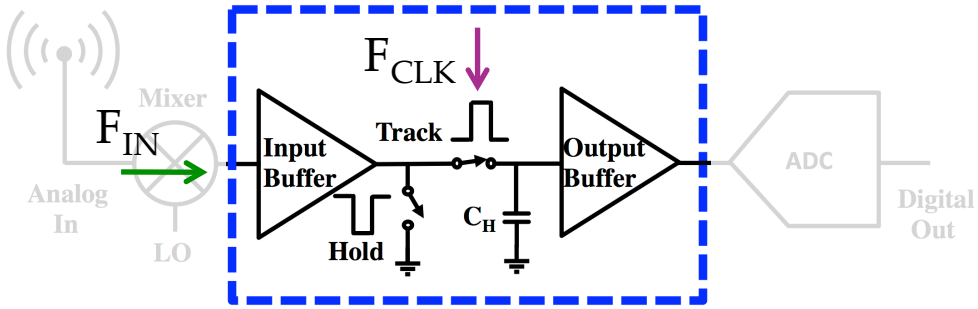
CISCO, "Cisco Visual Networking Index: Mobile Data Traffic Forecast Update, 2013-2018," 2014



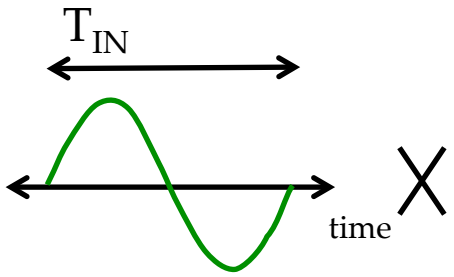
40Gb/s, 100Gb/s
Ethernet standards[1]

http://rdssolutions.com/wp-content/uploads/2012/03/Fiber-Ethernet.jpg

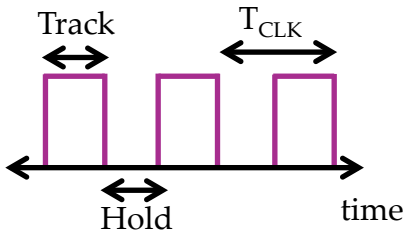
Track/Hold Amplifier (THA) Operation



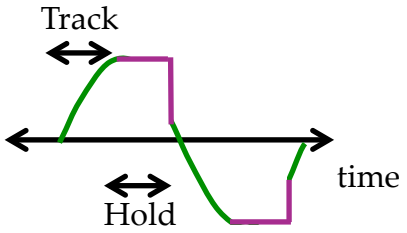
- C_H buffered at input & output
- C_H charged/discharged to track/hold input on alternating clock cycles



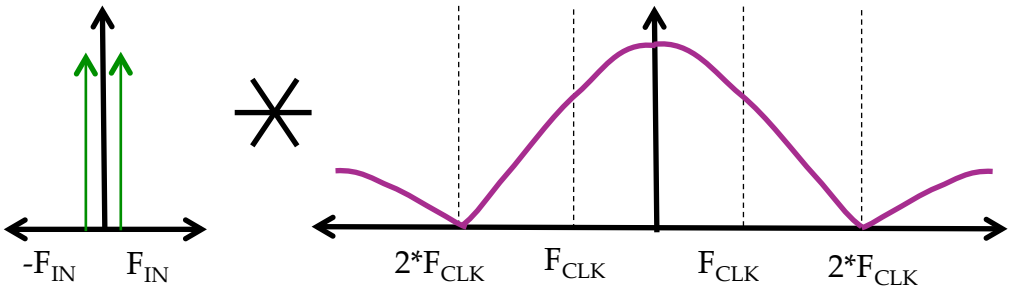
$F_{IN}=1/T_{IN}$

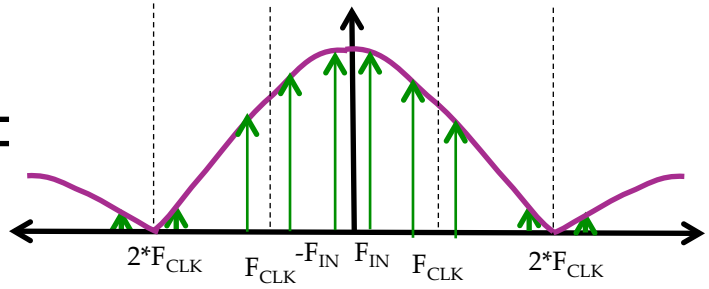


$F_{CLK}=1/T_{CLK}$



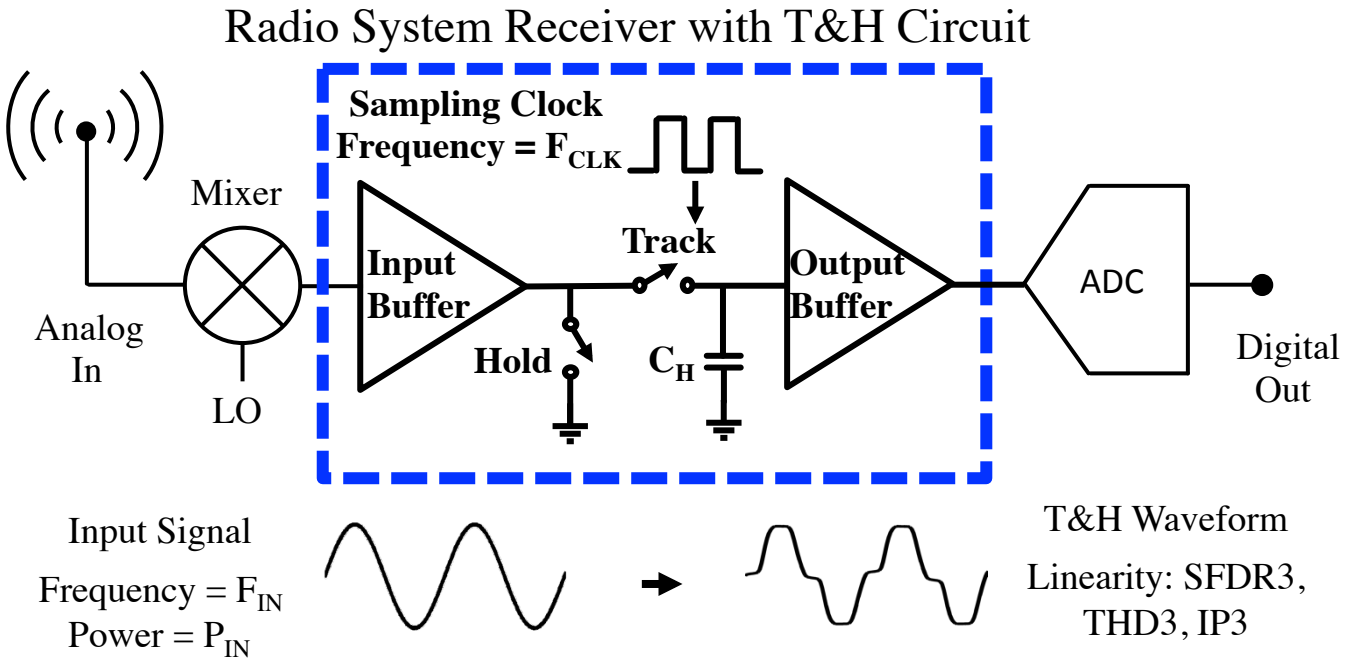
Output Waveform





Application

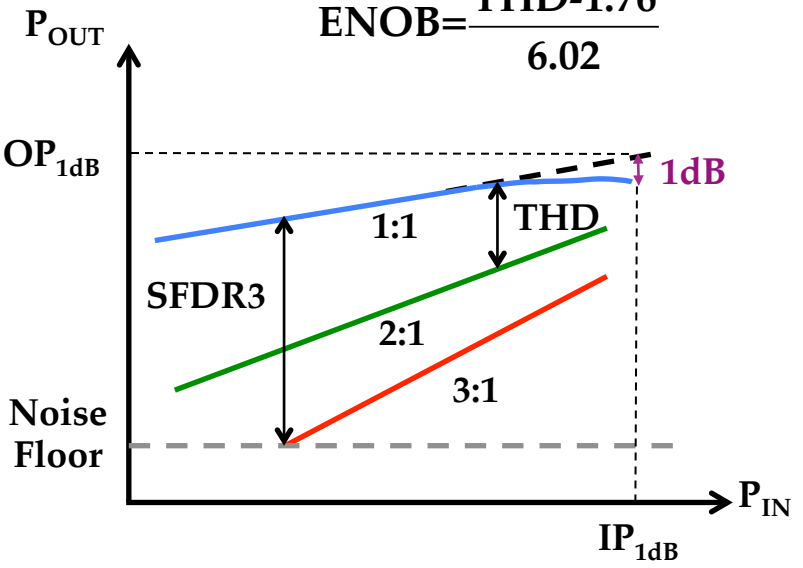
- Communication systems use ADCs for DSP
- ADCs periodically sample, quantize and digitize received signal
- Signal holding capability during sampling provided by Track-and-Hold (THA) circuit

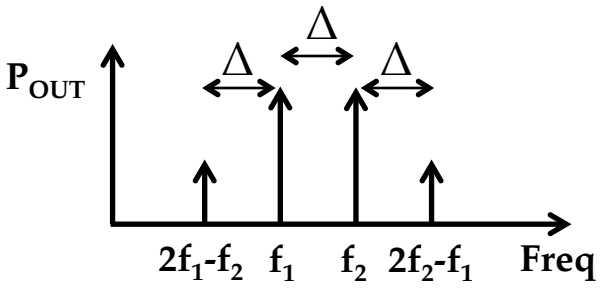


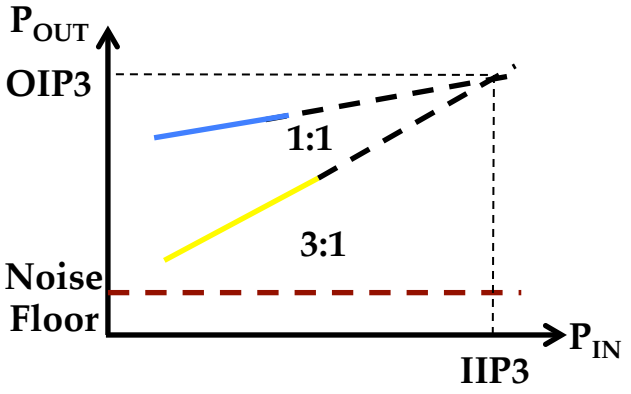
Performance Metrics

- Spurious Free Dynamic Range (SFDR)
  - Dynamic Range between fundamental tone and spur when spur exceeds noise floor
- P_{1dB}: 1-dB compression point
- Total Harmonic Distortion, THD
- Effective Number of Bits, ENOB (Resolution)
- In-Band Intermodulation Products (IP3): Two Tone tests

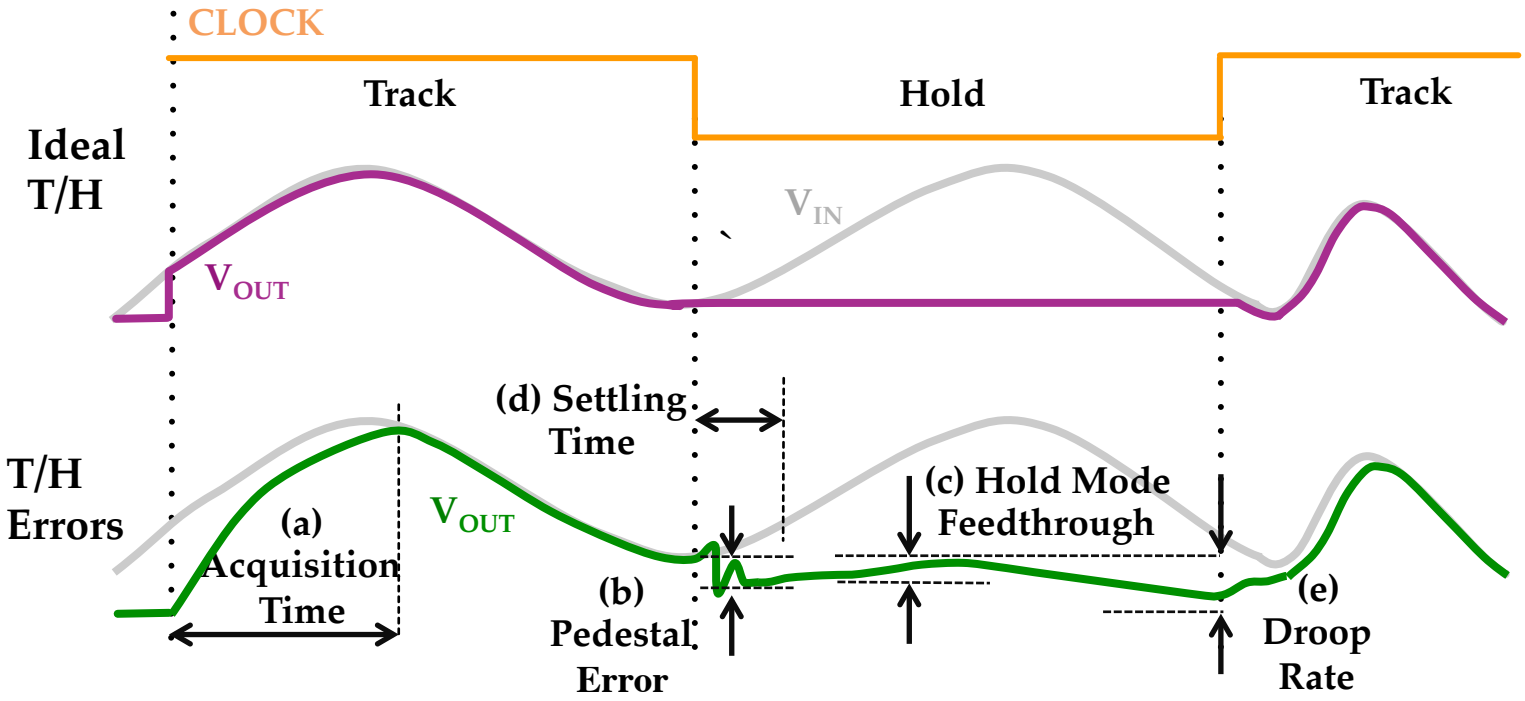
$$ENOB=\frac{THD-1.76}{6.02}$$



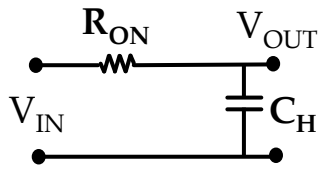




Non-Linearities in THA



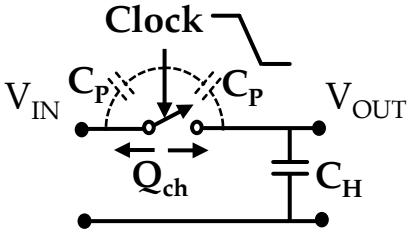
(a) Acquisition Time



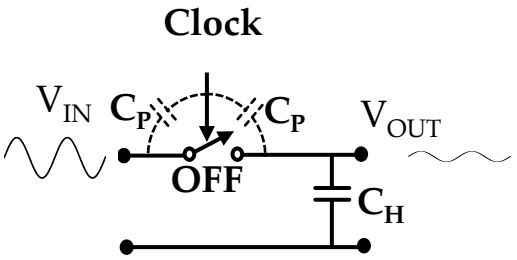
Finite Track BW

$$\tau = \frac{1}{BW} = R_{ON} C_H$$

(b) Pedestal Error

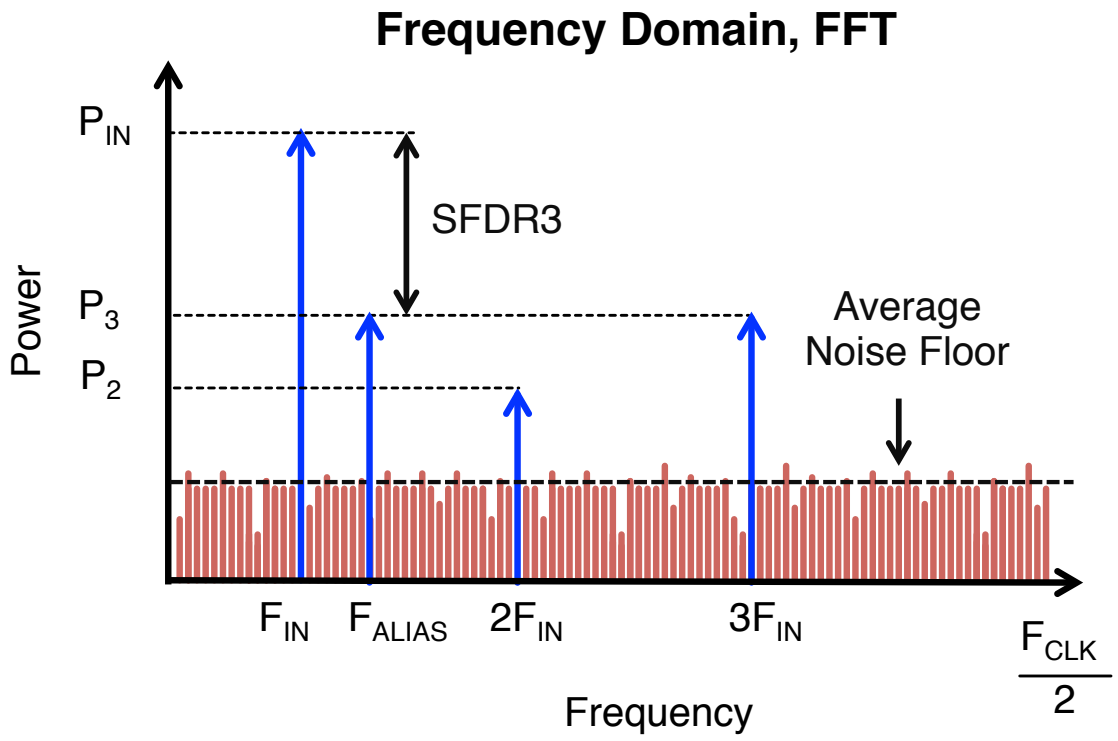


(c) Hold-Mode Feedthrough

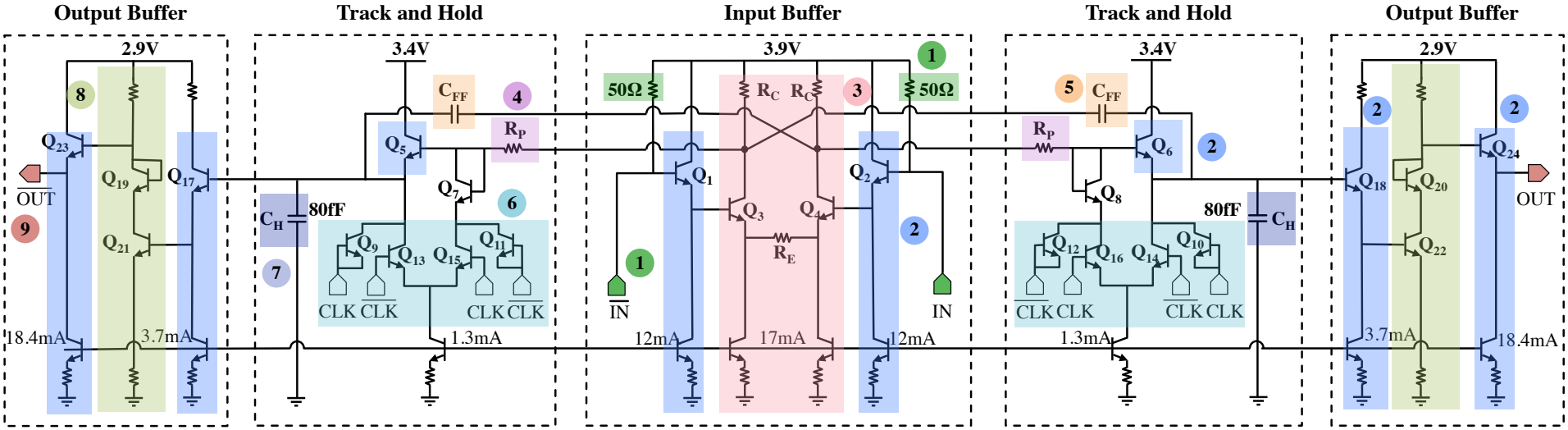


Other Errors:
-Device Mismatch
-Clock swing not fully differential
-Low output resistance of current generators

Non-Linearities in THA

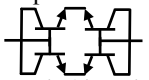


Circuit Design & Architecture

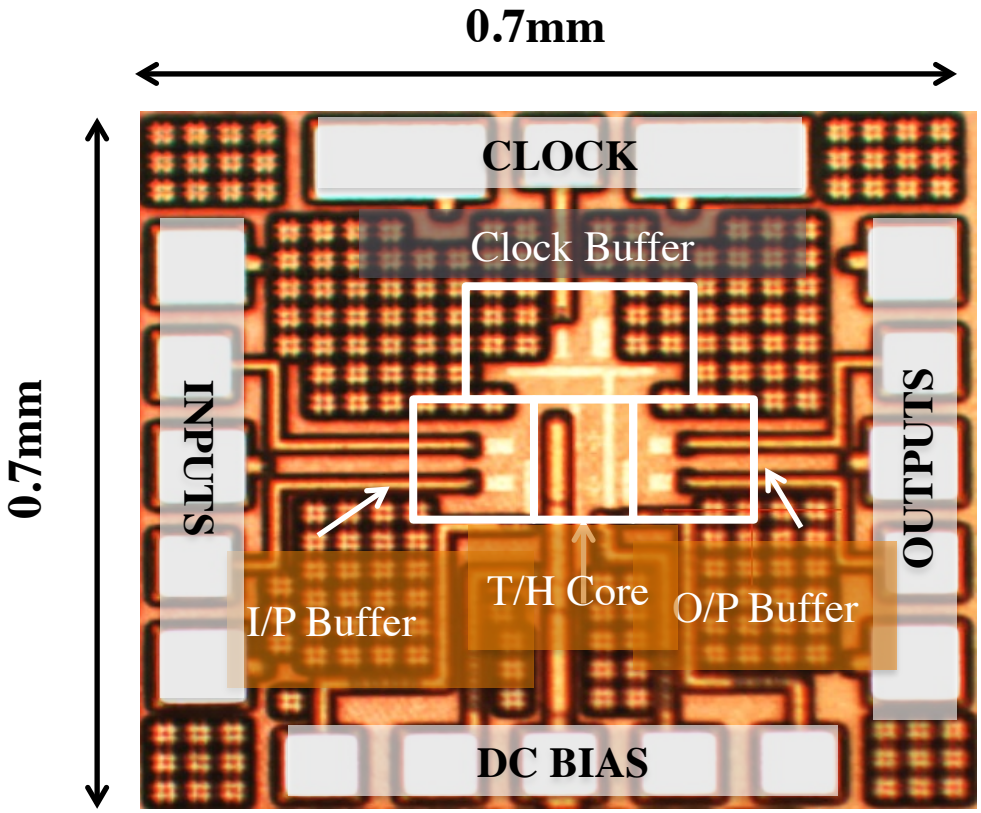


- Differential design minimizes
  - Even order harmonics
  - Common-mode noise
- Current biasing with diode connected devices
- Single ended clock input converted to differential through buffer amplifier
- Peak f_T biasing of switches

1. 50Ω Input matching
2. Emitter Followers used for input/output buffering
3. Differential Pair for high speed current steering, Gain<1 to minimize distortion
4. R_P generates voltage drop to turn off base of Q5, Q6
5. Feedforward Compensation Capacitors

   C_{FF} ⊣⊢ ≡ 
6. Current steering switching circuit. Q9-12 are dummy transistors to counteract charge injection from switching
7. Hold Capacitor
8. Degenerated Common Emitter with Gain<1, lowers output swing
9. High impedance output

Layout and Fabrication



- Design laid out in SiGe HBT 90nm technology
  - f_T=300GHz, f_{MAX}>300GHz

Measurement Setup

Input

Signal Generator
Agilent 83650B (Single Tone)
Agilent PSG 20GHz (Two Tone)

F_{IN} = 1-15GHz,
P_{IN}=-30dBm to 10dBm

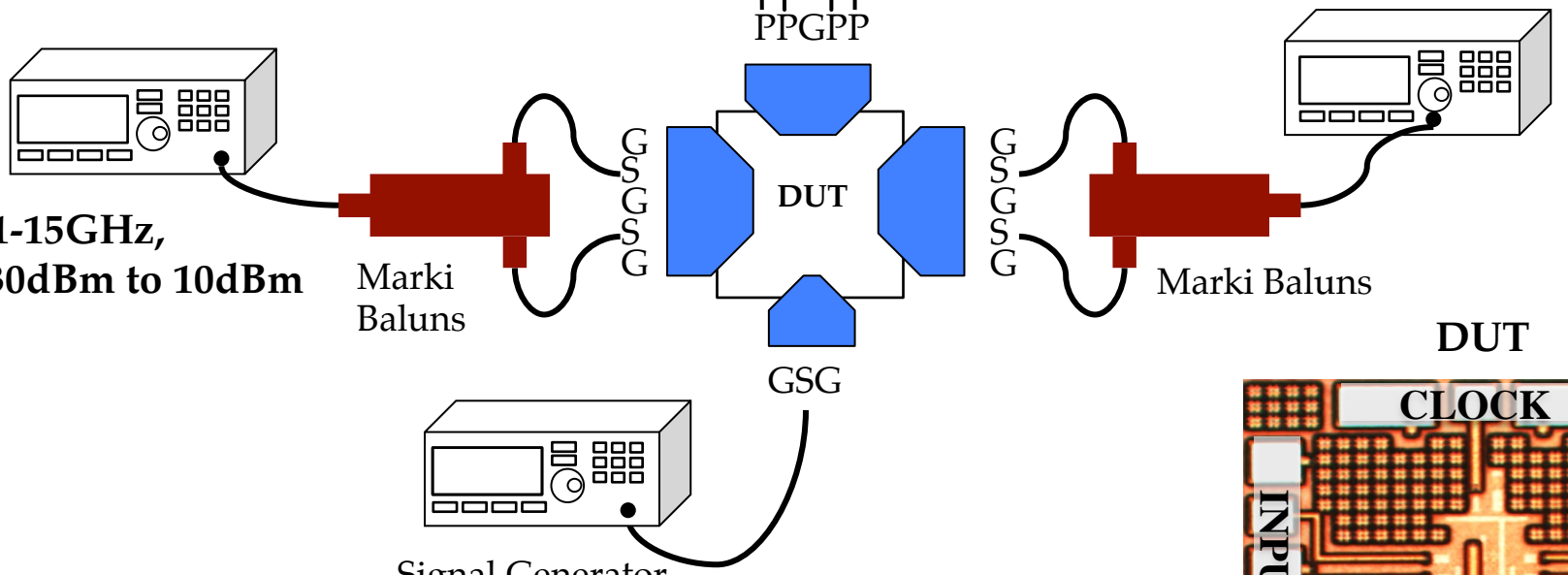
Power Supply

PPGPP

Output

Oscilloscope
R&S RTO 1024

Spectrum Analyzer
R&S FSUP



Marki Baluns

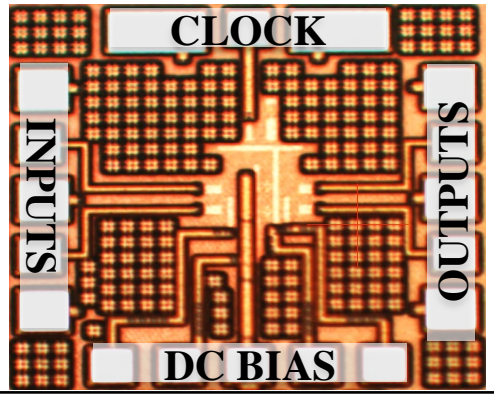
Marki Baluns

Signal Generator
HP E8267C

Clock

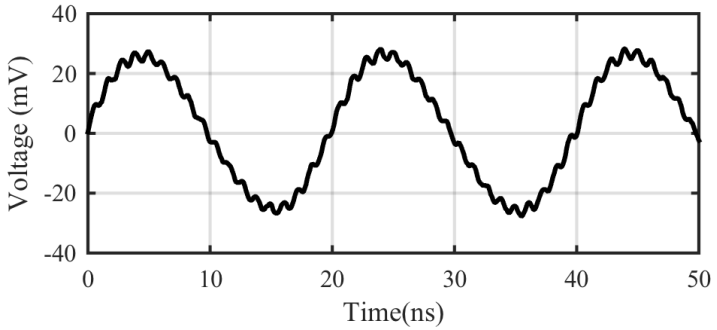
F_{CLK} = 40GHz
P_{CLK}=3dBm

DUT



T/H Operation Achieved

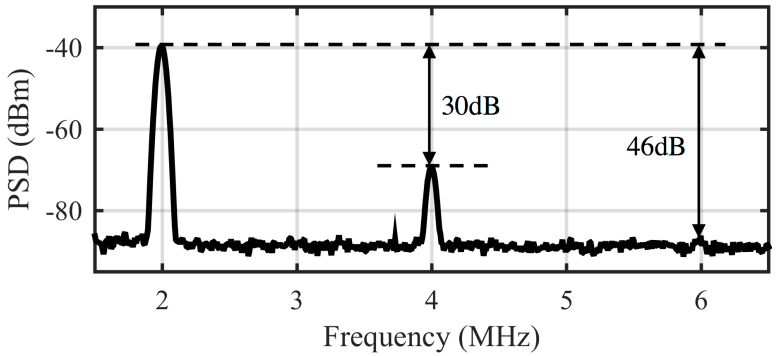
Time Measurement



2GHz Oscilloscope

F_{IN} = 50MHz, P_{IN} = -10dBm
F_{CLK} = 0.9GS/s

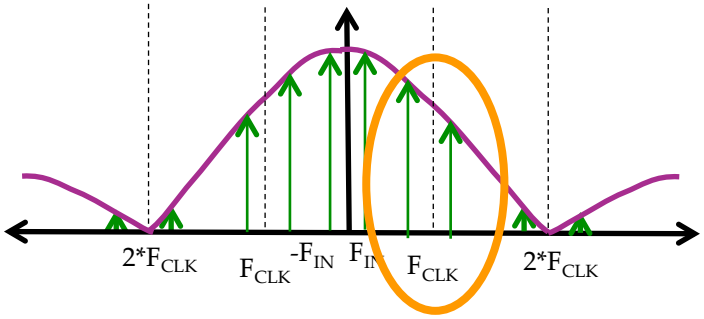
Beat Frequency Test



F_{IN}=40.002GHz
F_{CLK}=40GHz

High frequency operation tested for signal at 2MHz

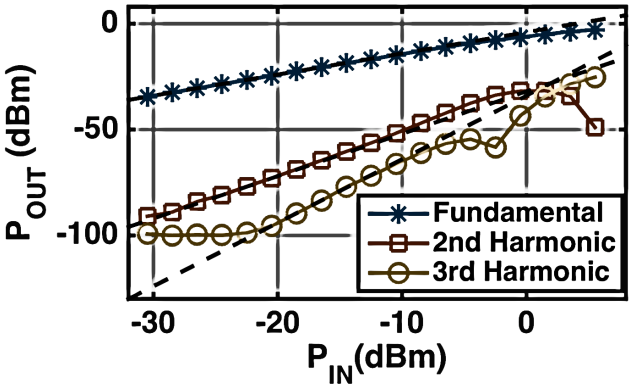
Nyquist Zone Clocking



Presence of Aliased F_{IN} around F_{CLK} confirmed on Spectrum Analyzer

Linearity Results @ 40GS/s

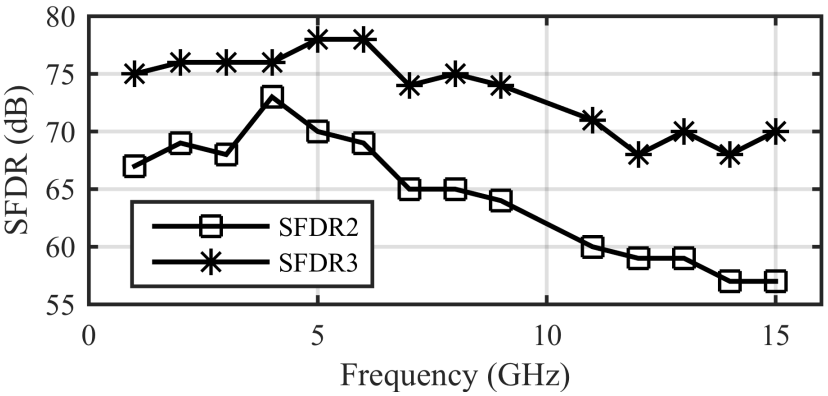
Output Harmonics



F_{IN}=5GHz
F_{CLK}=40GHz

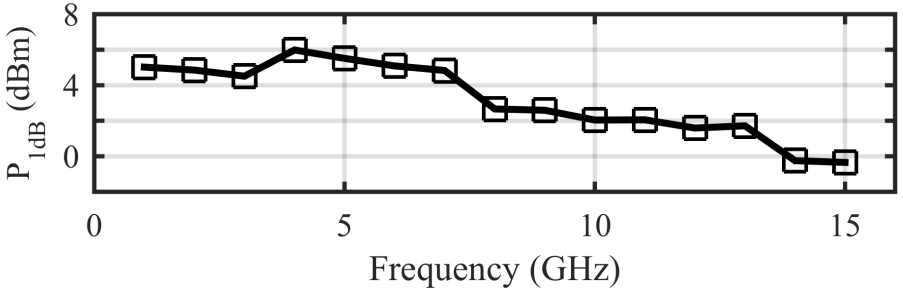
Second Harmonic dominates linearity

SFDR



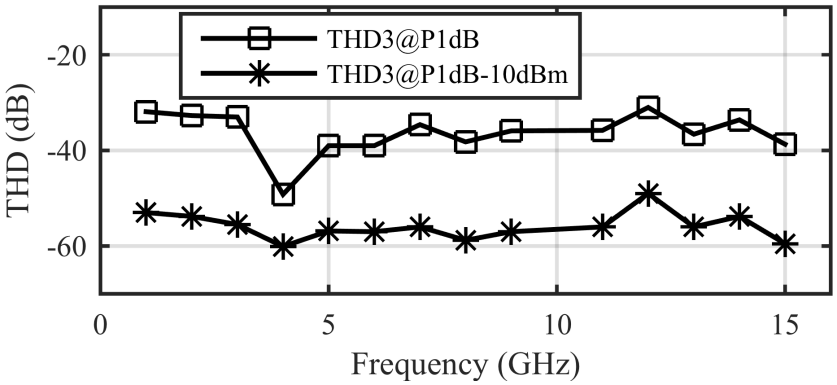
SFDR3>65dB, Noise Floor=-100dBm

Input P_{1dB}



P_{1dB} remains above 0dBm for 1-15GHz input

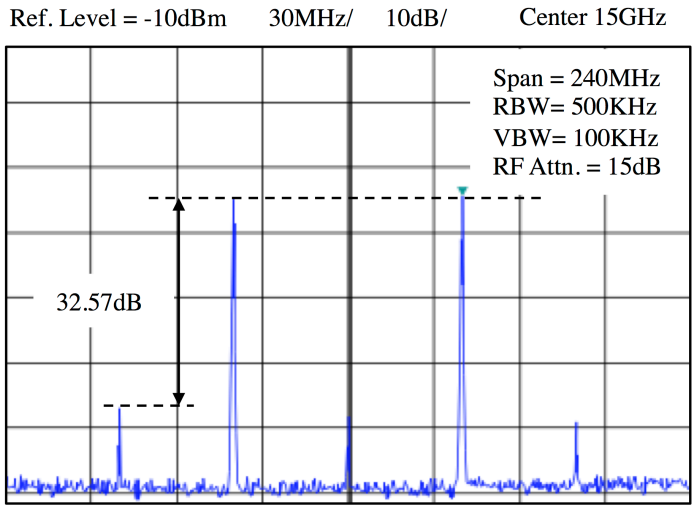
THD



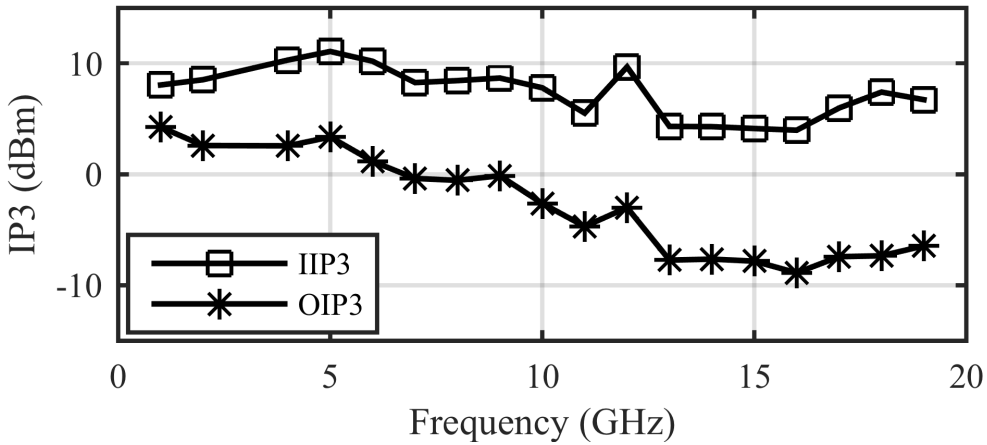
THD3 with ENOB>4.9 bits

Linearity Results @ 40GS/s

Two Tone Tests: Intermodulation Products



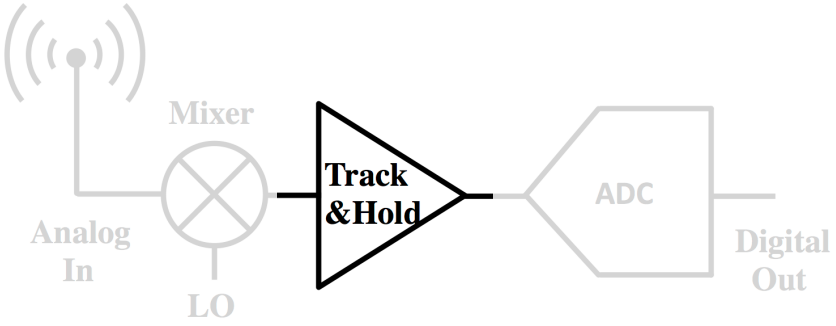
Spectrum showing intermodulation products for two tones at 14.96 GHz and 15.04 GHz



Measured results for two tone tests showing IIP3 and OIP3 for input frequencies upto 19GHz

Design Figures Achieved

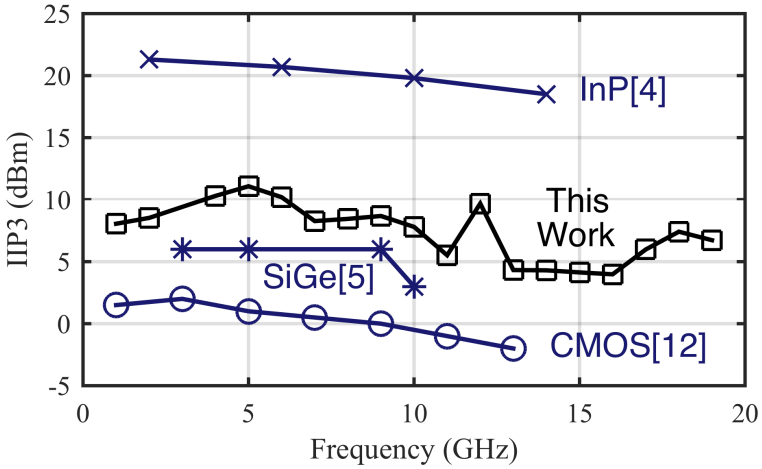
High-speed
Digital Receivers



-Low Distortion		THD3>4.9 bits
-High BW		BW limited
-Medium Power		560mW
-High Sensitivity		SFDR3>65dB
-High Sampling Speed		F_{CLK} = 40GS/s

Conclusion

Peformance Metric	Measurement
Sample Rate	40GS/s
Peak P_{IN}	6dBm
SFDR3@ F_{IN}/F_{CLK}	78dB@6GHz/40GHz
THD3@ F_{IN}/F_{CLK}	-39dB@6GHz/40GHz
IIP3@ F_{IN}/F_{CLK}	11.1dBm@5GHz/40GHz
DC Power Consumption	560mW
Voltage Supply	3.9V
Die-Size	$0.49mm^2$
Process, f_T	90nm SiGe HBT, 300GHz



- A highly linear, 40GS/s THA designed in 90-nm SiGe technology
- Performance compares with InP designs at half the power consumed

Future Work

- Further measurements to characterize
  - Noise of the system
  - Two tone tests
- Address Bandwidth limitations of design
- Attempt integration with ADC circuits

References

- [4] Daneshgar, S.; Griffith, Z.; Rodwell, M.J.W., “A High IIP3, 50 GSamples/s Track and Hold Amplifier in 0.25um InP HBT Technology," Compound Semiconductor Integrated Circuit Symposium (CSICS), 2012 IEEE, vol., no., pp.1,4, 14-17 Oct. 2012
- [5] Shahramian, S.; Carusone, A.C.; Voinigescu, S.P., ``Design Methodology for a 40-GSamples/s Track and Hold Amplifier in 0.18um SiGe BiCMOS Technology," Solid-State Circuits, IEEE Journal of, vol.41, no.10, pp. 2233,2240, Oct. 2006
- [12] Shahramian, S.; Voinigescu, S.P.; Carusone, A.C., “A 30-GS/sec Track and Hold Amplifier in 0.13-µm CMOS Technology," Custom Integrated Circuits Conference, 2006. CICC '06. IEEE, vol., no., pp.493,496, 10-13 Sept. 2006