A DC-to-12.5Gb/s 4.88mW/Gb/s All-rate CDR with a single LC VCO in 90nm CMOS

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Abstract

Main features

- A dual-lane all-rate CDR IC with a single LC VCO in 90nm CMOS
- All-rate clock generator
  - ➢ Static fractional dividers
    - Generate all-rate frequencies without any puncture
  - ➢ Asynchronous phase calibration scheme
    - Obviate phase mismatches of clock signals under PVT variation
- Automatic loop gain control scheme
  - ➢ Autocorrelation function-based CDR loop gain adjustment
    - Operate in the background for the optimum BER performance
  - ➢ Internal accumulation jitter generator
    - Support built-in self-test (BIST) mode with various jitter conditions

Other features

- Reference-less CDR operation for all-rate frequencies
- TRX equalization which covers up to 20dB loss channel
  - ➢ A two stage CTLE and a one-tap DFE RX equalization
  - ➢ A three-tap pre-emphasis TX equalization
- The sensitivity of a CDR – 12mV$_{pp,diff}$
- The power efficiency of the dual-lane CDR operation – 4.88mW/Gb/s

Introduction

Problem statement

- Coexistence of the high-speed and legacy links
- Limitations of conventional CDRs
  - ➢ Limited operational frequency range
    - Cannot offer backward compatibility for low-frequency legacy links
  - ➢ Manual CDR loop gain control
    - Require external controls to optimize the loop gain for each links

→ Wide-band VCO-based CDR with the automatic loop gain control is required

Prior works

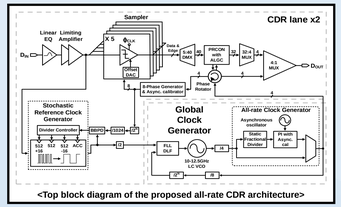
- Wide-band ring VCO-based CDRs [1]-[2]
  - ➢ Small active area
  - ➢ Large random jitter caused by poor noise immunity
    - Prohibit the widespread commercial use in high-speed links
- Multiple LC VCO-based CDRs [3]-[5]
  - ➢ Large active area
    - Increase the unit cost of CDR IC
  - ➢ Low phase noise and good jitter performance
- Manual CDR loop gain setting with the external control

Objective

- All-rate CDR with a small active area and a low phase noise clock
  - ➢ A single LC VCO-based all-rate CDR structure
    - Guarantee low phase noise with small active area
  - ➢ All-rate clock generator from a single LC VCO
    - Extend the clock frequency range from the narrow-band VCO clock without a phase mismatch
- Automatic loop gain control for plug-and-play CDR operation
  - ➢ Background loop gain control
    - Maintain the optimum BER with the perturbation of the input jitter

Top block diagram

- Global clock generator
  - ➢ A single LC VCO
  - ➢ All-rate clock generator
    - Static fractional divider
    - Asynchronous calibration loop
- Two quadrature CDR lanes from DC to 12.5Gb/s
  - ➢ SRCG-based reference-less FLL [1]
  - ➢ Automatic loop gain control
  - ➢ Analog front-end with a two stage CTLE
  - ➢ A one-tap quadrature DFE
  - ➢ A three-tap TX pre-emphasis
- CDR operation
  - ➢ Baud-rate sampling mode
    - 6.25Gb/s to 12.5Gb/s
  - ➢ Oversampling mode
    - DC to 6.25Gb/s



<Top block diagram of the proposed all-rate CDR architecture>

Static fractional divider

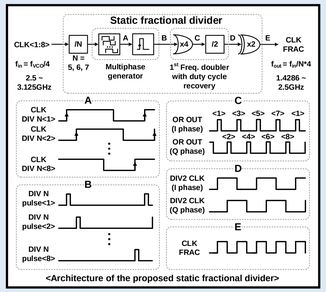
- All-rate clock generation covering between $f_{max.VCO}/2$ and $f_{max.VCO}$
  - ➢ 10GHz to 12.5GHz clock from LC VCO tuning range
  - ➢ 6.25GHz to 10GHz clock from the static fractional divider
- Required resolution of the fractional division ratio for all-rate clock generation without any puncture

$$D_{resol} = (f_{max.VCO} - f_{min.VCO}) / f_{min.VCO}$$

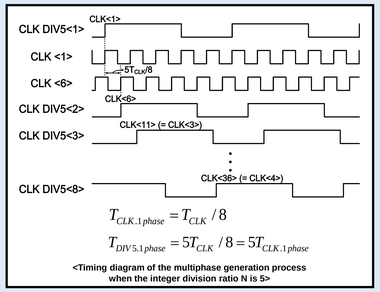
- Generated output frequency of the static fractional divider

$$f_{out} = f_{in} / N \times 4 \quad (N = 5, 6, 7)$$

- Efficient Implementation of 0.25 division ratio with CMOS integer dividers and two frequency multipliers
  - ➢ Power consumption of 10mW and the active area of 0.05mm^2
  - ➢ No additional modulation or dithering process



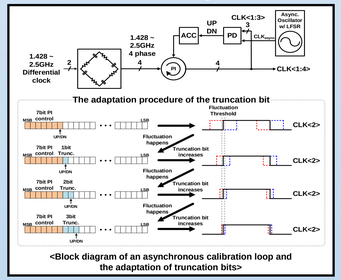
<Architecture of the proposed static fractional divider>



<Timing diagram of the multiphase generation process when the integer division ratio N is 5>

Asynchronous calibration loop

- Poly phase filter and asynchronous calibration loop
  - ➢ Quadrature phase clock generation
  - ➢ Phase mismatch correction
- Automatic adjustment of the truncation bits
  - ➢ Optimization of the convergence time



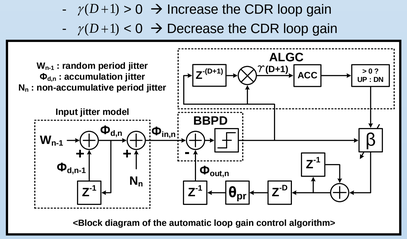
<Block diagram of an asynchronous calibration loop and the adaptation of truncation bits>

Automatic loop gain control

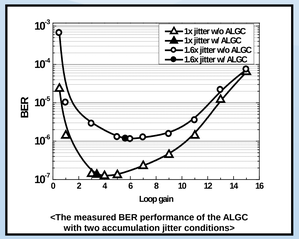
- The optimum CDR loop gain that minimizes MSE between the input data and the recovered clock of a CDR
  - ➢ Standard deviation of the input accumulation jitter σ_W [6]
- A equation describing the input accumulation jitter σ_W in a rotator-based BB CDR

$$\sigma_W^2 \approx (\beta\theta_{pr})^2 \left(1 + 2\gamma(D+1) / K_{BBPD}\beta\theta_{pr}\right)$$

- The sign of the autocorrelation function $\gamma(D+1)$ of the BBPD output
  - ➢ The index of the loop gain adjustment
    - $\gamma(D+1) > 0$ → Increase the CDR loop gain
    - $\gamma(D+1) < 0$ → Decrease the CDR loop gain



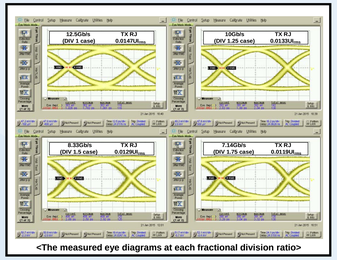
<Block diagram of the automatic loop gain control algorithm>



<The measured BER performance of the ALGC with two accumulation jitter conditions>

Experimental results

- Dual-lane reference-less CDR error-free operation
  - ➢ PRBS31 NRZ input from 50Mb/s to 12.5Gb/s
    - Low freq. limit of test equipment – 50Mb/s
  - ➢ With 20dB loss FR4 backplane channel
  - ➢ The sensitivity of the CDR – 12mVpp.diff
  - ➢ The power efficiency – 4.88mW/Gb/s

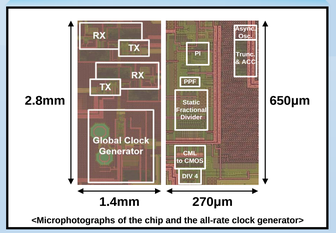


<The measured eye diagrams at each fractional division ratio>

Comparison of the CDR performance

	ISSCC 2014 [2]	CICC 2014 [4]	CICC 2014 [5]	This work (Ring VCO for performance comparison)	This work
Technology	65nm	0.13μm	20nm	90nm	**90nm**
Supply (V)	1.2/1.0	3.3/1.8/1.2	1.2/1/0.95	1.0	**1.0**
Architecture	Half rate Single RX	Half rate Single lane	Half rate Quad lane	Quad rate Dual lane	**Quad rate Dual lane**
Data rate	4Gb/s - 10Gb/s	6.5Mb/s - 11.3Gb/s	0.5Gb/s - 16.3Gb/s	50Mb/s - 12.5Gb/s	**50Mb/s - 12.5Gb/s**
Oscillator	Ring	4 LC VCOs	4 LC & 4 Ring VCOs	Ring	**Single LC VCO**
VCO tuning range (GHz)	2-7.5 (57.9%)	5.6-11.5 (34.5%)	LC : 8-16.3 (34.2%) Ring : 2-6.4 (52.4%)	6.25-12.5 (33.3%)	**10-12.5 (11.1%)**
Automatic CDR loop gain control	X	X	X	O	**O**
Recovered clock jitter (UI_{rms})	0.011 (2.2ps$_{rms}$ @200p)	Not specified (TX RJ 0.0045UI$_{rms}$)	Not specified (TX RJ 0.0057UI$_{rms}$)	0.009 (5.8ps$_{rms}$ @640p)	**0.004 (2.6ps$_{rms}$ @640p)** T_{clk}=640ps)
Power (mW)	22.5 @10Gb/s	415 @11.3Gb/s	278 / lane @16.3Gb/s	242 @12.5Gb/s	**244 @12.5Gb/s**
FoM (mW/Gb/s)	2.25	18.36	8.53	4.84	**4.88**
Area (mm^2)	1.63	4	4.36	2.63	**3.03**

Chip photograph



<Microphotographs of the chip and the all-rate clock generator>

Conclusion

Entire architecture

- A dual-lane all-rate CDR with a single LC VCO in 90nm CMOS
  - ➢ Two quadrature CDR lanes from DC to 12.5Gb/s
    - SRCG-based reference-less FLL
    - Automatic loop gain control
    - Analog front-end with a two stage CTLE
    - A one-tap quadrature DFE
    - A three-tap TX pre-emphasis
  - ➢ Global all-rate clock generator
    - A single LC VCO which covers 10GHz to 12.5GHz
    - Static fractional divider
    - Asynchronous calibration loop

All-rate clock generator

- Static fractional divider
  - ➢ All-rate clock frequency generation without any puncture
  - ➢ A fractional division ratio of 0.25
  - ➢ No additional modulation or dithering process
  - ➢ CMOS-based power- and area-efficient design
- Asynchronous calibration loop
  - ➢ Reduction of phase mismatch of the quadrature clock
  - ➢ Fast convergence of the calibration loop via automatic adjustment of the truncation bits

Automatic loop gain control

- Autocorrelation function-based background loop gain control
  - ➢ Automatically adjusted CDR loop gain for the lowest BER depending on the input jitter condition
- Internal accumulation jitter generator
  - ➢ Support built-in self-test (BIST) mode under various input accumulation jitter condition

Measured results

- Error-free operation under 20dB loss channel
- The sensitivity of the CDR in the dual-lane operation – 12mVpp.diff
- The power efficiency in the dual-lane operation – 4.88mW/Gb/s

References

[1] R. Inti, et al., "A 0.5-to-2.5-Gb/s reference-less half-rate digital CDR with unlimited frequency acquisition range and improved input duty-cycle error tolerance," ISSCC Dig. Tech. Papers, pp. 438-439, Feb. 2011.

[2] G. Shu, et al., "A 4-to-10.5Gb/s 2.2mW/Gb/s continuous-rate digital CDR with automatic frequency acquisition in 65nm CMOS," ISSCC Dig. Tech. Papers, pp. 150-151, Feb. 2014.

[3] D. Dalton, et al., "A 12.5-Mb/s to 2.7-Gb/s continuous-rate CDR with automatic frequency acquisition and data-rate read back," ISSCC Dig. Tech. Papers, pp. 230-231, Feb. 2005.

[4] Kenney, J., et al., "A 6.5Mb/s to 11.3Gb/s continuous-rate clock and data recovery," IEEE CICC, pp. 1-4, Sept 2014.

[5] Savoj, J., et al., "Wideband flexible-reach techniques for a 0.5–16.3Gb/s fully-adaptive transceiver in 20nm CMOS," IEEE CICC, pp. 1-4, Sept 2014.

[6] J. Lee and H. Bae, "Application of Kalman Gain for Minimum Mean-Squared Phase-Error Bound in Bang-Bang CDRs," IEEE Trans. Circuits Syst. I, Reg. Papers, vol.59, no.12, pp.2825-2834, Dec. 2012.