A 16nm Configurable Pass-Gate Bit-Cell Register File for Quantifying the V_{MIN} Advantage of PFET versus NFET Pass-Gate Bit Cells

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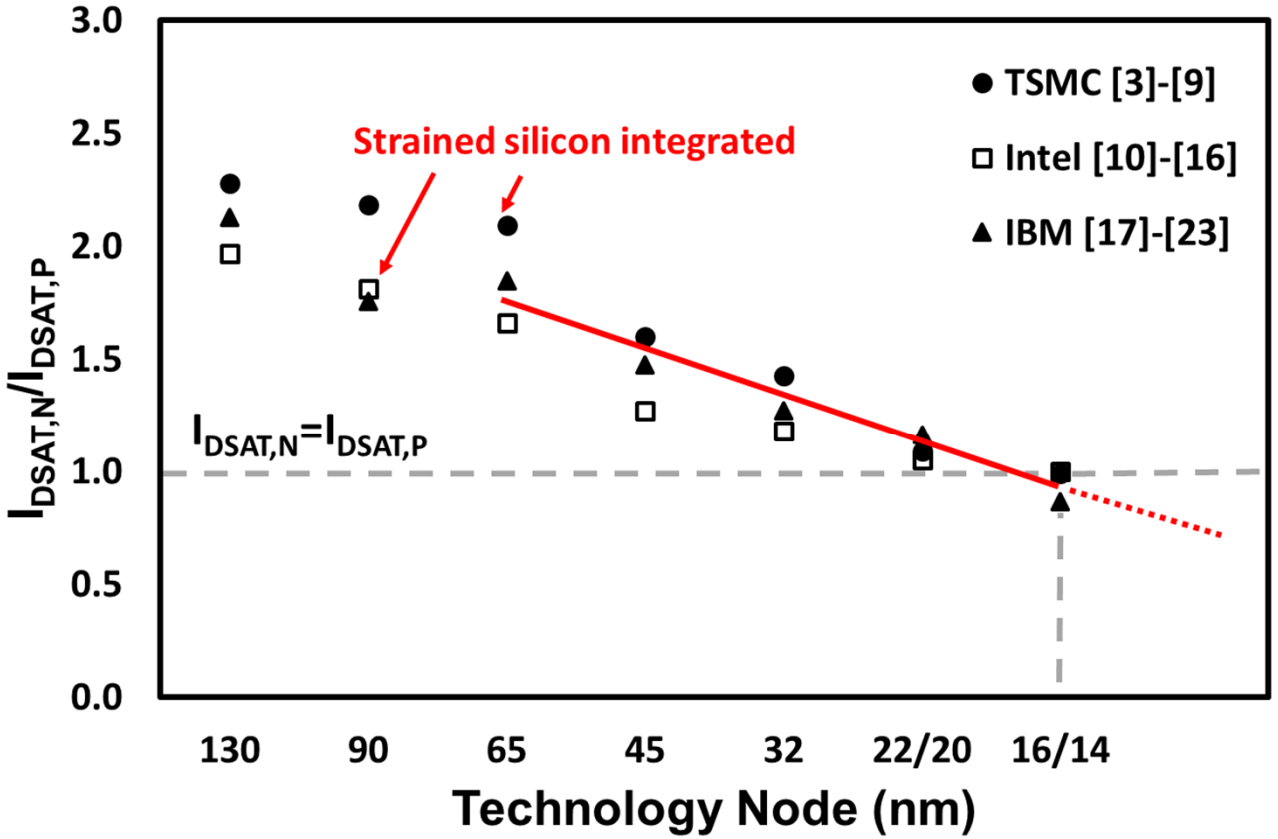
Outline

- Motivation
- Design and Implementation
- Measurement Results
- Conclusion

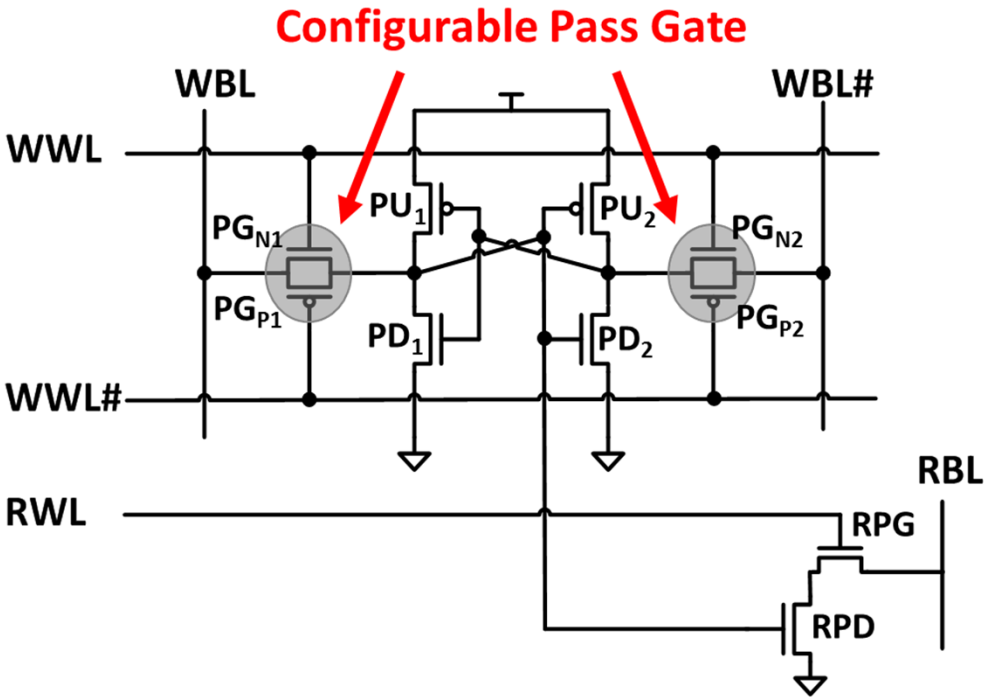
Motivation



- PFET I_{DSAT} ≥ NFET I_{DSAT} in 14/16nm technology.
  - Significantly affects circuits that depend on the PFET and NFET I_{DSAT} strengths.

Configurable Pass-Gate Bit Cell

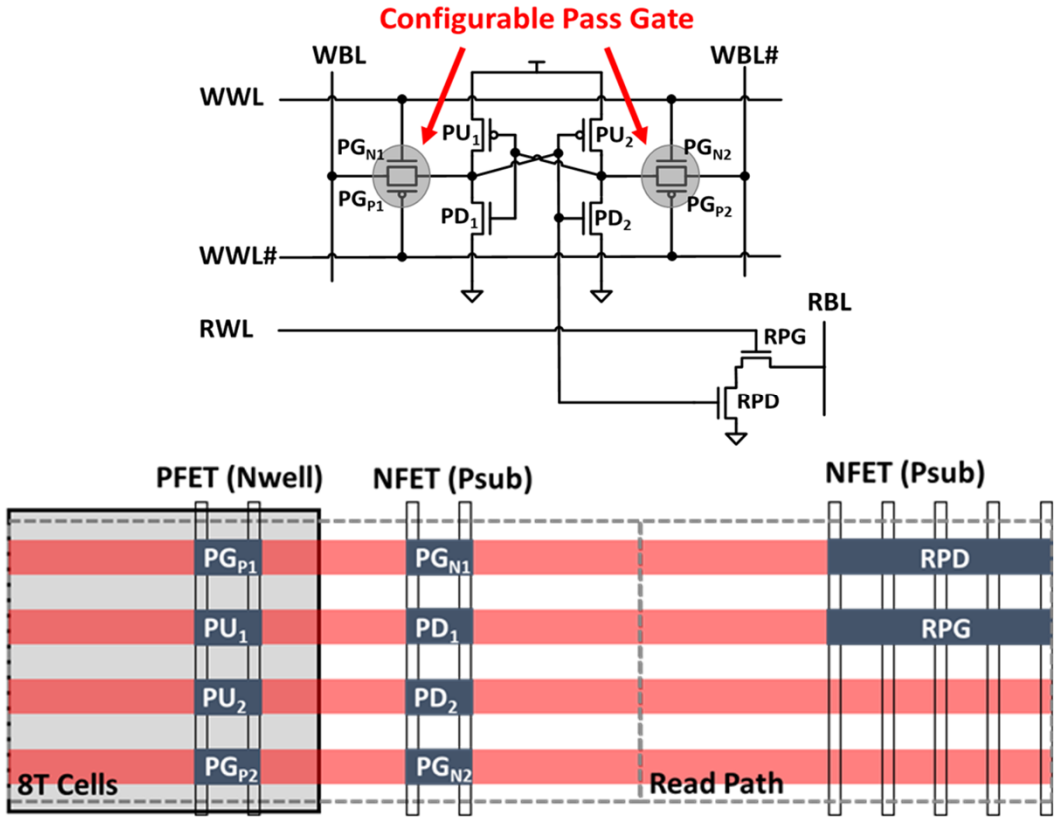
Schematic



- The configurable pass gate enables either
  - Transmission gate, NFET pass gate, or PFET pass gate.
- PU,PD, and PG are 2-fin devices with the same channel length and V_{th} type.

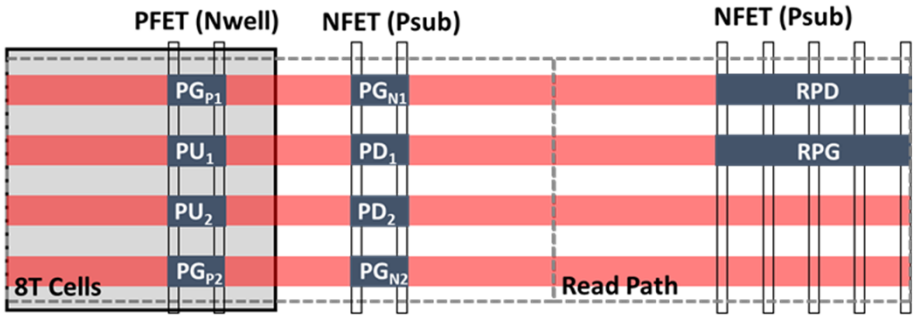
Configurable Pass-Gate Bit Cell

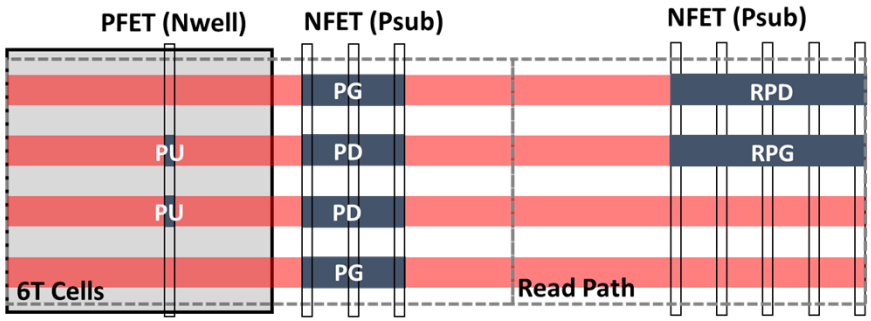
Layout



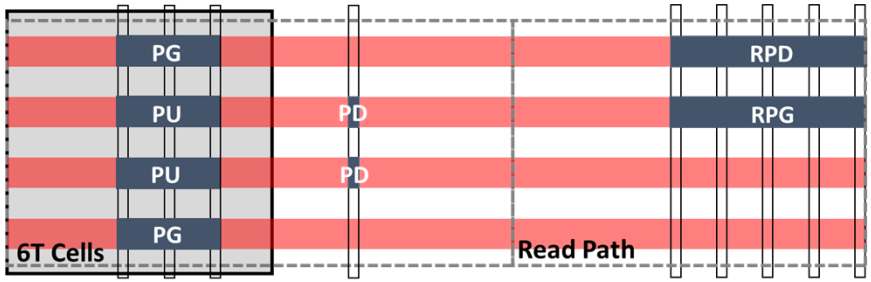
- A register-file bit-cell layout employs 4 poly pitches.
- The bit-cell area is 0.204μm^2 in a 16nm FinFET technology.

PFET vs NFET Pass-Gate Bit-Cell Layout





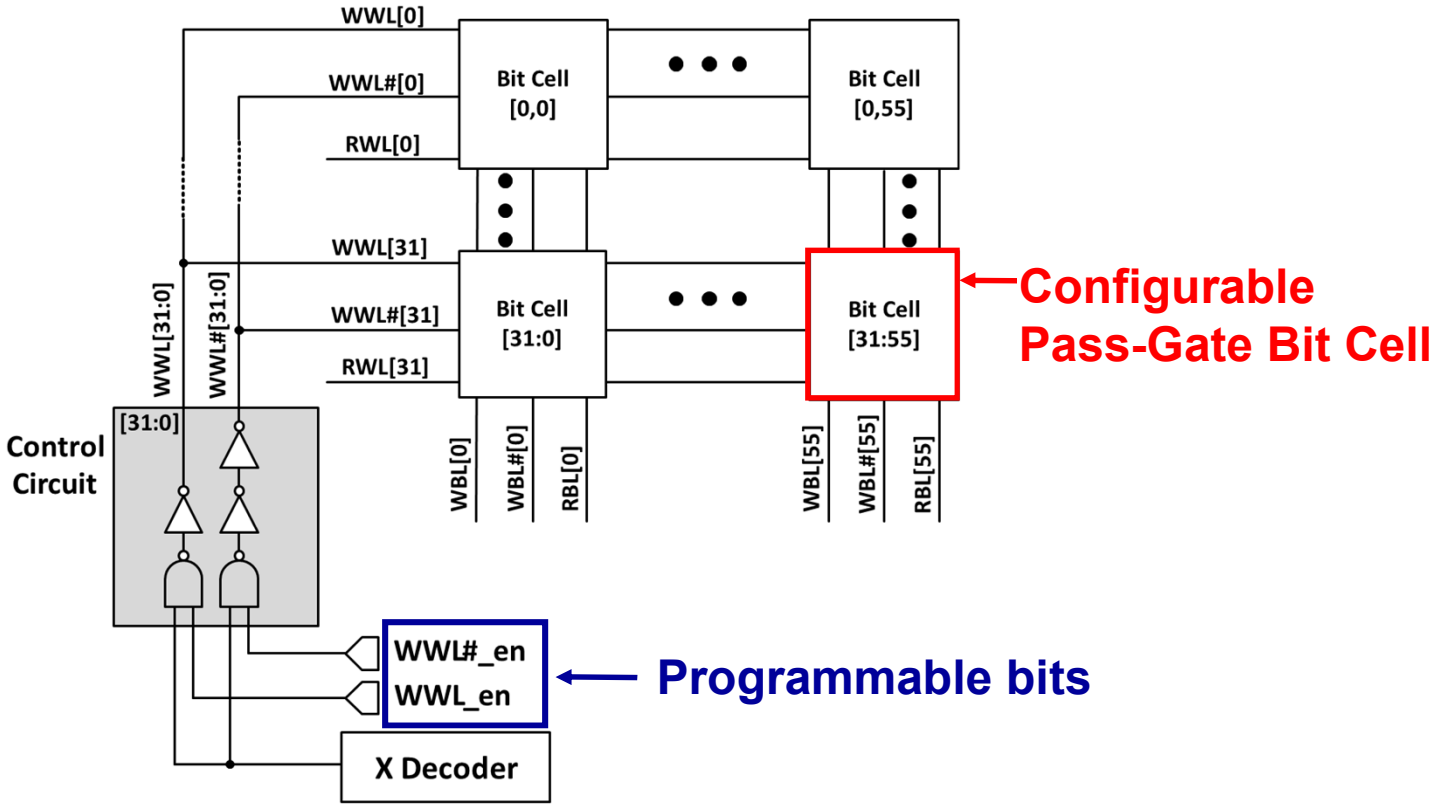
(a) NFET pass-gate bit cell with a fin width of PU:PD:PG = 1:3:3



(b) PFET pass-gate bit cell with a fin width of PU:PD:PG = 3:1:3

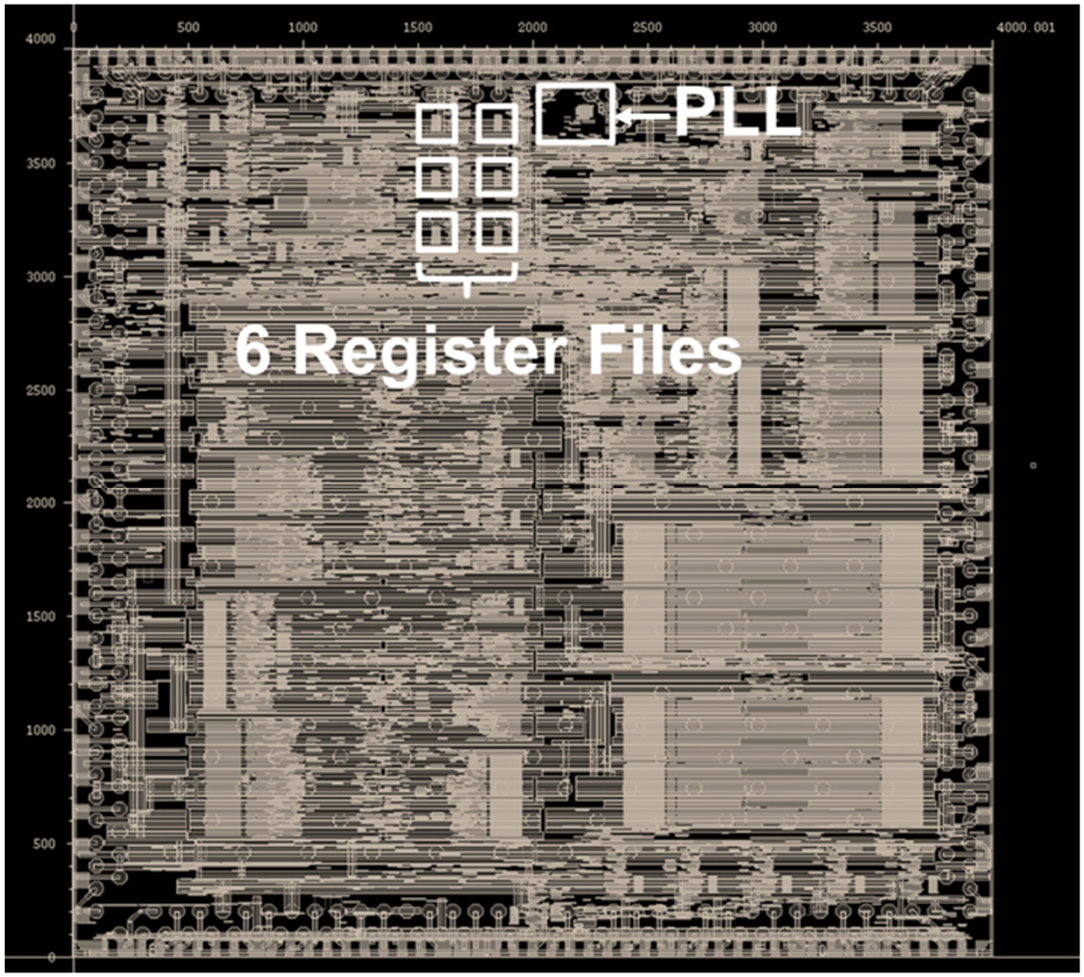
- **(a) NFET pass-gate bit cell with PU:PD:PG=1:3:3 area is 0.190μm^2.**
- **(b) PFET pass-gate bit cell consumes the same area.**

Bit-cell Array and Control Circuits



- A control circuit generates WWL and WWL#.
- Programmable WWL_en and WWL#_en bits enable three pass-gate configurations.

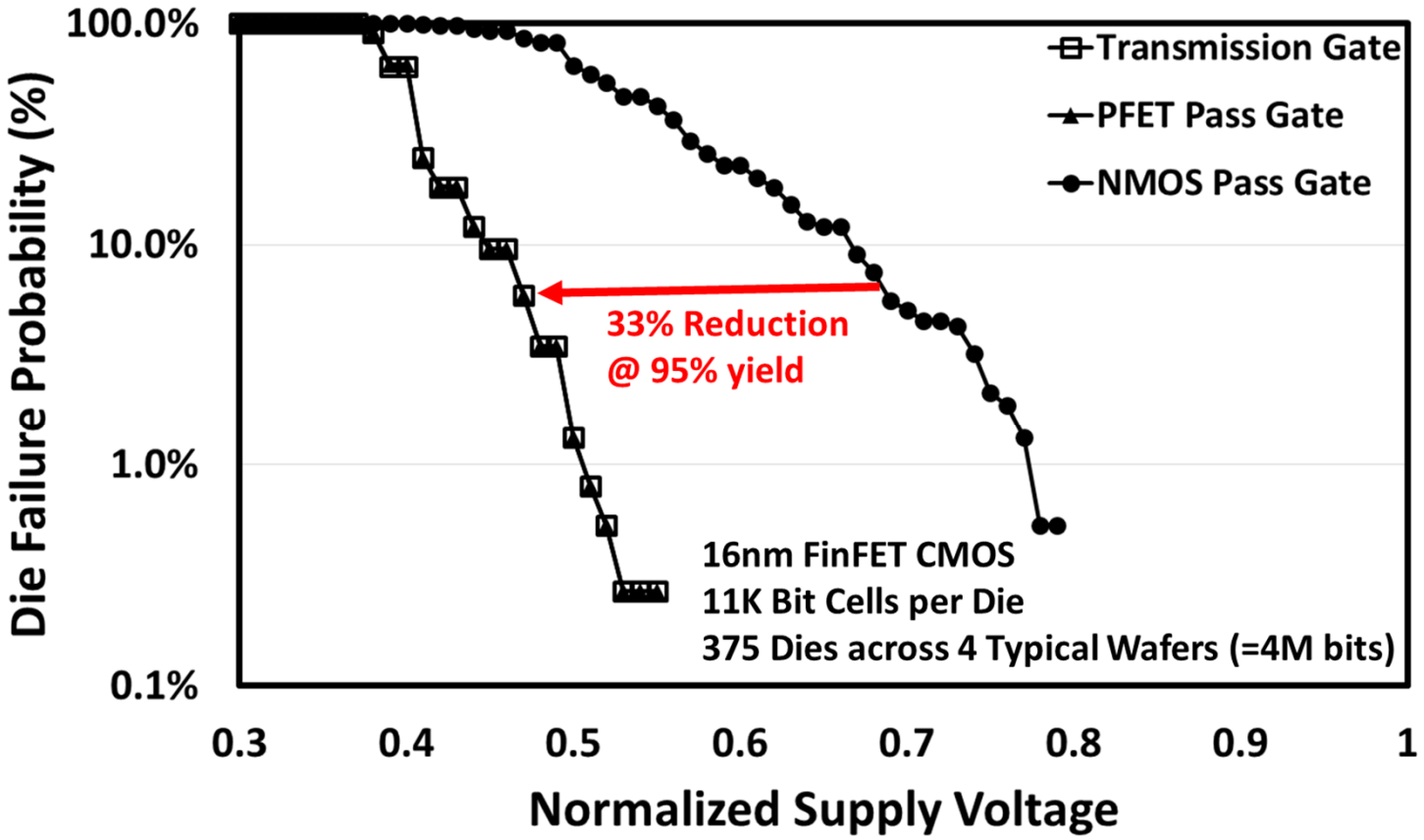
Test Chip Micrograph and Features



Technology	16nm FinFET CMOS
Die Area	16mm^2
Register File Configuration	32 word x 56 bit
Register File Area	2,868μm^2
Total Capacity	11Kb (6 x Register File)

Measured Die Failure Probability Distribution

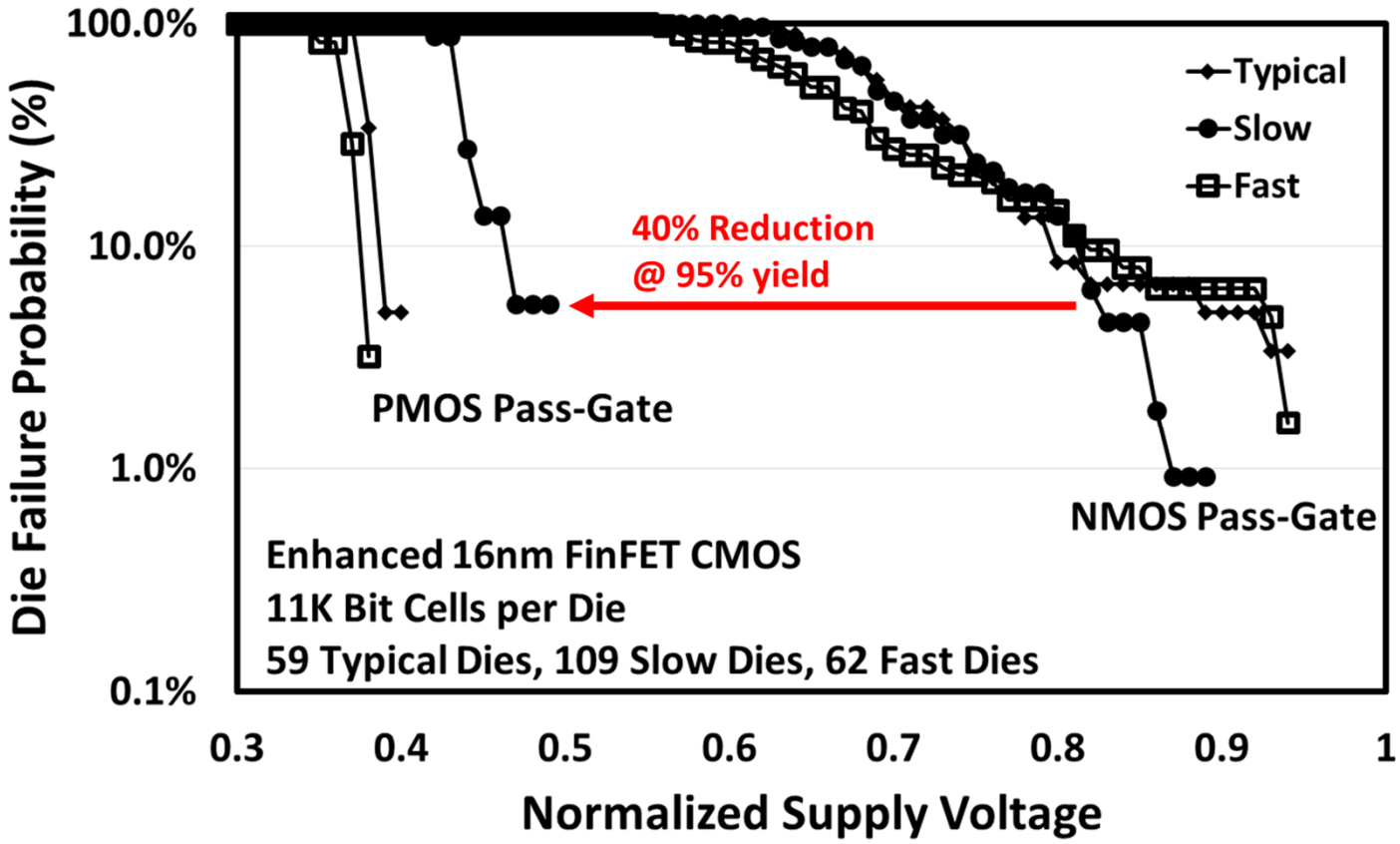
16nm FinFET CMOS



- 33% V_{MIN} reduction for the PFET pass gate at 95% yield.

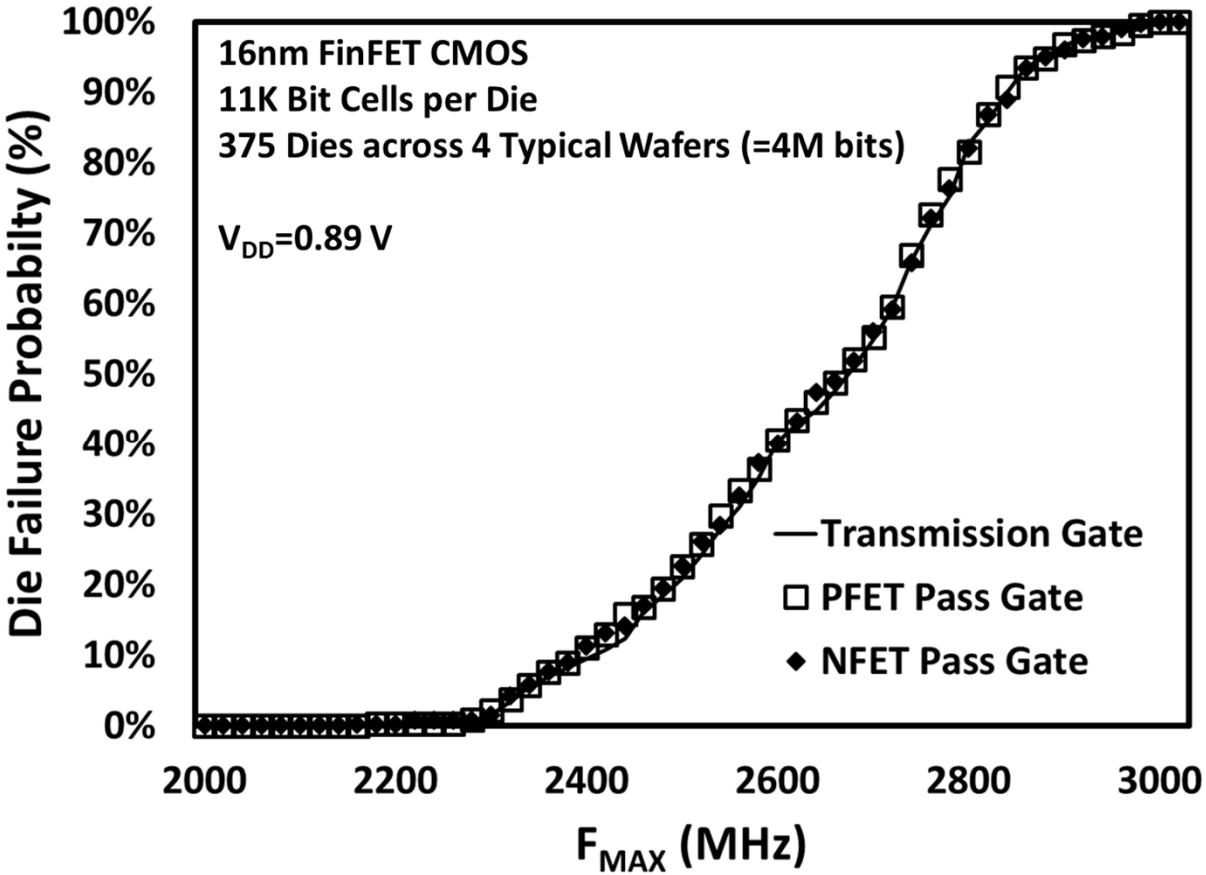
Measured Die Failure Probability Distribution

Advanced 16nm FinFET CMOS



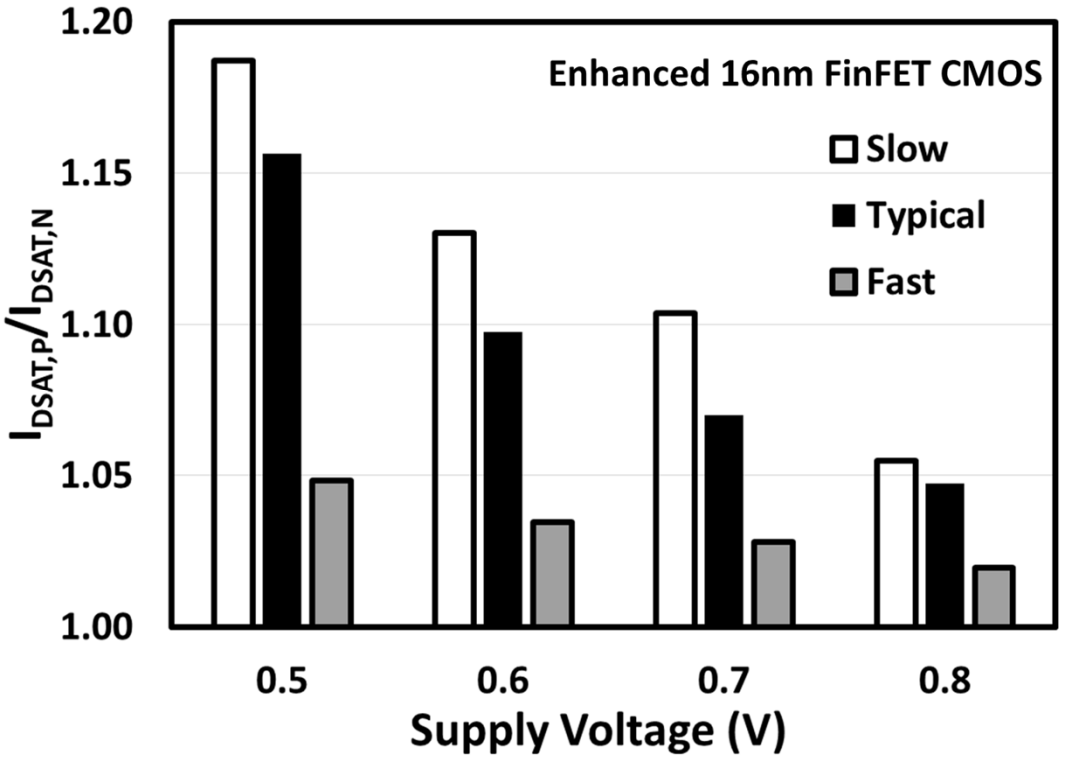
- **Measurements consistently demonstrate a significant V_{MIN} reduction (>40%) for the PFET pass gate.**

Measured F_{MAX} at Nominal Voltage



- At 0.89V, F_{MAX} for the Transmission gate, PFET pass-gate, and NFET pass-gate are almost equal.
  - No performance degradation for the PFET pass-gate.

Measured $I_{DSAT,P}/I_{DSAT,N}$ vs Supply Voltage



- PFET I_{DSAT} for TT is:
  - ~5% higher than NFET I_{DSAT} at 0.8V.
  - ~15% larger than NFET I_{DSAT} at 0.5V.
- The improvement in PFET I_{DSAT} relative to NFET I_{DSAT} at low V_{DD} contributes to the large V_{MIN} reduction.

Conclusion

- A configurable pass-gate bit-cell register file is implemented in two 16nm FinFET technologies to allow a direct comparison of NFET and PFET pass-gate bit cells.

- The PFET pass-gate bit cell provides a 33% and >40% V_{MIN} reduction at 95% yield w/o area or performance disadvantage.

- The superior PFET drive strength at low voltages explains the V_{MIN} benefit for the PFET pass-gate bit cell.

Thank You!