A Field-Programmable Noise-Canceling Wideband Receiver with High-Linearity Hybrid Class-AB-C LNTAs

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Motivation

Modern SDR receivers demand high linearity and sensitivity. OB linearity usually limited by LNAs.

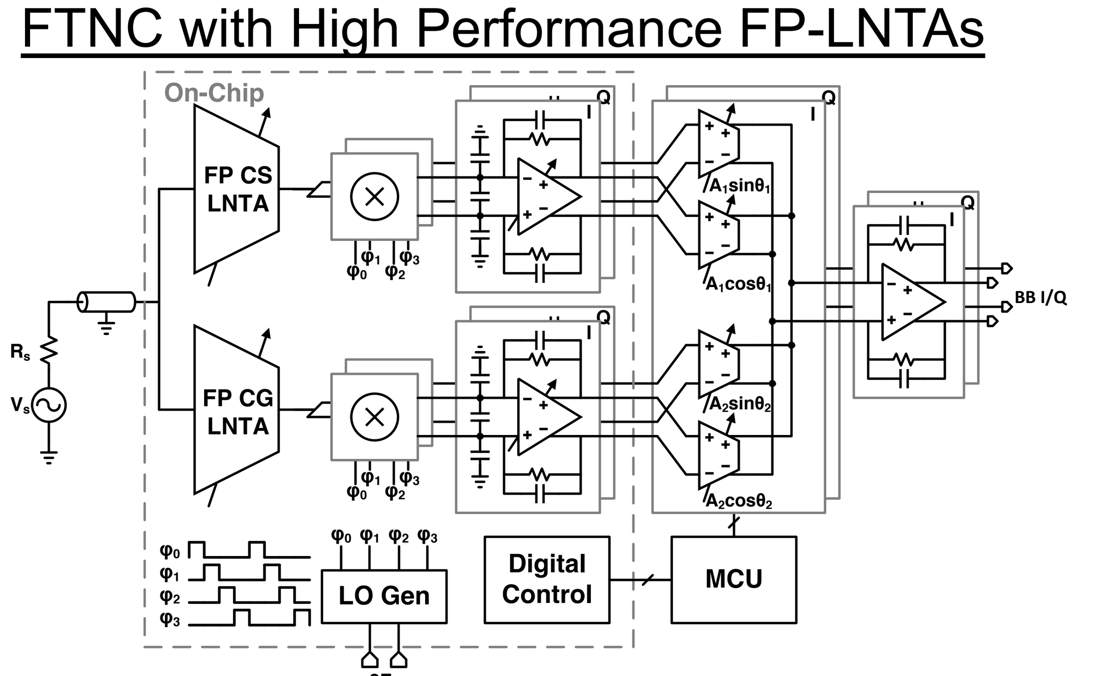
- Mixer-first receiver [1]:
  - High linearity, High NF
- FTNC receiver [2]:
  - CS LNTA limits linearity, Low NF

These two architectures lack LNTA reverse isolation and suffer from LO leakage to the antenna.

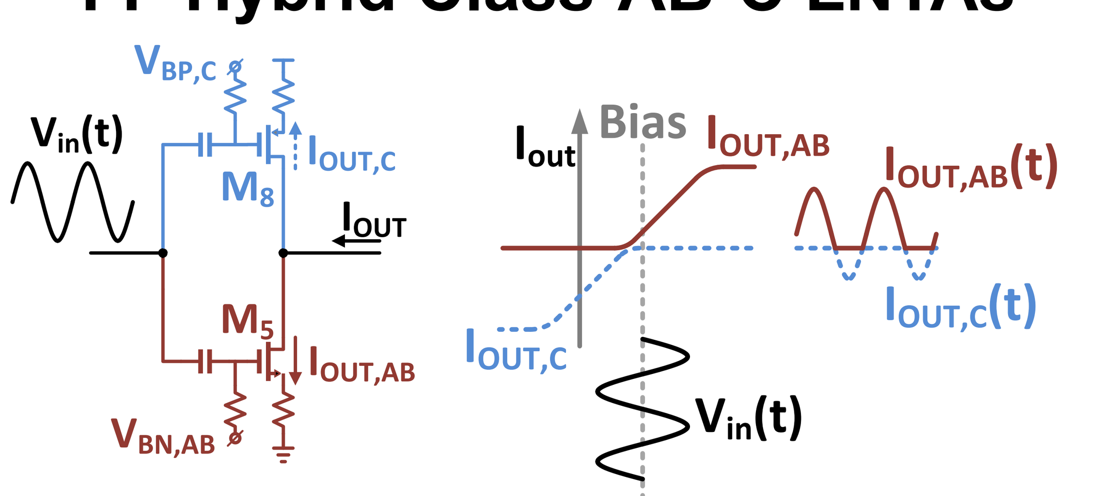
In addition to linearity and NF, field-programmable operation is also desired so that an SDR does not need to be designed for the worst case scenario across all supported standards and to save power consumption.

In this paper, we propose a receiver architecture that combines high performance field-programmable CS and CG LNTAs with the FTNC principle to achieve high linearity, low NF and low LO leakage.

FTNC with High Performance FP-LNTAs



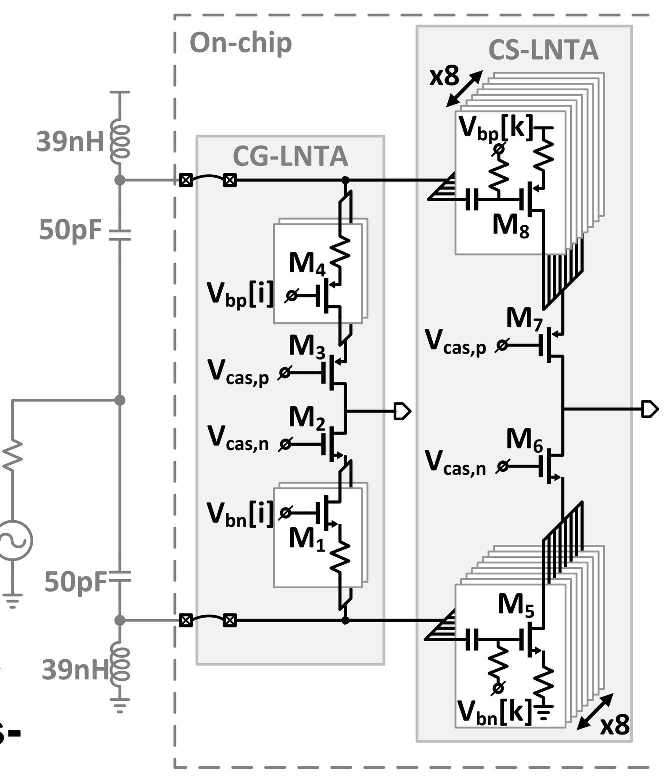
FP Hybrid Class-AB-C LNTAs



For strong-inversion and energy-efficient operation, V_{ov} of transistors is usually between 150mV and 200mV. Under large blocker voltage swings, a single NMOS cell operates in Class-AB (brown). When paired with a Class-C biased PMOS (blue), linear operation range is greatly extended. Now compression is limited by output swing.

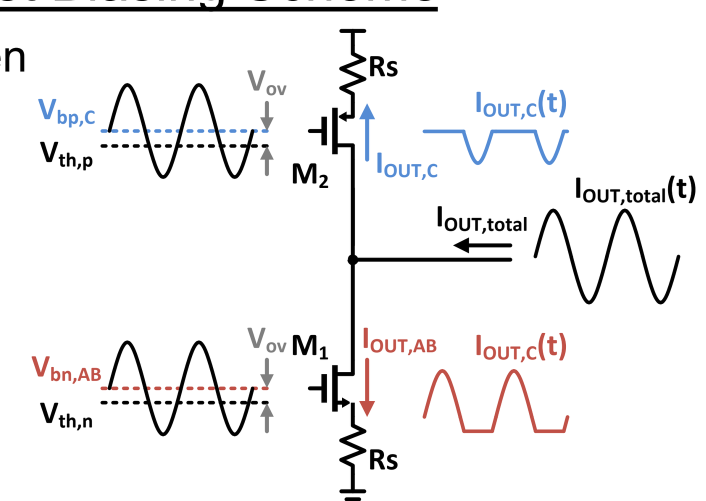
Implementation of FP CS-CG LNTAs

- CS-LNTA: x8 slices
- CG-LNTA: x2 slices
- Res-degen Gm cells
  - Better linearity
  - Improve P-N matching
  - Reduce voltage swing seen by transistors
- Each PMOS and NMOS Gm cell can be individually biased in **Class-AB**, **Class-C** or **Off** mode.



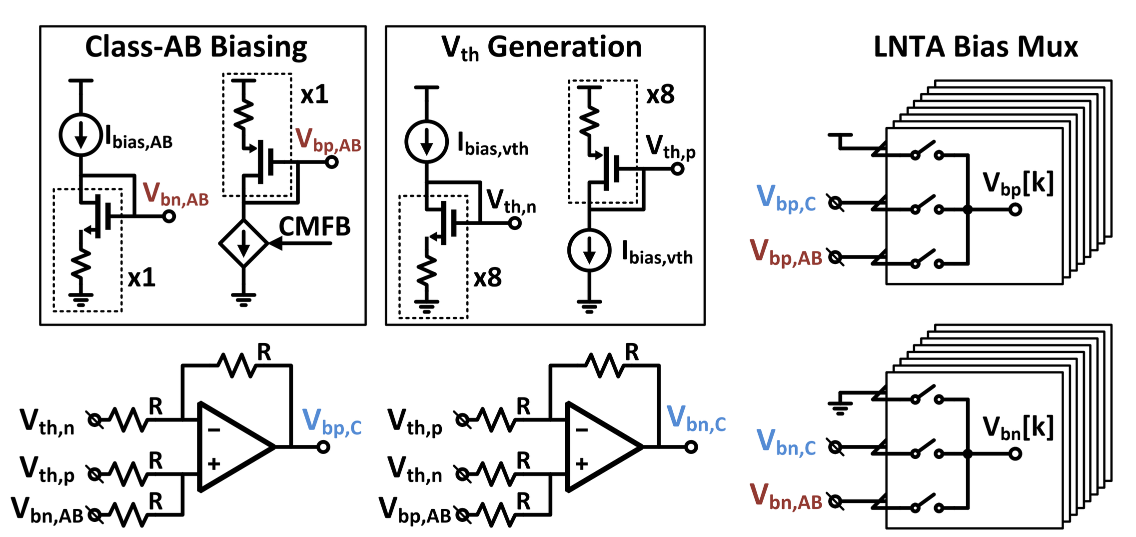
PVT-Robust Biasing Scheme

- PMOS turned on when NMOS turned off
- P-N transfer curve aligned across PVT
- Class-AB and Class-C bias voltages need to track V_{th} of PMOS and NMOS



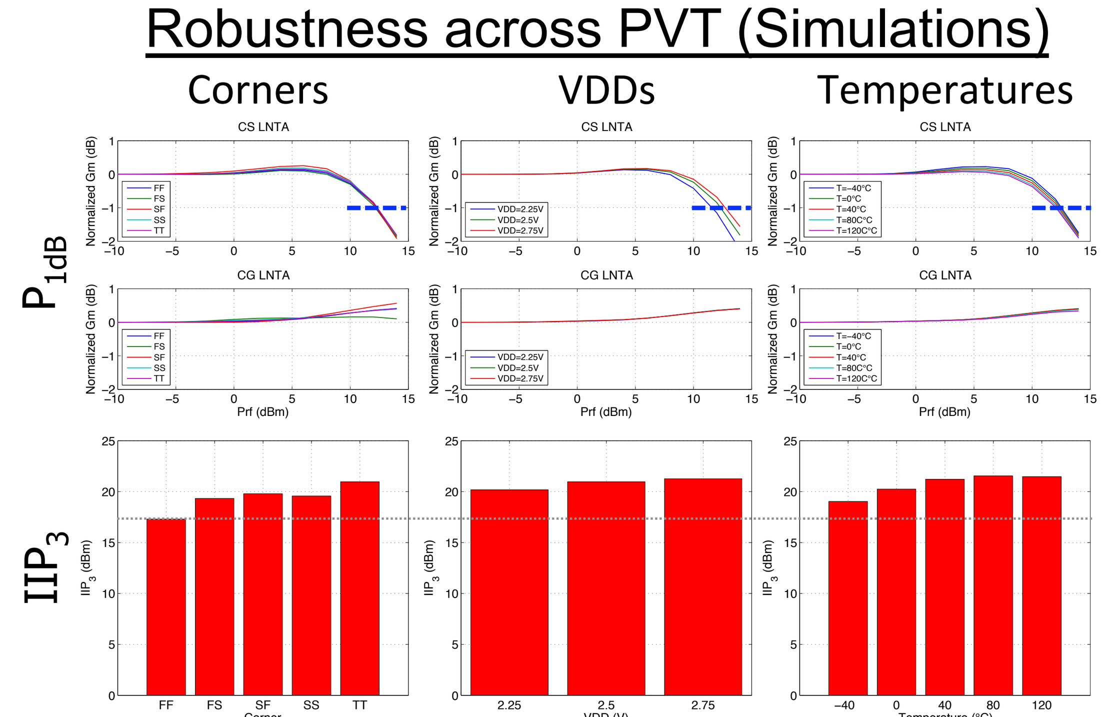
$$V_{bp,C} = V_{th,p} + V_{bn,AB} - V_{th,n}$$

$$V_{bn,C} = V_{th,n} + V_{bp,AB} - V_{th,p}$$



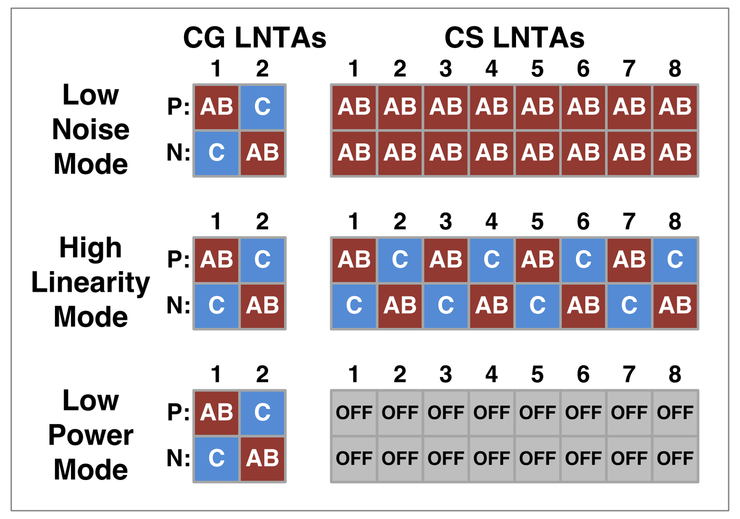
Class-AB bias voltages and V_{th} of NMOS and PMOS cells are generated with constant current biasing. Class-C bias voltages are calculated with OpAmps.

Robustness across PVT (Simulations)



Field-Programmable Operation

The LNTAs can be configured into many different operation modes. Here, we show the programmability of the design with three specific modes:



Low Noise Mode: all CS LNTAs are biased in Class-AB. This is for cases where highest sensitivity is needed. NF is minimized but power is high.

High Linearity Mode: half of CS LNTAs are biased in Class-C the other half are biased in Class-AB. Best linearity – NF tradeoff.

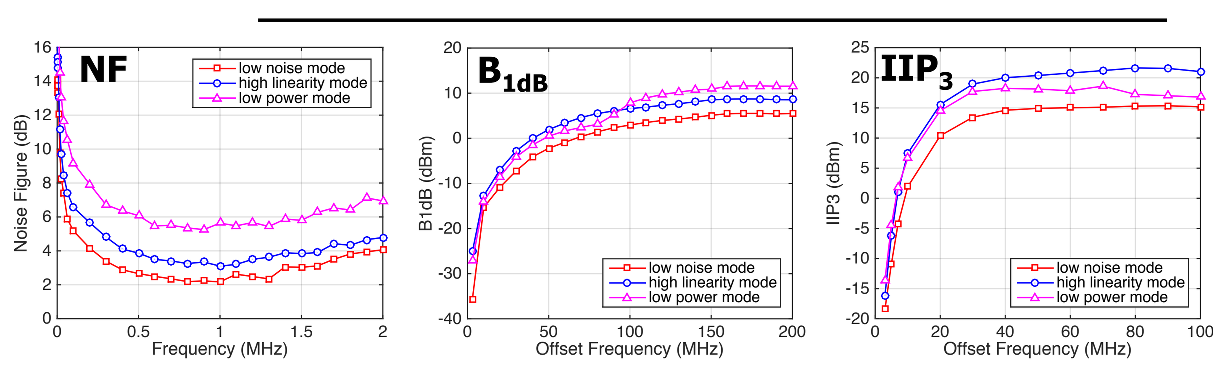
Low Power Mode: the entire CS branch is powered down. CG LNTA offers excellent linearity but higher NF. Power is much lower.

CG LNTAs are always biased in Class-AB-C across the three modes.

Measurement Results

Performance and power consumption of the receiver are measured across different operation modes. The results meet our predictions and very high performance is demonstrated.

	NF	B_{1dB}	IIP_3	P_{DC}
Low NF Mode	Low ☺ (2.2dB)	Moderate (+5dBm)	Moderate (+15dBm)	High ☹ (49mA)
High Lin. Mode	Moderate (3dB)	High ☺ (+8.5dBm)	High ☺ (+21dBm)	Moderate (42mA)
Low Power Mode	High ☹ (5.5dB)	High ☺ (+11dBm)	High ☺ (+17dBm)	Low ☺ (20mA)

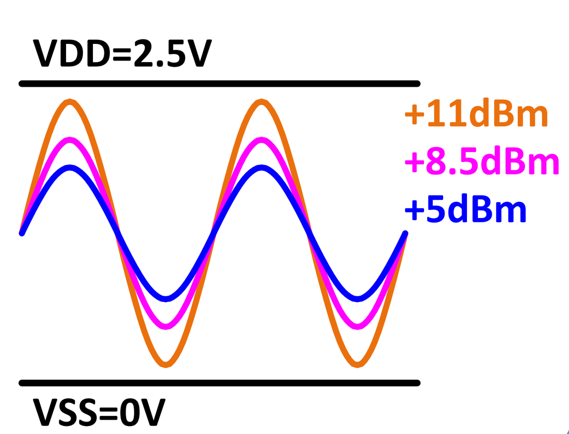


The receiver demonstrate very high linearity in all three modes. The corresponding blocker voltage swings for B1dB point are:

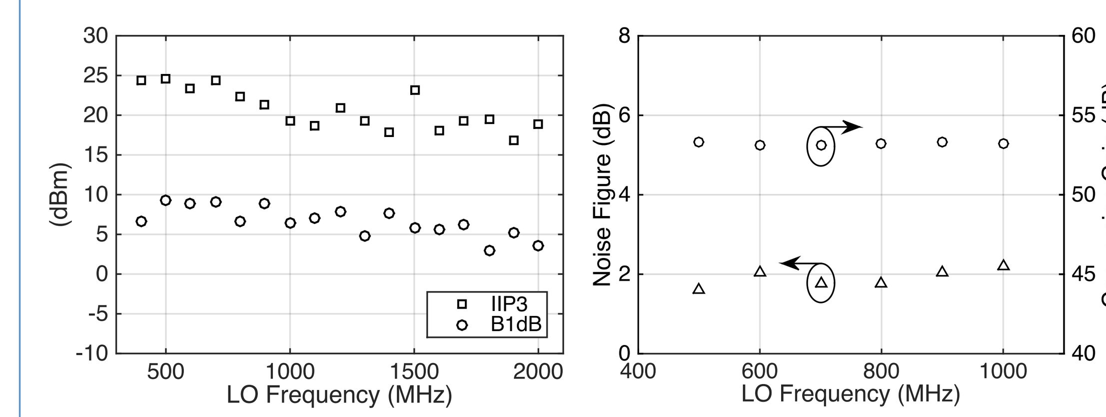
- +11dBm → 2.24Vpp
- +8.5dBm → 1.68Vpp
- +5dBm → 1.12Vpp

It can almost handle **rail-to-rail blocker**

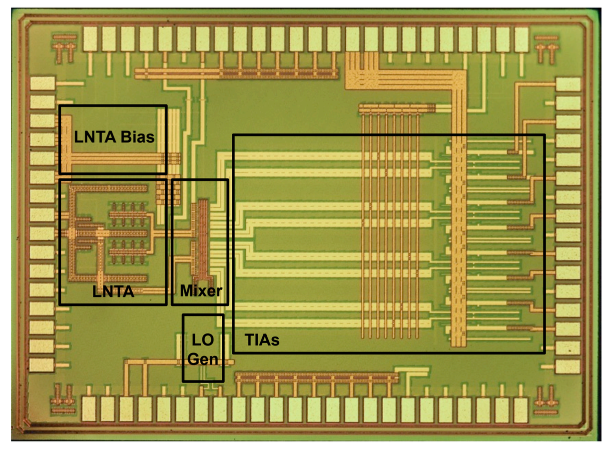
Measured @flo=900MHz



Performance vs. LO Freq.



- Fabricated in 40nm CMOS LP technology
- 1.8mm x 1.3mm
- Active area 1.6mm2
- Analog VDD = 2.5V
- LO path VDD = 1.1V



Comparison to the State of the Art

Design Type	Field-Programmable RX			Wideband RX				LNTA
Reference	This Work			[1]	[2]	[4]	[5]	[6]
	Low Noise	High Linearity	Low Power					
CMOS Technology	40nm			65nm	40nm	28nm	40nm	65nm
Frequency (GHz)	0.4-2.0			0.05-2.4	0.3-2.9	0.4-6	0.1-2.8	1.5-2.0
Max Gain (dB)	53	47	47	80	58	70	50	100mS
NF (dB)	2.2	3	5.5	5.5	1.9-2.1	1.8	1.8	6.5
OB IIP3 (dBm)	+15	+21	+17	+27	+12	+5	+3	+20
B1dB-CP (dBm)	+5	+8.5	+11	+5**	0	0	N/R	+8
LO Leakage (dBm)	-84.6	-85.6	-84.2	N/R	N/R	N/R	-82	N/R
Analog Current (mA)	39.9	32.8	15.0	12	24	20.4	24	7.5
LO Current (mA)	4.4-20	4.4-20	2.2-10	6-33	3-36	1.6-23.6	0.5-12.2	N/R
Power Supply (V)	2.5(Analog)/1.1(LO)			1.2(LO) / 2.5(BB)	1.3	0.9	1.1	1.5

N/R = Not Reported **Estimated

- This design has comparable linearity to [1] and better NF.
- The designs in [2], [4], [5] have slightly better NF, but this work has much higher blocker tolerance and IIP3.
- The LNTA in [6] has a very high measured blocker tolerance, but the LNTAs presented here deliver similar linearity with much lower NF.

Acknowledgments

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References

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