A 130nm Canary SRAM for SRAM Dynamic Write V_{MIN} Tracking across Voltage, Frequency, and Temperature Variations

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Introduction

MOTIVATION

- Dynamic voltage and frequency scaling (DVFS) lowers supply voltage and reduces energy per operation and boosts performance in need in system on chips (SoCs)
- Device scaling and process variation limits the SRAM minimum operating voltage (V_{MIN})
- Hard to lower overall SoC V_{MIN} sharing the same rail with logic and SRAM which creates a bottle neck

PRIOR WORKS

- Peripheral assists and dual-rail techniques can lower the V_{MIN} at the cost of energy and area
- Canary SRAMs can track SRAM V_{MIN} in theory with lower overhead for bigger SRAMs

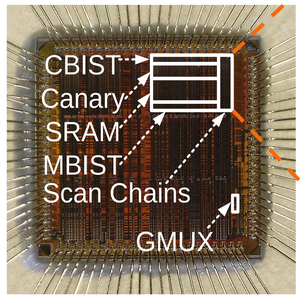
CHALLENGES

- Track SRAM V_{MIN} with variation in voltage, frequency, temperature (VFT) conditions.
- Avoid the cost associated with the design for the worst case methodology

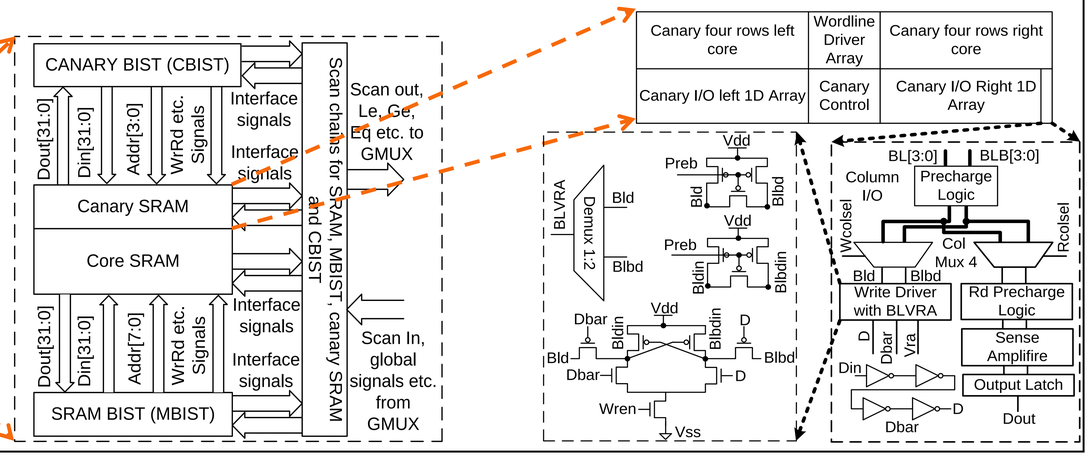
Block Diagram of the Test Chip

TESTCHIP SUB-BLOCKS

- A 8Kb SRAM
- A 512b canary SRAM
- An SRAM BIST (MBIST)
- A canary BIST (CBIST)
- Scan chains
- Global mux (GMUX)



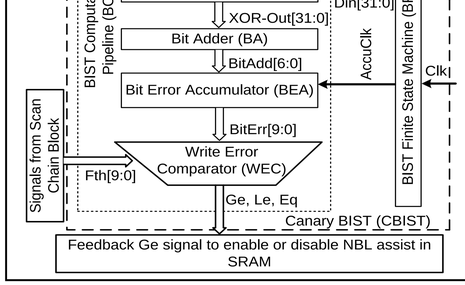
- This work showcases the first silicon results supporting that a canary SRAM can track SRAM dynamic write V_{MIN} using reverse assists



Inbuilt Testing Circuitry and Test Setup

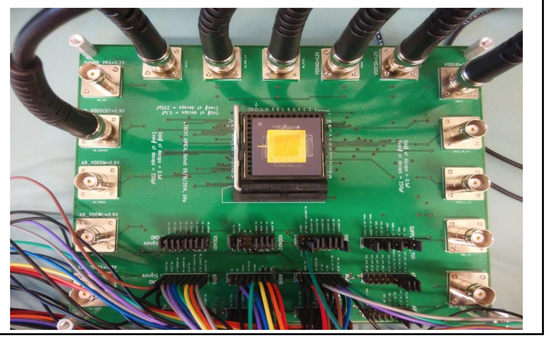
TESTING CIRCUITRY

- Built-in self-test for SRAM and canary to characterize the write failures with assists and reverse assists
- Scan chain loads a known word in the BIST to write it to the SRAM or canary SRAM, and reads back to compare and calculate the number of write failures



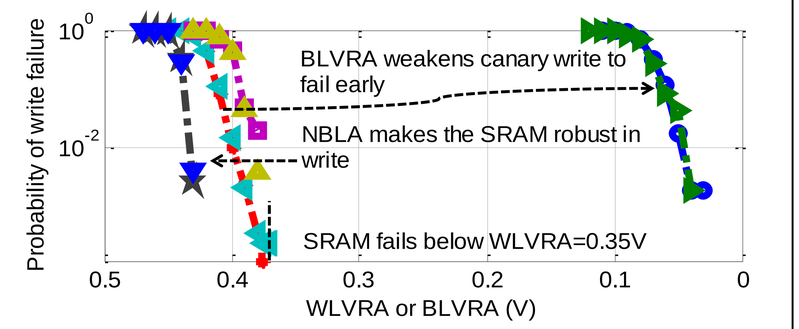
TEST SETUP

- Scan chain loads a known word to initialize the SRAM; then it loads the inverted word and writes and reads all words for comparison using the BIST
- We vary the BLVRA and WLVRA voltages and measure the write '0' and '1' failures using the SRAM BIST across VFT conditions



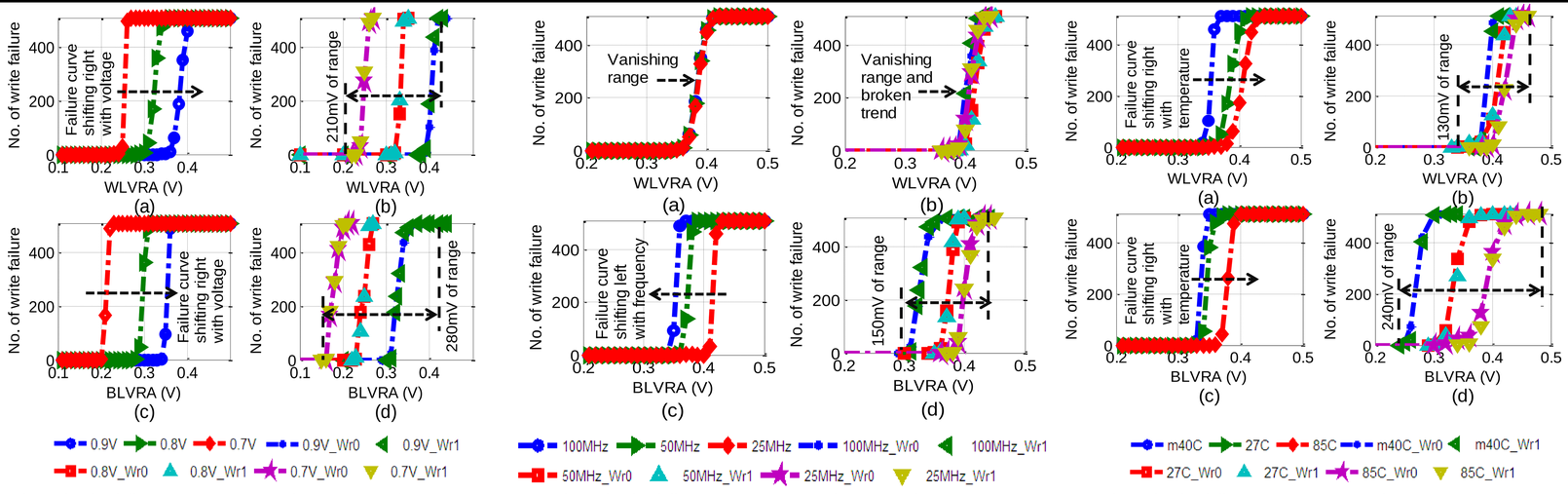
Results for Tracking SRAM Dynamic Write V_{MIN} using Canary SRAM with Reverse Assists

- With the same wordline type reverse write assist (WLVRA), SRAM and canary start failing near 0.4V WLVRA
- Adding bitline type reverse assist (BLVRA) fails the canary before the SRAM starts to fail
- Observing canary failures, we can turn on a negative bitline assist (NBL) in SRAM to make it more robust
- SRAM write V_{MIN} tracking depends on canary failure response with reverse assists across VFT conditions



Probability of write failure vs. WLVRA or BLVRA at 0.9V_24C_100MHz

Canary Failure Response with Reverse Assists across Voltage, Frequency and Temperature Variations



Number of write failures vs. reverse assists across voltage:
(a), (c) are simulated and (b) and (d) are measured (24C_100MHz)

Number of write failures vs. reverse assist across frequency:
(a), (c) are simulated and (b) and (d) are measured (0.9V_24C)

Number of write failures vs. reverse assist across temperature:
(a), (c) are simulated and (b) and (d) are measured (0.9V_100MHz)

Conclusion

- First silicon results showing that we can track SRAM write V_{MIN} using canaries and take a necessary action, such as turning on assist for the SRAM
- Canary SRAM failure rate varies with amount of reverse assist for BLVRA and WLVRA
- BLVRA can track VFT variations; however, WLVRA is limited to track voltage and temperature variations only
- Voltage type reverse assists, BLVRA and WLVRA have limitations in tuning range

Future Work

- Improving the tuning range of the reverse assist for the ease of tunability
- Circuit design of reverse assist for least overhead in SRAMs