A Flash-Based Non-Uniform Sampling ADC Enabling Digital Anti-Aliasing Filter in 65nm CMOS

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***Abstract* —This paper introduces a different class of ADC architecture that non-uniformly samples the analog input but generates uniform digital output. The proposed non-uniform sampling ADC utilizes 4-bit voltage quantizer and time quantizer with 10 ps accuracy. Combined with the proposed digital anti-aliasing filter, it improves SNR by nearly 30 dB in comparison with a conventional 4-bit uniform sampling ADC. Furthermore, the unwanted blocker signal can be attenuated within this non-uniform sampling ADC architecture without an analog anti-aliasing filter. As a proof of concept, the ADC prototype in 65nm CMOS measures EVM of -27 dB for a 16-QAM input signal under 50-dB higher blocker.**

***Index Terms* — Asynchronous processing, non-uniform sampling, ADC, alias free.**

I. Introduction

In contrast to conventional uniformly sampled ADCs, this proposed non-uniform sampling (NUS) ADC architecture enables new possibilities to a) move anti-aliasing (AA) filtering from analog to digital domain, and b) shift from conventional voltage quantization to a hybrid quantization paradigm where both voltage and time quantization are utilized. As a consequence, this NUS ADC architecture can a) significantly relax analog AA filter requirement, b) enhance achievable SNR as voltage quantization noise can be removed post non-uniform sampling, c) benefit from technology scaling with low supply voltage operation since the burden of fine voltage quantization is partially offloaded to time quantization, and d) lead to a highly flexible system as the computation in digital filter can be easily reconfigured. To prove the concept, a NUS ADC prototype in 65nm CMOS is implemented and achieves SNR of 55 dB (integrating over 20MHz bandwidth) with only 4-bit voltage quantizer. Together with the proposed digital AA filter, it measures EVM of -27 dB for a 16-QAM modulated signal under the presence of nearby 50-dB higher blocker without any analog AA filter.

II. Proposed ADC Concept and Architecture

Fig. 1 illustrates the high-level concept of the proposed NUS ADC architecture. Conventional ADCs utilize a uniform sampler followed by the voltage quantizer. Since the uniform sampling introduces spectral aliasing, an analog AA filter is typically required prior to the sampler in order to prevent any unwanted signal folded in band. For example, the spectral aliasing causes the voltage quantization noise to spread over the entire Nyquist band with a total power of $LSB^2/12$. The key idea of the proposed NUS ADC essentially reverses the sequence of conventional analog-to-digital conversion. The voltage quantization is performed first and hence generates non-uniform digital samples. One unique property of non-uniformly sampled signal is the absence of spectral aliasing, i.e. alias free [1-3]. Therefore, it preserves the analog spectrum and potentially allows AA filtering in the digital domain. A non-uniform DSP algorithm [3] is proposed to achieve digital anti-aliasing filtering and embedded interpolation functions. Finally, the uniform sampler is still applied at the very last stage and produces uniform digital samples in order to interface with synchronous digital processors. As a result, the unwanted blocker signal as well as voltage quantization noise can be attenuated internally, leading to improved SNR and dynamic range in comparison with conventional uniform-sampling ADCs.

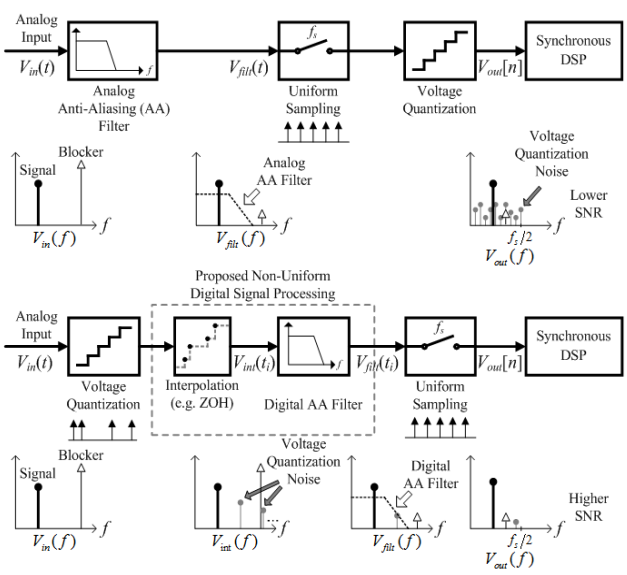

Fig. 1. The proposed non-uniform sampling ADC architecture (bottom) compared with conventional ADCs (top).

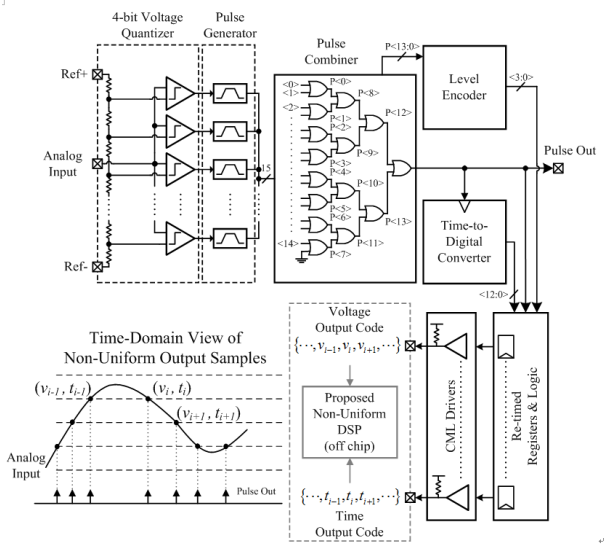

Fig. 2. Block diagram of the flash-based NUS ADC prototype.

Fig. 2 shows the block diagram of the proposed NUS ADC prototype. The analog input is continuously compared with the 4-bit voltage quantizer, i.e. 15 continuous-time comparators. Whenever the analog signal passes through a certain reference voltage level, a pulse is generated via the pulse generator. The pulses from all comparators are summed through a pulse combiner tree, and drive the time-to-digital converter (TDC) to record this pulse time instant, i.e. time quantization. Additionally, a level encoding logic utilizes the internal information of the pulse combiner and indicates which reference level is being crossed by the analog input, i.e. voltage quantization. Both voltage and time quantization codes are retimed and sent to external logic analyzer via CML output drivers. The proposed digital AA filter algorithm then utilizes both voltage and time codes to reconstruct the final output signal.

III. Circuit Implementation

The circuit implementation along the critical signal path is shown in Fig. 3. The continuous-time comparator is composed of 4-stage differential amplifiers with a total gain of > 40 dB. The multi-stage design helps reduce the kickbacks from the large output swing and provides enough gain. One key design constraint of the continuous-time comparator is to minimize its delay variation over input slew rates. In this work, we aim for delay variation less than 100 ps, which leads to > 500 MHz comparator bandwidth. The reference levels dependent delay variation is minimized by the nature of fully differential topology.

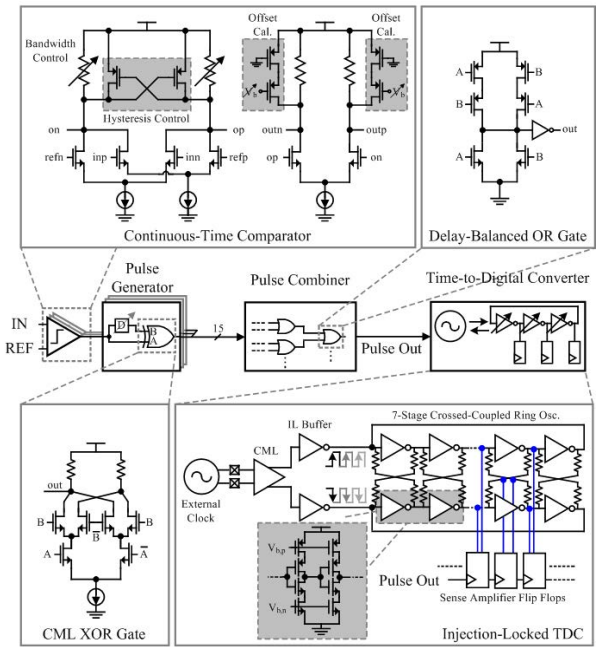

Fig. 3. Implementation of voltage and time quantization.

In addition, coarse offset calibration is implemented by 5-bit current DACs on chip and fine offset calibration is achieved digitally off chip. Tunable comparator bandwidth and hysteresis are included for characterization purpose. The pulse generator at comparator output is composed of a differential CML XOR gate and a differential delay cell to minimize the signal dependent delay variation. Since the propagation delay and rise/fall time must be balanced between the paths in the pulse combiner, a delay-balanced OR gate is exploited. Finally, the time quantization is done via an injection-locked TDC composed of 7-stage ring oscillator [4]. In conjunction with the passive phase interpolation, a time quantization step around 10 ps is achieved by injection locking to the external 4 GHz clock source.

IV. Digital Anti-Aliasing Filter

Fig. 4 illustrates the proposed digital AA filter algorithm enabled by the non-uniform sampling ADC architecture. We examine the case where the analog input is composed of the desired signal component (white triangle) and the band-limited noise (shaded box), and observe the output SNR. In the case of conventional digital FIR filter, the spectrum aliasing due to fixed tap delay causes noise folding. Instead, our proposed digital filter algorithm constructs a time-varying, signal-dependent FIR filter whose tap delay matches the time gap

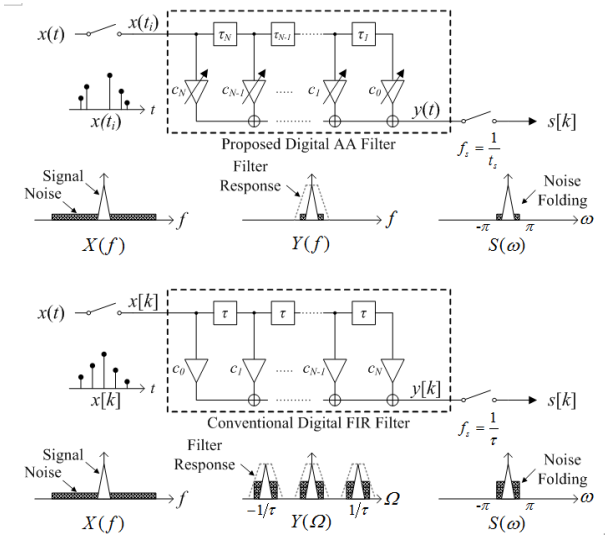

Fig. 4. Proposed digital AA filter algorithm.

of non-uniform samples. Since the proposed digital AA filter is able to remove any out-of-band components before final-stage uniform sampling, it can substantially relax the noise requirement of the quantizer, which is not possible in conventional uniform sampling ADCs. Furthermore, the tap coefficient is computed in real time by integrating the intended AA filter impulse response in between the adjacent time instants [3]. This mathematical expression of filtering operation essentially performs a continuous-time convolution; therefore, the filter response does not repeat at integer multiples of 2π, i.e. equivalent to an analog filter. Together with the alias-free property of asynchronous sampling, the output SNR matches that of an analog AA filter. Finally, the filter response can be easily reconfigured and implemented in ASIC or FPGA. For example, the pre-computed sine-integral function can be stored in memory for a low-pass filter response, and relax the real-time computation to only one adder. Moreover, the filter computation only occurs at the final-stage uniform sampling rate instead of first-stage non-uniform sampling rate, which further reduces the computation cost. Another advantage of the proposed AA filter scheme is the ease of reconfigurability in the digital domain, leading to a more flexible platform beyond conventional analog AA filter.

V. Measurement Results

The silicon prototype is packaged in 64-pin QFN and attached to PCB via a twist-lock socket. Fig. 5 shows the measurement results of single-tone input. The pulse output

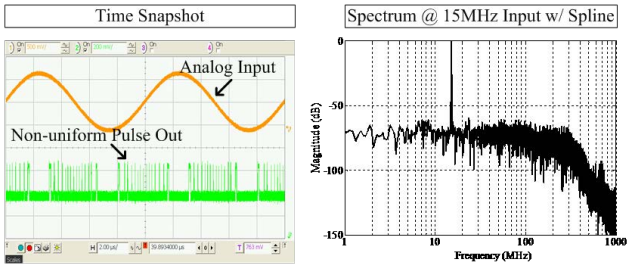

Fig. 5. Measured time domain waveform and reconstructed spectrum.

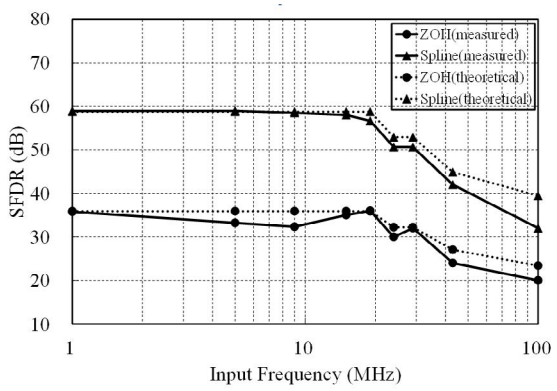

Fig. 6. Comparison between measured and theoretical SFDR.

from the non-uniform sampling ADC is recorded via a digital sampling oscilloscope and the pulse spacing is non-uniform as expected. The output spectrum before digital AA filter is reconstructed with both voltage and time output codes using spline interpolation. SFDR is reported in Fig. 6 with two representative interpolation methods, i.e. zero-order-hold (ZOH) and spline, which is 0.2 to 4 dB lower than ideal behavioral simulation. Note that, since the data acquisition throughput of external logic analyzer is limited, the input signal swing must be reduced when input frequency is beyond 20 MHz, causing SFDR degradation instead of being limited by the ADC itself. Therefore, the input frequency is measured up to 100 MHz with -8.5 dBFS. For the remaining measurements, we only apply ZOH in the digital AA filter due to its low computation cost. Since the total noise power scales linearly with the digital AA filter bandwidth, we calculate SNR with 20 MHz bandwidth around input frequency shown in Fig. 7 as a reference study.

Fig. 8 shows the output spectrum of two-tone test with low-pass and band-pass digital AA filter. Two tones are at 4 MHz and 5 MHz with -40 dBFS and -1 dBFS, respectively. The filter corner is at 4.05 MHz for the low-pass

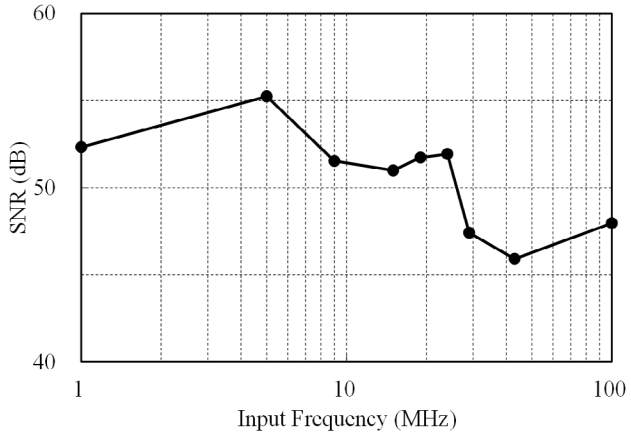

Fig. 7. Measured SNR over 20 MHz bandwidth using ZOH.

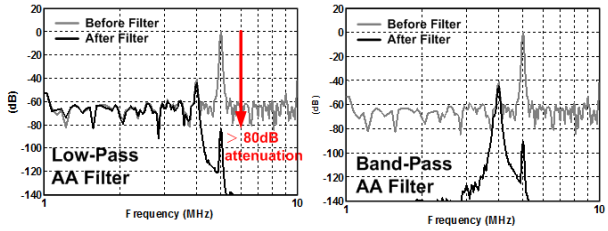

Fig. 8. Measured two-tone signal with proposed digital AA filter.

filter and 3.95 MHz / 4.05 MHz for the band-pass filter. The 5 MHz tone can be attenuated by more than 80 dB which would otherwise require more than 40th order analog Butterworth AA filter for conventional ADCs. In the modulated signal test, we inject -1 dBFS single-tone blocker at 15 MHz with a 50-dB lower 8 MHz 16-QAM signal. The EVM shown in Fig. 9 is evaluated at the final-stage uniform sampler output, which shows -27 dB thanks to the digital AA filter. The chip consumes an active area of 0.3 mm^2 and a total power of ~30 mW, while voltage and time quantizer consumes 17.5 and 4.8 mW, respectively. The power consumption can be further improved, as most building blocks were over-designed for prototyping purpose. The comparison with the state-of-the-art ADCs utilizing non-uniform samples is summarized in Table I and the chip micrograph is shown in Fig. 10.

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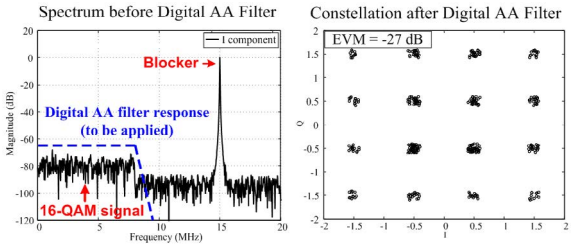

Fig. 9. Measured 16-QAM modulated signal.

TABLE I
COMPARISON WITH ADCS UTILIZING NON-UNIFORM SAMPLES

	Proposed NUS ADC	**[2]**	**[5]**
Alias-free Sampling	Yes	Yes	No
Post-sampling Filter	Yes	No	No
Synchronous Output	Yes	No	Yes
Time Quantization	Yes (~10 ps)	No	Yes (~ 500 ps)
Voltage Quantization	4-bit	8-bit	1-bit
Signal Bandwidth	20 MHz	35 KHz	300 KHz
SNR	54 dB	53 dB	49 dB
SFDR	35 dB(ZOH) 58 dB(spline)	47dB	58 dB

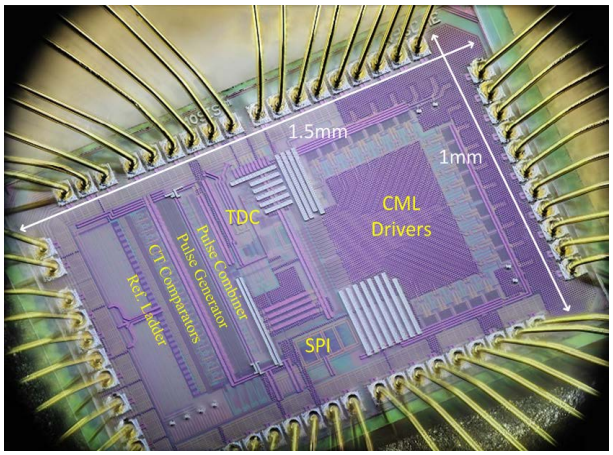

Fig. 10. Chip micrograph in 65nm CMOS.

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