A Dual-Band 802.11abgn/ac Transceiver with Integrated PA and T/R Switch in a Digital Noise Controlled SoC

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***Abstract*—This paper describes a dual-band 802.11abgn/ac compliant transceiver in a 4-in-1 combo connectivity SoC. It integrates the PAs, LNAs, T/R switches, and the 5GHz Balun. Due to the transmitter architecture and adaptive biasing scheme both are tailored for wide bandwidth, the 5GHz transmitter achieves 18.2dBm average output power for 802.11ac VHT80 MCS9 (Modulation and Coding Scheme 9). Within the 80MHz channel bandwidth, the IQ mismatch becomes frequency dependent, and is compensated through calibration. In the 2.4GHz transmitter, its PA load-line is adjustable. The power efficiency is thus remained similarly regardless the output power is at 20dBm for long range operation, or 8dBm for short range operation. By controlling the turn-on resistance of power island switch in digital baseband, and properly sizing the filler cap, the switching noise can be well controlled. The chip occupies 24.9mm^2 in 55nm 1P6M CMOS technology, where 1.3mm^2 is for 5GHz WLAN and 2.1mm^2 is for 2.4GHz WLAN/BT.**

***Index Terms*—WLAN, load-line, VHT80 (Very-High throughput 80MHz Bandwidth)**

I. INTRODUCTION

The increasing popularity of internet-connected mobile devices continues driving the demand to integrate multiple radios on a combo SoC to reduce cost, form factor and external BOM [1,2]. Besides, new connectivity wireless standards continue providing better quality of service: 802.11ac for higher throughput, Bluetooth 4.1 (BT/BLE) for reduced power consumption, high voice-quality in FM, and robust positioning service with world-band GNSS [3]. Particularly, WLAN is the key standards to enable new features and applications such as Wi-Fi hotspots, Miracast, Wi-Fi Direct, data collection in Big-Data mining [4].

Due to 2.4GHz ISM band is shared by WLAN, Bluetooth, Zigbee and more applications, it is difficult to improve throughput using this frequency band. The new 802.11ac standard operating in 5GHz band (FCC: 5.15GHZ to 5.925GHz [5]) is therefore proposed. It is less crowded, has more available channels, and has greater flexibility in channel bandwidth, and is backward compatible with the previous 802.11a. Utilizing a wider channel bandwidth and more advanced modulation scheme, the PHY data rate can reach up to 433Mbps in VHT80 MCS9. However, these new modulation schemes create stringent design challenges for the wireless system and radio transceiver.

In 802.11ac, the channel bandwidth is extended from 20MHz to 80MHz in Stage 1, and further to 160MHz in Stage 2. Such wide bandwidth introduced extra impairment factors for receiver signal-to-noise-ratio (SNR) and transmitter EVM. For example, Frequency Dependent IQ imbalance (FD-IQ) caused by the 3dB corner mismatch between the LPFs in the transceiver I/Q paths becomes worse at 80MHz and 160MHz [6]. This FD-IQ mismatch is not only due to the finite Gain-BW product of OP-Amp, but also the process gradient effect in deep sub-micron process. More advanced modulation scheme imposed new challenges to the transceiver as well: the 802.11ac TX EVM requirement is -32dB for 256QAM modulation MCS9, which is 4dB lower than 802.11n 64QAM; and the corresponding RX SNR requirement is also 6dB tighter. The DC offset in the direct-conversion receiver architecture needs to be further improved for meeting the EVM criteria for wide receiving power dynamic range. The synthesizer integrated phase noise would also need to be improved from 802.11a.

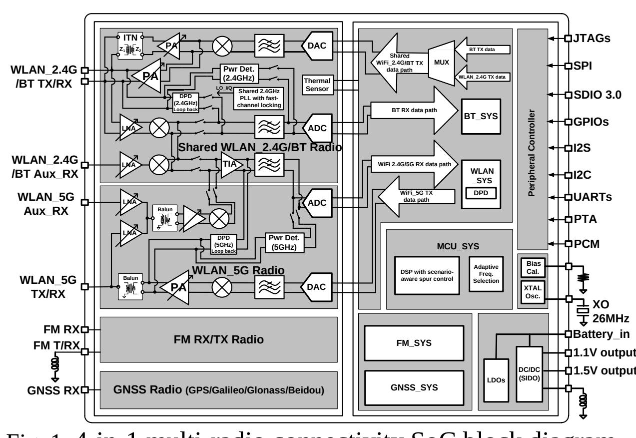


Fig. 1. 4-in-1 multi-radio connectivity SoC block diagram

The reported 802.11abgn/ac transceiver with integrated dual-band power amplifier and T/R switches in a 4-in-1 (802.11abgn/ac, BT4.1+HS, FM TRX, GNSS,) connectivity combo SoC is shown in Fig. 1. It adopts conventional direct-conversion receiver (DCR) and direct-conversion transmitter (DCT) architectures. Pseudo T/R switch, power amplifiers, power detectors, and 5GHz

Balun are integrated to offer 50Ω interface. Therefore there is no external BOM required for 5GHz band, allowing direct connection from chip to the antenna port. Auxiliary RX paths in dual-band WLAN are designed for receiver antenna diversity. The WLAN 2.4GHz transceiver can be reconfigured to become Bluetooth (BT) transceiver. In BT RX mode, it selects the path with complex BPF to become low-IF (LIF) topology for flicker noise consideration. In TX mode, a low-power PA (LP_PA) with impedance transformation network (ITN) is designed to be in parallel with full-power WLAN PA (Full_PA) by sharing the same I/Q modulator stage to deliver 13dBm BT power. This LP_PA can also deliver WLAN power at 7~10dBm for short range applications.

In the SoC environment, digital baseband operation generates digital switching noise which may potentially degrade receiver sensitivity, which becomes even more severe when receiving high-throughput modulation scheme. In this paper, a spur control mechanism which can be easily implemented in standard digital design flow is introduced to mitigate switching noise coupling.

Other key functional blocks in this combo chip includes a low phase noise synthesizer and its LO generation and distribution networks, an integrated power management unit (PMU) and a variety of host interfaces.

II. TRANSMITTER ARCHITECTURE

To meet the stringent EVM requirement of VHT80 MCS9, a broadband TX architecture is proposed as shown in Fig. 2. A pair of 10-bit TX DAC is designed to operate at 960MSps followed by a simple first-order passive RC filter. Comparing to the high-order LPFs in conventional TX architecture with DACs operating at relatively low clock frequency, the broadband TX architecture mitigates the FD-IQ mismatch and eliminate the need of the more complex FD-IQ compensation. A simple 1st order RC LPF is designed after DAC to filter out the DAC image spectrum by setting the 3dB corner frequency to be around 100MHz. Gain control is provided in the low pass filter by tuning the R ratio with 2dB per step to achieve the gain range from +2dB to -6dB to optimize the TX link budget. After I/Q baseband signal, the current of the Gm stage passes through the LO I/Q switches and up-converts the baseband signal to the desired frequency band. The 6dB per step programmable gain function is merged by cascode devices over the switches.

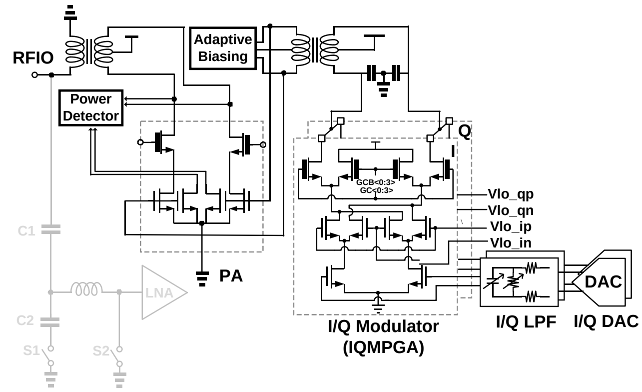


Fig. 2. Broadband TX architecture in 5GHz

Because the 2.4GHz band also will be used by low power applications such as IoT and wearable devices, which does not require the PA to operate at the same output power level, a load-line adjustable PA is proposed. It allows the PA to have similar power efficiency when operating with reduced output power. In 2.4GHz band, the Tx IQ modulator delivers the RF current into the multi-winding transformer, whose output drives PA branches in different PA modes as shown in Fig. 3. The output of the PA branches are connected to a transformer, which is an Impedance Transformation Network (ITN) to optimize both the linearity and the current consumption when PA operates in wide power range in the modes of full PA (Full_PA) or low power (LP_PA) [7]. The turn ratio of 4:4 and 4:2 are set for the multi-winding transformer in Full_PA and LP_PA, respectively. To increase the PA output impedance for reducing the LP_PA mode current consumption, the ITN is designed with a transformer in series with a cap. In LP_PA mode, the drain current flows through the tunable ITN, which changes the PA load-line to higher impedance (~200 Ω) for better efficiency for 5-10dBm output power level. The differential outputs of ITN are differentially connected to the open-drain output of Full to deliver the PA current into the final Balun. The LP_PA mode is also shared to BT system to act as the BT PA for delivering 13dBm power to keep similar power efficiency like in standalone BT chip.

To deliver 23dBm WLAN CCK power and other high OFDM power, the output Balun provides the impedance transformation from 50Ω to 35Ω in Full_PA mode. Moreover, parts of PA branches are selectively turned off to further optimize power consumption in the power range between Full and LP_PA modes.

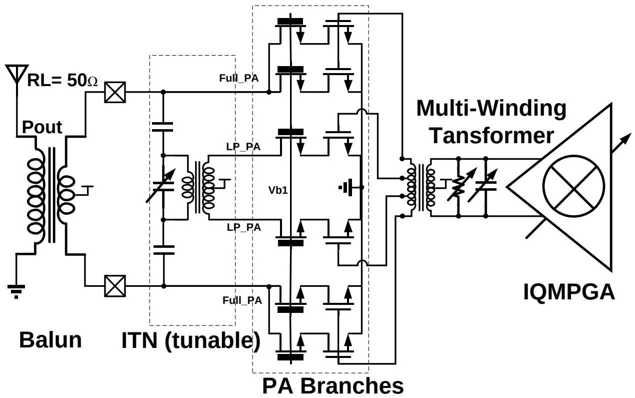


Fig. 3. PA architecture with load-line adjustment in 2.4GHz TX

In the WLAN transmitter chain, the power amplifier nonlinearity usually will dominate the EVM performance in high output power range. Due to the increased channel bandwidth for higher data rate, the memory effect in PA design can become another factor deteriorating EVM. The PA memory effect comes from time-variant transfer function caused by the frequency-dependent biasing and matching network [8]. If memory effect exists, the two-tone test will be worse in IM3 when the tone spacing increases. Therefore, for increased channel bandwidth, previously acceptable memory effect may become harmful.

In this work, class-AB PAs are chosen for high linearity and efficiency for both 2.4GHz and 5GHz bands. One key contributor to PA memory effect is its biasing circuit. To mitigate memory effect, this circuit needs to adaptively track the instantaneous peak amplitude of the PA input signal to boost the PA biasing voltage for improving the PA linearity. This is particularly important for OFDM signals which has a high value of peak-to-average ratio (PAPR). To adjust PA bias timely, the bandwidth of the adaptive biasing tracking circuit needs to be approximately several times the channel BW. In the conventional PA design, the PA is biased through a large bias resistor with AC-coupled to the driving stage of PGA or I/Q modulator as shown Fig. 4(a). The large bias resistor and PA input parasitic capacitor form a RC-LPF and limit the BW of tracking bias signal significantly. In this design of Fig. 4(b), the adaptive tracking bias is connecting to the central-tap of the transformer secondary coil of IQMPGA load to directly bias the PA branches without tracking bias BW limitation to reduce the PA memory effect.

With the help of wide-bandwidth adaptive tracking biasing technique, the system analysis shows that a simple time-invariant Digital Pre-Distortion (DPD) algorithm is sufficient improve EVM at high output power range when PA's AM-to-AM conversion and AM-to-PM conversion started dominating EVM performance. The loop-back path is connected to the differential PA outputs via a tunable attenuator to cover a wide output power range to allow for the detection for pre-distortion.

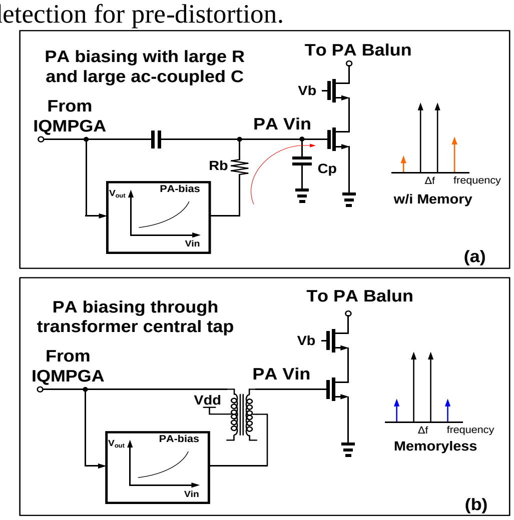


Fig. 4. PA biasing technique (a) with large R and large ac-couple C, (b) through transformer central tap.

To precisely control the dual-band PA output power, dual-band power detectors are designed to achieve the TX per-packet power control. Comparing to the narrow spectrum (~80MHz) in 2.4GHz band, the wide bandwidth (~1GHz), available at 5GHz presents great challenges on power detector design. The function of conventional power detector is to perform the $I_{out}*V_{out}$ using a multiplier, where V_{out} is from PA output and I_{out} is generated usually from a PA replica. Considering the layout induced parasitic effects and process corner variations, additional introduced phase delay, ψ_{par}, can affect the power detector accuracy over the entire 5GHz band. Fig. 5 shows the block diagram of the proposed power detector with the phase compensation control loop. The insertion of additional phase φ from a tunable phase rotator can effectively compensate for the parasitic phase delay to reduce the power detector sensitivity to VSWR over the whole frequency band [7]. The power detector provided 12 adjustable phases within the whole 2π circle. Which phase will be selected will be determined by phase selection algorithm, and with interpolation, +/- 1dB detection accuracy over whole 5GHz frequency band under VSWR=2:1 is achieved.

III. RECEIVER AND T/R SWITCH

Pseudo T/R switches are integrated to co-design with LNAs and PAs for both bands. In 2.4GHz, external Balun is used to achieve better power efficiency for TX and less insertion loss for RX in narrow band of 80MHz. However, at 5GHz band, less choice of external Balun is available which could cover the entire frequency range of 5150MHz~5925MHz. Besides, the external matching network is more sensitive at 5GHz than at 2.4GHz, making the difficulty of maintaining stable performance over whole frequency band at mass-production stage. Therefore, the proposed architecture of integrating PA, LNA and T/R switch is shown in Fig. 6 to achieve the 50ohm output for whole frequency range, allowing direct connection from the chip to the antenna without any external matching components.

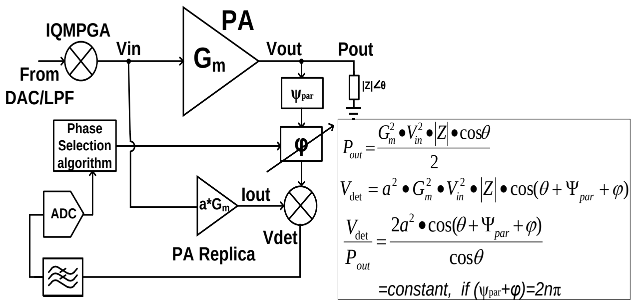


Fig. 5. Phase compensated power detector in 5GHz band

The 5GHz virtual T/R switch is composed of C_1, C_2, S_1, S_2, L_1 and C_{in}. In RX mode, two switches S_1 and S_2 are open with the series AC coupled capacitor C_1 and series RX matching inductor L_1. The C_{in} can be properly tuned to form the LC tank with PA Balun and LNA parasitic cap, peaking at the desired operation frequency for achieving highest RX gain and lowest noise figure (NF). Because the RX path is connected from single-ended port of PA Balun, the Balun induced RX loss is around 1dB lower than the case of connecting from the differential ports, where additional magnetic coupling loss caused more RX gain and NF loss. In the TX mode, two switches S_1 and S_2 are connected to ground, where the C_2/C_1 ratio is chosen to be 10 for 20dB attenuation at node N1, and switch S_2 provide extra 5dB attenuation to protect the LNA input Gm for device reliability.

For achieving low NF requirement and wide-band impedance matching in the 5GHz RX path, a single-ended LNA architecture with resistor shunt-shunt feedback is chosen to provide the real part for matching and low noise characteristic over ~1GHz frequency range. A transformer load of LNA converts single-ended signal to differential signals for driving the next mixer stages, which are composed of the gm stages and I/Q passive mixers. The separated complementary P/NMOS inverter-type Gm stages are designed with current re-use to boost the trans-conductance to drive the passive mixer I/Q switching stages for eliminating the IQ cross-talk issue. The down-converted I/Q current signals enters the trans-impedance amplifier (TIA) to become the voltage mode signals. The strong out-of-band blockers can be firstly filtered out by 1st order LPF at TIA stage by setting the RC corner at ~ 2X the signal BW, without suffering the FD-IQ mismatch effect.

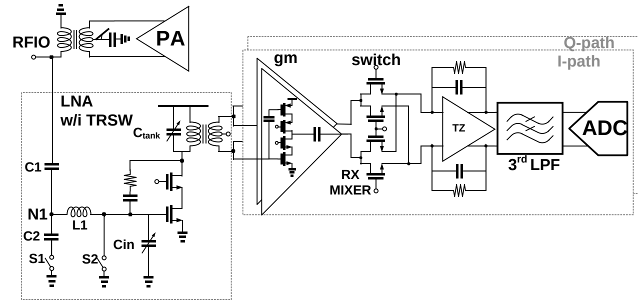


Fig. 6. 5GHz RX chain with T/R switch and Balun

A 3rd order Chebyshev low-pass filter is placed after the trans-impedance amplifier (TIA) for adjacent and alternative-adjacent channel rejection, as shown in Fig. 7. As the channel bandwidth increases, the device mismatch induced OP Gain-BW product variation will increase to cause the FD-IQ mismatch. The mismatch usually will be significant near the filter corner frequency. Therefore, FD-IQ calibration is required to keep the image-rejection ratio (IRR) to be low enough in the entire 80MHz of VHT80 MCS9. The DC offset can also be compensated by injecting the IDAC current into the input of LPF to minimize the residue DC offset of LPF output to be less than 50mV. During the packet receiving, the IDAC compensation current will be dynamically controlled by the digital baseband to adjust the DC offset for obtaining best receiving SNR signal quality.

For better out-of-band blocker management, the RSSI (receiving signal strength index) circuit is designed to monitor the wide-band blocker power level. Combined with the in-band signal power level detection through LPF, the RX AGC can be properly set by digital baseband to control the LNA gain mode and analog baseband gain at LPF to avoid voltage saturation happened at circuit internal node under blocker test.

The conventional IQ calibration method with single tone test is insufficient to effectively compensate the FD-IQ mismatch at wide bandwidth LPF. Therefore, a new RX FD-IQ calibration has been developed as shown in Fig. 8. Two different calibration signals are sent by TX baseband, which are consisting of multi-tone signals with frequencies above and below the LO signal sequentially back to the RX. By observing the received loop-backed signals, the frequency domain IQ imbalance compensation coefficients of each tone are measured by calculating the magnitude and phase of their corresponding image tones.

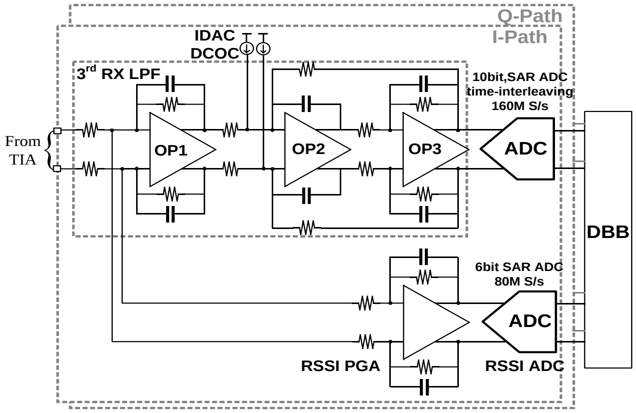


Fig. 7. Analog baseband circuit in RX chain

Then, the time-domain coefficients of the FIR filter are obtained by the transferred function from the frequency domain compensation coefficients. After the compensation, the RMS image rejection ratio (IRR) could be lower than -45dBc, which minimizes the FD-IQ imbalance effect to a negligible level [6].

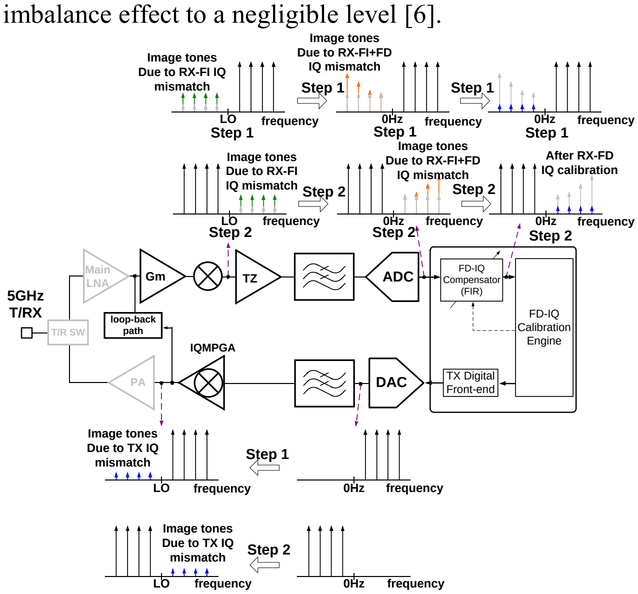


Fig. 8. RX-FD IQ calibration block diagram

IV. LOW-PHASE NOISE SYNTHESIZER AND LO GENERATION

To achieve the stringent RX and TX EVM requirement in VHT80, 256QAM, MCS9 operation, the integrated SX phase noise needs to be less than 0.4 degree from system analysis to achieve overall EVM performance better than -32dB. Fig. 9 shows the synthesizer block diagram and the LO generator circuit blocks.

The reference clock of 26MHz is chosen to share with the mobile phone platform. To reduce the phase noise contribution from reference clock, a frequency doubling circuit (DBL) is designed with duty-cycle calibration to convert the reference clock to 52MHz for entering PFD to compare with the feedback clock frequency and phase of Multi-Modulus divider (MMD) [9]. The VCO is operating in the frequency range of 7.84GHz~9.4GHz for the following LO generator stage to synthesize the frequency of 9.8GHz~11.85GHz by double side-band mixer (DSB). To maintain the LO signal quality, the 4-bit cap tuning is designed for tracking the LC tank of DSB and repeater (REP) to cover the whole frequency range. Next, the divided by two (DIV2) circuits are applied to create I/Q LO signals for RX and TX separately, whose layout are located near the RX mixer and TX modulator to shorten the length of LO trace, reducing the I/Q mismatch. Due to the LO generator architecture, the VCO frequency is not located at the harmonics of PA operating frequency. Therefore, the SX and VCO performance still keeps unchanged even the PA is operating at very high output power level as 20dBm OFDM modulation.

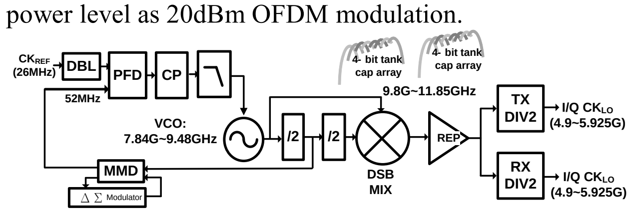


Fig. 9. SX block diagram with LO generator

V. COUPLING AND DE-SENSITIZATION IN SOC

There are many inductors being deployed in this reported 4-in-1 combo SoC. For the magnetic coupling among these inductors, and the digital switching noise coupling to sensitive victims such as VCOs or LNAs, it needs to be carefully considered. To mitigate mutual magnetic coupling among inductors, quadrupole inductor layout topology is adopted in VCOs [10]. As shown in Fig. 10, assuming the distance S_1 an S_2 are sufficiently larger than r1 and r3, the mutual coupling to VCO inductor can be mitigated.

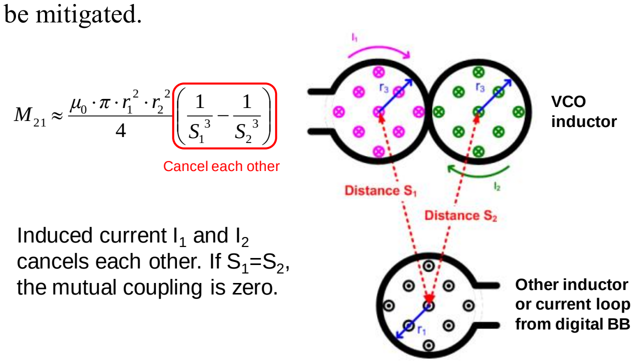


Fig. 10. Quadrupole layout for VCO inductor

Regarding digital switching noise reduction, one technique is to apply frequency hopping for the channels having degraded sensitivity [2]. However, when more wireless systems are in operation simultaneously, the determination algorithm becomes more complicated, and there may not be a suitable frequency to be hopped to. Alternatively, in this paper, scenario-aware spurious tone control is proposed, as shown in Fig. 11. In digital baseband design, MTCMOS technique is commonly used to help effectively control the digital blocks in different power island for saving current consumption by controlling the power switch on top of the digital circuit blocks. In standard digital circuit implementation flow, adding filler caps inside the digital circuits is an effective method to solve the IR drop issue during dynamic digital operation. From RX desense perspective, once the high-frequency digital spurious tone are generated by high-speed switching devices, then it is easy for these spurious tones to leak out to the package or PCB and then coupled to the RX input resulting in sensitivity degradation. Therefore, by proper arrangement for filler cap density and power switch number, an equivalent current-mode RC filter can be formed to localize the high-frequency spurious signals near the digital circuit itself; where the resistance R comes from the parasitic resistance of power switches, and the capacitance C is from filler cap. The effective RC corner is located at around 300MHz, which provides approximately 18dB and 25dB of attenuation at 2.4GHz and 5.5GHz, respectively.

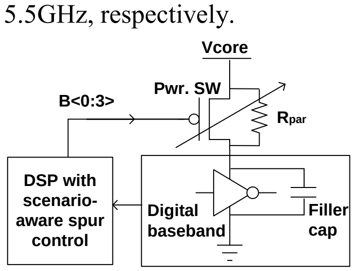


Fig. 11. Scenario-aware spurious tone control for digital baseband

VI. MEASUREMENT RESULTS

Fig. 12 shows the integrated SX phase noise for 802.11ac application to be lower than 0.4 degree, covering the frequency range from 4.9GHz to 5.9GHz. Lower in-band phase noise is due to the less noise contribution from reference clock and charge pump by the nature of lower feedback divider umber in the phase-lock loop.

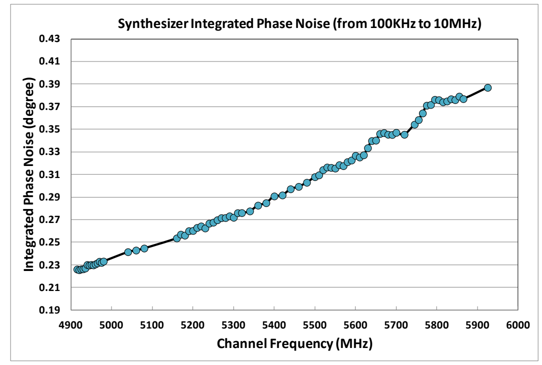


Fig. 12. SX integrated phase noise for 802.11ac

In 2.4GHz band, the TX performance is measured for two PA operation modes with on-chip reconfiguration for load-line adjustment as shown in Fig. 13. The current consumption can be around 100mA saved from changing Full_PA mode to LP_PA mode at 8dBm for short range operation in Fig. 14(a), while the PA efficiency is much improved from 1.8% to 10% in Fig. 14(b). Under same EVM criteria of -25dB from Fig. 14(c), the PA efficiency of LP_PA mode is worse than the Full_PA efficiency of 18% due to implementation loss.

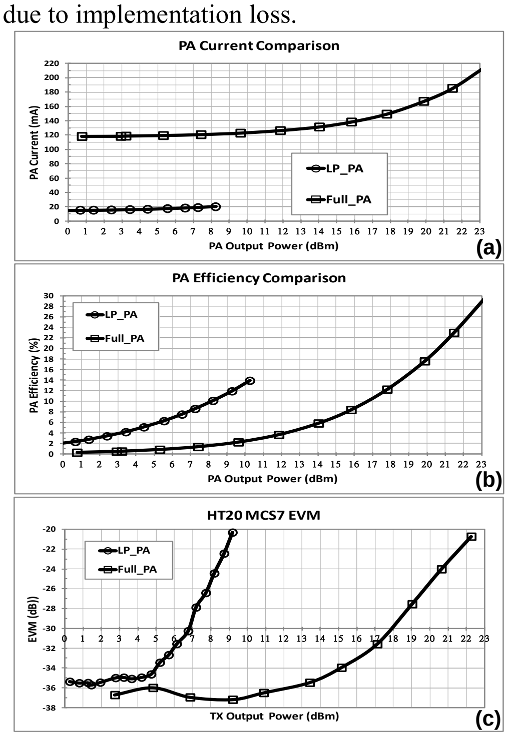
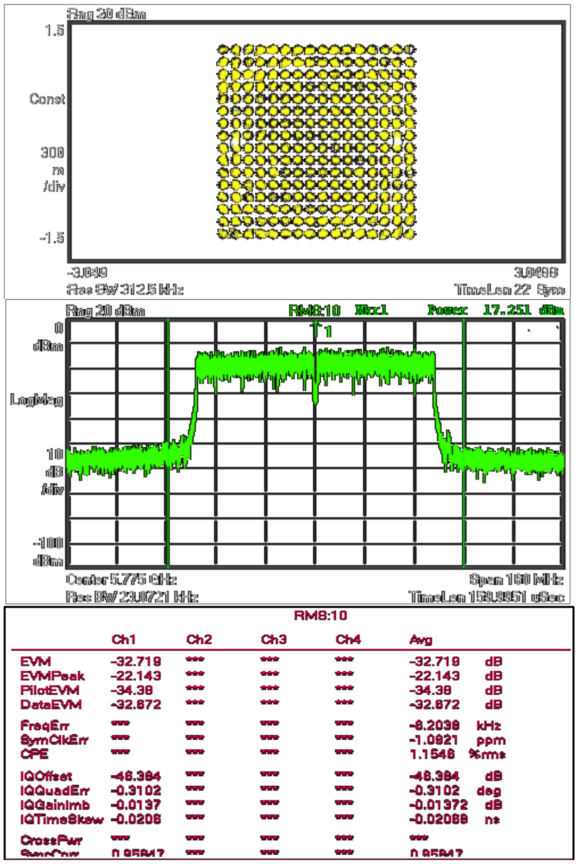


Fig. 13. 2.4GHz TX performance comparison in Full_PA and LP_PA modes (a) PA current consumption, (b) PA efficiency, and (c) HT20 MCS7 EVM

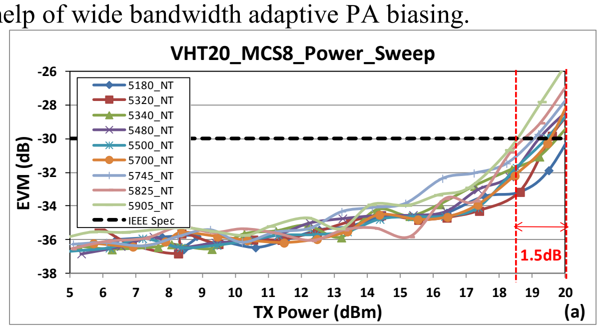
The performance due to the choice of wide BW transmitter architecture, improving bandwidth of PA adaptive bias, and applying the digital pre-distortion, is shown in Fig. 14, for high frequency channel of 5.775GHz 802.11ac Stage 1 VHT80 256QAM. The transmitter could output 17.2dBm while meeting the IEEE EVM spec. of -32dB.



	Ch1	Ch2	Ch3	Ch4	Avg	
EVM	-32.719	***	***	***	-32.719	dB
EVMPeak	-22.143	***	***	***	-22.143	dB
PilotEVM	-34.38	***	***	***	-34.38	dB
DataEVM	-32.672	***	***	***	-32.672	dB
FreqErr	***	***	***	***	-6.2038	kHz
SymClkErr	***	***	***	***	-1.0921	ppm
CPE	***	***	***	***	1.1546	%rms
IQOffset	-46.384	***	***	***	-46.384	dB
IQQuadErr	-0.3102	***	***	***	-0.3102	deg
IQGainImb	-0.0137	***	***	***	-0.01372	dB
IQTimeSkew	-0.0206	***	***	***	-0.02068	ns
CrossPwr	***	***	***	***	***	

Fig. 14. TX output performance of 802.11ac

The 802.11ac TX EVM vs. output power curve is measured in Fig. 15 for (a) VHT20 MCS8 and (b) VHT80 MCS9 in whole frequency range. The achieved power level between lowest and highest channel has the gap of 1.5dB due to degraded SX phase noise at higher frequency. The gap is similar for VHT80 MCS9 and VHT20 MCS8 means the memory effect in PA is not obvious with the help of wide bandwidth adaptive PA biasing.



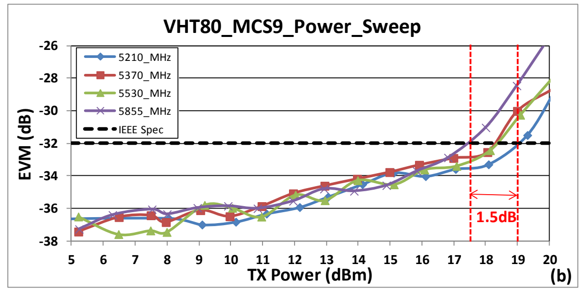


Fig. 15. 802.11ac TX EVM measurement (a) VHT20 MCS8 (b) VHT80 MCS9

Fig. 16 shows the measured 5GHz receiver sensitivity with and without the implementation of digital scenario-aware spur control algorithm, where the testing conditions are (a) VHT20 MCS8 and (b) VHT80 MCS9. It can be observed that the receiving sensitivity can be much improved to align to base-line performance with the proposed algorithm, where 5.5dB and 8.5dB improvement can be achieved for VHT20 MCS8 and VHT80 MCS9, respectively. The worse sensitivity degradation by the spurious tone at VHT80 MCS9 is due to the more digital switching noise by higher digital activities, while the harmonics of 832MHz baseband operation plays the major role.

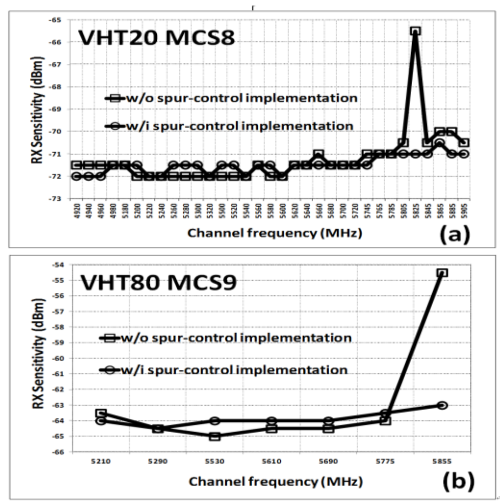


Fig. 16. 5GHz sensitivity measurement before and after spur-control implementation (a) VHT20 MCS8 (b) VHT80 MCS9

The die size of combo SoC is 24.9mm^2 in 1P6M 55nm CMOS technology and its die micrograph is shown in Fig. 17, while the 2.4GHz and 5GHz WLAN RF transceivers occupies 2.1 mm^2 and 1.3 mm^2, respectively. The WLCSP package with 0.25mm bump size and 0.4mm bump pitch is used for chip-on board application. The performance benchmark for performance comparison with previous published work is summarized in Table I.

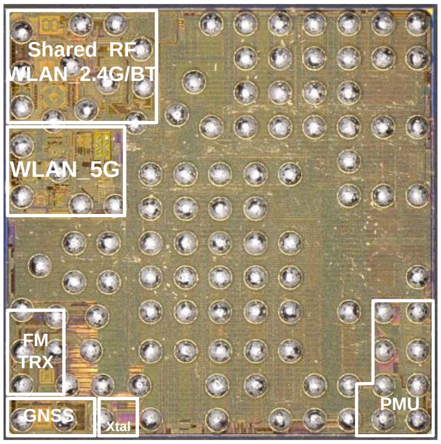


Fig. 17. Die photo with the bump size and pitch are 250um and 400um, respectively.

VII. CONCLUSIONS

Various innovations had been presented in this paper to address wide-bandwidth / high-throughput, low power, and spur / coupling control and mitigation. For wide-bandwidth, the transmitter architecture, PA bias scheme, frequency-dependent IQ imbalance remedies had been proposed. An adjustable load-line PA is introduced for short-range, low power applications such as wearable devices. Finally, the scenario-aware spurious control algorithm is introduced for the SoC environment. The reported RF transceiver is the smallest in area comparing to recent publications, while using a less advanced process node.

ACKNOWLEDGEMENT

The authors would like to thank various Mediatek teams RF, WCN, DT and CSD divisions.

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TABLE I
PERFORMANCE SUMMARY

		This work	ISSCC 2013 [11]	ISSCC 2014 [12]
Support WLAN standards		1X1 11bgn +1X1 11a	2X2 11bgn +1X1 11a	4X4MIMO 11abgn/ac
Integrate PA,T/R SW, Balun	2.4GHz 5GHz	Yes/Yes/No Yes/Yes/Yes	Yes/Yes/Yes Yes/No/Yes	No/No/No No/No/No
Support BW(MHz)	2.4GHz 5GHz	20/40 20/40/80	20/40 20/40	20/40 20/40/80
Int. LO PN (deg.)	2.4GHz 5GHz	0.3 0.37	N/A 0.42	0.19 0.37
Chip-in RX NF (dB)	2.4GHz 5GHz	4.2 (w/i SW) 4.7 (w/i SW)	4.2 (w/i SW) 4.2 (w/o SW)	3.0 (w/o SW) 4.3 (w/o SW)
Aux port RX NF (dB) for RX diversity	2.4GHz 5GHz	3.0 3.7	No support No support	No support No support
Chip-in RX sensitivity (dBm)	2.4GHz,LG54M 5GHz,LG54M 5GHz,VHT80MCS9	-77.5 -77 -63.5	-78 -78 N/A	N/A N/A N/A
TX Psat(dBm)	2.4GHz(Full_PA) 2.4GHz(LP_PA) 5GHz	28 (w/i SW) 17 (w/i SW) 26.5(w/i SW)	29 (w/i SW) No support 26 (w/o SW)	N/A No support 4 (w/o SW)
TX Pout(dBm)	2.4GHz,LG54M 5GHz,LG54M 5GHz,VHT80MCS9	20.5 18.5 18.2	20.5 17.3 N/A	-5 N/A -5
RF Power Consumpt.	RX 2.4GHz TX 2.4GHz	84mW (HT40,1SS) 705mW @20.5dBm (HT40,1SS)	101mW (HT40,2SS) 111mW(*1) (HT40,1SS)	1170mW(*2) (HT40,3SS) 1080mW(*2) (HT40,3SS)
	RX 5GHz TX 5GHz	156mW (VHT80,1SS) 996mW @18.5dBm (HT40,2SS)	105mW (HT40,2SS) 123mW(*1) (HT40,1SS)	2080mW(*2) (VHT80,3SS) 1520mW(*2) @-5dBm (VHT80,3SS)
Technology		55 nm	45nm	40nm
RF Die Area(mm^2)		3.4 (*3)	3.8	21.5

(*1) Power Consumption excluding PA & Driver
(*2) SoC Power Consumption in [12]
(*3) Including BT RF area