An Electrical and Optical Concurrent Design Methodology for Enlarging Jitter Margin of 25.8-Gb/s Optical Interconnects

Takashi Takemoto, Hiroki Yamashita, Yasunobu Matsuoka, Yong Lee, and Masaru Kokubo

Hitachi, Ltd., Research & Development Group, Center for Technology Innovation – Electronics,
1-280 Higashi-Koigakubo, Kokubunji, Tokyo, 185-8601, Japan
Tel: +81-42-323-1111, E-mail: takashi.takemoto.tj@hitachi.com

***Abstract* — An electrical and optical concurrent design methodology for enlarging the jitter margin of 25.8-Gb/s optical interconnects is proposed and evaluated. As the key for establishing this design methodology, a simple method for modeling characteristics of a laser diode (LD) (hereafter, "LD modeling method") is adopted. The LD modeling method calculates an optical eye diagram on the basis of measured rising/falling step responses, and the calculated eye diagram agrees well the measured one; namely, the jitter error between them is less than 1.6 ps. Error-free 25.8-Gb/s optical transmission between FPGAs was experimentally demonstrated by optimizing equalization gain of the FPGAs on the basis of the developed design methodology. Moreover, random jitter (RJ) due to relative intensity noise of a LD was reduced by 20% by shortening the transition time of an optical transmitter (TX).**

***Index Terms* — Optical interconnect, LD modeling method, deterministic jitter, random jitter, and relative intensity noise**

I. Introduction

Recent growth of network services, such as high-quality photo and video sharing and social networking, demands a rapid increase in the total throughput of information and communication technology (ICT) systems. To meet these increasing throughput requirements, 25.8-Gb/s short-reach communications (such as intra- and inter-rack transmissions) are required. Optical interconnects using multi-mode fiber (MMF) can provide low-power 25.8-Gb/s-class short-reach communications because of their negligible transmission loss and signal reflections [1, 2]. However, it is difficult to design optical interconnects because, as data rate increases, intrinsic noise and non-linear effects of laser diodes (LDs) significantly reduce the jitter margin. It is therefore necessary to establish an electrical and optical concurrent design methodology that maximizes the jitter margin by considering electrical and optical transmission systems as one. To establish that design methodology, a method for modeling the characteristics of a LD is proposed in the present study. This method can calculate optical eye diagrams with high accuracy by simply measuring step responses of a fully-modularized optical transmitter (TX). As an example of considering optical interconnects inside ICT systems, a 25.8-Gb/s optical transmission between FPGAs was experimentally evaluated. In the experimental evaluation, equalization gain of the FPGA was optimized by using the developed design methodology, and 25.8-Gb/s optical error-free transmission demonstrated.

II. Challenges for designing optical interconnects

The structure of the evaluation board fabricated for the transmission experiment is shown in Figure 1. On the board, TX and receiver (RX) electrical interfaces (I/Fs) (consisting of FPGAs) are connected through an optical link, which is mainly composed of an optical TX and RX, optical connectors, and MMFs. The circuit blocks inside the optical TX and RX, namely, an LD driver (LDD) and a transimpedance amplifier (TIA), are all-analog circuits, and a VCSEL (operating at 850-nm wavelength) is used as an optical source. To develop the 25.8-Gb/s optical link, two challenges, namely, loss and jitter budgets, must be tackled. The loss budget is mainly determined by three components: (i) a TX penalty due to relative intensity noise (RIN) of a LD, (ii) losses at optical couplings and connectors, and (iii) TIA sensitivity. Designing the loss budget is fairly simple because it is only necessary to manage optical losses for meeting targeted TIA sensitivity. Moreover, TIA sensitivity can be improved by applying circuit techniques to suppress power-supply noise and offset voltage [3]. As for the jitter budget which consists of two kinds of jitter, namely, deterministic jitter (DJ) and random jitter (RJ), three components must be addressed: (i) inter-symbol interference (ISI) due to nonlinearity and lack of bandwidth of a LD, (ii) chromatic dispersion at a MMF, and (iii) RIN of a LD. In the case of short-reach communication i.e., transmission length less than 100 m, the effects of dispersion are negligible [4].

DJ of the electrical I/Fs can be accurately estimated by modeling the characteristics of the input/output circuits of the FPGAs and those of the transmission lines on the basis of measured S-parameters. As for the optical link, the rate equation is conventionally used for calculating DJ of LDs because it can represent non-linear effects due to variable LD bandwidth [5]. As shown in Fig. 2(a), the rate equation can reproduce the frequency responses of a

VCSEL at various current levels by tuning the parameters of the rate equation. The calculated 25-Gb/s eye diagram is shown in Figure 2(b). It was obtained by incorporating the rate-equation-based VCSEL characteristics and the characteristics of the LDD and transmission lines on the basis of measured S-parameters. The calculated eye diagram agrees well with measured one (see Fig. 2(c)), which indicates jitter error of less than 1.3 ps. However, in the case of a fully modularized optical TX such as commercial optical modules, it is difficult to obtain refined rate-equation parameters because each component such as the LDD and LD cannot be evaluated individually.

In this study, as an alternative to the conventional method based on the rate equation, a simple method for modeling LD characteristics for a fully modulated optical TX, which is based on measured rising/falling step responses, is proposed. The proposed method represents a 25.8-Gb/s optical eye diagram with a small difference in jitter (less than 1.6 ps) in comparison with that of the corresponding measured eye diagram. On the other hand, as data transmission rate increases, in addition to DJ, RJ due to RIN of a LD also reduces the jitter margin significantly. By using the gain equalization of the FPGA, it was therefore possible to experimentally demonstrate the effect of reducing RJ.

III. MODELING AND EVALUATION RESULTS

A. LD-modeling method and 25.8-Gb/s-optical-transmission experiment

The methods for modeling and evaluating DJ of the fully modularized optical TX are explained as follows. The frequency responses of directly modulated LDs (such as a VCSEL and a DFB-LD) are varied according to the magnitude of an input current. As a result, the LDs exhibit two characteristic non-linearity effects: a ringing waveform and asymmetric rising and falling edges. Therefore, convolution of impulse responses (based on S-parameter), which is widely used for calculating waveforms, cannot represent DJ of the LDs because of the non-linearity effects. To solve this issue, a method for modeling DJ of LDs, which calculates the optical waveforms for an arbitrary data pattern on the basis of measured rising/falling step responses of the optical TX, is proposed as follows. Firstly, to represent the asymmetric rising and falling edges, both rising and falling step responses are generated from an output waveform of the optical TX with an n-bits sequence pattern (see Fig. 3(a)). Next, the eye diagram is calculated by superposing the measured rising/falling responses in relation to the timings of the data transition for the targeted data pattern (see Fig. 3(b)). To represent a ringing waveform, the bit number, *n*, is determined by using the time that the step response settles to a final high- and low- level of optical power after ringing occurs. In the transmission experiment, a 16-bit

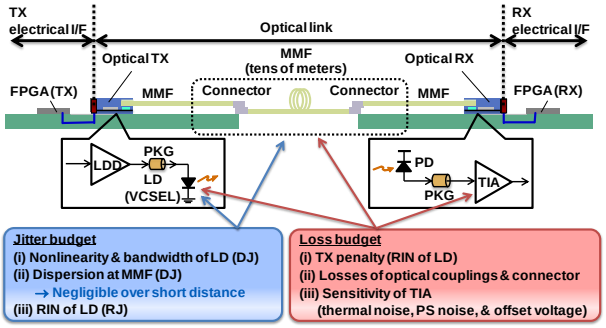

Fig. 1. Structure of fabricated evaluation board mounted on optical TX/RX for 25-Gb/s optical transmission among FPGAs

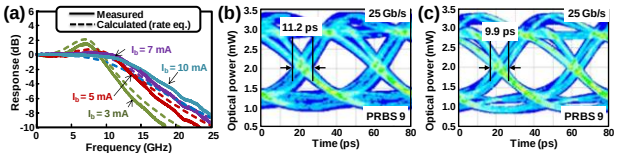

Fig. 2. (a) Calculated and measured frequency responses of VCSEL and (b) calculated and (c) measured 25-Gb/s eye diagrams of optical TX

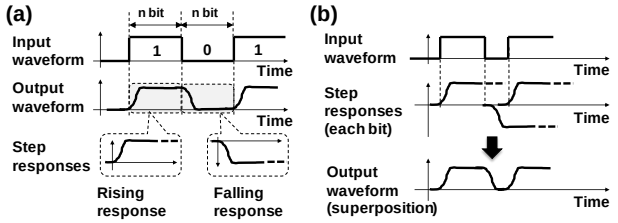

Fig. 3. Methods for calculating (a) rising/falling step responses and (b) optical-output waveform on the basis of step responses

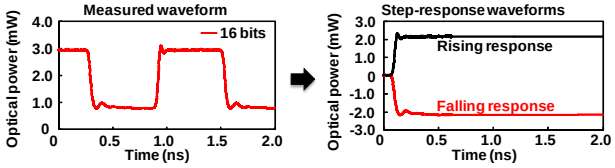

Fig. 4. Generated rising/falling step responses based on a measured optical waveform for a 16-bit sequence pattern

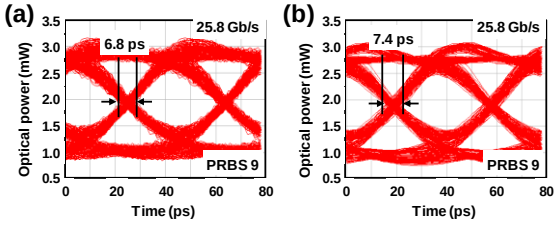

Fig. 5. Comparison between (a) calculated and (b) measured 25.8-Gb/s optical eye diagrams

sequence pattern, which reaches more than 98% of final high- and low- level of optical power, is used for generating rising/falling step responses. The generated rising/falling step responses, which are extracted from the measured output waveform of the optical TX for the 16-bit sequence pattern, are shown in Figure 4. As shown in Figs. 5(a) and (b), with the rising/falling step responses superposed, the calculated 25.8-Gb/s eye diagram agrees well with the measured one. The DJs of the calculated and measured eye diagrams are 6.8 ps and 7.4 ps, respectively, and the jitter error between them is only 0.6 ps.

The effects of the TX electrical I/F on DJ of the optical TX were investigated by using the fabricated evaluation board (see Fig. 1). As shown in Fig. 6(a), the FPGA has a 2-taps feed-forward equalizer (FFE) with pre- and post-cursors as the output circuit. The transmission losses between the FPGA and the optical TX are −14 dB at 12.9 GHz. As shown in Fig. 6(b), the output waveforms of the optical TX for 16-bits sequence pattern are almost constant regardless of changes in the input waveform, made by adjusting equalization gain of the FFE, because the LDD usually has a limiting amplifier to keep a constant output current regardless of the amplitude of the input signals. The proposed LD-modeling method can thus generate the rising/falling step responses even if the conditions of the TX electrical I/F are changed.

On the other hand, the optical 25.8-Gb/s eye diagrams for a PRBS pattern change significantly according to the values of the equalization gain. The changes of the eye diagrams are due to DJ at the electrical I/F, which is determined by the characteristics of the FFE and the transmission lines. To consider the effects of DJ at the electrical I/F, an input waveform through the TX electrical I/F was simulated by a behavior model based on the S-parameter. The calculated 25.8-Gb/s eye diagram at equalization gain of 8.8 dB, which was obtained by superposing the measured rising/falling step responses on the simulated input waveform, is shown in Figure 6(c). As shown in Fig. 6(d), the calculated eye diagram reproduces the measured one well with jitter error of 1.6 ps between them.

As shown in Fig. 7(a), 25.8-Gb/s optical transmission between FPGAs was experimentally demonstrated. In this experiment, the FPGA evaluation board was connected to another evaluation board (mounted on the optical TX/RX) through SMP connectors and coaxial cables. Equalization gain must be adjusted to obtain error-free 25.8-Gb/s optical transmission because electrical transmission losses significantly reduce the jitter margin for the optical link. The relations between calculated and measured total jitters (TJs) at the input of the FPGA on the RX side and equalization gains of the FPGA on the TX side are shown in Figure 7(b). The calculated TJs (including RJ of 0.5 ps_{rms}), which were obtained by the proposed LD modeling method and electrical behavior models, exhibit the largest jitter margin when the equalization gain is set to 6.5 dB. Also, when the same equalization gain was set, the measurement results show the smallest TJ and error-free operation with jitter margin of 0.54 UI.

B. Evaluation results and method for reducing RJ

To investigate the contribution of RJ due to a LD, TJ of a previously developed optical TX [6], which consists of an LDD and a DFB-LD operating at 1.3-μm wavelength, was measured. For this measurement, the optical TX was connected to a 40-GHz digital sampling oscilloscope with a jitter-analysis function through an optical attenuator and MMF, as shown in Fig. 8(a). Modulation and bias currents of the LDD were 21 mApp and 60 mA, respectively. Results of jitter analysis at data rates of 25, 32, and 40 Gb/s, where RJ of the LDD was measured by using a sample without implementing the DFB-LD, are shown in Fig. 8(b). RJ values of the DFB-LD were almost constant, namely, about 10 ps, regardless of the data rate. Therefore, as data rate increases, RJ of the DFB-LD significantly reduces jitter margin of an optical link. Measured 25- and 40-Gb/s optical eye diagrams of the optical TX are shown in Figures 8(c) and (d). As clear from the figures, the 40-Gb/s eye diagram exhibited lower signal-to-noise ratio than the 25-Gb/s one because of its higher rate of RJ.

The output of directly modulated LDs exhibits fluctuations in intensity, namely, RIN, even if the LD is biased at a constant current without current fluctuations. In the case of an optical interconnect, where the LD generally operates at small extinction ratio (ER) to improve power efficiency, the effects of RIN must be evaluated in terms of RIN_{OMA}. Relations between RIN_{OMA} and RJ (at BER of less than 10^{-12}) to ER, which were evaluated by using the same measurement setup as shown in Fig. 6(a) are shown in Figures 9(a) and (b). In this measurement, three kinds of optical TXs consisting of different VCSELs and LDDs, namely, modules A, B, and C, were used. Moreover, in regard to module A, the relations in the case of two output modulation currents, namely, 2.6 and 5.2 mApp, were measured. As shown by the line fitted on the basis of the measurement results for module A (dotted lines), to reduce RJ, ER for the VCSEL must be increased because degradation of ER increases RIN_{OMA}. Regardless of the value of ER, module C exhibited larger RJ than the RJs of the other optical TXs. 25.8-Gb/s optical eye diagram for modules B and C are shown in Figures 9(c) and (d), respectively. Clearly, the eye diagram of module C shows significant ringing, which enhances the increment of RJ due to RIN, because it

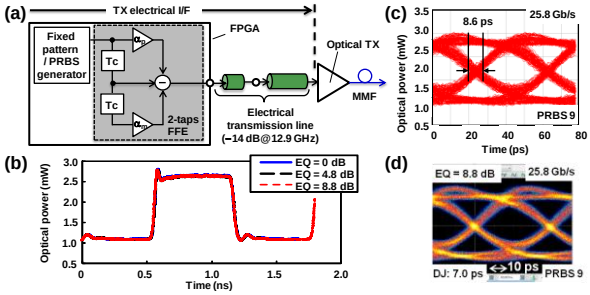

Fig. 6. Effects of optical waveforms on TX electrical I/F: (a) measurement setup, (b) measured optical waveforms for a 16-bit sequence pattern, (c) calculated, and (d) measured 25.8-Gb/s eye diagrams

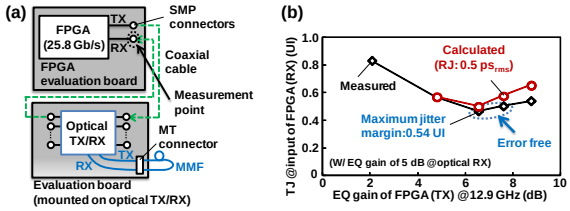

Fig. 7. Experiment on 25.8-Gb/s optical transmission among FPGAs: (a) measurement setup and (b) relations between measured and calculated jitters at input of FPGA (RX) and equalization gain of FPGA (TX)

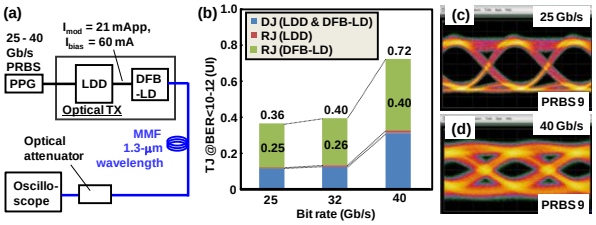

Fig. 8. (a) Measurement setup for evaluating jitter performance, (b) results of measured-jitter analysis, and (c) 25-Gb/s and (d) 40-Gb/s optical eye diagrams for DFB-LD-based optical transmitter operating at 1.3-μm wavelength

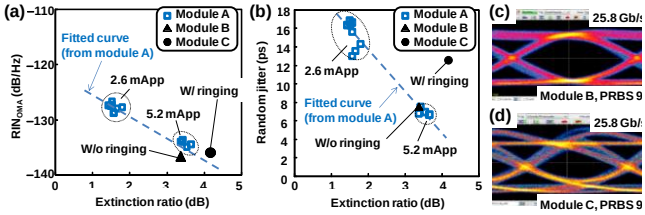

Fig. 9. Measured relationship between (a) RIN_{OMA} and (b) RJ to ER, and measured 25.8-Gb/s optical eye diagrams of (c) module B and (d) module C

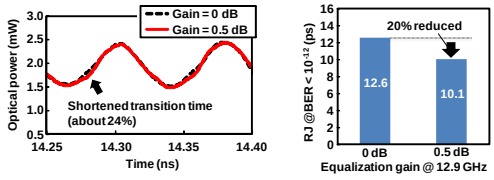

Fig. 10. Reduction of RJ by shortening transition time of the optical TX (module C)

shortens the transition time of the output waveform of the optical TX. As shown in Fig. 10, the fabricated evaluation board mounted on module C as an optical TX was used to evaluate the effect of reducing RJ by shortening the transition time of the optical TX. The transition time was shortened by adjusting the pre-tap of the two-taps FFE inside the FPGA. As shown in the right graph, RJ was reduced by 20% by shortening transition time by about 24%.

IV. Conclusion

A 25.8-Gb/s optical interconnect must accommodate the jitter budget of the optical link. To enlarge the jitter margin, by considering the electrical I/F and optical link as one, an electrical and optical concurrent design methodology was established. The developed design methodology can calculate an optical eye diagram similar to the measured one with jitter error between them of less than 1.6 ps. As the key for establishing the design methodology, a simple LD modeling method based on measured step responses is proposed. The design methodology makes it possible to optimize equalization gain (at the electrical I/F) for maximizing the jitter margin of the optical link. Error-free 25.8-Gb/s optical transmission between FPGAs with jitter margin of 0.54 UI was experimentally demonstrated by optimizing the equalization of the FPGAs. Moreover, it was confirmed that RJ at the optical link is reduced by 20% by shortening the transition time by about 24%.

References

[1] J. Proesel et al., "25Gb/s 3.6pJ/b and 15Gb/s 1.37pJ/b VCSEL-based optical links in 90nm CMOS," ISSCC Dig. Tech. Papers, pp. 418-420, Feb., 2012.

[2] T. Takemoto et al., "A 25-Gb/s 2.2-W 65-nm CMOS Optical Transceiver Using a Power-Supply-Variation-Tolerant Analog Front End and Data-Format Conversion," IEEE JSSC, vol. 49, pp. 471-485, 2014.

[3] T. Takemoto et al., "A 25-to-28 Gb/s High-Sensitivity (–9.7 dBm) 65 nm CMOS Optical Receiver for Board-to-Board Interconnects," IEEE JSSC, vol. 49, pp. 2259-2276, 2014.

[4] T. Takemoto et al., "A 25-Gb/s 100-m multi-mode fiber optical link based on 1.3μm lens-integrated surface-emitting laser and CMOS receiver," Proc. SPIE 9010, Feb., 2014.

[5] G.P. Agrawal, "Fiber-Optic Communication Systems", Wiley Series in Microwave and Optical Engineering. Fourth ed., John Wiley & Sons. Inc. ISBN: 978-0-470-50511-3

[6] T. Takemoto et al., "A 50-Gb/s NRZ-modulated Optical Transmitter based on a DFB-LD and a 0.18-μm SiGe BiCMOS LD Driver," Proc. OFC 2015, Tu3G.2, 2015.