A Highly Linear Dual-Band Mixed-Mode Polar Power Amplifier in CMOS with An Ultra-Compact Output Network

Jong Seok Park[1], Song Hu[1], Yanjie Wang[2], and Hua Wang[1]

[1]Georgia Institute of Technology, Atlanta, GA 30308, USA [2]Intel Corporation, OR 97124, USA

***Abstract* — This paper presents a highly linear dual-band mixed-mode polar power amplifier fully integrated in a standard 65nm bulk CMOS process. An ultra-compact single-transformer passive network provides dual-band optimum load-pull impedance matching, parallel power combining, and double even-harmonic rejection without any tunable element or band selection switch. The mixed-mode architecture leverages both digital and analog techniques to suppress the AM-AM and AM-PM distortions and achieves high linearity. As a proof-of-concept design, the dual-band mixed-mode polar power amplifier is implemented in a 65nm CMOS process. We demonstrate the peak output power of +28.1dBm/+26.0dBm with the PA drain efficiency of 40.7%/27.0% at 2.6/4.5GHz. Measurement with 1MSym/s 256-QAM signal achieves rms EVM of 2.05%/1.03% with the average output power of +21.51dBm/+19.27dBm at 2.35/4.7GHz. The measured 2nd-harmonic rejection for the 2.35GHz signal is 37.7dB.**

***Index Terms* — Digital, dual-band, mixed-mode, power amplifiers, transformer.**

I. Introduction

Modern wireless systems often need multi-band and multi-mode operations to simultaneously support different communication standards. Similarly, frequency agile and highly reconfigurable systems are widely needed in defense electronics for optimum spectrum access. These rapidly growing demands have posed tremendous challenges for next-generation radio frequency (RF) power amplifiers (PA) development.

A popular multi-band PA scheme is to directly assemble several single-band PAs either in a single chip or on a multi-chip module (MCM) [1] [2]. However, this approach often suffers from several major limitations, such as increased cost, large chip/module area, dedicated antenna interface, and complicated packaging.

On the other hand, high-order passive networks and/or tunable passives can be utilized to achieve multi-band impedance matching and power combining for RF PAs [3] [4]. However, these solutions require high-order networks with multiple inductors and excessive area. Moreover, tunable components can lead to nonlinearity and reliability concerns. In addition, they often present compromised passive efficiency, resulting in reduced PA efficiency.

To address these challenges, we present a highly linear dual-band mixed-mode polar PA architecture which can be fully integrated as a one-chip solution in bulk CMOS processes. An ultra-compact output network based on a single transformer simultaneously provides dual-band PA load-pull impedance matching, parallel power combining, and double even-harmonic rejection without any tunable element or switch. Our polar PA achieves highly linear operation by incorporating mixed-mode linearization techniques, i.e., digital high-precision amplitude controls and analog varactor phase compensations, to suppress both AM-AM and AM-PM distortions. The design details and measurement results of our proof-of-concept dual-band PA design are presented in the following sections.

II. Mixed-Mode Dual-Band Polar PA Architecture

The proposed dual-band mixed-mode PA is composed of two sub-PAs and a single-transformer output passive network (Fig.1). Each sub-PA contains 7-bit binary-weighted 3-stage digital PA cells and one driver chain. The five most significant bits of the PA cells are thermometer-coded for optimum matching and the remaining two bits are binary-coded. The unit PA cell is a cascode class-D^{-1} amplifier for enhanced output power.

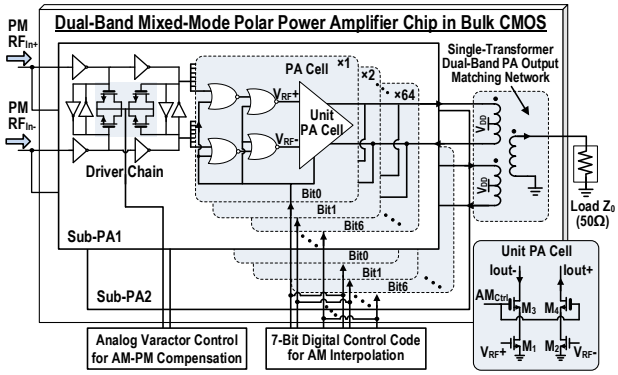

Fig.1. Proposed dual-band mixed-mode polar PA schematic.

During the PA operation, a differential phase modulated (PM) RF input signal is equally divided and fed to the two sub-PAs. These two RF signals are buffered by the driver chain in each sub-PA and multi-stage back-to-back inverters ensure the differential signaling. The PM RF signals then drive the 7-bit PA cells. At the same time, 7-bit digital amplitude modulation (AM) control codes turn on the proper number of PA cells to synthesize the desired amplitude [5]. Thus, the PA performs the polar operation and recovers the complex modulated signals at the output. The single-transformer output network combines the two sub-PAs for further output power enhancement.

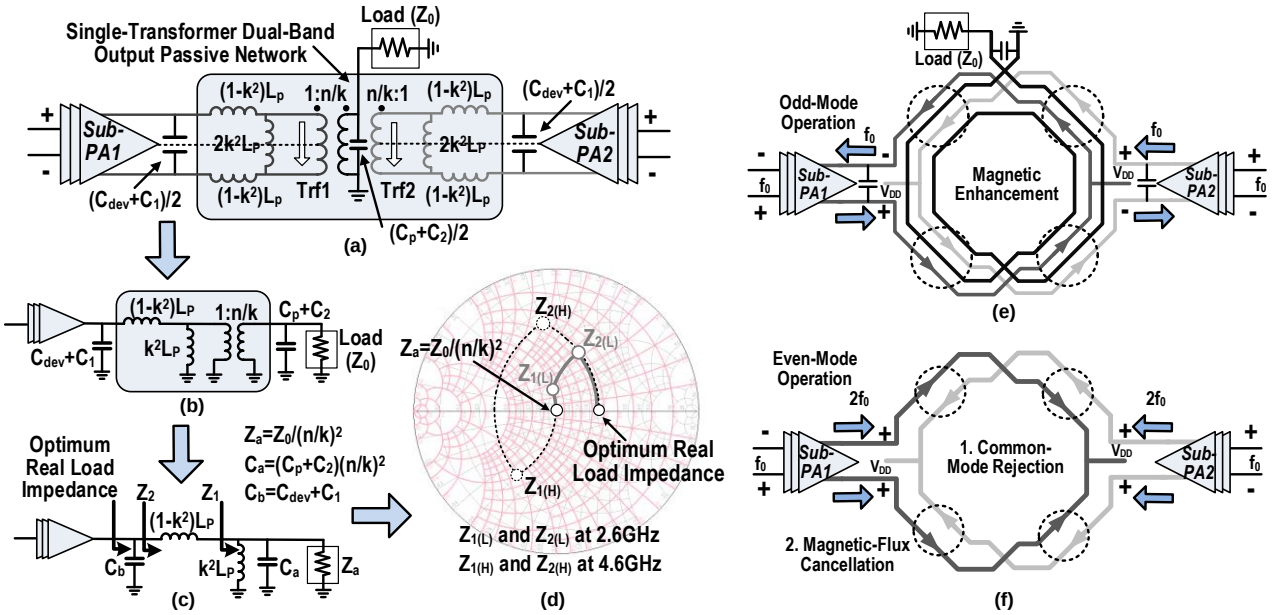

Fig.2. (a) Proposed single-transformer output network. (b) Single-transformer output network in its single-ended configuration. (c) Equivalent lumped-element model. (d) Dual-band impedance matching on the Smith chart. Layout of the single-transformer output network with (e) magnetic enhancement for odd-mode signals and (f) magnetic double cancellation for even-mode signals.

A. Single-Transformer Dual-Band PA Output Matching Network with No Tunable Element or Switch

The proposed single-transformer dual-band output passive network is depicted in Fig.2a with its odd-mode half-circuit shown in Fig.2b. The physical transformer can be modeled as an ideal 1:(n/k) transformer with the magnetizing inductance k^2L_p and the leakage inductance $(1-k^2)L_p$ [6]. The two transformer inductors together with its parasitic capacitor C_p, device output capacitor C_{dev}, and extra capacitors C_1 and C_2 form a 4th-order passive network, providing load-pull impedances at two different frequencies (Fig.2c and Fig.2d). The dual-band matching is explained as follows. For the high-band case, the LC shunt resonator (k^2L_p and C_a) behaves capacitive and transforms the load $Z_a=Z_0/(n/k)^2$ to impedance $Z_{1(H)}$. A series-L/parallel-C matching by $(1-k^2)L_p$ and C_b then converts $Z_{1(H)}$ to the optimum load for the PA device. The optimum load is real, since the device capacitance C_{dev} is absorbed in the matching network. Note that the ideal 1:(n/k) transformer and the 4th-order network together provide load impedance down-transformation. The low-band case operates similarly (Fig.2c and Fig.2d).

Parallel power combining is achieved by two transformers Trf1 and Trf2 (Fig.2a). We arrange two transformers within one-inductor footprint for substantial area reduction (Fig.2e). The layout maintains full symmetry and provides magnetic field enhancement for desired odd-mode signals from the two sub-PAs (Fig.2e). Moreover, it achieves double cancellation of the unwanted even-mode signals (Fig.2f). The even-mode harmonics of the differential sub-PA1 and sub-PA2 are first suppressed by the common-mode rejection of the differential coils. Furthermore, the layout forces the two sub-PAs' even-mode signals to run in an anti-parallel fashion, which cancels their magnetic flux for further suppression. This double even-mode suppression is critical in multi-band/broadband PAs, since even-order harmonics of the low-band signals may fall into the high band.

We implement this PA output network in a standard bulk 65nm CMOS process (Fig.3). After absorbing the PA device output capacitance, single-ended load impedances of 13Ω and 12Ω are respectively achieved at 2.6GHz and 4.6GHz, which match well with the target optimum loads (13Ω/13Ω at 2.6GHz/4.6GHz) by the large-signal PA load-pull simulations. The passive efficiency for the desired odd-mode operation is 78.5% and 62% for 2.6GHz and 4.6GHz, respectively. The simulated suppression of the 2.35GHz signal's 2nd-harmonic (4.7GHz) is 40dB.

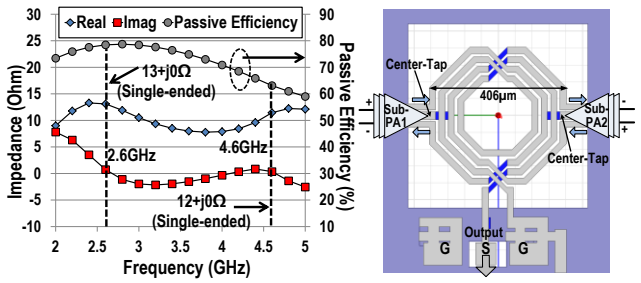

Fig.3. Simulated dual-band load impedance matching and network passive efficiency using full 3D EM modeling.

B. Mixed-Mode Linearization Techniques

Mixed-mode linearization techniques are employed to enhance the PA linearity when amplifying signals with large peak-to-average-power-ratios (PAPRs).

First, the proposed PA adopts 7-bit digital AM control codes for the amplitude modulation. This allows precise interpolation of the transient envelope and direct pre-distortion, which largely suppress the AM-AM distortions.

Secondly, the AM-PM distortion is mainly caused by the device parasitic capacitance variations due to the turning on/off different numbers of PA cells and different large-signal voltage swings. For example, the nonlinear drain capacitances of the cascode devices in the unit PA cell (M_3/M_4 in Fig.1 inset) are often the main contributors [7]. Our single-transformer output network employs extra Metal-Oxide-Metal (MOM) capacitor C_1 (1.8pF) in parallel with the PA output parasitic capacitor C_{dev} (1.6pF), making the total capacitance less sensitive to different power levels.

To further suppress the phase distortions, we employ 2-stage differential varactors in each driver chain. Their analog control voltages are varied dynamically to compensate the remaining AM-PM nonlinearity (Fig.1).

III. Measurement Results

As a proof-of-concept design, we implement the dual-band mixed-mode polar PA in a standard 65nm CMOS process with 1.5mm×1.5mm chip area. The ultra-compact single-transformer output network with the diameter of 406μm achieves dual-band matching without any tunable element or switch. The supplies for the PA cores and digital drivers are 3V and 1.5V, respectively.

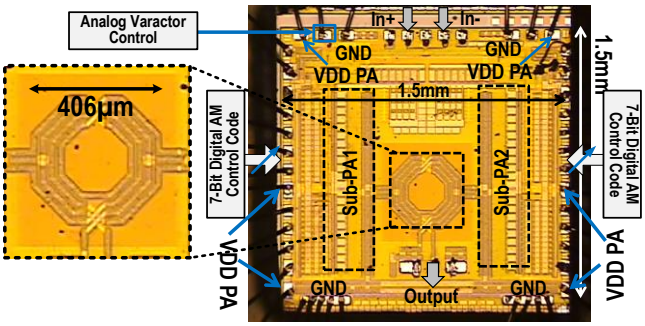

Fig.4. The dual-band PA chip microphotograph.

The PA is first characterized by continuous-wave (CW) signals. The measured peak PA drain efficiency and power added efficiency (PAE) are 40.7%/27.0% and 35%/21.2% with +28.1dBm/+26.0dBm output power (P_{out}) at 2.6/4.5GHz, which verify the dual-band operation (Fig.6a). The 0.5dB P_{out} bandwidth is 2.3GHz-3.3GHz at the low band and 4GHz-4.7GHz at the high band.

The 2nd-harmonic suppression of 37.7dB is achieved at 2.35GHz (2nd-harmonic at in-band 4.7GHz) with no extra filtering, verifying double even-mode rejection (Fig.6b).

The measured AM-PM distortion and compensation are shown in Fig.6c. First, the AM-PM responses (referenced to the peak P_{out}) are measured with no compensation, yielding maximum AM-PM distortions of 32° at 2.35GHz and 27° at 4.7GHz. By adjusting the varactor control voltages, the AM-PM distortions are largely compensated.

Next, the PA is characterized with complex modulated signals of 64-QAM (5.76dB PAPR) and 256-QAM (6.62dB PAPR) modulations. The PM RF signal is synthesized by a vector signal generator, while the AM signal is digitized as 7-bit digital control codes by an FPGA board at ×10 over-sampling ratio (OSR).

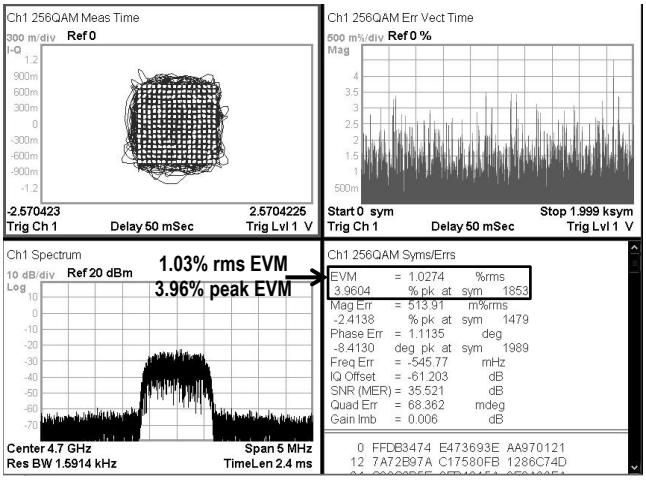

Fig.5. Measured EVM with 1MSym/s 256QAM at 4.7GHz.

The measurement with 1MSym/s 64-QAM signal demonstrates rms EVM of 2.44%/1.11% with average +22.28dBm/+20.09dBm P_{out} and PA drain efficiency of 19.1%/14.9% at 2.35/4.7GHz, respectively. The measurement with 1MSym/s 256-QAM signal shows rms EVM of 2.05%/1.03% with average +21.51dBm/ +19.27dBm P_{out} and PA drain efficiency of 18.5%/13.6% at 2.35/4.7GHz. Figure 5 shows the detailed measurement results for 1MSym/s 256-QAM signal at 4.7GHz. The rms EVM is only 1.03% and the peak EVM is 3.96%. The close-in out-of-band spectrum is kept below -35dBc with no additional filtering (Fig.7a). The measured rms EVMs for 0.5MSym/s 256-QAM signal versus P_{out} back-off up to 12dB are shown in Fig.7b, achieving rms EVM consistently below 2.05%. Figure 7c shows the output power spectrum density (PSD) for 1MSym/s 256-QAM signal at a wide frequency span. For 1MSym/s modulation with ×10 OSR, the sampling images appear at 4.71GHz and 4.69GHz with 36.7dB suppression, which is 11dB better than the zero-th-order hold sampling images and can be further improved by pulse shaping techniques [5].

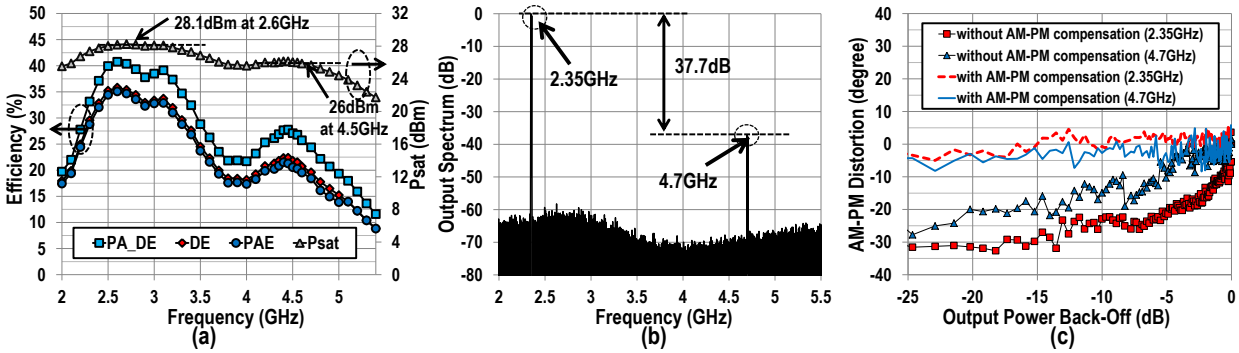

Fig.6. (a) Measured PA output power and efficiency. (b) Measured 2nd-harmonic rejection at 2.35GHz/4.7GHz. (c) Measured AM-PM distortion with and without AM-PM compensation.

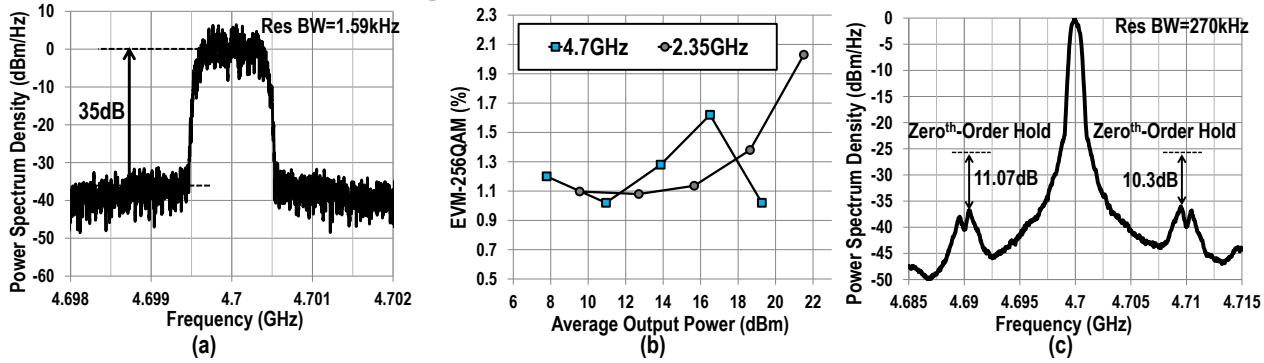

Fig.7. (a) Measured instantaneous PA close-in output spectrum for 1MSym/s 256QAM. (b) Measured rms EVMs for 0.5MSym/s 256QAM versus output power back-off. (c) Measured PA output spectrum for 1MSym/s 256QAM at a wide frequency span.

IV. Conclusion

A highly linear dual-band mixed-mode polar PA fully integrated in a standard 65nm CMOS is demonstrated. The output passive network occupies only one-inductor footprint and achieves dual-band optimum load matching, parallel power combining, double even-mode rejection, and differential to single-ended conversion. Mixed-mode techniques are employed to largely suppress the AM-AM and AM-PM distortions. The PA achieves +28.1dBm/ +26.0dBm peak P_{out} with 40.7%/27.0% peak PA drain efficiency at 2.6/4.5GHz with 37.7dB 2nd-harmonic suppression. The PA supports high-fidelity amplification of high-order QAM modulations and demonstrates 2.05% and 1.03% rms EVMs for 1MSym/s 256-QAM signal at 2.35GHz and 4.7GHz.

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TABLE I. Performance Comparison with Reported CMOS Dual-Band PAs

	Freq. (GHz)	Configuration	Output Network Configuration	Peak P_{out} (dBm)	Peak Efficiency (%)	Modulation Test (rms EVM/P_{out}/Efficiency)	Technology
This Work	**2.6/4.5**	**Single PA**	**1 transformer (no switch or tunable element)**	**28.1/26.0**	**35/21.2 (PAE) 40.7/27.0 (PA DE)**	**2.05% (256QAM)/21.51dBm/18.5% (PA DE) at 2.35GHz 1.03% (256QAM)/19.27dBm/13.6% (PA DE) at 4.7GHz**	**65 (nm)**
Ref [1]	2.4/5	Multiple PAs	2 transformers	28.3/26.7	35.3/25.3 (DE)	3.98% (OFDM)/19.5dBm/14.1% (DE)	65 (nm)
Ref [2]	2.4/5	Multiple PAs	2 transformers	29/26	33.9/32.1 (DE)	5.6% (64QAM)/18.7dBm/N.A.	45 (nm)
Ref [7]	1.95/2.4	Single PA	4 transformers	31.8/32	28.8/32.4 (PAE)	2.8% (OFDM)/23.8dBm/N.A.	65 (nm)
Ref [8]	2.4/5	Multiple PAs	N.A.	26.8/26.6	N.A.	3.9% (OFDM)/17dBm/17.5% (PA_DE)	90 (nm)
Ref [9]	2/6	Single PA	1 transformer+3 inductors	22.4/20.1	28.4/19 (PAE)	2.5% (256QAM)/11.3dBm/N.A.	65 (nm)