A 3.9 mW, 35-44/41-59.5 GHz Distributed Injection Locked Frequency Divider

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***Abstract*—Distributed injection-locked frequency division concept, principle, and design methodology at mm-wave frequencies are presented. A proof-of-concept prototype, realized in a foundry 130 nm BiCMOS SiGe HBT technology, achieves a measured locking range of 35-44 GHz and 41-59.5 GHz while consuming 3.9 mW from a 1.1 V supply.**

***Index Terms*—Injection locked frequency Divider, divide-by-two circuit, mm-wave, locking range**

I. Introduction

The demand for higher data rates have resulted in a surge of mm-wave systems and applications including 5G cellular, back-haul, automotive radar, WiFi, etc. The high non-recurring engineering cost associated with mm-wave wireless transceivers in state-of-the-art technologies and larger number of designated mm-wave frequency bands, each with a wide contiguous bandwidth, for the same or similar applications, motivate wideband software programmable mm-wave transceivers and related building blocks. A wideband power-efficient compact frequency synthesizer is an important enabler for this vision. Phase Locked Loops (PLL) are common frequency synthesis blocks. Wideband Voltage Controlled Oscillators (VCO) at mm-wave frequencies have been reported [1]. The first frequency divider following the wideband VCO must also be wideband and operate at mm-wave frequencies. As non-autonomous nonlinear dynamical systems, frequency dividers operate over a finite frequency range commonly referred to as locking range.

Among different topologies, injection locked frequency dividers are capable of operating at high frequencies; but a conventional design will result in a limited frequency locking range. Different techniques have been explored to improve the locking range of the injection locked dividers [2][4][5]. These techniques generally aim at improving the injection efficiency over wider range of frequencies using passive structures. For example in [1], a passive LC circuit is added between the injection device and the active core to track the impedance of the tank and improve injection strength over a wider range of frequencies. Here, we propose a very effective method in achieving wideband injection locked dividers. The idea is inspired by distributed amplifiers and takes advantage of a distributed injection network. The basics of the proposed solution, along with the integrated implementation, simulations and measurements are discussed in the following Section.

II. Proposed Distributed Injection Locked Frequency Divider

A. Basics of operation and design guidelines

Figure 1(a) shows a simplified schematic of a conventional injection locked divide-by-two circuit. Through the gate of the NMOS device, a signal is injected at a frequency close to double the self-oscillation frequency of the active structure. Within a frequency locking range, an oscillation with a frequency of half of that of the injected signal will be sustained across the active structure. The locking range depends on the injection power, size of the injection device, quality factor of the tank, and the active core [2]. Larger injection device size and input power are desirable to increase the strength of the injected signal. Larger size of the injection device in turn increases its conductance which can stop the output from oscillation (reduced gain condition). Larger size also increases the parasitic capacitance at tank nodes resulting in lower maximum frequency and/or higher power consumption (smaller inductor, higher power). Lower quality factor tank generally increases the locking range, but requires increased power consumption to satisfy the gain condition. The proposed solution aims at mitigating these trade-offs. Figure 1(b) shows the proposed concept of distributed injection locked frequency divider. In this scheme, multiple injection devices are used. Multiple injection signals experience equal delays and add-up coherently to create a strong overall injection. The injection transistors' parasitics are incorporated in the distributed transmission line network and result in a wideband passive network. Common-mode termination ($Z_0'/2$) is used to absorb the reflected waves at the injection frequency. This resistor does not affect the quality factor of the resonator at output frequency since it is at the virtual ground node. Compared with the conventional design, the injection device is broken down into smaller devices and the injection through these devices add coherently, while their parasitics are absorbed in the artificial transmission line.

As an example, a $0.13\mu m$ BiCMOS SiGe HBT technology is used to examine the proposed scheme and explain design trade-offs. Microstrip transmission lines are used to implement the inductors. The geometry of the transmission lines are similar to the final implementation as shown in Fig. 4. The power consumption is set to 4 mW. In general, higher number of injection points results in a wider locking range, at the cost of more complex layout and higher sensitivity to parasitics. As a compromise, 5 taps are used as in the final implementation. The emitter lengths of the cross-coupled devices are set to 4 μm to maximize the cross-coupled transconductance at the frequency of operation. The self-oscillation frequency of the divider is set to 25 GHz. The required reactance of the distributed passive network is therefore known at 25 GHz (72 Ω in this design example), and must resonate with the parasitic capacitance of the cross-coupled pair. The trade-off in determining the size of switches is similar to the conventional design, *i.e.* larger switches will increase the injection strength (improving the phase condition predicted by Adler Equation [2][3]), but add loss and reduce quality factor and eventually result in the gain condition to become the bottleneck. 15 μm is found to be the optimum width for NMOS injection transistors, and the DC gate-source voltage is set around 0.4 V. The output transmission line geometries are set based on the switch size, required self-oscillation frequency, and the optimum quality factor to maximize the locking range. The input transmission lines are designed such that the delays between multiple injections are aligned and hence the locking range is maximized. Figure 2 shows the simulated sensitivity curve, when all layout parasitics are ignored. For comparison, the sensitivity curve of an optimally designed conventional divider for the same power consumption and technology is also shown. Component values are tuned in the final design to account for layout parasitics and output buffer loading impedance and are shown in final schematics (Fig. 4).

B. Simulation and measurement results

Figure 3 shows the micrograph of the chip. The chip has an area of 1 $mm \times 0.9$ mm and is fabricated in the IBM 8HP technology. The divider's active area is 630 $\mu m \times 90$ μm as marked in Fig. 3. Figure 4 shows the complete schematics of the fabricated chip. Five Microstrip transmission lines are used for the input feed and coupled differential transmission lines are used for the core distributed resonator. The parasitics of the input Electro-Static Discharge (ESD) diode are incorporated into the input transmission line network, preventing it from limiting the input bandwidth. An additional switched MIM capacitor is added across the cross-coupled pair to extend the division frequency to lower frequencies by

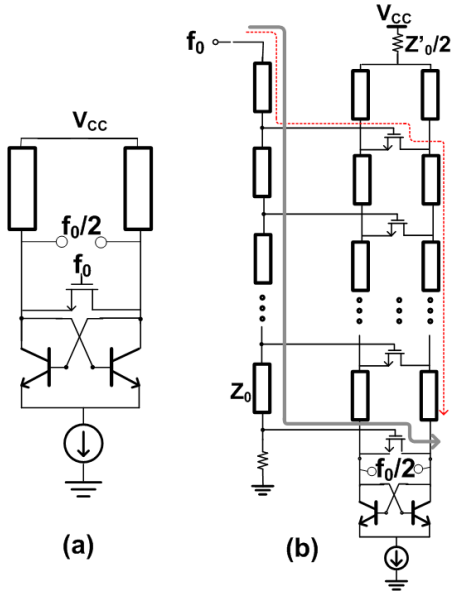

Fig. 1. (a) Conventional injection locked divider, (b) proposed distributed injection locked divider.

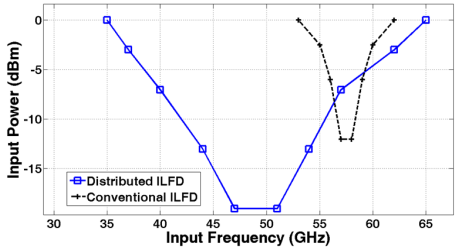

Fig. 2. Simulated sensitivity curves of the representative mm-wave injection locked dividers with similar power consumption and technology.

reducing the self oscillation frequency of the divider. The buffer is an open-collector differential pair with resistive degeneration to reduce the capacitive loading of the buffer on the divider core. Figure 5 shows the measurement setup. For frequencies below 40 GHz, an Agilent E8257C signal generator is used to provide the input tone. For frequencies beyond 40 GHz, a frequency multiplier ($\times 4$) is used in tandem with a variable attenuator to provide the input to the divider. Figure 6 shows the spectrum measurements of the output signal read directly from the Spectrum Analyzer. The spectrum of the self-oscillation (at right), and locked spectrum (at left) for the high-band (*i.e.*, when the MIM capacitor is not switched in), are shown. For nominal bias conditions ($V_G = 1.6V$, $V_{CC} = 1.2V$, $I_{core} = 4mA$, $I_{buf} = 1.5mA$), the self-oscillation frequency for the high and low bands are 25.9 and 21.3 GHz, respectively. The output power for nominal bias conditions is measured at -21 dBm single-ended (simulated -19 dBm), and is -25 dBm for the low-band. Figure 7 shows the simulated and measured sensitivity

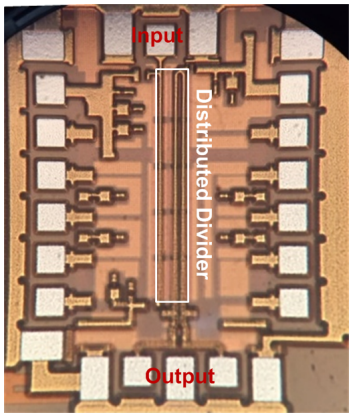

Fig. 3. Micrograph of the mm-wave distributed injection-locked frequency divider.

curves for nominal design bias conditions. The spectrum beyond the senstivity curve region shows characteristics of a pulled oscillator spectrum, indicating that locking is lost by not satisfying the phase condition. As expected, the achieved locking range is varied as the bias conditions (*e.g.* gate-source voltage of injection devices, core and buffer bias current) are changed. As an example, Figure 8 shows sensitivity curves for different core currents, for a certain set of bias conditions. One interesting observation is that for divider bias currents below 2.8 mA, at the edge of the locking range, the output signal disappears, indicating that the gain condition is not satisfied due to injection switches loss [1]. For $V_G = 1.54V$, $V_{CC} = 1.1V$, $I_{core} = 3.5mA$, $I_{buf} = 0.9mA$, maximum locking range of 41-59.5 GHz for the high band, and 35-44 GHz for the low band for 0 dBm input power are achieved. Figure 9 shows the measured phase noise of the input and divided output for a 48 GHz input signal with -10 dBm power. The phase noise at lower offsets follow the input phase noise with 6 dB difference (the standard deviation from the ideal divided phase noise from 1 kHz to 1 MHz is 0.73 dB). The phase noise floor beyond 1 MHz varies as the bias current of the buffer (and hence output power) is changed, indicating that it is the combined phase noise floor of the buffer and the measurement instrument. Table 1 shows the comparison with state of the art mm-wave frequency dividers. It should be noted that the injection switches in this design are 0.13 μm CMOS transistors, and migrating to a lower CMOS node is expected to improve the locking range even further.

III. Conclusion

In this paper, the concept of distributed injection locked frequency division is introduced to realize wide locking range mm-wave frequency dividers. The concept is used to implement a frequency divider in 0.13 μm RF BiCMOS

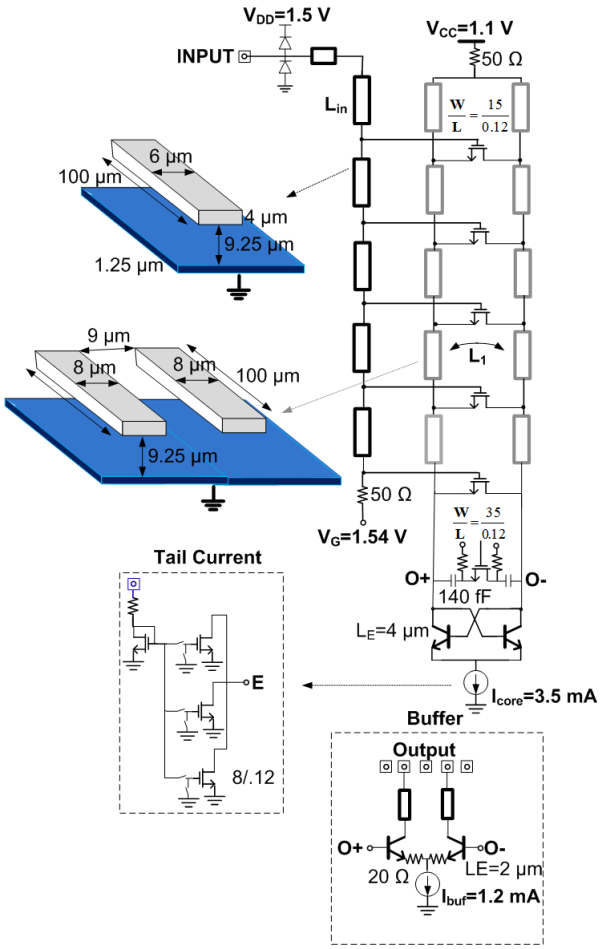

Fig. 4. Schematics of the fabricated mm-wave distributed injection locked frequency divider with optimum bias conditions.

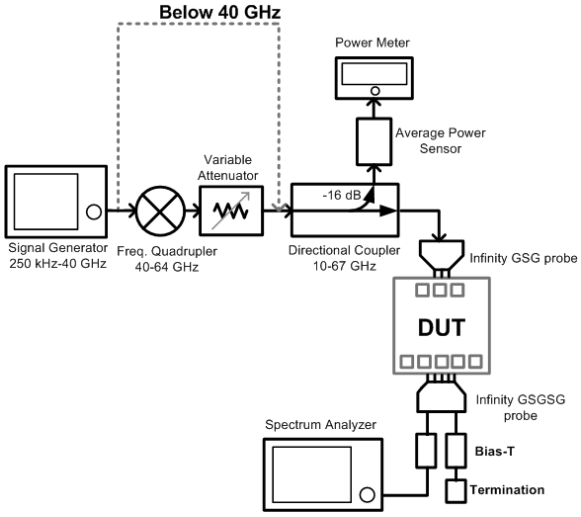

Fig. 5. Measurement setup.

TABLE I
Comparison with mm-wave frequency dividers

	Technology	Opration Frequency (GHz)	Locking Range	Power Consumption (mW)	Core Area (mm^2)	Topology
This Work	**0.13 µm BiCMOS**	**35 - 44 41 - 59.5**	**Low band: 22% High band: 37% Total: 53%**	**3.8**	0.046	**Distributed Injection Locking (IL)**
[7]	32 nm CMOS	40 - 70	54%	4.8	0.001	Dynamic latch with load modulation
[2]	65 nm CMOS	53.4 - 79	39%	2.9	0.126	Freq. Track IL
[4]	65 nm CMOS	48.5 - 62.9	25.9%	1.65	0.015	Multi-order tank IL
[5]	0.13 µm CMOS	59.6 - 67	11.6%	1.6	0.017	Class-B IL
[6]	0.18 µm CMOS	37.5 - 49	26.6%	6	0.428	regenerative

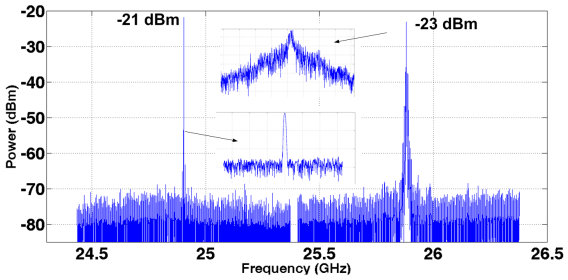

Fig. 6. Free-running and locked output frequency spectrum (zoomed spectrum shown across 30 MHz span).

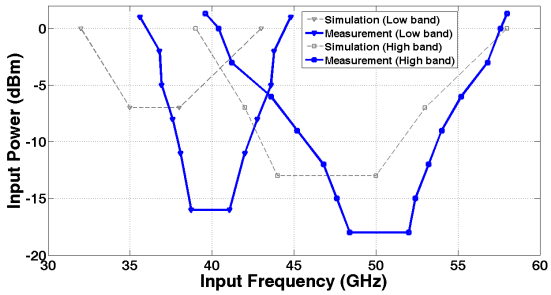

Fig. 7. Simulated and measured sensitivity curves for high and low bands for nominal bias conditions.

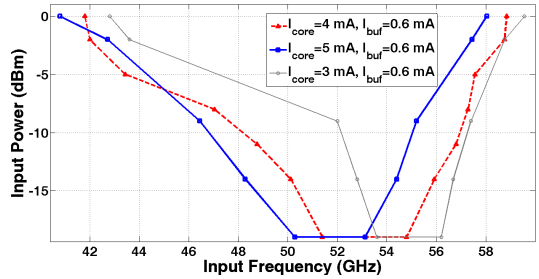

Fig. 8. Measured sensitivity curves for different divider DC currents and lower buffer DC current.

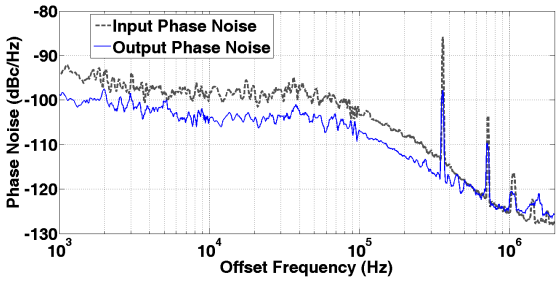

Fig. 9. Measured phase noise of input (48 GHz), and output signals of the frequency divider.

technology, covering 35-59.5 GHz while consuming 3.9 mW of power.

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