A 51 pW Reference-Free Capacitive-Discharging Oscillator Architecture Operating at 2.8 Hz

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***Abstract*—This paper presents a gate-leakage-based Hz-range oscillator that achieves ultra-low-power frequency-stable operation in a small area via a capacitive-discharging architecture. By pre-charging two capacitors to V_{DD}, and then allowing one to discharge through a temperature stable discharging path, an accurate clock period is generated independent of V_{DD} and without a power-expensive reference. By exploiting the opposite temperature dependencies of different gate-leakage transistors, a stable oscillation frequency is achieved. Implemented in a 65 nm CMOS process, the proposed oscillator consumes 51 pW at 2.8 Hz. Across a temperature range of -40 °C to 60 °C, the oscillator deviates down to ±0.05% /°C, enabling an accurate, low-cost, low-power timing solution at Hz-range frequency.**

***Index Terms*—Ultra-low power, timer, oscillator, temperature-stable, gate-leakage.**

I. Introduction

Next-generation wireless sensing devices are pushing power consumption boundaries down to extremely low levels in part by aggressively duty-cycling active circuitry [1]. The overall power consumption in such applications is often limited by the quiescent power during sleep mode, which is usually dominated by the sleep timer. In order to minimize energy-expensive guards band where active radios are turned on early in order to compensate for timing uncertainty, the sleep mode timer should be designed to be frequency-stable under the presence of environmental (e.g., temperature) effects. In addition, many such applications are size and cost constrained, and thus cannot afford an external crystal or post-fabrication calibration routines. Thus, it is imperative to design fully-integrated sleep timers that feature both ultra-low-power consumption and sufficient frequency stability.

The most common fully-integrated oscillator architecture is based on a constant-current relaxation topology, where temperature-stabilized current source is used to charge a capacitive network. In such oscillators, phase transitions are typically determined by a fixed, temperature-compensated threshold voltage, thereby ensuring highly-accurate frequencies. However, design of temperature-compensated current and voltage sources generally consume power overhead to achieve the requisite performance [2]. In addition, for most such applications, the oscillation period is based on an RC time constant, which for Hz-range frequencies is on the order of hundreds of milliseconds, necessitating a total capacitance on the order of 10 nF with an on-chip realizable resistance on the order of hundreds of MΩ, or a total resistance on the order of 10 GΩ with an on-chip realizable capacitance on the order of tens of pF, both of which are prohibitively large for on-chip integration. To reduce area, one-hot topologies operate at Hz-range frequencies by employing gate-leakage transistors as ultra-low-current sources [3] [4]. However, the timer in [3] shows high jitter and temperature sensitivity since the change of phases is determined by the Schmitt trigger instead of a well-defined threshold voltage. To combat this, a multistage structure with a high-gain triggering buffer and boosted capacitance charging is proposed in [4], however, at the price of increased power consumption.

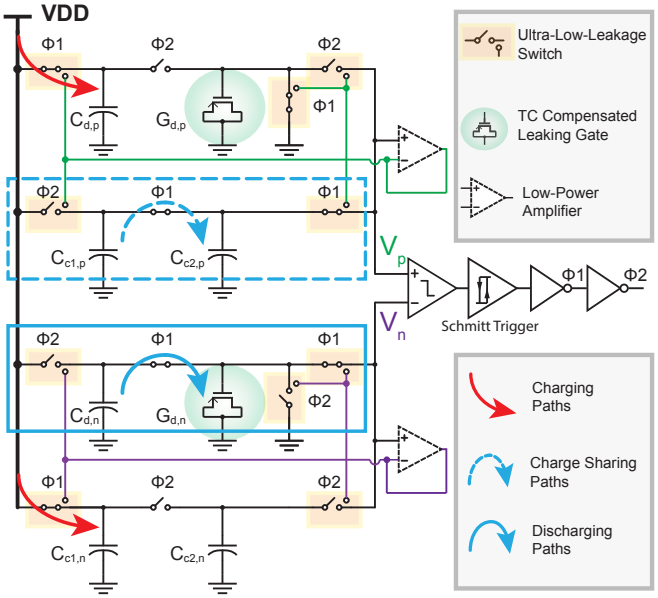

Fig. 1. Architecture of the proposed reference-free capacitive-discharging oscillator.

In this work, a capacitive-discharging gate-leakage oscillator is presented where the oscillation frequency is set primarily by a collection of gate-leakage transistors and reservoir capacitors. Compared to one-hot-topology-based oscillators, the intrinsic relaxation-like operation of the proposed oscillator ensures a highly-accurate frequency. Meanwhile, unlike conventional relaxation oscillators, the proposed topology does not require any temperature-stabilized reference voltage or reference current, enabling ultra-low-power operation. In addition, a Hz-range frequency is achieved with a small active area by employing gate-leakage transistors to effectively serve as large resistors. Therefore, the proposed oscillator achieves frequency-stable, ultra-low-power, and area-efficient operation

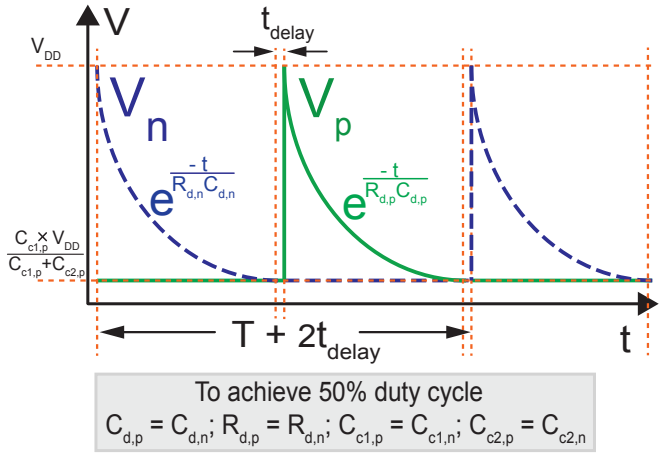

Fig. 2. Timing diagram of the waveforms at the inputs of the comparator over the course of three oscillator cycles.

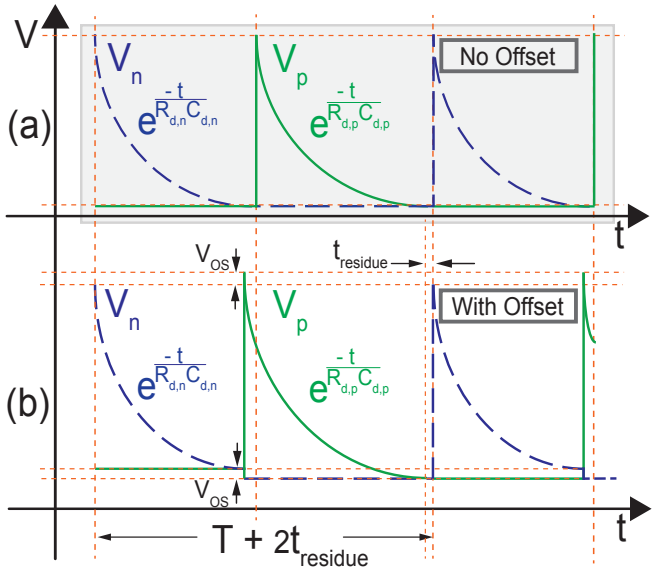

Fig. 3. Waveforms with (a) no comparator offset and (b) positive comparator offset illustrating that the proposed architecture is able to cancel the comparator offset.

at Hz-range frequencies without requiring any external components.

II. Capacitive-Discharging Ultra-Low-Power Oscillator

A. Overview of The Proposed Architecture

The architecture of the proposed oscillator is shown in Fig. 1. In this diagram, discharging capacitors $C_{d,\{n,p\}}$ and charge sharing capacitors $C_{c1,\{n,p\}}$ serve as charge reservoirs. During phase 1, charge sharing capacitor $C_{c1,p}$, which was pre-charged to V_{DD} in the preceding phase, shares its charge with capacitor $C_{c2,p}$. In this case, the voltage generated at the positive terminal of the comparator can be calculated using:

$$V_{ref} = V_{DD}\frac{C_{c1,p}}{C_{c1,p}+C_{c2,p}}. \tag{1}$$

At the same time, discharging capacitor $C_{d,n}$ is being discharged through the temperature-compensated gate-leakage transistors $G_{d,n}$, resulting in an decaying voltage V_{decay} at the negative terminal of the comparator. During this phase, discharging capacitor $C_{d,p}$ and charge sharing capacitor $C_{c1,n}$ are both pre-charged to V_{DD}. When the decaying voltage V_{decay} falls below V_{ref}, the circuit enters phase 2 after a comparator delay, t_{delay}, at which point the negative and positive charge-sharing/discharging roles are reversed, thereby inherently rejecting, to a first order, the temperature-dependent comparator offset voltage [5].

The voltages observed at the comparator inputs during three successive cycles are shown in Fig. 2. In this case, the period of the oscillator is T+2t_{delay}, where the ideal period T is twice the time taken by the decaying voltage to fall below the reference voltage at the other comparator input. The gate-leakage transistors $G_{d,\{p,n\}}$ effectively serve as resistors, $R_{d,\{p,n\}}$, in the discharging paths. Thus, at the point in time when the decaying voltage is equal to the reference voltage, the following equation holds:

$$\frac{C_{c1,p}V_{DD}}{C_{c1,p}+C_{c2,p}} = V_{DD}e^{-\frac{T/2}{R_{d,n}C_{d,n}}}. \tag{2}$$

Therefore, the ideal period T can be calculated by:

$$T = 2R_{d,n}C_{d,n}\ln\frac{C_{c1,p}+C_{c2,p}}{C_{c1,p}}. \tag{3}$$

B. Frequency Accuracy and Stability Versus Supply Voltage, Temperature, and Comparator Offset

Since the initial charge-sharing voltage and decaying voltage are initialized from the same source, V_{DD}, supply noise and variation appear as common-mode noise that is rejected by the 75 dB CMRR of the comparator. The oscillator frequency stability and accuracy is therefore primarily affected by the temperature dependencies of the capacitors and effective resistance of the gate-leakage transistors.

Comparator offset can also significantly affect frequency accuracy and stability. Fortunately, the proposed architecture shows an intrinsic ability to reject the comparator offset. As shown in Fig. 3, the offset voltage is sampled onto both the decaying voltage and the reference voltage in adjacent clock cycles, thereby cancelling, to a first order, the comparator offset voltage through averaging. Since the profile of the decaying voltage is exponential, rather than a static value as in the case for a DC reference potential, there is a small residue error. Simulation results show that the proposed architecture is able to reduce the frequency variation due to comparator offset by over 25.5 dB.

Frequency accuracy and stability is also affected by variation in comparator delay, t_{delay}. In order to limit the impact of variation, the bandwidth of the comparator is set such that the delay is nominally less than 10 ppm of the period.

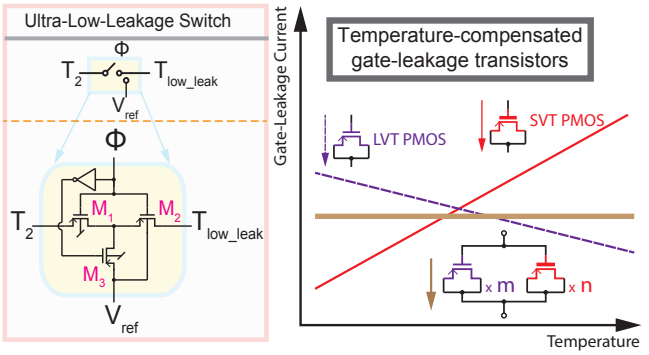

Fig. 4. Circuit schematic of the ultra-low-leakage switch (left) used in the oscillator. LVT and SVT PMOS of opposite temperature dependencies are exploited to minimize the temperature coefficients of the gate-leakage transistor (right).

III. Circuit Design

A. Capacitor, Gate-Leakage Transistor, and Ultra-Low-Leakage Switch

Frequency accuracy and stability is directly affected by the temperature characteristics of the capacitors employed as charge reservoirs and the effective resistance of the gate-leakage transistors employed as the discharging paths. MIM capacitors have negligible temperature variations, which means the charge reservoirs are stable versus temperature. Meanwhile, gate-leakage shows significant temperature variation [2] [6]. To compensate, SVT and LVT PMOS transistors, which have opposite gate-leakage temperature coefficients, are designed to operate in parallel, thereby minimizing the temperature coefficient of the effective resistors $R_{d,\{p,n\}}$.

Since the proposed oscillator operates at Hz-level frequencies, the absolute currents flowing in the circuit are extremely small, and thus charge leakage through phase-transition switches can significantly impact the oscillator frequency. To minimize this effect, ultra-low-leakage switches are employed [7]. As shown in Fig. 4, PMOSs M_1 and M_2 are on when ϕ is low and thus T_2 and T_{low_leak} are electrically connected. However, when ϕ is high M_1 and M_2 are in the off state while M_3 is on, which is employed to bias the source of M_2 at a voltage, V_{ref}. The low-bandwidth, ultra-low-power amplifiers shown in Fig. 1 then bias the drain of M_2 (T_{low_leak}) at V_{ref}. As a result, M_2's source, drain, and bulk terminals are all biased at the same voltage, therefore minimizing charge leakage by over 68 dB.

B. Comparator

A detailed circuit schematic of the comparator is shown in Fig. 5. The amplifier is biased with gate-leakage transistors to avoid the requirement of a power and area-expensive current bias generator. Since the employed SVT PMOS transistors have PTAT characteristics, the amplifier attains roughly constant g_m and bandwidth, thereby minimizing the otherwise temperature-dependent delay impact on the oscillation frequency.

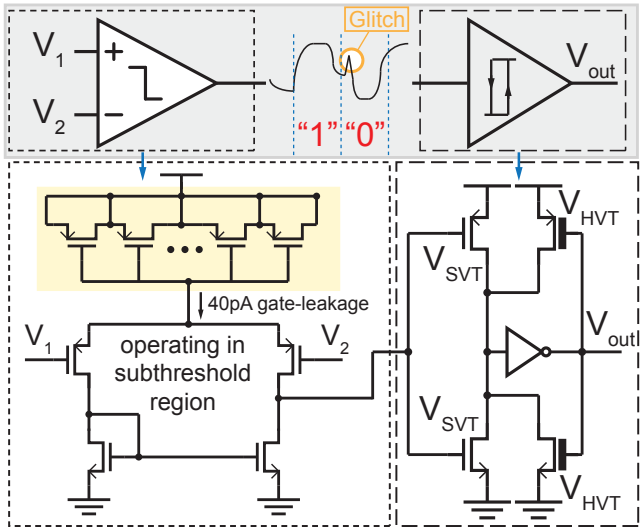

Fig. 5. Detailed circuit schematic of the self-biased comparator using gate-leakage current as bias current (left) and the Schmitt trigger (right) used in the oscillator. Standard-V_t and high-V_t transistors are used in the Schmitt trigger.

To prevent glitches that nominally occur at the output of the comparator between phase transitions, a Schmitt trigger is employed as the first buffer stage after the comparator. As shown in Fig. 5, the transitioning threshold voltage from high to low, $V_{th,high2low}$, and the transitioning threshold voltage from low to high, $V_{th,low2high}$, are now purposely mismatched to each other, thus resulting in a hysteresis voltage of approximately tens of millivolts.

IV. Experimental Results

To validate the performance of the proposed topology, the oscillator is implemented in a 65 nm CMOS process. A die photo is shown in Fig. 6. The capacitive-discharging oscillator occupies an area of 0.0255 mm^2 and oscillates at 2.8 Hz. Capacitors $C_{d,\{n,p\}}$ are sized to be 1.1 pF, and gate-leakage transistors $G_{d,\{n,p\}}$ occupy a total area of 200 μm^2.

Operating from a 0.5 V supply, the proposed oscillator consumes 51 pW at 20 °C including all biasing and peripheral blocks for self-contained oscillator functionality, enabling an ultra low power solution for a frequency-stabilized oscillator in the Hz-range. Although the topology does not employ any temperature-stabilized current or voltage references, it still achieves a voltage accuracy of ±1.9 % and ±3.5 % at ±10 mV and ±20 mV offset, respectively, thereby enabling relaxed supply regulation requirements. The temperature performance of the oscillator is shown in Fig. 7. From -40 °C to 60 °C, the oscillator shows an ability to achieve a frequency variation of as low as 937 ppm/°C.

Throughout the temperature range from -40 °C to 60 °C, the measurement result shows that the oscillator consumes 16-129 pW as shown in Fig. 7. The oscillator achieves an Allan deviation floor under 500 ppm at room temperature, thereby indicating its ability to accurately sleep for long periods of

TABLE I
COMPARISON WITH STATE-OF-THE-ART HZ-RANGE OSCILLATORS THAT CAN BE EMPLOYED AS ACCURATE LONG-TERM TIMERS

Hz-Range Timers	[3] CICC'07	[2] ISSCC'09	[4] ISSCC'11	**This Work**	
Process	130 nm	130 nm	130 nm	**65 nm**	
Area [μm^2]	480	19,000	15,300[a]	**25,500**	
Frequency [Hz]	0.09	11.11	$\sim$ 5	**2.8**	
Power [pW]	120[b]	150[c]	660	**51**	
Temperature Accuracy [ppm/^{o}C]	1600	490	31	**937**	
Temperature Range [$^\circ$C]	0 to 80	0 to 90	-20 to 60	**-40 to 60**	
Supply Sensitivity	$\pm$7.5% @$\pm$50 mV Offset	+4%/-2% @$\pm$50 mV Offset	N/A	**$\pm$1.9%** @$\pm$10 mV Offset	**$\pm$3.5%** @$\pm$20 mV Offset
Allan Deviation Floor	N/A	N/A	N/A	$<$ **500 ppm**	

[a] The area of the Timer and Controller is 10,500 μm^2 and 4,800 μm^2, respectively.
[b] Operates at 450 mV.
[c] 100 pW when refreshed every 4 minutes.

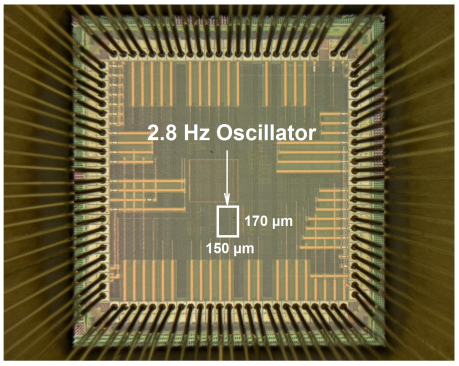

Fig. 6. Micrograph of the proposed capacitive-discharging oscillator.

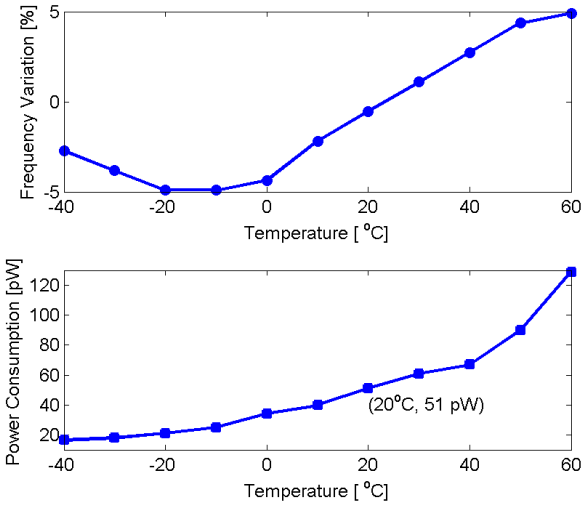

Fig. 7. Measured frequency (top) and measured power consumption (bottom) versus temperature of the proposed oscillator.

time. Table I summarizes these results and compares to current state-of-the-art.

V. CONCLUSIONS

This paper has proposed a capacitive discharging gate-leakage oscillator architecture that can be employed as an accurate long term timer. By pre-charging two capacitors to V_{DD}, and then allowing one to discharge through an effective resistor implemented by gate-leakage transistors that are temperature compensated, an accurate clock period is generated independent of V_{DD} and is suitable for low frequency timers occupying a small active area. Operating from a 0.5 V supply, the proposed oscillator works at 2.8 Hz consuming 51 pW.

VI. ACKNOWLEDGMENT

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