A Near-Optimum 13.56 MHz Active Rectifier with Circuit-Delay Real-Time Calibrations for High-Current Biomedical Implants

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***Abstract* — This paper presents a 13.56MHz active rectifier with enhanced power conversion efficiency (PCE) and voltage conversion ratio (VCR) for high-current biomedical implants. Near-optimum operation with compensated circuit delays is achieved by the proposed real-time NMOS on/off calibrations, which minimize the reverse current and maximize the transistor conduction time under various process, voltage, temperature and loading conditions. Adaptive sizing (AS) is also introduced to optimize the PCE over a wide loading range. Measurements in TSMC 65nm show more than 36% and 17% improvement in PCE and VCR, respectively, by the proposed techniques. With 2.5V input amplitude, the rectifier achieves a peak PCE of 94.8% with an 80Ω loading, a peak VCR of 98.7% with a 1kΩ loading, and a maximum output power of 248.1mW.**

***Index Terms* — Active rectifier, wireless power transfer, biomedical implants, circuit delays, real-time calibrations, reverse current, conduction time, adaptive sizing, power conversion efficiency, voltage conversion ratio**

I. Introduction

Wireless power transfer (WPT) is widely used as a battery-less solution for biomedical implants, such as retinal prostheses, cochlear implants and neural recording, due to the elimination of bulky and replacement-required batteries. For these applications, usually 10 to 100mW or even higher power are required to enable more functions and processing power [1], [2]. High power conversion efficiency (PCE) of the receiver is thus important to avoid reaching the human tissue specific absorption rate (SAR) and obtain high overall system efficiency. Fig.1 shows the system diagram of a generic WPT system for biomedical implants. The received AC voltage is firstly converted to a DC voltage by an active rectifier, and then regulated to supply the biomedical functional circuits. For the rectifier, the PCE and the voltage conversion ratio (VCR) are important as part of the receiver efficiency and to ensure proper operation under loosely coupled conditions. Circuit delays in the control path of the active power transistors, which introduce reverse current loss and shorten the conduction time, are one of the critical barriers to achieve high PCE and VCR. To the best of the authors' knowledge, there are still no universal solutions to compensate the delays under various process, voltage, temperature (PVT) and loading conditions.

In this work, both NMOS on and off calibrations are proposed to make sure the rectifier always operates at near-optimum conditions with circuit-delay elimination under different PVT corners and loadings, so that both PCE and VCR are significantly improved. NMOS adaptive sizing (AS) is also introduced for PCE optimization over a wide loading range. The paper is organized as follows. Section II discusses the importance of circuit-delay issues and reviews the literature. Section III describes the proposed techniques in detail with illustrations and simulations. Measurement results are provided in Section IV. Finally conclusions are given in Section V.

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II. Discussions on Circuit-Delay Issues

A. Circuit-Delay Issues

As shown in Fig. 2 (a), at ideal case with optimum operation, no circuit delays exist thus the conduction time T_{COND} is maximized to deliver power to the output while no reverse current degrades the efficiency. However, reality is cruel and the world is not perfect. Circuit delays in ns range exist in comparators, power transistor buffers and other logics, especially considering offsets and post-layout parasitics. T_{COND} is shortened and reverse current is introduced, as shown in Fig. 2 (b). PCE degrades rapidly by around 30% with the increase of circuit delays from 0 to 4ns, as shown in Fig. 2 (c) simulated with an input amplitude |VIN| of 2.5V and a 200Ω load. Circuit delays are highly dependent on PVT conditions, and compensation is required to maintain high PCE under different conditions and maximize VCR with a heavy load.

B. Literature Review

In terms of off-delay compensation, constant offsets are applied to the comparator by either unbalanced currents [2]-[4] or input transistors [5], which help with only specific conditions, while significant inaccuracy would occur over

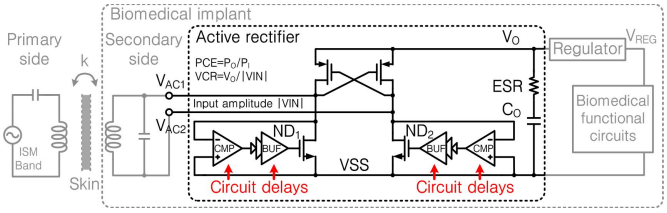

Fig. 1. A generic WPT system for biomedical implants

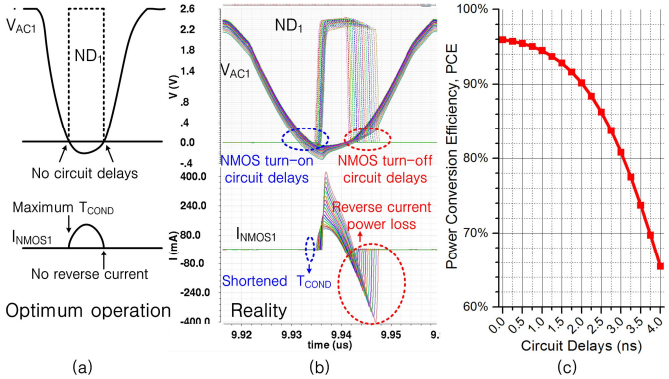

Fig. 2. Circuit-delay issues illustration of an active rectifier. (a) The Optimum operation; (b) simulation waveforms and (c) PCE degradation with 0-4ns overall circuit delays inserted.

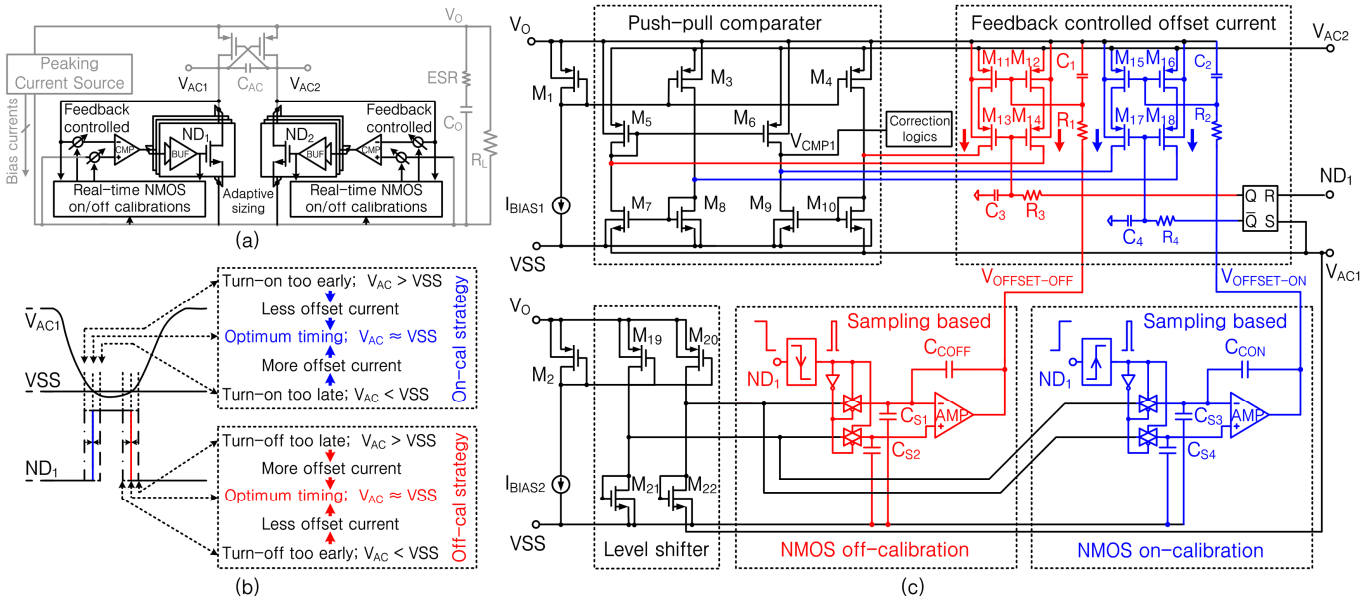

Fig. 3. (a) System diagram of the proposed rectifier, (b) the strategies and (c) the detailed circuitry of the real-time on/off calibrations for one side of rectifier.

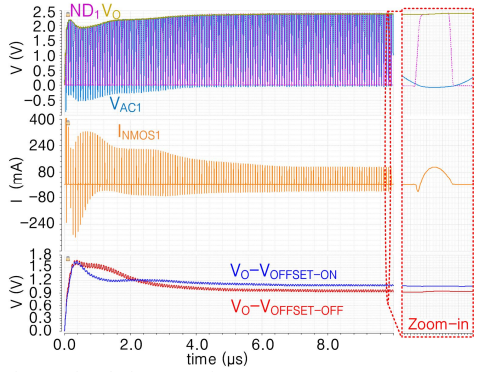

Fig. 4. Simulation waveforms at start-up.

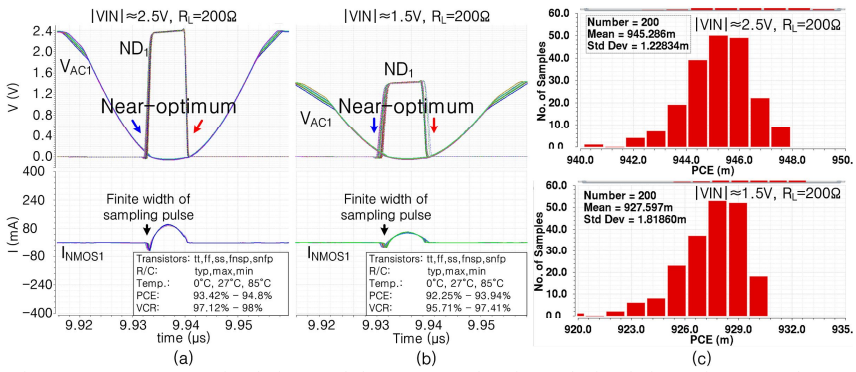

Fig. 5. (a) PVT corners simulations and (b) Monte Carlo mismatch simulations of 200 samples.

different PVT corners. Time-varying offsets are applied to the comparator for better matching with different voltages in [1] [6], while still depends on the accuracy of the process model and suffers from process and temperature variations. [1]-[3], [5], [6] only compensate the off-delay, while a constant offset is applied in [4] to compensate the on-delay to lengthen the $T_{COND,}$ with the accuracy also suffers from PVT variations. As a conclusion, there are still no universal solutions to ensure optimum operation under PVT conditions, and PCE and VCR are still not well optimized. [7] introduced a sampling based feedback loop to calibrate the circuit delays for fully-integrated 100MHz switching converters, which shows a great potential to be employed and adapt with this application.

III. Proposded Near-Optimum Active Rectifier

A. Real-Time NMOS On/Off Calibrations

The V_{AC} signals contain the information whether the active diodes (NMOS in this work) are turned on/off too early, late or at the optimum timing. So by sampling the V_{AC} when the NMOS turn-on/off and building negative feedback loops to adjust the NMOS on/off timing, the circuit delays can be calibrated. Fig. 3 shows the system diagram of the proposed rectifier, the strategies and detailed circuitry of the on/off calibrations for one side of the rectifier. It contains a push-pull comparator (M_3-M_{10}), with the on and off offset currents (M_{15}-M_{18} and M_{11}-M_{14}) controlled by two separate feedback loops. Take the off-calibration as an example, a sampling pulse is generated from the falling edge of the NMOS gate-drive signal ND_1 and samples the level-shifted V_{AC1} and VSS. The signals are then held by C_{S1} and C_{S2} and fed to an error amplifier for comparison. A DC voltage $V_{OFFSET-OFF}$ is then generated by the amplifier to control the offset currents. If the V_{AC1} is larger/smaller than the VSS which indicates the NMOS turns off too late/early, the $V_{OFFSET-OFF}$ is decreased/increased to allow more/less offset current to turn off the NMOS earlier/later, as shown in Fig. 3 (b) and (c). In this way, a negative feedback loop is formed to finally pull the sampled V_{AC1} equals to VSS, which indicates the optimum NMOS turn-off timing. The NMOS on-calibration works in a similar way with a reverse polarity. The on/off offset currents are switched accordingly by ND_1, and R_3, R_4 and C_3, C_4 are used to smoothen the transitions. R_1, R_2 and C_1, C_2 are used as low-pass filters for a better supply noise rejection for the offset currents. Low power current-mirror amplifiers are good enough for these calibrations since bandwidth and gain are not important here. Some correction logics after V_{CMP1} are implemented to filter high-frequency noises brought by

parasitic package bondwire inductors and avoid potential multiple-pulsing. Overall there are four calibrations in the rectifier, two for both sides. As a result, with the help of the real-time on/off calibrations, the rectifier is able to reach near-optimum operation, with minor errors introduced by the finite width of the sampling pulses that the NMOS are turned on/off slightly earlier than the most optimum timing, and the impact in terms of PCE and VCR is ignorable. Fig. 4 shows the start-up of some critical signals for the calibrations. The rectifier reaches near-optimum steady-states after several µs.

To verify the capability of maintaining near-optimum operation under different conditions, PVT corners and Monte-Carlo mismatch simulations are performed, as shown in Fig. 5. With the help of the proposed real-time on/off calibrations, the rectifier always works at near-optimum conditions with on/off delay compensated, and a relatively high PCE and VCR under various PVT corners are achieved.

B. Transistor Sizing Optimization

In this design, NMOS are used as active diodes due to the higher mobility and efficiency compared to PMOS, and the sizing of passive PMOS are designed much larger than NMOS for smaller on-resistance and better PCE and VCR. The gate capacitance of PMOS does not dissipate power and is contributed as part of the resonant capacitor C_{AC} [6].

Adaptive sizing (AS), which is widely used to optimize the efficiency at different loading conditions for switching converters [7] is also introduced in this design. NMOS are divided into three segments, which represent 1X, 4X and 12X, to adapt with different loadings. The segments are selected manually in this work to demonstrate the merits, with the assumption that the load could indicate the rectifier for its power level, for example, the enabling signals of part of the functioning circuits. The AS strategy is designed as follows: 12X when $R_L \leq 70\Omega$; 4X when $70\Omega < R_L \leq 250\Omega$; 1X when $R_L > 250\Omega$.

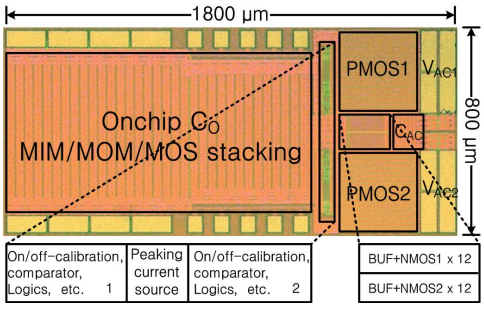

Fig. 6. Chip photo of the proposed active rectifier.

IV. Measurement Results

The chip is fabricated in TSMC 65nm with 2.5/3.3V devices, as shown in Fig. 6. The overall chip area is 1.44mm^2, or 0.46mm^2 if excludes the integrated output capacitors (C_O). Fig. 7 shows the measured waveforms comparison between enabling and disabling the proposed on-calibration (ON-CAL) or off-calibration (OFF-CAL) at |VIN|=2.5V and R_L=200Ω. If the NMOS turn-on too late with delay, V_{AC} dives very negative until NMOS turns on and the T_{COND} is shortened, as shown in Fig. 7 (a) and (c) with ON-CAL off; while if the NMOS turn-off too late with delay, the T_{COND} is longer than necessary and V_{AC} rises above positive, as shown in Fig. 7 (a) and (b) with OFF-CAL off. As shown in Fig. 7(b) and (c), the

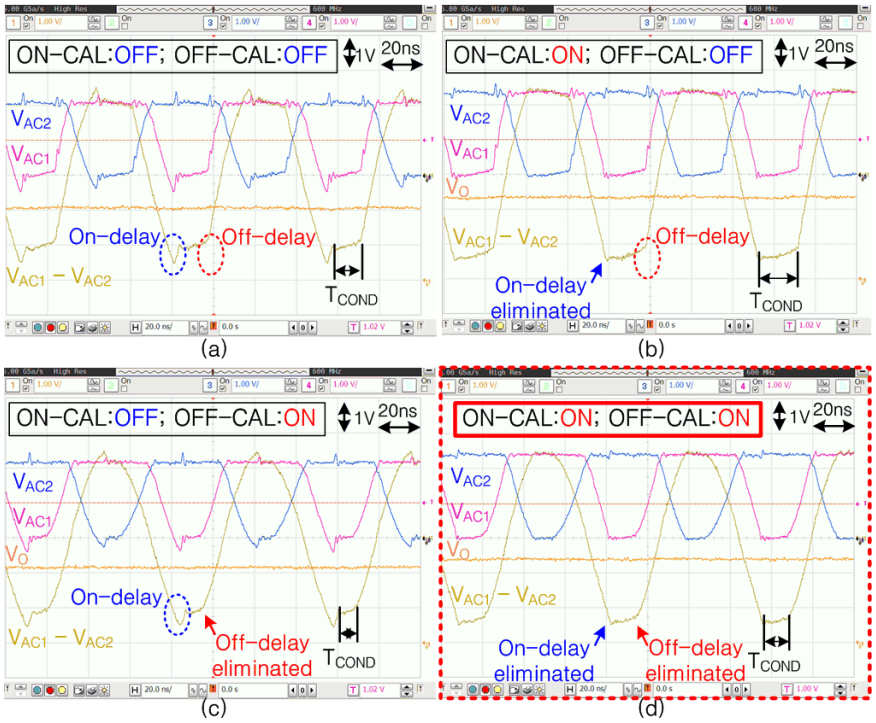

Fig. 7. Measured waveforms of comparisons between (a) all calibrations are disabled; (b) ON-CAL enabled while OFF-CAL disabled; (c) OFF-CAL enabled while ON-CAL disabled and (d) all calibrations are enabled; with the conditions of |VIN|=2.5V, R_L=200Ω and NMOS size of 4X.

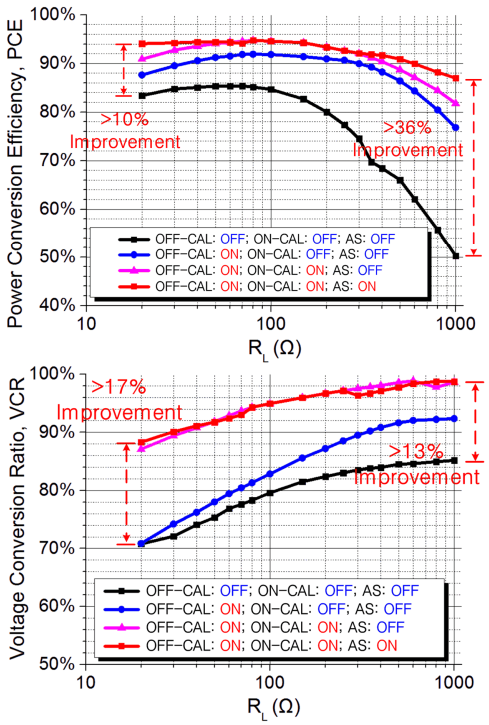

Fig. 8. Measured PCE and VCR improvements after enabling the proposed techniques.

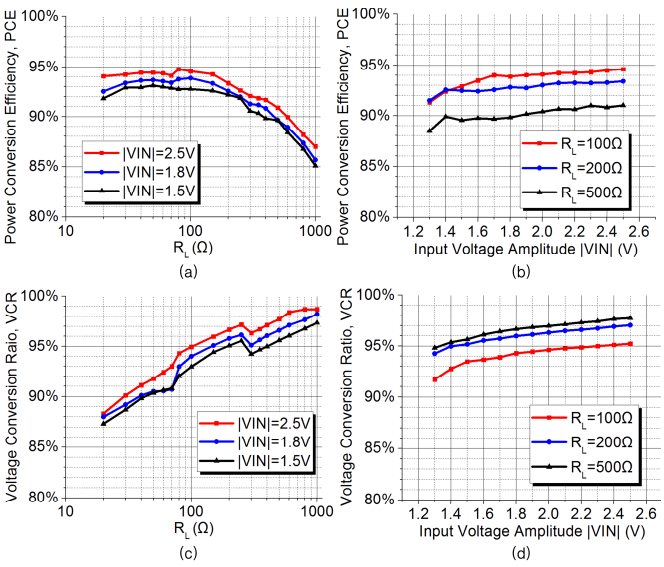

Fig. 9. Measured PCE and VCR characteristics under different conditions.

on/off delays are eliminated accordingly with ON-CAL or OFF-CAL enabled. Both on and off delays are eliminated with near-optimum T_{COND} when on and off calibrations are both enabled, as shown in Fig. 7 (d).

Fig. 8 shows the performance comparison between the proposed techniques enabled and disabled. With the proposed techniques enabled, both PCE and VCR are significantly improved. More than 36% of PCE and 17% of VCR enhancement are observed. The off-calibration is relatively more effective for PCE at light-load with eliminated reverse current loss, while the on-calibration has more contribution for VCR at heavy-load with extended T_{COND} to deliver more power to the loads. Fig. 9 shows more characteristics of the proposed rectifier with different |VIN| and R_L. The PCE and VCR maintain above 90% for most of the cases, and a maximum PCE of 94.8% with 80Ω loading and a maximum VCR of 98.7% with 1kΩ are observed. Comparisons with prior works are shown in Table. I. Both the PCE and VCR are much higher than previous works due to the near-optimum operation under different conditions and the maximum output capability is also larger.

V. Conclutions

In this paper, a near-optimum active rectifier with real-time NMOS on/off calibrations is presented. Thanks to the calibrations, the circuit delays are compensated not only in specific conditions but under various PVT corners. Adaptive sizing is also introduced for better PCE over a wide loading range. Measurement results show more than 36% and 17% improvement in PCE and VCR, respectively, by the proposed techniques. A peak PCE of 94.8%, a peak VCR of 98.7% and a maximum output power of 248.1mW are achieved.

References

[1] Y. Lu, X. Li, W.-H. Ki, C.-Y. Tsui and C. P. Yue, "A 13.56MHz Fully Integrated 1X/2X Active Rectifier with Compensated Bias Current for Inductively Powered Devices," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2013, pp. 66-67.

[2] S. Guo and H. Lee, "An efficiency-enhanced CMOS rectifier with unbalanced-biased comparators for transcutaneous-powered high-current implants," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1796-1804, Jun. 2009.

[3] Y.-H. Lam, W.-H. Ki and C.-Y. Tsui, "Integrated low-loss CMOS active rectifier for wirelessly powered devices," *IEEE Trans. Circuits Syst. II Express Briefs*, vol.53. no. 12, pp. 1378-1382, Dec. 2006.

[4] H.-M. Lee and M. Ghovanloo, "An integrated power-efficient active rectifier with offset-controlled high speed comparators for inductively powered applications," *IEEE Trans. Syst. I Regul. Pap.*, vol. 58, no. 8, pp. 1749-1760, Aug. 2011.

[5] H.-K. Cha, W.-T. Park and M. Je, "A CMOS rectifier with a cross-coupled latched comparator for wireless power transfer in biomedical applications," *IEEE Trans. Circuits Syst. II Express Briefs*, vol 59, no. 7, pp. 409-413, Jul. 2012.

[6] Y. Lu and W.-H. Ki, "A 13.56 MHz CMOS active rectifier with switched-offset and compensated biasing for biomedical wireless power transfer systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 3, pp. 334-344, Jun. 2014.

[7] C. Huang and P. K. T. Mok, "An 84.7% efficiency 100-MHz package bondwire-based fully integrated buck converter with precise DCM operation and enhanced light-load efficiency," *IEEE J. Solid-State Circuits,*vol. 48, no. 11, pp. 2595-2607, Nov. 2013.

[8] S. S. Hashemi, M. Sawan and Y. Savaria, "A high-efficiency low-voltage CMOS rectifier for harvesting energy in implantable devices," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 4, pp. 326-335, Aug. 2012.

[9] H. Chung, A. Radecki, N. Miura, H. Ishikuro and T. Kuroda, "A 0.025-0.45 W 60%-efficiency inductive-coupling power transceiver with 5-Bit dual-frequency feedforward control for non-contact memory cards," *IEEE J. Solid-State Circuits,*vol.47, no. 10, pp. 2496-2504, Oct. 2012.

Table I. Comparison With Prior Art

	[3] TCAS-II 06	[2] JSSC 09	[4] TCAS-I 11	[5] TCAS-II 12	[8] TBCAS 12	[9] JSSC 12	[1]† ISSCC 13	[6] TBCAS 14	**This Work**
Technology	0.35μm	0.35μm	0.5μm	0.18μm	0.18μm	0.18μm	0.35μm	0.35μm	**65nm 2.5/3.3V Devices**
Area	0.107mm²	1.03mm²	0.263mm²	0.009mm²	0.608mm²	0.34mm²	1.42mm²#	0.186mm²	**1.44mm²#**
Freq.	13.56MHz	1.5MHz	13.56MHz	13.56MHz	10MHz	13.56MHz	13.56MHz	13.56MHz	**13.56MHz**
Input Amp.	1.5-3.5V	1.2-2.4V	3.3-5V	0.9-2V	0.8-2.7V	N/A	1.5-4V	1.5-4V	**1.3-2.5V**
Output Volt.	1.2-3.22V (R_L=1.8kΩ)	1.13-2.28V (R_L=2kΩ) 0.98-2.08V (R_L=100Ω)	2.5-3.9V (R_L=500Ω)	0.45-1.78V (R_L=1kΩ)	0.3-2.0V (R_L=2kΩ)	1.2V (load chip)	1.27-3.6V (R_L=500Ω)	1.28V-3.56V (R_L=1.8kΩ) 1.19V-3.52V (R_L=500Ω)	**1.24-2.44V (R_L=500Ω) 1.2-2.39V (R_L=100Ω)**
P_{OUT} (Max.)	5.76mW	43.3mW	30.42mW	3.2mW	2mW	112.5mW	32mW	24.8mW	**248.1mW**
VCR	78%-92% (R_L=1.8kΩ)	94%-95% (R_L=2kΩ) 82%-84% (R_L=100Ω)	76%-81% (R_L=500Ω)	82%-89% (R_L=1kΩ)	60%-89% (R_L=2kΩ)	N/A	85%-90% (R_L=500Ω)	87.3%-93% (R_L=1.8kΩ) 79%-89% (R_L=500Ω)	**94.8%-97.7% (R_L=500Ω) 91.7%-95.2% (R_L=100Ω)**
PCE	65%-89%* (R_L=1.8kΩ)	82%-87%* (R_L=100Ω)	68%-80.2% (R_L=500Ω)	60%-81.9% (R_L=1kΩ)	37%-80% (R_L=2kΩ)	93%* (load chip)	81%-84.2% (R_L=500Ω)	82.2%-90.1% (R_L=500Ω)	**91.3%-94.6% (R_L=100Ω)**

* Simulation results.
† Compared with 1X structure.
# Integrated output capacitor C_O included.