A 4mW Wide Bandwidth Ring-Based Fractional-N DPLL with 1.9ps$_{\mathrm{rms}}$ Integrated-Jitter

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***Abstract*—In this paper, a ring oscillator based fractional-N DPLL that achieves low jitter by extending bandwidth using noise cancellation techniques is presented. A dual-path digital loop filter architecture is employed to resolve the $\Delta\Sigma$ DAC quantization noise challenge. Fabricated in 65nm CMOS process, the proposed PLL operates over a wide frequency range of 4GHz-5.5GHz and achieves 1.9ps$_{\mathrm{rms}}$ jitter while consuming only 4mW. The measured in-band phase noise is better than -96 dBc/Hz at 1MHz offset. The proposed FNDPLL achieves wide bandwidth up to 6MHz using a 50 MHz reference. The FoM is -228.5dB, which is at least 20dB better than all reported ring-based FNDPLLs.**

***Index Terms*—DPLL, Fractional-N, ring VCO, DCO, jitter, time amplifier, TDC, fractional divider, DTC.**

I. Introduction

Fractional-N digital phase locked loops (FNDPLLs) offer several advantages compared to their analog counterparts in terms of loop dynamics reconfigurability, scalability to newer process, and smaller silicon area. As a result, they are particularly well suited for variable and flexible high frequency clock generation in server applications and system-on-a-chip (SoC) platforms. In these applications, ring-based clock generators are preferred for their compact area compared to LC-based ones. However, the ring-based voltage controlled oscillators (VCOs) suffers from poor phase noise performance which limits the overall jitter performance of ring-based FNDPLLs.

Fig. 1(a) shows a block diagram of a conventional FNDPLL. The noise from different blocks of the DPLL is filtered out depending on the loop dynamics. For example, time-to-digital converter (TDC) quantization error is low-pass filtered while VCO phase noise is high-pass filtered (see Fig. 1(b)). A wide loop bandwidth is highly desirable, so that the poor phase noise of ring VCO can be tolerable. However, quantization error introduced by TDC, digital-to-analog converter (DAC), and fractional divider severely degrades the FNPLL jitter performance as shown in Fig. 1(c). Conventional techniques to minimize these quantization errors are usually power and area-consuming [1]–[6]. A conventional delay-line TDC occupies considerable amount of area and power to achieve the required input dynamic range . Instead of using a conventional delay-line TDC as in [7], an embedded TDC can be realized using multiple phases of the ring VCO to save power and area [1], [2]. Phase interpolation can be used to enhance time resolution [5]. However, achieving fine TDC resolution (<3ps) to get low in-band phase noise performance and effective fractional divider quantization noise cancellation is very challenging and comes at the expense of a large power penalty. Furthermore,

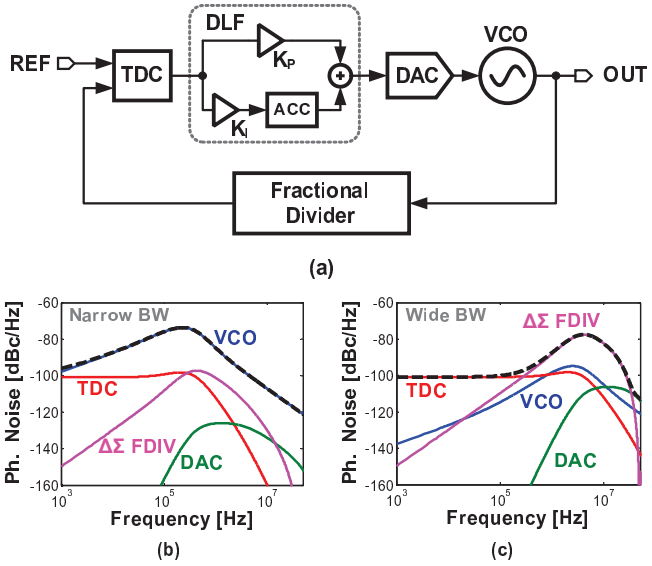

Figure 1. (a) Block diagram of the conventional fractional-N DPLL. Phase noise contributions for (b) low- and (c) high-bandwidth.

the quantization noise of DAC represents a real challenge in wide bandwidth DPLLs, as its noise is not sufficiently filtered by the loop especially for large VCO gain (K_{VCO}) associated with ring VCOs. Increasing the $\Delta\Sigma$ DAC clock frequency and noise shaping order can reduce the noise impact at the expense of large power penalty and extra design complexity [1], [4]. As a result, ring-based FNDPLLs have at least 20dB worse figure-of-merit (FoM) than the best reported analog FNPLLs and integer-N DPLLs.

In this paper, we present a wide bandwidth ring-based FNDPLL that achieves low jitter and low power by using highly digital/synthesizable enhancement techniques. The quantization error of TDC and FDIV is suppressed by using a time amplifier (TA) and digital-to-time converter (DTC)-based noise cancellation, respectively [8]. Additionally, a dual-path digital loop filter architecture is used to resolve the DAC quantization noise challenge. This architecture helps also to mitigate limit cycle behavior, typically associated with DPLLs, and achieve wide bandwidth to maximize suppression of ring oscillator phase noise. The effectiveness of proposed techniques is validated by a prototype FNDPLL, which operates over 4GHz-5.5GHz frequency range and achieves 1.9ps$_{\mathrm{rms}}$ integrated jitter while consuming 4mW. Both jitter and power

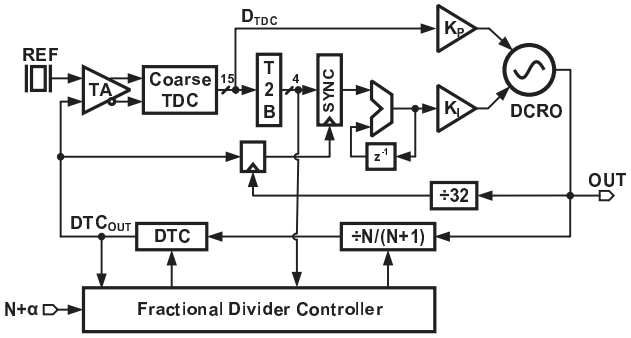

Figure 2. Block diagram of the proposed fractional-N DPLL.

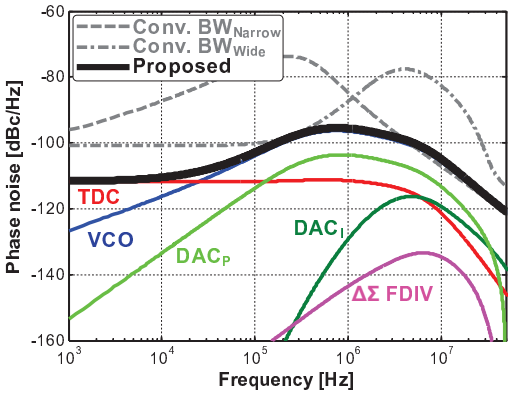

Figure 3. Simulated phase noise plot for the proposed fractional-N DPLL.

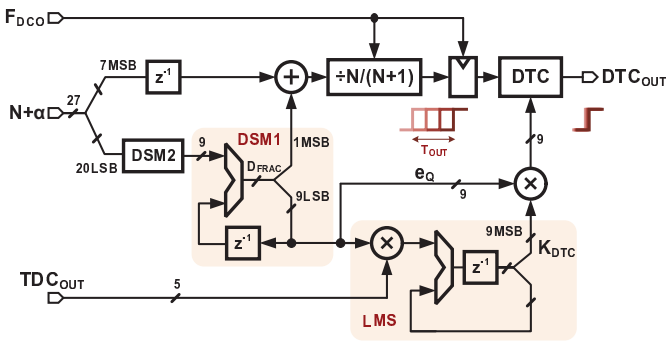

Figure 4. Fractional divider with DTC quantization noise cancellation.

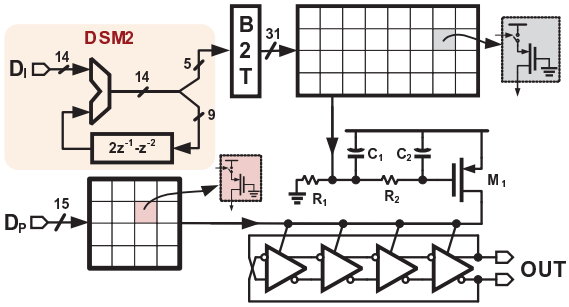

Figure 5. Schematic of the digitally controlled ring oscillator (DCRO).

are the lowest reported as indicated by the FoM of -228.5dB, which is at least 20dB better than previously reported ring-based Fractional-N DPLLs. The rest of the paper is organized as follows. Section II describes the system architecture of the proposed FNDPLL. Section III details circuit design of different circuit blocks. Measurement results of the prototype are presented in section IV. Finally, conclusions are given in section V.

II. System Architecture

Figure 2 shows the block diagram of the proposed fractional-N DPLL. A time amplifier (TA) magnifies the input phase difference ($\Delta\Phi$) between reference and feedback clocks and feeds it to a coarse time-to-digital converter (TDC). The TDC, implemented using simple 4-bit CMOS inverter-based delay line [7], measures the amplified input phase error and digitizes it into 15-level thermometer-coded output (D_{TDC}) with a resolution of 1 inverter delay, which is about 15ps in 65nm CMOS process. However, when referred to the input of the TA, the resolution is improved by the amount of TA gain, about 15 in our implementation, thereby achieving 1ps effective resolution [8]. Type-II response of the PLL is realized by using a proportional-integral loop filter. The scaled TDC output directly controls digitally controlled ring oscillator (DCRO) and implements the proportional control. For the integral control path, the TDC output is converted to 4-bit binary word, which is synchronized to the feedback clock, scaled by K_I and integrated using 18-bit accumulator. Only 14-MSBs of the accumulator output are fed to DCRO to attenuate the amplitude of limit cycle and reduce dithering jitter. Unlike conventional DPLLs which adds the proportional and integral controls in digital domain [1]–[6], the proposed FNDPLL employs a dual path realization of the loop filter which helps reduce dithering jitter by minimizing loop delay.

An N/N+1 multi-modulus divider (MMD), dithered to generate N+α fractional division ratio, divides the DCRO output. Dithering of the divider generates instantaneous phase jumps of at least one VCO period, which are large enough to saturate the TDC and severely degrade the jitter performance. A DTC is used at the output of MMD to mitigate dithering jitter and reduce $\Delta\Phi$ to be within the linear range of TDC [8], [9].

III. Circuit Design of System Blocks

A. Fractional Divider

Figure 4 shows the detailed implementation of the fractional divider. The 7-MSBs of the 27-bit input frequency control word represent the integer part (N) and the remaining 20-LSBs denote the fractional part (α) of the division ratio, N+α. The 20-bit fractional bits are truncated to 9-bits using a 2nd order delta sigma ($\Delta\Sigma$) modulator and accumulated to generate 10-bit output, D_{FRAC}. The average value of the MSBs (D_{FRAC}) is equal to α and can therefore be added to N before controlling the MMD. As a result, MMD is dithered between N and N+1 such that the average division ratio is N+α. The error resulting from truncating 20-bits to 1-bit, denoted as e_Q, appears as phase quantization error at the

output of the MMD. Instead of lowering the PLL bandwidth to suppress e_Q, a DTC is used to cancel it at the MMD output. Because the 9-LSBs of D_{FRAC} represents e_Q, DTC converts them to equivalent phase quantization error and subtracts it from the MMD output. Compared to either using multiple phases [2], [3] or phase interpolator [5], [6], the DTC-based approach offers superior phase noise cancellation and helps extend the PLL bandwidth, which is paramount in reducing the phase noise of DCRO. However, the gain of DTC is PVT-sensitive and therefore must be calibrated using a background least-mean square (LMS) algorithm. To this end, DTC input is scaled based on the correlation between TDC_{OUT}, which contains residual e_Q, and e_Q itself [9]. Multiplying TDC_{OUT} and 9-LSBs of D_{FRAC}, and accumulating the resulting output implements the correlation function (see Fig. 4). Only 9-MSBs were used for DTC gain scaling because of the limited resolution of the DTC, which is 0.5ps in our implementation.

B. Digitally Controlled Ring Oscillator (DCRO)

Figure 5 shows the schematic of the split-tuned DCRO. It is composed of four pseudo differential delay cells connected in ring topology. Each of the delay cells is implemented using two current starved CMOS inverters with a resistor feed-forward coupling for differential operation. The frequency is controlled by the current drawn by the delay cells. The 15-level thermometer-coded TDC output (DP) directly controls the DCRO frequency through a 4-bit current-mode DAC. The cell current can be varied to control the DPLL bandwidth. To reduce hardware complexity of a high resolution DAC, 14-bit integral control word, D_I, is truncated to 5-bits using a 2nd order error-feedback based digital $\Delta\Sigma$ modulator and a simple 31-levels thermometer-coded DAC generates the output control current, which is converted to voltage by resistor R_1. A 3rd order low pass filter with the 3rd pole located at the drain of current source transistor, M1, is used to suppress $\Delta\Sigma$ truncation error. Thanks to the dual path architecture, the bandwidth of the 3rd order low pass filter of the integral path can be lowered less than 1MHz with no stability concerns even for a wide DPLL bandwidth of $F_{REF}/8$.

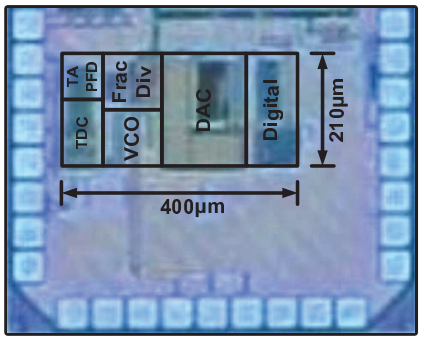

Figure 6. Die micrograph of the fractional-N DPLL.

IV. Measurement Results

The fractional-N DPLL is implemented in a 65nm CMOS technology and occupies an active area of 0.084mm^2. Die micrograph is shown in Fig. 6. It operates from 4GHz to 5.5GHz using a 50MHz reference frequency, and at 5GHz it consumes 4mW from a 0.9V supply. The measured phase noise plots at 5.2GHz output frequency in both integer- and fractional-N modes is shown in Fig. 7. Integrated jitter is about 1.7ps$_{rms}$ in both modes, which illustrates the effectiveness of DTC calibration (jitter increased to 8.9ps$_{rms}$ when the DTC calibration is disabled). Figure 8 (a) shows the measured integrated jitter (1kHz to 100MHz) as a function of the bandwidth. The integrated jitter is less than 2ps$_{rms}$ for bandwidth > 2MHz and increases at lower BW due to less suppression of DCRO phase noise. At 5MHz bandwidth, the integrated jitter is 1.75ps$_{rms}$. Figure 8 (b) plots the measured integrated jitter for different fractional offset frequency where the worst-case jitter is <1.9ps$_{rms}$ across the entire fractional offset frequency range, illustrating a variation of only 150fs.

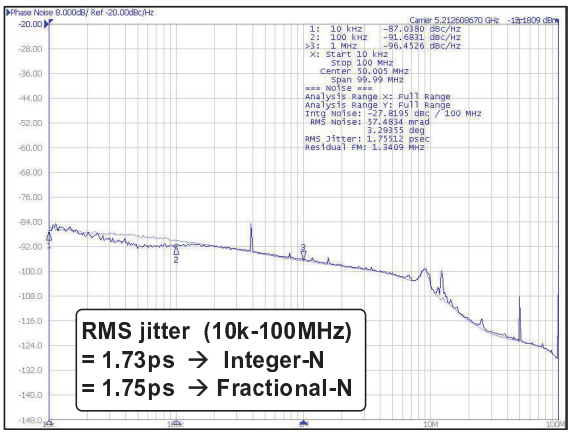

Figure 7. Measured phase noise at 5.2GHz output frequency for integer-N and fractional-N modes. .

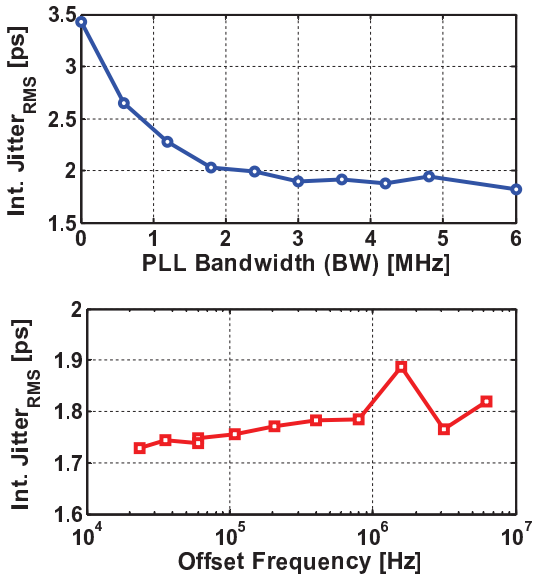

Figure 8. Measured integrated jitter as a function of: (a) PLL bandwidth and (b) fractional output frequency.

The measured reference of the DPLL at 5MHz bandwidth ($F_{REF}/10$) settings is around -44dBc, while the worst case fractional spur is illustrated in the spectrum of DPLL output shown in Fig. 9, it is less than -41.6dBc at 196kHz fractional offset frequency.

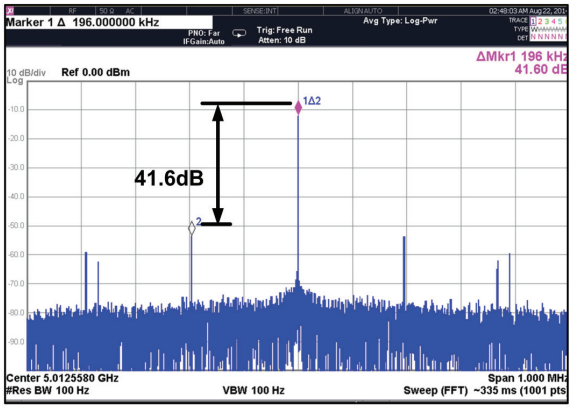

Figure 9. Measured worst case fractional spur of -41.6dBc at 196kHz fractional offset frequency.

Table I compares the measured performance of the proposed fractional-N DPLL with state-of-the-art ring-based fractional-N DPLLs. The proposed DPLL achieves the best FoM of -228.5dB, which is at least 20dB better than other state-of-the-art ring-based designs as shown in Fig. 10. Compared to recently published designs; the proposed design achieves 20dB better in-band noise, while occupying a smaller normalized area, 2X better power efficiency, and 5X lower integrated jitter. The proposed FNDPLL demonstrates the best power efficiency of 0.8mW/GHz while operating from 0.9V supply.

Table I
COMPARISON WITH RECENT DPLL PUBLICATIONS

	[1]	[4]	[5]	[6]	This Work
Technology [nm]	65	22	28	20	65
Supply [V]	1.1-1.3	1	1	0.9	0.9
Output Freq. [GHz]	0.6-0.8	0.6-3.6	0.03-2.0	0.8-1.6	4.0-5.5
Ref. Freq. [MHz]	26	25-200	30	25	50
Power [mW]	3.2	15.4	5.3	3.1	4
BW [MHz]	1	0.003-4	4	5	5
IBPN [dBc/Hz]*	-72.1	-63.6	-75.7	-74.1	-97
RMS Jitter [ps]	21.5	10	19.3	28	1.9
FoM_J [dB]	**-208.3**	**-208**	**-207**	**-206.1**	**-228.5**
P. Eff. [mW/GHz]	**4**	**4.3**	**2.65**	**1.94**	**0.8**
Area [mm^2]	0.027	0.03	0.026	0.012	0.084

*Normalized In-band PN to 5GHz

V. CONCLUSIONS

A wide bandwidth low jitter ring oscillator based fractional-N DPLL is proposed that employs a high resolution TDC, a truly fractional divider, and a dual-path loop filter. The measured integrated jitter is only 1.9ps_{rms}, while the power consumption is less than 4mW from 0.9V supply voltage for an output frequency range 4-5.5GHz. This translates to a best reported FoM of -228.5dB.

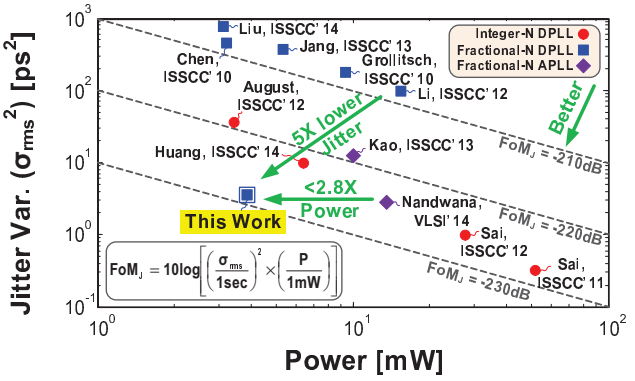

Figure 10. FoM comparison.

ACKNOWLEGMENT

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