A Field-Programmable Noise-Canceling Wideband Receiver with High-Linearity Hybrid Class-AB-C LNTAs

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***Abstract*— A field-programmable noise-canceling wide-band receiver front end with high performance LNTAs is presented. The common-source (CS) and common-gate (CG) LNTAs are split into several cells whose bias point can be individually programmed in class AB or C yielding a highly linear hybrid class-AB-C LNTA. The 40nm LP CMOS receiver prototype can be programmed on the fly to adapt to different RF environments; it was tested in a low noise mode, a high linearity mode and a low power mode. Across these modes, the receiver has maximum gain of 53dB, a minimum NF of 2.2dB, a maximum B_{1dB} of +11dBm, and a maximum OB-IIP_3 of +21dBm ; the signal path consumes between 15 and 40mA from a 2.5V supply and the LO current varies from 2.2 to 20mA from a 1.1V supply across operating frequencies. The measured LO emission at the antenna port is <-84dBm.**

I. Introduction

Modern wireless receivers need to support multiple standards at different frequencies, with varying sensitivity and linearity requirements. The traditional multi-standard radio with multiple narrowband front ends optimized for each band can be replaced with a wideband front end but the linearity requirements become more stringent due to absence of RF band select filters. Recently several wideband solutions have been demonstrated. Mixer first receivers have very high linearity [1], but have limited noise figure (NF). Frequency-translational noise-canceling receivers (FTNC) [2] cancel the noise contribution from the mixer-first path and can achieve a NF <2dB, but their out-of-band linearity is limited by the common-source LNTA. Both solutions also have limited reverse isolation for in-band spurious LO emissions.

The design of wideband highly linear LNTAs remains a critical challenge. A field-programmable architecture is further highly desirable to avoid having to use a worst-case design strategy across all possible required operating conditions and the associated power penalty. We present a wide-band field-programmable receiver using high-linearity hybrid class-AB-C LNTAs in common-source (CS) and common-gate (CG) configurations. Each LNTA is composed of parallel G_m cells whose bias can be individually programmed. With this feature, the receiver can be programmed to work in different modes to optimize NF, linearity and power consumption to adapt to the RF signal environment or standard.

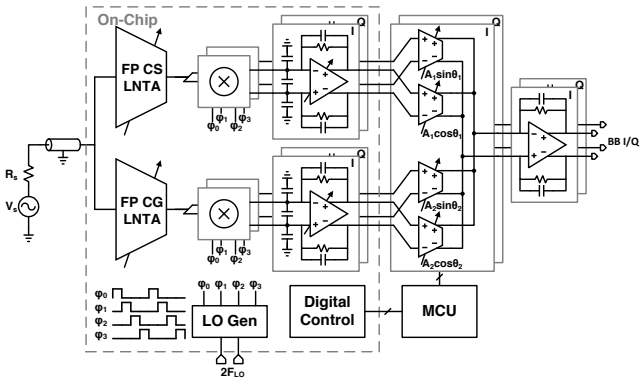


Fig. 1: *Block diagram of the field-programmable frequency-translational noise-canceling receiver using a common-gate and common-source path.*

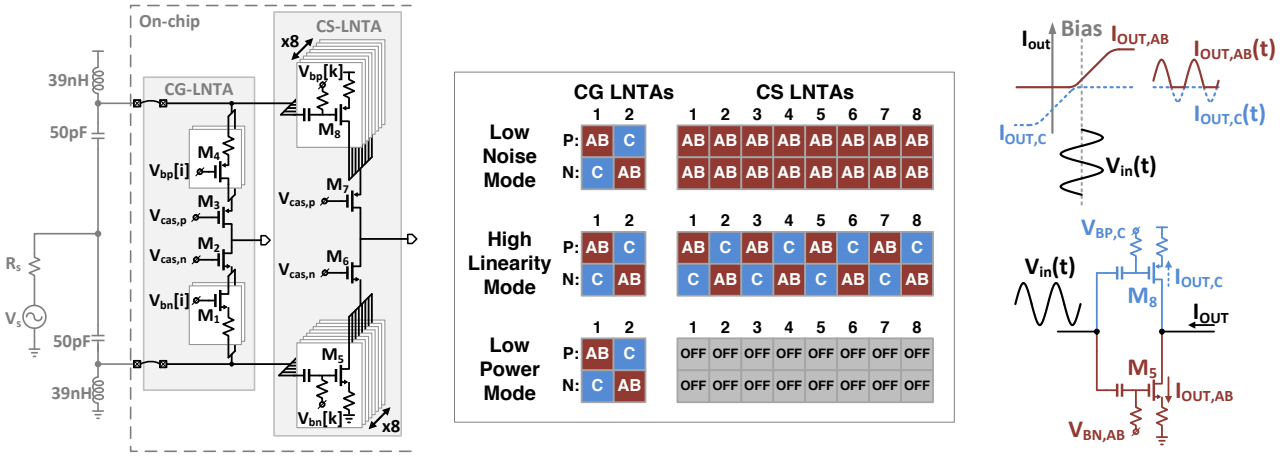
II. Receiver Architecture

The proposed receiver (Fig. 1) uses an FTNC architecture [2], but with the mixer-first receiver replaced with a CG LNTA to achieve wideband input matching with reverse isolation to limit LO leakage. The noise of the CG LNTA is sensed by the CS LNTA and canceled in the complex baseband, and the receiver NF is dominated by the CS LNTA [2]. The programmable CS and CG LNTAs are followed by I/Q single balanced current-driven 4-phase passive mixers. The downconverted current signals are filtered and amplified by TIAs and then combined with appropriate phase and gain adjustments.[1] The I/Q downconversion mixers use 4-phase 25%-duty-cycle clocks generated with a divide-by-2 circuit. The LNTAs are DC coupled to the passive mixers to reduce the load impedance seen by the LNTAs.

III. Field-Programmable High-Performance Hybrid Class-AB-C LNTAs

In the current-reuse CS and CG LNTAs (Fig. 2a) both the NMOS and PMOS contribute to the transconductance of the LNTA. Such complementary topology offers lower noise than a single-transistor transconductor with a current-source load, where the load noise contributes excess noise. This is particularly important for the CG LNTA since it has no current gain due to the input

[1]In our prototype the baseband combiners are realized off-chip for testing flexibility.



(a) (b) (c)

Fig. 2: *(a) Schematic of the CS-CG LNTAs (bias not shown); (b) LNTA bias configurations for the three operation modes tested; (c) the operation of the high linearity mode with an NMOS class-AB G_m cell and a PMOS class-C G_m cell.*

impedance matching constraint. The CG LNTA uses two off-chip choke inductors to provide the DC bias currents with low noise penalty.

The CG LNTA is composed of two parallel G_m cells (30mS each) and the CS LNTA has eight G_m cells (20mS each). Each of the G_m cells can be individually biased with a bias-voltage selection MUX in three different modes: class-AB, class-C and OFF. In class-AB mode the transistor is biased in strong inversion, in class-C mode the transistor is biased in deep weak inversion, and in the OFF mode the $|V_{GS}|$ is set to 0V.

A. Highly Linear Hybrid Class-AB-C Operation

The LNTA linearity is critical for the overall receiver performance and is particularly challenging in wideband designs which typically lack off-chip band-select filters. The LNTAs drive their output current into low input-impedance passive mixers ($R_{IN} < 15\Omega$ @200MHz offset); the out-of-band blocker signals do not undergo voltage gain prior to baseband filtering which helps alleviating LNTA output compression. Fig. 2c shows an NMOS CS G_m cell. When $v_{in}(t)$ goes more than $(V_{GS} - V_{th})$ below its gate bias, the NMOS transistor turns off resulting in hard clipping and strongly non-linear LNTA transfer curves. Using a higher $(V_{GS} - V_{th})$ increases the input swing range but at a cost of a lower g_m/I_D and thus reduced power efficiency.

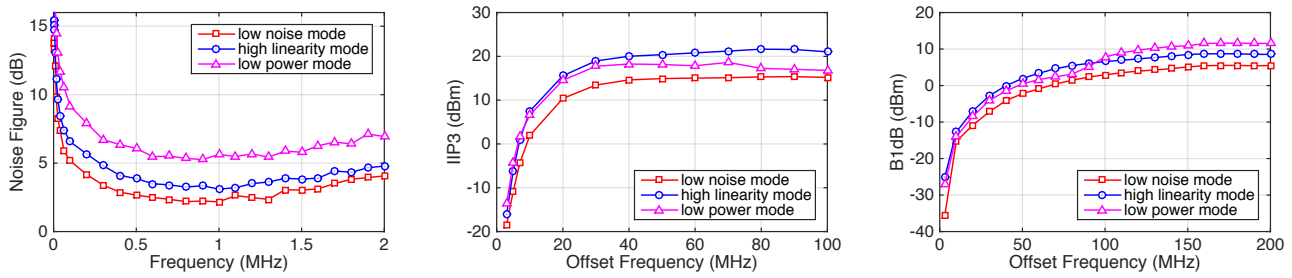
To overcome this limitation, we use a second PMOS CS G_m cell that is biased in Class-C such that it turns on and pushes out current when the NMOS is cut off as shown in Fig. 2c. The combined transfer curve of the NMOS and PMOS G_m exhibits an almost twice as large linear amplification region and the input clipping non-linearity is removed resulting in a significantly higher tolerance to input blocking signals. To reduce even order distortion in the combined transfer curve due to mobility mismatch between NMOS and PMOS cells, source degeneration resistors are used. A degeneration resistor value equal to $1/g_m$ of the transistors offers a good compromise between linearity improvement and noise penalty. All degeneration resistors are of the same type and size; they improve the matching of G_m of the P and N cells across class-AB and class-C operation, improve their small-signal linearity, and reduce the voltage swing on the transistor to half the input swing so that reliability is improved.

The class-AB-C operation also improves small signal 3^{rd}-order linearity as measured by IIP_3. When biased in class-C mode, a CS G_m cell is not completely off but has a small g_m of $50\mu S$. The 3^{rd}-order distortion from the class-C cell has opposite sign of the class-AB cell's and partially cancels its 3^{rd}-order distortions. This cancellation principle is similar to that of the complementary DS method [3], however, the traditional DS method only cancels 3^{rd} order nonlinearity and does not improve compression when higher order nonlinearities become significant. The proposed hybrid class-AB-C technique improves large and small signal linearity at the same time.

Fig. 4 shows the bias voltage generation. The class AB bias is generated with current mirrors. The class-C bias voltage is derived from the class-AB bias voltage and the V_{th} of the NMOS and PMOS cells, which are obtained with large transistors biased with a small constant current. Opamp based adders calculate the overdrive voltage and subtract it from V_{th} to generate the class-C bias voltages. This bias scheme keeps the class-AB and class-C transfer curves robustly aligned across variations in V_{th} and V_{DD}.

B. Field-Programmable Operation

The flexible LNTA architecture has a large number of possible biasing combinations which makes a dynamic



(a) (b) (c)

Fig. 3: *The receiver performance measured with a 900MHz LO for different operation modes: (a) noise figure vs. IF frequency (b) OB-IIP$_3$ vs. two-tone offset frequency (c) B_{1dB} vs. blocker offset frequency*

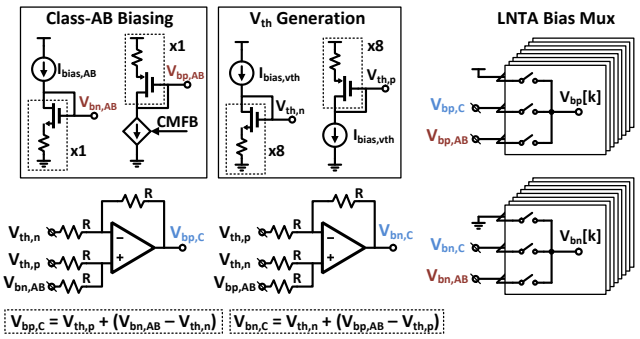


Fig. 4: *Class-AB and class-C bias voltage generation that is robust against PVT variations.*

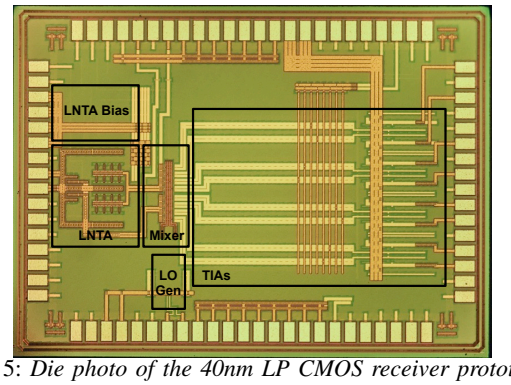


Fig. 5: *Die photo of the 40nm LP CMOS receiver prototype*

tradeoff between LNTA noise and linearity performance and power consumption possible in the field. To maintain balance in the DC bias current, the number of class-AB NMOS cells needs to match the number of class-AB PMOS cells; additionally, if class-C cells are used, their number needs to be matched with an equal number of class-AB cells. In this paper, we focus on three typical modes of operation shown in Fig. 2b. The CG G_m cells are always kept in the hybrid Class-AB + Class-C mode, while the configuration of the CS cells is changed.

Low Noise Mode: When there are no extremely large blockers present and the highest sensitivity is desired, all 8 cells of the CS LNTA are programmed with class-AB bias to maximize the CS branch G_m at the expenses of increased power dissipation.

High Linearity Mode: When large out-of-band blockers appear at the input, the CS LNTA is programmed into a high-linearity mode with half the cells biased in Class-AB and the other half in Class-C to handle the large blocker without compression. The NF degrades slightly due to lower G_m and conversion gain.

Low Power Mode: In a benign RF environment with moderate blockers and a strong desired signal, the CS path can be shut down completely to save power at the cost of an increased NF; in the current implementation the CG path remains configured in the hybrid class-AB-C mode and the receiver linearity remains excellent.

IV. Experimental Results

The 40nm CMOS LP receiver chip has an active area of 1.6mm^2 (Fig. 5). Fig. 3 shows the measured NF, out-of-band IIP$_3$ and B_{1dB} for a 900MHz LO frequency across the three operating modes. The low noise mode has a 2.2dB NF, +15dBm OB-IIP$_3$ and +5dBm B_{1dB} while consuming 49mA. The high linearity mode has a slightly degraded NF of 3dB, but the OB-IIP$_3$ improves to +21dBm, B_{1dB} improves to +8.5dBm and current reduces to 42mA. The low power mode has a higher NF of 5.5dB and a moderate OB-IIP$_3$ of +17dBm; the B_{1dB} of +11dBm is the highest due to the higher blocker tolerance of the CG LNTA. Assuming the CS downconversion path is powered down[2], current consumption reduces to 20mA. The LO path power dissipation depends on LO frequency and is the same for low noise and high linearity modes, but is half for low power mode.

OB-IIP$_3$ measurements have been performed across the 3 modes and exhibit clean 3dB/dB slopes indicating that the linearity improvement is largely independent of signal power and that the IIP$_3$ can be reliably obtained

[2]Our prototype chip does not include the TIA and LO power down circuits, but they can be easily added; current consumption of the low noise mode has been estimated based on the measured TIA and LO path current consumption.

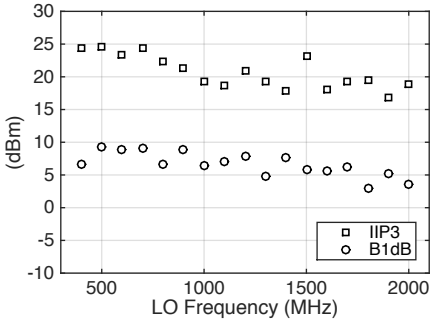


Fig. 6: *OB-IIP$_3$ and B$_{1dB}$ at different LO frequencies, OB-IIP$_3$ measured at 80MHz offset and spacing and B$_{1dB}$ measured for a 200MHz offset*

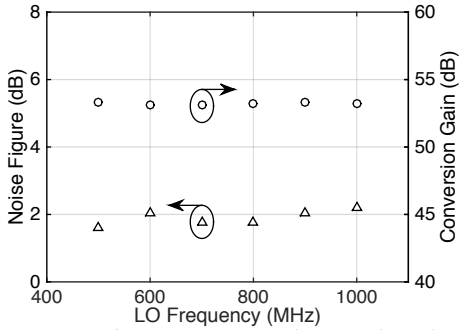


Fig. 7: *DSB NF and conversion gain for LOs from 0.5 to 1GHz*

by extrapolation. Fig. 6 and Fig. 7 show the linearity measurements for the high linearity mode and the NF and conversion gain measurements for the low noise mode across LO frequencies.[3] The baseband complex combiner is reconfigured at each LO frequency for noise cancellation [2] whereas the LNTA biasing does not require calibration.

A key advantage of using a CG impedance matching path instead of a mixer-first path is the significantly reduced LO leakage. The measured LO leakage of our prototype is as low as -84dBm.

Table I summarizes the measured performance, which matches well with the simulated performance in the TT corner, and provides a comparison with the state of the art in wideband receivers and LNTAs. The presented design has comparable linearity to [1] but better NF. The designs in [2], [4], [5] have slightly better NF, but this work has much higher blocker tolerance and IIP$_3$. The LNTA in [6] has a very high measured blocker tolerance, but the LNTA presented here demonstrates similar linearity with much lower NF. This prototype is designed in a CMOS LP technology and a high V_{DD} is used to provide more headroom over the large V_{th}.

Note that the other designs are fixed whereas the field-programmability of the presented design further allows to adapt to the RF signal environment, and switch to a low power mode when extreme noise or linearity performance is not needed.

[3]NF measurements for higher frequencies are ongoing.

TABLE I
MEASUREMENT SUMMARY AND COMPARISON TO THE STATE OF THE ART

Design Type	Field-Programmable RX			Wideband RX				LNTA
Reference	This Work			[1]	[2]	[4]	[5]	[6]
	Low Noise	High Linearity	Low Power					
CMOS Technology	40nm			65nm	40nm	28nm	40nm	65nm
Frequency (GHz)	0.4-2.0			0.05-2.4	0.3-2.9	0.4-6	0.1-2.8	1.5-2.0
Max Gain (dB)	53	47	47	80	58	70	50	100mS
NF (dB)	2.2	3	5.5	5.5	1.9-2.1	1.8	1.8	6.5
OB IIP3 (dBm)	+15	+21	+17	+27	+12	+5	+3	+20
B1dB-CP (dBm)	+5	+8.5	+11	+5**	0	0	N/R	+8
LO Leakage (dBm)	-84.6	-85.6	-84.2	N/R	N/R	N/R	-82	N/R
Analog Current (mA)	39.9	32.8	15.0	12	24	20.4	24	7.5
LO Current (mA)	4.4-20	4.4-20	2.2-10	6-33	3-36	1.6-23.6	0.5-12.2	N/R
Power Supply (V)	2.5(Analog)/1.1(LO)			1.2(LO) / 2.5(BB)	1.3	0.9	1.1	1.5

N/R = Not Reported **Estimated

V. CONCLUSIONS

The proposed field-programmable wide-band noise-canceling receiver achieves a minimum NF of 2.2dB, a maximum B$_{1dB}$ of +11dBm, max OB-IIP$_3$ of +21dBm while keeping LO leakage <-84dBm. The high linearity stems from the use of hybrid class-AB-C CG and CS LNTAs. The ability to dynamically trade off noise and linearity performance with power consumption in the field makes it a promising candidate for multi-standard software defined radios.

ACKNOWLEDGMENTS

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