A 16nm Configurable Pass-Gate Bit-Cell Register File for Quantifying the V_{MIN} Advantage of PFET versus NFET Pass-Gate Bit Cells

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***ABSTRACT* — A 16nm configurable pass-gate bit-cell register file allows a direct comparison of NFET versus PFET pass-gate bit cells for early technology evaluation. The configurable pass gate enables either a transmission-gate (TG), an NFET pass gate, or a PFET pass gate. From silicon test-chip measurement, the register file with PFET pass-gate bit cells achieves a 33% minimum supply voltage (V_{MIN}) reduction in a 16nm FinFET technology and a 40% V_{MIN} reduction in an enhanced 16nm FinFET technology as compared to a register file with NFET pass-gate bit cells. Test-chip measurements highlight the superior benefits of the PFET drive current relative to the NFET drive current at low voltages. The V_{MIN} improvement with a PFET pass-gate bit cell represents a paradigm-shift from traditional CMOS circuit-design practices.**

I. Introduction

Since the advent of CMOS technology, the NFET historically provides a superior drive current relative to the PFET due to the larger effective carrier mobility for electrons as compared to holes. As a result, circuit designs traditionally employ NFETs for performance-critical transistors such as the evaluation path in dynamic logic or the pass gates in a memory bit cell. The integration of strained silicon in the transistor channel significantly enhances the carrier mobility in both PFET and NFET transistors, resulting in higher saturation drain currents (I_{DSAT}). Strained silicon techniques for the PFET aim to apply compressive stress (i.e., squeezing atoms) in the channel such as embedded source/drain stressors (e.g., SiGe) [1]. In contrast, strained silicon engineering for the NFET targets tensile strain (i.e., stretching atoms) in the channel. Examples include stressed metal gates [1], stressed over-layers, or stress memorization technique [2]. Transistor measurements [1]-[2] demonstrate that compressive stress enhances the PFET I_{DSAT} more than the tensile stress benefits the NFET I_{DSAT} [1]. Since the integration of strained silicon, technology trends indicate a significant improvement in the PFET I_{DSAT} as compared to the NFET I_{DSAT} (Fig. 1) [3]-[23]. At the 14/16nm node, the PFET I_{DSAT} is nearly equal to, or in the case of one foundry, larger than the NFET I_{DSAT}. This trend significantly affects circuits that depend on the ratio of PFET and NFET I_{DSAT} strengths, including an SRAM or register-file bit cell.

In this paper, a register file with configurable pass-gate bit cells is designed and implemented in two 16nm FinFET CMOS technologies [9], [24] to evaluate the PFET and NFET pass-gate bit cells. As technology scaling continues, the comparison of NFET versus PFET pass-gate bit cells from early test-chip measurements enables critical insight toward designing the SRAM and register-file bit cells for a production system-on-chip (SoC) processor. Although SRAM caches and processor cores can operate on separate supply voltage (V_{DD}) rails to mitigate the impact of cache V_{DD} scaling on the core V_{MIN}, register-file circuits often limit the core V_{MIN}. Thus, improving the register-file V_{MIN} typically enhances the core V_{MIN} scaling, and consequently, the overall core energy efficiency.

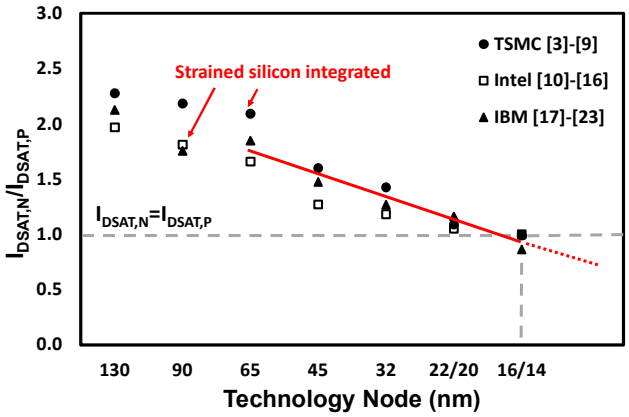


Figure 1. The ratio of NFET to PFET saturation drain current across technology nodes for three semiconductor foundries.

II. Configurable Pass-Gate Bit-Cell Register File

The configurable pass-gate bit cell (Fig. 2) consists of 10 transistors and decouples the read and write ports. The two NFETs in the read path are sized to 5 fins to ensure the write operation limits the bit-cell V_{MIN}. The remaining 8 transistors includes the back-to-back inverters and the configurable pass gate as an experimental feature. The configurable pass gate enables either a combined NFET and PFET transmission gate (TG), an NFET-only pass gate, or a PFET-only pass gate. All 8 transistors consist of 2-fin devices with the same target gate length and threshold-voltage type. Thus, the bit cell does not favor either the NFET or the PFET pass-gate options.

For an SRAM array which has many more wordlines (WLs) than bitlines (BLs), an SRAM bit-cell layout uses only two poly pitches. The narrow and long bit-cell layout minimizes the WL dimension to reduce the BL capacitance and provide an effective aspect ratio for the SRAM array. A typical

register-file array, however, contains fewer WLs than BLs, thus the register-file bit-cell layout employs four poly pitches for a lower WL capacitance and an effective aspect ratio. The configurable bit-cell (Fig. 2) layout uses four poly pitches. Since the two NFETs in the read path occupies only two poly pitches, these NFETs in two adjacent bit cells share the four poly pitches to minimize the effective layout area. The area of the configurable bit cell is 0.204µm^2 in a 16nm FinFET technology. As a comparison, the layout of a conventional NFET only pass-gate bit cell is illustrated in Fig. 3 (a). The area of this bit cell with a fin width of pull up (PU): pull down (PD): pass gate (PG) =1:3:3 is 0.190µm^2. Since the register-file bit-cell layout uses four poly pitches, the PFET only pass-gate bit-cell layout with a fin width of PU: PD: PG=3:1:3 (Fig. 3 (b)) consumes the same area as the NFET only pass-gate bit cell.

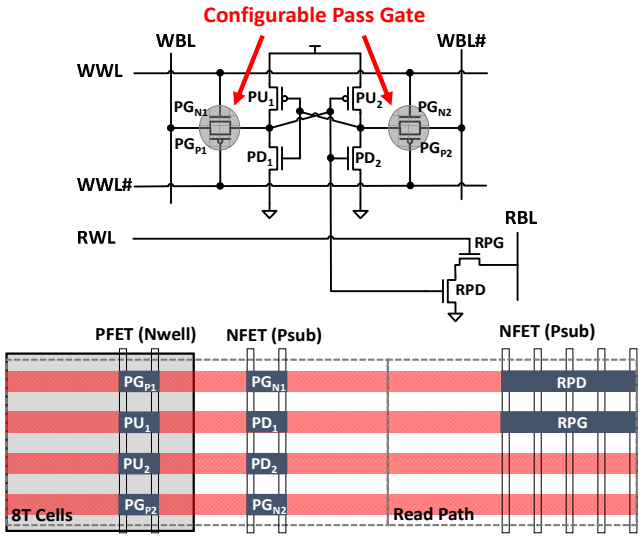


Figure 2. Configurable pass-gate bit cell schematic and layout to enable either a transmission gate, an NFET pass gate, or a PFET pass gate in a register file for logic process.

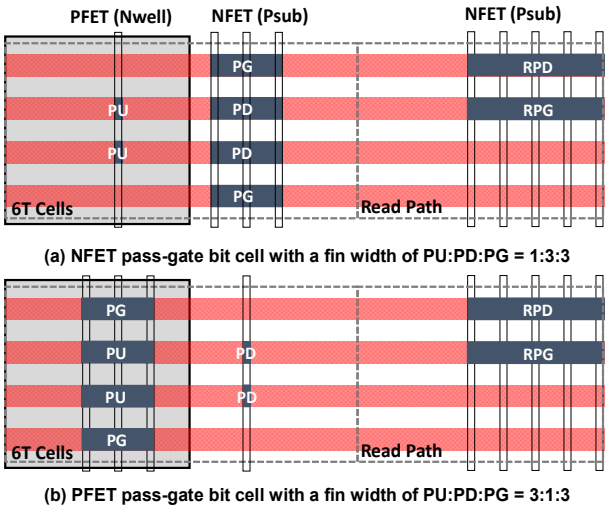


Figure 3. Layout of (a) the NFET pass-gate bit cell and (b) the PFET pass-gate bit cell in a register file for logic process.

The register file (Fig. 4) contains an array of bit cells with 32 rows and 56 columns. A control circuit generates the write wordline (WWL) and the write wordline complement (WWL#) signals for each row in the array based on the selected data from an X decoder as well as the WWL enable (WWL_en) and WWL# enable (WWL#_en) bits. JTAG scan controller programs the WWL_en and WWL_en# bits for configuring the bit-cell pass-gate design. The register-file area is 2,868µm^2. The test chip (Fig. 5) integrates six of the register files for a total of 11Kb per die in two 16nm FinFET technologies [9], [24].

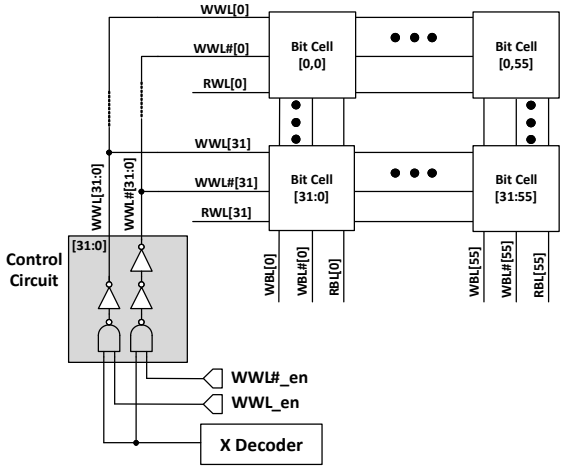
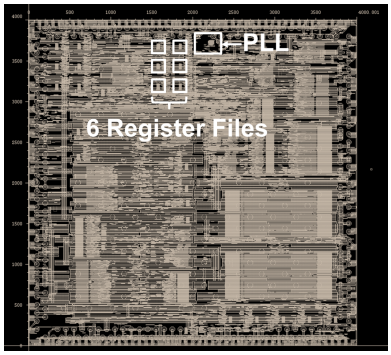


Figure 4. Block diagram of bit-cell array and control circuits.



Technology	16nm FinFET CMOS
Die Area	16mm^2
Register File Configuration	32 word x 56 bit
Register File Area	2,868µm^2
Total Capacity	11Kb (6 x Register File)

Figure 5. Test-chip die micrograph and characteristics.

III. Measurement Results

Silicon measurements of the die failure probability distribution (Fig. 6) highlight the V_{MIN} differences between configuring the pass gate as a TG, an NFET pass gate, or a PFET pass gate in a 16nm technology. The data is from 375 dies across four typical wafers for a total of 4Mb. In comparing the NFET and PFET pass-gate configurations, the

PFET pass gate provides a 33% V_{MIN} reduction as compared to the NFET pass gate at 95% yield. Moreover, the die failure probability distributions for the PFET pass gate and the TG are nearly equal, thus the NFET contribution to the TG is negligible when writing the bit cell at low voltages. In an enhanced 16nm FinFET technology [24], measurements of the die failure probability distribution (Fig. 7) from 59 typical dies, 109 slow-skewed dies, and 62 fast-skewed dies consistently demonstrate significant benefits for the PFET pass gate. In comparison to the NFET pass gate, the PFET pass gate reduces V_{MIN} by 40%, 55%, and 59% for the slow-skewed dies, the typical dies, and the fast-skewed dies, respectively.

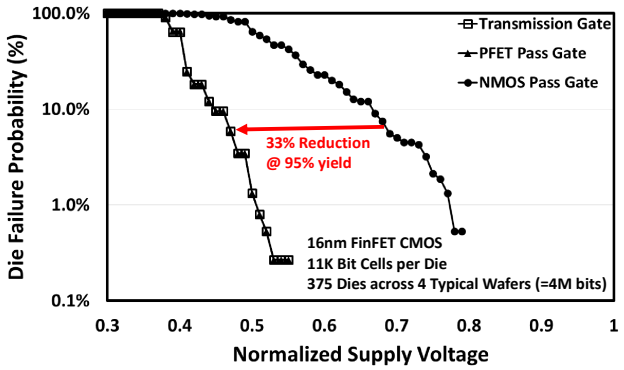


Figure 6. Measured die failure probability versus supply voltage for a 16nm technology.

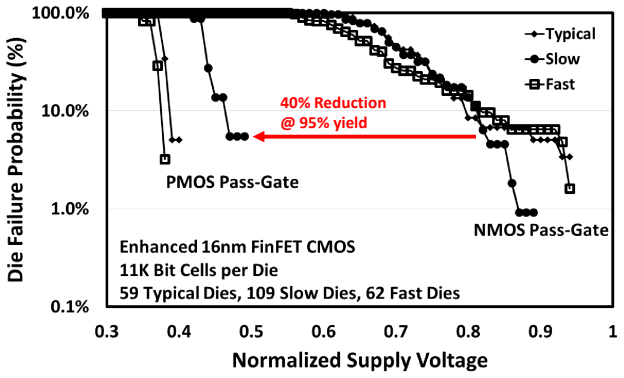


Figure 7. Measured die failure probability versus supply voltage for an enhanced 16nm technology.

To provide insight into the large V_{MIN} benefits of the register file with PFET pass-gate bit cell relative to the NFET pass-gate bit cell, individual device test structures allow current measurements of the NFET and PFET devices across V_{DD} for the enhanced 16nm technology (Fig. 8). At 0.8V, the PFET I_{DSAT} is ~5% higher than the NFET I_{DSAT} for the typical and slow-skewed dies. This difference in I_{DSAT} amplifies as V_{DD} reduces, where the PFET I_{DSAT} is more than 15% larger than the NFET I_{DSAT} at 0.5V for the typical and slow-skewed dies. Thus, the improvement in PFET I_{DSAT} relative to the NFET I_{DSAT} at low V_{DD} directly results in the large V_{MIN} benefits for the PFET pass-gate bit cell.

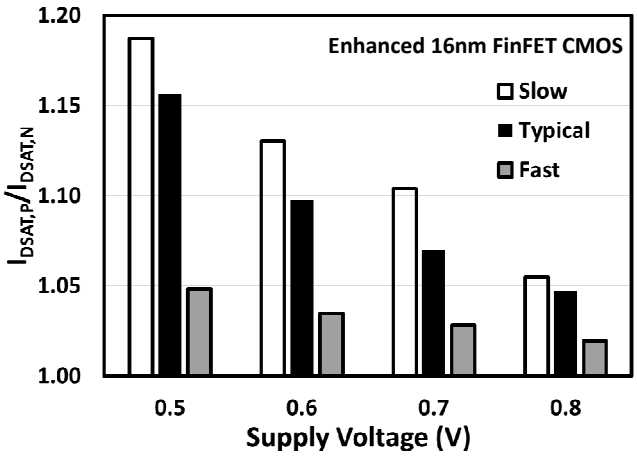


Figure 8. Measured $I_{DSAT,P}/I_{DSAT,N}$ versus supply voltages.

At high V_{DD} values, the bit-cell performance is the primary metric of concern. At 0.89V, F_{MAX} distribution measurements (Fig. 9) from 375 dies across four typical wafers in the 16nm technology [9] demonstrate close agreement between the TG, PFET pass-gate, and NFET pass-gate configurations. These silicon measurements (Figs. 5-8) clearly reveal that the PFET pass-gate provides a substantial V_{MIN} reduction in comparison to the NFET pass-gate with no compromise in performance at high V_{DD} for the two 16nm technologies.

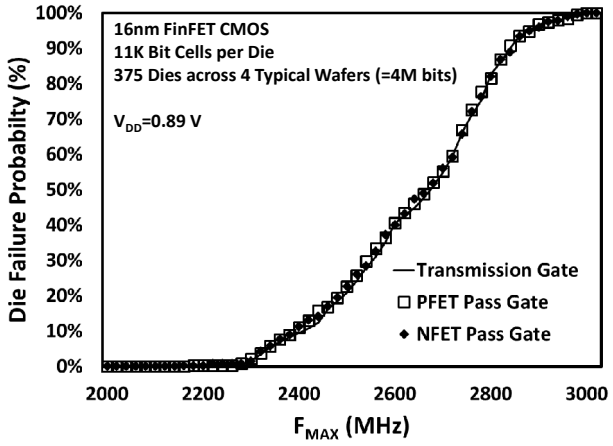


Figure 9. Measured die failure probability versus F_{MAX} at nominal voltage.

In the 16nm process technologies, $I_{DSAT,P}$ is significantly larger than $I_{DSAT,N}$ at low V_{DD} while $I_{DSAT,P}$ and $I_{DSAT,N}$ are approximately equal at high V_{DD}. Depending on the sensitivity of $I_{DSAT,P}$ and $I_{DSAT,N}$ to V_{DD} scaling as well as the high-performance V_{DD} and V_{MIN} set points, $I_{DSAT,N}$ may be larger than $I_{DSAT,P}$ at high V_{DD} while $I_{DSAT,P}$ may become greater than $I_{DSAT,N}$ at low V_{DD}. In this scenario, a tradeoff exists between the F_{MAX} at high V_{DD} and the V_{MIN} for the individual NFET and PFET pass-gate bit cells. Although the primary purpose of the configurable pass-gate bit-cell register file is to compare NFET versus PFET pass-gate bit cells in early technology test chips, the transmission-gate bit cell

design is highly applicable as a single write-port register file when this tradeoff is significant. Thus, the configurable pass-gate bit cell would provide the highest F_{MAX} and the lowest V_{MIN} at a bit-cell area cost of ~7%.

IV. Conclusion

A configurable pass-gate bit-cell register file is implemented in two 16nm FinFET technologies to allow a direct comparison of NFET and PFET pass-gate bit cells. From silicon test-chip measurements of 375 dies across four typical wafers in a 16nm FinFET technology, the PFET pass-gate bit cell provides a 33% V_{MIN} reduction at 95% yield as compared to an NFET pass-gate bit cell. In addition, measurements from 59 typical dies, 109 slow-skewed dies, and 62 fast-skewed dies in an enhanced 16nm FinFET technology consistently demonstrate significant V_{MIN} benefits for the PFET pass gate. The PFET pass-gate bit cell reduces V_{MIN} by 40%, 55%, and 59% for the slow-skewed dies, the typical dies, and the fast-skewed dies, respectively, as compared to the NFET pass-gate bit cell. To provide insight into the large V_{MIN} benefits of the PFET pass-gate bit cell relative to the NFET pass-gate bit cell, the saturation drain currents of the PFET and NFET are measured from individual test structure across voltage. These measurement results indicate that the $I_{DSAT,P}$ is nearly equal to $I_{DSAT,N}$ at nominal voltage, while $I_{DSAT,P}$ outperforms $I_{DSAT,N}$ as voltage reduces. The superior PFET drive strength at low voltages explains the V_{MIN} benefit for the PFET pass-gate bit cell. These silicon measurements clearly reveal that the PFET pass-gate bit cell provides a substantial V_{MIN} reduction in comparison to the NFET pass-gate bit cell with no compromise in area or performance for the two 16nm technologies.

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References

[1] S E. Thompson, et al., "A 90-nm Logic Technology featuring Strained-Silicon," *IEEE Trans. Electron Dev.*, 2004.

[2] S. Flachowsky, et al., "Understanding Strain-Induced Drive-Current Enhancement in Strained-Silicon n-MOSFET and p-MOSFET," *IEEE Trans. Electron Dev.*, 2010.

[3] K. K. Young, et al., "A 0.13 mm CMOS Technology with 193 nm Lithography and Cu/Low-k for High Performance Applications," *IEDM*, pp. 563-566, 2000.

[4] C. C. Wu, et al., "A 90-nm CMOS Device Technology with High-speed, General-purpose, and Low-leakage Transistors for System on Chip Applications," *IEDM*, pp. 65-68, 2002.

[5] S. K. H. Fung, et al., "A 65 nm CMOS High Speed, General Purpose and Low Power Transistor Technology for High Volume Foundry Application," *Symp. VLSI Tech*, pp. 92-93, 2004.

[6] K. Cheng, et al., "A Highly Scaled, High Performance 45nm Bulk Logic CMOS Technology with 0.242 μm^2 SRAM Cell," *IEDM*, pp. 243-246, 2007.

[7] C. H. Diaz, et al., "32nm Gate-First High-k/Metal-Gate Technology for High Performance Low Power Applications," *IEDM*, pp. 1-4, 2008.

[8] C. C. Wu, et al., "High Performance 22/20nm FinFET CMOS Devices with Advanced High-K/Metal Gate Scheme," *IEDM*, pp. 600-603, 2010.

[9] S. Wu, et al., "A 16nm FinFET CMOS Technology for Mobile SoC and Computing Applications," *IEDM*, pp. 224-227, 2013.

[10] S. Thompson, et al., "An Enhanced 130nm Generation Logic Technology featuring 60nm Transistors Optimized for High Performance and Low Power at 0.7 – 1.4 V," *IEDM*, pp. 1161-1164, 2001.

[11] T. Ghani, et al., "A 90nm High volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors," *IEDM*, pp. 1161-1163, 2003.

[12] P. Bai, et al., "A 65nm Logic Technology Featuring 35nm Gate Lengths, Enhanced Channel Strain, 8 Cu Interconnect Layers, Low-k ILD and 0.57μm^2 SRAM Cell," *IEDM*, pp. 657-660, 2004.

[13] K. Mistry, et al., "A 45nm Logic Technology with High-k+Metal gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," *IEDM*, pp. 247-250, 2007.

[14] P. Packan, et al., "High Performance 32nm Logic Technology Featuring 2nd Generation High-k+Metal Gate Transistors," *IEDM*, pp. 1-4, 2009.

[15] C. Auth, et al., "A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors," *Symp. VLSI Tech*, pp. 131-132, 2012.

[16] S. Natarajan, et al., "A 14nm Logic Technology Featuring 2nd-Generatin FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588mm^2 SRAM cell size," *IEDM*, pp. 371-373, 2014.

[17] E. Leobandung, et al., "Scalability of SOI Technology into 0.13 μm 1.2 V CMOS Generation," *IEDM*, pp. 403-406, 1998.

[18] H. S. Yang, et al., "Dual Stress Liner for High Performance sub-45nm Gate Length SOI CMOS Manufacturing," *IEDM* pp. 1075-1077, 2004.

[19] E. Leobandung, et al., "High Performance 65nm SOI Technology with Dual Stress Liner and low capacitance SRAM cell," *Symp. VLSI Tech*, pp. 126-127, 2005.

[20] S. Narasimha, et al., "High Performance 45-nm SOI Technology with Enhanced Strain, Porous Low-k BEOL, and Immersion Lithography," *IEDM*, pp. 1-4, 2006.

[21] B. Greene, et al., "High Performance 32nm SOI CMOS with High-k/Metal Gate and 0.149μm^2 SRAM and Ultra Low-k Back End with Eleven Levels of Copper," *Symp. VLSI Tech*, pp. 140-141, 2009.

[22] S. Narasimha, et al., "22nm High-Performance SOI Technology Featuring Dual-Embedded Stressors, Epi-Plate High-K Deep-Trench Embedded DRAM and Self-Aligned Via 15LM BEOL," *IEDM*, pp. 331-334, 2012.

[23] C-H. Lin, et al, "High Performance 14nm SOI FinFET CMOS Technology with 0.0174μm^2 embedded DRAM and 15 Levels of Cu Metallization," *IEDM*, pp. 381-383, 2014.

[24] S. Wu, et al., "An Enhanced 16nm CMOS Technology Featuring 2nd Generation FinFET Transistors and Advanced Cu/low-k Interconnect for Low Power and High Performance Applications," *IEDM*, pp. 311-314, 2014.