Design of PVT Tolerant Inverter Based Circuits for Low Supply Voltages

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***Abstract*—The design of differential pair based OTAs is becoming increasingly difficult in finer geometries due to lower supply voltages. Inverter based designs have proven to have better transconductance efficiency, higher swing and better linearity but have degraded CMRR, worse PSRR and limited PVT tolerance. In this tutorial, we discuss traditional amplifiers and why inverter based amplifiers are better suited for lower supplies. We then describe the design procedure for inverter based OTA designs with an emphasis on improving their performance, including PVT tolerance, CMRR and PSRR. In particular, we introduce new biasing techniques for inverters to improve their PVT tolerance. We finally validate our designs using measurement results from a number of fabricated designs.**

I. Introduction

Operational transconductance amplifiers (OTAs) are widely employed as active elements in filters, data converters and buffer amplifiers. The increase in demand for battery operated portable devices and implantable medical devices has placed added pressure on lowered supply voltages. Technology scaling proportionally scales supply voltages to maintain device reliability but threshold voltages have not scaled as rapidly to limit the off current leakage in transistors. This severely constrains the tail current overdrive voltage deteriorating CMRR and also prevents the use of cascode devices limiting gain. Non-cascoded inverter based OTA designs with common mode cancellation was proposed in [1]. Body input low voltage OTA designs limit linearity [2], [3]. Linearity improvement using cancellation cancelation techniques have been proposed for higher supply voltages [4]–[7]. Ring amplifiers was proposed for low voltage switched capacitor circuits in [8].

In conventional OTAs, the minimum input common mode voltage is bounded by a threshold voltage and the overdrive voltages of the differential pair plus that of the tail source limiting the input voltage swing. Further, the large signal linearity of differential pairs is limited by the finite tail current.

The linearity and noise of a two stage OTA is typically dominated by the front end gain stage which can be a traditional differential pair or an inverter. Fig. 1 shows a comparison of the input common mode range of a traditional differential pair and a pseudo differential inverter. We will use some typical numerical numbers to illustrate our example. The overdrive voltage (V_{ov}) of all the devices are assumed to 125mV. Due to body effect the transistors (M3, M4) have a threshold voltage (V_{TN}) of 440mV (50mV above nominal). Therefore, the minimum input common mode voltage for the differential pair is $V_{TN} + V_{OV3} + V_{OV5}$ = 690mV. This clearly limits the input signal range. Furthermore, in most continuous time systems, that are once again becoming popular due to the limited headroom for switches, the input and output common mode voltages become equal due to the DC negative feedback around the loop. Hence the minimum output common mode is also 690mV. With a power supply of 0.9V and one overdrive drop at the PMOS transistor, the maximum attainable swing is now 170mVpp. Inverter based OTAs ($M_{6,8}$ and $M_{7,9}$) allow rail-to-rail input swing because of the class AB operation. Hence the input and output common mode can be at mid supply for optimal signal swing. This translates to a maximum attainable output swing of 650mVpp (4x larger than traditional OTAs). Further the transistors do not suffer from body effect resulting in higher linearity and transconductance. In fact, current reuse in inverters enables at least a 2X higher transconductor (g_m/I_d) efficiency compared to an OTA.

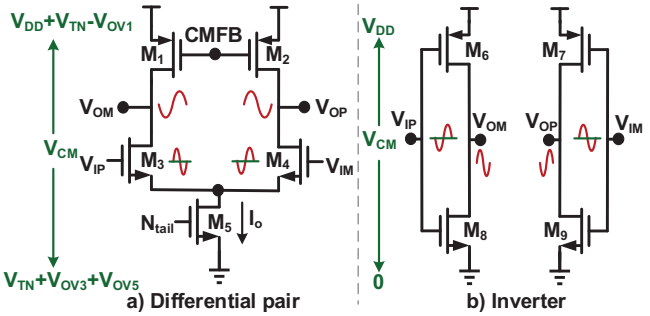

Fig. 1: Input and output swings of differential pair and inverter OTAs

The input referred noise for a differential pair and for a pseudo differential inverter is given by Eqn. (1).

$$v^2_{n,diffpair} = \frac{8kT\gamma}{gm_3}\left(1+\frac{gm_1}{gm_3}\right);\ v^2_{n,inv} = \frac{8kT\gamma}{gm_6+gm_8} \quad (1)$$

The transconductance g_{m3} is assumed to be equal to the inverter transconductance $gm_6 + gm_8$ for the sake of comparison. The excess noise factor for the inverter is 1 which is less than that for the corresponding differential pair $[(1 + gm_1/gm_3)]$. This is because all the transistors in the inverter contribute both to the signal transconductance and to the noise whereas in the differential pair the load transistor (M_1 and M_2) contribute only to the noise. The overall linearity is normally determined by the linearity of the input transconductor. Assuming square law operation and fully differential circuits, the output current for the differential pair and for the pseudo differential inverter is given by Eqns. (2) and (3) [9].

$$I_{diffpair} = -V_{IN}\frac{\beta_n}{2}\sqrt{\frac{4I_o}{\beta_n} - V^2_{IN}} \quad (2)$$

$$I_{inv} = -V_{IN}\frac{\beta_n}{2}\left[(V_{CM}-V_{TN}) + \frac{\beta_p}{\beta_n}(V_{DD}-V_{CM}-|V_{TP}|)\right] \quad (3)$$

The current limit due to the tail current in the differential pair leads to nonlinear components as seen in Eqn. (2), whereas the output current in the inverter is highly linear. Further the body effect incurred by the differential pair deteriorates its linearity

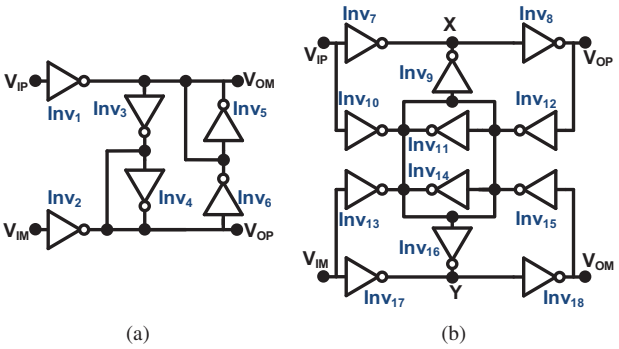

Fig. 2: (a) Nauta inverter transconductor (b) Inverter based 2 stage OTA

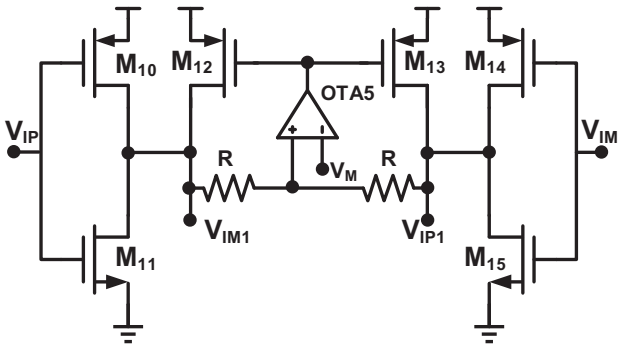

Fig. 3: Common mode rejection stage in inverter based OTA design

even more. Improved linearity in the inverter with its ability to support higher signal swing with lower noise contribution in comparison to a differential pair makes it an attractive alternative particularly in lower technologies. However, the PVT variance and poor CMRR and PSRR has traditionally limited the use of inverter based amplifiers.

II. Inverter Transconductor

Fig. 2(a) shows the inverter transconductor circuit from Nauta [9], [10]. The inverters $Inv_{1,3,5}$ are identical to those of the differential counterpart $Inv_{2,4,6}$. The common mode level of the output voltages V_{OP} and V_{OM} is controlled by the four inverters Inv_{3-6}. The output common mode voltage is at the meta stable point of the inverters $(Inv_{4,5})$. Inverters (Inv_{3-6}) are designed to offer negative impedance to differential signals by making g_{m3} greater than g_{m4}. This is used to increase the differential mode gain by increasing the effective differential impedance. The common mode and differential mode impedance offered by these inverters are $1/(g_{m3}+g_{m4})$ and $1/(g_{m4}-g_{m3})$. The transconductance has a large bandwidth because of the absence of internal nodes [9]. The transconductance in this design is set by altering the supply voltage and hence requires an on chip power regulator. To partially address this issue, tunable inverters using body terminals in a master slave approach was proposed in [11].

A 2 stage inverter based differential OTA is shown in Fig. 2(b) [1]. The first stage has feedforward paths (Inv_{9-11}) for common mode cancellation, while the second stage uses additional feedback paths for the common-mode $(Inv_{9,11,12})$. The transconductances of inverters (Inv_{7-12}) are identical to those of inverters (Inv_{13-18}) for fully differential operation. The input common mode voltage (ΔV_{cm}) generates a current of $(g_{m7} - g_{m9}g_{m10}/g_{m11})\Delta V_{cm}$ at node X and Y. If the transconductance $(g_{m9}g_{m10}/g_{m11})$ is made equal to g_{m7}, then the voltages at node X and node Y are invariant to any input common mode variations.

However, unlike a traditional differential pair where only the differential mode components are converted to current, here both the differential and common mode components are converted to current and only at the outputs are the common mode currents cancelled. The common mode transfer function from node X to output V_{OP} is given by Eqn. (4). The common mode signals are suppressed in the feedforward path and then further suppressed by the gain given by Eqn. (4) in the feedback path. Unlike [9], this design uses high impedance nodes for gain such that it requires frequency compensation for both the differential and common mode feedback loops.

$$\frac{V_{OP}}{X} \approx \left(\frac{g_{m11}}{g_{m12}}\right)\frac{g_{ds9}}{g_{m9}} \tag{4}$$

Circuit simulations were used to show a low frequency CMRR of 65.8dB at 1.8V along with a differential mode gain of 48.2dB in [1]. Since the metastable point of the inverter varies with PVT, the designs in [1], [9]–[11] and other inverter based designs [12]–[14] are sensitive to PVT variations. This is one of the primary issues we address in Section IV.

III. Common Mode Rejection

Unlike a differential pair, in both the designs [1], [9] the input common mode signal affects the biasing of the main inverter $Inv_{1,7}$, which makes the differential mode gain and bandwidth to be a function of input common mode voltage. Additionally, power supply variation or a common mode signal clock also directly affects the differential performance due to limited common mode rejection. The improved common mode rejection in a traditional differential pair is obtained due to negative feedback offered by the high impedance tail current source(M_5 in Fig. 1) to common mode signals. The tail current source in a differential pair reduces the common mode transconductance by providing large source degeneration to common mode signals at the differential pair transistors. This ensures that only the differential mode voltage is converted to a current by the differential pair and the common mode voltage appears directly at the tail node. The dependency of the bias current to common mode signals is only due to any drain source modulation of the tail current source and hence is much smaller in magnitude.

To circumvent the finite input CMRR of inverter based amplifiers, we designed and fabricated a 3 stage inverter based OTA in TSMC's 40nm technology. In this design the primary purpose of the first stage is to provide common mode rejection (CMRS) as shown in Fig. 3. It also has some finite gain to reduce the noise impact of the following stages. The second stage is a cascoded high gain stage (Fig. 5) discussed in the next sub-section. The low output impedance third stage is used to drive a resistive load of 3 kΩ and a capacitive load of

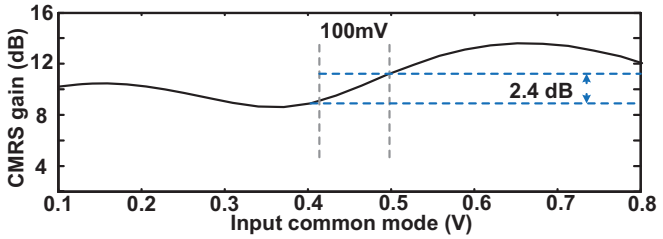

Fig. 4: Common mode rejection stage gain with input common mode voltage

2pF. Common mode rejection in the inverter based OTA is introduced via an external common mode feedback as shown in Fig. 3. The input signal along with the common mode is converted to current using transistors (M_{10-11} and M_{14-15}). The common mode voltage at the output of the first inverter ($M_{10,11} and M_{14,15}$) is sensed using the two R resistors and is fixed to a known voltage using OTA5 in negative feedback.

The transistors (M_{10-11} and M_{14-15}) are common to both differential and common mode signals thereby converting both to current. However, negative feedback (OTA5) provides a low $(1/(g_{m12}A_{OTA5}))$ impedance to common mode signals and a high impedance (≈R) to the differential mode signals. This attenuates the common mode signals but amplifies the differential mode signals. The CMRS stage gain should be minimized in order to reduce the differential gain and bandwidth dependency on the common mode signal. Further, a higher CMRS gain reduces the phase margin of the OTA and also increases the power consumption in OTA5. However, a lower transconductance in transistors (M_{10-11} and M_{14-15}) increases the input referred noise of the circuit. In this design the CMRS stage gain is selected to be 3 (9.5dB) with an input transconductance equal to 1mS and R resistors are 3kΩ. Fig. 4 shows the simulated gain of the CMRS stage versus the input common mode voltage. As can be seen in the figure the gain changes only by 2.4 dB with 100mV change from the nominal common mode voltage (450mV) for a 0.9V power supply. The CMRS gain change is limited to a little over 8.5dB to 13.5dB for an extreme 700mV input common mode voltage range.

A. Cascoding in inverter amplifiers

Although use of negative resistance in [9] improves DC gain, it contributes to noise while, cascading increases the DC gain at the cost of increased power and the number of poles. Cascoding is often used in the first stage in a typical two stage differential pair based OTA to increase the DC gain without increasing the input referred noise or deteriorating the frequency response. The constant current biasing in a differential pair makes low voltage cascoding possible. However, the bias current in inverters is a function of input common mode voltage and the power supply making normal low voltage cascode biasing difficult.

In this design the CMRS stage rejects the input common mode voltage and fixes the common mode to the meta stable voltage (V_M) of inverters (M_{16} and M_{19} in Fig. 5). Hence the current in the high gain stage is independent of any common mode variations. The known common mode voltage V_M enables cascode biasing for $M_{17,18,21,22}$ in the high gain

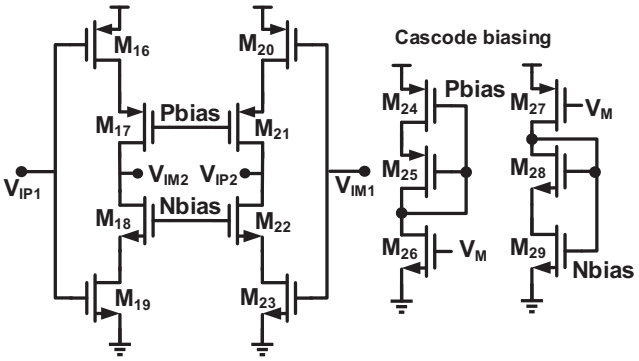

Fig. 5: Cascode gain stage in the inverter based OTA design

stage. Cascoding the inverters increases the DC gain by about 20dB. Cascoding utilizes the bias circuits shown to the right of Fig. 5. Here M_{24} and M_{29} are in triode to create over drive voltage required to maintain transistors M_{16}, M_{19} M_{20}, and M_{23} in saturation.

IV. PVT Tolerant Biasing

Inverter amplifiers have traditionally been biased using a constant voltage replica biasing technique. The replica is typically an equal sized inverter with input and output shorted [9]. This method of biasing ensures that the inverters are biased at their maximum transconductance (g_m) and that the input and output common mode voltages remain equal at V_M. Unfortunately, this method of replica biasing has its limitations as the bias point is directly affected by PVT variations. In fact, using this technique the effective transconductance can vary $\approx 40\%$ with PVT variations impacting bandwidth, stability and gain. To solve this problem we introduce three techniques, semi-constant current biasing (SCCB), constant current biasing and constant gm biasing. We have verified the semi-constant current biasing technique using multiple fabricated designs, while the constant current and gm biasing technique have only been verified using circuit simulations. Therefore, we first introduce the semi-constant current biasing technique and evaluate its performance. This is followed by constant current and gm biasing techniques.

A. Semi-constant current biasing

To implement SCCB the inverters are skewed in size such that even at the fast-slow corner, the transconductance for the NMOS is greater than for the PMOS. We need this additional degree of freedom to control PVT variations. In our design the NMOS transistor is the same size as the PMOS transistor. This choice gives up some transconductance efficiency ($\approx 30\%$ for $\mu_n/\mu_p = 2.5$) for increased PVT tolerance. The NMOS in the main unit inverter (IU) is biased with a constant current as shown in Fig. 6 [15]. The W/L size of the NMOS transistor is selected such that the gate voltage (V_b) is close to mid supply. For the nominal supply voltage the voltage V_m is equal to V_b due to the OTA$_b$ feedback loop. The auxiliary inverter (I_A) is used to make the input and output voltage of the unit inverter equal using negative feedback. This is necessary to ensure that the main inverter (I_M) remains in saturation and it also makes

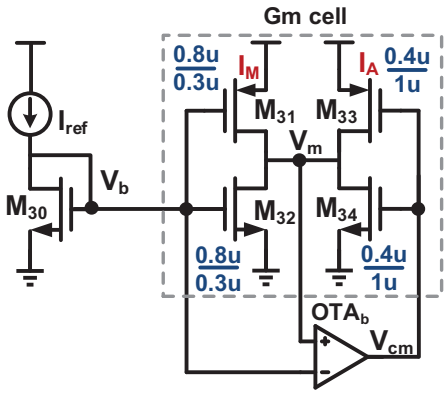

Fig. 6: Circuit schematic for semi-constant current inverter biasing

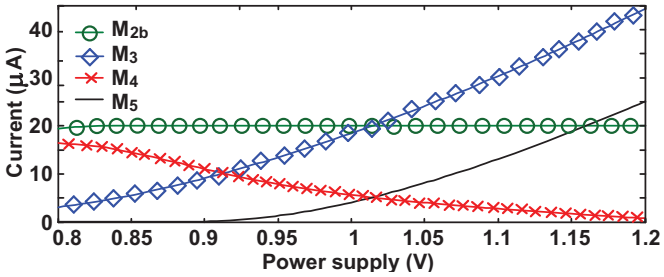

Fig. 7: Biasing network current with power supply variation

the cascading of inverters possible. Further, this reduces any drain source voltage mismatch between the NMOS transistor in the main inverter (M_{32}) and the diode connected NMOS (M_{30}). Fig. 7 shows the current in the different transistors with changes in the power supply. At the nominal supply voltage the current in the NMOS(M_{32}) is higher than in the PMOS (M_31) making the NMOS transconductance higher than for the PMOS, recall that both devices are sized the same. The NMOS (M_{32}) in the main inverter is biased at a constant current and hence it is constant with power supply. An increase in the supply voltage increases the PMOS (M_{31}) current thereby increasing the voltage V_m in Fig. 6. However the negative feedback increases the gate of M_{34} to absorb the extra PMOS current to restore the voltage V_m to V_b. Hence the PMOS (M_{33}) current reduces while the NMOS (M_{34}) current increases with an increase in the power supply voltage making the sum of the currents nearly constant. As we will see next this stabilizes the NMOS + PMOS transconductance. The common-mode voltage V_{cm} is used to bias the rest of inverters in the design.

Fig. 8 shows the variation of transconductance with temperature (left) and with supply voltage (right). We note that though the overall transconductance is not completely constant it only varies from 320μS to 260μS with a 140° change in temperature. Regarding supply variation, the NMOS transconductance is constant with power supply and is higher than the PMOS transconductance limiting the overall transconductance variation from 220μS to 320μS (37%) with a 40% change in power supply. The variation in transconductance with normal replica biasing [9] would have been from 180μS to 361μS (67%) for the same conditions. As we will see later with

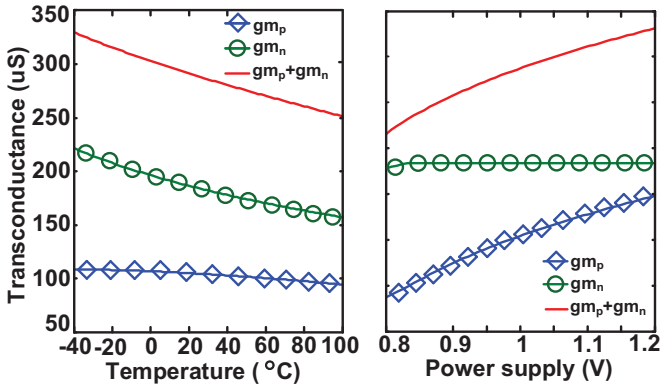

Fig. 8: Variation of inverter transconductance with temperature and supply

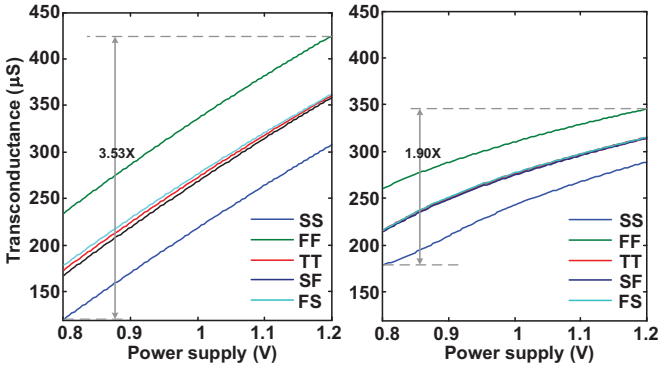

Fig. 9: Variation of inverter transconductances with power supply across process corner for traditional replica biased inverters and SCCB inverters

constant-gm biasing, in the next sub-section, even these variations will be eliminated. However, before we discuss constant-gm biasing let us discuss the tradeoffs involved in the ratioing of the NMOS and PMOS transistors.

1) Optimal NMOS-PMOS ratioing: To evaluate the tradeoffs involved in ratioing the NMOS and PMOS transistors we study the variation of the overall transconductance for different NMOS-PMOS ratios, i.e., Wp=2Wn, Wp=Wn, and Wp=0.5Wn versus the power supply voltage. The variation of transconductance using SCCB is observed to be always lower than the corresponding traditional replica biasing technique. Second, as we keep reducing the PMOS size the variation of the overall transconductance with power supply is reduced. However, this reduces the overall transconductance and also demands a higher current in the PMOS of the auxiliary inverter. Hence for this and other designs the PMOS and NMOS widths are selected to be of equal size as a design compromise.

Fig. 9 shows the transconductance variation of SCCB (right) and traditional replica biased (left) inverters with power supply across process corners. The transconductance variation of SCCB inverter is 1.9X while that for the replica biased inverter is 3.53X. This is roughly a 50% reduction in the transconductance variation using this technique alone. All the auxiliary inverters used in the fabricated designs are biased with the voltage V_{cm}. This will make sure that all the NMOS transistors in these inverters have the same bias current of Iref.

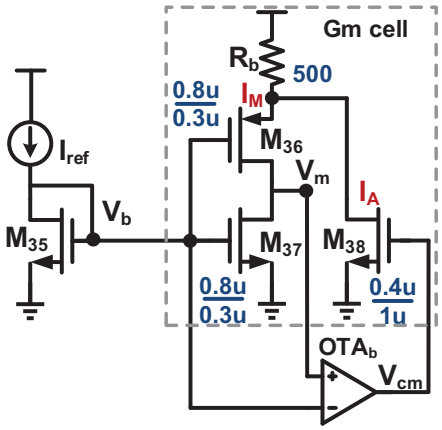

Fig. 10: Circuit schematic for constant current biasing for inverters

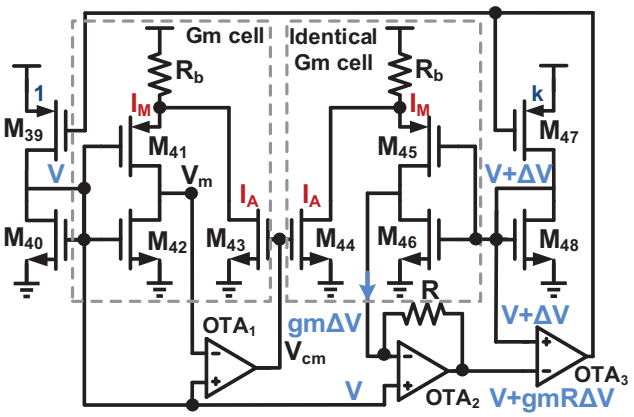

Fig. 12: Circuit schematic for constant gm biasing for inverters

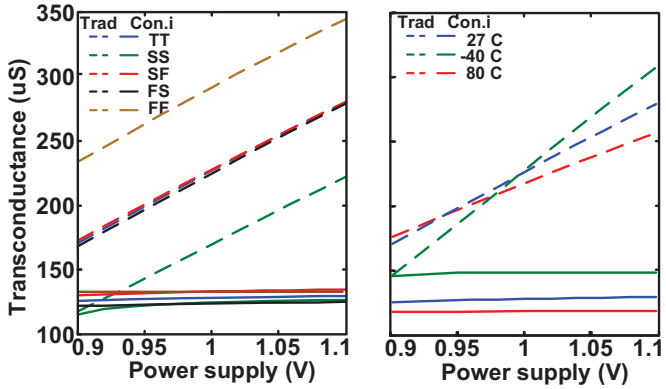

Fig. 11: Variation of constant current biased inverter gm with power supply across process corners at 27°C and with temperature in typical corner

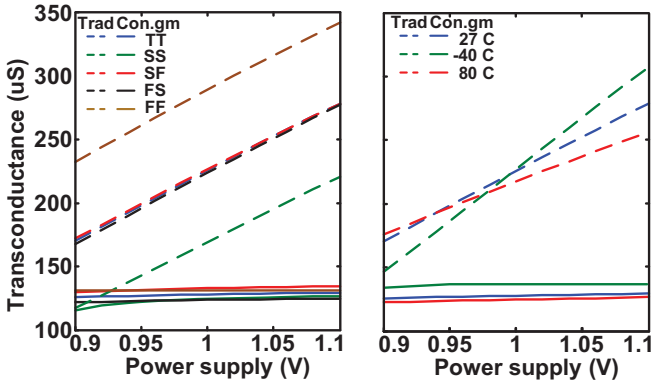

Fig. 13: Variation of constant gm biased inverter transconductance with power supply across process corners

With PVT variations the NMOS transconductance remains constant but the PMOS transconductance will vary. Since we have designed the PMOS transconductance to be lower than the NMOS transconductance, the overall transconductance variation is reduced. Any mismatch between the transistors in the biasing network and the forward path will only result in an input referred offset due to feedback around the loop.

Semi constant biasing allows us to have different currents in the PMOS and NMOS transistor. This enables us to select an optimal NMOS bias current where the PMOS and NMOS nonlinearity is mutually cancelled as discussed in Section V.

B. Constant current biasing

SCCB fixes the current in one transistor (NMOS in this design) while the current in other transistor (PMOS) varies with PVT. However, the PMOS transistor current can be fixed by adjusting its source voltage as shown in Fig. 10. Like in SCCB, the NMOS transistor (M_{37}) in Fig. 10 is biased using a constant current reference (I_{ref}). The input and output voltage of the main inverter (M_{36} and M_{37}) is made equal by using an auxiliary NMOS transistor (M_{38}) and OTA_b in negative feedback. Transistor (M_{38}) creates a voltage drop across the bias resistor R_b by pulling current from the source of M_{36} to make the PMOS (M_{36}) and NMOS (M_{37}) equal to I_{ref}. The resistor R_b and transistor M_{38} are selected such that they maintain a finite non-zero voltage drop across R_b over PVT. At the nominal conditions the drop across the resistor is around 20mV in this design. For example when the power supply increases, the negative feedback increases the voltage drop across R_b by increasing the current in M_{38}. This modulates the source voltage of M_{36} to make its current equal to I_{ref}.

Fig. 11 show the simulated variation of the inverter transconductance with a 20% variation in power supply voltage across process corners at 27°C (left) and with temperature at typical corner (right). The dotted line corresponds to the variation of a traditionally biased inverter (Fig. 2(a)) of the same size. The solid lines shows the transconductance variation for the constant current biasing technique. The variation of transconductance with process corners is only 9% with constant current biasing as compared to 97% variation with traditional inverter biasing. However, the transconductance of the constant current biased inverter and traditionally biased inverter varies by 22% and 66% with temperature at typical process corner. This is because the mobility of the transistors changes along with the threshold voltage with temperature. Constant current biasing provides constant transconductance only with a change in the threshold voltage and not with mobility change. Hence we adopt a constant gm biasing scheme to solve the transconductance dependence on mobility as described in the next sub-section.

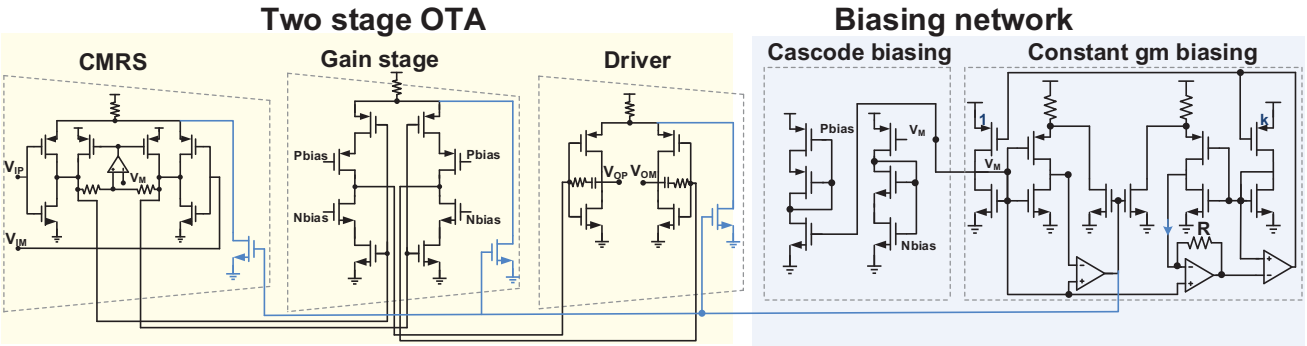

Fig. 14: Schematic of the constant gm biased inverter based OTA

C. Constant-gm biasing

Constant gm biasing for differential pair OTAs with PVT tolerance was proposed in [16]. We adopt the technique for inverters and update the bias current I_{ref} in Fig. 10 to make the transconductance PVT tolerant. Fig. 12 shows the circuit schematic for constant gm biasing for inverters. Here I_M and I_A are the main inverter and auxiliary transistor. The negative feedback loop with OTA_1 ensures the input and output of the main inverter is equal to V by generating the bias voltage V_{cm}. If we reuse the main (I_M) and auxiliary inverters (I_A) as a gm cell in the design with I_A biased at V_{CM}, then I_M will be biased at the constant gm as in the bias network. The transistor M_{39} creates a voltage V at the gate of $M_{41,42}$ by pumping current into the diode connected transistor (M_{40}). Further the transistor M_{39} and M_{47} has a slight difference in their aspect ratio (1:k) to create a small voltage ΔV greater than any offset across identical gm cells ($M_{41,42}$ and $M_{45,46}$). An input of V+ΔV is given to an identical gm cell with its auxiliary biased at V_{cm}. The output current $g_m \Delta V$ is converted to a voltage $g_m \Delta V R$ using the transimpedance amplifier (OTA_2). The gate of transistor M_{39} and M_{47} are controlled using OTA_3 to make $gmR = 1$ using negative feedback. With PVT variations, the voltage V is adjusted by the bias network so that the transconductance (g_m) of the inverter remains constant at $1/R$. If the main inverter and the auxiliary transistor in the gm cell is biased with voltage V and V_{cm}, then the gm cell has the transconductance of $1/R$. To avoid the variation of R across corners ($\pm$20%), the resistor R is selected to be an offchip component.

Fig. 13 shows the simulated variation of the inverter transconductance with a 20% variation in the power supply voltage across process corners at 27°C (left) and with temperature at typical corner (right). The dotted line corresponds to the variation of a traditionally biased inverter (Fig. 2(a)) of the same size. The solid lines shows the transconductance variation for constant gm biasing technique. The variation in transconductance reduces from 97 % to 8.7 % across process corners at 27°C and power supply with the constant-gm biasing technique. The variation in transconductance reduces from 66 % to 9.2 % across temperature at 27°C and power supply with the constant-gm biasing technique.

The constant-gm technique is an updated version of the

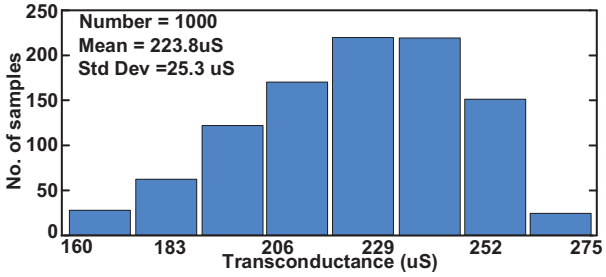

Fig. 15: Monte Carlo simulation for a constant gm inverter

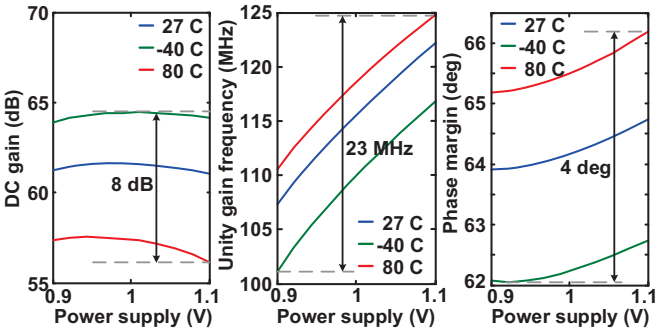

Fig. 16: Simulated variation of DC gain, unity gain frequency and phase margin with power supply across temperature

constant current biasing technique discussed above and to a large extent solves the PVT variability of inverter based designs making them significantly more production friendly. Since replica biasing relies on the matching of the transistors, a Monte Carlo simulation was performed on the constant gm biased inverter (size: PMOS/NMOS 1u/0.2u) as shown in Fig. 15. The mean and standard deviation in transconductance for 1000 runs is obtained as 223.8 μS and 25.3 μS.

A two stage Miller compensated inverter based OTA was designed in TSMC 65nm using the constant gm biasing as shown in Fig. 14. The first stage rejects the common mode variation, the second stage is cascoded for higher gain and third stage is used to drive the load of 1pF. All the stages are biased with the constant gm biasing technique. The common mode feedback circuitry is not shown for clarity purposes.

Fig. 16 shows the simulated variation of DC gain, unity gain frequency and phase margin with power supply in typical process corner for three different temperatures. The blue, green and red color show the variation at 27°, -40° and 80°. Al-

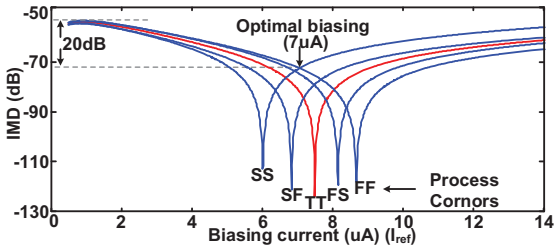

Fig. 17: Choice of bias current based on intermodulation distortion

though the DC gain varies by 8dB across temperature, it varies less than 2dB with power supply for a given temperature. Unity gain frequency varies by 23 MHz and 10MHz with power supply and temperature and the phase margin remains above 60° for the entire range.

Interesting note: A doubling in the width of both the PMOS and NMOS transistors does not change its gain. It is equivalent to adding the gm cells in parallel where both gm and gds increases by same amount. Hence only the channel length determines the gain of the inverter. Any increase in the width of the transistor results in an increase in its gm resulting in an increase in the system UGF. This property of inverter based designs separates the gain and gm parameters simplifying design. Simulations show that with constant gm biasing, the effective gds varies less than 20% across PVT variations.

V. Non-linearity cancellation techniques

We start off by making the following observation, the product of a function and its inverse is equal to 1, i.e., $ff^{-1} = 1$. If a function is multiplied by its inverse, then any non-linearity in the function is canceled. This property is widely exploited to cancel the nonlinearity of circuits, i.e., in the design of current mirrors, filters [17] and ADC drivers [15]. The nonlinearity cancellation technique can also be used to increase the inherent linearity of inverters. Using a square law model, the output current is given as the difference between the NMOS and PMOS currents as in Eqn. (5).

$$I_o = (\beta_n - \beta_p)V_{in}^2 + V_{TN}^2\beta_n - |V_{TP}|^2\beta_p - 2V_{in}\left[\beta_n V_{TN} - (V_{DD} - V_{TP})\beta_p\right] \quad (5)$$

The quadratic nonlinearity is cancelled by selecting $\beta_n = \beta_p$. Additionally, the fully differential implementation inherently cancels the even order harmonics leading to highly linear operation. When the input signal swing is large, one transistor enters the subthreshold regime. The nonlinearity for short channel devices can be cancelled by the choice of bias current in the transistors. The SCCB biasing technique allows for different currents in the NMOS and PMOS transistors making this possible.

For analysis purposes let us assume that the NMOS is in saturation and the PMOS is in subthreshold. If the input to the inverter is V_{IN}, the short channel NMOS current in saturation and the PMOS subthreshold current is given by Eqns. (6) and (7) [18].

$$I_N = \beta_n\left[(V_{IN} - V_{TN})^2 - \theta_n(V_{IN} - V_{TN})^3\right] \quad (6)$$

$$I_P = I_o \exp\left(\frac{(V_{DD} - V_{IN} - V_{TP})}{\eta U_T}\right) \quad (7)$$

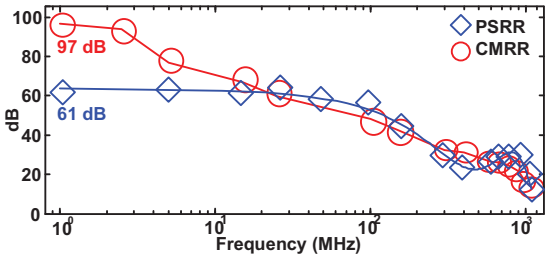

Fig. 18: Measured PSRR & CMRR of the inverter amplifier at 0.9V Vdd

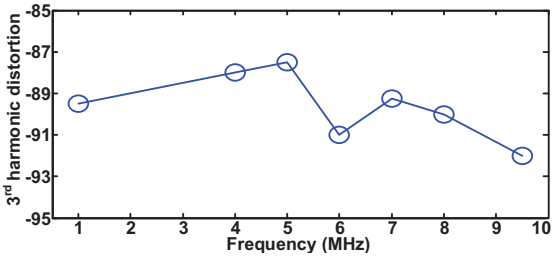

Fig. 19: Measured 3^{rd} harmonic distortion of the inverter based amplifier for a 0.9V pp differential swing using a 0.9V Vdd

where I_o is the characteristic subthreshold current of the PMOS transistor and U_T is the thermal voltage. The output current $(I_{out} = I_P - I_N)$ in a differential implementation can be approximated by Eqn. (8). The third order coefficient can be minimized, improving the linearity, by choosing the peak PMOS current close to be the product of β_n and θ_n of the NMOS.

$$I_{out} = b_1 V_{IN} + b_3 V_{IN}^3 \quad \text{where} \quad (8)$$
$$b_1 = \beta_n\left(2V_{TN} + 3\theta_n V_{TN}^2\right) - \left(6 + 9(V_{DD} - V_{TP})^2\right) I_0$$
$$b_3 = (\theta_n\beta_n - I_0)$$

To confirm this, a SCCB inverter was simulated with a 450mV peak to peak input for various bias currents. The PMOS current is adjusted automatically set by the negative feedback in the SCCB. The output current is driven into a low impedance node and the intermodulation distortion is measured. As seen from Fig. 17, the IMD decreases with bias current, it reaches a minimum and then increases. Since the IMD is sensitive to process, the simulation is done across slow-slow(SS), slow-fast(SF), fast-slow(FS), fast-fast(FF) and typical(TT) corners. The optimal bias current of 7μA ensures that even across corners inter modulation distortion is always less than -72dB. This gives a 20dB improvement in the open loop linearity of the inverter across corners with respect to constant voltage biasing while maintaining the input and output common modes near mid power supply.

VI. Measurement Results

We use measurements from 3 designs to validate our approach. All the amplifiers used in the design are inverter based. Improved linearity and PSRR are verified using replica biasing in TSMC's 40nm GP process and SCCB was verified via an ADC driver and a filter in TSMC's 65nm GP process.

Replica biasing: An inverting amplifier with gain one was designed in TSMC's 40nm GP technology to verify cascoding, CMRR, PSRR of inverter based OTA at 0.9V Vdd. The OTA

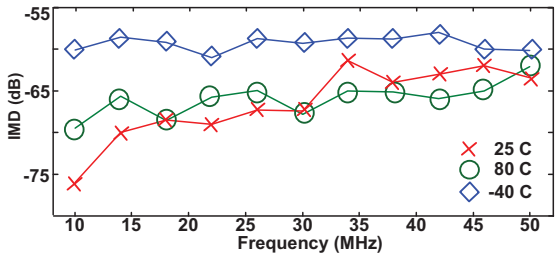

Fig. 20: Measured IM distortion of ADC driver over temperature

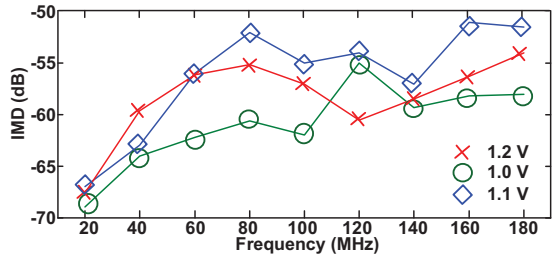

Fig. 21: Measured IM distortion of filter at highest tuning over power supply

was biased using replica biasing and occupies an area of $0.0025mm^2$. Similar to Fig. 14, the OTA has three stages the low gain CMRS stage, cascoded gain stage and driver stage to drive 2pF and 3kΩ load. The OTA has a UGF of 502MHz. Fig. 18 shows the measured PSRR and CMRR for the amplifier. Low frequency CMRR is measured as 97dB and 3dB point is at 2.5MHz. PSRR is 61 dB till 30MHz and the 3dB point is at 35 MHz. Fig. 19 shows the 3^{rd} harmonic distortion of the OTA with a 0.9V Vdd and a 900mV pp differential input swing. The third harmonic distortion is less than -87 dB over the entire 10 MHz signal band. This is due to the higher inherent linearity of inverters and higher loop gain which was made feasible by cascoding.

SCCB: The SCCB technique was verified by designing an ADC driver [15] and filter in TSMC's 65nm GP technology. The ADC driver has a DC gain of 8 and is used to drive a 10 bit ADC with 1pF input capacitance to rail to rail swing. The design has been verified across temperature and power supply by measuring its intermodulation distortion. Fig. 20 shows the IMD of the ADC driver measured across temperature with nominal power supply of 1V. At Nyquist frequency the IMD varies by only 4dB over 80°C. A 3rd order Butterworth filter was designed to have the cut off frequency tunable from 31-314MHz and it occupies an area of $0.007mm^2$. The measured IMD of the filter for a ± 10% variation in power supply at a 3dB frequency of 314MHz is plotted in Fig. 21. The linearity in both the designs is obtained partly by SCCB biasing partly by non-linearity cancellation using inverters. Fig. 22 shows the micrograph of the fabricated OTA, filter and ADC driver in TSMC's 40nm and 65nm technologies.

VII. Conclusions

Inverters has proven to have better transconductor efficiency and are inherently linear. This paper provides a tutorial of PVT tolerant inverter based circuits. Semi constant current biasing and constant gm biasing to improve PVT tolerance and linearity were verified via simulation results. While, measurements from semi constant current biased inverters in the ADC driver and 3rd order filter were used to verify improved PVT tolerance. Further it is shown that non-linearity cancellation techniques using inverse functions can be exploited to improve the linearity of inverter based circuits.

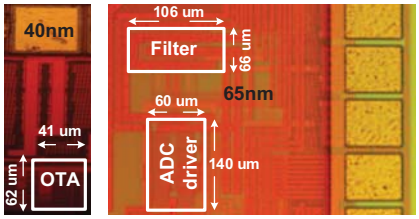

Fig. 22: Micrographs of fabricated inverter based OTA, ADC driver and filter

VIII. Acknowledgements

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