A System-Verilog Behavioral Model for PLLs for Pre-Silicon Validation and Top-Down Design Methodology

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***Abstract* — This paper presents a System-Verilog behavioral model for charge-pump PLLs based on piece-wise constant (PWC) real number modeling and table lookup. The proposed model exploits the sampled nature of the PLL where most of its analog behavior takes effect during the phase detection, and remains almost constant during the rest of the reference cycle. The PLL model simulation run time takes only 1 second, which makes it a perfect fit for pre-silicon digital validation as well as top-down design methodology. Compared to transistor-level Spice simulations, the proposed model shows a correlation of more than 97% for the PLL locking behavior, jitter, and phase noise. The PLL model is used to exercise critical features like spread-spectrum clocking (SSC) and adaptive frequency system (AFS). In addition, the model was integrated in a pre-silicon validation environment and enabled catching design bugs.**

I. Introduction

Phase Locked Loops (PLLs) have been widely used in clock generation, clock and data recovery, and high speed IOs [1-3]. Spice simulators provide the highest accuracy in simulating the PLLs, but they are very slow as they solve single full matrix for the entire circuit. This is problematic especially when simulating features that require mixed signal modeling like Spread Spectrum Clocking (SSC) and Adaptive Frequency System (AFS) [1]. Fast Spice simulators offer speed up by employing table lookup models for transistors, and design partitioning for multi-rate time stepping [4]. Simulation run time though is still too high for the two aforementioned types of simulation. For example, running a mixed-signal simulation for a PLL to exercise SSC feature may take months or days with Full Spice and Fast Spice respectively. The slow simulation time turnaround adds risks of potential pre-silicon bug escapes. Therefore, PLLs behavioral models with different simulation techniques have been proposed to address these challenges.

In [5] a top-down HDL-A behavioral PLL model has been utilized to reduce design development time, with very good correlation and 5x faster simulation time. HDL-A language (like Verilog-A or VHDL-A) can capture key dynamics of analog circuits, but it does not fit well in a complete digital event-driven validation framework. The behavioral model proposed in [6] utilizes a digital event-driven approach using Verilog to model analog blocks in a serial link system. This enables co-simulating analog with large digital functions while maintaining fast simulation time. This approach uses simple slow-events integer-based description that makes it limited to low accuracy signals. However, it may fail with more complex analog blocks that require high accuracy and high resolution. The Verilog piecewise-linear behavior model proposed in [7] and [8] represents a continuous signal with an initial voltage and a slope. The signal continues with the same slope until the next event. This solution achieves faster simulation time and captures the PLL dynamics but fails to express signals with abrupt slopes and still requires fine time steps with small phase errors.

We propose a System-Verilog behavioral model for charge-pump PLLs based on piece-wise constant (PWC) real numbers and table lookup that runs in only 1 second. The proposed technique exploits the sampled PLL characteristics where most of its analog behavior occurs during phase detection, while remains constant during the rest of the cycle. The model fits well in any pre-silicon event-driven digital validation framework, for top-down design methodology, and is capable of expressing continuous and abrupt slope signals. By capturing the analog dynamics of the PLL, the model can be used to validate features only possible today with lengthy mixed signal simulations. This helps increase the validation coverage by running more test vectors for complex features. In addition, the model can be used in top-down design methodology, as shown in Fig.1, where PLL designers can control actual circuit parameters (Capacitors, Resistances, Currents, etc.) to exercise the behavior of the PLL for performance optimization.

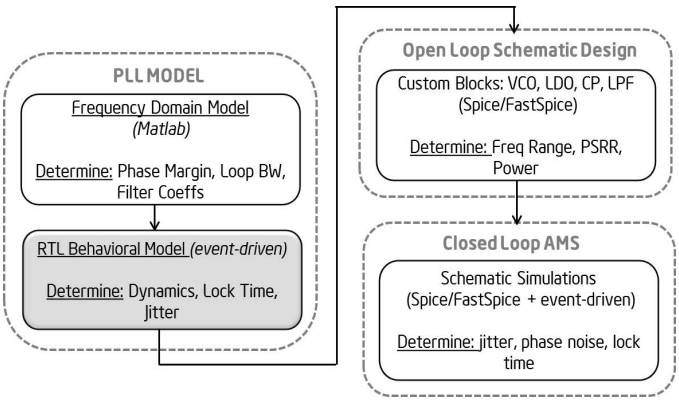

Fig. 1. PLL top-down design methodology

The paper is organized as follows; Section II describes the modeling approach with design examples. Section III presents the model results and its applications in top-down design methodology and pre-silicon validation. Section V concludes.

II. PLL System Verilog Behavioral Model

A. Modeling Approach:

The PLL system has non-linear characteristics where it reacts every reference cycle and updates the VCO frequency only during the phase error, as demonstrated in Fig. 2. This indicates most of the analog "continuous" behavior of the PLL blocks happens during the phase detection. The rest of the cycle the PLL exhibits constant response with the exception of the leakage impact.

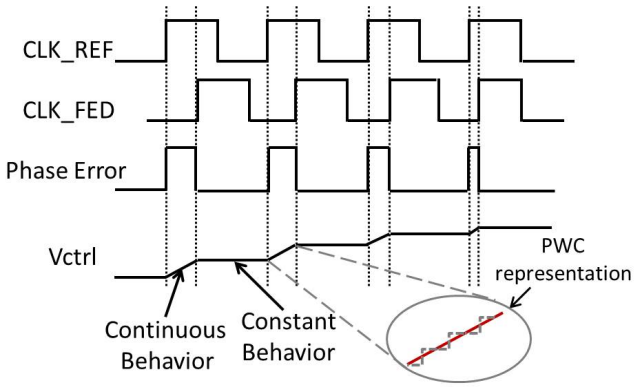

Fig. 2. PLL dynamics with non-linear characteristics

By exploiting the non-linear characteristics of the PLL, analog signals (like currents and voltages) can be expressed by PWC waveforms with fine time steps (fast events) only during the phase error, as demonstrated in Fig.2. During the rest of the reference cycle, the behavior is considered constant, and no events need to be created. This implies most of the simulation run time will be consumed during phase/frequency acquisition when the PLL reacts to high phase errors to acquire lock, while during the locked state, the simulation run time is extremely fast.

Furthermore, in practical circuit implementation, analog signals are not ideal and may exhibit non-linearity. This includes charge pump currents that could change based on the integrated voltage value across the loop filter capacitor. Also, the VCO Frequency-Voltage (F-V) curve won't be linear for the entire range. To address this non-linearity, look-up tables have been created to match actual circuit behavior and provide better correlation with the PLL complete system response. This will be demonstrated in the following sub-sections.

Moreover, noise models have been created to predict the PLL output jitter and phase noise. VCO thermal noise is considered the main contributor to the PLL phase noise. The VCO circuit has been simulated using Spice in open loop with thermal noise, and then the output clock jitter is measured. The resulting jitter is modeled as Gaussian random noise and added to the VCO output clock. Then the model open loop phase noise is compared against Spice to match the VCO circuit performance. Finally, closed loop simulations were run using the model to estimate the PLL output phase noise. Future enhancement will include VCO flicker, supply, and reference clock noises.

B. *Example PLL Model:*

The model is applied to the PLL introduced in [9] which utilizes a sample-reset loop filter (SR-LF) to have a ripple-free control signal. The loop filter is modified and the PLL system time-domain behavioral model is shown in Fig. 3. During the phase error between the reference and feedback clocks, the Charge-Pump (CP) pumps proportional current I_{cpp} and integral current I_{cpi} to be integrated through the SR-LF and form the VCO control voltage V_{ctrl}. The equation that governs this behavior is shown in Fig.3. All currents, capacitors, and voltages are modeled as real numbers. Fine time steps representing Δt are applied only during the phase error. Every rising edge of the reference clock, the SR-LF resets C_{2A} to V_{rst} with an *abrupt* slope, so all proportional charges are lost and the loop filter maintains only the integral charges. This is required for loop stability.

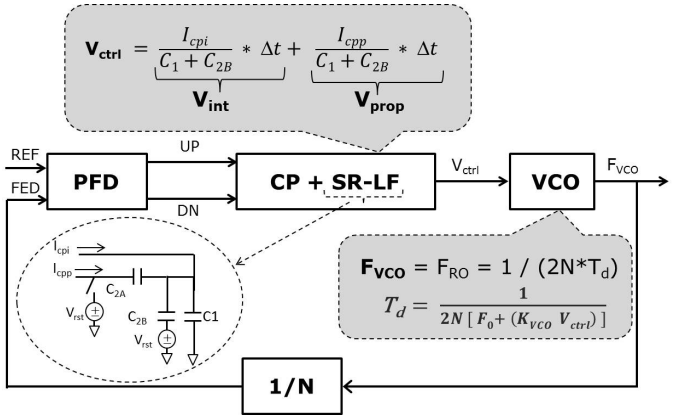

Fig. 3. SR-LF Based PLL Behavioral Model

Ideally, I_{cpp} should have constant value; however, due to circuit non-linearity, its value is dependent on the voltage across C_{2A} as demonstrated in Fig.4 (a). To address this, look-up tables have been extracted from circuit simulations across different PVT corners, and added to the model to have better matching with the circuit behavior. As shown in Fig.4 (a), the modeled proportional current I_{cpp} at typical and -40°C provides good correlation with the actual circuit behavior.

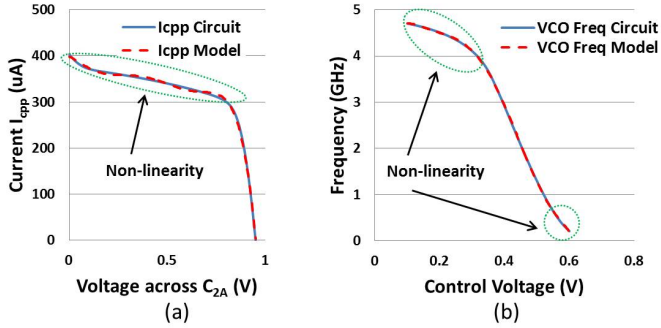

Fig. 4. PLL System non linearity look-up table for PVT at typical,-40°C, (a) Charge pump proportional current, (b) VCO Frequency

The VCO is modeled as a 3-stage ring oscillator. The ring oscillator frequency F_{RO} is shown in equation (1). The VCO

frequency is governed by (2). By equating (1) and (2), each stage delay (T_d) of the ring oscillator can be represented as a function of the number of stages (N), control voltage (V_{ctrl}), VCO gain (K_{vco}), and VCO initial frequency (F_0), as demonstrated in Fig.3. As mentioned previously, all voltages and frequencies are modeled as real numbers, to be updated only during the phase error. To address the F-V VCO non-linearity, a look-up table has been created to provide better correlation with the actual VCO circuit behavior as demonstrated in Fig.4. (b).

$$F_{RO} = 1 / (2N*T_d) \quad (1)$$

$$F_{VCO} = F_0 + K_{VCO} * V_{ctrl} \quad (2)$$

The rest of the PLL blocks, PFD and loop divider, are described in RTL using System Verilog with no modeling techniques required as these blocks are implemented digitally.

III. PLL Model Simulation Results and Applications

A. *Model results and correlation with Full Spice:*

Fig. 5 shows the locking behavior of the PLL before optimization compared against different types of simulations, including a Verilog-A model created for the same PLL. The proposed model has more than 97% correlation with Full Spice with only 1 second of run time. Correlation is measured by how much the model deviates from Full Spice in terms of time domain dynamics and phase noise. There is a slight offset in the final VCO control voltage due to the slight mismatch of the F-V curve with the actual circuit. Table.1 summarizes the simulation time and accuracy compared against other models.

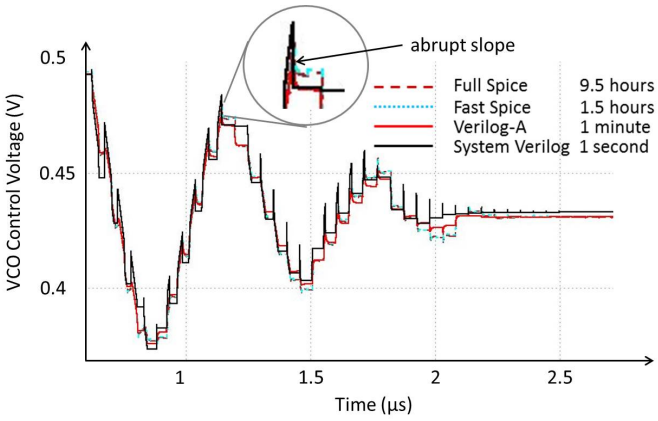

Fig. 5. PLL locking behavior

Table 1: PLL 5µs simulation time and accuracy

	Run Time	Correlation with Full Spice
Full Spice	**9.5 hours**	**N/A**
Fast Spice	**1.5 hours**	**99.99%**
Verilog-A	**1 minute**	**98.8%**
System-Verilog	**1 second**	**97.6%**

Noise models are then turned on to analyze jitter and phase noise. Fig.6 compares the phase noise results with Full Spice simulation. The PLL measures 0.64ps rms period jitter and -103 dBc/Hz at 10MHz offset, which matches well with Full Spice. The Spice open loop phase noise looks higher than the model in the low frequency range due to the flicker noise that is not modeled in the current work.

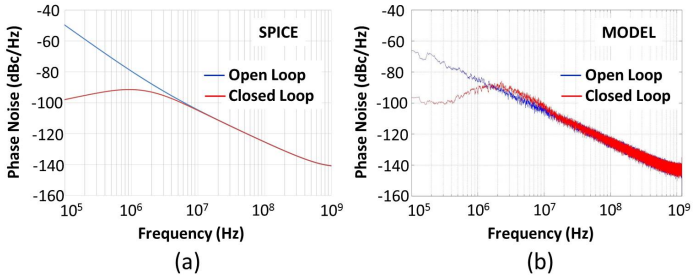

Fig. 6. PLL Phase Noise (a) Full Spice, (b) System Verilog Model

B. *Model Applications in top-down design methodology:*

Prior to the lengthy mixed-signal Spice simulations, the model is utilized to exercise critical features and determine the proper settings and configurations. Fig.7 shows the PLL output frequency using two different loop bandwidths with Spread Spectrum Clocking (SSC) enabled. The SSC feature modulates the PLL frequency at 0.5% down spread at 32 KHz modulation frequency. Proper loop bandwidth has been determined for optimum PLL performance using this model.

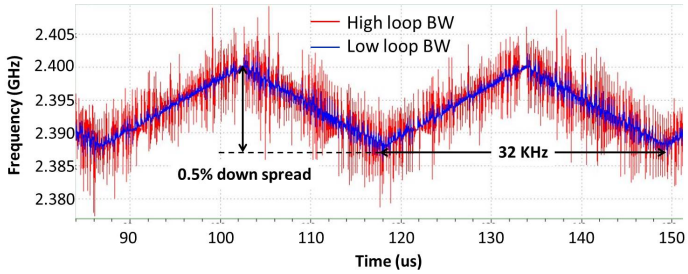

Fig. 7. PLL output frequency in SSC mode (Verilog Simulation)

Fig.8 is another simulation example utilizing the model to optimize the PLL Adaptive Frequency System (AFS) feature [1]. Different sensitivities to supply voltage droops are demonstrated. Based on PLL output frequency overshoot, accumulated phase error, and relock time, frequency sensitivity can be determined for optimum performance.

C. *Model Applications in pre-silicon validation:*

The proposed System-Verilog model fits well in a pure digital pre-silicon validation environment to provide better validation coverage. Fig.9 shows a glitch caught using the model when validating a feature named Zero Distribution Latency to Full Distribution Latency (ZDL-to_FDL) that is used to reduce clock distribution power [10]. This feature runs the PLL in a tight loop (feeds the pre-distribution clock to the loop divider), then switches to full loop (feeds the post-distribution clock to the loop divider) when the PLL frequency is close to the target. Validating such a feature requires

running many test vectors as well monitoring the input to the loop divider to avoid glitches during the switching event. The model was able to catch glitches during the switch in limited scenarios, and fixes are identified and implemented.

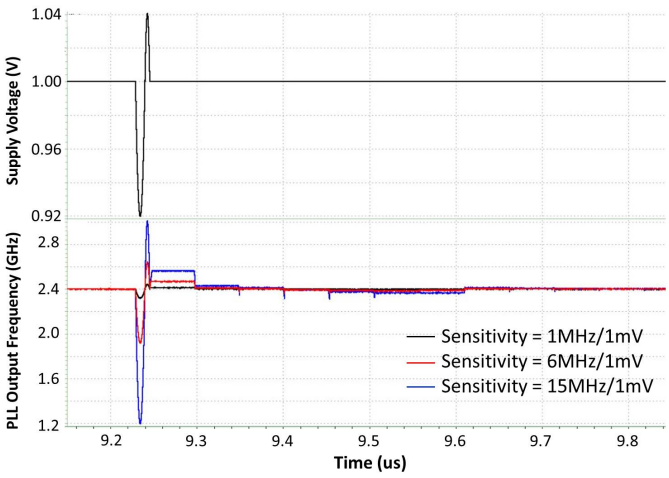

Fig. 8. Adaptation of PLL model output frequency to supply droops

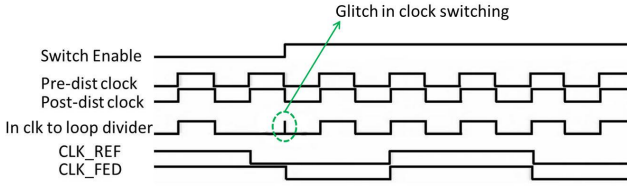

Fig. 9. PLL model catching a glitch in pre-silicon validation for ZDL-to_FDL feature

Fig.10 shows another bug caught by the model when validating the SSC feature. There was a wrong connection in the sigma-delta modulator (SDM) block that is used to provide fraction steps to the loop divider, which caused brief none monotonic output frequency.

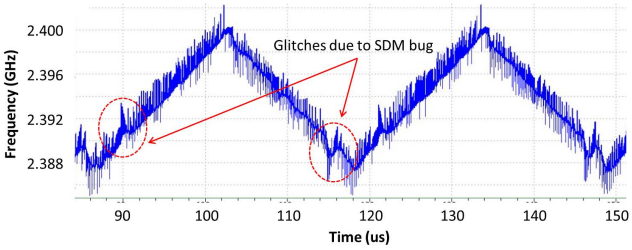

Fig. 10. PLL model catching glitches in pre-silicon validation for SSC feature

Finally, Table.2 compares the performance of the model with other techniques presented in the literature.

V. Conclusion

We presented a pure digital System-Verilog behavioral model for charge-pump PLLs that runs in only 1 second. The model makes use of the PLL characteristics where most of its analog behavior is demonstrated during phase detection. The model integrates nicely with pre-silicon validation framework, and is capable of catching real design bugs that require lengthy mixed-signal simulations. In addition, the model is used to quickly exercise critical PLL features such as SSC and AFS. The model has showed more than 97% correlation with Full Spice simulations and up to four orders of magnitude shorter run time.

Table2: Model Comparison with other techniques

	[5]	[7]	[8]	**This**
Model	HDL-A	S-Verilog	S-Verilog	S-Verilog
Type	Analog	Digital	Digital	Digital
Technique	-	PWL	PWL	PWC
Modeled slopes	Cont/ abrupt	Only Cont	Only Cont	Cont/ abrupt
Run time	24 hrs	-	4.4 sec	1 sec
Correlation	99%	-	-	97.6%

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