An Eight Channel Analog-FFT Based 450MS/s Hybrid Filter Bank ADC With Improved SNDR for Multi-Band Signals in 40nm CMOS

[1]Hundo Shin, [1]Rakesh Kumar Palani, [1]Anindya Saha, [2]Fang-Li Yuan, [2]Dejan Markovic, [1]Ramesh Harjani
[1]University of Minnesota, Minneapolis, MN 55455; [2]University of California, Los Angeles, CA 90095

***Abstract*—We present a fully integrated hybrid filter bank ADC based on an analog-FFT geared for baseband signal processing in wireless receivers. The design consists of an 8-point A-FFT for an analysis filter bank, a VGA bank and a sub-ADC bank in the analog domain, and an inverse VGA bank, calibration and inverse FFT for the synthesis filter in the digital domain. The proposed structure enables the signals in each channel of the 450MHz wide band system to be separately digitized using the full dynamic range of the ADC. The prototype is implemented in TSMC's 40nm CMOS GP process. A hybrid filter bank ADC does not have a constant average noise floor and is best used when both large and small signals are present. After calibration, the reconstructed signal with an asymmetric (40dB difference) two tone input, i.e., one large at 1MHz and one small at 225.05MHz shows 55.7dB of image rejection. The SNDR of the smaller signal improves by 6.0dB in comparison to a non-channelized ADC. The total power consumption for both the analog and digital sections is 90.4mW. As far as we are aware this is the first integrated implementation of the full hybrid filter bank principle.**

I. Introduction

To accommodate the increased data rates of wireless terminals, mobile communications is moving towards carrier aggregation and multi-band operation. Hence, there is a desire to replace the multiple narrow-band receivers with a single wide multi-band one. Time-interleaved ADCs [1] and mixer-based channelizers [2] have limitations for wideband digitization. Time interleaving reduces the speed requirement of the individual ADCs, but the dynamic range requirement remains the same. Mixer based channelizers are able to reduce both the speed and dynamic range requirement of the individual ADCs. However, reconstruction of the signal is problematic due to the phase distortion of the IIR LPFs used after down conversion. Additionally, the mixers, PLLs and LPFs can be power hungry, and harmonic mixing due to spurs can severely distort the channelized signal.

A FFT based hybrid filter bank ADC [3] reduces the speed and dynamic range requirement for the ADCs through channelization in a manner similar to the mixer approach. However, here the mixers are replaced by down sampling to perform the frequency shift operation which reduces power consumption. Unlike in the mixer approach in a hybrid filter bank a complex filter precedes the down conversion process and avoids signal aliasing. The channelized signal is then readily reconstructed by synthesis filters in the digital domain. In this paper, a prototype hybrid filter bank ADC based on an FFT-IFFT analysis-synthesis filter pair is shown.

II. Analog-FFT Based Hybrid Filter Bank ADC

Fig. 1 shows the detailed structure for the analog-FFT (A-FFT) based hybrid filter bank ADC. An 8-point A-FFT with

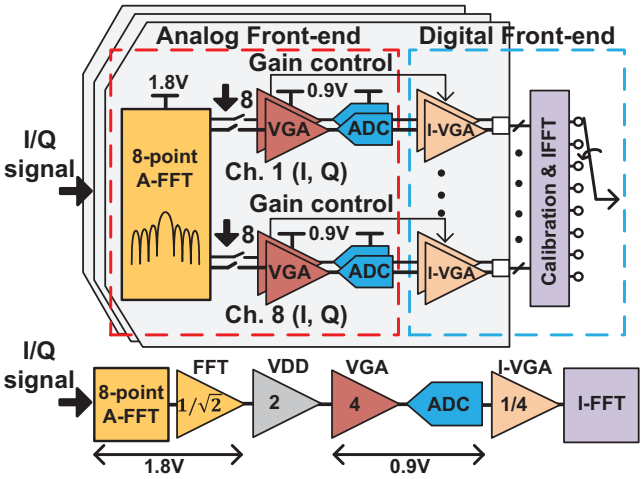


Fig. 1: Overall structure of the analog-FFT based hybrid filter bank ADC

rectangular windows is employed as the 8-channel analysis filter. Each channel provides a *Sinc* transfer function with different center frequencies. The linear phase characteristic of the A-FFT facilitates the reconstruction of the signal.

Each of *Sinc*s of the A-FFT places a notch at the center frequency of the other channels resulting in high channel selectivity. For the 8-point A-FFT in the prototype, the sampling frequency of each channel after the A-FFT is decimated by 8 so as to fold each of the channels to DC which enables low speed VGAs and ADCs to be used. Even though the signal is down-sampled by 8, there is no information loss due to the orthogonal relationship between the channels. The A-FFT is followed by a bank of VGAs to amplify the channelized signals to the maximum signal range of the ADC. This operation enables even small signals to be digitized with the full ADC dynamic range without worrying about signal saturation that may have resulted from a large signal. After A/D conversion, the amplitude of each signal is recovered by the inverse VGA bank (I-VGA), i.e., if the gain in the channel is large due to presence of only small signals then the inverse gain at the I-VGA is also large such that the quantization noise is reduced. After the I-VGA, signals from all the channels is recombined to the original by the I-FFT. During the I-FFT operation, the quantization noise of each channel is *Sinc*-shaped and shifted to the corresponding band at full rate, f_s. This operation reduces the quantization noise of both the large and small signals due to the VGA gain, but the effect is more significant for smaller signals due to the larger VGA gain.

Fig. 2(a) and (b) show simulation results for a single ADC and an 8 channel hybrid filter bank ADC each with 20MHz wide 16-QAM modulation signals. The difference in amplitude

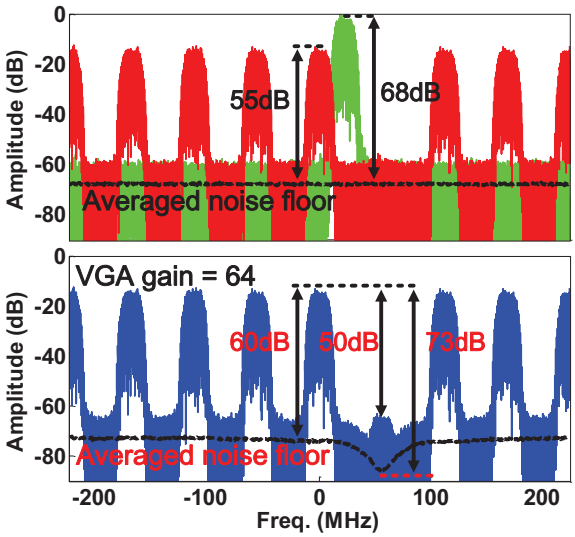


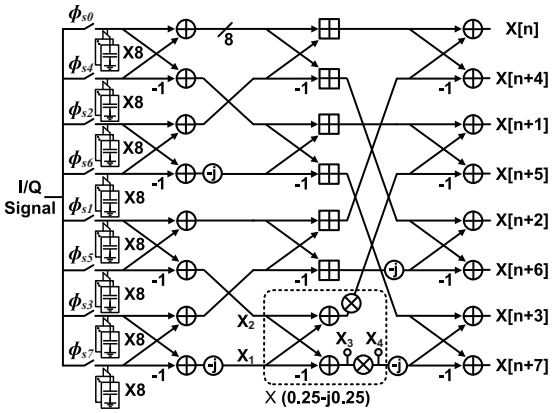
Fig. 2: (a) Simulation result for single 8bit, 450MS/s ADC (b) Simulation result for proposed structure

between the largest and smallest signal is 50dB. For both the single ADC and the A-FFT the input peak-to-peak amplitude is 1V. The simulation was performed with 8 bit ADCs and with VGAs having a maximum gain of 64.

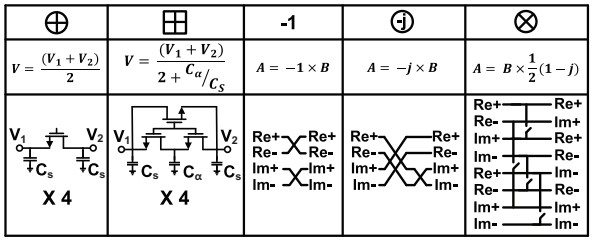
Fig. 2(a), shows the output spectrum for a single modulated signal in green and the output spectrum for a multi-signal input with seven large and one small signal, in red, all using a single ADC. For the single modulated signal, the signal-to-noise floor ratio is 68dB, but for the multi-band signal it decreases to 55dB due to increased peak to average power ratio (PAPR). Additionally, the small signal in the 6th channel is completely lost here. In Fig. 2(b) we note that after A/D conversion with the proposed channelization scheme, the average noise floor for both the large and small signals is lower than for the single ADC. In particular, the noise floor close to the large signal is 60dB below the peak signal amplitude resulting in a 5dB improvement in SNR. For the small signal, the noise floor is 73dB below the peak signal amplitude and results in an 18dB improvement in SNR. For this channelizer, the noise floor difference between the channels with the large and small signals is 13 dB. However, if small and large signal are very close to each other in the same channel then the performance degrades. This problem can be solved by increasing the number of channels at the cost of increased complexity.

For continuous operation, 3 copies of the A-FFT are time-interleaved. For the 8-channels, a total of 48 VGAs and ADCs (3 copies of 8 channels, I/Q signals) were implemented in the analog domain. In the digital domain, 48 I-VGAs, calibration and I-FFT block are used for signal reconstruction.

Quantization in the sub-ADC confines the quantization noise to that channel. This leads to an increase in the quantization noise in the whole bandwidth after the synthesis filter [4]. The total quantization noise power increases by a number of channels(N)(8 in this case). In order to maintain the same SNR as a single ADC, we need to have a gain of $\sqrt{N}$ in front of



(a) Trellis structure for the 8-point A-FFT



(b) A-FFT math operations and realizations

Fig. 3: Trellis structure and circuit implementation for the 8-point A-FFT

the sub-ADCs. A simplified channelization model is shown at the bottom of Fig. 1 for the small signal case. The passive A-FFT has an attenuation of $\sqrt{2}$. The maximum VGA gain in this design is 4 leading to an overall gain of $\sqrt{8}$ before the sub-ADCs. The A-FFT operates with a V_{dd} of 1.8V. The ADC and VGA use a 0.9V V_{dd}. This inherently reduce the quantization noise by a factor of two (due to the lower V_{dd}) resulting in an effective gain of 2. The overall gain before the sub-ADC is thus $2\sqrt{8}$. However, we require a gain of $\sqrt{N} = \sqrt{8}$ to maintain the same SNR as a single wideband ADC. The extra gain of 2 leads to a 6dB improvement in overall SNR as discussed in the measurement section

III. Circuit Implementation

A. Analog-FFT

For the analysis filter bank, decimation-in-time 8-point A-FFT was designed using charge re-use techniques for low power consumption [5]. In this structure, signal processing is performed via passive operations (charge sharing, charge stealing, and wire-swapping). This passive scheme ensures high speed, high linearity and low power consumption. Additionally, these simple switch based operations improve with technology scaling.

The trellis structure for the A-FFT is shown in the Fig. 3(a). Each input sample is stored on a set of 8 capacitors (2 copies each of the pseudo-differential, complex inputs) for the butterfly operation, and a total of 64 capacitors and sampling switches are used for this 8-point FFT operation. The necessary switches for these operations are shown in Fig. 3(b). The complex number coefficients required for the

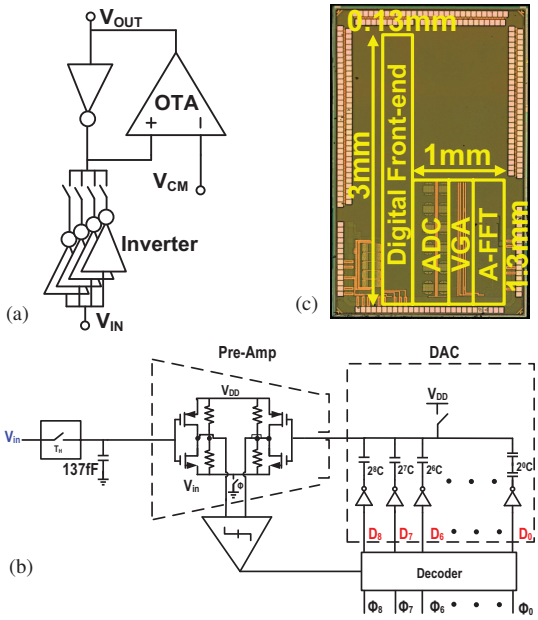


Fig. 4: (a) Circuit diagram for the VGA (b) Circuit diagram for the ADC (c) Die microphotograph (includes addition circuits [6])

multiplication operation of this 8-point FFT is *0.25 - j0.25* in Fig. 3(a). This multiplication can be separated into two phases as shown in *Eq.(1)*, and the coefficient of 2nd operation, *0.5 - j0.5*, can be implemented as done in *Eq.(2)*.

$$X_3 = 0.5 \cdot (X_1 + X_2); \quad X_{R,4} + jX_{I,4} = X_3 \cdot (0.5 - j0.5) \quad (1)$$

$$\begin{aligned} X_{R,4} + jX_{I,4} &= (X_{R,3} + jX_{I,3}) \cdot (0.5 - j0.5) \\ X_{R,4} &= 0.5 \cdot (X_{R,3} + X_{I,3}); \quad X_{I,4} = 0.5\,(-X_{R,3} + X_{I,3}) \end{aligned} \quad (2)$$

This multiplication operation was implemented in two clock periods. This technique reduces the number of switches, the dynamic power consumption, the area and wire-routing complexity by half at the cost of one additional clock period in comparison with [5]. The A-FFT was implemented with I/O devices to handle the large PAPR of multi-band signals. Each sampling capacitor is 500fF and the V_{dd} is 1.8V.

B. VGA and ADC

The circuit diagram for the inverter-based single-ended VGA is shown in Fig. 4(a) [7]. The OTA in the feedback loop forces the amplitude of output to be the same as the input voltage, canceling out the nonlinear currents produced by the inverters. For our first prototype, used to validate the hybrid filter bank approach, only two gains (1 and 4) were used for the VGA. The gain is controlled by the ratio of inverters. The VDD for the unused inverters are disconnected to reduce power consumption. The circuit diagram for the sub-ADC is shown in Fig. 4(b). This ADC has low input capacitance due to an active gate leakage cancellation scheme, which eases the design constraints on the preceding sampler and input buffer. The VGA and the sub-ADC use a 0.9V VDD, and the sub-ADC was designed for 9bits. We are able to use a lower VDD for the VGA and sub-ADC and use higher performance core

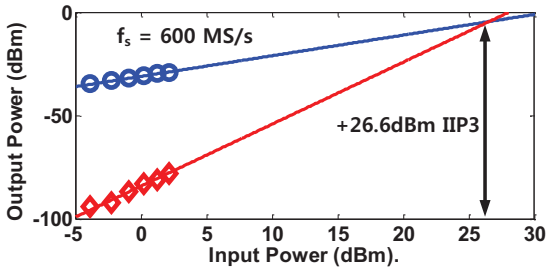


Fig. 5: Measured IIP3 of the 8-point A-FFT (all channels are similar)

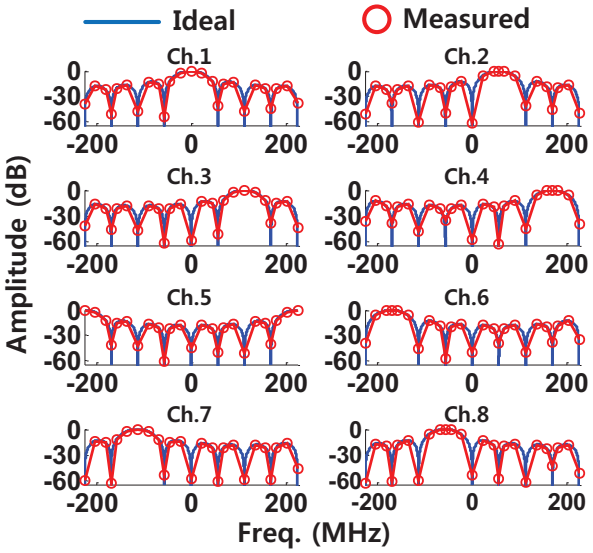


Fig. 6: Measured frequency response of individual A-FFT channels

devices because the individual channel outputs for the A-FFT have lower amplitudes due to the reduction of the PAPR.

IV. Measurement Results

The hybrid filter bank was implemented in TSMC's 40nm GP process and a micrograph is shown in Fig. 4(c). The analog area is 1.3 mm^2 and the digital area is 0.39 mm^2. The integrated I-FFT is included in the digital front-end and bundled with other functions [6]. In this paper, the output of the I-VGA was measured. Calibration and I-FFT operation was performed off-chip due to limited signal access.

The A-FFT was tested independently using 50 Ω matched baluns and the measured IIP3 of 26.6dBm for the A-FFT is shown in Fig.5. A two-tone input signal with 150MHz center frequency and 20kHz spacing was applied at 600MS/s operation. This high linearity is a direct result of the passive operation and the large signal handling capability of I/O devices. The measured ENOB of the fabricated 9 bit 34MS/s rail-to-rail input ADC was 8.5 bit. The signal swing at the output of the VGA is half the supply due to head room requirements of the VGA. This unfortunately leads to an maximum attainable ENOB of 7.5 bit. The ADC data is captured on the 8M byte onchip memory. Each channel is tested separately to study the channelization and data is combined externally using an I-FFT. The system has three time interleaved hybrid banks for real time data output. The frequency response of the analysis filter bank (A-FFT,VGA,ADC) is plotted in Fig. 6. The red circles

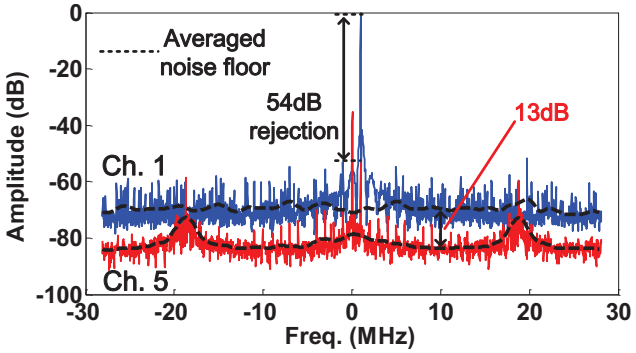


Fig. 7: Measured output spectrum before reconstruction

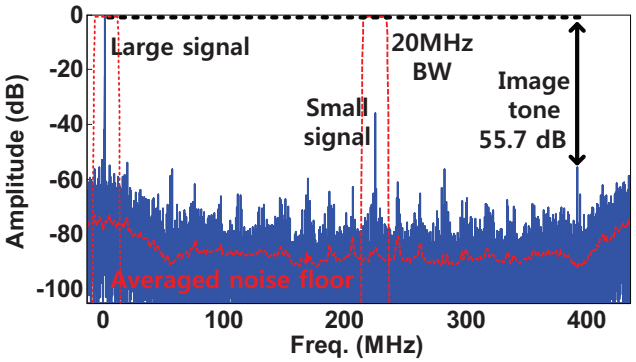


Fig. 8: Measured output spectrum after reconstruction

and blue line shows the good match between the measurements and the ideal FFT sinc function.

The sub-ADCs were tested with a single tone and the average SNDR was measured to be 40dB (6.4 bit). The 1 bit loss is likely a result of VGA non-linearity due to non-ideal common mode voltage and gate leakage. Extracted simulations show a gate leakage droop of 6-7mV at the input of the VGA during its conversion time of 58 ns. In order to validate the channelization benefit, a two tone test is performed with a large @1 MHz ($1.584V_{pp,diff}$) and small signal @225.05 MHz ($15.84mV_{pp,diff}$). The large signal is 40dB above the small signal. The large and small signals are separated to channel 1 and 5 and their output spectrums after the I-VGA is shown in Fig 7. The channel 1 spectrum is shown in blue with a VGA gain = 1 and the channel 5 spectrum is shown in red with the VGA gain = 4. The I/Q sub-ADC signal bandwidth spans $\pm$28.125MHz due to the inherent downsampling operation in the FFT. The 1MHz large signal is shown in blue in Fig 7 and 225.05 MHz small signal (shown in red) is down converted to 50kHz. The residual large signal that appears in channel 5 is attenuated by 54dB due to the FFT sinc filter. The small signal is amplified by the VGA gain of 4 before the sub-ADC and hence after the I-VGA we see a 13dB reduction in the quantization noise. Ideally we expect 12dB reduction but due to a +10% VGA gain error, we see a 13 dB reduction.

The output spectrum of the full filter bank (with time interleaving) after I-FFT is shown in Fig. 8. The largest image tone on the Ch. 8 is due to capacitor mismatch in the FFT. The quantization noise is coloured due to the different VGA gains in each channel. Hence, it is lower near the small signal as compared to the large signal. A hybrid filter bank is used when there are a large number of signals and hence a signal bandwidth of 20MHz is assumed for comparison purposes. A sharp band pass filter of 20MHz is placed centered around the large and the small signal. The SNDR obtained for them in 20MHz bandwidths are 47dB and 20dB. The maximum measured SNDR of a channel with VGA gain set to one is 40dB. Hence the system is compared with a single wide band 450MS/s ADC with an SNDR of 40dB. Similar to the channelizer, a sharp band pass filter is placed over the large and small signals and the SNDR of each is estimated to be 54 dB and 14 dB. We see an improvement in the SNDR of the small signal by 6dB as expected from this architecture. This architecture facilitates selectively amplifying small signals in the presence of large signals. In this prototype we see an improvement of only 6dB due to the max VGA gain of 4. However for VGA gain steps of 8,16, the expected improvement is 12 and 18 dB. The total power consumption of this design is 90.4mW. The 3 copies of the analog FFT and the state machine consume 14.4mW, and the 48 copies of the VGA and the ADC consume 30mW and 40mW, respectively. Power consumption for the digital is 6mW.

V. Conclusion

In this paper, a prototype hybrid filter bank ADC based on a A-FFT is demonstrated in 40nm CMOS process. This is the first integrated implementation of a hybrid filter bank ADC. The hybrid filter bank enables improved SNR for small signals in presence of out of band large signals or blockers. In this prototype, we see a 6dB improvement in SNR for the small signal in comparison with a single wide band ADC by using a VGA of gain 4. However, with higher VGA gain steps of 8, 16, we expect an improvement of 12 and 18 dB. This filter bank was designed for a wideband signal classifier engine [6] but is equally useful for next generation radio receivers with carrier aggregation and multi-band operation.

Acknowledgment

This research was funded by the DARPA CLASIC program.

References

[1] I. D. ODonnell and R. W. Brodersen, "An ultra-wideband transceiver architecture for low power, low rate, wireless systems," *IEEE Transactions on Vehicular Technology*, vol. 54, no. 5, pp. 1623–1631, 2005.

[2] V. Singh *et al.*, "A 16-band channelizer employing harmonic rejection mixers with enhanced image rejection," *IEEE Proceedings of the Custom Integrated Circuits Conference*, pp. 1–4, 2014.

[3] S. R. Velazquez and T. Q. Nguyen, "Design of hybrid filter banks for analog/digital conversion," *IEEE Transactions on Signal Processing*, vol. 46, no. 4, pp. 956–967, 2002.

[4] P. Lowenborg and H. Johansson, "Quantization noise in filter bank analog-to-digital converters," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1199–1211, 2013.

[5] B. Sadhu *et al.*, "Analysis and design of a 5 GS/s analog charge-domain FFT for an SDR front-end in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 5, pp. 1199–1211, 2013.

[6] F.-L. Yuan *et al.*, "A throughput-agnostic 11.9-13.6GOPS/mW multi-signal classification soc for cognitive radios in 40nm CMOS," in *IEEE VLSI Circuits Symposium*, June 2015, pp. 10–3.

[7] R. K. Palani and R. Harjani, "High Linearity PVT Tolerant 100MS/S Rail-to-Rail ADC Driver with Built-in Sampler in 65nm CMOS," *IEEE Custom Intergrated Circuit Conference*, Sep. 2014.