A Voltage Doubling Passive Rectifier/Regulator Circuit for Biomedical Implants

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***Abstract*- A circuit called prectulator is proposed in this paper. It utilizes the output transistor (M_{PR}) of a linear regulator also as a passive rectifier for providing a regulated DC output from an AC input. The bulk voltage and the gate voltage (V_G) of M_{PR} are biased by an auxiliary rectifier and an error amplifier (A_E), respectively. During startup and overload situations, overdriving M_{PR} may occur and is prevented by limiting V_G inside A_E. Using this technique, a voltage doubling prectulator was implemented in a 0.18μm CMOS process. At 15MHz with a peak AC voltage of 3.6V, a power efficient of 87.7% and a voltage conversion ratio of 1.67 were achieved for a 6V output with a load power of 46.8mW.**

1. Introduction

Power management is one of the most important and challenging aspects in the design of a biomedical implant. Although alternative methods for harvesting energy from different energy sources such as ultrasonic energy source [1] have been investigated, inductive coupling is still the most common method for delivering power wirelessly to the implants from an external controller (EC) outside the body. The EC usually consists of a coil driver driving a primary coil, which is inductively coupled to a secondary coil L_S inside the implant. The received AC power on L_S can be used for supplying different implant circuits directly or for recharging the battery inside the implant. In most implant designs, the received power on L_S is first converted to an unregulated DC voltage using a rectifier. The frequency for delivering the AC power is typically selected to be 13.56MHz [2] or other lower values [3]. Furthermore, in some applications, high DC supply voltages (sometimes higher than the peak AC voltage on L_S) are required for implant circuits such as electrical stimulators. As a result, voltage doubler [2][4] or other step-up converters may be required. Nevertheless, for a simple conventional power management scheme, a rectifier followed by a linear regulator as shown in Fig. 1a is often used for providing a regulated DC supply output. The rectifier in this case is an active design that utilizes the comparator CO_1. When the received AC voltage, V_{AC}, is higher than the unregulated DC voltage, V_{UDC}, CO_1 will turn on M_1. Hence, V_{UDC} will be charged to a value equal to the peak voltage of V_{AC} given as V_{ACP} ideally. However, due to the on-resistance of M_1 and the current flow through M_1 as well as the delay of CO_1, the maximum V_{UDC} is V_D lower than V_{ACP} where V_D is typically in the range between 0.2V and 0.7V [3][5]. The regulated output, V_O, is obtained by regulating the current flow on M_2 using an error amplifier A_E, which adjusts the gate voltage of M_2 until V_O measured through the resistor divider (R_1 and R_2) is equal to the input reference voltage V_{ref}. However, a minimum voltage drop (dropout voltage) given as V_{DO} in the range of 0.2V to 0.4V between V_{UDC} and V_O is required by the linear regulator. As a result, for a desired V_O, the minimum peak voltage requirement for V_{AC}, min[V_{ACP}], is equal to $V_O+V_{DO}+V_D$. Since the voltage conversion ratio, R_V, is defined as V_O/min[V_{ACP}], R_V for a conventional rectifier is typically in the range of 0.7-0.92 [3][5]. If V_{DO} of the regulator is included, R_V will be dropped to the range of 0.65-0.8 [4]. Furthermore, the overall maximum power efficiency, η_P, defined as the power dissipated on R_L (P_L) divided by the input power (P_{in}) from V_{AC} at min[V_{ACP}] is in the range of 65-80% [4] due mainly to the power dissipations on both M_1 and M_2 as illustrated in Fig. 1a. To improve both R_V and η_P, a circuit called *rectulator* that combined an active rectifier and a linear regulator was proposed in [6]. The basic concept is shown in Fig. 1b. If $V_{AC} > V_O$, CO_1 will turn on switch S_1 and turn off switch S_2, allowing amplifier A_E to control the gate voltage of the main transistor M_S such that V_O is regulated to the desired output voltage given as $(1+R_1/R_2)\cdot V_{ref}$. If $V_{AC} < V_O$, CO_1 will turn off S_1 and turn on S_2 such that M_S is turned off with no current flow between V_{AC} and V_O. Since only one transistor is between V_{AC} and V_O, most of the power dissipates on M_S and the voltage drop between V_{AC} and V_O given as V_S is only one source-to-drain voltage drop. Hence, both R_V and η_P can be improved. However, when f_{AC} increases to over 10MHz, η_P starts to degrade due to the limitations on the response time of CO_1. In this paper, a technique that combines a *passive* rectifier and a linear regulator (called prectulator) without using a comparator is proposed. Since there is no speed limitation due to comparator, the proposed technique can achieve a higher f_{AC}. Based on this technique, a voltage doubling prectulator was designed for powering biomedical implants using a f_{AC} of 13.56MHz or higher.

2. Proposed Passive Rectifier/Regulator Combo Technique

Similar to the rectulator, the proposed prectulator technique has only one transistor between V_{AC} and V_O as shown in Fig. 2a. However, unlike the rectulator in [6], the output transistor M_{PR} is not only used for controlling the output current I_O but also used as a passive rectifier directly without using a comparator. This can be achieved if the bulk terminal voltage, V_B, is always higher than $V_{ACP} - V_{Di}$ and $V_O - V_{Di}$ where V_{Di} is the forward bias voltage of a PN junction diode (~0.65V). In this case, the parasitic bipolar transistor associated with M_{PR} will not turn on for the given ranges of V_{AC} and V_O. V_B is obtained from an auxiliary rectifier, which can be realized using a Schottky diode as shown in Fig. 2b. For a process that does not provide Schottky diode, MOS realization, for example, based on bootstrapping technique [3] as shown in Fig. 2c can also be used for generating V_B with a rectifier voltage drop less than V_{Di}. If the threshold voltage of the NMOS is < ~0.45V, a diode-connected NMOS can be used directly for the auxiliary rectifier. Since the current drawn from V_B is relatively small, the η_P of the auxiliary rectifier has negligible contributions on the overall η_P of the prectulator.

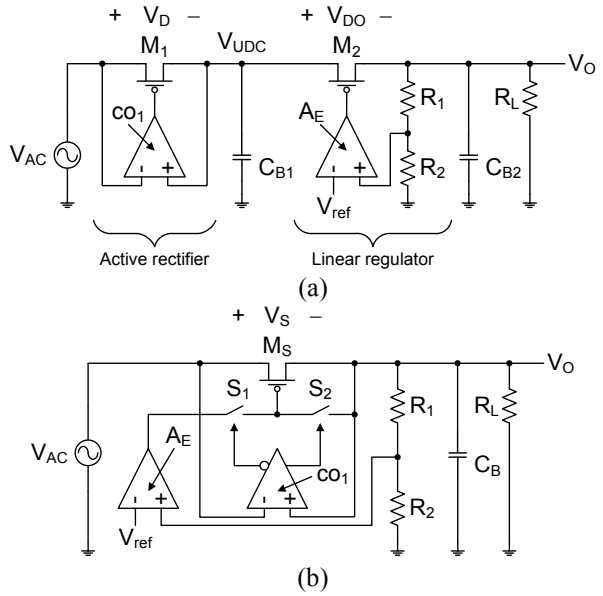

Fig. 1: Powering implant based on (a) conventional method and (b) active rectifier/regulator combo circuit proposed in [6]

For $V_{AC} > V_G + |V_{TP}|$ and $V_{AC} > V_O$, I_O will flow from V_{AC} to V_O as shown in Fig. 2a where V_{TP} is the threshold voltage of M_{PR}. To have a regulated V_O, the average I_O, I_{Oavg}, is adjusted by controlling V_G, which is determined by the feedback loop that consists of R_1, R_2 and A_E. V_G is assumed to be relatively constant. For a given reference input voltage, V_{ref}, the desired V_O is equal to $(1+R_1/R_2)\cdot V_{ref}$. By considering M_{PR} as the output transistor of a linear regulator that has an equivalent transconductance, design techniques for linear regulator can be applied to design the prectulator. For $V_{AC} < V_O$, M_{PR} should be off ($I_O = 0$) with $V_G > V_O - |V_{TP}|$. This condition is satisfied if A_E does not overdrive M_{PR} into triode region even for large I_L when V_{AC} is greater than V_O. To achieve this, A_E is required to limit the range of V_G when the situation of overdriving M_{PR} is detected as discussed below.

3. Proposed Voltage Doubling Prectulator Design

To maximize the DC output voltage from the AC input, a voltage doubling prectulator is proposed as shown in Fig. 3. It consists of two prectulators – p-prectulator and n-prectulator, which rectify the AC input, V_{AC}, and produce a regulated positive output, V_{OP}, and a regulated negative output, V_{OM}, respectively. The total output voltage, V_{OC}, equal to $V_{OP} - V_{OM}$ is doubled when compared to the one shown in Fig. 2a. The ideal values of V_{OP} and V_{OM} are equal to $(1+R_{T1}/R_{T2})\cdot V_{Tref}$ and $(1+R_{B1}/R_{B2})\cdot V_{Bref}$, respectively, where V_{Tref} and V_{Bref} are reference input voltages. For the selected process, Schottky diode is available and is used for realizing the auxiliary rectifiers. Since the currents drawn by the amplifiers – A_T and A_B are relatively low, their supply voltages (V_{DD}, ground and V_{SS}) are provided by the auxiliary rectifiers. To extend the range of V_{AC} to about double of the maximum drain-to-source voltage limits of the MOSFETs, M_{T1} and M_{B1} are added. For the positive cycle of V_{AC}, M_{T1} is on with its source voltage, V_{ACT}, following V_{AC}. For the negative cycle of V_{AC}, M_{T1} is off. V_{ACT} will stay at ~0V. As a result, both M_{T1} and M_{T2} only see a maximum swing of about half the peak-to-peak value of V_{AC}. Similarly, M_{B1} is added to reduce the voltage swing seemed by both M_{B1} and M_{B2} in the n-prectulator.

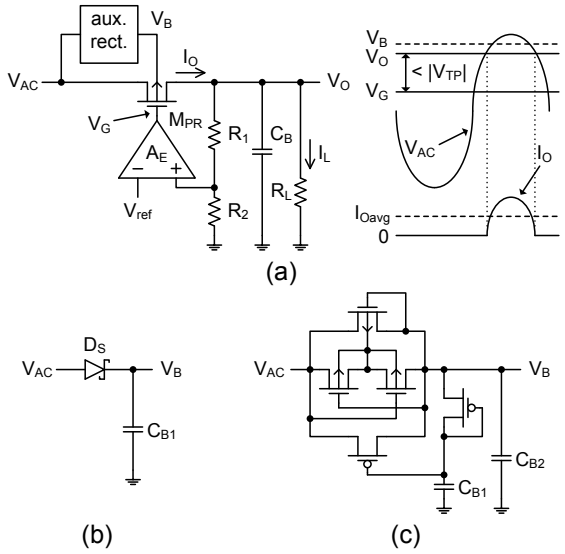

Fig. 2: (a) conceptual prectulator design and auxiliary rectifier design based on (b) Schottky diode and (c) MOS realization

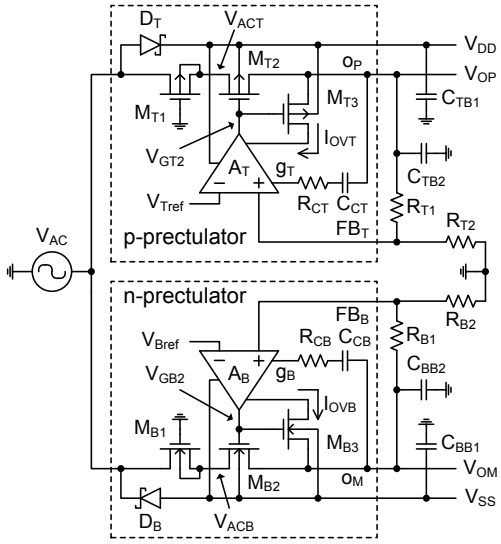

Fig. 3: Proposed voltage doubling prectulator

In the p-prectulator, during startup with V_{AC} being applied initially, the gate voltage of M_{T2}, V_{GT2}, is ~0V. When M_{T2} is turned on for increasing V_{AC}, V_{OP} can be charged to a voltage higher than one $|V_{TP}|$ above ground. Hence, M_{TP} can be overdriven and current flow back from V_{OP} to V_{AC} can occur for $V_{AC} < V_{OP}$. As a result, V_{OP} cannot be charged up further. In addition, for $V_{OP} < (1+R_{T1}/R_{T2})\cdot V_{Tref}$, A_T will try to increase V_{OP} by holding V_{GT2} at ~0V. Hence, V_{OP} will be stuck below $(1+R_{T1}/R_{T2})\cdot V_{Tref}$ as observed in simulations. This startup situation is similar to the situation of overdriving M_{RP} in Fig. 2 for large I_L as discussed in Section 2. Similar overdriven situations can also occur to M_{B2} in the n-prectulator.

To detect overdriven situations on M_{T2} in Fig. 3, M_{T3} is added in the p-prectulator. When overdriven situations occur, V_{GT2} is less than $V_{OP} - |V_{TP}|$. Hence, M_{T3} will turn on and

conduct a current of I_{OVT}, which is used in A_T to prevent M_{T3} from being overdriven. Fig. 4 shows the design of A_T. Similar to a conventional low dropout regulator design, it consists of a high gain folded-cascode input stage (M_{11} – M_{20}) and a low impedance source follower stage (M_{21} – M_{22}) that drives the output transistor M_{T2}. Capacitor C_{AT} is for keeping V_{GT2} relatively stable. The overall frequency response is compensated by R_{CT} and C_{CT} shown in Fig. 3. M_{21} in Fig. 4 is a native NMOS. It allows A_T to have sufficient output swing to drive V_{GT2} close to V_{DD} under low I_L conditions. If M_{T2} is overdriven with $V_{GT2} < V_{OP} - |V_{TP}|$ in overdriven situations discussed above, M_{T3} will conduct a non-zero I_{OVT} that has a maximum value equal to the drain current of M_{22} (I_{D22}). In this case, M_{21} will be off and A_T will not continue to drive V_{GT2} below ~($V_{OP} - |V_{TP}|$). To keep M_{T2} from being overdriven, the width-length ratio of M_{T3} is selected to be relatively large such that M_{T3} is in subthreshold region to have its source-to-gate voltage less than $|V_{TP}|$ for $I_{OVT} = I_{D22}$. Note that although A_T does not overdrive M_{T2} under startup and high I_L situations to prevent current flow back from V_{OP} to V_{AC}, voltage regulation on V_{OP} can no longer be maintained in these situations.

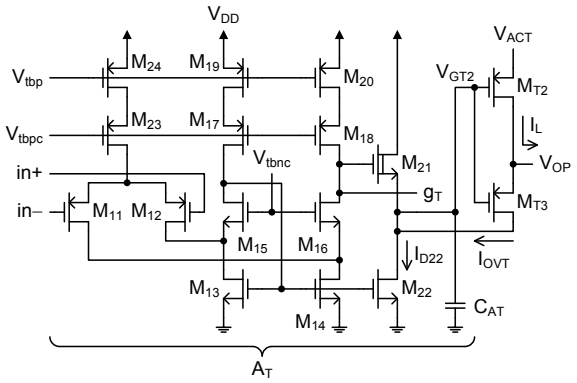

Fig. 4: Design of amplifier A_T

In the n-prectulator (Fig. 3), M_{B3} is used for detecting overdriven situations for M_{B2} such that a current I_{OVB} is generated to prevent A_B from further overdriving M_{B2}. Fig. 5 shows the design of A_B. Unlike the case in A_T, I_{OVB} cannot be used directly to turn off M_{41} in the source follower stage. Instead, I_{OVB} is mirrored to node X in the input stage such that when I_{OVB} is equal to I_{D43}, the output of the input stage and hence, the gate voltage of M_{B2}, V_{GB2}, will not increase further.

4. Implementation and Experimental Results

The voltage doubling prectulator was implemented in a conventional 0.18μm CMOS process. Only 3.3V I/O devices were used. Fig. 6 shows the die photo and the layout of the prectulator. The active area is 560×200 μm^2. R_{T1}, R_{T2}, R_{B1} and R_{B2} in Fig. 3 were selected to have the same value. For testing the prectulator, a 50Ω AC source in series with a 10Ω resistor was used as the input source. The input power to the prectulator, P_{in}, was measured using the 10Ω resistor. Two 1μF bypass capacitors were connected between the prectulator outputs (V_{OP} and V_{OM}) and ground. Fig. 7 shows the input and output waveforms of the prectulator for a f_{AC} of 15MHz. By setting V_{Tref} and V_{Bref}, V_{OP} and V_{OM} were set to +3V and –3V, respectively for a total output voltage, V_{OC}, of 6V. V_{ACP} was set to the minimum value, min[V_{ACP}], which was 3.6V for a change on V_{OC} of < 0.2%. Two 385Ω resistors were connected to V_{OP} and V_{OM} for a total load power, P_L, of 46.8mW. Overload situations with reduction in V_{OC} occurred for further decrease in V_{ACP} or increase in P_L. The power efficiency, η_P, defined as P_L/P_{in} at min[V_{ACP}] and the voltage conversion ratio, R_V, defined as V_{OC}/min[V_{ACP}] were measured to be 87.7% and 1.67, respectively. The startup time (the time from V_{AC} began to apply with V_{OC} = 0V to the time that V_{OC} settled to the final value) was measured to be < 145μs. Fig. 8 shows η_P vs. P_L for different V_{OC}'s at f_{AC} = 15MHz. Higher η_P's were measured for higher V_{OC}'s due to relatively lower voltage drops and losses on M_{T2} and M_{B2}. η_P > 80% were achieved for P_L > 5mW and V_{OC} > 4V. Before overload situations occurred, load regulation was measured to be –1.9mV/mA at f_{AC} = 15MHz. When overload situation occurred with V_{OC} decreased by > 0.1V from a regulated V_{OC} of 4V, η_P dropped < 0.13% for a P_L of ~65mW. This indicated that no significant current flow back occurred during overload situations. The input regulation defined as change on V_{OC} over change on V_{ACP} ($\Delta V_{OC}/\Delta V_{ACP}$) was measured to be 1.1mV/V for V_{OC} = 4V, P_L = 14.5mW and V_{ACP} changed between 2.6V and 4.6V. When AM modulation with different modulation frequencies, f_{AM}'s, were applied to V_{AC}, $\Delta V_{OC}/\Delta V_{ACP}$ vs. f_{AM} were measured as shown in Fig. 9.

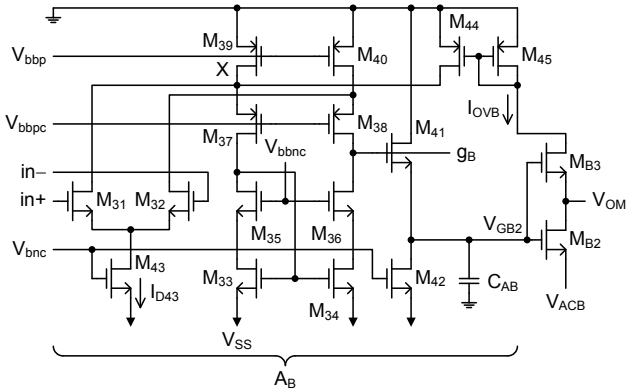

Fig. 5: Design of amplifier A_B

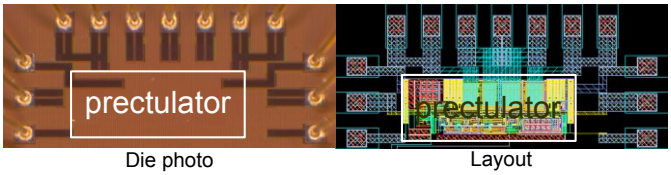

Fig. 6: Die photo and layout

Fig. 10 shows R_V vs. f_{AC} for different V_{OC}'s and P_L's. The voltage drops between the positive V_{ACP} (the negative V_{ACP}) and V_{OP} (V_{OM}) were between ~0.2V for low f_{AC}'s and ~0.7V for high P_L's and f_{AC}'s (up to 100MHz). A maximum R_V of 1.71 was measured at 15MHz. Fig. 11 shows η_P vs. f_{AC} for different V_{OC}'s and P_L's. Current measurements from V_{AC} became inaccuracy for f_{AC} ≥ 20MHz. Very high R_V (> 1.8) and η_P (> 93%) were measured at low f_{AC} (≤ 1MHz). Table I compares the performances of recent published works and the proposed prectulator. The prectulator achieved higher R_V when compared to the design that used a voltage doubler rectifier followed by regulators [4]. The prectulator also

achieved high η_P's at high f_{AC}'s. Notice that both positive and negative cycles of V_{AC} were utilized for supplying the load current in [6]. Hence, its load regulation at 5MHz was better.

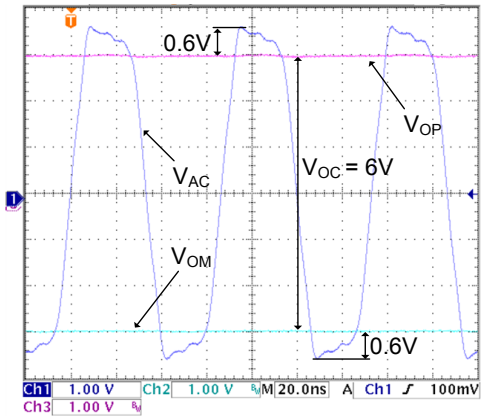

Fig. 7: Experimental results for f_{AC} = 15MHz & P_L = 46.8mW

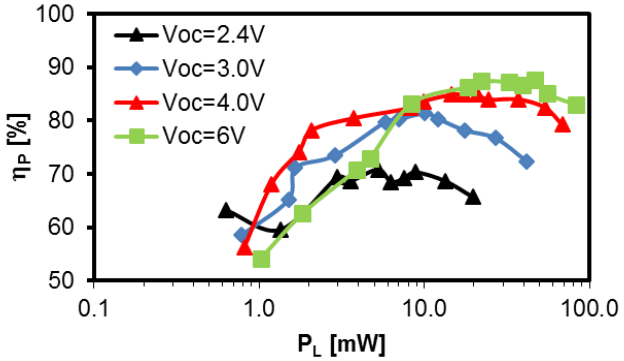

Fig. 8: Measured η_P vs. P_L for f_{AC} = 15MHz

5. Summary and Conclusion

In this paper, a circuit called prectulator is proposed. The output transistor used for regulating the output voltage in a linear regulator is also used as a passive rectifier. To achieve rectification without turning on the parasitic bipolar transistor of the output transistor, an auxiliary rectifier is used for biasing the bulk terminal of the output transistor. However, the output transistor can be overdriven during startup and high load situations. Current can flow from the DC output back to the AC input. These overdriven situations are detected by another transistor, which generates a current to prevent the error amplifier (used for regulating the output) from further overdriving the output transistor. Based on this technique, a voltage doubling prectulator that provides a positive output and a negative output was implemented in a conventional 0.18µm CMOS process. The proposed prectulator achieved a maximum η_P of 87.7% and a maximum R_V of 1.71 at 15MHz.

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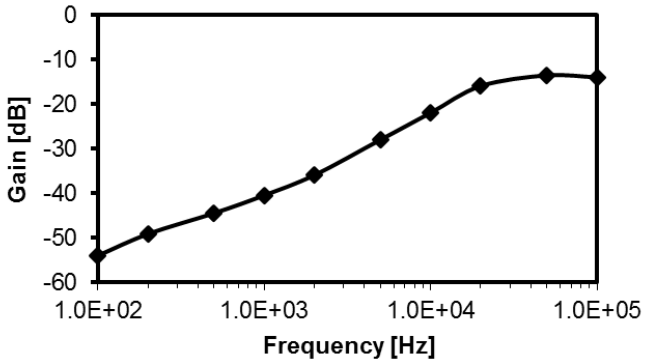

Fig. 9: Measured $\Delta V_{OC}/\Delta V_{ACP}$ vs. f_{AM} for f_{AC} = 15MHz

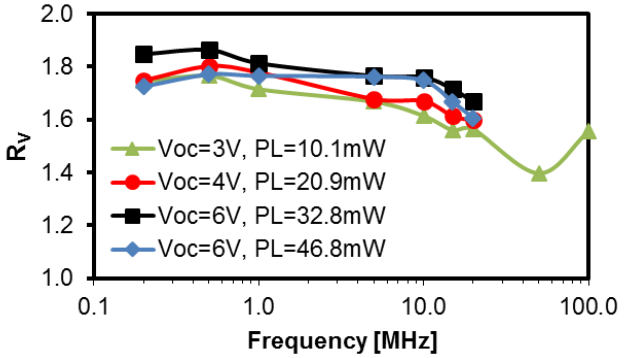

Fig. 10: Measured R_V vs. f_{AC} for different load conditions

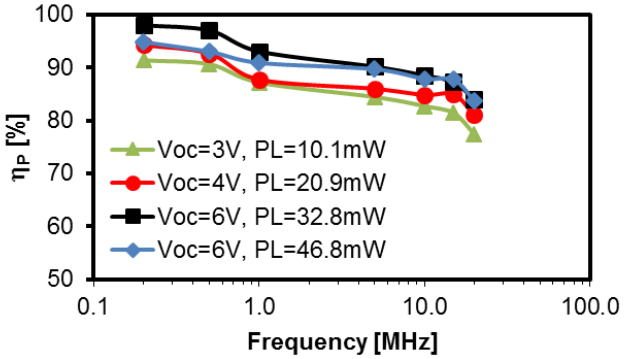

Fig. 11: Measured η_P vs. f_{AC} for different load conditions

Table I: Comparison with previous designs

	[4]	[5]	[6]	This work
Technology	0.18µm	0.35µm	0.18µm	0.18µm
Output range (V)	1.8	1.19 – 3.56	1.5 – 3.4	2.4 – 6.4
Active area	0.12mm^2	0.186mm^2	0.07mm^2	0.112mm^2
max[P_L]	40mW^A	24.8mW*	58.1mW	83.2mW
f_{AC} (MHz)	13.56	13.56	0.5 – 15	0.2 – >20
R_V	1.5^B	0.79 – 0.93*	0.57 – 0.96	1.4 – 1.86
max[η_P] (%) @ f_{AC} (Hz)	74.8 @ 13.56M	90.1* @ 13.56M	81.5 @ 15M	87.7 @ 15M 84.0 @ 20M
Load regulation	–	No	< 61µV/mA	< 1.9mV/mA

*rectifier only; ^{A}voltage doubler only; ^{B}including linear regulators