Physics-based Compact Models for Insulated-Gate Field-Effect Biosensors, Landau-Transistors, and Thin-Film Solar Cells

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***Abstract*— As the future of Moore's law appear uncertain, semiconductor electronics is being reinvented with a broader focus on energy efficient 3D computing, flexible electronics, biosensors, energy harvesting, etc. These devices are gradually being integrated onto the CMOS fabric as 'More-than-Moore' components, with transformative impact on consumer electronics. Unfortunately, a lack of physics-based, experimentally validated, numerically stable, well-documented compact models makes integration of these components in a CMOS design flow difficult. In this paper, we describe physics-based compact models for three very different components that are likely to be integrated in future systems, namely, FET-based nanobiosensors for pH sensing, Landau-transistors for low-power electronics, and thin-film solar cells for energy harvesting. Our physics-based approach should inspire the community to develop similar models for other emerging devices, so as to make their integration onto CMOS platform a routine affair.**

***Index Terms*—Compact model, integrated system, FET pH sensor, Landau-transistor, solar cell**

I. Introduction

From the earliest days of the semiconductor industry, physics-based compact models have served two important functions, namely, connecting process information to device performance and establishing system implications of a given device technology. The very first text-book of the field, W. Shockley's "Electrons and Holes in Semiconductor" [1] begins with a compact model of a bipolar transistor to describe the essential metrics of transistor operation. The subsequent widespread and effective use of Ebers-Moll model for bipolar transistors [2] and Berkeley Short-Channel IGFET model (BSIM) [3] for MOSFET attests to the power of compact models in shaping decisions from process optimization to system design. The power of the compact model derives not because it is compact, but because the need for compactness forces one to identify the most important variables that govern device operation.

After almost half a century of exponential growth, the era of Moore's law is coming to an end. Electronics industry is in transition and the field is being reinvented with a broader focus on energy efficient computing, energy-harvesting, and bioelectronics. More specifically, the raw scaling of CMOS transistors must now be supplemented by much more energy efficient computing elements (e.g. Phase transition or Landau switches, tunnel-FET, and spin-FET, etc.), new classes of integrated energy sources (e.g. energy harvesters, compact solar cells), and new functional capabilities (e.g. biosensors, MEMS switches), etc. An entire product category can be transformed by the integration of even one or two "More-than-Moore" components, e.g., iPhone or iWatch.

Many of these emerging devices have been explored through detailed device modeling and the performance of isolated elements are generally well understood. After all, solar cells was invented in 1954, the field-effect ion sensors in 1970 [4], and various forms of Landau-switches have been known in 1980s. Unfortunately, many of these devices lack physics-based, numerically stable, well-documented compact model that will help define the system implications, especially in the context of integrated circuits. In this paper, we discuss the compact model for three devices and demonstrate how physics-based compact model allows analysis of system-level performance. The models proposed here are illustrative; we anticipate that over time a community-wide effort will refine these models further.

II. A Compact Model for the FET-based pH Sensors

A. Background

The density of hydronium ions of a solution (defined by its pH) is an important marker of many biological and chemical systems [5]. For example, the genome sequencing technology from Ion Torrent™ relies exclusively on measurement of pH change to decode the sequence of human genome [6]–[8]. Direct measurement of blood plasma pH is also relevant for keeping a check on certain diseases such as ketoacidosis, etc. In the following, we describe a generalized compact model for field-effect transistor (FET) based pH sensors, implemented in Verilog-A language. The model is versatile and can describe the pH sensing operation of different classes of FET sensors

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like single-gated, double-gated FET, etc.

B. Model Description

Operational principle: Fig. 1(a) shows the operation of a single-gated FET. As the pH ($pH = -\log_{10}[H^+]$) of the solution changes, the surface groups (AOH) get protonated or deprotonated leading to a net surface charge density [9]. This surface charge brings about a change in the voltage drop (ψ_e) between the electrolyte/oxide and reference electrode. This changes the effective gate voltage which can be observed as a change in I-V characteristics of the transistor.

Model: The sensor is modeled as two decoupled circuit elements *i.e.* pH dependent nonlinear voltage source and a transistor (see, Fig. 1(b)). **pH dependent voltage source**: The potential (ψ_e) *i.e.* the difference between the fluid gate voltage (V_{FG}) and effective gate voltage ($V_{\mathrm{g,eff}}$) is a function of the pH. Therefore, the pH dependence of the sensor can be captured using a pH dependent voltage source. In the model, pH is represented as an external voltage source (V_{pH}) to enable transient and small signal analysis with respect to pH in circuit simulator. **Transistor**: The second element in the model involves a classical MOSFET transistor with gate, source, and drain terminals. It can be any FET which is supported by circuit-simulator such as long-channel MOSFET, a double gated FET or more generally, an externally defined Verilog-A FET model. The gate of the transistor is actuated by $V_{\mathrm{g,eff}}$ which is responsive to the pH of the solution.

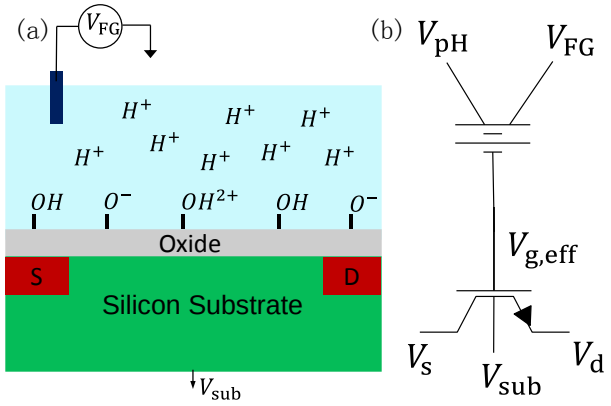

Fig. 1. (a) Sketch of Single-gated MOSFET pH sensor (b) Circuit representation of the model. The sensor is modeled as two decoupled elements 1) pH dependent voltage source 2) Transistor

C. Compact Model

The net gate-charge can be calculated by the charge neutrality (Eq. (1) of TABLE 1) requirement in the system. Surface charge (σ_{OH}) is compensated by the charge in electrolyte due to accumulation of ions (σ_{dl}) and the charge in transistor (σ_{mos}). **Surface charge:** The surface charge due to protonation or deprotonation of surface-groups is dictated by the reactions taking place at the interface (Eqs. (2) and (3) of TABLE 1). The net surface charge can be expressed [10] in terms of the surface potential (ψ_{e}) as given in Eq. 4 of TABLE 1. **Electrolyte charge**: The electrolyte sees a potential (ψ_0) smaller than the potential (ψ_{e}) at oxide/electrolyte interface as the ions have finite size and cannot approach infinitesimally close to the interface. To account for this, there is an additional capacitance (C_{stern}) in addition to the oxide capacitance (Eq. (5) of TABLE 1). The accumulation density of ions can be expressed [11] in terms of the potential that the electrolyte sees (Eq. 6). **Transistor charge:** For physiological salt concentrations, $\sigma_{\mathrm{mos}} \ll \sigma_{\mathrm{dl}}$; and hence the voltage drop across electrolyte (ψ_{e}) is independent of the type of transistor.

Solution of Eqs. (1), (4), (5), and (6) of TABLE 1 leads to an implicit equation for ψ_{e} in terms of pH (Eq. (7)). This equation is represented as a self-voltage and pH dependent voltage source in Verilog-A. The compact model parameters are listed in TABLE 2.

TABLE 1. Compact model for FET based pH sensors

$\sigma_{dl} + \sigma_{OH} + \sigma_{\mathrm{mos}} = 0$		(1)
$\mathrm{AOH_2^+} \rightleftarrows \mathrm{AOH} + \mathrm{H_s^+}$	K_a	(2)
$\mathrm{AO}H \rightleftarrows \mathrm{AO^-} + \mathrm{H_s^+}$	K_b	(3)
$\sigma_{OH} = q([\mathrm{AOH_2^+}] - [AO^-]) = -2qN_s \dfrac{(\tanh(q\psi_e/kT + 2.3\,\Delta pH))}{(10^{\Delta pK/2}\,\mathrm{sech}(q\psi_e/kT + 2.3\,\Delta pH) + 2)}$		(4)
$\psi_e = \psi_0 + \sigma_{OH}/C_{stern}$		(5)
$\sigma_{\mathrm{dl}} = -\sqrt{8kT\varepsilon_w n_0}\sinh\left(\dfrac{q\psi_0}{2kT}\right)$		(6)
$\psi_{\mathrm{e}} = \dfrac{2kT}{q}\mathrm{asinh}\left(\dfrac{\sigma_{OH}}{\sqrt{8kT\varepsilon_w n_0}}\right) + \dfrac{\sigma_{\mathrm{OH}}}{C_{\mathrm{stern}}}$		(7)
$V_{\mathrm{g,eff}} = V_{\mathrm{fg}+\psi_{\mathrm{e}}}$		(8)
$\Delta pH = pH - (pK_a + pK_b)/2$		(9)
$\Delta pK = pK_b - pK_a$		
$pK_a = -\log_{10}(K_a),\ \ pK_b = -\log_{10}(K_b)$		(10)

TABLE 2. Parameter Summary of the compact model

pK_a	Negative logarithm of dissociation constant (K_a)
pK_b	Negative logarithm of dissociation constant (K_b)
N_s	Number density of ionizable groups (#/cm^2)
n_0	Ionic concentration of the solution
C_{stern}	Stern Layer Capacitance (F/m^2)

D. Results and Discussions

Fig. 2 shows the match between the compact model and experimental data obtained from Go *et al.* [12] for a single-gated n-channel FET.

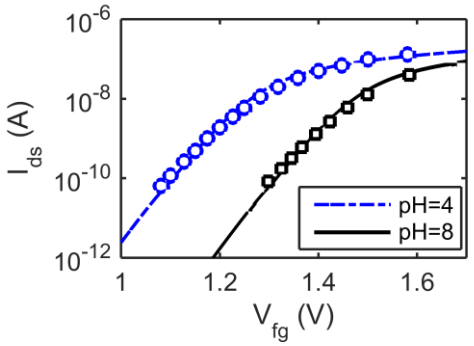

Fig. 2. Match of experimental data (symbols) obtained from Go et al. [12] to the compact model (line). Parameters: $\boldsymbol{pK_a = 6}$, $\boldsymbol{pK_b = 10}$, $\boldsymbol{N_s = 8 \times 10^{14}\ cm^{-2}}$ [11]

The model (line) is in excellent agreement with the experimental data (symbols). The surface parameters (N_s, pK_a, pK_b) used are obtained from Hal *et al*. [9]. For higher pH, the amount of proton concentration in the solution is small. This leads to deprotonation of the surface (AOH) groups and results in a net negative charge on the surface. Therefore, the threshold voltage increases and the I_{ds} curve shifts to the right.

Next, we demonstrate the usefulness of the model by considering two examples *i.e.* sensitivity enhancement in double-gated FET by dc analysis and response of a single-gated FET to stepwise change in pH.

Sensitivity enhancement in double-gated FET pH sensor

The sensitivity of a single-gated FET sensor is limited by Nernst Limit (59 mV/dec at room temperature). This limit can be overcome by using a double gated FET as reported in Go *et al.* [12], [13]. In order to obtain higher sensitivity, the electrolyte is exposed to the thinner oxide interface (Fig. 3 (a)) and one sweeps the voltage at the gate of thicker oxide (V_{MG}). A tunable bias is applied to the fluid gate (V_{FG}), and the pH sensitivity is measured in terms of the threshold voltage shift of the thicker oxide gate ($\Delta V_{\mathrm{T,MG}}/\Delta \mathrm{pH}$).

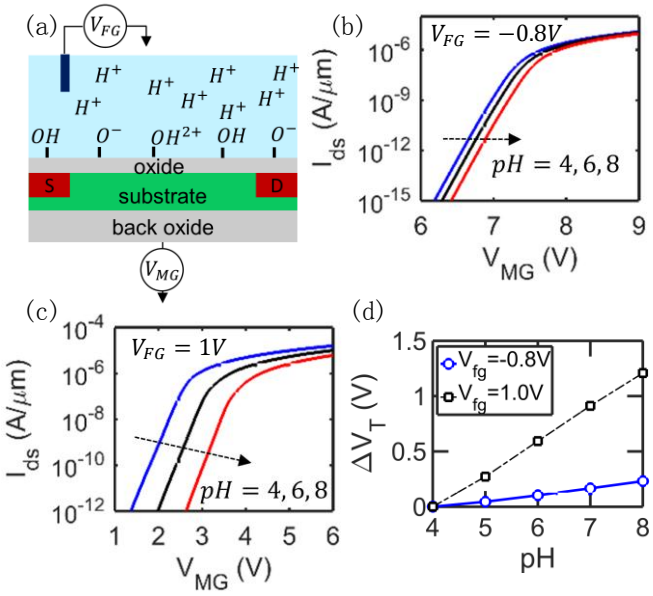

Fig. 3. (a) Double gated sensor configuration for enhanced sensitivity. The electrolyte is exposed to the thinner oxide. (b), (c) Transfer characteristics with respect to metal gate voltage for two different fluid gate voltages. (d) Threshold voltage change as a function of pH for $\boldsymbol{V_{FG} = -0.8V}$ (solid line) and $\boldsymbol{V_{FG} = 1V}$ (dash-dotted line). The sensitivity improves by almost 5x as the $\boldsymbol{V_{FG}}$ changes from $\boldsymbol{-0.8V}$ to $\boldsymbol{1V}$.

The maximum sensitivity that can be achieved is given by, $\mathrm{S} = \frac{\Delta \mathrm{V_{T,MG}}}{\Delta \mathrm{pH}} = \frac{C_{FG}}{C_{\mathrm{MG}}} \frac{\Delta \mathrm{V_{T,FG}}}{\Delta \mathrm{pH}}$, where $\frac{\Delta \mathrm{V_{T,FG}}}{\Delta \mathrm{pH}}$ is the pH sensitivity (limited by Nernst Limit) with fluid gate operation and a constant metal gate voltage. This high sensitivity occurs when both the fluid gate channel and metal gate channel are inverted, and when the capacitance of oxide exposed to fluid gate (C_{FG}) is larger than the capacitance of the metal gate oxide (C_{MG}). Fig. 3(b) and (c) shows the comparison of $\mathrm{I_{ds}} - \mathrm{V_{gs}}$ characteristics for two different fluid gate voltages. Fig. 3(d) shows the corresponding change in threshold voltage as a function of pH for $V_{\mathrm{FG}} = -0.8V$ (solid line) and $V_{\mathrm{FG}} = 1V$ (dash-dotted line). The device sensitivity (S) increases by almost 5x as the fluid gate voltage changes from -0.8V ($\mathrm{S} = 58\ \mathrm{mV/pH}$, accumulation-inversion) to 1.0V ($\mathrm{S} = 306\ \mathrm{mV/pH}$, depletion-inversion mode). The sensitivity amplification was tested using BSIM SOI FD model in HSPICE for the transistor.

Response of ion-sensitive FET to stepwise change in pH

As an example of the robustness of the model, we simulated the response of n-channel, partially depleted (PD) SOI MOSFET in response to a stepwise change in pH value. Fig. 4(a) and (b) show the applied input pH value and the corresponding output current as a function of time respectively. As pH value increases from 3 to 8, the proton ion concentration decreases; therefore, the surface is deprotonated giving a more negative charge on the surface. This leads to decrease in channel conductance and hence the output current.

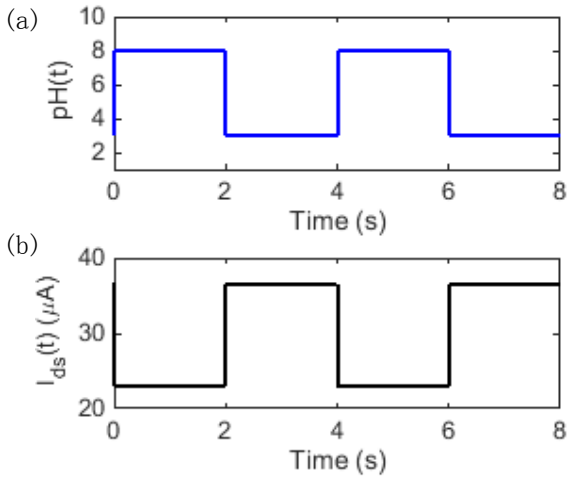

Fig. 4. Response of SOI MOSFET sensor to stepwise change in pH: (a) Input pH, (b) Output Current as a function of time. Surface charge becomes more negative as pH increases from 3 to 8.

E. Conclusions

The model presented in this section characterizes the response of FET based pH sensors. The physics of surface charging due to change in solution pH is captured in terms of a simplified pH dependent voltage source. The model can also be easily generalized to include biomolecule binding. The model should have broad implications in design of circuits such as pH based genome-sequencers, etc. An implementation of model in Verilog-A is available at *nanohub.org* [14].

III. A Compact Model of Landau FET

A. Background

Successive down scaling of MOSFET dimensions over the last 50 years have dramatically increased of the transistor density and the performance of the integrated circuits (IC). Recently, however, the trade-off between off and on-currents (dictated by the subthreshold slope, S) have made it difficult to further reduce the supply voltage, V_D (and thereby power dissipation, P_D). Indeed, the proposed future technology nodes anticipate almost no improvement in P_D [15], [16]. At these voltages, one expects significant self–heating of FinFET [17]

and gate-all-around transistors (GAA-FET) [18], [19], with important implications for circuit reliability [18], [20]–[22]. The techniques proposed so far to lower V_D all rely reducing S below the Boltzmann limit ($S_{BZ} = 60$ mV/dec), see Fig. 5(a). There are two ways to improve S: (1) improving channel conduction based on tunneling through the barrier (tunnel FET) and (2) amplification of gate bias due to negative capacitance (NC) dielectric (NC-FET) in a Landau switch (Fig. 5(b)-(d)) [23]–[27]. The negative capacitance arises from biasing a ferroelectric gate insulator in the unstable region.

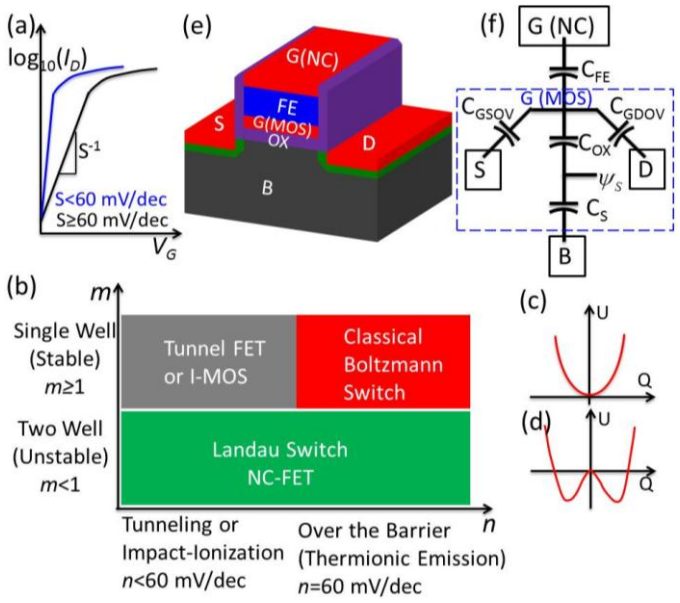

Fig. 5. (a) Reduced threshold voltage (V_T) allows same drive current (I_D in on-state) and performance with lower applied bias. (b) Sub-threshold slope (S) can by improved either by improving the m or the n factor (equations (1)-(2)). Tunnel FET offers n<60 mV/dec and Landau switch offers m<1 with negative capacitance (NC) effect by ferroelectric (FE) dielectric [23]. (c) Conventional dielectric shows single well energy landscape and can offer only positive capacitance, (d) NC dielectric shows double well energy landscape. (e) Device structure of the NC-FET with FE and gate-oxide (OX) as gate dielectric stack. (f) Equivalent capacitor model for the device geometry in (e). The dotted blue box region represents conventional MOS-FET.

The operating principle of long channel Landau-FET (also called negative-capacitor, or NC-FET) is well understood [27]. A BSIM-like compact model will help evaluate the performance potential of this device in an IC. In this section, we develop the compact model of the NC-FET by integrating the MVS model [28] (Eqs. (3)-(9)) of the conventional short channel MOS-FET with Landau theory (Equations (10)-(11)) (TABLE 3). For illustration, we will consider two technology nodes: 45 nm and 32 nm. All the key parameters for the NC-FET compact model are included in TABLE 4.

B. Device Geometry and Circuit Model

Fig. 5(e) explains different components of a NC-FET. The equivalent capacitor model of the structure is shown in Fig. 5(f). C_S and C_{OX} are the channel and gate oxide capacitances, respectively, of the conventional MOSFET. C_{GSOV} and C_{GDOV} represent gate-source and gate-drain overlap capacitances, (including fringing field) and C_{FE} is the capacitance of the FE material. S is the function of the C_S, C_{OX}, and C_{FE}, (Eqs. (1)-(2), TABLE 3) and only gate charge (Q_G) is affected by the C_{GSOV} and C_{GDOV}.

TABLE 3. List of equations for the compact model of the NC-FET. Equations (1)-(2) defines sub-threshold slope, (3)-(9) defines MVS model for conventional MOS-FET [28] and (10)-(11) explains the relation between bias, gate charge, and ferroelectric capacitance through Landau theory [23], [27]. Prime (′) sign is used to represent the potential of the intermediate node while including the parasitic source (S)/drain (D) resistance (R_S and R_D).

$S = \frac{dV_{GS}}{dlog_{10}(I_D)} = \left(\frac{dV_{GS}}{d\psi_S}\right)\left(\frac{d\psi_S}{dlog_{10}(I_D)}\right) = m \times n$	(1)
$m = \left(\frac{dV_{GS}}{d\psi_S}\right) = \left(1 + C_S\left(\frac{1}{C_{OX}} + \frac{1}{C_{FE}}\right)\right)$	(2)
$I_D = Q_{ix_0} v_{x_0} F_S$	(3)
$F_S = \frac{V'_{DS}/V_{DSAT}}{(1 + (V'_{DS}/V_{DSAT})^{\beta})^{1/\beta}}$	(4)
$Q_{ix_0} = C_{inv} n\phi_t ln\left(1 + exp\frac{V'_{GS} - (V_T - \alpha\phi_t F_f)}{n\phi_t}\right)$	(5)
$V_T = V_{T0} - \delta V'_{DS}$	(6)
$V_{DSAT} = V_{DSATs}(1 - F_f) + \phi_t F_f$	(7)
$V_{DSATs} = \frac{v_{x_0} L_C}{\mu}$	(8)
$F_f = \frac{1}{1 + exp\left(\frac{V'_{GS} - (V_T - \alpha\phi_t/2)}{\alpha\phi_t}\right)}$	(9)
$V_{FE} = 2\alpha_{FE} t_{FE} Q_G + 4\beta_{FE} t_{FE} Q_G^3$	(10)
$C_{FE} = \frac{1}{2\alpha_{FE} t_{FE} + 12\beta_{FE} t_{FE} Q_G^2}$	(11)

TABLE 4. Different parameters used in the model in this work to analyze the performance of the NC-FET for 45 nm and 32 nm nodes.

	$L_G = 45\ nm$	$L_G = 32\ nm$
$W\ (\mu m)$	1	1
$EOT\ (nm)$	0.9	0.75
$\varepsilon_{OX}\ (\varepsilon_0)$	3.9	3.9
$N_{sub}\ (cm^{-3})$	6.5×10^{18}	8.7×10^{18}
$V_{T0}\ (V)$	0.3423	0.3558
$\mu\ (cm^2/VS)$	295	238
$v_{x_0}\ (cm/S)$	1.595×10^{7}	1.821×10^{7}
$R_S = R_D\ (\Omega - \mu m)$	52.5	40
$C_{GSOV} = C_{GDOV}$ (F/cm)	2.1×10^{12}	2×10^{12}
n	1.15	1.15
$\delta\ (V/V)$	0.0332	0.0424
β	1.8	1.8
α	2	2
$\gamma\ (\sqrt{V})$	0.1	0.1
$\alpha_{FE}\ (cm/F)$	-3×10^{11}	-3×10^{11}
$\beta_{FE}\ (cm^5/F/Coul^2)$	4×10^{23}	4×10^{23}

C. Results and Discussions

We divide the results and discussions section in two parts: performance of the MOSFET before (Fig. 6) and after (Fig. 7)

incorporation of the negative capacitance. For short channel device, thicker gate oxide results in non-uniform gate-channel electrostatic coupling due to differential enhancement of parasitic flux from gate to channel, source, and drain, respectively. For NC-FET, the presence of the intermediate metallic layer G (MOS) (i.e., the gate of the conventional MOSFET) ensures uniform distribution of electrostatic potential in the channel along the source-drain direction.

Fig. 6(a) shows the C-V profile of a classical MOSFET (Fig. 6(a)), the total gate capacitance (C_G) is the summation of the C_{GSOV} and C_{GDOV} and intrinsic MOS capacitance. In sub-threshold region (marked by left blue bracket) intrinsic capacitance is dominated by the depletion capacitance (C_S=C_{Dep}) and in inversion region dominated C_{OX}.

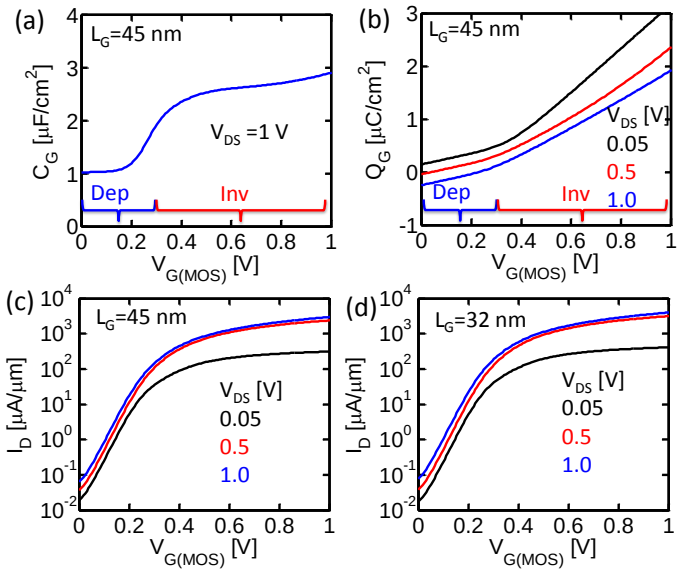

Fig. 6. Analysis of the performance of the conventional MOS-FET (without FE) with MVS model for 45 nm and 32 nm technology node. (a) Capacitance vs gate bias (C-V) characteristics of the MOSFET with V_{DS}=1 V. At ($V_{G(MOS)}$<V_T=0.3423 V) the device is in depletion and above in inversion. (b) Gate charge vs gate bias (Q-V) characteristics for different V_{DS}. Drain current vs gate bias (I-V) characteristics of the MOS-FET for different V_{DS} for (c) 45 nm and (d) 32 nm nodes.

In Fig. 6(b), with the increase of the V_{DS}, C_G decreases and the gate charge, Q_G follows the C_G. Due to the parasitic coupling of the gate and source/drain through C_{GSOV} and C_{GDOV}, Q_G can be negative if the V_D>$V_{G(MOS)}$. In Fig. 6(c), current increases with $V_{G(MOS)}$ due to increase of carrier concentration through inversion. Current increases with V_{DS} in on-state ($V_{G(MOS)}$>V_T) and in sub-threshold region current increases with V_{DS} due to DIBL effect (Equation (6)). In Fig. 6(d), for 32 nm node, DIBL effect is higher, increasing more current with larger V_{DS}.

The Q-V profile of the NC-FET is shown in Fig. 7(a). For the fictitious FE dielectric, the material parameters are chosen such that polarization range (-0.37 to +0.37 $\mu C/cm^2$) of the instability region matches with the Q_G of the conventional MOSFET. Polarization *vs.* V_{FE} characteristics of FE dielectric, P(VDF-TrFE), has a closer match with the inset's profile. The log scale plot of I-V becomes highly nonlinear in the sub-threshold region, Fig. 7(b). Effect of the NC on the I-V characteristics of NC-FET depends on the match of C_S, C_{OX}, and C_{FE}, according to Equation (2). *S* improves significantly with larger V_{DS}. But, it happens only in narrow range of $V_{G(NC)}$. Improvement of the *S* sustains with the scaling of the channel length and even becomes better (Fig. 7(d) for 32 nm node).

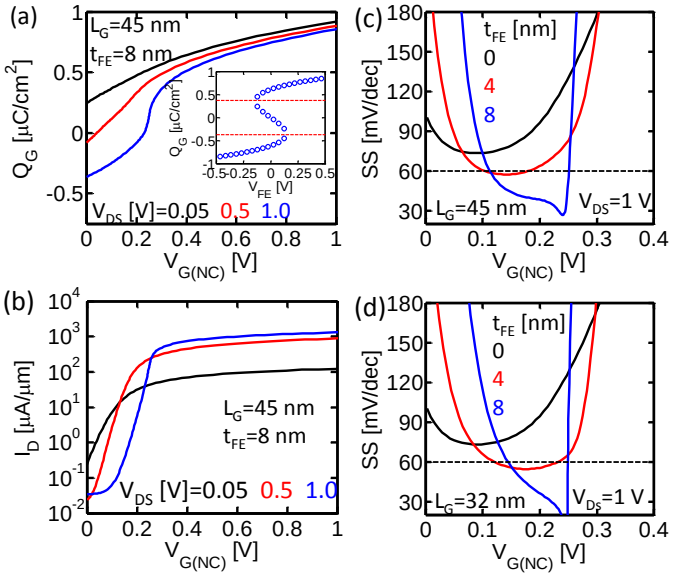

Fig. 7. Performance evaluation for the NC-FET. (a) Q-V and (b) I-V characteristics after inclusion of the FE with different V_{DS} for 45 nm node. Inset in (a) polarization vs voltage profile of the FE (Equation (10)). (c) *S* of the NC-FET in the sub-threshold region as a function of bias $V_{G(NC)}$ from Fig. 7(b). We vary the FE thickness and observe the effect on *S*. (d) Evaluation of the *S* for 32 nm node.

D. Conclusions

We have developed a compact model of the short channel NC-FET for two different gate lengths (45 nm and 32 nm) by modifying the MVS model for conventional MOSFET. We observe significant improvement of the sub-threshold slope (30 mV/dec). This compact model can be an important tool for circuit level analysis of the performance of the NC-FET targeting application for high-performance and low voltage digital logic.

IV. A Compact Model for Thin-film Solar Cells

A. Background

Energy harvesting by solar cells has the potential to reduce our dependence on traditional energy sources, such as, coal and gas. It has also the potential to be a power source for broad range of applications involving distributed sensors, micro-satellites, and other electronic components. A solar cell operates as follows: 1) photons hit the solar absorber; 2) electron-hole carrier pairs are generated; 3) the carriers collected by the electrodes delivers power to the load. In practice, many subcells must be connected in series and parallel to form solar modules, which scale up to solar arrays. To properly simulate such a large system in a circuit network, one needs an equivalent circuit (compact model) that can describe the light-power performance of the system.

There are three types of solar cells: the pn junction, p-i-n junction, and heterojunction. The conventional five-parameter

model is only applicable to the pn junction solar cell, e.g., c-Si, because it obeys the superposition principle, namely, that the light current is the uncorrelated sum (superposition) of dark current and a constant photocurrent source [29]. In the p-i-n junction and heterojunction solar cells, however, the photocurrent varies with bias. With reasonable assumptions, we found that the bias-dependence of photocurrent is analytically solvable. So far we have developed two kinds of physics-based compact models for the p-i-n junction [30] and heterojunction solar cells, respectively [31]. Because the model is physics-based, it can be used by experimentalists to characterize existing devices. More importantly, the temperature dependence of the IV characteristics is described analytically by the physical parameters, which makes the model a suitable for simulating the self-heating effect associated with partial shading degradation in solar panels. In this paper, we develop a compact model for heterojunction solar cell, more specifically, for CIGS technology.

B. *Compact Model*

The intrinsic equivalent circuit of CIGS solar cells consisting of five components is demonstrated in Fig. 8. Each circuit component is discussed, and all the equations and physical parameters are listed in TABLEs 5 and 6, respectively. Note that the external series resistance (can be easily included) is not included in this model.

TABLE 5. Equation list of the compact model

$J_{photo} = J_{tot}\dfrac{(1-\exp(-\Delta\sqrt{\frac{V_{bi}-V}{V_{bi}}}))}{1+\alpha_C\exp(\beta\frac{(V-V_{bi})}{V_{bi}})}$	(1)
$J_{RB} = J_{RB0}Vexp(\frac{q}{kT}\sqrt{\frac{V}{m}})$	(2)
$J_{shunt} = G_{SH}V + I_{0SH}V^{n_{sh}}$	(3)
$J_{diode} = J_0(\exp\left(\frac{qV}{AkT}\right)-1)$	(4)
$J'_{photo} = f_{smooth1}J_{tot}\dfrac{\left(1-\exp\left(-\Delta\sqrt{\frac{V_{bi}-V}{V_{bi}}f_{smooth2}}\right)\right)}{1+\alpha_C\exp\left(\beta\frac{(V-V_{bi})}{V_{bi}}\right)}$	(5)

1) *Voltage-dependent photocurrent*

The first current source in Fig. 8 denotes the voltage-dependent photocurrent source. The physical origins of the voltage-dependence are the shrinkage of the depletion region where electric field assists carrier collection as well as carrier blocking by the conduction band offset between the buffer layer and CIGS absorber. By analytically solving the drift-diffusion equation coupled with the continuity equations, we derived Eq. (1) of TABLE 5 for the photocurrent. In Eq. (1), J_{tot} is the maximum generation current; Δ is the product of the equilibrium depletion width and the average absorption coefficient over the solar spectrum; V_{bi} is the total junction built-in potential; β is the voltage partition between the CdS buffer layer and CIGS absorber layer; α_c is a fitting parameter that is determined by the conduction band offset at the interface and the recombination lifetime in the bulk. The detailed derivation is not discussed here. Note that the numerator in the second term represents the effect from decreasing depletion width; as V approaches V_{bi}, the photocurrent is closer to zero. Small bulk lifetime and large conduction band offset make α_c larger in the denominator, which reduces J_{photo}.

TABLE 6. Parameter summary of the compact model

Parameters	Definition
J_{tot}	total generation current (mA/cm^2)
Δ	Product of equilibrium depletion width and average absorption coefficient
V_{bi}	junction built-in voltage (V)
β	voltage partition factor
α_C	fitting parameter (ratio between front and back surface recombination velocities)
J_{RB0}	breakdown current prefactor (mA/(V.cm^2))
m	breakdown current index (V$^{-0.5}$)
G_{SH}	ohmic shunt conduction (mS/cm^2)
I_{0SH}	SCL shunt conduction (mS/cm^2)
J_0	diode saturation current (mA/cm^2)
A	diode ideality factor

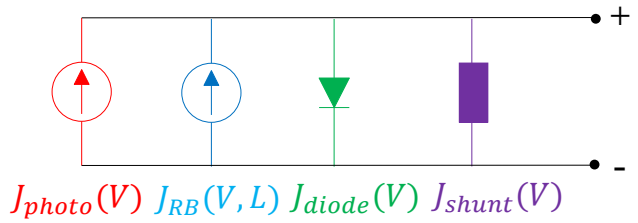

Fig. 8. The equivalent circuit for CIGS solar cell. J_{RB} represents the reverse breakdown current, which is a function of voltage and illumination intensity.

2) *Light-enhanced reverse breakdown current*

Reverse breakdown characteristic of CIGS is equally important as the photocurrent at forward bias. Under partial shading condition, the shaded cells could be stressed into reverse breakdown, which leads to permanent damage as well as local heating in the modules [32]. Recent results have shown that the reverse breakdown mechanism of CIGS devices is greatly enhanced under illumination [33], [34]. The light-enhanced revere breakdown current functions similar to an intrinsic bypass diode to reduce the reverse stress.

The second current source describes the reverse breakdown current in CIGS as a function of voltage bias and illumination intensity. We interpret the essential physics of this light-enhanced breakdown current to the tunneling-assisted Poole-Frenkel conduction [35] formulated as Eq. (2), TABLE 5. The prefactor J_{RBO} depends on the illumination and is proportional to $exp\ (-q\Phi_T/kT)$, where Φ_T is the defect level assisting the tunneling breakdown current in the buffer layer. Due to light-dependent defect response, Φ_T is found to be shallower under light than dark resulting larger J_{RBO}, with weaker temperature dependence. Finally, m is determined by the dielectric constant and the buffer layer thickness.

3) Non-Ohmic shunt current and diode current

One of the key factors causing cell-module efficiency gap and affecting efficiency variability in large-scale thin film module is the significant shunt leakage current [31], [36], [37]. The shunt current in CIGS is often found to be non-ohmic, described by the space charge limited (SCL) conduction [38]–[40]. In this compact mode, the shunt current is treated using the following empirical formula Eq. (3) of TABLE 5, where the first term on right side denotes linear shunt leakage while the second term accounts for the SCL current.

The diode represents the dark recombination current. The current follows Eq. (4) of TABLE 5 where the temperature dependency of the saturation current J_0 and the ideality factor A depends on the bandgap and defect distribution of the absorber layer [41].

C. Model Validation

The validation process consists of two steps: 1) we fit the model to data obtained from the literature, to extract the physical parameters at room temperature. 2) Based on the temperature dependences of the built-in potential, etc., we analytically extrapolate the room-temperature parameters to other temperatures. Remarkably, the compact model reproduces the temperature dependences of the IV measurement varying from reverse bias to forward bias, see Fig. 9 and Fig. 10. The extracted parameters (e.g. junction built-in voltage, bandgap, etc.) are in excellent agreement with the results obtained from the capacitance-voltage and external quantum efficiency measurements. Based on the outstanding fitting results, it is convincing that the compact model can provide experimentalists a straightforward characterization technique merely using the IV characteristics

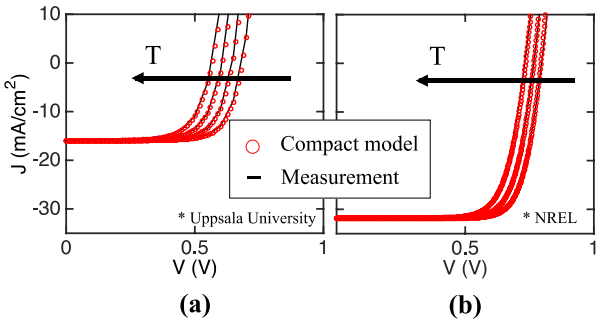

Fig. 9. Benchmark results of temperature-dependent light IV against the compact model. (a) CIGS data (efficiency ~ 15%) obtained from Uppsala University from 280 K to 340 K with a 20 K interval [34]. The low short circuit current is due to monochromatic light source. (b) CIGS data provided by NREL at T = 257 K, 273 K, 293 K.

D. Numerical Issues

Since the compact model is designed for large-scale simulation, it is essential to ensure that the model is numerical robust to avoid any possible convergence difficulties. To do so, we need to smoothen the functions so that the functions and the corresponding derivatives are continuous. As a result, numerical methods, e.g., the Newton–Raphson method that strongly rely on the derivatives of the functions can converge successfully. For instance, in our model, Eq. (1) in Table 5 is not valid for $V > V_{bi}$. A solar cell never operates in this regime, but a transient overshoot during simulation of scaled-up panel, could cause the voltage across a cell to exceed V_{bi}. Physically, it is justifiable that J_{photo} should be zero above V_{bi} [42]. To implement the transition at V_{bi} in the compact model, we rewrite Eq. (1) into Eq. (5) of TABLE 5, where $f_{smooth1} = 0.5 \times (1 - \tanh(10^5(V - 0.99 \times V_{bi})))$ and $f_{smooth2} = \tanh(10^5(V_{bi} - V))$ are two smooth functions. $f_{smooth1}$ can provide a continues but sharp transition at V_{bi}, and $f_{smooth2}$ acts as a continuous sign function for $V_{bi} - V$ so there would not be any negative input under the square root.

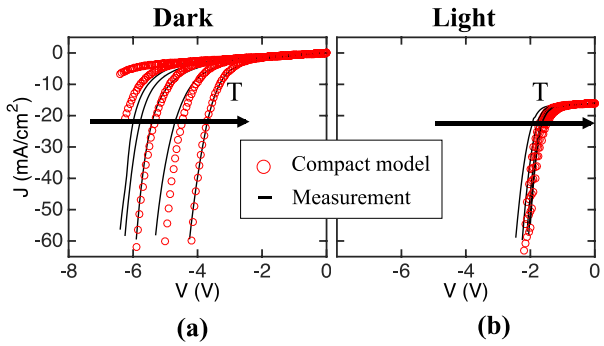

Fig. 10. Benchmark results of temperature-dependent reverse breakdown IV against the compact model. Data was measured at Uppsala University, and temperature varies from 260 K to 340 K with a 20 K interval [34]. (a) Reverse breakdown fitting results in darkness. (b) Reverse breakdown fitting results under illumination.

E. Conclusions

The model presented describes the operation of CIGS solar cells including voltage-dependent photocurrent and light-enhanced reverse breakdown. Like the model for p-i-n solar cells [30], [43], the Verilog-A version of the CIGS model will be available on nanoHUB.org soon. This model allows an electrical-thermal coupled panel simulation framework that can be used to investigate and predict the impact of partial shading degradation.

V. Conclusions

In this paper, we have described compact models for three electronic devices, i.e., Landau-switch for low-power electronics, FET-based pH sensors, and finally, thin-film solar cells. There principles of operation of these devices have been discussed in detail in our previous publications; here, we have focused on developing physics-based, numerically stable, compact models for these devices so that they can integrated with CMOS design flow. A collection of such models will dramatically simplify the design of system involving such components.

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