# A 298-fJ/writecycle 650-fJ/readcycle 8T Three-Port SRAM in 28-nm FD-SOI Process Technology for Image Processor

Haruki Mori[1], T. Nakagawa[1], Y. Kitahara[1], Y. Kawamoto[1], K. Takagi[1], S. Yoshimoto[1], S. Izumi[1], K. Nii[2], H. Kawaguchi[1] and M. Yoshimoto[1]
[1]Kobe University, Kobe, Japan, [2]Renesas Electronics, Tokyo, Japan
Email: mori.haruki@cs28.cs.kobe-u.ac.jp

***Abstract* — This paper presents a low-power and low-voltage 64-kb 8T three-port image memory using a 28-nm FD-SOI process technology. Our proposed SRAM accommodates eight-transistor bitcells comprising one-write/two-read ports and a majority logic circuit to save active energy. The test chip can operate at a supply voltage of 0.46 V and an access time of 140 ns. The energy minimum point is a supply voltage of 0.54 V and an access time of 55 ns (= 18.2 MHz), at which 298 fJ/cycle in a write operation and 650 fJ/cycle in a read operation are achieved with the help of the majority logic; these factor are 87% and 52% smaller than those in a 28-nm FD-SOI 6T SRAM.**

***Index Terms* — Image Memory, Multiport SRAM, 8T, FD-SOI, 28-nm, Majority Logic.**

## I. Introduction

Application of image recognition is being extended to various fields such as an automatic driving system, robot vision, and an augmented reality system with improving image resolution. Image resolution enhancement leads the increase of SRAM capacity, area and power consumption because of the image data amount increase. The power consumption in SRAM dissipates 43% of a whole image processor in a 65-nm CMOS process [1]. For wearable devices handling image information, an energy-efficient SRAM will be expected, as shown in Fig. 1.

28-nm Fully-Depleted SOI (FD-SOI) technology is known as promising to provide high speed at low voltage SRAM [2]. 28-nm FD-SOI is implementing fully depleted transistors and an ultra-thin silicon body and BOX layer giving them an excellent electrostatic control. Therefore, 28-nm FD-SOI brings the stable features at low voltage operation. A BOX layer effectively reduces the leakage current to control the electrical flow from a source node to a drain node in a transistor. Moreover, BOX layer reduces the parasitic capacitance between source node and drain node. This feature of 28-nm FD-SOI is allow to make an ultra-low power SRAM [3-7].

In this paper, we design a 28-nm FD-SOI 8T three-port SRAM for a low power image processor and compare it to a 28-nm FD-SOI 6T SRAM. We demonstrate high energy-efficiency of sub-pJ/cycle in the proposed SRAM.

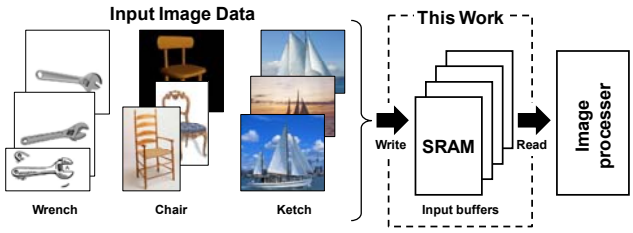


Fig. 1. Memory system in image processing.

## II. Proposed Three-Port 8T SRAM

### *A. 8T Three-Port SRAM Cell Design*

The circuit schematic of the proposed 8T three-port SRAM is shown in Fig. 2(a); it has a pair of write bitlines and two single-ended read bitlines (one-write/two-read bitcell structure). The proposed SRAM has two pull-up PMOSs (load-PMOS), two pull-down NMOSs (drive-NMOS) and four transfer NMOSs (access-NMOS). In this circuit, M7 and M8 transistors are used as two single-ended read ports. The source nodes of M7 and M8 transistors are connected to node Q, the drain node connected to read bitlines (RBL_A, RBL_B) and the gate node are connected to the read wordlines (RWL_A, RWL_B).

Figs. 2(b) and 2(c) shows the bitcell layout of the proposed 8T three-port SRAM. The size of the SRAM cell is determined by the number of horizontal and vertical wires. In our proposed SRAM, two read ports consists of M7 and M8 transistors are configured as two single-ended read ports have three bitlines and three wordlines. The cell area is 0.56μm$^2$ on a logic rule base, which is as small as the dual-port 8T bitcell [8] although the number of ports is increased.

The operating waveforms in the read operation is depicted in Fig. 3. There is no read current flowing through the read bitlines (RBL_A and RBL_B) when the internal node, node Q, is "1". Maximizing the number of "1"s at node Q is important to reduce dynamic power in the read operation. In the write cycle, successive data of same values save energy because the proposed SRAM needs not to have a precharge scheme on the write bitlines.

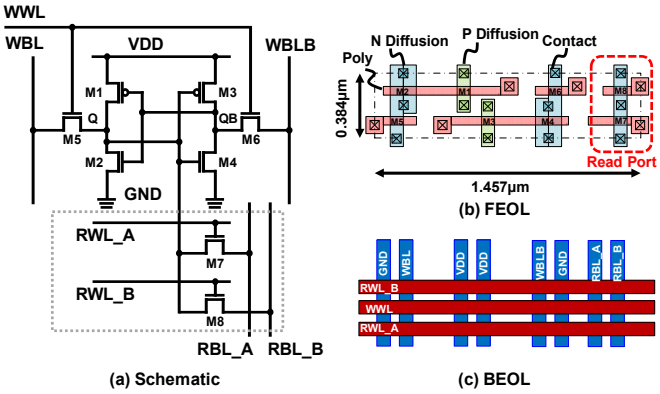


Fig. 2. (a)Schematic, (b) FEOL and (c) BEOL bitcell layouts of the proposed 8T three-port SRAM.

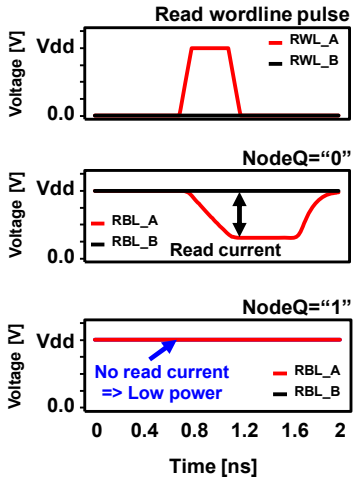


Fig. 3. Waveforms of the proposed 8T three-port SRAM in read operation.

### *B. SNM of proposed 8T Three-Port SRAM*

In the multiport SRAM, simultaneous reads happen at the dual read ports [9]. Fig. 4 shows the variety of read situations in the 1W2R (one-write two-read) three-port SRAM cell. Fig. 4(a) depicts the single port read situation (different two SRAM cells on different row addresses and different column addresses). Fig. 4(b) depicts the simultaneous dual-port reads on same row addresses and column addresses (RWL_A and RBL_B are simultaneously driven in a single cell). In this case, both RBL_A and RBL_B are enabled and double read currents flow from RBL_A and RBL_B to Node Q. Therefore, the read margin (static noise margin) is deteriorated and lowered.

Fig. 5 shows the simulation results of the static noise margin (SNM) at several Vdd voltages from 1.0 V to 0.4 V. Fig. 5(a) depicts the standard butterfly curves in the single port read situation; the SNM of 171 mV are achieved at 1.0 V, remaining 85% of the SNM in the

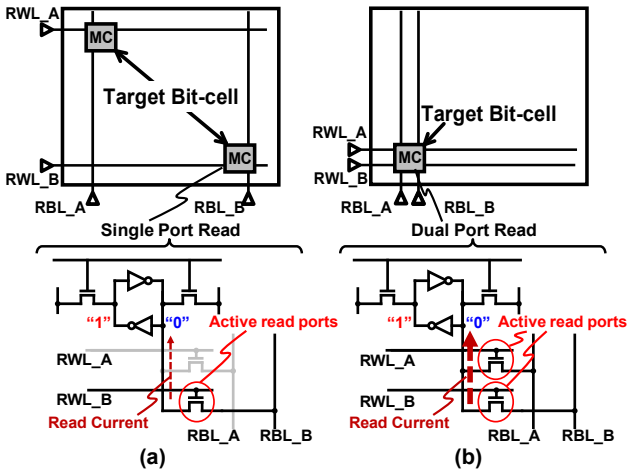


Fig. 4. Variety of the access situations of the 1W2R three-port SRAM.

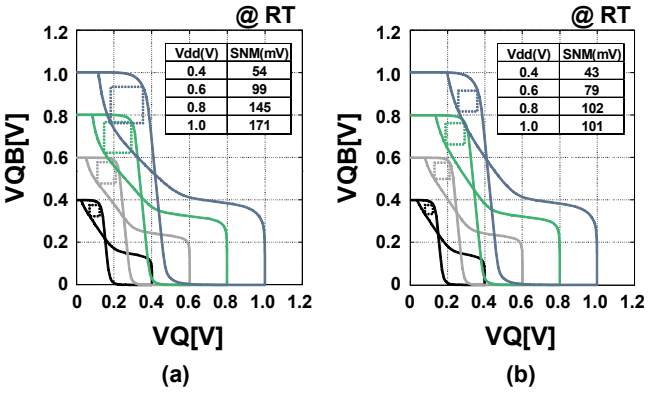


Fig. 5. Simulated butterfly curves at several Vdd from 1.0V down to 0.4V. (a) Single port read, and (b) dual port read.

conventional 6T SRAM [2]. Fig. 5(b) depicts the worst-case butterfly curves in the simultaneous dual-port reads. The SNM is reduces to 101 mV at 1.0 V. The interesting point is that the maximum SNM of 102 mV is observed at 0.8 V.

## III. Majority Logic

Fig. 6(a) shows a block diagram of the proposed SRAM with the majority logic [10]. Image data reflects luminance information; bright pixels have many "1" data and dark pixels have many "0" data. For the read energy reduction, the dark pixel having many "0"s should be inverted by the majority logic. To maximize the number of "1"s, a majority-logic circuit counts the number of "1"s and decides if input data should be inverted in a write cycle, so that "1"s are in the majority. The inversion information ("1" denotes inversion) is stored in an additional flag bit,

as depicted in Fig. 6(b). In a read cycle, the procedure is reversed. Output data are inverted if a flag bit is true, so that the original data can be read. Note that the majority logic does not reduce write energy because the "1" write energy and the "0" write energy is the same.

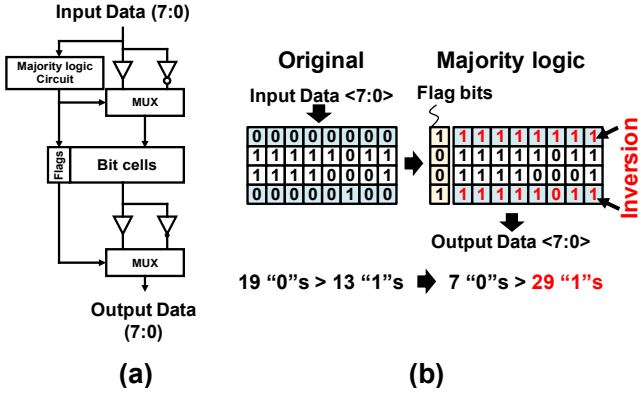


Fig. 6. Concept of SRAM with majority logic. (a) Block diagram, and (b) flag bit.

The mechanism on the RBL power reduction is shown in Fig. 7. We assume the bit-width of the input data is eight. If the number of "1"s in the input data is five and over, the data is not inverted, and one "0" is stored as flag bit. This means one read current is made by RBL, in witch is a power overhead. If the number of "1"s in the data is four or less, the data is inverted by majority logic to maximize the number of "1"s, and reduces the read power. When input data have a random pattern, the number of charges/discharges is four out of eight RBLs on average. However, the majority logic reduces this value to 3.27 although the number of RBLs is increased to nine. This indicates that the majority logic statistically saves 18% of an RBL power even if the data are random.

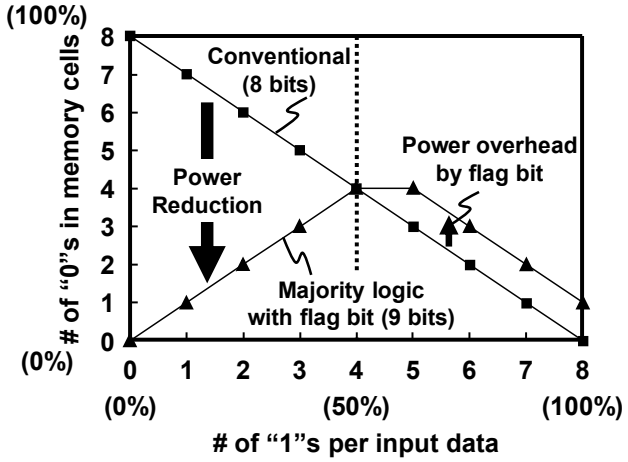


Fig. 7. A comparison of RBL powers between the conventional and proposed SRAM with majority logic.

## IV. Chip Implementation and Measurement Results

We fabricated a 64-kb 8T three-port SRAM macro using a 28-nm FD-SOI process technology. Fig. 8 shows the test chip micrograph. The macro area is 0.058 $mm^2$. Fig. 9 shows a measured Shmoo plot of the proposed SRAM macro. We verified that it can operate at a supply voltage of 0.46 V and an access time of 140 ns. At room temperature, the operating point, which achieves the minimum energy per cycle, is a supply voltage of 0.54 V and a cycle time of 55 ns (= 18.2 MHz). Fig. 10 illustrate that the measured leakage and active energies. The write energy is 298 fJ/cycle, which is 78% smaller than that in the 6T SRAM. In the read operation, the "0" and "1" read energies are 1440 fJ/cycle and 148.5 fJ/cycle, respectively. Thus, the energy saving in the "1" read operation is 73%; the read energy improvement is, however, merely 25% on average with no majority logic.

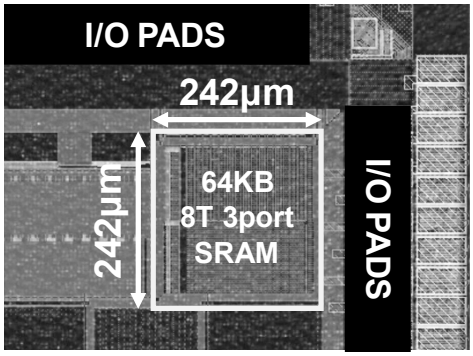


Fig. 8. Chip photo.

Fig. 11 shows the impact of the majority logic on the read energy saving. In the bright Image1, the read energy reduced by 23% while, in the dark Image1, that reaches a 47% saving; dark image is more appropriate and effective for the majority logic. In this case, the read energy is 650 fJ/cycle. TABLE I summarize the characteristics of the test SRAM.

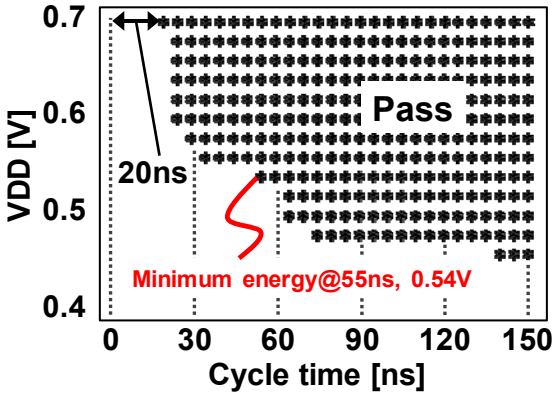


Fig. 9. Shmoo plot.

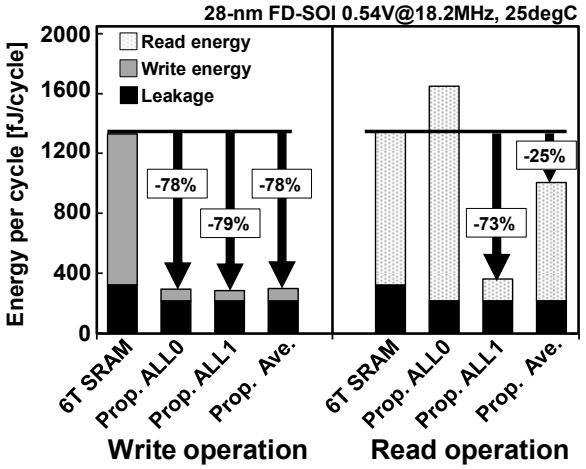


Fig. 10. Measured write energies, read energies, and comparison.

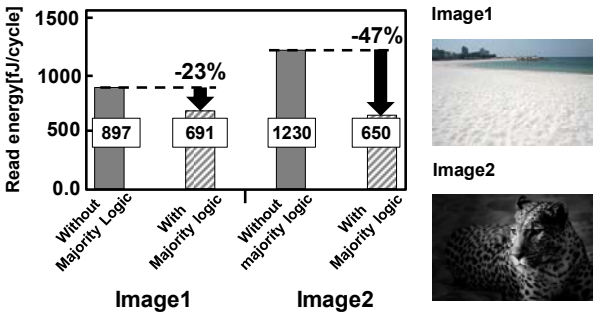


Fig. 11. Impact of majority logic on read energy in actual image data.

TABLE I FEATURES OF TEST CHIP

| | |
|---|---|
| Technology | 28-nm FD-SOI |
| Supply voltage | 0.5-0.7V (Memory macro) |
| | 1.8V (I/O) |
| Chip area | 1.0x1.0mm$^2$ |
| Macro size | 242x242μm$^2$ |
| Macro configulation | 64kb (32kb X 2), 16bits/word |
| Cell size | 0.384x1.457μm$^2$ |
| Frequency | 7.14MHz@0.46V, 50MHz@0.7V |
| Write active energy | 298fJ@0.54V, 18.2MHz, RT |
| Read active energy with majority logic | 650fJ@0.54V, 18.2MHz, RT |

## V. SUMMARY

As described in this paper, we presented 8T three-port SRAM for Image processor. The proposed SRAM is comprising one-write/two-read ports and a majority logic circuit to save active energy. We fabricated a 64kb 8T three-port SRAM in a 28-nm FD-SOI process technology. The test chip exhibits 0.46 V operation and an access time of 140 ns. The energy minimum point is a supply voltage of 0.54 V at a frequency of 18.2 MHz, at which 298 fJ/cycle in a write operation and 650 fJ/cycle in a read operation are achieved with the help of the majority logic; these factor are 87% and 52% smaller than those in a 28-nm FD-SOI 6T SRAM.

## ACKNOWLEDGEMENT

We would like to thank STMicroelectronics for chip implementation. This work was supported by STARC, VLSI Design and Education Center (VDEC), The University of Tokyo with the collaboration with Cadence Corporation, Mentor Graphics Corporation, Synopsys Inc., CMP Inc., and Renesus Electronics Corporation.

## REFERENCES

[1] J. Miyakoshi, Y. Murauchi, K. Hamano, M. Miyama and M. Yoshimoto, "A Low-Power Systolic Array Architecture for Block-Matching Motion Estimation" *IEICE Trans. Electron*, vol.E88-C, no.4, pp.559–569, April 2005.

[2] N. Planes, O. Weber, V. Barral et al., "28-nm FDSOI Technology Platform for High-Speed Low-Voltage Digital Applications" *IEEE Symposium on VLSI Tech.*, pp.133–134, June 2012.

[3] P. Flatresse, B. Giraud, J. Noel, et al., "Ultra-Wide Body-Bias Range LDPC Decoder in 28-nm UTBB FDSOI Technology" *ISSCC Dig. of Tech. Papers*, pp.424–425, Feb. 2013.

[4] C. Fenouillet-Beranger, S. Denorme, B. Icard et al., "Fully-Depleted SOI Technology using High-K and Single-Metal Gate for 32nm Node LSTP Applications featuring 0.179μm$^2$ 6T-SRAM bitcell" *IEEE IEDM*, pp.267–270, Dec. 2007.

[5] O. Thomas, B. Zimmer, B. Pelloux-Prayer, N. Planes, K-C. Akyel, L. Ciampolini, P. Flatresse and B. Nikolić, "6T SRAM Design for Wide Voltage Range in 28-nm FDSOI" *IEEE Int. SOI Conf.*, pp. 1–2, Oct. 2012.

[6] H. Fujiwara, T. Takeuchi, Y. Otake, M. Yoshimoto, and H. Kawaguchi, "An Inter-Die Variability Compensation Scheme for 0.42-V 486-kb FD-SOI SRAM using Substrate Control" *IEEE Int. SOI Conf.*, pp. 93–94, Oct. 2008.

[7] L. Hutin, C. Royer, F. Andrieu et al., "Dual Strained Channel Co-Integration into CMOS, RO and SRAM cells on FDSOI down to 17nm Gate Length" *IEEE IEDM Tech. Dig.*, pp. 11.1.1–11.1.4, Dec. 2010.

[8] S. Yoshimoto, M. Terada, S. Okumura, T. Suzuki, S. Miyano, H. Kawaguchi and M. Yoshimoto, "A 40-nm 0.5-V 20.1-μW/MHz 8T SRAM with Low-Energy Disturb Mitigation Scheme" *IEEE Symposium on VLSI Circ.,* pp. 72–73, June 2011.

[9] D. Wang, H. Lin, C. Chuang and W. Hwang, "Low-Power Multiport SRAM With Cross-Point Write Word-Lines, Shared Write Bit-Lines, and Shared Write Row-Access Transistors" *IEEE Trans. Circuits and Systems II Exp. Briefs*, vol61, no.3, pp. 188–192, March 2014.

[10] H. Fujiwara, K. Nii, H. Noguchi, J. Miyakoshi, Y. Murachi, Y. Morita, H. Kawaguchi and M. Yoshimoto, "Novel Video Memory Reduces 45% of Bitline Power Using Majority Logic and Data-Bit Reordering" *IEEE Trans. VLSI Systems*, vol.16, no.6, pp. 620–627, June 2008.