A Dual-Tank LC VCO Topology Approaching Towards the Maximum Thermodynamically-Achievable Oscillator FoM

Amir Nikpaik[1,2], Abdolreza Nabavi[2], Amir Hossein Masnadi Shirazi[1], Sudip Shekhar[1], Shahriar Mirabbasi[1]

[1]University of British Columbia, Vancouver, BC, Canada. [2]Tarbiat Modares University, Tehran, Iran

***Abstract* —There exists a fundamental limit in improving the phase noise performance of LC-tank oscillators. Impediments to reach this limit are first discussed, and then a clipping LC VCO topology based on dual tank is presented to mitigate them. This topology can approach within 3 dB of the maximum thermodynamically achievable figure-of-merit (FoM) limit. Compared to conventional class-B/C/D/F oscillators, it is capable of reducing both close-in and far-out phase noise. As a proof of concept, a prototype 4.17 – 4.95 GHz VCO in a 0.13-µm CMOS process achieves a phase noise of –97 and –143 dBc/Hz at 30 kHz and 3 MHz offset, respectively.**

***Index Terms* —impulse sensitivity function, low phase noise**

I. Introduction

Wireless standards such as 802.11a/b/g and GSM demand strict close-in and far-out phase noise specifications, respectively, for mobile handsets and base-stations [1]. Together with CMOS scaling that has reduced the supply voltage and increased the flicker noise corner, design of low phase noise CMOS *LC*-VCOs has been a significant challenge and a major research focus over the last decade [2]-[7].

A major limitation in lowering the phase noise of CMOS LC VCOs comes from the constrain of implementing small tank inductance, L, with high tank quality factor, Q. Consider Leeson's expression [3] for thermally induced phase noise of a sinusoidal oscillator at an offset of $\Delta\omega$ from the oscillation frequency of ω_{osc} :

$$\mathcal{L}(\Delta\omega) = 10log\left(\frac{kT}{2Q^2}\frac{F}{P_{RF}}\left(\frac{\omega_{osc}}{\Delta\omega}\right)^2\right) \quad (1)$$

where k is the Boltzmann constant, T is the absolute temperature, P_{RF} is the power dissipated in the tank and F is a topology-dependent phase-noise factor. Clearly, maximizing P_{RF} and Q, and minimizing F results in minimum attainable phase noise for a specific topology. As $P_{RF} = A_0^2/(2R_p)$, where, A_0 is the oscillation amplitude and R_p is the equivalent parallel loss of the tank, maximum P_{RF} is achieved when the voltage swing across the tank is maximized while R_p is minimized. Finally, as $R_p = L\times Q\times\omega_{osc}$, L should be decreased to lower the phase noise, although at the cost of higher power consumption. *In practice*, L could not be arbitrarily lowered, as small inductors have inferior quality factors which not only mask the phase noise improvement achieved by decreasing R_p but also adversely affect the oscillation start-up and FoM. FoM compares the phase noise of different oscillators normalized to their DC power consumption, P_{DC} [3]:

$$FoM = 10log\left(\frac{2Q^2}{10^3kT}\frac{1}{F}\frac{P_{RF}}{P_{DC}}\right) = FoM_{MAX} + 10log\left(\frac{\eta_P}{F}\right) \quad (2)$$

where $\eta_P=P_{RF}/P_{DC}$ is the oscillator power efficiency, and FoM_{MAX} is the maximum thermodynamic FoM limit with F = 1 and η_P = 100% [3]. Beyond maximizing Q and minimizing F, the oscillator power efficiency η_P should be maximized for the largest possible FoM.

A solution to mitigate the trade-off between inductor value and the tank Q is to use transformers in the oscillator core [4], [5]. Shaping the oscillator voltage swing by superimposing a differential excitation at fundamental and common-mode excitation at the 2nd harmonic using two transformers, [5] realized an R_p reduction. However, designing a transformer in which both primary and secondary inductors exhibit maximum Q is challenging. Moreover, the design and optimization of the transformers needs extensive and time-consuming electromagnetic simulations which add to design complexity and decrease design flexibility.

In this paper, we leverage a dual tank using two inductors to shape the differential and common-mode excitations, and present a VCO which is capable of delivering very low phase noise oscillations without sacrificing the tank quality factor. The presented structure could exhibit a power efficiency near 90% and shows lower noise factor (F) compared to ideal class-B [6], class-C [3], and class-D [2] oscillators. Furthermore, the structure is optimized to up-convert less amount of flicker noise to phase noise using floating-tank capacitance. The advantage of floating-tank capacitance in improving far-out phase noise has been shown earlier [2]; herein, we leverage it in suppressing flicker-noise upconversion in the proposed topology. Simulation results show that the proposed oscillator could approach within 3 dB of FoM_{MAX}.

II. A Dual-Tank Hard-Clipping LC-VCO

Fig. 1 shows the proposed oscillator topology employing a dual LC tank. The resonance circuit is similar to that used

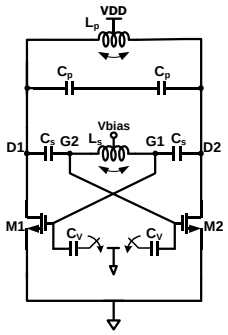

Fig. 1. A dual-tank hard-clipping LC oscillator.

in [7], however, the behavior of the oscillator is quite different. First, C_p in the proposed tank is a floating capacitance and the tank is modified to exhibit another resonance peak at $2\omega_{osc}$ when excited with a common-mode input current. Second, the transistor sizing is chosen such that the output voltage is clipped to ground when transistors turn on.

The frequency response of the tank for its different nodes is shown in Fig. 2. The G1 and D1 differential-mode curves show the gate and drain voltage response to the odd mode input current, respectively, whereas the common-mode curve exhibits the drain voltage response to an even mode current excitation. As shown in Fig. 2, this resonator exhibits two (odd mode) resonance frequencies, i.e., ω_1 and ω_2:

$$\omega_{1,2} = \frac{1}{\sqrt{2}}\omega_p\sqrt{\frac{2m+n+1\pm\sqrt{4m^2+(n-1)^2}}{mn+m+n}} \qquad (3)$$

where, $C_s = mC_p$, $C_v = nC_p$, and $\omega_p = 1/\sqrt{L_pC_p}$. Only the phase shift at ω_2 satisfies the Barkhausen criteria, leading to the desired oscillation frequency at ω_2. For example, assuming $L_p = L_s$, $C_p = 3C_s$ and a negligible C_v, $\omega_2 \approx 2\omega_p$ or $1.15\omega_s$.

A. Tank Equivalent Impedance, R_p, and Quality Factor, Q

From Fig. 2, depending on the proximity of ω_2 to ω_s, the input impedance of the tank at the oscillation frequency (R_p) could be decreased. For example, for the abovementioned tank components and with $C_v = C_s$, R_p of the proposed tank is equivalent to that of a conventional LC tank with an inductance = *L/6* and the *same Q*. Thus, using this dual-tank circumvents the use of impractically scaled inductors which not only have an inferior Q but also are more vulnerable to further degradation in Q due to the parasitic series resistance of the interconnects.

Another advantage of using the proposed tank is that it provides a passive voltage amplification between the drain and the gate nodes, which, as will be discussed later, is beneficial in increasing η_p and decreasing F. The voltage gain from V_D to V_G can be expressed as:

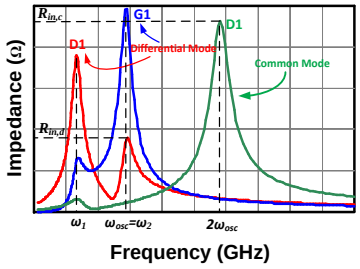

Fig. 2. Frequency response of the dual-tank.

$$G = \left|\frac{V_G}{V_D}(j\omega)\right|_{\omega=\omega_1} \cong \frac{mk^2}{(m+n)k^2-1} \qquad (4)$$

where, $k = \omega_1/\omega_p$. The amplification factor can be set by choosing a capacitance ratio (i.e., m and n). For the abovementioned tank elements, G ≈ 3.3. As mentioned earlier, achieving such a relatively high passive gain and low R_p using transformers may be difficult unless the overall tank Q is degraded.

B. Power Efficiency (η_P)

The output voltage of the oscillator is clipped to near 0 V in about half of the period, hence, it contains a strong second harmonic. The tank's resonance peak at the second harmonic causes this 2nd harmonic voltage to add *in-phase* with the fundamental component. Fig. 3 (a) and (b) show the drain and the gate voltage waveforms with single-ended and floating C_p, respectively. In the former case, the 2nd harmonic resonance is eliminated by connecting the middle node of the C_p capacitors to the ground. The tank remains unchanged from the 1st harmonic perspective. V_D starts to depart from 0 V when V_G is still quite high (Fig. 3(a)) and thus the transistor is conducting a significant current. Consequently, the product of the drain voltage and the channel current will be not be insignificant. In contrast, in the latter case with the floating C_p, V_D remains close to the ground when V_G has a large value. As a result, the product of channel current and drain voltage will be close to zero across the oscillation period. Also, since the voltage swing at the gate of the transistors is increased, their R_{on} decreases which further improves the power efficiency. Simulations show that the voltage efficiency (V_{RF}/V_{DD}) and current efficiency (I_{RF}/I_{DC}) of the proposed circuit is about 1.45 and 0.63, respectively, which results in a power efficiency of more than 90%.

C. Phase-Noise Factor (F)

According to Hajimiri's phase noise theory [8]:

$$F = \sum_i \frac{1}{T}\int_T \left(\Gamma_i(\omega_{osc}t)\alpha(\omega_{osc}t)\right)^2 dt \qquad (5)$$

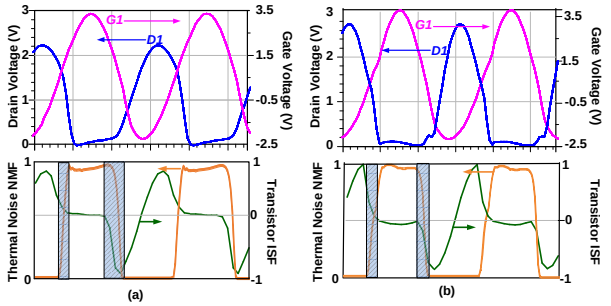

Fig. 3. The oscillator waveforms (top) and the simulated ISF and NMF (down) for (a) single-ended and (b) floating C_p.

where T is the oscillation period, Γ_i is the impulse sensitivity function (ISF) of the oscillator phase associated with the perturbation from the i^{th} noise source and $\alpha(\omega_{osc}t)$ is the periodic noise modulating function (NMF), capturing the time-varying properties of the noise power spectral density (PSD).

In the proposed circuit, the conversion of the channel thermal noise to phase noise has been significantly suppressed because of the following:

1) As shown in Fig. 3, the sensitivity of the oscillator to noise (ISF) is near zero when the output voltage is clipped [4]. Transistor noise translates into phase noise only during rise/fall time where both ISF and NMF have nonzero value, shown as the shaded area in Fig. 3. As illustrated in these plots, in the case with even mode resonance, in-phase second harmonic voltage aligns the transistor's NMF with its ISF and reduces their overlap, whereas in the case without even harmonic resonance, anti-phase second harmonic increases the effective ISF (i.e. product of ISF and NMF, depicted by the width of the shaded area). Phase noise simulations show that the contribution of the transistors channel thermal noise is only about 16% of the total phase noise, while for the VCO without 2nd harmonic peak, it is about 40%.

2) Voltage amplification between the gate and the drain sharpens rise and fall times wherein the oscillation phase is most sensitive to the circuit noise.

3) The gate is biased (V_{bias}) near the threshold voltage of the transistor to reduce MOS thermal noise excess factor (γ). Fig. 4 shows that the simulated γ for a transistor increases significantly with its gate-source voltage. For example, when V_{bias} = 1 V the transistor generates twice the thermal noise compared to when V_{bias} = 0.5 V with same g_m. In the proposed VCO, transistor's channel thermal noise mostly converts to phase noise near rise/fall time of the waveform, thus a lower V_{bias} suppresses noisier transitions.

D. Flicker Noise to Phase Noise Conversion

Due to the time-varying operation of the transistors, their flicker noise is cyclostationary stochastic in nature

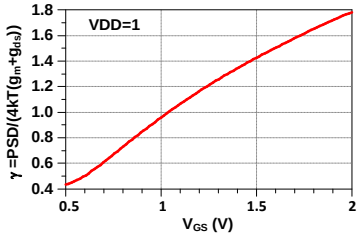

Fig. 4. Simulated thermal noise excess factor (γ) for a short-channel device.

with a periodic time-varying PSD. As a result, it gets multiplied by a periodic NMF and up-converts to the components around the carrier harmonics and injects into the tank. Depending on the shape of the NMF, these noise components could be injected as phase-modulation (PM) sidebands or amplitude-modulation (AM) sidebands. PM sideband of the noise current directly modulates the phase of the oscillation and hence directly translates into the phase noise, while AM noise components may convert to the phase noise by changing the effective tank capacitance or by modulating the harmonic content of the tank (incremental Groszkowski effect [10]). As mentioned before, common mode resonance causes the fundamental tone of the channel current to be in-phase with respect to the output voltage. Since flicker noise PSD of a MOS transistor is proportional to its instantaneous channel current, in-phase channel current and output voltage leads to negligible PM noise current, thereby significantly reducing the close-in phase noise of the proposed oscillator. A similar technique has been recently reported to mitigate flicker noise upconversion [11], [12]. It should be noted that intrinsic amplitude limiting mechanism of the proposed oscillator, due to its hard clipping behavior, mitigates AM-to-PM conversion significantly [4].

III. Simulations and Measurement Results

For a fair comparison, taking into account various secondary effects (e.g. device short-channel effects), different oscillator topologies have been simulated in the same CMOS process with inductors of equal quality factor. Each topology has been separately optimized to achieve the highest possible FoM. Fig. 5 compares their oscillator design efficiency (ODE) [13], $\Upsilon = \eta_P/F$. ODE is a measure of attaining the thermodynamic limit FoM_{MAX} in (2), with Υ=100%. The proposed topology can reach a FoM within 3 dB of FoM_{MAX}.

The proposed dual-tank VCO is implemented in a 0.13-μm RF CMOS process, employing standard symmetrical center-tapped inductors available in the technology design kit. The tank capacitor bank comprises of four binary-weighted switched capacitors, implemented as metal-

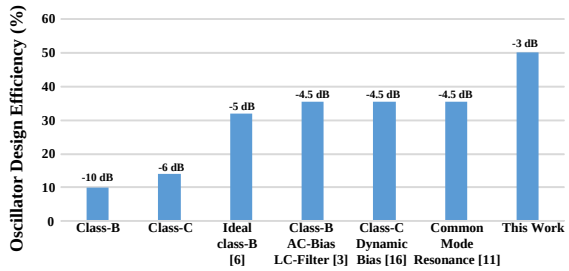

Fig. 5. ODE comparison of different topologies

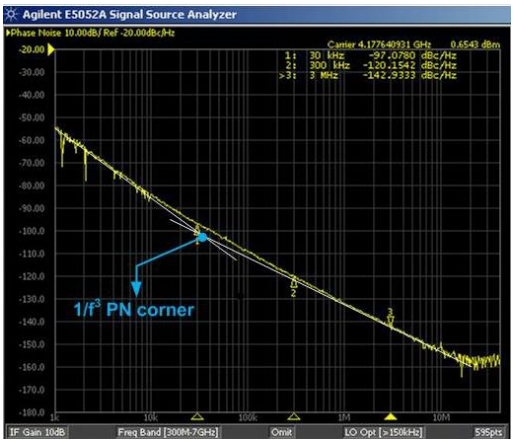

Fig. 6. Measured phase noise at 4.17 GHz.

insulator-metal (MIM) capacitors. Thick-oxide devices are used to withstand high voltage swings at the gate and drain of the transistors for reliability. Open-drain buffers are used to deliver the oscillation voltage out of the chip. The output frequency of the oscillator spans a range from 4.17 GHz to 4.95 GHz. Fig. 6 shows the measured phase noise at 4.17 GHz with the VCO consuming 33 mA from a 0.9 V supply. The phase noise is measured as −143 dBc/Hz at 3 MHz frequency offset which extrapolates to −172.6 dBc/Hz at a 20 MHz offset when the frequency is normalized to a 915 MHz GSM carrier [1]. The flicker noise corner is about 30 kHz, and increases to about 130 kHz at 4.95 GHz oscillation frequency. FoM variation at a given offset frequency is less than 2 dB across the tuning range. Fig. 7 shows the die micrograph of the implemented oscillator. Table I summarizes the performance of the proposed oscillator and compares it with the state-of-the-art designs.

IV. Conclusion

An LC oscillator that leverages a dual-tank with floating capacitor and hard limiting swing is presented to break the trade-off between the inductor value and Q in order to attain ultra-low phase noise at *both* thermal- and flicker-noise dominated regions. The proposed oscillator can exhibit an

TABLE I: Performance Summary and Comparison to VCOs with FoM >190

	This Work	[1]	[2]	[4]	[5]	[14]	[11]	[12]	[15]
CMOS Tech [nm]	130	350	65	65	65	65	28	40	130
VDD [V]	0.9	2.5	0.4	1.5	1.3	1.25	0.9	1.0	1.4
Frequency [GHz]	4.17	1.2	3	3.92	4.35	3.7	3.33	5.4	2.4
Tuning Range [%]	16	18	46	10.2	19	25	27.2	25	1.7
Power [mW]	30	9.25	6.8	48	41.6	15	6.8	12	4.2
≈1/f Noise Corner [kHz]	30	200	2000	650	300	750	200	60	NA
FoM (30kHz) [dB]	185.3	NA	NA	NA	181	NA	183	187	189.8
$\mathcal{L}_N$*(3MHz) [dBc/Hz]	-156.2	-154.8	-149	-157.2	-158.3	-154.3	-150.8	-152	-146.3
FoM (3MHz) [dB]	191.3	195	191	190.1	191.5	192.2	192.2	190.5	190
# spirals	2	2	1	2	2	1	1	1	1
EM Simulation	No	No	No	Yes	Yes	Yes	Yes	Yes	No

*$\mathcal{L}$ normalized to 915 MHz carrier frequency

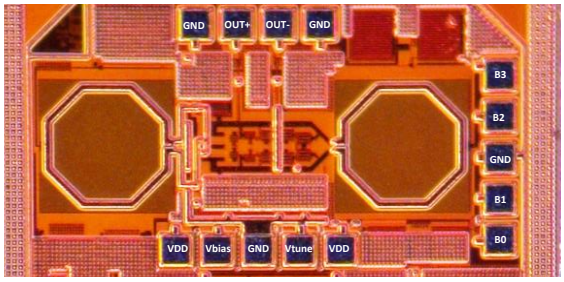

Fig. 7. Die Micrograph.

Oscillator design efficiency exceeding 50% which is equivalent to a FoM within 3 dB of FoM_{MAX}. At the area expense of two inductors, the proposed prototype attains state-of-the-art phase noise and FoM at close-in and far-out offsets, low flicker-noise corner frequency, >15% tuning range from a low supply voltage, and does not require complicated EM simulations.

Acknowledgement

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