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April 16 and 17th, 2025 – Boston, MA – USA

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Keynote Speakers

Petascale photonic connectivity for energy efficient computing

Prof. Keren Bergman

Columbia University

Chip to Chip Communication for Next Generation AI Datacenters

Dr. Tom Gray

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Speakers

Tod Dickson

IBM

Tony Mastroianni

SIEMENS

Andreas Olofsson

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Deepak Kulkarni

AMD

Luca Benini

ALMA MATER STUDIORUM UNIVERSITÀ DI BOLOGNA

Tony Chan Carusone

ALPHAWAVE

Surhud Khare

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Yin Hang

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Henry Sheng

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Mehul Shroff

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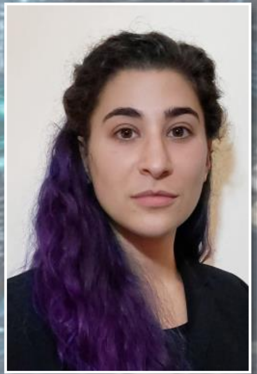

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Chip to Chip Communication for Next Generation AI Datacenters

ABSTRACT: AI applications on GPU systems have exploded with single-chip inference performance increasing 1000X over the last 10 years. Tens of thousands of datacenter connected GPUs are needed for training and inference of state-of-the-art generative AI models. Bandwidth density requirements increase on the order of 2x in each generation. At the core of these systems, processors and switches are implemented as multiple die in 2.5D and 3D configurations. Ultra efficient interconnect between these die in the system is required to support the overall system bandwidths. This talk will look at state-of-the-art current and future electrical and optical chip-to-chip communication from the standpoint of circuits, packaging, power delivery, and thermal management targeting energy efficiencies <100fJ/b and bandwidth density >10Tbps/mm.

Dr. Tom Gray

NVIDIA

BIO: C. Thomas Gray received the B.S. degree in computer science and mathematics from Mississippi College, Clinton, MS, USA, and the M.S. and Ph.D. degrees in computer engineering from North Carolina State University, Raleigh, NC, USA. He worked in a variety of different roles at IBM, Cadence Design Systems, Artisan/ARM, and Nethra Imaging in the Raleigh/Durham, NC, USA, area primarily as a SerDes System Architect. His work experience includes digital signal processing design and CMOS implementation of DSP blocks as well as high-speed serial link communication systems, architectures, and implementation. In 2011, he joined NVIDIA, Inc., Durham, NC, USA, where he is currently Senior Director of Circuit Research, leading activities related to high-speed electrical signaling, photonics, power delivery, security circuits, low-energy and resilient memories, circuits for machine learning, and variation-tolerant clocking and power delivery.

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Petascale photonic connectivity for energy efficient computing

ABSTRACT: High-performance systems are increasingly bottlenecked by the energy and communications costs of interconnecting numerous compute and memory resources. Current systems face a gap of nearly two orders of magnitude between on-chip, intra-socket, communication capacities, and the capacities of links transporting data over longer distances. The per bit energy cost of data movement dominates that of data processing, as does density, throughput, and latency. Integrated silicon photonics offer the opportunity of optical connectivity that delivers high off-chip communication bandwidth densities with low power consumption. To realize these benefits the co-integration of photonics with the compute and memory is critical. This talk will cover approaches for leveraging photonic IO that can scale to realize Petabit/s chip escape bandwidths with sub-picojoule/bit energy consumption, as well as new architectural approaches that enable flexible connectivity tailored to accelerate distributed AI/ML applications.

Prof. Keren Bergman

Columbia University

BIO: Keren Bergman is the Charles Batchelor Professor of Electrical Engineering at Columbia University where she also serves as the Faculty Director of the Columbia Nano Initiative. Bergman received the B.S. from Bucknell University in 1988, and the M.S. in 1991 and Ph.D. in 1994 from M.I.T. all in Electrical Engineering. At Columbia, Bergman leads the Lightwave Research Laboratory encompassing multiple cross-disciplinary programs at the intersection of computing and photonics. Since 2023 Bergman is the Director of the Center for Ubiquitous Connectivity (CUbiC), a 5-year multi-university center funded by DARPA and the Semiconductor Research Corporation (SRC) under the Joint University Microelectronics Program 2.0 (JUMP 2.0). Bergman serves on the Leadership Council of the American Institute of Manufacturing (AIM) Photonics leading projects that support the institute’s silicon photonics manufacturing capabilities and Datacom applications. She is the recipient of the IEEE Photonics Engineering Award and is a Fellow of Optica and IEEE.

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Chiplets and Connectivity Driving Next-Gen AI Networks

Prof. Tony Chan Carusone

ALPHAWAVE SEMI

ABSTRACT: This talk describes the critical synergy between chiplets and connectivity: chiplets enable the connectivity for next-generation AI networks, while die-to-die connectivity enables chiplet architectures. We will see why heterogeneous integration is desirable for high-speed wireline transmitter and receiver circuits, motivating the disaggregation of SerDes from large processors and switch chips onto their own dedicated I/O chiplets. The changing role of electrical and optical links in networks for AI clusters will be highlighted. These evolving applications are creating new demands; principal among them in high-performance systems is bandwidth density. Whereas co-packed optics (CPO) promises an ultimate solution, combining high aggregate bandwidth and low power consumption remains challenging. Alternative CPO chiplet architectures will be presented and evaluated in pursuit of those goals. The tradeoffs between higher serial data rates vs. higher parallelism are explored. New CPO architectures also present unique demands on the associated chiplet interfaces. With advanced packaging technologies continuing to evolve, and new packaging technologies emerging, chiplet interfaces must also progress. The presentation will also consider the role of standards during this period of rapid technological evolution.

BIO: Tony Chan Carusone (S’96–M’02–SM’08–F’22) received his Ph.D. from the University of Toronto in 2002 and has since been a professor in the University of Toronto’s Department of Electrical and Computer Engineering. He has also been a consultant to industry in the areas of integrated circuit design and digital communication since 1997. He is currently the Chief Technology Officer of Alphawave Semi. Prof. Chan Carusone has co-authored 9 Best Paper Award winners at leading conferences on wireline electrical and optical transceivers and analog integrated circuits. He co-authored the popular textbooks “Analog Integrated Circuit Design” and “Microelectronic Circuits.” He was Editor-in-Chief of the IEEE Transactions on Circuits and Systems II: Express Briefs in 2009, an Associate Editor for the IEEE Journal of Solid-State Circuits 2010-2017, and Editor-in-Chief of the IEEE Solid-State Circuits Letters 2021-2023. He was a Distinguished Lecturer for the IEEE Solid-State Circuits Society 2015-2017 and has served on the Technical Program Committee of several IEEE conferences including the International Solid-State Circuits Conference 2016-2021. He is an IEEE Fellow.

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Power-Efficient Short Reach Electrical Links for the AI Era

ABSTRACT: Data center, compute, and AI applications continue to demand higher bandwidth from electrical interconnects. The volume of short-reach links (less than a few cm) has exploded to facilitate high-bandwidth data movement between compute engines and memory in the AI era. This massive growth will continue as the industry moves towards highly-parallelized die-to-die interfaces to support chiplet-based architectures. However, power efficiency in these links is of paramount importance to maintain reasonable power levels within a compute drawer. This talk will focus on trends and advancements in power-efficient short reach links that aim to maximize the shoreline bandwidth density. Multi-disciplinary approaches involving circuit innovations, architectural advancements, data signaling techniques, and packaging technologies are required to deliver linear bandwidth densities above 1 Tbps/mm at power efficiencies below 500 fJ/bit.

Dr. Tod Dickson
IBM T.J. Watson Research Center

BIO: Timothy (Tod) Dickson received the BS and M.Eng. degrees from the University of Florida, and the Ph.D. degree from the University of Toronto. Since 2006 he has been with the IBM T.J. Watson Research Center in Yorktown Heights, NY where he is currently a Principal Research Scientist. His research is on circuits and architectures for power-efficient serial communication. He is also an Adjunct Professor at Columbia University in New York, NY.

Dr. Dickson has been an author or co-author of several papers that have received best paper awards, including the inaugural VLSI Circuits Symposium Best Student Paper Award in 2004, the IEEE Journal of Solid-State Circuits Best Paper in 2009, the ISSCC Beatrice Winner Award in 2009, and the IEEE CICC Best Regular Paper Award in 2015 and Best Invited Paper Award in 2024. He served on the TPC of the IEEE CICC from 2017-2023 and was an Associate Editor of the IEEE Solid State Circuits Letters over the same time period. He is currently an Associate Editor of the IEEE Open Journal of the Solid-State Circuits Society and IEEE SSCS Distinguished Lecturer. He is an IEEE Senior Member.

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Open Chiplet Platforms for Embodied AI

Prof. Luca Benini

ALMA MATER STUDIORUM
UNIVERSITÀ DI BOLOGNA

ABSTRACT: AI capabilities are being "embodied" everywhere, from earbuds to cars. Embodied AI needs to tackle major challenges in energy efficiency, safety, security, and real-time predictability, while curtailing computational complexity. Chiplet-based architectures are needed for achieving the level of embodied intelligence needed for autonomous agents in the physical word: robots, cars, satellites. In this talk I will describe Occamy, a chiplet-based RISC-V architecture for embodied, agentic AI, and detail its design, implementation, and the roadmap for future evolution. I will emphasize the strategic importance of an open-platform approach to ensure a healthy innovation ecosystem, long term sustainability, safety and security.

BIO: Luca Benini holds the chair of digital Circuits and systems at ETHZ and is Full Professor at the Università di Bologna. He received a PhD from Stanford University. His research interests are in energy-efficient parallel computing systems, smart sensing micro-systems and machine learning hardware. He is a Fellow of the IEEE, of the ACM, a member of the Academia Europaea and of the Italian Academy of Engineering and Technology. He is the recipient of the 2016 IEEE CAS Mac Van Valkenburg award, the 2020 EDAA achievement Award, the 2020 ACM/IEEE A. Richard Newton Award, the 2023 IEEE CS E.J. McCluskey Award, and the 2024 IEEE CS Open Source Hardware contribution Award.

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Architecting Heterogenous System-of-Chiplets for Data Center and AI Era

Surhud Khare

ABSTRACT: Data Center CPU, GPU and AI accelerators have evolved from monolithic System-on-Chip designs to heterogenous System-of-Chiplets to enable “More-than-Moore” scaling of system-level performance and energy efficiency at lower costs. This presentation highlights importance of interdisciplinary System-Technology Co-Optimizations (STCO) for architecting such heterogenous System-of-Chiplets. We will discuss architecture and design considerations for optimizing compute, memory and interconnect components, as well as trade-offs and co-optimization opportunities with process/packaging technologies, power delivery, thermals and system architectures. We will also highlight future trends and innovations required to drive continued performance and efficiency improvements for the AI era.

BIO: Surhud Khare is a Principal Engineer in Data Center and AI Silicon Engineering Group at Intel Corporation. His areas of expertise include 3DIC process/packaging technologies, Silicon architecture/design optimizations for Heterogenous Integration and System-Technology Co-Optimization (STCO). Most recently, Surhud has contributed to Intel’s EMIB, Foveros and Foveros-Direct (Hybrid Bonding) technology definitions and physical architecture/design co-optimizations for multiple generations of Intel Xeon® and AI products. Surhud joined Intel in 2009 as part of Advanced Microprocessor Research Lab working on low-voltage circuits and CPU/SoC test-chip designs. Subsequently, he was a technical lead in Extreme-Scale Computing group working on energy-efficient interconnects/accelerator architectures and silicon/package prototype designs for Exascale Computing R&D projects. Surhud holds M.S. degree in Electrical and Computer Engineering from Georgia Institute of Technology, Atlanta. He has co-authored 24 patents/publications and serves on technical program committees for several premier technical conferences. Surhud is a Senior Member of IEEE.

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Building Composable Chiplets

Andreas Olofsson

zero

ABSTRACT: Chiplets present a compelling approach to reducing the cost and time of chip design by raising the abstraction level to the die. In this talk, I will share my decade-long experience with chiplets and examine the current challenges blocking effective chiplet-based design for startups, government, and academia. Additionally, I will introduce recent work on composable (“interchangeable”) chiplets, where O(M^N) unique silicon systems can be assembled from N chiplets arbitrarily selected from a library of size M. To illustrate the potential of this approach, consider a 10 chiplet system built from a library of 10 chiplets, enabling the creation of 10^9 unique configurations. In contrast, fewer than 10^3 unique chip tape-outs occur worldwide each year. Standing up a practical composable chiplet platform on par with the existing SoC design ecosystem will require enormous investments, but if done right has the potential of fundamentally disrupting the semiconductor industry.

BIO: Andreas Olofsson is the founder and CEO of Zero ASIC, a semiconductor startup on a mission to democratize silicon. From 2017 - 2020, Andreas was a program manager at DARPA, where he managed 8 different US research programs in heterogeneous integration, EDA, high performance computing, machine learning, and analog computing. From 2008-2017, Andreas founded and managed Adapteva, an ultra lean fabless semiconductor startup that led the industry in processing energy efficiency. Prior to Adapteva he worked at Analog Devices for 10 years as a design manager and architect for advanced DSPs and mixed signal devices, developing products that shipped in over 100 million systems. Andreas received his Bachelor of Science in Physics and Electrical Engineering and Master of Science in Electrical Engineering from the University of Pennsylvania. He is a senior member of IEEE and holds nine U.S. patents.

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Enabling AI revolution through innovations in advanced packaging and chiplet technology

Dr. Deepak Kulkarni

AMD

ABSTRACT: The rise of large language models is leading to significant demand for memory and high-bandwidth interconnects between compute and memory chips. However, the slowdown of Moore’s Law has made it difficult to meet this demand using traditional monolithic processors. Chiplet architecture offers a solution to address the ever-growing need for compute and memory. By creating custom, modular chiplets and integrating heterogeneous architectures into a single package, overall processor performance can be improved. Advanced packaging technologies, such as 2.5D and 3D packaging, provide methods to enhance the energy efficiency of these interconnects. In this talk, we will explore the compute and memory demand for AI accelerator chips in greater detail. We will review AMD's latest innovations in utilizing 2.5D and 3D packaging to enhance performance and energy efficiency. Additionally, we will discuss the design processes and co-optimizations necessary to achieve higher performance while managing costs and power consumption. We will conclude with a summary of the opportunities and challenges that lie ahead in this evolving field.

BIO: Deepak Kulkarni is currently a Senior Fellow at Advanced Micro Devices (AMD), where he leads the Advanced Technology Integration team. In his role, Deepak is responsible for designing and developing innovative packaging technologies across AMD’s extensive product portfolio, which includes Central Processing Units (CPUs), Graphics Processing Units (GPUs), and Artificial Intelligence (AI) accelerators. With 19 years of experience in packaging, Deepak has overseen the development of several industry-leading innovations, including panel-level fan-out, Embedded Multi-die Interconnect Bridge (EMIB), Elevated Fan-Out Bridge (EFB), and 3.5D packaging solutions. Prior to his tenure at AMD, he served as Senior Director at Intel Corporation. Deepak's areas of interest include multi-physics simulations, AI-based design-for-manufacturing, and design-technology co-optimization. He holds 31 patents and has authored over 20 publications related to 2.5D/3D architectures and AI applications in yield management. His significant contributions to the semiconductor industry have been recognized with several awards, including the Intel Achievement Award, AMD Next 5% Award, and the Best Paper Award from ITHERM. Deepak earned his PhD in Mechanical Engineering with a minor in Computational Science from the University of Illinois at Urbana-Champaign.

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STCO, a new design paradigm to meet the challenges in designing 3D IC designs

Tony Mastroianni

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ABSTRACT: System technology co-optimization (STCO) is a new design paradigm introduced by IMEC to address the increasing cost and diminishing performance scaling in today’s advanced IC technology nodes. This innovative design paradigm leverages new advanced package manufacturing technologies to integrate multiple IC’s, referred to as chiplets into a single package referred to as a 3D IC design. 3D IC designs require a system-oriented approach, integrating system, IC, package and multi-physics simulation tools and workflows as well as a new set of design enablement kits to support a heterogeneous manufacturing supply chain. In this presentation we explore these new STCO design methods which enable the design planning, implementation, verification, manufacturing and deployment of these new 3D IC designs.

BIO: Tony Mastroianni has extensive engineering management experience in the global semiconductor industry. In recent years, he has focused significantly on advanced ASIC package design workflow development (2.5/3D). He currently leads development of Advanced Packaging Solutions for Siemens Digital Industries Software. Prior to joining Siemens, he served in engineering leadership positions at Inphi and eSilicon. He earned a bachelor’s degree in electrical engineering from Lehigh University and a master’s degree in electrical engineering at Rutgers University. He is the author of several technical articles and has presented at several industry conferences and has been interviewed in several technical publications. He is an active member in the OCP Chiplet Design Exchange (CDX) working group that is actively driving new and open 3D IC standards and workflows.

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EDA Solutions for Chiplet-based Multi-Die Systems

Dr. Henry Sheng

SYNOPSYS®

ABSTRACT: Chiplet-based design has rapidly grown in significance and complexity. This design process involves the creation of systems built from chips and interconnects using multiple silicon node technologies, package technologies, optical technologies, thermal mitigation, and more. This demands a new class of EDA solution which enables the design and management of complex heterogeneous systems. At the same time the scale of integration has increased non-linearly with the pitch of die-to-die interconnect such as bump and hybrid bonds. Higher levels of integration also enable key standards such as HBM to grow in bit count. These factors accumulate and demand scalable EDA solutions for chiplet based design. As integration densities grow, automation and optimization become the only viable way to sustainably implement large complex chiplet-based systems. This puts forth a need for automation and optimization at a system scale across heterogeneous components for key system QoR (quality of results) metrics such as SIPI, EMIR and Thermal.

BIO: Henry Sheng is Executive Director of R&D at Synopsys where he currently works on 3DIC design and implementation, advanced visualization and silicon innovation. He previously worked on physical implementation and led R&D efforts on foundry enablement of advanced nodes. He received his B.S. and Ph.D. degrees from the University of California, Berkeley in 1990 and 1996, respectively.

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Navigating the Cooling Conundrum: A Thermal Roadmap for AI Modules

Dr. Yin Hang

Meta

ABSTRACT: Advanced packaging technologies, such as chiplet architectures and heterogeneous architectures like 2.5D, 3D, and 3.5D hybrid bonded technologies, are becoming increasingly popular for driving performance and cost improvements in AI/ML hardware. However, these solutions also introduce additional complexity and thermal challenges. To address these challenges, ASIC and module cooling technology development is a key strategic enabler to ensure the competitiveness and scalability of AI/ML hardware roadmaps. These technologies aim to solve the high total power and increased power density challenges faced by AI/ML systems. This talk will identify areas for future thermal technology exploration at the ASIC and module level that require investment to extend the cooling capabilities of future AI/ML roadmaps. Investing in these areas will help ensure the continued development of high-performance and scalable AI/ML hardware.

BIO: Yin Hang is a Technical Lead Manager for thermal engineering at Meta Infra HW team. She leads the development of thermal designs and technologies for multiple platforms, including AI/ML, General Compute and Storage, and liquid cooling technology such as AALC (air assisted liquid cooling). Currently, she is focused on planning and pathfinding ASIC level cooling solutions, including package level, on die level, and new thermal interface materials and associated cooling solutions such as cold plate and embedded silicon microchannel technologies. Yin Hang holds a Ph.D. degree from Purdue University with a focus on heat transfer. She has contributed to technical papers and panel discussions and talks in conferences such as Itherm, Open Compute Project (OCP), and serves as the thermal lead on the NIC OCP group and co-lead on the Heterogeneous Integration Roadmap (HIR) thermal chapter.

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Reliability and Test of System-of-Chiplets in the AI Era

ABSTRACT: Semiconductor demand is rapidly expanding for existing and new applications, with more products being introduced for automotive, industrial, medical, avionics, and space applications in addition to the traditional computing and mobile applications. Diverse functionality and increased performance and reliability are needed to support high-criticality applications. Technologies continue to scale to ever-shrinking dimensions with novel materials, device architectures, and packaging to realize new power-performance-area levels. As a result, the industry is actively moving to a system-in-package approach where multiple chips, supporting different functions, are assembled in a single package. Comprehensive but cost-efficient test coverage is necessary to minimize escapes that lead to post-assembly or field failures. In addition to chip-level reliability, overall reliability of the multi-chip package needs to be assessed and guaranteed to ensure that the package does not fail prematurely. To meet these stringent requirements, chip designers, silicon and assembly manufacturers, product and test engineers, and design-tool vendors must collaboratively optimize technology, packaging, design, and test in a cohesive and transparent partnership while leveraging state-of-the-art machine-learning and artificial-intelligence techniques. This talk will explore the key considerations for silicon- and package-level reliability and test to ensure successful and cost-effective deployment of reliable products.

Mehul Shroff

BIO: Mehul Shroff is a Fellow and Six Sigma Black Belt at NXP Semiconductors in Austin, TX, with over 29 years of experience in the semiconductor industry. His current interests are focused on reliability tools and methodologies, design for reliability, and data science and machine learning for quality and reliability. His prior experience includes process integration and device engineering in manufacturing, technology transfer, and development, module development, yield engineering, and test vehicles and test structures. He holds graduate degrees in Chemical Engineering and Software Engineering.

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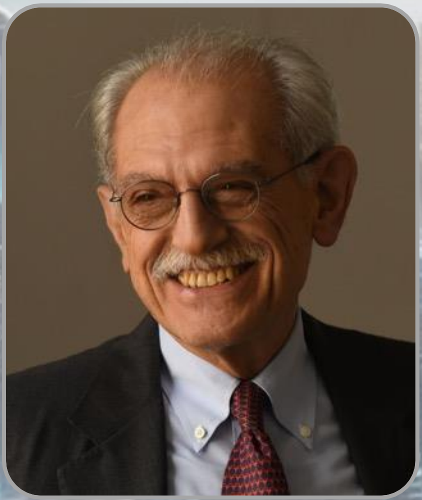

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