April 21-24, 2024
Denver, Colorado, USA
www.ieee-cicc.org

CICC

IEEE Custom Integrated Circuits Conference

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Welcome from the CICC Committee!

Welcome to the CICC 2024 conference! On behalf of the Steering Committee and the Technical Program Committee, we are honored and delighted to present the 44th annual IEEE Custom Integrated Circuits Conference (CICC) – a showcase for Integrated Circuits. The conference will be organized as a live event, on-site at the DoubleTree by Hilton Denver in Denver, Colorado. Our conference will be a vibrant forum for sharing state of the art techniques and results, learning from world-renowned experts in custom IC designs and adjacent fields, and networking in person with old and new colleagues.

CICC 2024 officially starts with 4 Educational Sessions on Sunday April 21st, followed by daily keynote presentations and technical lectures from Monday through Wednesday. Throughout the conference, 25 Technical Sessions, 4 Forum Sessions, and 4 Panel Sessions are strategically placed to highlight the latest trends and challenges. The Outstanding Paper awards and closing ceremony is scheduled at the end of the conference. Registration covers all the events including the Educational Sessions on Sunday. Top-rated papers will be invited to the special issues in the IEEE Journal of Solid-State Circuits and the IEEE Solid State Circuits Letters.

The four Educational Sessions provide background tutorial information on several topics of active research, including “Deep Learning and Compute-in-Memory Designs and Applications”, “Introduction to Quantum Computing for Circuit Designers”, “Optical and Wireline Communication Circuit Techniques” and “Nascent Sensing Devices and Interfaces”. All presenters are well known for their contributions in their respective areas.

The Technical Sessions are the backbone of our conference. This year’s Technical Sessions will showcase original innovative analog and digital circuit techniques covering a broad spectrum of technical topics, including: Analog Circuits, Data Converters, Design Foundations, Digital Circuits, Emerging Technologies, Power Management, Wireless Circuits, and Wireline Circuits. This year we are proud to offer a strong technical program with 126 lecture presentations, including 17 invited papers.

These Technical Sessions are complemented by Forums and Panels covering various popular areas related to integrated circuits and systems. We are pleased to offer 4 Forum Sessions, including “AI-based Chip/Chiplet Generation”, “Cutting-edge Energy Harvesting Interface Circuits & Systems”, “Wireless Transceivers Towards Next G” and “Circuits and Packaging Techniques for Next-gen Wireline Communications”. In addition, we offer 4 Panel Sessions, including “Cognitive Connections: Exploring Brain-Computer-Interfaces through Systems and Experiments”, “Will open source design be the future direction?”, “Can Academia Effectively Participate in Heterogeneous Integration Research and How?” and “How can LLMs help hardware design and will it replace digital design roles in the years to come?”.

Moreover, we will hold exciting social events that include the Welcome Reception on Monday evening, SSCS Young Professionals and Women in Circuits Mentoring Event on Tuesday afternoon followed by the Conference Reception. The conference will close strong on Wednesday with the Best Paper Poster Session, and the Closing Ceremony where this year’s outstanding paper winners will be announced.

Finally, the CICC Chairs and Steering Committee would like to extend their sincere thanks to the authors and the Technical Program Committee members for their hard work in writing and reviewing the papers and oral presentations. Your tireless efforts are essential to the success of CICC 2024 and are greatly appreciated. Please kindly join us at the conference in Denver this year!

Nan Sun
Technical Program Committee Chair
2024 IEEE Custom Integrated Circuits Conference

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2024 Program-at-a-Glance

Denver, Colorado, USA (Mountain Daylight Time (MDT)

Sunday, April 21, 2024

****All Sunday sessions are included with conference registration****

Crystal Ballroom I	*Crystal Ballroom II*	*Crystal Ballroom III*	*Colorado Ballroom II/III*
9:00 am-4:45 pm *(12:15 pm-1:30 pm break)* **Educational Session 1:** Deep Learning and Compute-in-Memory Designs and Applications	9:00 am-4:45 pm *(12:15 pm-1:30 pm break)* **Educational Session 2:** Introduction to Quantum Computing for Circuit Designers	9:00 am-4:45 pm *(12:15 pm-1:30 pm break)* **Educational Session 3:** Optical and Wireline Communication Circuit Techniques	9:00 am-4:45 pm *(12:15 pm-3:15 pm break)* **Educational Session 4:** Nascent Sensing Devices and Interfaces

Monday, April 22, 2024

8:00 am-8:20 am
Welcome and Opening Remarks
Grand Ballroom I/II

8:20 am-9:10 am
Session 1: Keynote Session
Grand Ballroom I/II

9:10 am-9:30 am BREAK
Grand Ballroom Foyer

Grand Ballroom I/II	*Crystal Ballroom I*	*Crystal Ballroom II*	*Crystal Ballroom III*	*Colorado Ballroom II/III*	*Grand Ballroom IV*
9:30 am-11:00 am **Session 2:** Panel: Cognitive Connections: Exploring Brain-Computer-Interfaces through Systems and Experiments	9:30 am-11:30 am **Session 3:** Forum: AI-based Chip/Chiplet Generation	9:30 am-11:30 am **Session 4:** Forum: Cutting-edge Energy Harvesting Interface Circuits & Systems	9:30 am-11:40 am **Session 5:** Advances in RF/mmWave Wireless Transceivers	9:30 am-11:00 am **Session 6:** Panel: Will open source design be the future direction?	9:30 am-11:35am A-SSCC Best Student Papers
11:40 am-1:00 pm LUNCH BREAK (on own)					
1:00 pm-4:15 pm *(2:45 pm-3:00 pm break)* **Session 7:** Mixed-Signal Compute in Memory	1:00 pm-2:45 pm **Session 8:** Emerging Systems and Integration Techniques 3:00 pm-4:30 pm **Session 8b:** Panel: Can Academia Effectively Participate in Heterogeneous Integration Research and How?	1:00 pm-4:40 pm *(2:45 pm-3:00 pm break)* **Session 9:** Power Management Techniques	1:00 pm-4:40 pm *(2:45 pm-3:00 pm break)* **Session 10:** mmWave and THz Circuits and Systems	1:00 pm-4:15 pm *(2:45 pm-3:00 pm break)* **Session 11:** Emerging Computing Technologies and Applications	1:00 pm-2:45 pm **Session 12:** High-voltage and Dynamic Comparators 3:00 pm-5:10 pm **Session 13:** Analog Sensor Interfaces

5:30 pm-7:30 pm
Welcome Reception
Grand Ballroom III

7:30 pm CICC 2024 Brewery Night
CICC will cover the first round of beer for the first 150 attendees @ Station 26 Brewery

2024 Program-at-a-Glance

Denver, Colorado, USA (Mountain Daylight Time (MDT)

Tuesday, April 23, 2024				
Grand Ballroom I/II	***Crystal Ballroom I***	***Crystal Ballroom II***	***Crystal Ballroom III***	***Colorado Ballroom II/III***
8:00 am-11:15 am *(9:45 am-10:00 am break)* **Session 14:** Domain-Specific Accelerators	8:00 am-11:15 am *(9:45 am-10:00 am break)* **Session 15:** Innovations in Sensing, Communication, and Imaging Technologies	8:00 am-11:40 am *(9:45 am-10:00 am break)* **Session 16:** Energy Harvesting and Isolated Power Conversion	8:00 am-11:15 am *(9:45 am-10:00 am break)* **Session 17:** RF/mm-Wave VCO and Phase Locked Loops	8:00 am-11:40 am *(9:45 am-10:00 am break)* **Session 18:** Power Efficient and Application-Oriented ADCs
12:00 pm-1:30 pm **Session 19:** Keynote Luncheon Session (Registration required) *Grand Ballroom III*				
1:45 pm-5:00 pm *(3:30 pm-3:45 pm break)* **Session 20:** Digital Circuit Techniques	1:45 pm-5:25 pm *(3:30 pm-3:45 pm break)* **Session 21:** Machine Learning and Vision Processing Systems	1:45 pm-5:25 pm *(3:30 pm-3:45 pm break)* **Session 22:** DC-DC Converters	1:45 pm-5:00 pm *(3:30 pm-3:45 pm break)* **Session 23:** Wireline Transceivers and Clocking Techniques	1:45 pm-5:25 pm *(3:30 pm-3:45 pm break)* **Session 24:** High-Resolution ADCs
4:30 pm-6:00 pm **IEEE SSCS Young Professionals and Women in Circuits Mentoring Event** *Characters Bar (next to Colorado Ballroom)*				
5:30 pm-7:30 pm **CICC Conference Reception** *Grand Ballroom IV*				
Wednesday, April 24, 2024				
8:00 am-8:50 am **Session 25:** Keynote Session *Grand Ballroom I/II*				
8:50 am-9:10 am BREAK				
Grand Ballroom I/II	***Crystal Ballroom I***	***Crystal Ballroom II***	***Crystal Ballroom III***	***Colorado Ballroom II/III***
9:10 am-11:35 am *(10:30 am-10:45 am break)* **Session 26:** Digital Compute in Memory	9:10 am-12:25 pm *(10:30 am-10:45 am break)* **Session 27:** Advanced Neural Interfaces	9:10 am-12:25 pm *(10:30 am-10:45 am break)* **Session 28:** High-Speed Data Converters	9:10 am-10:55 am **Session 29:** Energy-efficient Radios for IoT and Emerging Systems	9:10 am-12:25 pm *(10:30 am-10:45 am break)* **Session 30:** Optical Transceivers and Building Blocks
12:25 pm- 1:45 pm LUNCH BREAK (on own)				
1:45 pm-3:15 pm **Session 31:** Panel: How can LLMs help hardware design and will it replace digital design roles in the years to come?	1:45 pm-3:30 pm **Session 32:** Emerging Systems and Integration Techniques (Part 2)	1:45 pm-3:05 pm **Session 33:** Timing References	1:45 pm-3:50 pm **Session 34:** Forum: Wireless Transceivers Towards Next G	1:45 pm-3:50 pm **Session 35:** Forum: Circuits and Packaging Techniques for Next-gen Wireline Communications
3:45 pm-4:00 pm BREAK *Grand Ballroom Foyer*				
4:00 pm-5:00 pm **Best Paper Poster Session & Closing/Awards Ceremony –** *Grand Ballroom I/II*				

Sunday, 21 April

9am — **Educational Session 1: Deep Learning and Compute-in-Memory Designs and Applications**
Crystal Ballroom I
Chaired by: Prof. Weiwei Shan (China) and Prof. Yongpan Liu (China)

9am — **ES1-1: Fundamentals of In-memory Computing**
» Prof. Naresh Shanbhag (United States)[1] (1. University of Illinois at Urbana-Champaign)

10:45am — **ES1-2: Circuit and Architectural Challenges for Analog In-Memory Compute**
» Dr. Pritish Narayanan (United States)[1] (1. IBM Research - Almaden)

9am — **Educational Session 2: Introduction to Quantum Computing for Circuit Designers**
Crystal Ballroom II
Chaired by: Siddharth Joshi (United States)

9am — **ES2-1: Ising Machine: An Intersection of Quantum and Classical Annealing**
» Prof. Ali Sheikholeslami (Canada)[1] (1. University of Toronto)

10:45am — **ES2-2: Introduction to Quantum Computing: from Algorithm to Hardware**
» Prof. Hiu Yung Wong (United States)[1] (1. San Jose State University)

9am — **Educational Session 3: Optical and Wireline Communication Circuit Techniques**
Crystal Ballroom III
Chaired by: Sudipto Chakraborty (United States) and Prof. Armin Tajalli (United States)

9am — **ES3-1: Transceiver Architectures for Future System Interconnect Demands**
» Dr. Samuel Palermo (United States)[1] (1. Texas A&M University)

10:45am — **ES3-2: The Latest High Speed Wireline SerDes Technology**
» Dr. Cathy Liu (United States)[1] (1. Broadcom)

9am — **Educational Session 4: Nascent Sensing Devices and Interfaces**
Colorado Ballroom II/III
Chaired by: Prof. Constantine Sideris (United States) and Prof. Kyeongha Kwon (Korea, Republic of)

9am — **ES4-1: Capacitance-to-Digital Converters (CDCs), Interfacing with Capacitive Sensors**
» Prof. Minkyu Je (Korea, Republic of)[1] (1. Korea Advanced Institute of Science and Technology)

10:45am — **ES4-2: Micro- and Nanoscale Electro-fluidics: From Basic Research to Translational Medicine**
» Prof. Mehdi Javanmard (United States)[1] (1. Rutgers University)

12:15pm — **Break**
Grand Ballroom Foyer

1:30pm — **Educational Session 1: Deep Learning and Compute-in-Memory Designs and Applications**
Crystal Ballroom I
Chaired by: Prof. Weiwei Shan (China) and Prof. Yongpan Liu (China)

1:30pm — **ES1-3: SRAM-based In-Memory Computing Hardware: Analog vs Digital and Macros to Microprocessors**
» Prof. Mingoo Seok (United States)[1] (1. Columbia University)

3:15pm — **ES1-4: Architecture and System Integration of In-memory Computing: Programmability, Scalability and Functionality beyond Matrix Multiplication**
» Dr. Hongyang Jia (China)[1] (1. Tsinghua University)

1:30pm — **Educational Session 2: Introduction to Quantum Computing for Circuit Designers**
Crystal Ballroom II
Chaired by: Siddharth Joshi (United States)

Continued from **Sunday, 21 April**

1:30pm **ES2-3: Principles and Cryo-CMOS Control of Spin Qubit based Quantum Computers**
» Dr. Sushil Subramanian (United States)[1] (1. Intel)

3:15pm **ES2-4: Cryo-CMOS Quantum-Classical Interfaces to Quantum Processors: from a Wild Idea to Working Silicon**
» Dr. Sudipto Chakraborty (United States)[1] (1. IBM)

1:30pm **Educational Session 3: Optical and Wireline Communication Circuit Techniques**
Crystal Ballroom III
Chaired by: Prof. Armin Tajalli (United States) and Sudipto Chakraborty (United States)

1:30pm **ES3-3: Design of Silicon photonics based high throughput optical transceivers.**
» Dr. Mayank Raj (United States)[1] (1. AMD)

3:15pm **ES3-4: Interconnect for the chiplet era: circuit techniques and standards**
» Mr. Gerald Pasdast (United States)[1] (1. Intel)

3:15pm **Educational Session 4: Nascent Sensing Devices and Interfaces**
Colorado Ballroom II/III
Chaired by: Prof. Constantine Sideris (United States) and Ulkuhan Guler (United States)

3:15pm **ES4-3: Highly Power-Scalable Circuits for Purely-Harvested Sensing Systems down Well Below Leakage**
» Prof. Massimo Alioto (Singapore)[1] (1. National University of Singapore)

Monday, 22 April

8am **Welcome and Opening Remarks**
Grand Ballroom I/II

8:20am **Session 1: Keynote Session**
Grand Ballroom I/II

8:20am **Semiconductor in Artificial Intelligence Era**
» Dr. Tsung-Yung Jonathan Chang (Taiwan)[1] (1. TSMC)

9:10am **Break**
Grand Ballroom Foyer

9:30am **Emerging Technologies, Systems, and Applications IV - Session 2: Panel: Cognitive Connections: Exploring Brain-Computer-Interfaces through Systems and Experiments**
Grand Ballroom I/II
Chaired by: Sungwon Chung (United States) and Chul Kim (Korea, Republic of)

9:30am **Foundation of System Design I - Session 3: Forum: AI-based Chip/Chiplet Generation**
Crystal Ballroom I
Chaired by: Xinfei Guo (China) and Siddharth Joshi (United States)

9:30am **3-1: From Quips to Chips: Leveraging LLMs for Microelectronics Design and Specification**
» Prof. Siddharth Garg (United States)[1] (1. Department of Electrical and Computer Engineering, New York University)

10am **3-2: ChipNeMo: Domain-adapted LLMs for Chip Design**
» Dr. Haoxing (Mark) Ren (United States)[1] (1. Nvidia)

Continued from **Monday, 22 April**

10:30am **3-3: AI for Chip Design:When, Where, and How?**
» Prof. David Pan (United States)[1] (1. The University of Texas at Austin)

11am **3-4: How ML can improve digital and analog design**
» Prof. Sachin Sapatnekar (United States)[1] (1. University of Minnesota, Twin Cities)

9:30am **Power Management I -**
Session 4: Forum: Cutting-edge Energy Harvesting Interface Circuits & Systems
Crystal Ballroom II
Chaired by: Prof. Hyun-Sik Kim (Korea, Republic of) and Inhee Lee (United States)

9:30am **4-1: Efficient and Low-cost Kinetic Energy Harvesting: Review & Recent Progress**
» Prof. Sijun Du (Netherlands)[1] (1. Delft University of Technology)

10am **4-2: Advances in Energy Harvesters and Ultra-Low Power Circuits Towards Edge Computing**
» Dr. Joey Sankman (United States)[1] (1. Analog Devices (USA))

10:30am **4-3: Multi-source Energy Harvesting Integrated Circuit for Battery-free IoT Devices**
» Prof. Po-Hung Chen (Taiwan)[1] (1. National Yang Ming Chiao Tung University)

11am **4-4: Recent Developments in Interface Circuits for Piezoelectric Energy Harvesting**
» Prof. Ping-Hsuan Hsieh (Taiwan)[1] (1. National Tsing Hua University)

9:30am **Wireless Transceivers and RF/mm-Wave Circuits and Systems I -**
Session 5: Advances in RF/mmWave Wireless Transceivers
Crystal Ballroom III
Chaired by: Prof. Mustafijur Rahman (India) and Taiyun Chi (United States)

9:30am **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

9:35am **5-1: (INVITED) Interferer-Tolerant RX Front-End Architectures**
» Dr. Danilo Manstretta (Italy)[1] (1. University Of Pavia)

10:25am **5-2: A Beamforming Receiver Using a Time-Modulated LO-Path Vector Modulator Achieving Amplitude and Phase Control with 0.2 dB RMS Gain Error and 1.4 Degree RMS Phase Error**
» Mr. Petar Barac (United States)[1], Dr. Matthew Bajor (United States)[1], Dr. Tanbir Haque (United States)[1], Prof. Peter Kinget (United States)[1] (1. Columbia University)

10:50am **5-3: A 4x4 5-6GHz CMOS Wi-Fi Transceiver Front-End for Fiber-to-the-Room with Analog Beamforming Achieving 27dBm 1024 QAM MCS11 EIRP and -45dB EVM Floor**
» Mr. Xin Lei (China)[1], Mr. Xinhao Zheng (China)[1], Ms. Yiqian Nie (China)[1], Ms. Xinke Huang (China)[1], Mr. Kun Fu (China)[1], Mr. Yukun He (China)[1], Prof. Xiaoyan Gui (China)[1] (1. Xi'an Jiaotong University)

11:15am **5-4: A -10.1dBm IIP3, 0.3-40GHz Receiver Using Hybrid-Path Band-Selection with Reduced LO Coverage Bandwidth Supporting 480Mb/s 4096-QAM and 7.2Gb/s 64-QAM Modulation**
» Mr. Changxuan Han (China)[1], Prof. Xun Luo (China)[1] (1. University of Electronic Science and Technology of China (UESTC))

9:30am **Data Converters I -**
Session 6: Panel: Will open source design be the future direction?
Colorado Ballroom II/III
Chaired by: Seung-tak Ryu (Korea, Republic of) and Jie Gu (United States)

9:30am **A-SSCC Best Student Papers**
Grand Ballroom IV
Chaired by: Prof. Drew Hall (United States) and Dr. Sudipto Chakraborty (United States)

Continued from **Monday, 22 April**

9:30am **A 25kHz-BW 97.4dB-SNDR 100.2dB-DR 3rd-Order SAR-Assisted CT DSM with 1-0 Mash and DNC**
» Mr. Kent Edrian Lozada (Korea, Republic of)[1] (1. Korea Advanced Institute of Science and Technology (KAIST))

9:55am **SESOMP: a Scalable and Energy-Efficient Self-Organizing Map Processor with Computing-In-Memory and Dead Neuron Pruning**
» Mr. Zehao Li (Singapore)[1] (1. Nanyang Technological University)

10:20am **An 890uW Multichannel Injection-Locked OOK Transmitter with 23% Global Efficiency and 22 pJ/Bit Energy Efficiency**
» Mr. Zhi-Wei Lin (Taiwan)[1] (1. National Cheng Kung University)

10:45am **An Adaptive-Sampling Digital LDO with Statistical Comparator Selection Achieving 99.99% Maximum Current Efficiency and 0.25ps FoM in 65nm**
» Mr. Shun Yamaguchi (Japan)[1] (1. Kyoto University)

11:10am **A Wideband Low-Noise Linear Lidar Analog Front-End Achieving 1.6 GHz bandwidth, 2.7 pA/Hz0.5 Input Referred Noise, and 103 dBW Transimpedance Gain**
» Mr. Xinyu Shen (China)[1] (1. Chinese Academy of Sciences)

11:30am **Lunch Break (on own)**

1pm **Digital Circuits, SoCs, and Systems II -**
Session 7: Mixed-Signal Compute in Memory
Grand Ballroom I/II
Chaired by: Gregory Chen (United States) and Prof. Shreyas Sen (United States)

1pm **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

1:05pm **7-1: MixCIM: A Hybrid-Cell-Based Computing-in-Memory Macro with Less-Data-Movement and Activation-Memory-Reuse for Depthwise Separable Neural Networks**
» Mr. Xin Qiao (China)[1], Dr. Jiahao Song (China)[1], Mr. Youming Yang (China)[1], Mr. Renjie Wei (China)[1], Prof. Xiyuan Tang (China)[1], Prof. Meng Li (China)[1], Prof. Runsheng Wang (China)[1], Prof. Yuan Wang (China)[1] (1. Peking University)

1:30pm **7-2: A 28nm 8928Kb/mm2-weight-density hybrid SRAM/ROM Compute-in-Memory architecture reducing >95% weight loading from DRAM**
» Mr. Guodong Yin (China)[1], Mr. Yiming Chen (China)[1], Mr. Mingyen Lee (China)[1], Mr. Xirui Du (China)[1], Ms. Yue Ke (China)[1], Mr. Wenjun Tang (China)[1], Mr. Zhonghao Chen (China)[1], Mr. Mufeng Zhou (China)[1], Prof. Jinshan Yue (China)[2], Prof. Huazhong Yang (China)[1], Prof. Hongyang Jia (China)[1], Prof. Yongpan Liu (China)[1], Prof. Xueqing Li (China)[1] (1. Tsinghua University, 2. Institute of Microelectronics of the Chinese Academy of Sciences)

1:55pm **7-3: A 10T-2C Capacitive SRAM-based Computing-In-Memory Macro with Array-Embedded DAC and Shift-and-Add Functions**
» Mr. Eunhwan Kim (Korea, Republic of)[1], Mr. Hyunmyung Oh (Korea, Republic of)[1], Mr. Jehun Lee (Korea, Republic of)[2], Mr. Jihoon Park (Korea, Republic of)[2], Ms. Myeongeun Kwon (Korea, Republic of)[2], Prof. Jae-Joon Kim (Korea, Republic of)[2] (1. Pohang University of Science and Technology (POSTECH), 2. Seoul National University)

2:20pm **7-4: (Best Student Paper Candidate) A 28nm 16kb Aggregation and Combination Computing-in-Memory Macro with Dual-level Sparsity Modulation and Sparse-Tracking ADCs for GCNs**
» Mr. Zhaoyang Zhang (China)[1], Mr. Zhichao Liu (China)[1], Ms. Feiran Liu (China)[1], Mr. Yinhai Gao (China)[1], Mr. Yuchen Ma (China)[1], Ms. Yutong Zhang (China)[1], Mr. Tianzhu Xiong (China)[1], Mr. Jinwu Chen (China)[1], Mr. An Guo (China)[1], Mr. Xi Chen (China)[1], Mr. Bo Wang (China)[1], Mr. Yuchen Tang (China)[1], Ms. Xingyu Pu (China)[1], Mr. Xing Wang (China)[1], Prof. Jun Yang (China)[1], Prof. Xin Si (China)[1] (1. Southeast University)

1pm **Foundation of System Design II -**
Session 8: Emerging Systems and Integration Techniques
Crystal Ballroom I
Chaired by: Zhengya Zhang (United States) and Farhana Sheikh (United States)

Continued from **Monday, 22 April**

1pm **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

1:05pm **8-1: (INVITED) Silicon Photonics Chip I/O for Ultra High-Bandwidth and Energy-Efficient Die-to-Die Connectivity**
» Dr. Yuyang Wang (United States)[1], Mr. Songli Wang (United States)[1], Mr. Robert Parsons (United States)[1], Dr. Asher Novick (United States)[1], Mr. Vignesh Gopal (United States)[1], Mr. Kaylx Jang (United States)[1], Dr. Anthony Rizzo (United States)[2], Dr. Chia-Pin Chiu (United States)[3], Dr. Kaveh Hosseini (United States)[3], Dr. Tim Tri Hoang (United States)[3], Dr. Sergey Shumarayev (United States)[3], Prof. Keren Bergman (United States)[1] (1. Columbia University, 2. Air Force Research Laboratory, 3. Intel Corporation)

1:55pm **8-2: (INVITED) Leveraging Micro-Bump Pitch Scaling to Accelerate Interposer Link Bandwidths for Future High-Performance Compute Applications**
» Dr. Walker Turner (United States)[1] (1. Nvidia)

1pm **Power Management II -**
Session 9: Power Management Techniques
Crystal Ballroom II
Chaired by: Sriharsh Pakala (United States) and Alan Roth (United States)

1pm **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

1:05pm **9-1: A Pseudo-Adiabatic Switched-Capacitor Gate Driver for Si and GaN FETs Achieving >5x Power Reduction**
» Mr. Yanqiao Li (United States)[1], Dr. Ziyu Xia (United States)[2], Prof. Jason Stauth (United States)[1] (1. Dartmouth College, 2. Apple)

1:30pm **9-2: A 3-Phase Resonant Current-Mode Wireless Power Receiver with Residual-Free Energy Delivery and Digital-Assisted ZVS Achieving 94.5% Efficiency**
» Mr. Tianqi Lu (Netherlands)[1], Prof. Sijun Du (Netherlands)[1] (1. Delft University of Technology)

1:55pm **9-3: A 7V/µs-DVS Class-G Digital-Shunt-Aided Buck Voltage Regulator Achieving a 7% Dynamic-Efficiency Drop at a 600kHz DVS Occurrence Frequency in 28nm CMOS**
» Dr. Hong-Hyun Bae (Korea, Republic of)[1], Dr. Jeong-Hyun Cho (Korea, Republic of)[1], Mr. Kihyun Kim (Korea, Republic of)[1], Mr. Seunghwa Shin (Korea, Republic of)[1], Dr. Doojin Jang (Korea, Republic of)[2], Dr. Jun-Hyeok Yang (Korea, Republic of)[2], Prof. Hyun-Sik Kim (Korea, Republic of)[1] (1. KAIST, 2. Samsung Electronics)

2:20pm **9-4: A Quad-Output Hybrid Buck Converter with 8-Inductor Helping One Spot from All Quarters for Multi-Core XPUs**
» Dr. Xiangyu Mao (Macao)[1], Mr. Junwei Huang (Macao)[1], Mr. Zhiguo Tong (Macao)[1], Prof. R. P. Martins (Macao)[1], Prof. Yan Lu (Macao)[1] (1. University Of Macau)

1pm **Wireless Transceivers and RF/mm-Wave Circuits and Systems II -**
Session 10: mmWave and THz Circuits and Systems
Crystal Ballroom III
Chaired by: Ritesh Bhat (United States) and Prof. Vadim Issakov (Germany)

1pm **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

1:05pm **10-1: (INVITED) The Pursuit of Practical Applications of THz CMOS Chips**
» Prof. Ruonan Han (United States)[1] (1. Massachusetts Institute of Technology)

1:55pm **10-2: A 334-to-348-GHz 7×2 Radiator Array with Coupled-Line-Based Mode-Decoupling Harmonic Enhancement and Chip-to-Waveguide Interface Achieving 30-dBm EIRP**
» Mr. Meng Yang (China)[1], Mr. Changwenquan Song (China)[1], Prof. Liang Wu (China)[1] (1. The Chinese University of Hong Kong, Shenzhen, China)

Continued from **Monday, 22 April**

2:20pm

10-3: A Mm-Wave Phase-Time Co-Apertured Transceiver Array with Beam Squinting Mitigation for Wideband Beamforming/Spatial-Nulling

» Mr. Mohamed Eleraky (Switzerland)[1], Dr. Jeongsoo Park (Switzerland)[1], Mr. Basem Abdelaziz Abdelmagid (Switzerland)[1], Dr. Naga Sasikanth Mannem (United States)[2], Prof. Hua Wang (Switzerland)[1] (1. ETH Zürich, 2. Georgia Institute Of Technology)

1pm

Emerging Technologies, Systems, and Applications I - Session 11: Emerging Computing Technologies and Applications

Colorado Ballroom II/III

Chaired by: Shih-Chii Liu (Switzerland) and Dr. Kaiyuan Yang (United States)

1pm

Session Introduction

» Mx. Session Chair (United States)[1] (1. CICC)

1:05pm

11-1: (Best Invited Paper Candidate) Intelligent Neural Interfaces: An Emerging Era in Neurotechnology

» Prof. Mahsa Shoaran (Switzerland)[1], Mr. Uisub Shin (Switzerland)[2], Mr. MohammadAli Shaeri (Switzerland)[1] (1. EPFL, 2. EPFL & Cornell University)

1:55pm

11-2: A Neuron-Inspired 0.0032mm2-1.38μW/Ch Wireless Implantable Neural Interface with Direct Multiplexing Front-End and Event-Driven Spike Detection and Transmission

» Mr. Jinbo Chen (China)[1], Mr. Hui Wu (China)[1], Ms. Razieh Eskandari (China)[1], Mr. Xing Liu (China)[1], Ms. Siyu Lin (China)[1], Mr. Qiming Hou (China)[1], Mr. Fengshi Tian (Hong Kong)[2], Mr. Wenjun Zou (China)[1], Dr. Jie Yang (China)[1], Prof. Mohamad Sawan (China)[1] (1. Westlake University, 2. HKUST)

2:20pm

11-3: A Closed-loop Brain-Machine Interface SoC Featuring a 0.2μJ/class Multiplexer Based Neural Network

» Mr. Chao Zhang (China)[1], Mr. Yongxiang Guo (China)[1], Mr. Dawid Sheng (China)[1], Dr. Zhixiong Ma (China)[2], Mr. Chao Sun (China)[3], Mr. Yuwei Zhang (China)[3], Mr. Wenxin Zhao (China)[1], Ms. Fenyan Zhang (China)[2], Prof. Tongfei Wang (China)[2], Prof. Xing Sheng (China)[1], Prof. Milin Zhang (China)[1] (1. Tsinghua University, 2. Chinese Institute for Brain Research, Beijing, 3. Beijing Ningju Technology)

1pm

Analog Circuits and Techniques I - Session 12: High-voltage and Dynamic Comparators

Grand Ballroom IV

Chaired by: Devrim Aksin (United States) and Kailiang Chen (China)

1pm

Session Introduction

» Mx. Session Chair (United States)[1] (1. CICC)

1:05pm

12-1: (INVITED) Circuit Design Techniques for High-Voltage Comparators and Amplifiers

» Dr. Gonenc Berkol (Turkey)[1], Mr. Matt Whitney (United States)[1] (1. Analog Devices)

1:55pm

12-2: A 134-μW 50-MHz Quasi-Dynamic Comparator with A Novel Clock-Free Regenerative Latch

» Mr. Sun-Yang Tay (Singapore)[1], Dr. Victor Adrian (Singapore)[1], Ms. Rouli Fang (Singapore)[1], Mr. Yanshan Xie (Singapore)[1], Prof. Joseph Sylvester Chang (Singapore)[1] (1. Nanyang Technological University)

2:20pm

12-3: A 0.25pJ/Comparison, 27.3μV Input Noise Dynamic Comparator Exploiting Stacked Floating Preamplifier with Cross-Coupled Feedback Inverters in 180nm CMOS

» Dr. Jiangchao Wu (Macao)[1], Mrs. Ke Hu (Macao)[1], Mr. Xuanlin Chen (Macao)[1], Prof. Pui In Mak (Macao)[1], Prof. R. P. Martins (Macao)[1], Prof. Man Kay Law (Macao)[1], Mr. Guangshu Zhao (Chad)[2] (1. University Of Macau, 2. University Of Toronto)

2:45pm

Break

Grand Ballroom Foyer

Continued from **Monday, 22 April**

3pm **Digital Circuits, SoCs, and Systems II cont'd -**
Session 7: Mixed-Signal Compute in Memory
Grand Ballroom I/II
Chaired by: Gregory Chen (United States) and Prof. Shreyas Sen (United States)

3pm **7-5: A 28nm 314.6TLFOPS/W Reconfigurable Floating-Point Analog Compute-In-Memory Macro with Exponent Approximation and Two-Stage Sharing TD-ADC**
» Mr. Pengyu He (Macao)[1], Dr. Yuanzhe Zhao (Macao)[1], Mr. Heng Xie (Macao)[1], Dr. Yang Wang (China)[2], Prof. Shouyi Yin (China)[2], Dr. Li Li (Macao)[1], Prof. Yan Zhu (Macao)[1], Prof. R. P. Martins (Macao)[1], Prof. Chi-Hang Chan (Macao)[1], Prof. Minglei Zhang (Macao)[1] (1. University Of Macau, 2. Tsinghua University)

3:25pm **7-6: A 131TOPS/W 8b ACIM Exploiting Weight-Embedded Auto-Accumulation and Supporting Symmetric Quantization Networks**
» Mr. Wei He (China)[1], Mr. Puyi Bai (China)[1], Mr. Hongyang Luo (China)[1], Mr. Zhenghao Jin (China)[1], Ms. Han Wu (China)[1], Mr. Junyi Zhang (China)[1], Mr. Xingchen Chao (China)[1], Mr. Haiqi Liu (China)[2], Prof. Yajuan He (China)[1], Prof. Qiang Li (China)[1] (1. University Of Electronic Science And Technology Of China, 2. HiSilicon Technologies)

3:50pm **7-7: A 28nm 157TOPS/W 446.9Kb/mm² Compute-In-Memory SRAM Macro with Analog-Digital Hybrid Computing for Deep Neural Network Inference**
» Mr. Sangsu Jeong (Korea, Republic of)[1], Mr. Juyoung Oh (Korea, Republic of)[1], Prof. Dongsuk Jeon (Korea, Republic of)[1] (1. Seoul National University)

3pm **Foundation of System Design IV -**
Session 8b: Panel: Can Academia Effectively Participate in Heterogeneous Integration Research and How?
Crystal Ballroom I
Chaired by: Zhengya Zhang (United States) and Farhana Sheikh (United States)

3pm **Power Management II cont'd -**
Session 9: Power Management Techniques
Crystal Ballroom II
Chaired by: Alan Roth (United States) and Sriharsh Pakala (United States)

3pm **9-5: A distributed power supply scheme with dropout voltage in range 6mv-500mv and a low overhead retention mode**
» Mr. Siddharth Saxena (United States)[1], Dr. Sudhir S. Kudva (United States)[1], Mr. Vijay Srinivasan (United States)[1], Dr. Miguel Rodriguez (United States)[1], Mr. Walter Li (United States)[1], Mr. Shalimar Rasheed (United States)[1], Mr. Gaurav Ajwani (United States)[1], Dr. Tezaswi Raja (United States)[1], Mr. Santosh A (United States)[1], Dr. C Thomas Gray (United States)[1] (1. Nvidia)

3:25pm **9-6: (Best Regular Paper Candidate) A Closed-Loop EMI Regulated GaN Power Converter with 500MHz-Sampling-Bandwidth In-Situ EMI Sensing and 9kHz-Resolution Global Excess-Spectrum Modulation**
» Dr. Yingping Chen (China)[1], Mr. Kaiwen Shen (China)[1], Mr. Qing Yuan (China)[1], Prof. Ming Liu (China)[1] (1. Fudan University)

3:50pm **9-7: (Best Invited Paper Candidate) Challenges and Innovations in Fully Integrated DC-DC Converters for IoT and Modern Computing Platforms**
» Mr. Suyang Song (Switzerland)[1], Mr. Alessandro Novello (Switzerland)[1], Prof. Taekwang Jang (Switzerland)[1] (1. ETH Zürich)

3pm **Wireless Transceivers and RF/mm-Wave Circuits and Systems II cont'd -**
Session 10: mmWave and THz Circuits and Systems
Crystal Ballroom III
Chaired by: Prof. Vadim Issakov (Germany) and Ritesh Bhat (United States)

Continued from **Monday, 22 April**

3pm

10-4: A 20Gb/s QPSK Receiver with Mixed-Signal Carrier, Timing, and Data Recovery Using 3-bit ADCs

» Mr. Shunichi Kubo (Japan)[1], Dr. Yuji Gendai (Japan)[1], Mr. Satoshi Miura (Japan)[1], Dr. Shinsuke Hara (Japan)[2], Mr. Satoru Tanoi (Japan)[2], Dr. Akifumi Kasamatsu (Japan)[2], Prof. Shuhei Amakawa (Japan)[3], Prof. Takeshi Yoshida (Japan)[3], Prof. Satoshi Tanaka (Japan)[3], Prof. Minoru Fujishima (Japan)[3] (1. THine Electronics, Inc., 2. National Institute of Information and Communications Technology, 3. Hiroshima University)

3:25pm

10-5: A mm-Wave Blocker-Tolerant Harmonic-Resilient N-Path Mixer-First Receiver with 6.2 dB NF and 5 dBm OOB-B1dB

» Mr. Shimin Huang (United States)[1], Mr. Jamie Ye (United States)[1], Mr. Shahaboddin Ghajari (United States)[1], Dr. Alyosha Molnar (United States)[1] (1. Cornell University)

3:50pm

10-6: A Tri-mode Filtering Power Amplifier for 5G Millimeter-Wave Dual-Side LO Injection Systems with Power-Efficiency Enhancement

» Dr. Weisen Zeng (China)[1], Dr. Li Gao (China)[1], Dr. Hui-Yang Li (China)[1], Dr. Jin-Xu Xu (China)[1], Prof. Hongtao Xu (China)[2], Prof. Xiuyin Zhang (China)[1] (1. South China University of Technology, 2. Fudan University)

4:15pm

10-7: A 32-to-38GHz Variable-Gain Phase Shifter with Impedance-Invariant Vector Modulation Achieving RMS Phase/Amplitude Errors of 0.33°/0.10dB in PS mode and 0.23°/0.08dB in VGA mode

» Mr. Qingzhe Zhang (China)[1], Mr. Yi Lai (China)[1], Prof. Keping Wang (China)[1], Dr. Weisen Zeng (China)[2] (1. Tianjin University, 2. South China University of Technology)

3pm

Emerging Technologies, Systems, and Applications I cont'd - Session 11: Emerging Computing Technologies and Applications

Colorado Ballroom II/III

Chaired by: Dr. Kaiyuan Yang (United States) and Shih-Chii Liu (Switzerland)

3pm

11-4: (Best Student Paper Candidate) Modular Flexible 80-dB-DR Artifact-Resilient EEG Headset with Distributed Pulse-Based Feature Extraction and Multiplier-less Neuromorphic Boosted Seizure Classifier

» Mr. Alireza Dabbaghian (Canada)[1], Prof. Hossein Kassiri (Canada)[1] (1. York University)

3:25pm

11-5: An Analog Neuromorphic On-Chip Training System with IGZO TFT-Based 6T1C 367-State Synaptic Memory Achieving 0.99-R2 Linearity and 10^4-Times Enhanced Retention Time

» Mr. Minil Kang (Korea, Republic of)[1], Mr. Minseong Um (Korea, Republic of)[1], Mr. Jongun Won (Korea, Republic of)[2], Mr. Jaehyeon Kang (Korea, Republic of)[2], Mr. Sangjun Hong (Korea, Republic of)[3], Ms. Narae Han (Korea, Republic of)[2], Dr. Sangwook Kim (Korea, Republic of)[4], Prof. Sangbum Kim (Korea, Republic of)[2], Prof. Hyung-Min Lee (Korea, Republic of)[1] (1. Korea university, 2. Seoul National University, 3. Samsung Electronics, 4. Samsung Advanced Institute of Technology)

3:50pm

11-6: A 7.4μW and 860μm² per channel cryo-CMOS IC for 70-channel frequency-multiplexed μs-readout of semiconductor qubits

» Mr. Quentin Schmidt (France)[1], Mr. Brian Martinez (France)[1], Mr. Thomas Houriez (France)[1], Dr. Baptiste Jadot (France)[1], Dr. Aloysius Jansen (France)[2], Dr. Xavier Jehl (France)[2], Dr. Tristan Meunier (France)[3], Dr. Gaël Pillonnet (France)[1], Mr. Gérard Billiot (France)[1], Dr. Adrien Morel (France)[4], Dr. Yvain Thonnart (France)[5], Dr. Franck Badets (France)[1] (1. Univ. Grenoble Alpes, CEA, Leti, F-38000 Grenoble, France, 2. Univ. Grenoble Alpes, CEA, PHELIQS, F-38000 Grenoble, France, 3. Quobly, F-38000 Grenoble, France; Univ. Grenoble Alpes, CNRS, Institut Neel, F-38000 Grenoble, France, 4. SYMME, Univ. Savoie Mont Blanc, Annecy, France, 5. Univ. Grenoble Alpes, CEA, List, F-38000 Grenoble, France)

3pm

Analog Circuits and Techniques II - Session 13: Analog Sensor Interfaces

Grand Ballroom IV

Chaired by: Mark Oude Alink (Netherlands) and Prof. Linxiao Shen (China)

3pm

Session Introduction

» Mx. Session Chair (United States)[1] (1. CICC)

Continued from **Monday, 22 April**

3:05pm **13-1: (INVITED) Advanced Sensing Systems Exploiting the Integration of Flexible and Large-Area TFTs with Si-CMOS Technology**
» Dr. marco fattori (Netherlands)[1], Mr. Enrico Genco (Netherlands)[1], Dr. Carmine Garripoli (Netherlands)[1], Dr. Mohammad Zulqarnain (Netherlands)[1], Dr. Kris Myny (Belgium)[2], Prof. Eugenio Cantatore (Netherlands)[1] (1. Eindhoven University of Technology, 2. Katholieke Universiteit Leuven)

3:55pm **13-2: A 737nA Always-On MEMS Gyroscope with 5.45ms Start-up Time Using Burst Mode PLL Technique**
» Prof. longjie zhong (China)[1], Mr. Chengyue Li (China)[1], Prof. Shubin liu (China)[1], Mr. Mingsheng Zhong (China)[1], Dr. Xiayu Wang (China)[1], Prof. Zhangming Zhu (China)[1], Dr. Cui Yang (China)[1] (1. Xidian University)

4:20pm **13-3: A 0.64mm2 Sensor Size, 32.5μg/√Hz Noise Floor, High efficiency MEMS Capacitive Accelerometer using High-voltage Pulse Excitation Technique**
» Prof. longjie zhong (China)[1], Mr. Pengpeng Shang (China)[1], Prof. Shubin liu (China)[1], Mr. Wenfei Cao (China)[1], Prof. Lichen Feng (China)[1], Dr. Xiayu Wang (China)[1], Prof. Yuhua Liang (China)[1], Prof. Zhangming Zhu (China)[1] (1. Xidian University)

4:45pm **13-4: A 103.6dB-SNDR 760mVpp-Input-Range 7.8GΩ-Input-Impedance Direct-Digitization Sensor Readout with Pseudo-Differential Transconductors and Dummy DAC**
» Mr. Jianhong Zhou (China)[1], Mr. Yijie Li (China)[1], Mr. Kaiwen Zhou (China)[1], Ms. Yuying Li (China)[1], Ms. Tian Dong (China)[1], Prof. Zhiliang Hong (China)[1], Prof. Jiawei Xu (China)[1] (1. Fudan University)

5:30pm **Welcome Reception**
Grand Ballroom III
Chaired by: Eric Soenen

7:30pm **CICC 2024 will cover the first round of beer for the first 150 attendees! -**
CICC 2024 Brewery Night
Station 26 Brewery

Tuesday, 23 April

8am **Digital Circuits, SoCs, and Systems III - Session 14: Domain-Specific Accelerators**
Grand Ballroom I/II
Chaired by: Shanshan Xie (United States) and Prof. Weiwei Shan (China)

8am **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

8:05am **14-1: A 28nm 128TFLOPS/W Computing-In-Memory Engine Supporting One-Shot Floating-Point NN Inference and On-Device Fine-Tuning for Edge AI**
» Mr. Haikang Diao (China)[1], Mr. Haoyang Luo (China)[1], Dr. Jiahao Song (China)[1], Mr. Bocheng Xu (China)[1], Prof. Runsheng Wang (China)[1], Prof. Yuan Wang (China)[1], Prof. Xiyuan Tang (China)[1] (1. Peking University)

8:30am **14-2: A Mixed-Signal Near-Sensor Convolutional Imager SoC with Charge-Based 4b-Weighted 5-to-84-TOPS/W MAC Operations for Feature Extraction and Region-of-Interest Detection**
» Mr. Martin Lefebvre (Belgium)[1], Prof. David Bol (Belgium)[1] (1. Université catholique de Louvain (UCLouvain))

8:55am **14-3: Quartet: A 22nm 0.09mJ/Inference Digital Compute-in-Memory Versatile AI Accelerator with Heterogeneous Tensor Engines and Off-Chip-Less Dataflow**
» Mr. Yikan Qiu (China)[1], Prof. Yufei Ma (China)[1], Mr. Meng Wu (China)[1], Mr. Yifan Jia (China)[1], Mr. Xinyu Qu (China)[1], Mr. Zecheng Zhou (China)[1], Mr. Jincheng Lou (China)[1], Prof. Tianyu Jia (China)[1], Prof. Le Ye (China)[1], Prof. Ru Huang (China)[1] (1. Peking University)

9:20am **14-4: BEE-SLAM: A 65nm 17.96 TOPS/W 97.55%-Sparse-Activity Hybrid Mixed-Signal/Digital Multi-Agent Neuromorphic SLAM Accelerator for Swarm Robotics**
» Mr. Jaehyun Lee (Korea, Republic of)[1], Mr. Dong-gu Choi (Korea, Republic of)[1], Prof. Minyoung Song (Korea, Republic of)[1], Prof. Gain Kim (Korea, Republic of)[1], Prof. Jong-Hyeok Yoon (Korea, Republic of)[1] (1. DGIST)

Continued from **Tuesday, 23 April**

8am

Emerging Technologies, Systems, and Applications II -
Session 15: Innovations in Sensing, Communication, and Imaging Technologies
Crystal Ballroom I
Chaired by: Prof. Kyeongha Kwon (Korea, Republic of) and Prof. Jiawei Xu (China)

8am

Session Introduction
» Mx. Session Chair (United States)[1] (1. CICC)

8:05am

15-1: A 24.4µW Room Temperature Gas Sensor based on Molecularly Imprinted Polymers Demonstrating SARS-Cov-2 and D-Glucose Aerosol Sensing
» Mr. Ryan Burns (United States)[1], Mr. Austin Wiechmann (United States)[1], Ms. Pardis Sadeghi (United States)[2], Mr. Nader Lobandi (United States)[2], Mr. Nader Fathy (United States)[1], Mr. Rui Huang (United States)[2], Dr. Nian Sun (United States)[2], Dr. Patrick Mercier (United States)[1] (1. University of California San Diego, 2. Northeastern University)

8:30am

15-2: A CMOS-Integrated Color Center Pulse-Sequence Control and Detection System
» Mr. Jinchen Wang (United States)[1], Mr. Isaac Harris (United States)[1], Mr. Xibi Chen (United States)[1], Prof. Dirk Englund (United States)[1], Prof. Ruonan Han (United States)[1] (1. Massachusetts Institute of Technology)

8:55am

15-3: A Co-Integrated Optical Phased Array, Mach-Zehnder Modulator and Mm-Wave Driver for Free-Space Communication
» Mr. Youngin Kim (Switzerland)[1], Mr. Laurenz Kulmer (Switzerland)[1], Mr. Killian Keller (Switzerland)[1], Dr. Jeongsoo Park (Switzerland)[1], Mr. Basem Abdelaziz Abdelmagid (Switzerland)[1], Dr. Kyung-Sik Choi (Switzerland)[1], Mr. Dongwon Lee (Switzerland)[1], Mr. Yuqi Liu (Switzerland)[1], Prof. Juerg Leuthold (Switzerland)[1], Prof. Hua Wang (Switzerland)[1] (1. ETH Zürich)

9:20am

15-4: A 49.8mm2 Fully Integrated, 1.5m Transmission-Range, High-Data-Rate IR-UWB Transmitter for Brain Implants
» Ms. Cong Ding (Switzerland)[1], Mr. Mingxiang Gao (Switzerland)[1], Prof. Anja Skrivervik (Switzerland)[1], Prof. Mahsa Shoaran (Switzerland)[1] (1. EPFL)

8am

Power Management III -
Session 16: Energy Harvesting and Isolated Power Conversion
Crystal Ballroom II
Chaired by: Prof. Cheng Huang (United States) and Inhee Lee (United States)

8am

Session Introduction
» Mx. Session Chair (United States)[1] (1. CICC)

8:05am

16-1: (Best Student Paper Candidate) A 63ns Flipping Time, 93.6% Voltage Flipping Efficiency Auto-Calibrated Ultrasonic Energy Harvesting Interface from -25 to 85oC
» Mr. Guangshu Zhao (China)[1], Mr. Chao Xie (China)[2], Ms. chenxi wang (Macao)[1], Prof. Yang Jiang (Macao)[1], Prof. Milin Zhang (China)[2], Prof. Pui In Mak (Macao)[1], Prof. R. P. Martins (Macao)[1], Prof. Man Kay Law (Macao)[1] (1. University Of Macau, 2. Tsinghua University)

8:30am

16-2: A Single-Stage Bias-Flip Regulating Rectifier with Fully-Digital Fast-MPPT for Piezoelectric Energy Harvesting Achieving 9.3X Power Enhancement and 92.5% End-to-End Efficiency
» Ms. Xinling Yue (Netherlands)[1], Prof. Sijun Du (Netherlands)[1] (1. Delft University of Technology)

8:55am

16-3: A 1.58-nA CEPE-based Hill-climbing MPPT Technique with Compensated Ton Achieving 67.3% Efficiency at 10-nA Iload and > 97% MPPT Efficiency at VCR from 2 to 6
» Mr. Qiujin Chen (Macao)[1], Mr. Tian Xia (Macao)[1], Mr. Tingxu Hu (Macao)[1], Dr. Yuanfei Wang (Macao)[1], Prof. Mo Huang (Macao)[1], Prof. R. P. Martins (Macao)[1], Prof. Yan Lu (Macao)[1] (1. University Of Macau)

Continued from **Tuesday, 23 April**

9:20am **16-4: A 70-V Fully Integrated Dual-SSHC Rectifier for Triboelectric Energy Harvesting with Full-Digital Duty-Cycle-Based MPPT Achieving 598% Power Extraction Enhancement**

» Mr. Wenyu Peng (Netherlands)[1], Ms. Xinling Yue (Netherlands)[1], Prof. Willem van Driel (Netherlands)[1], Prof. Guoqi Zhang (Netherlands)[1], Prof. Sijun Du (Netherlands)[1] (1. Delft University of Technology)

8am **Wireless Transceivers and RF/mm-Wave Circuits and Systems III - Session 17: RF/mm-Wave VCO and Phase Locked Loops**

Crystal Ballroom III

Chaired by: Sudipto Chakraborty (United States) and Hamidreza Agahsi (United States)

8am **Session Introduction**

» Mx. Session Chair (United States)[1] (1. CICC)

8:05am **17-1: A 194.9dBc/Hz FoM and 6.8-to-11.6GHz Quad-Core Dual-Mode Class-F VCO Featuring Wideband Flicker Noise Suppression**

» Mr. Huanyu Ge (China)[1], Prof. Haikun Jia (China)[1], Prof. Wei Deng (China)[1], Mr. Ruichang Ma (China)[1], Prof. Baoyong Chi (China)[1] (1. Tsinghua University)

8:30am **17-2: A 6.0-to-6.9GHz 99fsrms-Jitter Type-II Sampling PLL with Automatic Frequency and Phase Calibration Method Achieving 0.62µs Locking Time in 28nm CMOS**

» Mr. Jian Yang (China)[1], Mr. Tailong Xu (China)[2], Dr. Xi Meng (China)[2], Mr. Zhenghao Li (China)[1], Prof. Jun Yin (Macao)[2], Prof. R. P. Martins (Macao)[2], Prof. Pui-In Mak (Macao)[2], Prof. Quan Pan (China)[1] (1. Southern University of Science and Technology, 2. University Of Macau)

8:55am **17-3: A 66.7fs-Integrated-Jitter Fractional-N Digital PLL Based on a Resistive-Inverse-Constant-Slope DTC**

» Dr. Pietro Salvi (Italy)[1], Dr. Simone Mattia Dartizio (Italy)[1], Dr. Michele Rossoni (Italy)[1], Dr. Francesco Tesolin (Italy)[1], Dr. Giacomo Castoro (Italy)[1], Prof. Andrea Leonardo Lacaita (Italy)[1], Prof. Salvatore Levantino (Italy)[1] (1. Politecnico di Milano)

9:20am **17-4: A 20-24-GHz DPSSPLL with Charge-Domain Bandwidth Optimization Scheme Achieving 61.3-fs RMS Jitter and -253-dB FoMJitter**

» Dr. Li WANG (China)[1], Ms. Zilu Liu (China)[1], Mr. Ruitao MA (China)[1], Prof. C. Patrick Yue (Hong Kong)[2] (1. Hong Kong University of Science and Technology, 2. Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology)

8am **Data Converters II - Session 18: Power Efficient and Application-Oriented ADCs**

Colorado Ballroom II/III

Chaired by: Yong Lim (Korea, Republic of) and Yong Liu (United States)

8am **Session Introduction**

» Mx. Session Chair (United States)[1] (1. CICC)

8:05am **18-1: (INVITED) Energy Efficient ADC Design Techniques**

» Dr. Pieter Harpe (Netherlands)[1] (1. Eindhoven University of Technology)

8:55am **18-2: A 44µW 140dB-DR Hybrid Light-to-Digital Converter with Current-Tracking Dynamic Zoom and Power-Scaling OTA**

» Mr. Chang Yao (China)[1], Mr. Zhen Lu (China)[1], Mr. Liheng Liu (China)[1], Mrs. Yaohua Pan (China)[2], Mr. Wenhui Qin (China)[2], Mr. Shaoyu Ma (China)[2], Mr. Yun Sheng (China)[2], Prof. Zhiliang Hong (China)[1], Prof. Jiawei Xu (China)[1] (1. Fudan University, 2. Novosense Microelectronics)

9:20am **18-3: A 181.8dB FoMs Zoom Capacitance-to-Digital Converter with kT/C Noise Cancellation and Dead Band Operation**

» Mr. Zilong Shen (China)[1], Mr. Jiajun Tang (China)[1], Mr. Haoyang Luo (China)[1], Mr. Zhongyi Wu (China)[1], Mr. Zongnan Wang (China)[1], Prof. Xing Zhang (China)[1], Prof. Xiyuan Tang (China)[1], Prof. Yuan Wang (China)[1] (1. Peking University)

9:45am **Break**

Grand Ballroom Foyer

Continued from **Tuesday, 23 April**

10am **Digital Circuits, SoCs, and Systems III cont'd -**
Session 14: Domain-Specific Accelerators
Grand Ballroom I/II
Chaired by: Prof. Weiwei Shan (China) and Shanshan Xie (United States)

10am **14-5: (INVITED) BioWAP: A Reconfigurable Biomedical AI Processor with Adaptive Processing for Co-Optimized Accuracy and Energy Efficiency**
» Mr. Jiahao Liu (China)[1], Mr. Ziyi Xie (China)[1], Mr. Xu Wang (China)[1], Mr. Xiao Liu (China)[1], Mr. Xiben Jiao (China)[1], Mr. Jiajing Fan (China)[1], Mr. Huajing Qin (China)[1], Mr. Chaozheng Guo (China)[1], Mr. Jianbiao Xiao (China)[1], Prof. Jun Zhou (China)[1] (1. University of Electronic Science and Technology of China (UESTC))

10:50am **14-6: A 0.078 pJ/SOP Unstructured Sparsity-Aware Spiking Attention/Convolution Processor with 3D Compute Array**
» Mr. chaoming fang (China)[1], Mr. Ziyang Shen (China)[1], Dr. Shiqi Zhao (China)[1], Mr. Chuanqing Wang (China)[1], Mr. Fengshi Tian (Hong Kong)[2], Dr. Jie Yang (China)[1], Prof. Mohamad Sawan (China)[1] (1. Westlake University, 2. HKUST)

10am **Emerging Technologies, Systems, and Applications II cont'd -**
Session 15: Innovations in Sensing, Communication, and Imaging Technologies
Crystal Ballroom I
Chaired by: Prof. Jiawei Xu (China) and Prof. Kyeongha Kwon (Korea, Republic of)

10am **15-5: A Mechanically Flexible 32-by-32-Element Pitch-Matched Ultrasound Front-End Transceiver with Two-Stage Beamforming for 3D Imaging**
» Mr. Jagannaath Shiva Letchumanan (United States)[1], Mr. Siddhesh Gandhi (United States)[1], Dr. Heyu Yin (United States)[1], Mr. Aditya Ramkumar (United States)[1], Prof. Kenneth Shepard (United States)[1] (1. Columbia University)

10:25am **15-6: A Wireless Subdural Optical Cortical Interface Device with 768 Co-Packaged Micro-LEDs for Fluorescence Imaging and Optogenetic Stimulation**
» Mr. Yatin Gilhotra (United States)[1], Mr. Henry Overhauser (United States)[1], Dr. Heyu Yin (United States)[1], Dr. Eric Pollmann (United States)[1], Mr. Guy Eichler (United States)[1], Mr. Andrew Cheng (United States)[1], Mr. Taesung Jung (United States)[1], Mr. Nanyu Zeng (United States)[1], Prof. Luca Carloni (United States)[1], Prof. Kenneth Shepard (United States)[1] (1. Columbia University)

10:50am **15-7: A 32×32 Flash LiDAR SPAD Sensor with Up-to-1kfps Motional Target Detection by Threshold-adaptive 2D Dynamic Vision**
» Prof. Zhangcheng Huang (China)[1], Ms. Jingyi Wang (China)[2], Mr. Bu Chen (China)[2], Ms. Hongyang Shang (China)[2], Mr. Jiapei Zheng (China)[2], Mr. Hankun Lv (China)[2], Prof. Chixiao Chen (China)[2], Prof. Qi Liu (China)[2], Prof. Ming Liu (China)[2] (1. Fudan University, 2. Fudan University)

10am **Power Management III cont'd -**
Session 16: Energy Harvesting and Isolated Power Conversion
Crystal Ballroom II
Chaired by: Prof. Cheng Huang (United States) and Inhee Lee (United States)

10am **16-5: A Resonant Synchronized Switch Harvesting Rectifier With Bias-Flip Charge Recycling for Piezoelectric Energy Harvesting Achieving 13.9x Power Enhancement**
» Ms. Xinling Yue (Netherlands)[1], Mr. Yiwei Zou (Netherlands)[1], Prof. Sijun Du (Netherlands)[1] (1. Delft University of Technology)

10:25am **16-6: (Best Regular Paper Candidate) A 73.3% Peak Efficiency Isolated DC-DC Converter with Gap-Time Modulation using Pseudo-Hysteresis Control for -12kV/μs Common-Mode Transient Immunity**
» Dr. Yang Liu (Hong Kong)[1], Mr. Yuan Yao (Hong Kong)[1], Dr. Lin Cheng (China)[2], Dr. Wing-Hung Ki (Hong Kong)[1] (1. Hong Kong University of Science and Technology, 2. University of Science and Technology of China)

Continued from **Tuesday, 23 April**

10:50am **16-7: A 24V-to-20V 6W 73.2%-Peak-Efficiency Isolated DC-DC Converter using a Transformer-Based Supply-Generating Technique**

» Dr. Dongfang Pan (China)[1], Dr. Weiwei Xu (China)[2], Mr. Xiangfeng Wu (China)[1], Mr. Aoyang Li (China)[1], Dr. Lin Cheng (China)[1] (1. University of Science and Technology of China, 2. Hefei CLT Microelectronics Co. Ltd.)

11:15am **16-8: A 2.4-to-240W, 95.04% Peak Efficiency LLC Isolate Converter Controller with Symmetric Pulse-Width Balancing and Fixed-period Hysteresis Burst Control**

» Ms. Hanyu Shi (China)[1], Mr. Mingchao Liang (China)[1], Mrs. Jie Zhu (China)[1], Mr. Zhuang Zhang (China)[1], Dr. Peng Cao (China)[1], Prof. Jiawei Xu (China)[1], Prof. Zhiliang Hong (China)[1] (1. Fudan University)

10am **Wireless Transceivers and RF/mm-Wave Circuits and Systems III cont'd -**

Session 17: RF/mm-Wave VCO and Phase Locked Loops

Crystal Ballroom III

Chaired by: Hamidreza Agahsi (United States) and Sudipto Chakraborty (United States)

10am **17-5: An 11.1-to-14.9GHz Digital-Integral Hybrid-Proportional Fractional-N PLL with an LC DTC Achieving 0.52µs Locking Time and 41.3fs Jitter**

» Mr. Hongzhuo Liu (China)[1], Prof. Wei Deng (China)[1], Prof. Haikun Jia (China)[1], Prof. Baoyong Chi (China)[1] (1. Tsinghua University)

10:25am **17-6: A 6.8-to-14.4GHz Octave-Tuning Fractional-N Charge-Pump PLL with Slide-Dithering-Based Background DTC Nonlinearity Calibration for Near-Integer Fractional Spur Mitigation Achieving 78fs RMS Jitter and -258.6dB FoMT**

» Mr. Zonglin Ye (China)[1], Mr. Xinlin Geng (China)[1], Mr. Zhixiang Shi (China)[1], Mr. Hongyang Zhang (China)[1], Prof. Qian Xie (China)[1], Prof. Zheng Wang (China)[1] (1. University Of Electronic Science And Technology Of China)

10:50am **17-7: A 59.3fs Jitter and -62.1dBc Fractional-Spur Digital PLL Based on a Multi-Edge Power-Gating Phase-Detector**

» Dr. Simone Mattia Dartizio (Italy)[1], Dr. Michele Rossoni (Italy)[1], Dr. Francesco Tesolin (Italy)[1], Dr. Giacomo Castoro (Italy)[1], Prof. Carlo Samori (Italy)[1], Prof. Andrea Leonardo Lacaita (Italy)[1], Prof. Salvatore Levantino (Italy)[1] (1. Politecnico di Milano)

10am **Data Converters II cont'd -**

Session 18: Power Efficient and Application-Oriented ADCs

Colorado Ballroom II/III

Chaired by: Yong Liu (United States) and Yong Lim (Korea, Republic of)

10am **18-4: A 75dB-SNDR 10MHz-BW 2-Channel Time-Interleaved Noise-Shaping SAR ADC Directly Powered by an On-Chip DC-DC Converter**

» Mr. Haoyu Gong (Macao)[1], Dr. Wen-Liang Zeng (Macao)[1], Prof. Mingqiang Guo (Macao)[1], Prof. Chi-Seng Lam (Macao)[1], Mr. Shulin Zhao (Macao)[1], Prof. R. P. Martins (Macao)[1], Prof. Sai-Weng Sin (Macao)[1] (1. University Of Macau)

10:25am **18-5: A 50MHz-BW 168.8dB-FoM 2x Time-interleaved Bandpass Noise Shaping SAR ADC Using Passive Filter**

» Mr. Seungjun Song (Korea, Republic of)[1], Mr. Dongsik Lee (Korea, Republic of)[1], Prof. Hyungil Chae (Korea, Republic of)[1] (1. Konkuk University, Seoul, Korea)

10:50am **18-6: An 80MS/s 70.79dB-SNDR 60.7fJ/conv-step Radiation-Tolerant Semi-Time-interleaved Pipelined-SAR ADC**

» Mr. Zheyi Li (Belgium)[1], Mr. Laurent Berti (Belgium)[1], Dr. Qiuyang Lin (Belgium)[1], Mr. Jinghao Zhao (Belgium)[2], Dr. Maxim Gorbunov (Belgium)[1], Mr. Geert Thys (Belgium)[1], Prof. Paul Leroux (Belgium)[2] (1. IMEC, 2. Katholieke Universiteit Leuven)

11:15am **18-7: A 7.9 ps Resolution, Multi-event TDC Using an Ultra-low Static Phase Error DLL and High Linearity Time Amplifier for dToF Sensors**

» Dr. Xiayu Wang (China)[1], Mr. Zhaoyang Zhou (China)[1], Mr. Chunlin Li (China)[1], Dr. Jin Hu (China)[1], Dr. Dong Li (China)[1], Prof. Rui Ma (China)[1], Prof. Yang Liu (China)[1], Prof. Zhangming Zhu (China)[1] (1. Xidian University)

Continued from **Tuesday, 23 April**

12pm **Session 19: Keynote Luncheon**
Grand Ballroom III

12pm **Integrated Voltage Regulators: from Research to Production**
» Dr. Noah Sturcken (United States)[1] (1. Ferric Semi)

1:45pm **Digital Circuits, SoCs, and Systems IV -**
Session 20: Digital Circuit Techniques
Grand Ballroom I/II
Chaired by: Divya Prasad (United States) and Visvesh Sathe (United States)

1:45pm **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

1:50pm **20-1: (INVITED) Scalable and Interpretable Brain-Inspired Hyper-dimensional Computing Intelligence with Hardware-software Co-design**
» Mr. Hanning Chen (United States)[1], Mr. Yang Ni (United States)[1], Mr. Wenjun Huang (United States)[1], Prof. Mohsen Imani (United States)[1] (1. University of California Irvine)

2:40pm **20-2: An Adaptive Wide-Voltage-Range Droop Detection and Protection System Assisted with Timing Error Detection in 28nm CMOS**
» Mr. Lishuo Deng (China)[1], Mr. Zhengguo Shen (China)[1], Ms. Zhuo Chen (China)[1], Mr. Cai Li (China)[1], Mr. Junyi Qian (China)[1], Mr. Yuxuan Du (China)[1], Mr. Kaize Zhou (China)[1], Mr. Keran Li (China)[1], Mr. Ruidong Li (China)[2], Mr. Tuo Li (China)[2], Mr. Xiaofeng Zou (China)[2], Prof. Weiwei Shan (China)[1] (1. Southeast University, 2. Shandong Yunhai Guochuang Cloud Computing Equipment Industry Innovation Co., Ltd.)

3:05pm **20-3: A 28nm All-Digital Droop Detection and Mitigation Circuit Using A Shared Dual-Mode Delay Line with 14.8% Vmin Reduction and 42.9% Throughput Gain**
» Mr. Minyoung Kang (Korea, Republic of)[1], Mr. Sunghoon Kim (Korea, Republic of)[1], Mr. Youngmin Park (Korea, Republic of)[1], Mr. Sangsu Jeong (Korea, Republic of)[1], Prof. Dongsuk Jeon (Korea, Republic of)[1] (1. Seoul National University)

1:45pm **Foundation of System Design III -**
Session 21: Machine Learning and Vision Processing Systems
Crystal Ballroom I
Chaired by: Zhengya Zhang (United States) and Siddharth Joshi (United States)

1:45pm **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

1:50pm **21-1: (INVITED) Next-Generation Domain-Specific Accelerators: From Hardware to System**
» Dr. Sophia Shao (United States)[1] (1. University of California, Berkeley)

2:40pm **21-2: A 0.59μJ/pixel High-throughput Energy-efficient Neural Volume Rendering Accelerator on FPGA**
» Mr. ZheChen Yuan (China)[1], Mr. Binzhe Yuan (China)[1], Mr. Yuhan Gu (China)[1], Mr. Yueyang Zheng (China)[1], Mr. Yunxiang He (China)[1], Mr. Xuexin Wang (China)[1], Mr. Chaolin Rao (China)[2], Prof. Pingqiang Zhou (China)[1], Prof. Jingyi Yu (China)[1], Prof. Xin Lou (China)[1] (1. ShanghaiTech University, 2. GGU Technology Co., Ltd.)

3:05pm **21-3: A 38.5TOPS/W Point Cloud Neural Network Processor with Virtual Pillar and Quadtree-based Workload Management for Real-Time Outdoor BEV Detection**
» Mr. Sukbin Lim (Korea, Republic of)[1], Mr. Jaehoon Heo (Korea, Republic of)[1], Mr. Jinho Yang (Korea, Republic of)[1], Prof. Joo-Young Kim (Korea, Republic of)[1] (1. KAIST)

Continued from **Tuesday, 23 April**

1:45pm **Power Management IV -**
Session 22: DC-DC Converters
Crystal Ballroom II
Chaired by: Raveesh Magod (United States) and XIAOCHENG JING (United States)

1:45pm **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

1:50pm **22-1: A 97.3%-Peak-Efficiency Always-Dual-Path Buck-Boost Converter with Single-Mode Operation and Fast Transient Responses**
» Mr. Ji Jin (China)[1], Mr. Yufa Zhou (China)[2], Dr. Weiwei Xu (China)[2], Dr. Lin Cheng (China)[1] (1. University of Science and Technology of China, 2. Hefei CLT Microelectronics Co. Ltd.)

2:15pm **22-2(Best Student Candidate)A 96.7%-Efficient 2.5A Scalable DC DC Converter Module with Complementary Dual-Mode Reconfigurable Hybrid Topology Achieving Always Inductor Current Reduction Continuously Adjustable VCR Range and Interleaving COUT Augmentation**
» Ms. Huihua Li (Macao)[1], Mr. Qiaobo Ma (Macao)[1], Prof. Yang Jiang (Macao)[1], Prof. Rui P. Martins (Macao)[1], Prof. Pui In Mak (Macao)[1] (1. University Of Macau)

2:40pm **22-3: A 12V-to-PoL CCC-based Easy-Scalable Multiple-Phase Hybrid Converter with Auto VCF Balancing and Inactive CF Charging**
» Mr. Jiacheng Yang (Macao)[1], Mr. Tingxu Hu (Macao)[1], Prof. Mo Huang (Macao)[1], Prof. R. P. Martins (Macao)[1], Prof. Yan Lu (Macao)[1] (1. University Of Macau)

3:05pm **22-4: A Multi-Phase Multi-Path Hybrid Buck Converter for 9-48V to 0.8-1.2V Conversion with Improved DCR-Loss Reduction and Alleviated CFLY Current Gathering Achieving 88.3% Peak Efficiency and 176A/cm³ Density**
» Mr. Qiaobo Ma (Macao)[1], Ms. Huihua Li (Macao)[1], Mr. Jiahao Shi (Macao)[1], Prof. Yang Jiang (Macao)[1], Prof. Rui P. Martins (Macao)[1], Prof. Pui In Mak (Macao)[1] (1. University Of Macau)

1:45pm **Wireline and Optical Communications Circuits and Systems I -**
Session 23: Wireline Transceivers and Clocking Techniques
Crystal Ballroom III
Chaired by: Prof. Tejasvi Anand (United States) and Xi Chen (United States)

1:45pm **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

1:50pm **23-1: (Best Invited Paper Candidate) Digital-to-Analog Converters for 100+ Gb/s Wireline Transmitters: Architectures, Circuits, and Calibration**
» Dr. Tod Dickson (United States)[1], Ms. Zeynep Deniz (United States)[1], Mr. Martin Cochet (United States)[1], Mr. John Bulzacchelli (United States)[1], Mr. Marcel Kossel (Switzerland)[2], Mr. Pier Andrea Francese (Switzerland)[2], Mr. Thomas Morf (Switzerland)[2], Mr. Herschel Ainspan (United States)[1], Mr. Matthias Brändli (Switzerland)[2], Mr. Mounir Meghelli (United States)[1] (1. IBM T.J. Watson Research Center, 2. IBM Research Zurich)

2:40pm **23-2: (INVITED) Design of 224Gb/s DSP-based transceiver in CMOS technology: signal integrity, architecture, circuits, and packaging**
» Dr. Jihwan Kim (United States)[1], Dr. Ariel Cohen (Israel)[1], Dr. Mike Peng Li (United States)[1], Dr. Ajay Balankutty (United States)[1], Dr. Sandipan Kundu (United States)[1], Dr. Ahmad Khairi (Israel)[1], Mr. Yoel Krupnik (Israel)[1], Mr. Yoav Segal (Israel)[1], Mr. Marco Cusmai (Israel)[1], Mr. Dror Lazar (Israel)[1], Mr. Ari Gordon (Israel)[1], Mr. Noam Familia (Israel)[1], Mr. Kai Yu (United States)[1], Mr. Yutao Liu (United States)[1], Mr. Matthew Beach (United States)[1], Ms. Priya Wali (United States)[1], Dr. Hsinho Wu (United States)[1], Mr. Masashi Shimanouchi (United States)[1], Ms. Jenny Xiaohong Jiang (United States)[1], Dr. Zhiguo Qian (United States)[1], Dr. Kemal Aygun (United States)[1], Mr. Itamar Levin (Israel)[1], Dr. Frank O'Mahony (United States)[1] (1. Intel Corporation)

1:45pm **Data Converters III -**
Session 24: High-Resolution ADCs
Colorado Ballroom II/III
Chaired by: Prof. Shaolan Li (United States) and Prof. Chia-hung Chen (Taiwan)

Continued from **Tuesday, 23 April**

1:45pm **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

1:50pm **24-1: A 16b 5MS/s 93.7dB-SNDR SAR ADC with a Split Sampling Technique and SRM-Assisted Self-Calibration**
» Mr. Qifeng Huang (Hong Kong)[1], Mr. Siji Huang (Hong Kong)[1], Mr. Yanhang Chen (Hong Kong)[1], Mr. Yifei Fan (Hong Kong)[1], Prof. Jie Yuan (Hong Kong)[1] (1. HKUST)

2:15pm **24-2: An 82dB-SNDR Input-Driving-Relaxed Noise-Shaping SAR with Amplifier-Reused In-Loop Buffering and NTF Leakage Reshaping**
» Mr. Tian Xie (United States)[1], Mr. Ken Li (United States)[1], Mr. Tzu-Han Wang (United States)[1], Mr. Wei-En Lee (United States)[1], Mr. Engin Esen (United States)[1], Mr. Dong Suk Kang (United States)[1], Prof. Shaolan Li (United States)[1] (1. Georgia Institute Of Technology)

2:40pm **24-3: A 188.6-µW Continuous-time Incremental Delta-Sigma ADC with Extended Counting achieving 95.2-dB SNDR and 175.4-dB FoMSNDR**
» Mr. Zhaonan Lu (China)[1], Prof. Menglian Zhao (China)[1], Prof. Zhichao Tan (China)[1] (1. Zhejiang University)

3:05pm **24-4: A 470µW 20kHz-BW 107.3dB-SNDR Nested CT DSM Employing Negative-R-based Cross-RC Filter and Weighted Multi-Threshold MSB-Pass Quantizer**
» Dr. Jing Jin (China)[1], Dr. Yuekang Guo (China)[1], Mr. Meng Xu (China)[1], Dr. Xiaoming Liu (China)[1], Prof. Nan Sun (China)[2], Prof. Jianjun Zhou (China)[1] (1. Shanghai Jiao Tong University, 2. Tsinghua University)

3:30pm **Break**
Grand Ballroom Foyer

3:45pm **Digital Circuits, SoCs, and Systems IV cont'd - Session 20: Digital Circuit Techniques**
Grand Ballroom I/II
Chaired by: Visvesh Sathe (United States) and Divya Prasad (United States)

3:45pm **20-4: A 98fJ/Bit Current-Starved-Ring-Oscillator-Based TRNG with High PVT Tolerance and Resilience to Frequency Injection Attack up to 1V**
» Mr. Jiacheng Hao (China)[1], Mr. Qingsen Zhuang (China)[1], Mr. Junhang Zhang (China)[1], Prof. Xiaojin Zhao (China)[1] (1. Shenzhen University)

4:10pm **20-5: A 40nm 1.26µJ/Op Energy-Efficient CRYSTALS-KYBER Post-Quantum Crypto-Processor with Comprehensive Side Channel Security Analysis and Countermeasures**
» Mr. Aobo Li (China)[1], Dr. Jiahao Lu (China)[1], Prof. Dongsheng Liu (China)[1], Mr. Xiang Li (China)[1] (1. Huazhong University of Science and Technology)

4:35pm **20-6: A Secure Digital In-Memory Compute (IMC) Macro with Protections for Side-Channel and Bus Probing Attacks**
» Ms. Maitreyi Ashok (United States)[1], Dr. Saurav Maji (United States)[1], Dr. Xin Zhang (United States)[2], Dr. John Cohn (United States)[3], Prof. Anantha Chandrakasan (United States)[1] (1. Massachusetts Institute of Technology, 2. IBM T.J. Watson Research Center, MIT-IBM Watson AI Lab, 3. MIT-IBM Watson AI Lab)

3:45pm **Foundation of System Design III cont'd - Session 21: Machine Learning and Vision Processing Systems**
Crystal Ballroom I
Chaired by: Siddharth Joshi (United States) and Zhengya Zhang (United States)

3:45pm **21-4: A 28nm 1.2GHz Scalable Vision/Point Cloud Deep Fusion Processor with CAM-based Universal Mapping Unit for BEVFusion Applications**
» Mr. Xiaoyu Feng (China)[1], Mr. Wenyu Sun (China)[1], Mr. Xinyuan Lin (China)[1], Mr. Shupei Fan (China)[1], Prof. Huazhong Yang (China)[1], Prof. Yongpan Liu (China)[1] (1. Tsinghua University)

4:10pm **21-5: A 4.2pJ/Pixel 480 fps Stereo Vision Processor with Pixel Level Pipelined Architecture and Two-path Aggregation Semi-Global Matching**
» Mr. Zehao Li (Singapore)[1], Mr. Yuncheng Lu (Singapore)[1], Dr. Anh Tuan Do (Singapore)[2], Prof. Tony Tae-Hyoung Kim (Singapore)[1] (1. Nanyang Technological University, 2. Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR))

Continued from **Tuesday, 23 April**

4:35pm

21-6: A 29.12 TOPS/W and 1.13 TOPS/mm2 NAS-Optimized Mixed-Precision DNN Accelerator with Vector Split-and-Combination Systolic in 28nm CMOS

» Dr. Kai Li (China)[1], Dr. Hantao Huang (China)[1], Prof. Mingqiang Huang (China)[1], Dr. Chenchen Ding (China)[1], Prof. Longyang Lin (China)[1], Dr. Leibin Ni (China)[1], Prof. Hao Yu (China)[1] (1. Southern University of Science and Technology)

5pm

21-7: 52.5 TOPS/W 1.7GHz Reconfigurable XGBoost Inference Accelerator based on Modular-Unit-Tree with Dynamic Data and Compute Gating

» Mr. Chang Eun Song (United States)[1], Mr. Yidong Li (United States)[1], Mr. Amardeep Ramnani (United States)[1], Mr. Pulkit Agrawal (United States)[1], Mr. Purvi Agrawal (United States)[1], Mr. Sung-Joon Jang (Korea, Republic of)[2], Mr. Sang-Seol Lee (Korea, Republic of)[2], Prof. Tajana Rosing (United States)[1], Prof. Mingu Kang (United States)[1] (1. University of California San Diego, 2. Korea Electronics Technology Institute)

3:45pm

Power Management IV cont'd -

Session 22: DC-DC Converters

Crystal Ballroom II

Chaired by: XIAOCHENG JING (United States) and Raveesh Magod (United States)

3:45pm

22-5: A Monolithic 3-Level Single-Inductor Multiple-Output Buck Converter with State-Based Non-Linear Control Capable of Handling 1A/1.5ns Transient with On-Die LC

» Dr. Junyao Tang (United States)[1], Mr. Jianqiang Jiang (United States)[1], Mr. Lei Zhao (United States)[1], Dr. Xin Zhang (United States)[2], Dr. Kang Wei (United States)[3], Prof. Cheng Huang (United States)[1] (1. Iowa State University, 2. IBM T.J. Watson Research Center, MIT-IBM Watson AI Lab, 3. Texas Instruments Inc.)

4:10pm

22-6: A 92%-Efficiency 0.828µs Settling Time FC5L Voltage Regulator Featuring Time-Domain Charge Balancing & Flying Capacitor Self-Switching for Wide Dynamic Range & Fast Transient Chiplet Applications

» Mr. Xichen Sun (China)[1], Dr. Xuliang Wang (China)[1], Dr. Jingshu Yu (China)[1], Prof. Jin Wei (China)[2], Prof. Junmin Jiang (China)[3], Prof. Chenchang Zhan (China)[3], Prof. Yan Wang (China)[1], Prof. Xiaosen Liu (China)[1] (1. Tsinghua University, 2. Peking University, 3. Southern University of Science and Technology)

4:35pm

22-7: An Emulated Peak/Valley Curve Assisted Fast-transient Buck Converter Achieving Precise One-Cycle Charge Balance with One-Parameter Calibration

» Mr. Zihao Tang (Macao)[1], Prof. Mo Huang (Macao)[1], Prof. R. P. Martins (Macao)[1], Prof. Yan Lu (Macao)[1] (1. University Of Macau)

5pm

22-8: A Fast-Slow Two-Module DC-DC Solution with Transient and Efficiency Improvements for 2.5D/3D Integration

» Mr. Junwei Huang (Macao)[1], Mr. Zhiguo Tong (Macao)[1], Dr. Xiangyu Mao (Macao)[1], Prof. Chi-Seng Lam (Macao)[1], Prof. R. P. Martins (Macao)[1], Prof. Yan Lu (Macao)[1] (1. University Of Macau)

3:45pm

Wireline and Optical Communications Circuits and Systems I cont'd -

Session 23: Wireline Transceivers and Clocking Techniques

Crystal Ballroom III

Chaired by: Prof. Tejasvi Anand (United States) and Xi Chen (United States)

3:45pm

23-3: A 29 GHz Sub-Sampling PLL with 25.6-fs-rms RJ based on a Discrete-Time Integrating PD in 45nm RF SOI

» Mr. Rajath Bindiganavile (United States)[1], Mr. Asif Wahid (United States)[1], Prof. Armin Tajalli (United States)[1] (1. University Of Utah)

Continued from **Tuesday, 23 April**

4:10pm **23-4: A 128Gb/s PAM-4 Transmitter with Edge-Boosting Pulse Generator and Pre-Emphasis Asymmetric Fractional-Spaced FFE in 28nm CMOS**
» Mr. Hongzhi Wu (China)[1], Mr. Weitao Wu (China)[1], Mr. Liping Zhong (China)[1], Mr. Xuxu Cheng (China)[1], Mr. Yangyi Zhang (China)[1], Mr. Xiongshi Luo (China)[1], Mr. Dongfan Xu (China)[1], Mr. Xindan Yu (China)[1], Prof. Quan Pan (China)[1] (1. Southern University of Science and Technology)

4:35pm **23-5: An 8-14GHz 180fs-rms DTC-Less Fractional ADPLL with ADC-Based Direct Phase Digitization in 40nm CMOS**
» Dr. Yizhuo Wang (China)[1], Prof. Hao Xu (China)[1], Ms. Guoyu Li (China)[1], Dr. Shuai Liu (China)[1], Mr. Yan Liu (China)[1], Prof. Rui Yin (China)[1], Prof. Hui Pan (China)[2], Prof. Na Yan (China)[1] (1. Fudan University, 2. Nanjing University)

3:45pm **Data Converters III cont'd -**
Session 24: High-Resolution ADCs
Colorado Ballroom II/III
Chaired by: Prof. Chia-hung Chen (Taiwan) and Prof. Shaolan Li (United States)

3:45pm **24-5: A 15MHz-BW 82.7dB-SNDR 98.8dB-SFDR Pipelined MASH 2-2 CT DSM in 65nm CMOS**
» Mr. Xinyu Qin (China)[1], Mr. Yichen Jin (China)[1], Prof. Guoxing Wang (China)[1], Prof. Sai-Weng Sin (Macao)[2], Prof. Maurits Ortmanns (Germany)[3], Prof. Yong Lian (Canada)[4], Prof. Liang Qi (China)[1] (1. Shanghai Jiao Tong University, 2. University Of Macau, 3. University of Ulm, 4. York University)

4:10pm **24-6: An 871nW 96.2dB-SNDR Pipelined NS SAR ADC Achieving 180.8dB-FoMSNDR with a Charge-Efficient CLS-Assisted Two-Stage FIA**
» Mr. Shan Zhang (China)[1], Mr. Lingxin Meng (China)[1], Mr. Zhaonan Lu (China)[1], Prof. Wanyuan Qu (China)[1], Prof. Shuang Song (China)[1], Prof. Menglian Zhao (China)[1], Prof. Zhichao Tan (China)[1] (1. Zhejiang University)

4:35pm **24-7: A 93.6dB-SNDR 5kHz-BW Fully Dynamic Hybrid CT-DT Noise Shaping SAR ADC**
» Mr. Lingxin Meng (China)[1], Prof. Menglian Zhao (China)[1], Prof. Zhichao Tan (China)[1] (1. Zhejiang University)

5pm **24-8: A 99.4 dB SFDR 91.9 dB DR Continuous-Time Incremental Delta-Sigma ADC with a Noise-Shaping SAR Quantizer and a Passive Input Feedforward Stabilization Path**
» Mr. Cheng-En Wei (Taiwan)[1], Mr. Shih-Che Kuo (Taiwan)[1], Prof. Chia-hung Chen (Taiwan)[1] (1. National Yang Ming Chiao Tung University)

4:30pm **IEEE SSCS Young Professionals and Women in Circuits Mentoring Event**
Characters Bar

5:30pm **CICC Conference Reception**
Grand Ballroom IV

Wednesday, 24 April

8am **Session 25: Keynote Session**
Grand Ballroom I/II

8am **Embracing A System-Driven Strategy to Semiconductor Technology Advancement**
» Prof. Suman Datta (United States)[1] (1. Georgia Tech)

8:50am **Break**
Grand Ballroom Foyer

9:10am **Digital Circuits, SoCs, and Systems V -**
Session 26: Digital Compute in Memory
Grand Ballroom I/II
Chaired by: Win-san (Vince) Khwa (Taiwan) and Shanshan Xie (United States)

Continued from **Wednesday, 24 April**

9:10am

Session Introduction

» Mx. Session Chair (United States)[1] (1. CICC)

9:15am

26-1: STAR-SRAM: 43.06-TFLOPS/W, 1.89-TFLOPS/mm2, 400-Kb/mm2 Floating-Point SRAM-based Digital Computing-in-Memory Macro in 28-nm CMOS

» Mr. Chuan-Tung Lin (United States)[1], Dr. Jonghyun Oh (United States)[1], Mr. Kevin Lee (United States)[1], Prof. Mingoo Seok (United States)[1] (1. Columbia University)

9:40am

26-2: SP-IMC: A Sparsity Aware In-Memory-Computing Macro in 28nm CMOS with Configurable Sparse Representation for Highly Sparse DNN Workloads

» Mr. Amitesh Sridharan (United States)[1], Mr. Fan Zhang (United States)[1], Dr. Jae-sun Seo (United States)[2], Dr. Deliang Fan (United States)[1] (1. Johns Hopkins University, 2. Cornell Tech)

10:05am

26-3: A 1-TFLOPS/W, 28-nm Deep Neural Network Accelerator featuring Online Compression and Decompression and BF16 Digital In-Memory-Computing Hardware

» Mr. Bo Zhang (United States)[1], Dr. Seunghyun Moon (United States)[1], Prof. Mingoo Seok (United States)[1] (1. Columbia University)

9:10am

Emerging Technologies, Systems, and Applications III -

Session 27: Advanced Neural Interfaces

Crystal Ballroom I

Chaired by: Sungwon Chung (United States) and Prof. Youngcheol Chae (Korea, Republic of)

9:10am

Session Introduction

» Mx. Session Chair (United States)[1] (1. CICC)

9:15am

27-1: (INVITED) Artificially Intelligent Closed-Loop Neurostimulators: Trade-offs Between Local and Remote Computing

» Mr. Jose Sales Filho (Canada)[1], Dr. Hossein Kassiri (Canada)[2], Prof. Xilin Liu (Canada)[1], Prof. Roman Genov (Canada)[1] (1. University Of Toronto, 2. York University)

10:05am

27-2: A Saturation-Free 3.6V/1.8V DM/CM Input Range 46.6mV/µs Artifacts Recovery Sensor Interface using CT Track-and-Zoom

» Mr. Qiao Cai (China)[1], Ms. Xinzi Xu (China)[1], Mr. Yanxing Suo (China)[1], Mr. Guanghua Qian (China)[1], Prof. Yongfu Li (China)[1], Prof. Guoxing Wang (China)[1], Prof. Yong Lian (Canada)[2], Prof. Yang Zhao (China)[1] (1. Shanghai Jiao Tong University, 2. York University)

9:10am

Data Converters IV -

Session 28: High-Speed Data Converters

Crystal Ballroom II

Chaired by: Filip Tavernier (Belgium) and Jin-tae Kim (Korea, Republic of)

9:10am

Session Introduction

» Mx. Session Chair (United States)[1] (1. CICC)

9:15am

28-1: (INVITED) The Race for the Extra Pico Second without Losing the Decibel: A Partial-Review of Single-Channel Energy-Efficient High-Speed Nyquist ADCs

» Prof. Chi-Hang Chan (Macao)[1], Prof. Minglei Zhang (Macao)[1], Mr. Yuefeng Cao (Macao)[1], Mr. Hongzhi Zhao (Macao)[1], Prof. R. P. Martins (Macao)[1], Prof. Yan Zhu (Macao)[1] (1. University Of Macau)

10:05am

28-2: (Best Student Paper Candidate) An 8b 1GS/s SAR ADC with Metastability-based Resolution/Speed Enhancement and Background Calibration Achieving 47.2dB SNDR at Nyquist Input

» Mr. Jie Li (China)[1], Prof. Linxiao Shen (China)[1], Mr. Siyuan Ye (China)[1], Mr. Jihang Gao (China)[1], Mr. Jiajia Cui (China)[1], Ms. Xinhang Xu (China)[1], Mr. Zhuoyi Chen (China)[1], Mr. Yaohui Luan (China)[1], Dr. Yuanxin Bao (China)[2], Prof. Ru Huang (China)[1], Prof. Le Ye (China)[1] (1. Peking University, 2. Nano Core Chip Electronic Technology, Hangzhou, China)

Continued from **Wednesday, 24 April**

9:10am **Wireless Transceivers and RF/mm-Wave Circuits and Systems IV - Session 29: Energy-efficient Radios for IoT and Emerging Systems**
Crystal Ballroom III
Chaired by: Renzhi Liu (United States) and Jane Gu (United States)

9:10am **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

9:15am **29-1: A 18.2mW Subsampling mm-Wave Receiver Employing a Subtractive Anti-Aliasing Active Bandstop Filter at 23GHz**
» Mr. Ahmed Gadelkarim (United States)[1], Dr. Patrick Mercier (United States)[1] (1. University of California San Diego)

9:40am **29-2: (Best Student Paper Candidate) A −104dBm-Sensitivity Receiver with Shared Wireless LO and Envelope-Tracking Mixer Achieving −46dB SIR**
» Mr. Heyu Ren (China)[1], Dr. Liangjian Lyu (China)[2], Ms. Binbin Chen (China)[1], Prof. C.-J. Richard Shi (United States)[3] (1. Fudan University, 2. East China Normal University, 3. University Of Washington)

10:05am **29-3: An Interference-Resilient 120-Degree-Apart Pseudo-I/Q BLE-Compliant Wake-Up Receiver Achieving -21dB SIR, -94dBm Sensitivity, and 4-D Wake-Up Signature**
» Mr. Junhong Sun (China)[1], Mr. Changgui Yang (China)[1], Mr. Yuxuan Luo (China)[1], Mr. Shurong Dong (China)[1], Prof. Bo Zhao (China)[1] (1. Zhejiang University)

10:30am **29-4: A 0.7cm2 3.5GHz, -31 dBm sensitivity batteryless 5G energy harvester backscattering chip for asset identification in IoT-enabled warehouses**
» Mr. Deniz Umut Yildirim (United States)[1], Mr. Jaeyoung Jung (United States)[2], Dr. Amr Elsakka (Sweden)[3], Dr. Giuseppe Moschetti (Sweden)[3], Dr. Miguel Lopez (Sweden)[3], Dr. Jonas Hansryd (Sweden)[3], Dr. Tomas Palacios (United States)[1], Prof. Anantha Chandrakasan (United States)[1] (1. Massachusetts Institute of Technology, 2. Analog Devices, 3. Ericsson Research)

9:10am **Wireline and Optical Communications Circuits and Systems - Session 30: Optical Transceivers and Building Blocks**
Colorado Ballroom II/III
Chaired by: Prof. Armin Tajalli (United States) and Haitao Tong (United States)

9:10am **Session Introduction**
» Mx. Session Chair (United States)[1] (1. CICC)

9:15am **30-1: (INVITED) Holistic Co-Design of Electronics and Photonics for High-Speed Optical Interconnects in SiP and CMOS Platforms**
» Dr. Arian Hashemi Talkhooncheh (United States)[1], Prof. Azita Emami (United States)[1] (1. California Institute of Technology)

10:05am **30-2: A 11pA/√Hz TIA with +15dB input OMA range for 112Gb/s PAM4 Optical Links in 22nm FDSOI**
» Dr. Mahdi Parvizi (Canada)[1], Mr. Toshi Omori (United States)[1], Dr. Bahar Jalali (United States)[1], Mr. John Rogers (United States)[1], Dr. Li Chen (United States)[1], Dr. Long Chen (United States)[1], Dr. Ricardo Aroca (United States)[1] (1. Cisco Systems)

10:30am **Break**
Grand Ballroom Foyer

10:45am **Digital Circuits, SoCs, and Systems V cont'd - Session 26: Digital Compute in Memory**
Grand Ballroom I/II
Chaired by: Shanshan Xie (United States) and Win-san (Vince) Khwa (Taiwan)

10:45am **26-4: S2D-CIM: A 22nm 128Kb Systolic Digital Compute-in-Memory Macro with Domino Data Path for Flexible Vector Operation and 2-D Weight Update in Edge AI Applications**
» Mr. Meng Wu (China)[1], Ms. Wenjie Ren (China)[1], Mr. Peiyu Chen (China)[1], Mr. Wentao Zhao (China)[1], Mr. Yiqi Jing (China)[1], Prof. Jiayoon Ru (China)[1], Dr. Zhixuan Wang (China)[1], Prof. Yufei Ma (China)[1], Prof. Ru Huang (China)[1], Prof. Tianyu Jia (China)[1], Prof. Le Ye (China)[1] (1. Peking University)

Continued from **Wednesday, 24 April**

11:10am

26-5: CILP: An Arbitrary-bit Precision All-digital Compute-in-memory Solver for Integer Linear Programming Problems

» Mr. Mengtian Yang (United States)[1], Mr. Yipeng Wang (United States)[1], Ms. Shanshan Xie (United States)[1], Mr. Chieh-Pu Lo (United States)[1], Ms. Meizhi Wang (United States)[1], Mr. Sirish Oruganti (United States)[1], Mr. Rishabh Sehgal (United States)[1], Prof. Jaydeep P. Kulkarni (United States)[1] (1. The University of Texas at Austin)

10:45am

Emerging Technologies, Systems, and Applications III cont'd - Session 27: Advanced Neural Interfaces

Crystal Ballroom I

Chaired by: Prof. Youngcheol Chae (Korea, Republic of) and Sungwon Chung (United States)

10:45am

27-3: (Best Student Paper Candidate) A 2.5-20kSps in-pixel direct digitization front-end for ECoG with in-stimulation recording

» Ms. Aditi Jain (United States)[1], Dr. Eric Fogleman (United States)[1], Dr. Paul Botros (United States)[1], Mr. Ritwik Vatsyayan (United States)[1], Dr. Corentin Pochet (United States)[1], Mr. Andrew Bourhis (United States)[1], Mr. Zhaoyi Liu (United States)[1], Mr. Suhas Chethan (United States)[1], Prof. Hanh-Phuc Le (United States)[1], Prof. Ian Galton (United States)[1], Prof. Shadi Dayeh (United States)[1], Prof. Drew Hall (United States)[1] (1. University of California San Diego)

11:10am

27-4: (Best Regular Paper Candidate) A 10V compliant 16-channel stimulator ASIC with sub-10nA mismatch and simultaneous ETI sensing for selective vagus nerve stimulation

» Dr. Haoming Xin (Netherlands)[1], Dr. Meiyi Zhou (Netherlands)[1], Mr. Roland van Wegberg (Netherlands)[1], Mr. Peter Vis (Netherlands)[1], Dr. Konstantinos Petkos (Netherlands)[1], Mr. Shrishail Patki (Netherlands)[1], Mr. Nicolo Rossetti (Netherlands)[1], Mr. Mark Fichman (Netherlands)[1], Dr. Vojkan Mihajlovic (Netherlands)[1], Dr. Carolina Mora Lopez (Belgium)[2], Dr. Geert Langereis (Netherlands)[1], Dr. Mario Konijnenburg (Netherlands)[1], Dr. Nick Van Helleputte (Belgium)[2] (1. IMEC the Netherlands, 2. IMEC)

11:35am

27-5: A Fully Integrated Dynamic-Voltage-Scaling Stimulator IC with Miniaturized Reconfigurable Supply Modulator and Channel Drivers for Cochlear Implants

» Mr. Kim-Hoang Nguyen (Korea, Republic of)[1], Mr. Quyet Nguyen (Vietnam)[2], Ms. Quynh-Trang Nguyen (Vietnam)[2], Mr. Thanh-Tung Vu (Vietnam)[2], Dr. Woojin Ahn (Korea, Republic of)[3], Prof. Loan Pham-Nguyen (Vietnam)[2], Prof. Hanh-Phuc Le (United States)[4], Prof. Minkyu Je (Korea, Republic of)[1] (1. KAIST, 2. Hanoi University of Science and Technology, 3. TODOC Co. Ltd., 4. University of California San Diego)

12pm

27-6: A 3.3-to-11V-Supply-Range 10µW/Ch Arbitrary-Waveform-Capable Neural Stimulator with Output-Adaptive-Self-Bias and Supply-Tracking Schemes in 0.18µm Standard CMOS

» Ms. Jeongyoon Wie (Korea, Republic of)[1], Mr. Sangwoo Jung (Korea, Republic of)[1], Dr. Taeryoung Seol (Korea, Republic of)[1], Mr. Geunha Kim (Korea, Republic of)[1], Dr. Sehwan Lee (Korea, Republic of)[1], Mr. Homin Jang (Korea, Republic of)[1], Dr. Samhwan Kim (Korea, Republic of)[1], Ms. Yeonjae Shin (Korea, Republic of)[1], Prof. Jae-Eun Jang (Korea, Republic of)[1], Prof. Jaeha Kung (Korea, Republic of)[2], Prof. Arup K. George (Korea, Republic of)[1], Prof. Junghyup Lee (Korea, Republic of)[1] (1. DGIST, 2. Korea university)

10:45am

Data Converters IV cont'd - Session 28: High-Speed Data Converters

Crystal Ballroom II

Chaired by: Jin-tae Kim (Korea, Republic of) and Filip Tavernier (Belgium)

10:45am

28-3: A PVT-Robust 8b 20GS/s Time-Interleaved SAR ADC with Quantization-Embedded Current-Mode Buffer and Differ-based Dither Timing Skew Calibration

» Mr. Wei Zhang (Macao)[1], Prof. Minglei Zhang (Macao)[1], Prof. Yan Zhu (Macao)[1], Prof. R. P. Martins (Macao)[1], Prof. Chi-Hang Chan (Macao)[1] (1. University Of Macau)

11:10am

28-4: A 13b 500MS/s Dual-Residue Pipelined-SAR ADC with One-Way Switching Capacitive Interpolation and Background Offset Calibration

» Prof. Wenning Jiang (China)[1], Mr. Yunbin Luo (China)[1], Mr. Peizhe Li (China)[1], Mr. Ji Guo (China)[1], Mr. Danfeng Zhai (China)[1], Prof. Chixiao Chen (China)[1], Prof. Qi Liu (China)[1] (1. Fudan University)

Continued from **Wednesday, 24 April**

11:35am **28-5: A 160MHz-BW 68dB-SNDR 30.8mW Continuous-Time Pipeline DSM with Correlative Passive Low-Pass Filters and DAC Image Pre-Filtering**

» Ms. Ke Li (Macao)[1], Mr. Congzhou Xianyu (Macao)[1], Prof. Liang Qi (China)[2], Prof. Mingqiang Guo (Macao)[1], Prof. R. P. Martins (Macao)[1], Prof. Sai-Weng Sin (Macao)[1] (1. University Of Macau, 2. Shanghai Jiao Tong University)

12pm **28-6: A 16-bit 10-GS/s Calibration-Free DAC Achieving <-77dBc IM3 up to 4.95GHz in 28nm CMOS**

» Mr. Chengyu Huang (China)[1], Mr. Kezhuo Ma (China)[1], Mr. Sihao Chen (China)[1], Mr. Jiaxuan Fan (China)[1], Prof. Nan Sun (China)[1], Prof. Huazhong Yang (China)[1], Prof. Xueqing Li (China)[1] (1. Tsinghua University)

10:45am **Wireline and Optical Communications Circuits and Systems II cont'd -**

Session 30: Optical Transceivers and Building Blocks

Colorado Ballroom II/III

Chaired by: Haitao Tong (United States) and Prof. Armin Tajalli (United States)

10:45am **30-3: A 56-Gbaud 7.3-Vppd Linear Modulator Transmitter with AMUX-based Reconfigurable FFE and Dynamic Triple-stacked Driver in 130-nm SiGe BiCMOS**

» Mr. Fuzhan Chen (China)[1], Prof. C. Patrick Yue (Hong Kong)[2], Prof. Quan Pan (China)[1] (1. Southern University of Science and Technology, 2. Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology)

11:10am **30-4: An Injection−Locked Clock Multiplier with Adaptive Pulsewidth Adjustment and Phase Error Cancellation Achieving 43.9fs RMS Jitter and −255.5dB FoM**

» Mr. Yu He (China)[1], Mr. Xuqiang Zheng (China)[1], Mr. Zedong Wang (China)[1], Mr. Zunsong Yang (China)[1], Mr. Hua Xu (China)[1], Mr. Fangxu Lv (China)[2], Mr. Mingche Lai (China)[2], Mr. Xinyu Liu (China)[1] (1. Institute of Microelectronics of the Chinese Academy of Sciences, 2. National University of Defense Technology)

11:35am **30-5: A 2λ×100 Gb/s Optical Receiver with Si-Photonic Micro-Ring Resonator and Photo-Detector for DWDM Optical-IO**

» Mr. Sikai Chen (China)[1], Mr. Jintao Xue (China)[2], Mr. Yihan Chen (China)[3], Ms. Yuean Gu (China)[3], Mr. Haoran Yin (China)[1], Mr. Shenlei Bao (China)[2], Dr. Guike Li (China)[1], Prof. Binhao Wang (China)[2], Prof. Nan Qi (China)[4] (1. State Key Lab. of Superlattices and Microstructures, Institute of Semiconductors, CAS, Beijing, China, 2. State Key Lab. of Transient Optics and Photonics, Xi'an Institute of Optics and Precision Mechanics, CAS, Xi'an, China, 3. University of Chinese Academy of Sciences, Beijing, China, 4. Institute of Semiconductors, Chinese Academy of Sciences)

12pm **30-6: An Integrated Burst-Mode 2R Receiver Employing Fast Residual Offset Canceller for XGS-PON in 40-nm CMOS**

» Mr. Yifei Xia (China)[1], Mr. Shuaizhe Ma (China)[1], Ms. Wanqing Zhao (China)[1], Mr. Jia Li (China)[1], Mr. Ruixuan Yang (China)[1], Ms. Yuye Yang (China)[1], Mr. Xi Liu (China)[1], Mr. Feiyang Zhang (China)[1], Mr. Jianyu Yang (China)[1], Mr. Wenbo Shi (China)[1], Mr. Lei Jing (China)[2], Prof. Xiaoyan Gui (China)[1], Prof. Bing Zhang (China)[1], Prof. Li Geng (China)[1], Prof. Dan Li (China)[1] (1. Xi'an Jiaotong University, 2. Huawei Technologies)

12:25pm **Lunch Break (on own)**

1:45pm **Digital Circuits, SoCs, and Systems I -**

Session 31: Panel: How can LLMs help hardware design and will it replace digital design roles in the years to come?

Grand Ballroom I/II

Chaired by: Farah Yahya (United States) and Prof. Weiwei Shan (China)

1:45pm **Foundation of System Design II cont'd -**

Session 32: Emerging Systems and Integration Techniques (Part 2)

Crystal Ballroom I

Chaired by: Farhana Sheikh (United States) and Zhengya Zhang (United States)

1:45pm **Session Introduction**

» Mx. Session Chair (United States)[1] (1. CICC)

Continued from **Wednesday, 24 April**

1:50pm **32-1: A 65nm and 130nm CMOS programmable analog standard cell library for scalable system synthesis**

» Mr. Pranav Mathews (United States)[1], Mr. Praveen Raj Ayyappan (United States)[1], Mr. Afolabi Ige (United States)[1], Mr. Swagat Bhattacharyya (United States)[1], Mr. Linhao Yang (United States)[1], Dr. Jennifer Hasler (United States)[1] (1. Georgia Institute Of Technology)

2:15pm **32-2: A 65nm 3mA 0.14-m-Accuracy TDR Based Leak Detection SoC for District Heating Networks with I/C Calibration Technique**

» Dr. Yarallah Koolivand (Iran, Islamic Republic of)[1], Dr. Alireza Mosalmani (Denmark)[2], Dr. Yasser Rezaeiyan (Denmark)[2], Mr. Hossein Esmailbeygi (Denmark)[2], Ms. Elham Hatamzadeh (Denmark)[2], Dr. Milad Zamani (Denmark)[2], Prof. Farshad Moradi (Denmark)[2], Dr. Margherita Ronchini (Denmark)[2] (1. KNT University of Technology, 2. Aarhus University)

2:40pm **32-3: A 65nm 21.9pJ/Sa Pixel to PWM Conversion SoC with Time-domain Body Communication for ULP Body-Worn Video Sensor Nodes with Distributed Real-Time Inference**

» Mr. Gourab Barik (United States)[1], Prof. Baibhab Chatterjee (United States)[2], Mr. Gaurav Kumar K (United States)[1], Prof. Shreyas Sen (United States)[1] (1. Purdue University, 2. University of Florida)

3:05pm **32-4: A Cryogenic Double-IF SSB Controller with Image Suppression and On-Chip Filtering implemented in 130nm SiGe BiCMOS Technology for Superconducting Qubit Control**

» Prof. Yatao Peng (Macao)[1], Mr. Jad Benserhir (Switzerland)[2], Ms. Yating Zou (Switzerland)[2], Prof. Edoardo Charbon (Switzerland)[2] (1. University Of Macau, 2. EPFL)

1:45pm **Analog Circuits and Techniques III - Session 33: Timing References**

Crystal Ballroom II

Chaired by: Prof. Antonio Liscidini (Canada) and Prof. Ping-Hsuan Hsieh (Taiwan)

1:45pm **Session Introduction**

» Mx. Session Chair (United States)[1] (1. CICC)

1:50pm **33-1: (Best Student Paper Candidate) A 0.144 mm2 12.5-16GHz PVT-Tolerant Dual-Path Offset-Charge-Pump-Based Fractional-N PLL Achieving 72.9 fsRMS Jitter, -271.5dB FoMN, and Sub-10% Jitter Variation**

» Mr. Xinyu Shen (China)[1], Prof. Zhao Zhang (China)[1], Prof. Yong Chen (China)[2], Mr. Yixi Li (China)[1], Ms. Yidan Zhang (China)[1], Dr. Guike Li (China)[1], Prof. Nan Qi (China)[1], Prof. Jian Liu (China)[1], Prof. Nanjian Wu (China)[1], Prof. Liyuan Liu (China)[1] (1. Institute of Semiconductors, Chinese Academy of Sciences, 2. University Of Macau)

2:15pm **33-2: ASIL-D and AEC-Q100 Grade 0 Compliant Automotive RC Oscillator with Farey Sequence-based Calibration**

» Mr. Jeongwon Han (Korea, Republic of)[1], Mr. Won-Jong Choi (Korea, Republic of)[1], Dr. Young-Suk Son (Korea, Republic of)[2], Prof. Sang-Gug Lee (Korea, Republic of)[1], Prof. Kyeongha Kwon (Korea, Republic of)[1] (1. KAIST, 2. Autosilicon)

2:40pm **33-3: A 16MHz CMOS RC Frequency Reference with ±125ppm Inaccuracy from -40°C to 85°C Enabled by a Capacitively Modulated RC Time Constant (CMT) Generation and a Die-to-Die Error Removal (DDER) Technique**

» Mr. Runtao Huo (China)[1], Mr. Dingguo Zhang (China)[1], Ms. Jing Jin (China)[1], Prof. Jianjun Zhou (China)[1], Prof. Hui Wang (China)[1] (1. Shanghai Jiao Tong University)

1:45pm **Wireless Transceivers and RF/mm-Wave Circuits and Systems V - Session 34: Forum: Wireless Transceivers Towards Next G**

Crystal Ballroom III

Chaired by: Taiyun Chi (United States) and Hamidreza Agahsi (United States)

1:45pm **34-1: Mixed-Signal Transceivers, Flexible for Future FR3 Frequencies**

» Dr. Jeffrey Walling (United States)[1] (1. Virginia Tech)

2:15pm **34-2: Design of Integrated Multibeam Phased-Array Chip**

» Dr. zhiwei xu (China)[1], Dr. Nayu Li (China)[2], Dr. Cunyi Song (China)[2] (1. Zhejiang University, 2. Donghai Lab; Zhejiang University)

Continued from **Wednesday, 24 April**

2:45pm **34-3: High-Speed D-band Point-to-Point Communications with High-Gain Antennas**
» Mr. Jose Luis Gonzalez Jimenez (France)[1] (1. CEA-Leti)

3:15pm **34-4: RFIC design innovation for silicon-based D-band phased arrays**
» Prof. Wooram Lee (United States)[1] (1. Penn State University)

1:45pm **Wireline and Optical Communications Circuits and Systems III - Session 35: Forum: Circuits and Packaging Techniques for Next-gen Wireline Communications**
Colorado Ballroom II/III
Chaired by: Shenggao (Victor) Li (United States) and Dr. Henry Park (United States)

1:45pm **35-1: High-speed Interconnects for 2.5D/3D Advance Packages**
» Mr. Chien-Chun Tsai (Taiwan)[1] (1. TSMC)

2:10pm **35-2: Advancements in D2D Interface Technologies: Paving the Way for the New Era of System Integration**
» Dr. Hyo Rhew (Korea, Republic of)[1], Dr. Byoung-Joo Yoo (Korea, Republic of)[1] (1. Samsung)

2:35pm **35-3: Development of a co-packaged Application Specific IC with optical engine chiplets**
» Mr. Jeff Hutchins (United States)[1] (1. RANOVUS)

3pm **35-4: Multi-Carrier ADC/DAC-Based Wireline Transceiver Architectures**
» Prof. Samuel Palermo (United States)[1] (1. Texas A&M University)

3:25pm **35-5: Pushing Limits of Arbitrary Waveform Generation: Insights into the Custom Power behind Ultra-High-Speed AWGs**
» Dr. Jens Muellrich (United States)[1], Dr. Rolf Schmid (Germany)[1], Mr. Ken Poulton (United States)[1], Dr. Ken Nishimura (United States)[1] (1. Keysight Technologies)

4pm **Best Paper Poster Session & Closing and Awards Ceremony**
Grand Ballroom I/II