April 24-27, 2022
Hybrid Conference
Renaissance Newport Beach, CA, USA
www.ieee-cicc.org

# CICC

## IEEE Custom Integrated Circuits Conference

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Technical Program Co-Chairs
**Arijit Raychowdhury**, Georgia Institute of Technology
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**Welcome from the CICC Committee**

Welcome to the CICC 2022 hybrid conference! On behalf of the Executive Committee and the Technical Program Committee, we are honored and delighted to present the 43rd annual IEEE Custom Integrated Circuits Conference (CICC) – a showcase for Integrated Circuits. The conference will be organized as a hybrid event with live sessions on-site at the Renaissance Newport Beach Hotel in Newport Beach, California, and live streamed to remote attendees. Our conference will be a vibrant forum for sharing state of the art techniques and results, learning from world-renowned experts in custom IC designs and adjacent fields, and networking with old and new colleagues in a virtual format.

CICC 2022 officially starts with 4 Educational Sessions on Sunday April 24th, followed by daily keynote presentations and technical lectures from Monday through Wednesday. Throughout the conference, 17 Technical Sessions, 4 Forum Sessions, and 4 Panel Sessions are strategically placed to highlight the latest trends and challenges. The Outstanding Paper awards and closing ceremony is scheduled at the end of the conference. Registration covers all the events including the Educational Sessions on Sunday. Top-rated papers will be invited to the special issues in the IEEE Journal of Solid-State Circuits and the IEEE Solid State Circuits Letters.

Four Educational Sessions provide background tutorial information on several topics of active research, including “Analog Automation Techniques”, “Design of High Power Density Voltage Regulator Circuits & Systems”, “System Design with Open Source Tools”, and “High Speed Link Design”. All presenters are well-known for their contributions in their respective areas.

The Technical Sessions are the backbone of our conference. This year’s Technical Sessions will showcase original innovative analog and digital circuit techniques covering a broad spectrum of technical topics, including: Analog Circuits, Data Converters, Design Foundations, Digital Circuits, Emerging Technologies, Power Management, Wireless Circuits, and Wireline Circuits. This year we are proud to offer a strong technical program with 98 lecture presentations, including 23 invited papers.

These Technical Sessions are complemented by Forums and Panels covering various popular areas related to integrated circuits and systems. We are pleased to offer 4 Forum Sessions, including “Next-generation computing”, “Power Management for harsh environments”, “Smart imaging”, and “Integrated circuits for sustainability”. In addition, we offer 4 Panel Sessions, including “Opensource Systems, Circuits, and Design: Is it the Future?”, “Automatic Circuit Generation and AI-Driven Design: Future of Circuit Design?”, “Is photonics going to save wireline?” and “Can quantum computing solve real-world problems?”.

Moreover, we will hold exciting social events that include the Welcome Reception on Monday evening, SSCS Young Professionals and Women in Circuits Mentoring Event on Tuesday afternoon followed by the Conference Reception. The conference will close strong on Wednesday with the Best Paper Poster Session, and the Closing Ceremony where this year’s outstanding paper winners will be announced.

Finally, the CICC Chairs and executive committee would like to extend their sincere thanks to the authors and the technical program committee members for their hard work in writing and reviewing the papers and oral presentations. Your hard work is greatly appreciated and is essential to the success of CICC 2022. Please kindly join us at the hybrid conference this year!

Arijit Raychowdhury
Technical Program Committee Chair
2022 IEEE Custom Integrated Circuits Conference

**Christophe Antoine**
General Chair

**Samuel Palermo**
Conference Chair

**Arijit Raychowdhury**
Technical Program Chair

**Eric Soenen**
Technical Program Co-Chair

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**2022 Program-at-a-Glance**
***Conference will take place in Pacific Daylight Time (PDT) (UTC-7)***

## Sunday, April 24, 2022

***All Sunday sessions are included with conference registration***

| *Bay Laurel North* | *Bay Laurel Central* | *Bay Laurel South* | *Citrus Ballroom* |
|---|---|---|---|
| 9:00 am-4:45 pm<br>**Educational Session 1:**<br>Analog Automation Techniques | 9:00 am-4:45 pm<br>**Educational Session 2:**<br>Design of High Power Density Voltage Regulator Circuits & Systems | 9:00 am-4:45 pm<br>**Educational Session 3:**<br>System Design with Open Source Tools | 9:00 am-4:45 pm<br>**Educational Session 4:**<br>High Speed Link Design |

## Monday, April 25, 2022

8:00 am-8:20 am
**Welcome and Opening Remarks**
*Bay Laurel Central & South*

8:20 am-9:10 am
**Session 1:** Keynote Session
*Bay Laurel Central & South*

| *Sequoia Ballroom 1&2* | *Bay Laurel North* | *Bay Laurel Central & South* | *Citrus Ballroom* | *Sequoia Ballroom 3&4* |
|---|---|---|---|---|
| 9:30 am-11:30 am<br>**Session 2:** Forum: Next Generation Computing | 9:30 am-11:40 am<br>**Session 3:** Imaging for Health and Automotive Systems | 9:30 am-11:40 am<br>**Session 4:** Power Management Directions | 9:30 am-11:40 am<br>**Session 5:** mm-Wave Transceivers and Systems | 9:30 am-11:00 am<br>**Session 6:** Panel: Opensource Systems, Circuits, and Design: Is it the Future? |
| 1:00 pm-5:05 pm<br>*(2:45 pm-3:00 pm break)*<br>**Session 7:** Computing-in-Memory | 1:00 pm-4:15 pm<br>*(2:45 pm-3:00 pm break)*<br>**Session 8:** Smart Sensors for the IoT, Wearables, and Implantables | 1:00 pm-4:40 pm<br>*(2:45 pm-3:00 pm break)*<br>**Session 9:** System Foundations for Intelligent Computing | 1:00 pm-4:15 pm<br>*(2:45 pm-3:00 pm break)*<br>**Session 10:** Advanced Transmitter & Receiver Circuits | 1:00 pm-2:30 pm<br>**Session 11:** Panel: Automatic Circuit Generation and AI-Driven Design: Future of Circuit Design? |

5:30 pm-7:30 pm
**Welcome Reception**
*Bamboo Garden*


**2022 Program-at-a-Glance**
***Conference will take place in Pacific Daylight Time (PDT) (UTC-7)***

| **Tuesday, April 26, 2022** | | | | |
|---|---|---|---|---|
| ***Sequoia Ballroom 1&2*** | ***Bay Laurel North*** | ***Bay Laurel Central & South*** | ***Citrus Ballroom*** | ***Sequoia Ballroom 3&4*** |
| 8:00 am-10:30 am<br>**Session 12:** Forum: Power Management for Harsh Environments | 8:00 am-12:05 pm<br>*(9:45 am -10:00 am break)*<br>**Session 13:** Advanced Technologies & Security | 8:00 am-11:40 am<br>*(9:45 am -10:00 am break)*<br>**Session 14:** High Speed Circuits and Systems for Electrical and Optical | 8:00 am-11:15 am<br>*(9:45 am -10:00 am break)*<br>**Session 15:** High-Speed Data Converters | 8:00 am-11:40 am<br>*(9:45 am -10:00 am break)*<br>**Session 16:** Next-Generation Computing and Neural Interfaces |
| 12:15 pm-1:45 pm<br>**Session 17:** Luncheon Keynote Session<br>*Citrus Ballroom* | | | | |
| 2:00 pm-5:40 pm<br>*(3:45 pm-4:00 pm break)*<br>**Session 18:** Analog Techniques | 2:00 pm-5:40 pm<br>*(3:45 pm-4:00 pm break)*<br>**Session 19:** High Performance Digital | 2:00 pm-4:10 pm<br>**Session 20:** Frequency Generation Techniques | 2:00 pm-3:30 pm<br>**Session 21:** Panel: Is Photonics Going to Save Wireline? | 2:00 pm-6:05 pm<br>*(3:45 pm-4:00 pm break)*<br>**Session 22:** Power Converters |
| 4:30 pm-6:00 pm<br>**SSCS Young Professionals and Women in Circuits Mentoring Event**<br>*Citrus Ballroom* | | | | |
| 6:00 pm-8:00 pm<br>**CICC Conference Reception**<br>*Bamboo Garden* | | | | |
| **Wednesday, April 27 2022** | | | | |
| 8:00 am-8:50 am<br>**Session 23:** Keynote Session<br>*Bay Laurel Central & South* | | | | |
| ***Sequoia Ballroom 1&2*** | ***Bay Laurel North*** | ***Bay Laurel Central & South*** | ***Citrus Ballroom*** | ***Sequoia Ballroom 3&4*** |
| 9:00 am-11:30 am<br>**Session 24:** Forum: Smart Imaging | 9:00 am-11:30 am<br>**Session 25:** Forum: IC for Sustainability | 9:00 am-11:35 am<br>**Session 26:** Quantum Computing and Energy Efficient Wireless Transceivers | 9:00 am-10:30 am<br>**Session 27:** Panel: Can Quantum Computing Solve Real World Problems? | 9:00 am-11:10 am<br>**Session 28:** High-Resolution and High-Security Data Converters |
| 1:00 pm-2:00 pm<br>**Best Paper Poster Session & Closing/Awards Ceremony**<br>*Bay Laurel Central & South* | | | | |

## Sunday, 24 April

9am **ED1 -**
**Educational Session 1: Analog Automation Techniques**
*Bay Laurel North*
Chaired by: Sudipto Chakraborty (United States) and Bongjin Kim (United States)

9am **ES1-1: Efficient Simulation of Analog/Mixed-Signal Circuits in SystemVerilog with Auto-Generated Models**
» Jaeha Kim (Korea, Republic of)[1] (1. Seoul National University)

10:45am **ES1-2: Analog and Mixed-Signal Layout Automation using Digital Place-and-Route Tools**
» Po-Hsuan Wei (United States)[1] (1. Nvidia Corporation)

9am **ED2 -**
**Educational Session 2: Design of High Power Density Voltage Regulator Circuits & Systems**
*Bay Laurel Central*
Chaired by: Hans Meyvaert (Belgium) and Hyun-Sik Kim (Korea, Republic of)

9am **ES2-1: Integrated High-Input Voltage Converters for High-Density, High-Efficiency Power Delivery Solutions**
» Nachiket Desai (United States)[1] (1. Intel)

10:45am **ES2-2: Pushing the Boundaries of Wide-Bandgap Power Conversion: A Journey Towards Monolithic Integration**
» Jef Thoné (Belgium)[1] (1. MinDCet NV)

9am **ED3 -**
**Educational Session 3: System Design with Open Source Tools**
*Bay Laurel South*
Chaired by: Xinfei Guo (China) and Xuan (Silvia) Zhang (United States) and Weidong Cao (United States)

9am **ES3-1: The OpenROAD Project: A Foundation for Research and Education in EDA and IC Design**
» Andrew B. Kahng (United States)[1] (1. University of California San Diego)

10:45am **ES3-2: Why is Google Investing in Fully Open Source IC Design and What is Next?**
» Tim 'mithro' Ansell (United States)[1] (1. Google)

9am **ED4 -**
**Educational Session 4: High Speed Link Design**
*Citrus Ballroom*
Chaired by: Tod Dickson (United States) and Xiang Gao (China)

9am **ES4-1: Architectural Considerations in 100+ Gbps Wireline Transceivers**
» Tony Chan Carusone (Canada)[1] (1. University of Toronto)

10:45am **ES4-2: Clocking for Serial Links  Frequency and Jitter Requirements, Phase-Locked Loops, Clock and Data Recovery**
» Saurabh Saxena (India)[1] (1. IIT Madras)

12:15pm **Break**

12:15pm **Break**

12:15pm **Break**

12:15pm **Break**

1:30pm **Educational Session 1: Analog Automation Techniques**
*Bay Laurel North*
Chaired by: Sudipto Chakraborty (United States) and Bongjin Kim (United States)

1:30pm **ES1-3: Has the Time for Analog Design Automation Finally Come?**
» David Reed (United States)[1], Avina Verma (United States)[1] (1. Synopsys)

Continued from **Sunday, 24 April**

3:15pm **ES1-4: Improving Analog/Custom Design Productivity with ML**
» Hongzhou Liu (United States)[1], Chandramouli Kashyap (United States)[1] (1. Cadence Design Systems)

1:30pm **Educational Session 2: Design of High Power Density Voltage Regulator Circuits & Systems**
*Bay Laurel Central*
Chaired by: Hans Meyvaert (Belgium) and Hyun-Sik Kim (Korea, Republic of)

1:30pm **ES2-3: High Performance Power Electronics for High Performance Computing: Design with Hybrid Switched Capacitor Circuits and Magnetics**
» Minjie Chen (United States)[1] (1. Princeton University)

3:15pm **ES2-4: Basics of Adaptive & Resilient Circuits & Integration into Future Voltage Regulators**
» Keith Bowman (United States)[1] (1. Qualcomm)

1:30pm **Educational Session 3: System Design with Open Source Tools**
*Bay Laurel South*
Chaired by: Xinfei Guo (China) and Xuan (Silvia) Zhang (United States) and Weidong Cao (United States)

1:30pm **ES3-3: Creating a World where a 14-year-old Designs a Chip**
» Mohamed Kassem (United States)[1] (1. Efabless Corporation)

3:15pm **ES3-4: Toward Agile, Intelligent and Open-Source Design Automation of Digital, Analog and Mixed-Signal ICs**
» David Z. Pan (United States)[1] (1. University of Texas at Austin)

1:30pm **Educational Session 4: High Speed Link Design**
*Citrus Ballroom*
Chaired by: Xiang Gao (China) and Tod Dickson (United States)

1:30pm **ES4-3: Equalization, Architecture, and Circuit Design for High-Speed Serial Link Receiver**
» Gain Kim (Korea, Republic of)[1] (1. DGIST)

3:15pm **ES4-4: Transmitter Design for High-speed Serial Data Communications**
» Jihwan Kim (United States)[1] (1. Intel)

## Monday, 25 April

8am **Welcome -**
**Welcome and Opening Remarks**
*Bay Laurel Central & South*
Chaired by: Christophe Antoine (United Kingdom) and Sam Palermo (United States) and Eric Soenen

8:20am **Keynote Session 1 -**
**Session 1: Keynote Session**
*Bay Laurel Central & South*
Chaired by: Christophe Antoine (United Kingdom) and Sam Palermo (United States) and Eric Soenen

8:20am **Design and Technology Directions to Enable the Zetta-Scale Computing Era**
» Dr. Eric Karl (United States)[1] (1. , Intel Fellow, Director, Advanced Design, Director, Embedded Memory Technology and Circuits)

9:30am **Forum Session 1 -**
**Session 2: Forum: Next Generation Computing**
*Sequoia Ballroom 1&2*
Chaired by: Sudipto Chakraborty (United States) and Shih-Chii Liu (Switzerland)

Continued from **Monday, 25 April**

9:30am

**2-1: Energy-Efficient Neuromorphic Computing-in-Memory**

» Gert Cauwenberghs (United States)[1] (1. University of California San Diego)

10am

**2-2: Phase-change memory-based analog in-memory computing for AI**

» Irem Boybat (Switzerland)[1] (1. IBM Zurich)

10:30am

**2-3: Silicon photonic neural networks for computing and AI**

» Bhavin Shastri (Canada)[1] (1. Queen's University)

11am

**2-4: Improvement of Ising machine by non-stoquastic operators and development for quantum simulations**

» Yuya Seki (Japan)[1] (1. Keio University)

9:30am

**Emerging Technologies, Systems, and Applications 1 - Session 3: Imaging for Health and Automotive Systems**

*Bay Laurel North*

Chaired by: Jong Seok Park (United States) and Chul Kim (Korea, Republic of)

9:30am

**Introduction: Imaging for Health and Automotive Systems**

» Jong Seok Park (United States)[1], Chul Kim (Korea, Republic of)[2] (1. Intel, 2. KAIST)

9:35am

**3-1: A Review of Silicon Photonics LiDAR (Invited)**

» Hossein Hashemi (United States)[1] (1. University of Southern California)

10:25am

**3-2: (Best Student Paper Candidate) Solid-State dToF LiDAR System Using an Eight-Channel Addressable, 20W/Ch Transmitter, and a 128x128 SPAD Receiver with SNR-Based Pixel Binning and Resolution Upscaling**

» Shenglong Zhuo (China)[1], Lei Zhao (China)[1], Tao Xia (China)[1], Lei Wang (China)[2], Shi Shi (China)[1], Yifan Wu (China)[2], Chang Liu (China)[1], Jier Wang (China)[1], Yuwei Wang (China)[2], Yuan Li (China)[1], Miao Sun (China)[3], Jie Li (China)[3], Hengwei Yu (China)[1], Jiqing Xu (China)[1], Long Wang (China)[2], Zhihong Lin (China)[1], Yun Chen (China)[1], Quan Pan (China)[4], Yajie Qin (China)[3], Jiawei Xu (China)[3], Rui Bai (China)[2], Xuefeng Chen (China)[2], Patrick Chiang (China)[1] (1. Fudan University, Shanghai, 2. PhotonIC Technologies, Shanghai, 3. Fudan University, 4. Southern University of Science and Technology)

10:50am

**3-3: A 13.1 mm2 512 x 256 Multimodal CMOS Array for Spatiochemical Imaging of Bacterial Biofilms**

» Kangping Hu (United States)[1], Joseph Incandela (United States)[2], Xiaoyu Lian (United States)[1], Joseph Larkin (United States)[2], Jacob Rosenstein (United States)[1] (1. Brown University, 2. Boston University)

11:15am

**3-4: A 36□40 Pixel Wireless Fluorescence Image Sensor for Real-time Microscopy in Cancer Immunotherapy**

» Rozhan Rabbani (United States)[1], Hossein Najafiaghdam (United States)[1], Biqi Zhao (United States)[1], Micah Roschelle (United States)[1], Megan Zeng (United States)[1], Vladimir Stojanovic (United States)[1], Rikky Muller (United States)[1], Mekhail Anwar (United States)[2] (1. University of California, Berkeley, 2. University of California, San Francisco & University of California, Berkeley)

9:30am

**Power Management 1 - Session 4: Power Management Directions**

*Bay Laurel Central & South*

Chaired by: John Pigott (United States) and Hans Meyvaert (Belgium)

9:30am

**Introduction: Power Management Directions**

» John Pigott (United States)[1], Hans Meyvaert (Belgium)[2] (1. NXP Semiconductors, 2. SoliDC)

Continued from **Monday, 25 April**

9:35am

**4-1: Piezoelectric-Based Power Conversion: Recent Progress, Opportunities, and Challenges (Invited)**

» Jessica Boles (United States)[1], Joshua Piel (United States)[1], Elaine Ng (United States)[1], Joseph Bonavia (United States)[1], Jeffrey Lang (United States)[1], David Perreault (United States)[1] (1. Massachusetts Institute of Technology)

10:25am

**4-2: An 86.7% Efficient Three-Level Boost Converter with Active Voltage Balancing for Thermoelectric Energy Harvesting**

» Loan Pham-Nguyen (Vietnam)[1], Nam Nguyen-Dac (Vietnam)[2], Thinh Tran-Dinh (Korea, Republic of)[3], Hieu Minh Pham (United States)[4], Minkyu Je (Korea, Republic of)[3], Sang-Gug Lee (Korea, Republic of)[3], Hanh-Phuc Le (United States)[4] (1. Hanoi University of Science and Technology, 2. Ha Noi University of Sience and Technology, 3. KAIST, 4. University of California San Diego)

10:50am

**4-3: (Best Student Paper Candidate) A 93.7%-Efficiency 5-Ratio Switched-Photovoltaic DC-DC Converter**

» Sandeep Reddy Kukunuru (United States)[1], Yashar Naeimi (United States)[1], Loai Salem (United States)[1] (1. University of California, Santa Barbara)

11:15am

**4-4: A 400 V-to-12 V Fully Integrated Switched-Capacitor DC-DC Converter Achieving 119 mW/mm² at 63.6 % Efficiency**

» Tuur Van Daele (Belgium)[1], Filip TAVERNIER (Belgium)[1] (1. Katholieke Universiteit Leuven)

9:30am

**Wireless Transceivers and RF/mm-Wave Circuits and Systems 1 - Session 5: mm-Wave Transceivers and Systems**

*Citrus Ballroom*

Chaired by: Aritra Banerjee (United States) and Jane Gu (United States)

9:30am

**Introduction: mm-Wave Transceivers and Systems**

» Aritra Banerjee (United States)[1], Jane Gu (United States)[2] (1. IMEC, 2. University of California, Davis)

9:35am

**5-1: (Best Student Paper Candidate) A 23-37GHz Autonomous Two-Dimensional MIMO Receiver Array with Rapid Full-FoV Spatial Filtering for Unknown Interference Suppression**

» Boce Lin (United States)[1], Tzu-Yuan Huang (United States)[1], Amr Ahmed (United States)[1], Min-Yu Huang (United States)[1], Hua Wang (United States)[1] (1. Georgia Institute of Technology)

10am

**5-2: IC and Array Technologies for 100-300GHz Wireless (Invited)**

» Mark Rodwell (United States)[1], Ali Farid (United States)[1], Ahmed Ahmed (United States)[1], Munkyo Seo (Korea, Republic of)[2], Utku Soylu (United States)[1], Amidreza Alizadeh (United States)[1], Navid Hosseinzadeh (United States)[1] (1. University of California, Santa Barbara, 2. Sungkyunkwan University)

10:50am

**5-3: A 220 GHz Sliding-IF Quadrature Transmitter With 38-dB Conversion Gain and 8-dBm Psat in 0.13-µm SiGe BiCMOS**

» Zekun Li (China)[1], Jixin Chen (China)[2], Jiayang Yu (China)[1], Huanbo Li (China)[1], Zichun Zheng (China)[1], Rui Zhou (China)[1], Peigen Zhou (China)[1], Zhe Chen (China)[1], Wei Hong (China)[2] (1. State Key Laboratory of Millimeter Waves, Southeast University. Nanjing, China, 2. 1.State Key Laboratory of Millimeter Waves, Southeast University. Nanjing, China; 2.Purple Mountain Laboratory, Nanjing, China)

11:15am

**5-4: (Best Student Paper Candidate) A 3.8-dB NF, 23-40GHz Phased-Array Receiver with 14-Bit Phase & Gain Manager and Calibration-Free Dual-Mode 28-52dB Image Rejection Ratio for 5G NR**

» Zhixian Deng (China)[1], Huizhen Qian (China)[1], Changxuan Han (China)[1], Yifan Li (China)[1], Xun Luo (China)[1] (1. University of Electronic Science and Technology of China)

9:30am

**Panel Session 1 - Session 6: Panel: Opensource Systems, Circuits, and Design: Is it the Future?**

*Sequoia Ballroom 3&4*

Chaired by: Mondira Pant (United States) and Jing Li (United States)

Continued from **Monday, 25 April**

1pm **Digital Circuits, SoCs, and Systems 1 -**
**Session 7: Computing-in-Memory**
*Sequoia Ballroom 1&2*
Chaired by: Jie Gu (United States) and Ekin Sumbul (United States)

1pm **Introduction: Computing-in-Memory**
» Jie Gu (United States)[1], Ekin Sumbul (United States)[2] (1. Northwestern University, 2. Meta)

1:05pm **7-1: Comprehending In-memory Computing Trends via Proper Benchmarking (Invited)**
» Naresh Shanbhag (United States)[1], Saion Roy (United States)[1] (1. University of Illinois at Urbana-Champaign)

1:55pm **7-2: (Best Regular Paper Candidate) 5GHz SRAM for High-Performance Compute Platform in 5nm CMOS**
» Rahul Mathur (United States)[1], Munish Kumar (India)[2], Vivek Asthana (India)[2], Shruti Aggarwal (United States)[1], Siddharth Gupta (India)[2], Dattatray Wanjul (India)[2], Abhishek Baradia (United States)[1], Srikanth Thota (United States)[1], Piyush Jain (India)[2], Bo Zheng (United States)[1], Antonio Cubeta (France)[2], Sriram Thyagarajan (United States)[1], Andy Chen (United States)[1], Yew Chong (United States)[1] (1. ARM Inc, 2. Arm)

2:20pm **7-3: (Best Regular Paper Candidate) An area-efficient 6T-SRAM based Compute-In-Memory architecture with reconfigurable SAR ADCs for energy-efficient deep neural networks in edge ML applications**
» Avishek Biswas (United States)[1], HETUL SANGHVI (United States)[1], Mahesh Mehendale (United States)[1], Preet Garcha (United States)[1] (1. Texas Instruments Inc)

1pm **Emerging Technologies, Systems, and Applications 2 -**
**Session 8: Smart Sensors for the IoT, Wearables, and Implantables**
*Bay Laurel North*
Chaired by: Drew Hall (United States) and SungWon Chung (United States)

1pm **Introduction: Smart Sensors for the IoT, Wearables, and Implantables**
» Drew Hall (United States)[1], Sungwon Chung (United States)[2] (1. University of California San Diego, 2. Neuralink)

1:05pm **8-1: Smart Threads for Tissue-Embedded Bioelectronics (Invited)**
» Sameer Sonkusale (United States)[1] (1. Tufts University)

1:55pm **8-2: Wireless Frequency-Division Multiplexed 3D Magnetic Localization for Low Power Sub-mm Precision Capsule Endoscopy**
» Michella Rustom (United States)[1], Constantine Sideris (United States)[1] (1. University of Southern California)

2:20pm **8-3: A Battery-Less Crystal-Less 49.8μW Neural-Recording Chip Featuring Two-Tone RF Power Harvesting**
» Ziyi Chang (China)[1], Changgui Yang (China)[1], Yunshan Zhang (China)[1], Zhuhao Li (China)[1], Tianyu Zheng (China)[1], Yuxuan Luo (China)[1], Shaomin Zhang (China)[1], Kedi Xu (China)[1], Yong Chen (China)[2], Gang Pan (China)[1], Bo Zhao (China)[1] (1. Zhejiang University, 2. University of Macau)

1pm **Foundation of System Design 1 -**
**Session 9: System Foundations for Intelligent Computing**
*Bay Laurel Central & South*
Chaired by: Siddharth Joshi (United States) and Jing Li (United States)

1pm **Introduction: System Foundations for Intelligent Computing**
» Siddharth Joshi (United States)[1], Jing Li (United States)[2] (1. University of Notre Dame, 2. University of Pennsylvania)

1:05pm **9-1: StreamGCN: Accelerating Graph Convolutional Networks with Streaming Processing (Invited)**
» Atefeh Sohrabizadeh (United States)[1], Yuze Chi (United States)[1], Jason Cong (United States)[1] (1. UCLA)

Continued from **Monday, 25 April**

1:55pm **9-2: An Energy-Efficient and Runtime-Reconfigurable FPGA-Based Accelerator for Robotic Localization Systems**
» Qiang Liu* (China)[1], Zishen Wan (United States)[2], Bo Yu* (United States)[3], Weizhuang Liu (China)[1], Shaoshan Liu (United States)[3], Arijit Raychowdhury (United States)[2] (1. Tianjin University, 2. Georgia Institute of Technology, 3. PerceptIn)

2:20pm **9-3: A 39pJ/label 1920x1080 165.7 FPS Block PatchMatch Based Stereo Matching Processor on FPGA**
» Hongyu Wang (China)[1], Wei Zhou (China)[1], Xiangyu Zhang (China)[1], Xin Lou (China)[1] (1. ShanghaiTech University)

1pm **Wireless Transceivers and RF/mm-Wave Circuits and Systems 2 - Session 10: Advanced Transmitter & Receiver Circuits**
*Citrus Ballroom*
Chaired by: Debopriyo Chowdhury (United States) and Amr Fahim (United States)

1pm **Introduction: Advanced Transmitter & Receiver Circuits**
» Debopriyo Chowdhury (United States)[1], Amr Fahim (United States)[1] (1. Broadcom)

1:05pm **10-1: A Phase-Modulation Phase-Shifting Phased-Array Transmitter with 10-Bit Fast-Locking Phase Self-Calibration and 0/2.5/6/12dB Power Back-Offs Efficiency Enhancement**
» Jie Zhou (China)[1], Huizhen Qian (China)[1], Bingzheng Yang (China)[1], Yiyang Shu (China)[1], Xun Luo (China)[1] (1. University of Electronic Science and Technology of China)

1:30pm **10-2: A 1-to-4GHz Multi-Mode Digital Transmitter in 40nm CMOS Supporting 200MHz 1024-QAM OFDM signals with more than 23dBm/66% Peak Power/Drain Efficiency**
» Mohammadreza Beikmirza (Netherlands)[1], Yiyu Shen (Netherlands)[1], Leo de Vreede (Netherlands)[1], Morteza Alavi (Netherlands)[1] (1. Delft University of Technology, Delft, The Netherlands)

1:55pm **10-3: Watt-Level Triple-Mode Quadrature SFCPA with 56 Peaks for Ultra-Deep PBO Efficiency Enhancement Using IQ Intrinsic Interaction and Adaptive Phase Compensation**
» Bingzheng Yang (China)[1], Huizhen Qian (China)[1], Yiyang Shu (China)[1], Jie Zhou (China)[1], Xun Luo (China)[1] (1. University of Electronic Science and Technology of China)

2:20pm **10-4: 22-30GHz Quadrature Hybrid SCPA with LO Leakage Self-Suppression and Distributed Parasitic-Cancelling Sub-PA Array for Linearity and Efficiency Enhancement**
» Bingzheng Yang (China)[1], Huizhen Qian (China)[1], Yiyang Shu (China)[1], Jie Zhou (China)[1], Xun Luo (China)[1] (1. University of Electronic Science and Technology of China)

1pm **Panel Session 2 - Session 11: Panel: Automatic Circuit Generation and AI-Driven Design: Future of Circuit Design?**
*Sequoia Ballroom 3&4*
Chaired by: Xin Zhang (United States) and Jong Seok Park (United States)

2:45pm **Break**

2:45pm **Break**

2:45pm **Break**

2:45pm **Break**

3pm **Digital Circuits, SoCs, and Systems 1 (cont.) - Session 7: Computing-in-Memory**
*Sequoia Ballroom 1&2*
Chaired by: Jie Gu (United States) and Ekin Sumbul (United States)

Continued from **Monday, 25 April**

3pm **7-4: A 915-1220 TOPS/W Hybrid In-Memory Computing based Image Restoration and Region Proposal Integrated Circuit for Neuromorphic Vision Sensors in 65nm CMOS**

» Xueyong Zhang (Singapore)[1], Arindam Basu (Hong Kong)[2] (1. Nanyang Technological University, 2. City Univ)

3:25pm **7-5: A 177 TOPS/W, Capacitor-based In-Memory Computing SRAM Macro with Stepwise-Charging/Discharging DACs and Sparsity-Optimized Bitcells for 4-Bit Deep Convolutional Neural Networks**

» Bo Zhang (United States)[1], Jyotishman Saikia (United States)[2], Jian Meng (United States)[2], Dewei Wang (United States)[1], Soonwan Kwon (Korea, Republic of)[3], Sungmeen Myung (Korea, Republic of)[3], Hyunsoo Kim (Korea, Republic of)[3], Sang Joon Kim (Korea, Republic of)[3], Jae-sun Seo (United States)[2], Mingoo Seok (United States)[1] (1. Columbia University, 2. Arizona State University, 3. Samsung Advanced Institute of Technology)

3:50pm **7-6: DCT-RAM: A Driver-Free Processing-In-Memory 8T SRAM Macro with Multi-Bit Charge-Domain Computation and Time-Domain Quantization**

» Zhiyu Chen (United States)[1], Qing Jin (United States)[2], Zhanghao Yu (United States)[1], Yanzhi Wang (United States)[2], Kaiyuan Yang (United States)[1] (1. Rice University, 2. Northeastern University)

4:15pm **7-7: A 133.6TOPS/W Compute-In-Memory SRAM Macro with Fully Parallel One-Step Multi-Bit Computation**

» Edward Choi (Korea, Republic of)[1], Injun Choi (Korea, Republic of)[1], Chanhee Jeon (Korea, Republic of)[1], Gichan Yun (Korea, Republic of)[1], Donghyeon Yi (Korea, Republic of)[1], Sohmyung Ha (United Arab Emirates)[2], Ik Joon Chang (Korea, Republic of)[3], Minkyu Je (Korea, Republic of)[1] (1. KAIST, 2. New York University Abu Dhabi, 3. Kyunghee University)

4:40pm **7-8: (Best Student Paper Candidate) T-PIM: A 2.21-to-161.08TOPS/W Processing-In-Memory Accelerator for End-to-End On-Device Training**

» Jaehoon Heo (Korea, Republic of)[1], Junsoo Kim (Korea, Republic of)[1], Wontak Han (Korea, Republic of)[1], Sukbin Lim (Korea, Republic of)[1], Joo-Young Kim (Korea, Republic of)[1] (1. KAIST)

3pm **Emerging Technologies, Systems, and Applications 2 (cont.) - Session 8: Smart Sensors for the IoT, Wearables, and Implantables**

*Bay Laurel North*

Chaired by: Drew Hall (United States) and SungWon Chung (United States)

3pm **8-4: Wireless, Batteryless, and Secure Implantable System-on-a-Chip for 1.37mmHg Strain Sensing with Bandwidth Reconfigurability for Cross-Tissue Adaptation**

» Mohamed Abdelhamid (United States)[1], Unsoo Ha (United States)[1], Utsav Banerjee (India)[2], Fadel Adib (United States)[1], Anantha Chandrakasan (United States)[1] (1. Massachusetts Institute of Technology, 2. Indian Institute of Science)

3:25pm **8-5: A 0.8V/0.6V 2.2µW Time-Domain Analog Front-End with 540mVpp Input Range, 81.6dB SNDR and 80MΩ Input Impedance**

» Liheng Liu (China)[1], Tianxiang Qu (China)[1], Pengjie Wang (China)[1], Yao Zhang (China)[1], Zhiliang Hong (China)[1], Jiawei Xu (China)[1] (1. Fudan University, Shanghai, China)

3:50pm **8-6: An Energy-Harvesting Stamp-Sized Reader for Distance-Immune Interrogation of Passive Wireless Sensors**

» Siavash Kananian (United States)[1], Cheng Chen (United States)[1], Ada S. Y. Poon (United States)[1] (1. Stanford University)

3pm **Foundation of System Design 1 (cont.) - Session 9: System Foundations for Intelligent Computing**

*Bay Laurel Central & South*

Chaired by: Siddharth Joshi (United States) and Jing Li (United States)

3pm **9-4: Hardware/Software Co-design for Neuromorphic Systems (Invited)**

» Rajit Manohar (United States)[1] (1. Yale University)

3:50pm **9-5: The Rise of SoC FPAA Devices (Invited)**

» Jennifer Hasler (United States)[1] (1. Georgia Institute of Technology)

Continued from **Monday, 25 April**

3pm **Wireless Transceivers and RF/mm-Wave Circuits and Systems 2 (cont.) -**
**Session 10: Advanced Transmitter & Receiver Circuits**
*Citrus Ballroom*
Chaired by: Debopriyo Chowdhury (United States) and Amr Fahim (United States)

3pm **10-5: A Compact Wideband Joint Bidirectional Class-G Digital Doherty Switched-Capacitor Transmitter and N-Path Quadrature Receiver through Capacitor Bank Sharing**
» Jeongseok Lee (United States)[1], Doohwan Jung (United States)[1], David Munzer (United States)[1], Hua Wang (Switzerland)[2] (1. Georgia Institute of Technology, 2. ETH Zurich)

3:25pm **10-6: A 0.5-3GHz Receiver with a Parallel Preselect Filter Achieving 120dB/dec Channel Selectivity and +28dBm Out-of-Band IIP3**
» Mohammad Ali Montazerolghaem (Netherlands)[1], Leo de Vreede (Netherlands)[1], Masoud Babaie (Netherlands)[1] (1. Delft University of Technology)

3:50pm **10-7: A 2GHz voltage mode power scalable RF-Front-End with 2.5dB-NF and 0.5dBm-1dBCP**
» Justin Yonghui Kim (Canada)[1], Antonio Liscidini (Canada)[1] (1. University of Toronto)

5:30pm **Welcome Reception**
*Bamboo Garden*

## Tuesday, 26 April

8am **Forum Session 2 -**
**Session 12: Forum: Power Management for Harsh Environments**
*Sequoia Ballroom 1&2*
Chaired by: Hanh-Phuc Le (United States) and Dina El-Damak (Egypt)

8am **12-1: Smart Power ICs for Harsh Automotive environment**
» Sri Navaneeth Easwaran (United States)[1] (1. Texas Instruments)

8:30am **12-2: Integrated Circuit Reliability in Radiation Environments**
» Robert Baumann (United States)[1] (1. Radiosity Solutions LLC)

9am **12-3: Power converter design in hostile environments - flying, shaking, freezing, and radiated**
» Robert Pilawa (United States)[1], Samantha Coday (United States)[1] (1. University of California, Berkeley)

9:30am **12-4: "Are We Alone? NASA Technologies to Find Life Beyond Earth and Answers to Other Science Questions"**
» Goutam Chattopadhyay (United States)[1] (1. NASA Jet Propulsion Laboratory (JPL))

8am **Digital Circuits, SoCs, and Systems 2 -**
**Session 13: Advanced Technologies & Security**
*Bay Laurel North*
Chaired by: Visvesh Sathe (United States) and Yoonmyung Lee (Korea, Republic of)

8am **Introduction: Advanced Technologies & Security**
» Visvesh Sathe (United States)[1], Yoonmyung Lee (Korea, Republic of)[2] (1. University of Washington, 2. Sungkyunkwan University)

8:05am **13-1: System technology co-optimization and design challenges for 3D IC (Invited)**
» Supreet Jeloka (United States)[1], Brian Cline (United States)[1], Shidhartha Das (United Kingdom)[2], Benoit Labbe (United Kingdom)[2], Alejandro Rico (United States)[1], Rainer Herberholz (United Kingdom)[2], Javier DeLaCruz (United States)[1], Rahul Mathur (United States)[1], Shawn Hung (United States)[1] (1. ARM Inc, 2. Arm Ltd)

Continued from **Tuesday, 26 April**

8:55am **13-2: TICA: A 0.3V, Variation-Resilient 64-Stage Deeply-Pipelined Bitcoin Mining Core with Timing Slack Inference and Clock Frequency Adaption**

» Jieyu Li (China)[1], Weifeng He (China)[1], Bo Zhang (United States)[2], Guanghui He (China)[1], Jun Yang (China)[3], Mingoo Seok (United States)[2] (1. Shanghai Jiao Tong University, 2. Columbia University, 3. Southeast University)

9:20am **13-3: A 334uW 0.158mm2 Saber Learning with Rounding based Post-Quantum Crypto Accelerator**

» Archisman Ghosh (United States)[1], Jose Maria Bermudo Mera (Belgium)[2], Angshuman Karmakar (Belgium)[2], Debayan Das (United States)[1], Santosh Ghosh (United States)[3], Ingrid Verbauwhede (Belgium)[2], Shreyas Sen (United States)[1] (1. Purdue University, 2. KU Leuven, 3. Intel Corporation)

8am **Wireline and Optical Communications Circuits and Systems 1 - Session 14: High Speed Circuits and Systems for Electrical and Optical**

*Bay Laurel Central & South*

Chaired by: Mayank Raj (United States) and Xi Chen (United States)

8am **Introduction: High Speed Circuits and Systems for Electrical and Optical**

» Mayank Raj (United States)[1], Xi Chen (United States)[2] (1. Xilinx, 2. Nvidia)

8:05am **14-1: (Best Invited Paper Candidate)110-GHz-Bandwidth InP-HBT AMUX/ADEMUX Circuits for Beyond-1-Tb/s/ch Digital Coherent Optical Transceivers**

» Munehiko Nagatani (Japan)[1], Hitoshi Wakita (Japan)[1], Teruo Jyo (Japan)[1], Tsutomu Takeya (Japan)[1], Hiroshi Yamazaki (Japan)[1], Yoshihiro Ogiso (Japan)[2], Miwa Mutoh (Japan)[1], Yuta Shiratori (Japan)[1], Minoru Ida (Japan)[1], Fukutaro Hamaoka (Japan)[3], Masanori Nakamura (Japan)[3], Takayuki Kobayashi (Japan)[3], Hiroyuki Takahashi (Japan)[1], Yutaka Miyamoto (Japan)[3] (1. NTT Device Technology Labs., NTT Corporation, 2. NTT Device Innovation Center, NTT Corporation, 3. NTT Network Innovation Labs., NTT Corporation)

8:55am **14-2: (Best Student Paper Candidate) A 112 Gb/s -8.2 dBm Sensitivity 4-PAM Linear TIA in 16nm CMOS with Co-Packaged Photodiodes**

» Dhruv Patel (Canada)[1], Alireza Sharif-Bakhtiar (Canada)[2], Tony Chan Carusone (Canada)[1] (1. University of Toronto, 2. Huawei Technologies)

9:20am **14-3: A 10/2.5-Gb/s Hyper-Supplied CMOS Low-Noise Burst-Mode TIA with Loud Burst Protection and Gearbox Automatic Offset Cancellation for XGS-PON**

» Chen Tan (China)[1], Wei Huang (China)[1], Yonghui Fan (China)[1], Jing Li (China)[1], Chuanhao Yu (China)[1], Wenbo Shi (China)[1], Shiti Huang (China)[1], Zhenyu Yin (China)[1], Chenfan Cao (China)[1], Lei Jing (China)[2], Zhixiong Ren (China)[2], Xiaoyan Gui (China)[1], Bing Zhang (China)[1], Li Geng (China)[1], Dan Li (China)[1] (1. Xi'an Jiaotong University, 2. Huawei Technologies)

8am **Data Converters 1 - Session 15: High-Speed Data Converters**

*Citrus Ballroom*

Chaired by: Vanessa Chen (United States) and Filip TAVERNIER (Belgium)

8am **Introduction: High-Speed Data Converters**

» Vanessa Chen (United States)[1], Filip Tavernier (Belgium)[2] (1. Carnegie Mellon University, 2. Katholieke Universiteit Leuven)

8:05am **15-1: A 48dB-SFDR, 43dB-SNDR, 50GS/s 9-bit 2x-interleaved Nyquist DAC in Intel 16**

» Hariprasad Chandrakumar (United States)[1], Thomas Brown (United States)[1], Dimitri Frolov (United States)[1], Zinia Tuli (United States)[1], Iwen Huang (United States)[1], Said Rami (United States)[1] (1. Intel Corp)

8:30am **15-2: A 10b 700MS/s single-channel 1b/cycle SAR ADC using a monotonic-specific feedback SAR logic with power-delay-optimized unbalanced N/P-MOS sizing**

» Minggiang Guo (China)[1], Sai-Weng Sin (Macao)[1], Liang Qi (China)[2], Gangjun Xiao (China)[3], Rui Paulo Martins (China)[1] (1. University of Macau, 2. Shanghai Jiao Tong University, 3. Amicro Semiconductor Co., Ltd)

Continued from **Tuesday, 26 April**

8:55am **15-3: A 38GS/s 7b Time-Interleaved Pipelined-SAR ADC with Speed-Enhanced Bootstrapped Switch in 22nm FinFET**

» Yuanming Zhu (United States)[1], Tong Liu (United States)[1], Srujan Kumar Kaile (United States)[1], Julian Camilo Gomez Diaz (United States)[1], Shiva Kiran FNU (United States)[1], Il-Min Yi (United States)[1], Ruida Liu (United States)[1], Sebastian Hoyos (United States)[1], Samuel Palermo (United States)[1] (1. Texas A and M University)

9:20am **15-4: (Best Regular Paper Candidate) A Calibration-Free 13b 625MS/s Tri-State Pipelined-SAR ADC with PVT-Insensitive Inverter-Based Residue Amplifier**

» Xiaofeng GUO (China)[1], Run CHEN (China)[2], Rongfeng XU (China)[1], Bin Li (China)[1], ZhenQi Chen (China)[2] (1. South China University of Technology, Guangzhou, 2. Newradio Technology Co., Ltd., Shenzhen)

8am **Emerging Technologies, Systems, and Applications 3 - Session 16: Next-Generation Computing and Neural Interfaces**

*Sequoia Ballroom 3&4*

Chaired by: Ulkuhan GULER (United States) and Yaoyao Jia (United States)

8am **Introduction: Next-Generation Computing and Neural Interfaces**

» Ulkuhan Guler (United States)[1], Yaoyao Jia (United States)[2] (1. Worcester Polytechnic Institute, 2. North Carolina State University)

8:05am **16-1: Spiking Neural Network Integrated Circuits: A Review of Trends and Future Directions (Invited)**

» Arindam Basu (Hong Kong)[1], Charlotte Frenkel (Switzerland)[2], Lei Deng (China)[3], Xueyong Zhang (Singapore)[4] (1. City University of Hong Kong, 2. Institute of Neuroinformatics, University of Zurich and ETH Zurich, 3. Tsinghua University, 4. Nanyang Technological University)

8:55am **16-2: An Analog Clock-free Compute Fabric base on Continuous-Time Dynamical System for Solving Combinatorial Optimization Problems**

» Muya Chang (United States)[1], Xunzhao Yin (China)[2], Zoltan Toroczkai (United States)[3], Xiaobo Hu (United States)[3], Arijit Raychowdhury (United States)[1] (1. Georgia Institute of Technology, 2. Zhejiang University, 3. University of Notre Dame)

9:20am **16-3: A 16-Channel 60μW Neural Synchrony Processor for Multi-Mode Phase-Locked Neurostimulation**

» Uisub Shin (Switzerland)[1], Cong Ding (Switzerland)[1], Laxmeesha Somappa (Switzerland)[1], Virginia Woods (United States)[2], Alik S. Widge (United States)[2], Mahsa Shoaran (Switzerland)[1] (1. EPFL, 2. University of Minnesota)

9:45am **Break**

9:45am **Break**

9:45am **Break**

9:45am **Break**

10am **Digital Circuits, SoCs, and Systems 2 (cont.) - Session 13: Advanced Technologies & Security**

*Bay Laurel North*

Chaired by: Visvesh Sathe (United States) and Yoonmyung Lee (Korea, Republic of)

10am **13-4: PVT Tolerant Zero Bit-Error-Rate Physical Unclonable Function Exploiting Hot Carrier Injection Aging in 7nm FinFET Technology**

» Jyothi Bhaskarr Velamala (United States)[1], Siang-Jhih Sean Wu (United States)[1], Padma Penmatsa (United States)[1], Kuan-Yueh James Shen (United States)[1], David Johnston (United States)[1], Rachael Parker (United States)[1] (1. Intel)

10:25am **13-5: A Lossless and Modeling Attack-Resistant Strong PUF with <4E-8 Bit Error Rate**

» Yan He (United States)[1], Qixuan Yu (United States)[1], Kaiyuan Yang (United States)[1] (1. Rice University)

Continued from **Tuesday, 26 April**

10:50am

**13-6: (Best Invited Paper Candidate) 3nm Gate-All-Around (GAA) Design-Technology Co- Optimization (DTCO) for succeeding PPA by Technology**

» Taejoong Song (Korea, Republic of)[1], Hakchul Jung (Korea, Republic of)[1], Giyoung Yang (Korea, Republic of)[1], Hoyoung Tang (Korea, Republic of)[1], Hayoung Kim (Korea, Republic of)[1], Dongwook Seo (Korea, Republic of)[1], Hoonki Kim (Korea, Republic of)[1], Woojin Rim (Korea, Republic of)[1], Sanghoon Baek (Korea, Republic of)[1], Sangyeop Baeck (Korea, Republic of)[1], Jonghoon Jung (Korea, Republic of)[1] (1. Samsung Electronics)

11:40am

**13-7: A Digital Cascoded Signature Attenuation Countermeasure with Intelligent Malicious Voltage Drop Attack Detector for EM/Power SCA Resilient Parallel AES-256**

» Archisman Ghosh (United States)[1], Dong-Hyun Seo (United States)[1], Debayan Das (United States)[1], Santosh Ghosh (United States)[2], Shreyas Sen (United States)[1] (1. Purdue University, 2. Intel Corporation)

10am

**Wireline and Optical Communications Circuits and Systems 1 (cont.) -**

**Session 14: High Speed Circuits and Systems for Electrical and Optical**

*Bay Laurel Central & South*

Chaired by: Mayank Raj (United States) and Xi Chen (United States)

10am

**14-4: Interconnect in the Era of 3DIC (Invited)**

» Shenggao Li (United States)[1] (1. TSMC)

10:50am

**14-5: A 60-Gb/s/pin single-ended PAM-4 transmitter with timing skew training and low power data encoding in mimicked 10nm class DRAM process**

» Joohwan Kim (Korea, Republic of)[1], Junyoung Park (Korea, Republic of)[1], Jindo Byun (Korea, Republic of)[1], Changkyu Seol (Korea, Republic of)[1], ChangSoo Yoon (Korea, Republic of)[1], EunSeok Shin (Korea, Republic of)[1], Hyunyoon Cho (Korea, Republic of)[1], Youngdo Um (Korea, Republic of)[1], Sucheol Lee (Korea, Republic of)[1], Hyungmin Jin (Korea, Republic of)[1], Kwangseob Shin (Korea, Republic of)[1], Hyunsub Norbert Rie (Korea, Republic of)[1], Minsu Jung (Korea, Republic of)[1], Jin-Hee Park (Korea, Republic of)[1], Go-Eun Cha (Korea, Republic of)[1], Minjae Lee (Korea, Republic of)[1], YoungMin Kim (Korea, Republic of)[1], Byeori Han (Korea, Republic of)[1], Yuseong Jeon (Korea, Republic of)[1], Jisun Lee (Korea, Republic of)[1], Hyejeong So (Korea, Republic of)[1], Sungduk Kim (Korea, Republic of)[1], Wansoo Park (Korea, Republic of)[1], Tae young Kim (Korea, Republic of)[1], Youngdon Choi (Korea, Republic of)[1], Jung-Hwan Choi (Korea, Republic of)[1], Hyungjong Ko (Korea, Republic of)[1], Sang-Hyun Lee (Korea, Republic of)[1] (1. Samsung Electronics)

11:15am

**14-6: A Jitter-Robust 40Gb/s ADC-Based Multicarrier Receiver Front End in 22nm FinFET**

» Yuanming Zhu (United States)[1], Julian Camilo Gomez Diaz (United States)[1], Srujan Kumar Kaile (United States)[1], Il-Min Yi (United States)[1], Tong Liu (United States)[1], Sebastian Hoyos (United States)[1], Samuel Palermo (United States)[1] (1. Texas A and M University)

10am

**Data Converters 1 (cont.) -**

**Session 15: High-Speed Data Converters**

*Citrus Ballroom*

Chaired by: Vanessa Chen (United States) and Filip TAVERNIER (Belgium)

10am

**15-5: (Best Invited Paper Candidate) High-Speed Digital-to-Analog Converter Design Towards High Dynamic Range**

» Shiyu Su (United States)[1], Mike Shuo-Wei Chen (United States)[1] (1. University of Southern California)

10:50am

**15-6: A 30-MHz BW 74.6-dB SNDR 92-dB SFDR CT ΔΣ Modulator with Active Body-Bias DAC Calibration in 22nm FDSOI CMOS**

» Marcel Runge (Germany)[1], Julius Edler (Germany)[1], Dario Schmock (Netherlands)[2], Tobias Kaiser (Germany)[1], Friedel Gerfers (Germany)[1] (1. TU Berlin, 2. Ethernovia BV)

Continued from **Tuesday, 26 April**

10am **Emerging Technologies, Systems, and Applications 3 (cont.) - Session 16: Next-Generation Computing and Neural Interfaces**
*Sequoia Ballroom 3&4*
Chaired by: Ulkuhan GULER (United States) and Yaoyao Jia (United States)

10am **16-4: A SAR-Assisted DC-Coupled Chopper-Stabilized 20μsArtifact-Recovery ΔΣ ADC for Simultaneous Neural Recording and Stimulation**
» Tania Moeinfard (Canada)[1], Georg Zoidl (Canada)[1], Hossein Kassiri (Canada)[2] (1. York University, 2. Department of Electrical Engineering and Computer Science, York University)

10:25am **16-5: A 6.8μW AFE for Ear EEG Recording with Simultaneous Impedance Measurement for Motion Artifact Cancellation**
» Aviral Pandey (United States)[1], Sina Faraji Alamouti (United States)[1], Justin Doong (United States)[1], Ryan Kaveh (United States)[1], Cem Yalcin (United States)[1], Mohammad Meraj Ghanbari (United States)[2], Rikky Muller (United States)[1] (1. University of California, Berkeley, 2. berkeley)

10:50am **16-6: A 92%-Efficiency Inductor-Charging Switched-Capacitor Stimulation System with Level-Adaptive Duty Modulation and Offset Charge Balancing for Muscular Stimulation**
» Kyeongho Eom (Korea, Republic of)[1], Han-sol Lee (Korea, Republic of)[1], Minju Park (Korea, Republic of)[1], Seung Min Yang (Korea, Republic of)[1], Jong Chan Choe (Korea, Republic of)[1], Suk-Won Hwang (Korea, Republic of)[1], Young-Woo Suh (Korea, Republic of)[2], Hyung-Min Lee (Korea, Republic of)[1] (1. Korea University, 2. Korea University Ansan Hospital)

11:15am **16-7: A 65nm Implantable Gesture Classification SoC for Rehabilitation with Enhanced Data Compression and Encoding for Robust Neural Network Operation Under Wireless Power Condition**
» Yijie Wei (United States)[1], Xi Chen (United States)[1], Jie Gu (United States)[1] (1. Northwestern University)

12:15pm **Keynote Session 2 - Session 17: Keynote Luncheon**
*Citrus Ballroom*
Chaired by: Sam Palermo (United States) and Christophe Antoine (United Kingdom) and Eric Soenen

12:15pm **Democratizing IC Design: The Story of a New Movement**
» Boris Murmann (United States)[1] (1. Professor of Electrical Engineering, Stanford University)

2pm **Analog Circuits and Techniques 1 - Session 18: Analog Techniques**
*Sequoia Ballroom 1&2*
Chaired by: Shaolan Li (United States) and Elnaz Ansari (United States)

2pm **Introduction: Analog Techniques**
» Shaolan Li (United States)[1], Elnaz Ansari (United States)[2] (1. Georgia tech, 2. Facebook)

2:05pm **18-1: Photoplethysmography (PPG) Sensor Circuit Design Techniques (Invited)**
» Qiuyang Lin (Belgium)[1], Wim Sijbers (Belgium)[1], Christina Avdikou (Belgium)[1], Chris Van Hoof (Belgium)[1], Filip Tavernier (Belgium)[2], Nick Van Helleputte (Belgium)[1] (1. imec, Leuven, Belgium, 2. Katholieke Universiteit Leuven)

2:55pm **18-2: A 1.8GΩ-Input-Impedance 0.15μV-Input-Referred-Ripple Chopper Amplifier with Local Positive Feedback and SAR-Assisted Ripple Reduction**
» Tianxiang Qu (China)[1], Qinjing Pan (China)[1], Xiaoyang Zeng (China)[1], Zhiliang Hong (China)[1], Jiawei Xu (China)[1] (1. Fudan University)

3:20pm **18-3: A Neural Recording Analog Front-End with Exponentially Tunable Pseudo Resistors and On-Chip Digital Frequency Calibration Loop Achieving 3.4% Deviation of High-Pass Cutoff Frequency in 5-to-500 Hz Range**
» Renze Gan (China)[1], Liangjian Lyu (China)[2], Geng Mu (China)[1], C. -J. Richard Shi (United States)[3] (1. Fudan University, 2. East China Normal Universisty, 3. University of Washington)

Continued from **Tuesday, 26 April**

2pm **Digital Circuits, SoCs, and Systems 3 - Session 19: High Performance Digital**

*Bay Laurel North*

Chaired by: Carlos Tokunaga (United States) and Kaiyuan Yang (United States)

2pm **Introduction: High Performance Digital**

» Carlos Tokunaga (United States)[1], Kaiyuan Yang (United States)[2] (1. Intel Corporation, 2. Rice University)

2:05pm **19-1: (Best Invited Paper Candidate) System-Level Design and Integration of a Prototype AR/VR Hardware Featuring a Custom Low-Power DNN Accelerator Chip in 7nm Technology for Codec Avatars**

» Ekin Sumbul (United States)[1], Tony Wu (United States)[1], Yuecheng Li (United States)[1], Syed Shakib Sarwar (United States)[1], William Koven (United States)[1], Eli Murphy-Trotzky (United States)[1], Xingxing Cai (United States)[1], Elnaz Ansari (United States)[1], Daniel Morris (United States)[1], Huichu Liu (United States)[1], Doyun Kim (United States)[1], Edith Beigne (United States)[1] (1. Meta)

2:55pm **19-2: MPAM: Reliable, Low-Latency, Near-Threshold-Voltage Multi-Voltage/Frequency-Domain Network-on-Chip with Metastability Risk Prediction and Mitigation**

» Chuxiong Lin (China)[1], Weifeng He (China)[1], Yanan Sun (China)[1], Lin Shao (China)[1], Bo Zhang (United States)[2], Jun Yang (China)[3], Mingoo Seok (United States)[2] (1. Shanghai Jiao Tong University, 2. Columbia University, 3. Southeast University)

3:20pm **19-3: A 2.86Gb/s Fully-Flexible MU-MIMO Processor for Jointly Optimizing User Selection, Power Allocation, and Precoding in 28nm CMOS Technology**

» Seungsik Moon (Korea, Republic of)[1], Namyoon Lee (Korea, Republic of)[1], Youngjoo Lee (Korea, Republic of)[1] (1. POSTECH)

2pm **Wireless Transceivers and RF/mm-Wave Circuits and Systems 3 - Session 20: Frequency Generation Techniques**

*Bay Laurel Central & South*

Chaired by: Hamidreza Agahsi (United States) and Wanghua Wu (United States)

2pm **Introduction: Frequency Generation Techniques**

» Hamidreza Agahsi (United States)[1], Wanghua Wu (United States)[2] (1. University of California Irvine, 2. Samsung)

2:05pm **20-1: Recent Advances in High-Performance Frequency Synthesizer Design (Invited)**

» Salvatore Levantino (Italy)[1] (1. Politecnico di Milano)

2:55pm **20-2: (Best Student Paper Candidate) A 9GHz 72fs-Total-Integrated-Jitter Fractional-N Digital PLL with Calibrated Frequency Quadrupler**

» Francesco Buccoleri (Italy)[1], Simone Mattia Dartizio (Italy)[1], Francesco Tesolin (Italy)[1], Luca Avallone (Austria)[2], Alessio Santiccioli (Italy)[1], Agata Iesurum (Italy)[3], Giovanni Steffan (Austria)[2], Andrea Bevilacqua (Italy)[3], Luca Bertulessi (Italy)[1], Dmytro Cherniak (Austria)[2], Carlo Samori (Italy)[1], Andrea Leonardo Lacaita (Italy)[1], Salvatore Levantino (Italy)[1] (1. Politecnico di Milano, 2. Infineon Technologies, 3. University of Padova)

3:20pm **20-3: A 12.5-to-15.4GHz, -118.9dBc/Hz PN at 1MHz offset, and 191.0dBc/Hz FoM VCO with Common-Mode Resonance Expansion and Simultaneous Differential 2ND-Harmonic Output using a Single Three-Coil Transformer in 65nm CMOS**

» Ruichang Ma (China)[1], Haikun Jia (China)[1], Wei Deng (China)[1], Zhihua Wang (China)[1], Baoyong Chi (China)[1] (1. School of Integrated Circuits, BNRist, Tsinghua University, China)

3:45pm **20-4: A 2-GHz Dual-Path Sub-Sampling PLL with Ring VCO Phase Noise Suppression**

» Yangtao Dong (Singapore)[1], Chirn Chye Boon (Singapore)[1], Kaituo Yang (Singapore)[1], Zhe Liu (Singapore)[1] (1. Nanyang Technological University)

Continued from **Tuesday, 26 April**

2pm **Panel Session 3 -**
**Session 21: Panel: Is Photonics Going to Save Wireline?**
*Citrus Ballroom*
Chaired by: Armin Tajalli (United States) and Zhipeng Li (United States)

2pm **Power Management 2 -**
**Session 22: Power Converters**
*Sequoia Ballroom 3&4*
Chaired by: Hans Meyvaert (Belgium) and John Pigott (United States)

2pm **Introduction: Power Converters**
» Hans Meyvaert (Belgium)[1], John Pigott (United States)[2] (1. SoliDC, 2. NXP Semiconductors)

2:05pm **22-1: Review, Survey, and Benchmark of Recent Digital LDO Voltage Regulators (Invited)**
» Zhaoqing Wang (United States)[1], Sung Justin Kim (United States)[1], Keith Bowman (United States)[2], Mingoo Seok (United States)[1] (1. Columbia University, 2. Qualcomm)

2:55pm **22-2: A Single-Mode Dual-Path Buck-Boost Converter with Reduced Inductor Current Across All Duty Cases Achieving 95.58% Efficiency at 1A in Boost Operation**
» Donghee Cho (Korea, Republic of)[1], Hyungjoo Cho (Korea, Republic of)[1], Sein Oh (Korea, Republic of)[1], Yoontae Jung (Korea, Republic of)[1], Sohmyung Ha (United Arab Emirates)[2], Chul Kim (Korea, Republic of)[1], Minkyu Je (Korea, Republic of)[1] (1. KAIST, 2. New York University Abu Dhabi)

3:20pm **22-3: A Fully In-Package 4-Phase Fixed-Frequency DAB Hysteretic Controlled DC-DC Converter with Enhanced Efficiency, Load Regulation and Transient Response**
» Lei Zhao (United States)[1], Junyao Tang (United States)[1], Cheng Huang (United States)[1] (1. iowa state university)

3:45pm **Break**

3:45pm **Break**

4pm **Analog Circuits and Techniques 1(cont.) -**
**Session 18: Analog Techniques**
*Sequoia Ballroom 1&2*
Chaired by: Shaolan Li (United States) and Elnaz Ansari (United States)

4pm **18-4: Switched-Capacitor Circuits (Invited)**
» David Allstot (United States)[1], Un-Ku Moon (United States)[1], Gabor Temes (United States)[1] (1. Oregon State University)

4:25pm **18-5: (Best Student Paper Candidate) A 20µs turn-on time, 24kHz resolution, 1.5-100MHz digitally programmable temperature-compensated clock generator with 7.5ppm/°C inaccuracy**
» Yongxin Li (United States)[1], Nilanjan Pal (United States)[1], Tianyu Wang (United States)[1], Mostafa Ahmed (United States)[1], Ahmed Abdelrahman (United States)[1], Mohamed Younis (United States)[1], Ruhao Xia (United States)[1], Kyu-Sang Park (United States)[1], Pavan Hanumolu (United States)[1] (1. University of Illinois at Urbana-Champaign)

4:50pm **18-6: A 19-30ppm/□ Temperature Coefficient Sub-nanowatt CMOS Voltage Reference with 10-µA Sourcing Capability**
» Hongchang Qiao (China)[1], Chenchang Zhan (China)[1] (1. Southern University of Science and Technology)

5:15pm **18-7: Filtering Trans-Impedance Amplifiers: from mW of Power to GHz of Bandwidth (Invited)**
» Nimesh Miral (Italy)[1], Karan Sohal (Italy)[1], Danilo Manstretta (Italy)[1], Rinaldo Castello (Italy)[1] (1. università degli studi di pavia)

4pm **Digital Circuits, SoCs, and Systems 3 (cont.) -**
**Session 19: High Performance Digital**
*Bay Laurel North*
Chaired by: Carlos Tokunaga (United States) and Kaiyuan Yang (United States)

Continued from **Tuesday, 26 April**

4pm

**19-4: An Energy-Efficient Cardiac Arrhythmia Classification Processor using Heartbeat Difference based Classification and Event-Driven Neural Network Computation with Adaptive Wake-Up**

» Jiahao Liu (China)[1], Jianbiao Xiao (China)[1], Jiajing Fan (China)[1], Qingsong Liu (China)[1], Zhen Zhu (China)[1], Sixu Li (China)[1], Zhaomin Zhang (China)[1], Siqi Yang (China)[1], Weiwei Shan (China)[2], Shuisheng Lin (China)[1], Liang Chang (China)[1], Liang Zhou (China)[1], Jun Zhou (China)[1] (1. University of Electronic Science and Technology of China, 2. Southeast University)

4:25pm

**19-5: DDPMnet: All-Digital Pulse Density-Based DNN Architecture with 228 Gate Equivalents/MAC Unit, 28-TOPS/W and 1.5-TOPS/mm2 in 40nm**

» Animesh Gupta (Singapore)[1], Viveka Konandur Rajanna (Singapore)[1], Thoithoi Salam (Singapore)[1], Saurabh Jain (Singapore)[1], Orazio Aiello (Singapore)[1], Paolo Crovetti (Italy)[2], Massimo Alioto (Singapore)[1] (1. ECE, National University of Singapore, 2. DET, Politecnico di Torino)

4:50pm

**19-6: A 181μW Real-Time 3-D Hand Gesture Recognition System based on Bi-directional Convolution and Computing-Efficient Feature Clustering**

» LU YUNCHENG (Singapore)[1], Zehao Li (Singapore)[1], Yuzong Chen (Singapore)[2], Tony Tae-Hyoung Kim (Singapore)[1] (1. Nanyang Technological University, 2. National University of Singapore)

5:15pm

**19-7: (Best Student Paper Candidate) An 0.92 mJ/frame High-quality FHD Super-resolution Mobile Accelerator SoC with Hybrid-precision and Energy-efficient Cache**

» Zhiyong Li (Korea, Republic of)[1], Sangjin Kim (Korea, Republic of)[1], Dongseok Im (Korea, Republic of)[1], Donghyeon Han (Korea, Republic of)[1], Hoi-Jun Yoo (Korea, Republic of)[1] (1. KAIST)

4pm

**Power Management 2 (cont.) -**
**Session 22: Power Converters**

*Sequoia Ballroom 3&4*

Chaired by: Hans Meyvaert (Belgium) and John Pigott (United States)

4pm

**22-4: A Hybrid Always-Dual-Path Recursive Step-Down Converter Using Adaptive Switching Level Control Achieving 95.4% Efficiency with 288mΩ Large-DCR Inductor**

» Woojoong Jung (Korea, Republic of)[1], Minsu Kim (Korea, Republic of)[1], Hyunjun Park (Korea, Republic of)[1], Sungmin Yoo (Korea, Republic of)[2], Taehwang Kong (Korea, Republic of)[2], Jun-Hyeok Yang (Korea, Republic of)[2], Michael Choi (Korea, Republic of)[2], Jongshin Shin (Korea, Republic of)[2], Hyung-Min Lee (Korea, Republic of)[1] (1. Korea University, 2. Samsung Electronics)

4:25pm

**22-5: A Highly-Integrated 20-300V 0.5W Active-Clamp Flyback DCDC Converter with 76.7% Peak Efficiency**

» Christoph Rindfleisch (Germany)[1], Jens Otten (Germany)[1], Bernhard Wicht (Germany)[1] (1. Leibniz University Hannover)

4:50pm

**22-6: A 0.66 W/mm2 Power Density, 92.4% Peak Efficiency Hybrid Converter with nH-Scale Inductors for 12 V System**

» Tianshi Xie (United States)[1], Jianglin Zhu (United States)[2], Tom Byrd (United States)[3], Dragan Maksimovic (United States)[2], Hanh-Phuc Le (United States)[1] (1. University of California, San Diego, 2. University of Colorado Boulder, 3. Lockheed Martin Corporation)

5:15pm

**22-7: An Up to 10MHz 6.8% Minimum Duty Ratio GaN Driver with Dual-MOS-Switches Bootstrap and Adaptive Short-Pulse Based High-CMTI Level Shifter Achieving 6.05% Efficiency Improvement**

» Xin Ming (China)[1], Zhiyi Lin (China)[1], Tianyi Sun (China)[1], Yao Qin (China)[1], Yuanyuan Liu (China)[1], Chunwang Zhuang (China)[1], Xince Gong (China)[1], Zhaoji Li (China)[1], Bo Zhang (China)[1] (1. UESTC)

5:40pm

**22-8: All Rivers Flow to the Sea: A High Power Density Wireless Power Receiver with Split-Dual-Path Rectification and Hybrid-Quad-Path Step-Down Conversion**

» Zixiao Lin (China)[1], Yan Lu (Macao)[1], Fangyu Mao (China)[1], Chuang Wang (China)[1], Rui Paulo Martins (China)[1] (1. University of Macau)

4:30pm

**SSCS Young Professionals and Women in Circuits Mentoring Event**

*Citrus Ballroom*

Continued from **Tuesday, 26 April**

6pm **CICC Conference Reception**
*Citrus Ballroom*

## Wednesday, 27 April

8am **Keynote Session 3 -**
**Session 23: Keynote Session**
*Bay Laurel Central & South*
Chaired by: Sam Palermo (United States) and Eric Soenen

8am **RF Transceivers, Pursuing the Endless Frontier**
» Reza Rofougaran (United States)[1] (1. CTO / Founder, Movandi)

9am **Forum Session 3 -**
**Session 24: Forum: Smart Imaging**
*Sequoia Ballroom 1&2*
Chaired by: Ping-Hsuan Hsieh (Taiwan) and Jerald Yoo (Singapore)

9am **24-1: Time-of-Flight depth sensing and imaging: design challenges, evolution and emerging trends**
» David Stoppa (Italy)[1] (1. Sony)

9:30am **24-2: Intelligent vision chip using mixed-mode processing-in-sensor technique and tiny machine-learning model.**
» Chih-Cheng Hsieh (Taiwan)[1] (1. National Tsing-Hua University)

10am **24-3: How can massively parallel, three-dimensional photon counting reshape image sensing**
» Edoardo Charbon (Switzerland)[1] (1. Swiss Federal Institute of Technology)

10:30am **24-4: X and γ Ray Detectors for Imaging and Spectroscopy in Space Missions**
» Piero Malcovati (Italy)[1] (1. University of Pavia)

11am **24-5: Superman Vision: Fully Integrated Terahertz Imaging Radar in CMOS**
» Ehsan Afshari (United States)[1] (1. University of Michigan)

9am **Forum Session 4 -**
**Session 25: Forum: IC for Sustainability**
*Bay Laurel North*
Chaired by: Elnaz Ansari (United States) and Armin Tajalli (United States)

9am **25-1: Tracking nitrogen in soil with printed chemical sensors**
» Ana Arias (United States)[1] (1. University of California, Berkeley)

9:30am **25-2: HW/SW Ecosystems for a Sustainable Planet**
» Doug Carmean (United States)[1] (1. Meta)

10am **25-3: End-to-End Design for Semiconductor Sustainability, a Quest**
» Andrew Byrnes (United States)[1] (1. Micron)

10:30am **25-4: Scaling AI Computing Sustainably: Environmental Implications, Challenges and Opportunities**
» Carole-Jean Wu (United States)[1] (1. Meta)

11am **25-5: From SoCs to Chiplet-Based SiPs**
» Ramin Farjadrad (United States)[1] (1. Eliyan Corp.)

9am **Wireless Transceivers and RF/mm-Wave Circuits and Systems 4 -**
**Session 26: Quantum Computing and Energy Efficient Wireless Transceivers**
*Bay Laurel Central & South*
Chaired by: Julian Tham (United States) and Steven Bowers (United States)

Continued from **Wednesday, 27 April**

9am

**Introduction: Quantum Computing and Energy Efficient Wireless Transceivers**

» Julian Tham (United States)[1], Steven Bowers (United States)[2] (1. Infineon Technologies, 2. University of Virginia)

9:05am

**26-1: ULP Receivers in Self-Powered Industrial IoT Applications: Challenges and Prospects (Invited)**

» Kuo-Ken Huang (United States)[1], Jonathan Brown (United States)[1], Richard Sawyer (United States)[1], Chris Lukas (United States)[1], Farah Yahya (United States)[1], Alice Wang (United States)[1], Nathan Roberts (United States)[1], Benton Calhoun (United States)[1], David Wentzloff (United States)[1] (1. Everactive)

9:55am

**26-2: A 0.14nJ/b 200Mb/s Quasi-Balanced FSK Transceiver with Closed-Loop Modulation and Sideband Energy Detection**

» Bowen Wang (China)[1], Cong Ding (China)[1], Yunzhao Nie (China)[1], Woogeun Rhee (China)[1], Zhihua Wang (China)[2] (1. Tsinghua University, 2. School of Integrated Circuits, BNRist, Tsinghua University, China)

10:20am

**26-3: A 7.25-7.75GHz 5.9mW UWB Transceiver with –23.8dBm NBI Tolerance and 1.5cm Ranging Accuracy Using Uncertain IF and Pulse-Triggered Envelope/Energy Detection**

» Bowen Wang (China)[1], Haixin Song (China)[1], Woogeun Rhee (China)[1], Zhihua Wang (China)[2] (1. Tsinghua University, 2. School of Integrated Circuits, BNRist, Tsinghua University, China)

10:45am

**26-4: (Best Invited Paper Candidate) Cryogenic CMOS for Qubit Control and Readout**

» Stefano Pellerano (United States)[1], Sushil Subramanian (United States)[1], Jong-Seok Park (United States)[1], Bishnu Patra (United States)[1], Todor Mladenov (United States)[1], Xiao Xue (Netherlands)[2], Lieven Vandersypen (Netherlands)[2], Masoud Babaie (Netherlands)[2], Edoardo Charbon (Switzerland)[3], Fabio Sebastiano (Netherlands)[2] (1. Intel Corporation, 2. Delft University of Technology, 3. Swiss Federal Institute of Technology)

9am

**Panel Session 4 -**

**Session 27: Panel: Can Quantum Computing Solve Real World Problems?**

*Citrus Ballroom*

Chaired by: Sudipto Chakraborty (United States) and Swaroop Ghosh (United States)

9am

**Data Converters 2 -**

**Session 28: High-Resolution and High-Security Data Converters**

*Sequoia Ballroom 3&4*

Chaired by: Derek Chia-Hung Chen (Taiwan) and Delong Cui (United States)

9am

**Introduction: High-Resolution and High-Security Data Converters**

» Derek Chia-Hung Chen (Taiwan)[1], Delong Cui (United States)[2] (1. National Chiao Tung University, 2. Broadcom)

9:05am

**28-1: Design Techniques for High Linearity and Dynamic Range Digital to Analog Converters (Invited)**

» Ayman Shabra (United States)[1], Yun-Shiang Shu (Taiwan)[1], Shon-Hang Wen (Taiwan)[1], Kuan-Dar Chen (Taiwan)[1] (1. MediaTek)

9:55am

**28-2: Randomized Switching SAR (RS-SAR) ADC Protections for Power and Electromagnetic Side Channel Security**

» Maitreyi Ashok (United States)[1], Edlyn Levine (United States)[2], Anantha Chandrakasan (United States)[1] (1. Massachusetts Institute of Technology, 2. MITRE Corporation)

10:20am

**28-3: A 77µW 115dB-Dynamic-Range 586fA-Sensitivity Current-Domain Continuous-Time Zoom ADC with Pulse-Width-Modulated Resistor DAC and Background Offset Compensation Scheme**

» Hao Zhang (China)[1], Linxiao Shen (China)[1], Shichuang Zhang (China)[2], Heyi Li (China)[1], Yihan Zhang (China)[1], Zeyu Cai (China)[1], Zhichao Tan (China)[3], Ru Huang (China)[1], Le Ye (China)[1] (1. Peking University, 2. Advanced Institute of Information Technology, 3. Zhejiang University)

Continued from **Wednesday, 27 April**

10:45am

**28-4: A 0.37mm2 250kHz-BW 95dB-SNDR CTDSM with Low-Cost 2nd-order Vector-Quantizer DEM**

» Wei Shi (United States)[1], Xing Wang (China)[2], Xiyuan Tang (China)[3], Abhishek Mukherjee (United States)[1], Raviteja Theertham (India)[4], Shanthi Pavan (India)[4], Lu Jie (China)[2], Nan Sun (United States)[5] (1. University of Texas at Austin, 2. Tsinghua University, 3. Peking University, 4. India Institute of Technology, 5. University of Texas at Austin, Tsinghua University)

1pm

**Best Paper Poster Session & Closing and Awards Ceremony**

*Bay Laurel Central & South*