

A Monolithic Buck Converter Using Differentially Enhanced Duty Ripple Control

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Abstract-This paper reports a monolithic DC-DC buck converter using the differentially enhanced duty ripple control (DE-DRC). Without any compensation circuit, this converter is stable over a wide input and output range. The switching frequency is kept constant by adjusting the on-time according to the input and output voltage. Because of the large duty ripple voltage with a big noise margin, the DE-DRC buck converter has better noise immunity than current mode and hysteretic control. The easily configured positive and negative differential difference amplifier (DDA) gains (K_p and K_n) can adjust the high and low frequency portion of the loop transfer function to achieve fast load transient response. Load transient test also showed 5mΩ pure resistive output impedance of this converter to achieve the adaptive voltage position (AVP) function. We demonstrated a 1.85MHz single phase converter with wide conversion range of 10%-86.6%. This circuit was implemented in 0.5μm BCD process of TI.

I. INTRODUCTION

The buck converters are widely used in portable devices to provide power from battery. In these applications, the DC-DC converter needs to regulate its output voltage to lower voltage and must quickly respond to fast load current transients to keep their output voltage within a limited range [1]. The Current Mode Control (CMC) and the Hysteretic Control are widely used for Buck converters to achieve a fast transient response. The major disadvantage of the CMC and the hysteretic control is the large noise on the small sensed current signal for the CMC or the output voltage ripple for the hysteretic control. This noise can prematurely terminate or initiate a switching period [2]. Another drawback is the switching frequency of the hysteretic control is affected by parasitic parameters and can change a lot with different input and output conditions, and degrades the performance of the converter.

In this work, a step down converter using differentially enhanced duty ripple control (DE-DRC) method is reported. The stable operation without compensation and constant switching frequency are achieved over a wide input and output voltage range. With large duty ripple voltage, the whole control system has very good noise immunity. With this unique control loop, the double pole peaking of the open-loop output impedance can be completely canceled out, and the constant output impedance with a fixed 180° phase shift in the control loop bandwidth can be achieved. This output impedance characteristic is preferred for the adaptive voltage position (AVP) design to change the output voltage according to load current to save the output capacitor. With a simple design procedure, the DE-DRC can not only have low noise susceptibility, but also achieve a fast transient response. The architecture of the proposed DE-DRC is introduced in Section

II, with the small signal model and simulation results showing the advantages of this control method. In Section III, the detailed circuit implementation is introduced. The circuit using the DE-DRC is tested and the experiment results are presented in Section IV. Section V gives the conclusion of this DC-DC Buck converter.

II. ARCHITECTURE OF DE-DRC

The architecture of the *DE-DRC* is shown in Fig.1. The sensing resistors, R_{s1} and R_{s2} , sense the output voltage (V_{out}) with a sensing gain of H . The voltage difference between V_{sen} and V_{ref} is amplified by the positive and negative differential difference amplifiers (DDA_p and DDA_n) to generate two differential error voltages (V_p and V_n). R_r and C_r are connected between the switch node and the output of the DDA_p to generate the Control Ripple Voltage (V_{rd}). This V_{rd} consists of two signals. One is the duty ripple (V_r) which is a low pass filtered signal from switch node voltage (V_{sw}) by R_r - C_r , and the other is the positive control voltage (V_{cp}) which is a high pass filtered signal from V_p by C_r - R_r . V_{rd} is compared with the negative control voltage (V_{cn}) which is equal to V_n , to generate the trigger signal for the On-Pulse Generator.

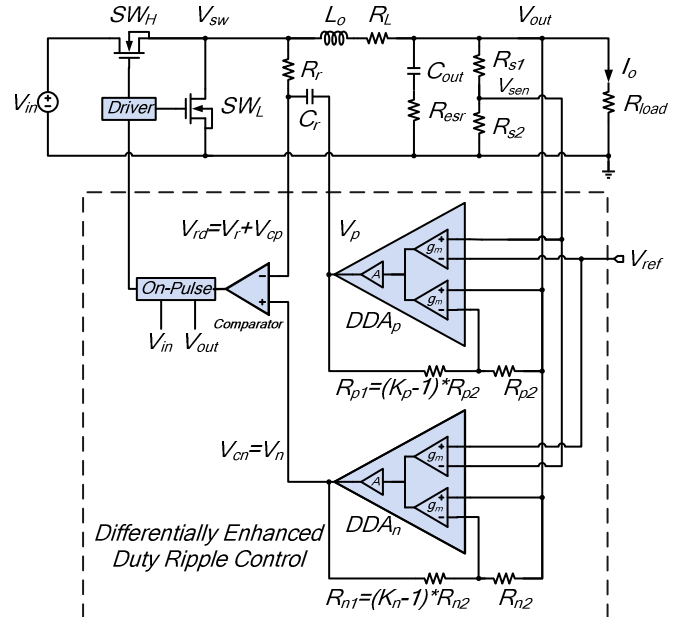


Fig. 1. Architecture of Differentially Enhanced Duty Ripple Control

The positive and negative DDA gains can be accurately set by the ratio of R_{p1}/R_{p2} and R_{n1}/R_{n2} , respectively. The differential difference amplifier [3-5] is an extension of the basic concept of operational amplifier. In the DDAs, two trans-conductance (g_m) blocks are identical and can generate two currents from the two differential voltages with the same

trans-conductance. These two currents are added together at the input of the voltage buffer. The function of the positive DDA is to amplify the voltage difference between V_{sen} and V_{ref} with a fixed gain (K_p) and add the amplified voltage with V_{out} . When the bandwidth of the DDA is much higher than the control loop bandwidth, the DDA can be treated as an ideal amplifier, and V_p can be expressed as,

$$V_p = K_p \times (H \cdot V_{out} - V_{ref}) + V_{out} \quad (1)$$

Similarly, the output of the negative DDA is,

$$V_n = -K_n \times (H \cdot V_{out} - V_{ref}) + V_{out} \quad (2)$$

Where, the sensing gain (H), the positive DDA gain (K_p), and the negative DDA gain (K_n) are expressed as,

$$H = \frac{R_{s2}}{R_{s1} + R_{s2}}, K_p = \frac{R_{p1} + R_{p2}}{R_{p2}}, K_n = \frac{R_{n1} + R_{n2}}{R_{n2}} \quad (3)$$

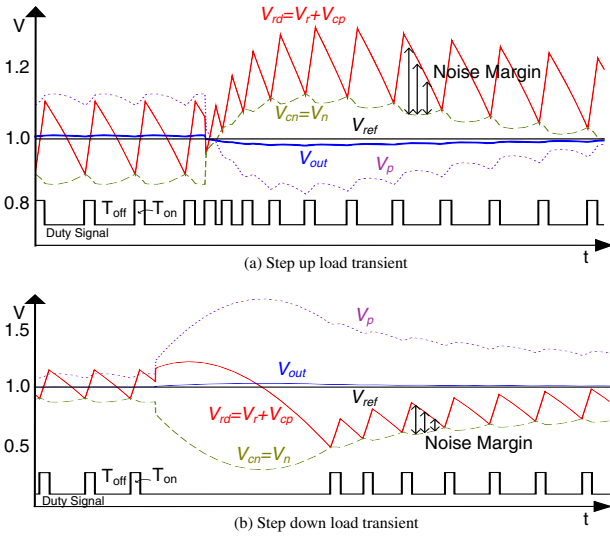


Fig. 2. Step up and step down load transient simulation

The simulated transient waveforms of the DE-DRC are shown in Fig. 2 with $H=1$. During steady-state, when the control ripple (V_{rd}) reaches V_{cn} , on-pulse generator will send out one on-pulse. The good noise immunity characteristics can be observed from the transient simulation results. The noise margin is the distance between V_{rd} and V_{cn} , and the amplitude of the noise margin is higher than 200mV, which is much larger than the tens millivolte noise margin of the CMC and the hysteretic control.

In Fig. 2 (a), V_{out} drops during a step up load transient, and the DDAs make V_p go down and V_n go up. The output signal of the DDA_p (V_p) goes through R_r - C_r network. As a result, the up slope of the control ripple voltage during the on-time is smaller than the steady-state case, and the down slope during the off-time becomes larger. With the slope changes and the higher V_{cn} , the duty cycle increases and the V_{out} is pulled back to the target value. During a step down load transient, the increased V_p and decreased V_n make the duty cycle smaller like Fig. 2 (b), and the V_{out} is kept at the target value.

By adding the R_r - C_r network, the AC part of the inductor current information is added into the control loop as a form of the duty ripple voltage V_r . The inductor current is indirectly

controlled and no longer a free variable in the buck converter system. As a result, the loop transfer function ($T(s)$) changes from a second order to a first order function, which is always stable even without any compensation. K_n of the negative DDA can be used to change the DC Gain of the $T(s)$, and K_p can adjust the high frequency part of $T(s)$ to achieve high control bandwidth and fast transient response.

A small signal model of DE-DRC based on average method including the sample and hold effect is derived and compared with the simulation result of SIMetrix/SIMPLIS simulator. The results are shown in Fig. 3. After the control loop is closed, the second order $G_{vd}(s)$ changes to the $T(s)$, which is first order system and doesn't need any compensation network to keep stable with enough phase margin. With different input and output voltages, the converter can still keep enough phase margin and bandwidth. So, DE-DRC can also provide good transient performance over wide input and output range.

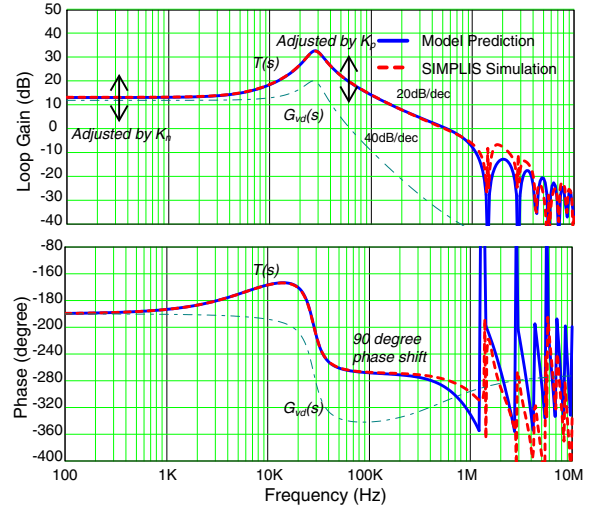


Fig. 3. DE-DRC control loop transfer functions

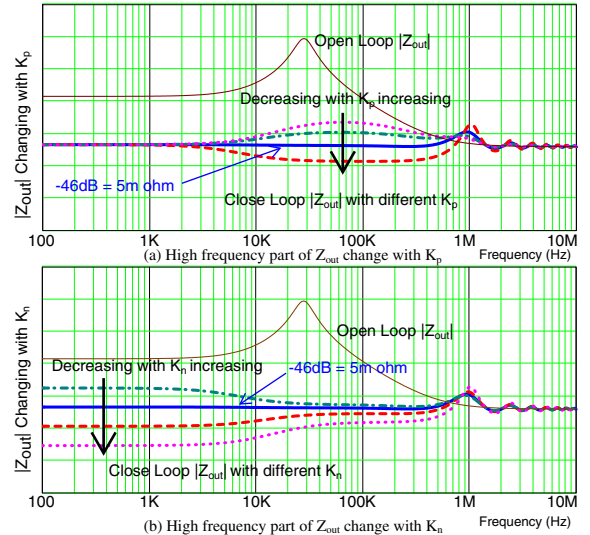


Fig. 4. Effects of K_p and K_n on the output impedance of DE-DRC

By changing the K_n and K_p , the low and high frequency part of the closed loop output impedance can also be well controlled. The double pole peaking in the open loop output

impedance is totally canceled out by the loop transfer function ($T(s)$) which also has a similar peaking at the resonant frequency of output filter. From Fig. 4, by choosing proper K_n and K_p , the output impedance with a $5\text{m}\Omega$ constant value and 180° phase shift within the control bandwidth can be achieved.

III. Implementation of DE-DRC Buck Converter

The adaptive on-time scheme is used in DE-DRC to keep the switching frequency constant over a wide input and output range. In order to eliminate the delay effect of comparator, two latched comparators with built-in offsets are used to generate the on-time. The input and output voltages are sensed by low pass filters in Fig. 5.

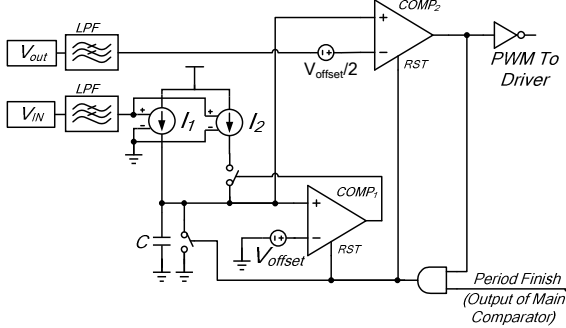


Figure 5. The on-pulse generator circuit

The timing sequence of the on-time generator is shown in Fig. 6. By using this circuit, the comparison delays (t_{delay}) and the built-in offsets (V_{offset}) of two comparators are canceled by each other and get the on-time shown in Equation (6). G_m is the trans-conductance of voltage controlled current sources, I_1 and I_2 .

$$T_{comp1} = C \frac{V_{offset}}{2 \cdot i} + t_{delay}, \text{ where } i = G_m \cdot V_{in} \quad (4)$$

$$T_{comp2} = T_{comp1} + \frac{C \cdot \left(V_{out} + \frac{V_{offset}}{2} - \frac{2i \cdot T_{comp1}}{C} \right)}{i} + t_{delay} \quad (5)$$

$$T_{on} = T_{comp2} = \frac{C}{G_m} \frac{V_{out}}{V_{in}} \quad (6)$$

The operation frequency of the buck converter is determined by Equation (7) if the conduction loss is ignored.

$$f_{sw} = \frac{V_{out}}{V_{in} \cdot T_{on}} = \frac{G_m}{C} \quad (7)$$

So, the switching frequency of DE-DRC buck converter will be constant with different input and output voltages.

The circuit of the differential difference amplifier used in this buck converter is shown in Fig. 7. The g_{m1} changes the input voltage $V_{p1}-V_{n1}$ into the drain current of M_{p6} , and M_{n5} , and g_{m2} changes the input voltage $V_{p2}-V_{n2}$ into the drain current of M_{p9} , and M_{n10} . The currents are summed at the source of M_{p16} and M_{n14} to drive the rail-to-rail output gain stage. This DDA can reach 45MHz bandwidth with 180uA current consumption.

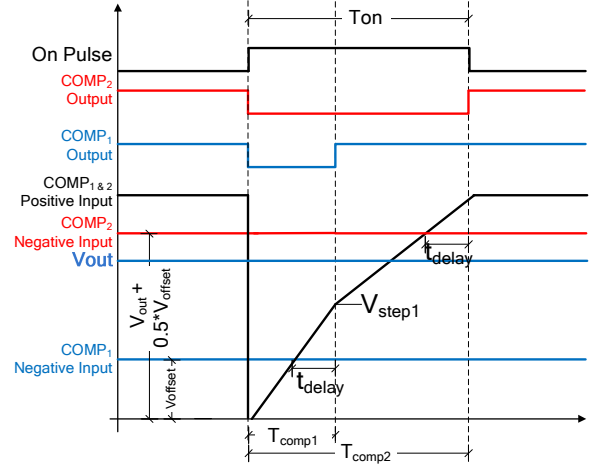


Fig. 6. Timing sequence of the on-time generator

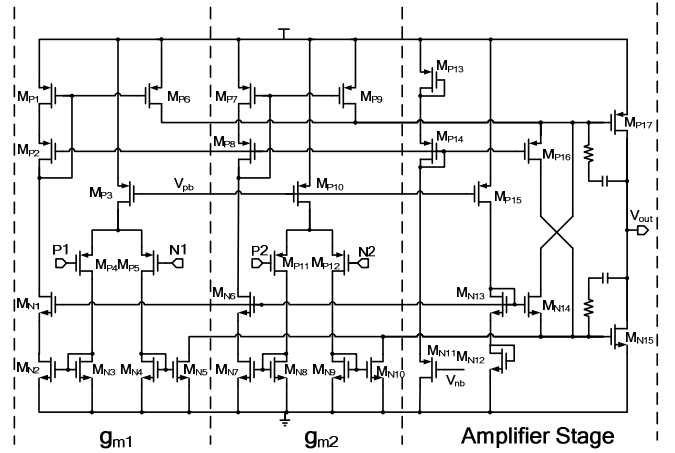


Figure 7. The differential difference amplifier circuit

IV. EXPERIMENTS

The integrated buck DC-DC converter with differentially enhanced duty ripple control was fabricated in TI's $0.5\mu\text{m}$ BCD process. The die photo is shown in Fig. 8. The control part of the chip occupies approximately 0.52mm^2 , which including a 20pF ripple capacitor C_r . The main control DDAs only measures $190\mu\text{m}$ by $250\mu\text{m}$.

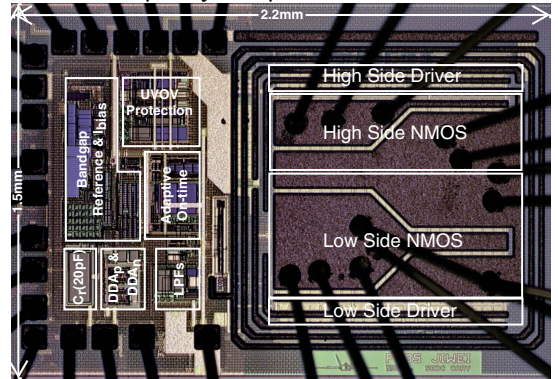
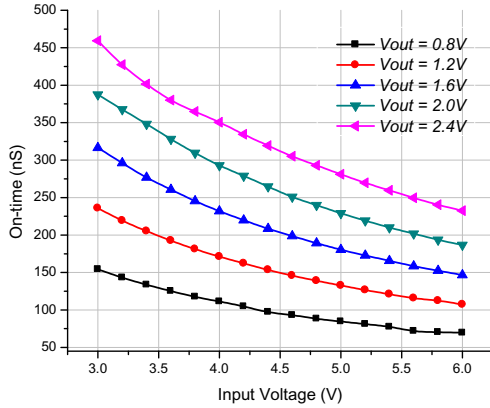


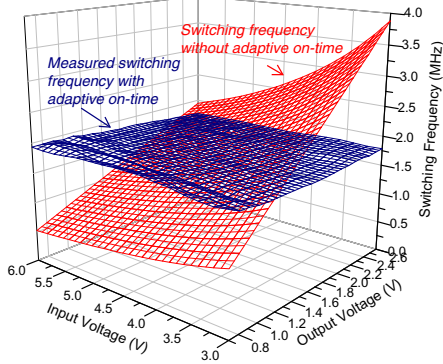
Fig. 8. Micro photograph of the chip

In order to evaluate the performance of the adaptive on-time generator and the switching frequency over large input and output range, the input and reference voltages are adjusted and the on-time width and switching frequency were measured

as shown in Fig. 8 (a) and (b). The input voltage changes from 3.0V to 6.0V, and the output voltage changes from 0.6V to 2.6V. With the adaptive on-time function, the switching frequency was kept at around 1.85MHz. The frequency change without adaptive on-time can be from 500KHz to 3.88MHz, which is also shown in Fig. 9. (b) for comparison. The detailed design parameters are shown in Table 1.



(a) Measured on-time change with different input and output voltage



(b) Measured switching frequency with different input and output voltage
Fig. 9. Measured on-time and F_{sw} over wide input and output range

TABLE 1. PERFORMANCE SUMMARY OF DE-DRC BUCK CONVERTER

Supply Voltage for control part	3.3V
Output voltage range	0.6V~2.6V
Input voltage range	3V ~ 6V
Maximum Load Current	1.1A
Peak Power Efficiency	86.8% @ 1A load
Output Inductor / Capacitor	470nH/80 μ F
Switching Frequency	1.98MHz ~ 1.75MHz @ 100mA load
Output impedance of converter	5m Ω
DDA Gain Parameters	$K_n = 10, K_p = 26, R_r = 80K$

In order to test the noise performance of this converter, the FastAcq function of the oscilloscope was used to check the switching jitters. The output voltage, inductor current, and switching node voltages are sampled hundreds times and the results were plot in an overlay mode. Fig. 10 shows good jitter performance, which proves the strong noise immunity of this buck converter. With 1A load change, the output transient response shows a 5m Ω pure resistance output impedance performance and fast transient response which is shown in Fig. 11.

V. CONCLUSIONS

This paper demonstrates a DE-DRC control scheme for DC-DC buck converter. The DC-DC converter was implemented in TI's 0.5 μ m BCD Process. The on-time pulse width was changed according to the input and output voltage to keep the switching frequency constant at 1.85MHz. Without any compensation, this buck converter can work over wide input and output range of 0.6V to 2.6V (V_{out}) and 3V to 6V (V_{in}). Design parameters K_n and K_p can be easily adjusted to change the output impedance value and get high control bandwidth. The transient response showed good transient response with 5m Ω pure resistance output performance, which implemented the AVP function. The large duty ripple voltage also provided good noise immunity for this converter.

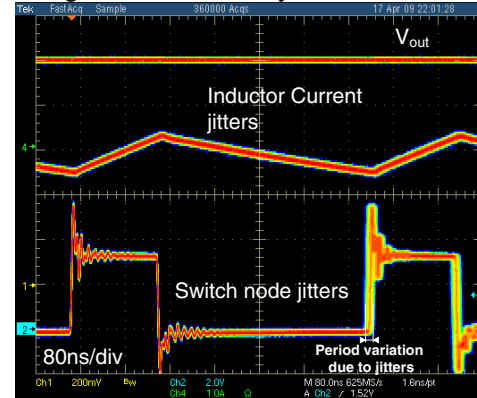


Fig. 10. Switching jitters waveforms

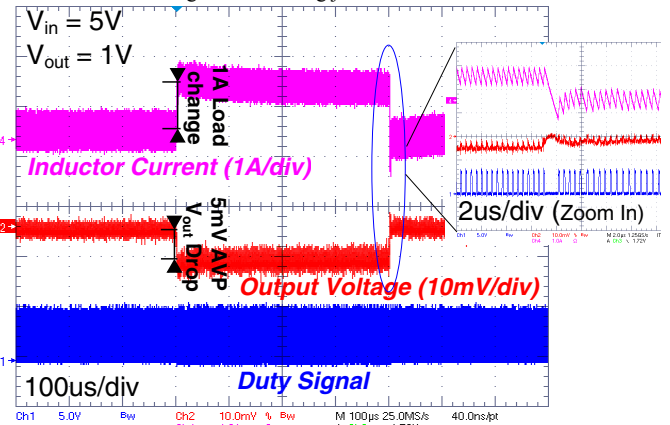


Fig. 11. The measurement of load transient change with AVP function

ACKNOWLEDGMENTS

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