

Minimizing the Supply Sensitivity of CMOS Ring Oscillator by Jointly Biasing the Supply and Control Voltage

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Abstract—A method to minimize the supply sensitivity of a CMOS ring oscillator is proposed through joint biasing of the supply and the control voltage. The technique can supplement a number of common supply rejection techniques. The proposed CMOS ring oscillator is designed and implemented with a charge-pump based phase-locked loop in 65-nm technology to demonstrate the robustness against the supply fluctuation. Taking advantage of the negative static supply sensitivity of the ring oscillator with proper combination of the bias voltages, the rms jitter of the 4-GHz output clock is reduced from 10.66-ps to 5.04-ps while subject to switching noise with magnitude of 2.5% of the supply voltage at 150-MHz. Furthermore, more than 4.5× of reduction in the power consumption is achieved.

I. INTRODUCTION

Voltage-controlled oscillators (VCOs) have been extensively used as a key part of phase-locked loops (PLLs) in high-performance microprocessors and high-speed digital communication systems for on-chip clock generators and clock recovery. The VCOs' jitter performance in these applications can impact the output clock's timing jitter which often limits the system performance. As more functional blocks are integrated onto a single IC, VCOs experience large supply noise because of the digital switching activities. The resulting timing jitter can be much larger than the jitter caused by the inherent device noise of the oscillator [1, 2]. Many methods have been adopted to suppress the supply noise seen by a VCO with the use of differential structures [3] and voltage regulators [4]. Other approaches compensate the VCO's intrinsic positive supply sensitivity with additional circuitry which has negative supply sensitivity [3, 5, 6].

This work proposes a technique that utilizes an inherent characteristic of many VCOs to reduce supply sensitivity. It has been observed that a VCO with the Lee-Kim delay cell [7] has positive supply sensitivity for most of the operating frequencies [6]. The VCO's supply sensitivity decreases at low supply voltage and even becomes negative at high operating frequencies. Thus, a bias point with zero static supply sensitivity exists for each operating frequency. The mechanism

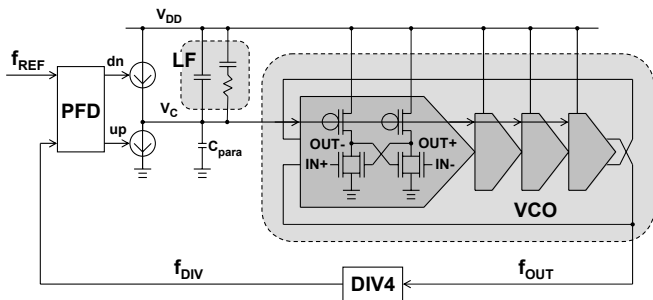


Fig. 1. Block diagram of the designed PLL.

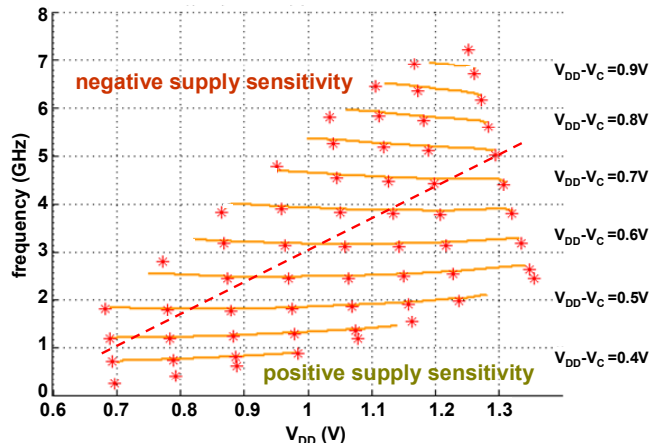


Fig. 2. Measured operating frequency vs. supply voltage with different $V_{DD}-V_C$.

is discussed in the first section of the paper. This optimal biasing can be adopted in conjunction with many other supply noise rejection techniques to further lower the supply sensitivity. This paper describes a possible implementation and measurement results. The results show additional benefits in power consumption.

II. THE VCO DESIGN

Fig. 1 shows the design of the VCO embedded in an analog PLL with the detailed schematic of the delay cell. NMOS transistors are used as the delay stage with PMOS transistors serving as current source loads. Cross-coupled pair is used to guarantee oscillation with differential outputs. The VCO's operating frequency is controlled by adjusting the PMOS transistors' current through the gate-to-source voltage V_{GS} . The delay cell is similar to the Lee-Kim delay cell. The NMOS-transistor cross-coupled pair is adopted for higher operating frequency [8].

Fig. 2 illustrates a variant of the typical K_{VCO} plot by showing how the oscillator's operating frequency is a function of the supply voltage (V_{DD}) for various control voltage bias of the PMOS transistor ($V_{DD}-V_C$). The measured results are plotted in the figure and match well the prediction from simulation. From this figure we notice that the VCO's supply sensitivity can be either positive or negative depending on different bias of the VCO's supply voltage and control voltage. The dotted line in Fig. 2 marks the transition (points of zero supply sensitivity).

On the right-hand side of the dotted line in Fig. 2, with a fixed V_{GS} of the PMOS transistors, as the supply voltage increases the operating frequency increases which corresponds to positive supply sensitivity. Fig. 3 shows the simulated oscillation waveform of the VCO running at 4.2-GHz with the supply

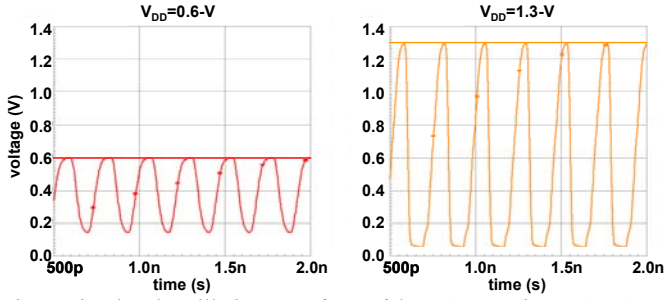


Fig. 3. Simulated oscillation waveform of the VCO running at 4.2-GHz with the supply voltages of 0.6-V and 1.3-V.

voltages of 0.6-V and 1.3-V. Note that as the supply voltage increases, the voltage swing also increases. The increase in frequency with supply is due to an increase in the NMOS current (larger V_{GS}) causing a faster falling edge. The PMOS current increases only slightly due to the finite output impedance. Because of the larger voltage swing, the rising transition is slower. The net impact on the frequency is the combination of the rising and falling edges. The increase in the current dominates over the increase in the oscillation amplitude and, as a result, causes positive supply sensitivity when the supply voltage is high.

On the left-hand side of the dotted line, where the supply voltage is low, the oscillation waveform is heavily clamped by the supply and reduced as the supply voltage decreases. Moreover, the lower bound of the oscillation waveform rises in order to increase the loop gain for sustaining the oscillation. With a smaller voltage swing, a constant PMOS current enables faster rising transitions. The higher lower-bound of the oscillation waveform leads to a smaller decrease in the average pull-down current. The net impact on frequency is again an increase with decreasing supply voltage.

Based on the previous paragraphs, the major reason for the oscillator to exhibit the negative supply sensitivity is the asymmetry in the pull-up and pull-down mechanism. The existence of the zero supply sensitivity and the magnitude of both the positive and negative supply sensitivity depend on the design parameters such as the P/N size ratio of the delay-cell transistors and the relative strength of the cross-coupled pairs. Fig. 4 shows the simulated operating frequency vs. supply voltage with different V_{GS} of the PMOS transistors in two cases with different P/N transistors size ratio. Fig. 4(a) shows the

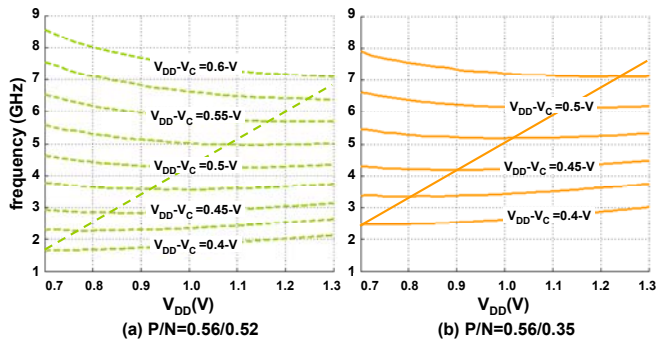


Fig. 4. The simulated operating frequency vs. supply voltage with different $V_{DD}-V_C$.

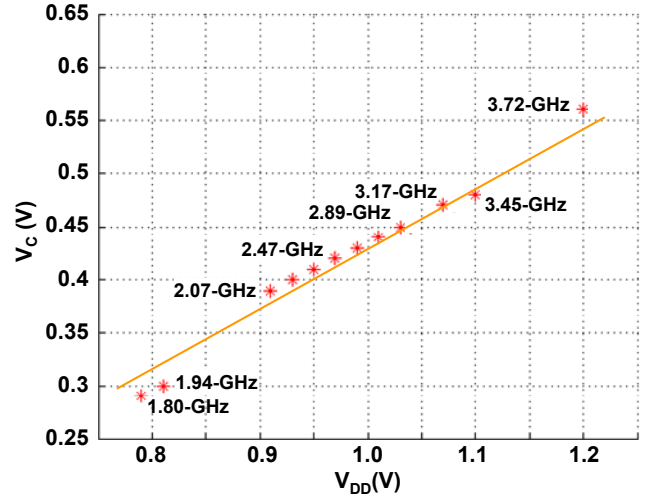


Fig. 5. The control vs. the supply voltage with zero supply sensitivity.

result with the P/N ratio of 0.56/0.52 while Fig. 4(b) shows the result with the P/N ratio of 0.56/0.35. The figures show that larger NMOS transistors shift the zero supply sensitivity towards the right and the resulting oscillator exhibits larger negative supply sensitivity. Note that increasing the NMOS transistors size has a tradeoff with the K_{VCO} because of the reduced frequency range. Zero supply sensitivity over a target operating frequency range can be achieved with proper sizing of the transistors.

III. SYSTEM IMPLEMENTATION

Either open-loop or closed-loop method can be employed to properly bias the oscillator's supply and control voltage in order to achieve low supply sensitivity. Fig. 5 shows the measured relationship between the supply voltage and the control voltage with the notation of operating frequency on top of the curve when the oscillator exhibits zero supply sensitivity. The result in Fig. 5 shows a roughly linear relationship. Therefore, a simple linear amplifier as shown in Fig. 6 can be adopted to change the supply voltage according to the control voltage while the control voltage is used as a port to change the oscillation frequency (or vice versa). On-chip timing jitter measurement circuitry [9] can be further adopted to measure the output clock's timing jitter and adjust the supply voltage to minimize jitter even in the presence of environmental change or dynamic supply noise.

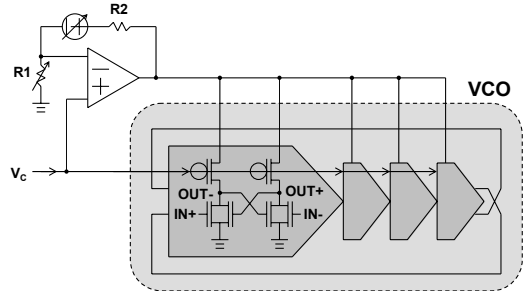


Fig. 6. Example of voltage biasing circuitry.

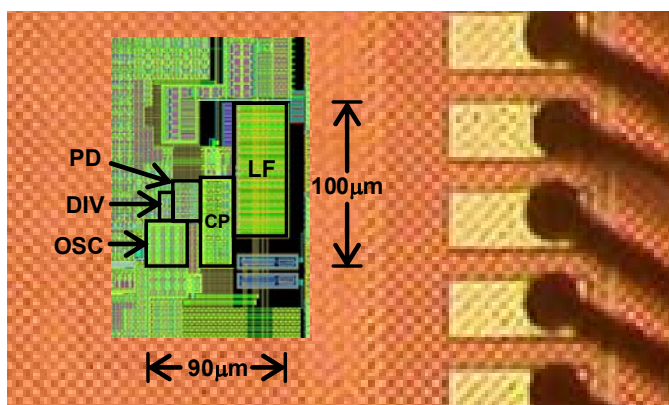


Fig. 7. Micrograph of the test-chip.

For an oscillator placed in a phase-locked loop as shown in Fig. 1, the V_{GS} of the PMOS transistors is controlled by the negative feedback loop such that the output frequency and phase track with the reference. Ideally, the control voltage follows the supply voltage in the presence of dynamic supply noise to maintain a constant $V_{DD}-V_C$. In practice, however, the V_{GS} of the PMOS is changed because of the parasitic capacitance between the PMOS gate and the ground as shown in Fig. 1. In the case shown, the change in the V_{GS} of the PMOS causes the operating frequency to increase as supply voltage increases. This positive supply sensitivity is limited often by careful layout. The proposed technique can further compensate the positive sensitivity by properly biasing the VCO in the region of negative supply sensitivity. Larger NMOS transistors can be used when designing the VCO to increase the region of negative supply sensitivity.

IV. MEASUREMENT RESULTS

The VCO with a charge-pump PLL is fabricated in 65-nm CMOS technology with nominal V_{DD} of 1.1-V. Fig. 7 shows the die micrograph overlaid with the layout picture. The entire PLL occupies $90\text{-}\mu\text{m}\times 100\text{-}\mu\text{m}$ with the VCO occupying

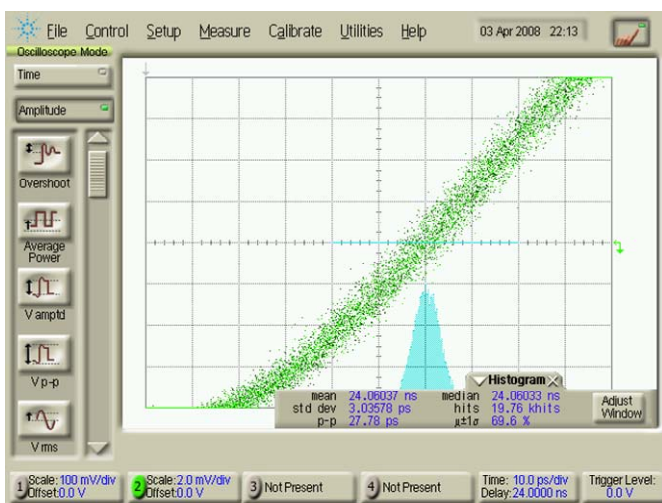


Fig. 8. PLL output histogram at 4-GHz with supply voltage of 1.04-V and $V_{DD}-V_C$ of 0.66-V.

TABLE I
SUMMARY OF THE TEST-CHIP PERFORMANCE

reference frequency	1-GHz					
output frequency	4-GHz					
loop bandwidth	$150\pm 5\text{-MHz}$					
supply voltage (V)	0.75	0.77	1.04	1.27	1.33	
supply current (mA)	10.29	11.15	18.92	25.20	26.65	
power (mW)	7.72	8.59	19.68	32.00	35.44	
quiet supply	rms jitter (ps)	3.20	3.10	3.04	3.11	3.21
100-MHz	rms jitter (ps)	3.43	3.62	4.02	4.56	5.99
130-MHz	rms jitter (ps)	4.23	5.71	6.54	7.17	8.06
150-MHz	rms jitter (ps)	5.04	6.00	6.60	8.59	10.66
200-MHz	rms jitter (ps)	3.73	3.64	3.78	4.57	4.99

$30\text{-}\mu\text{m}\times 30\text{-}\mu\text{m}$. Digital calibrations are built into the charge pump and the loop filter for adjustable loop characteristics. The PLL has an input reference frequency of 1-GHz, and an output clock at 4-GHz. A jitter histogram of the output clock from an oscilloscope is shown in Fig. 8. The VCO operates with the supply voltage of 1.04-V and $V_{DD}-V_C$ equal to 0.66-V, and the output clock has the rms jitter of 3.04-ps and the p2p jitter of 27.78-ps. However, the inherent noise of the oscilloscope is 2.5-ps rms and contributes a substantial amount of the measured noise.

The measurement results are summarized in Table 1. With quiet supply, the timing jitter is mostly due to the thermal noise in the devices. The jitter performance is worse when the supply voltage is high because of the poor symmetry between the pull-up and pull-down slope [10].

With the noise injection device switching on and off current out from the supply with the configuration as shown in Fig. 9 [11], noise with estimated amplitude of the 2.5% of the supply at different frequencies is injected onto the supply. Fig. 10 shows the measured output clock jitter when the circuit is biased at different supply voltages. The loop filter parameters such as the charge pump current, the loop filter resistance and the loop filter capacitance are adjusted such that the loop bandwidth is near $150\pm 5\text{-MHz}$ under different supply voltages. The noise from the supply experiences a band-pass filter to the clock output phase. As we can see, although the intrinsic noise performance tends to be better when the supply voltage is high,

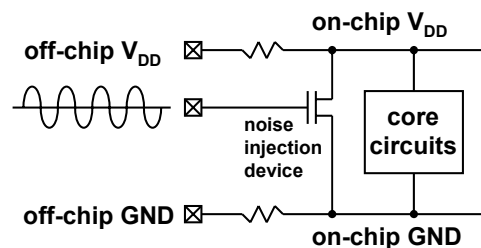


Fig. 9. Noise injection configuration.

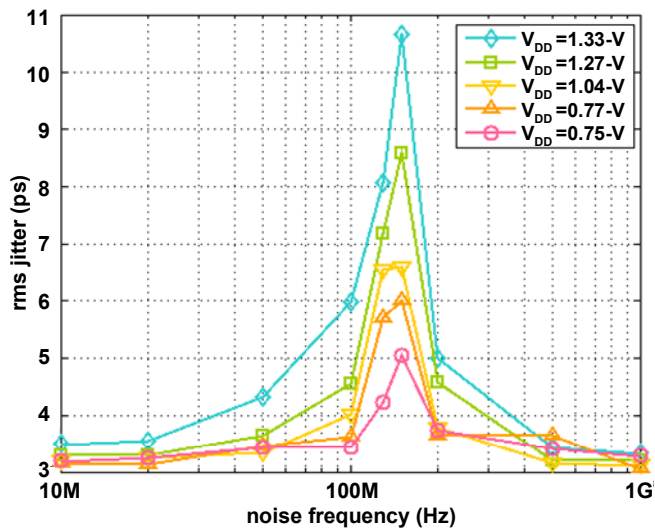


Fig. 10. Measured output rms jitter vs. switching noise frequency with different supply voltages.

the performance can be easily overwhelmed by the jitter due to the switching activities with the frequencies close to the loop bandwidth. By operating the VCO at lower supply voltage, the VCO is more robust to the supply fluctuation. The performance is improved as the oscillator is biased towards the optimum. In our design, while the supply sensitivity is substantially reduced, some residual sensitivity to the supply noise is consistently measured due to the large parasitic capacitance in our design. It is important to also note that the power consumption is dramatically reduced using the smaller supply voltage. As shown in Table 1, more than 4.5 \times of reduction in the power consumption is achieved when the supply voltage is decreased from 1.33V to 0.75V.

V. CONCLUSIONS

A ring oscillator is designed and implemented with a charge-pump based PLL in 65-nm CMOS technology. The supply sensitivity of the oscillator can be either positive or negative depending on the supply voltage and the operating frequency. For each operating frequency, there exists a set of bias voltages at which the VCO exhibits zero static supply sensitivity. The negative static supply sensitivity with low supply voltage can be utilized to compensate any positive supply sensitivity that may result from parasitic capacitance at the presence of dynamic supply noise. The measurement results show the oscillator's robustness against the supply fluctuation in the presence of switching noise.

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