

Best Regular Paper

Paper 23-1

A 0.077 to 0.168 nJ/bit/iteration Scalable 3GPP LTE Turbo Decoder with an Adaptive Sub-Block Parallel Scheme and an Embedded DVFS Engine, Chih-Chi Cheng, Yi-Min Tsai*, Liang-Gee Chen*, Anantha P. Chandrakasan, Massachusetts Institute of Technology, *National Taiwan University



Chih-Chi Cheng received B.S. degree and Ph.D. degree from National Taiwan University (NTU) in 2004 and 2009, respectively.

He is now with SoC design center of Quanta Computer where he is leading a team designing algorithms and circuits for computer vision and machine learning. Before joining Quanta in 2011, he was a Postdoctoral Associate in Microsystems and Technology Laboratories of MIT. In 2008, he was a visiting graduate student in Computer Science and Artificial Intelligence Laboratory of MIT.

Dr. Cheng is a winner of the 45th DAC/ISSCC Student Design Contest. He has been selected as one Outstanding College Youth in Taiwan. He received best annual dissertation awards from National Taiwan University and Taiwan IC Design Society. He is also a winner of Presidential Award in the Department of Electrical Engineering of NTU.