

A 120dB Dynamic Range 400mW Class-D Speaker Driver with 4th-order PWM Modulator

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Abstract--A 400mW class-D speaker driver is implemented in 65nm CMOS technology, using a 4th-order digital PWM modulator to eliminate the DAC and minimize the effects of analog imperfection. It achieves 120dB dynamic range with up to 88% power efficiency while driving an 8 Ω speaker load.

I. INTRODUCTION

Class-D speaker drivers are gaining more and more traction in audio applications requiring high efficiency. Battery driven mobile audio devices typically deliver speaker power of 1-Watt or less. Low quiescent current is needed to maximize power efficiency and battery life. The choice of the class-D topology and modulation technique impacts the efficiency and performance of the speaker driver. This paper presents a 400mW class-D speaker driver using a digital topology and pulse width modulation which achieves 120dB dynamic range (DR) and 88% peak efficiency, while only consuming 2mA quiescent current.

Class-D drivers can be implemented using analog and digital topologies, as shown in Fig. 1. Analog implementations consume static current for biasing and require a DAC which further increases power consumption. An advantage of the analog implementation is that it may use feedback from the output stage to improve performance [1]-[3]. An advantage of the digital implementation is that it only consumes dynamic power, and is capable of achieving lower quiescent current. The DAC that is necessary in an analog implementation is eliminated, and the modulator is shifted to the digital domain.

Class-D drivers can also be implemented either using pulse-width modulation (PWM) [1], [2] or pulse-density modulation (PDM) [3], [4]. Low pulse rate is preferred to reduce dynamic power and also to reduce the performance impact of switching errors. However, the drawback of a lower pulse rate is that the modulator loop feedback provides less error correction and is more difficult to stabilize. The PWM modulator provides performance advantages due to the fine timing

adjustment of the pulses and improved stability which enables high-order error correction loops. The pulse rate of a PWM modulator can be reduced significantly relative to that of a PDM modulator.

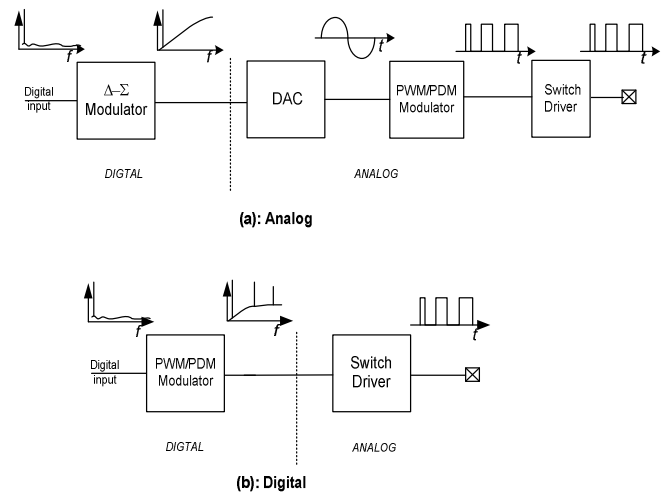


Fig. 1: Class-D amplifier topologies: (a) analog and (b) digital..

II. ARCHITECTURE

To achieve both high performance and low power consumption, a digital class-D speaker driver with a PWM modulator is desired. This paper presents a digital class-D amplifier with a 4th-order PWM modulator, as shown in Fig. 2. The amplifier consists of the 4th-order PWM digital modulator, two non-overlapping switch drivers, and a pair of MOSFET power switches for bridge-tie load (BTL). The digital class-D modulator converts the audio input to a PWM signal which drives the switch driver. The modulator bit-stream is re-timed by a low-jitter 24MHz clock at the input of the non-overlapping switch drivers. Non-overlapping switching drivers are used to prevent large crow-bar currents during switching. Large W/L aspect ratio of the power transistor is used to minimize the on-resistance of the devices to improve efficiency.

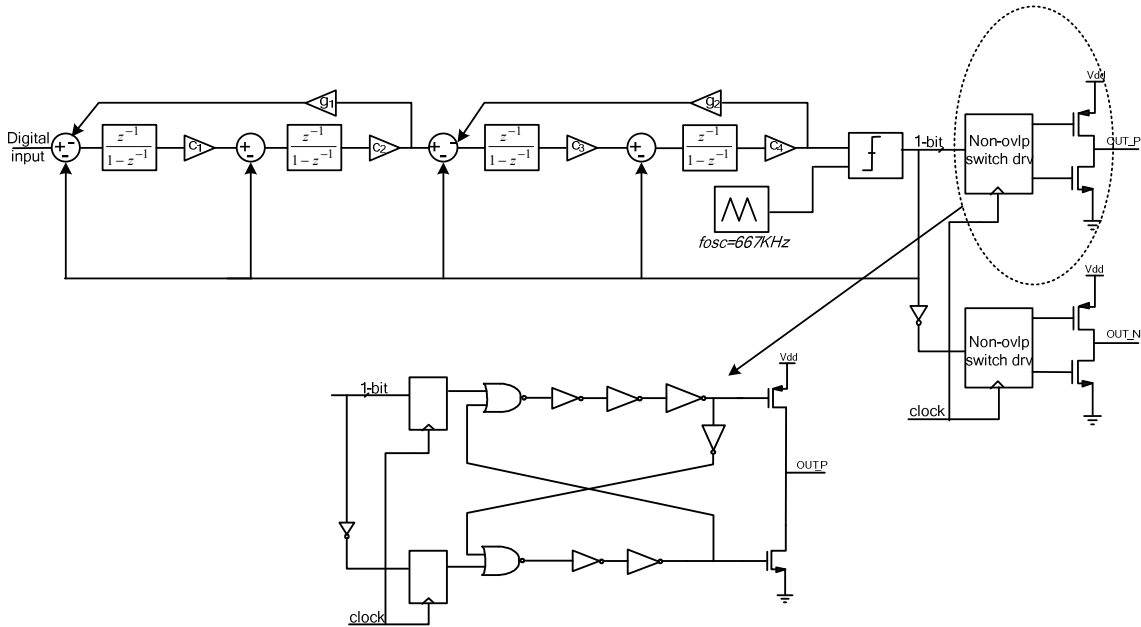


Fig. 2: Class-D modulator and output switch drivers.

III. MODULATOR IMPLEMENTATION

The design of the digital PWM modulator in Fig. 2 follows three major considerations. The first is the spectral shaping of the pulse and timing errors to enhance dynamic range (DR). The second is to maximize the input range for which the modulator is stable. The third is to reduce the switching rate as much as possible. A 4th-order structure was chosen to obtain sufficient spectral error shaping while also maintaining stability over a wide range of input amplitude. This modulator is designed to achieve 120dB DR and maintain high performance within -0.7dB of the full-scale amplitude. The lower limit of the switching rate is restricted by the unity-gain frequency of the loop transfer function. Specifically, the switching rate must be greater than π times the unity-gain frequency of the loop transfer function [2]. Otherwise, the rate of change of the comparator input signal can exceed the rate of change of the triangle waveform and can saturate the modulator. In this design, the switching rate of the triangle waveform has been chosen to be 2π times greater than the unity-gain frequency of the loop transfer function. Further reduction of the switching rate either compromises the stability margin, or must be accommodated by reducing bandwidth and degrading the spectral shaping. The output of this digital PWM modulator is limited to one pulse per triangle waveform

cycle. The output pulse rate is 667KHz, which is reduced 36 times with respect to the 24MHz modulator clock frequency. In contrast, a typical PDM modulator output pulse rate is equal to the modulator clock frequency.

IV. DISCUSSION

Digital class-D speaker drivers are susceptible to performance degradation due to power supply noise modulation of the output pulse amplitude. PWM modulation reduces the impact of supply noise by mixing the supply noise out of the audio band. Fig. 3 shows the measured power supply rejection (PSR) vs. signal power with a 70mVrms sine wave applied to the analog supply. The PSR is the ratio of the measured output RMS voltage at the disturbance and mixed frequencies to the input RMS voltage, i.e., 70mVrms. At low signal levels, the modulation is effective in mixing the supply noise out of the audio band. At high output levels, the modulation becomes less effective.

Fabricated in a single-poly six-metal 65nm CMOS technology, the prototype class-D amplifier occupies an active area of 0.76mm². Fig. 4 shows the measured SNDR vs. input signal level. The DR is 120dB, which is limited by the DR of the digital PWM modulator. The supply noise, the clock jitter, and other analog non-idealities do not degrade the driver performance at low

signal levels. At large signal levels, the supply current flows through the non-zero source impedance of the supply, causing supply variation which further degrades the THD performance. The digital modulator is overdriven when the input goes above -0.7dBFS , and THD+N drops sharply. Fig. 5 shows the class-D power efficiency vs. output power, achieving 88% peak efficiency.

This design is the first class-D amplifier reported with a digital PWM modulator. Existing class-D amplifiers with digital PDM modulator utilize single-bit $\Sigma\text{-}\Delta$ modulation, requiring a high switching rate. In contrast, this design utilizes a digital triangle-wave oscillator to reduce the output pulse rate to only one pulse per cycle of the low-rate oscillator. This design also utilizes high-rate digital signal processing to enhance spectral error shaping and loop stability. This combination of high-rate signal processing with a low output pulse rate minimizes the impact of switching errors in the driver output stage, enables high DR, and maintains stability over a wide range of input amplitude.

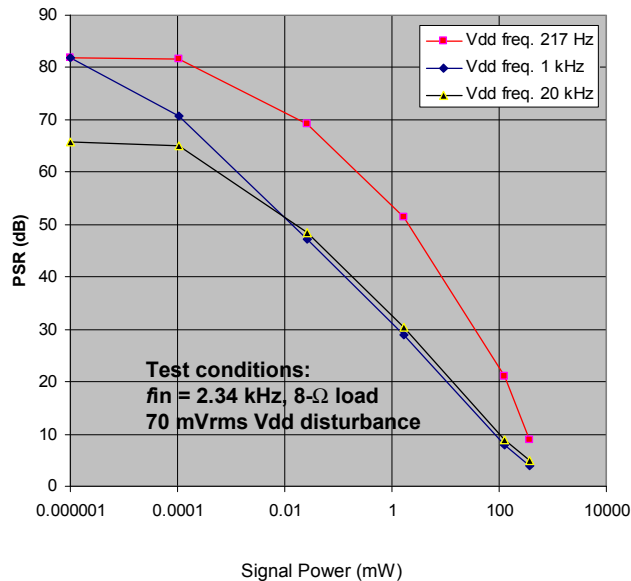


Fig. 3: Measured power supply rejection (PSR) vs. output power.

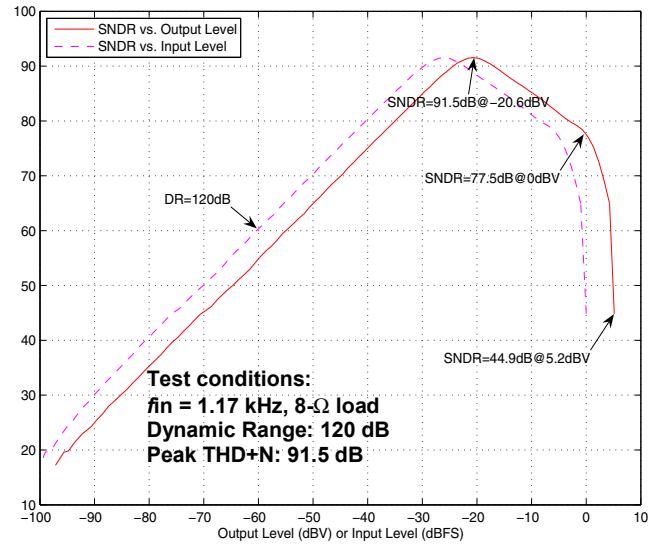


Fig. 4: SNDR vs. input signal level.

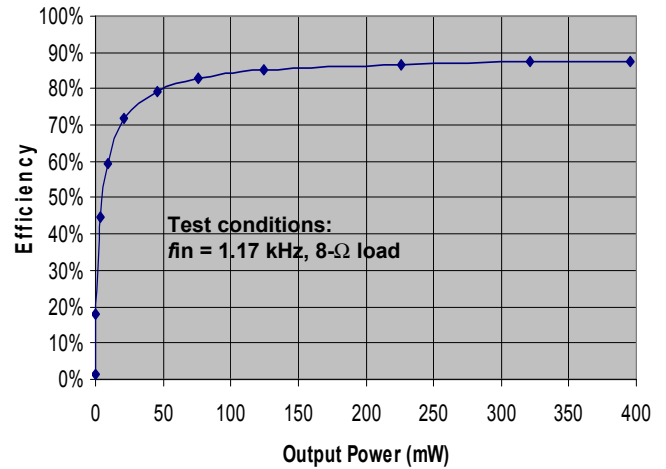


Fig. 5: Class-D power efficiency vs. output power.

VI. PERFORMANCE SUMMARY

A summary of key performance measures is listed in Fig. 6, including a comparison with existing state-of-the-art class-D amplifiers. This amplifier achieves 120dB DR, which is important for an audio driver due to the high sensitivity of human hearing to noise when audio signal power is low. A comparable class-D amplifier with a digital PDM implementation [4] has been reported with 83dB DR. Comparable class-D amplifiers with analog implementations [1]-[3] have been reported with up to 113dB DR.

PARAMETER	Test Conditions	Measured Performance	Comparison			
			Ref. [1]	Ref. [2]	Ref. [3]	Ref. [4]
Supply Voltage		3V (analog) 1.2V (digital)	35V (PVDD) 5V (analog) 1.8V (digital)	±30V (PVDD) 12V (analog)	12V (PVDD) 5V (analog) 5V (digital)	5V (analog) 5V (digital)
Process		TSMC65LP		HV-DMOS	HV-DMOS	0.5um CMOS
SNR		96 dB				
Peak THD+N		91.5 dB	94.9 dB	75.4 dB	98.4dB	<59dB
Max Efficiency	0 dBFS input	88%	81%	90%	88%	70%
Output Power	THD+N = 10%, 8-ohm load	0.4W	74W	50W	7.5W	1W
Quiescent Current	zero-input, analog	2 mA		27.5 mA	12 mA	
	modulator	0.4 mA			10mA	
Dynamic Range		120 dB	113 dB	103 dB	106 dB	83 dB
PSR	zero-input	82 dB				>90dB
Output RMS Noise	zero-input	1.7 uV		200 uV	50 uV	
Frequency Range		20 - 20,000 Hz	20 - 20,000 Hz	20 - 20,000 Hz	20 - 20,000 Hz	20 - 20,000 Hz
Die area		0.76 mm ²	11.5 mm ²	11.0 mm ²	10.2 mm ²	12 mm ²

Fig. 6: Measurement summary and performance comparison.

This digital PWM class-D amplifier provides low quiescent current, high power efficiency, and high performance, fitting well to address the ever increasing demand for small low-cost mobile audio devices in the electronics industry. The die micrograph is shown in Fig. 7.

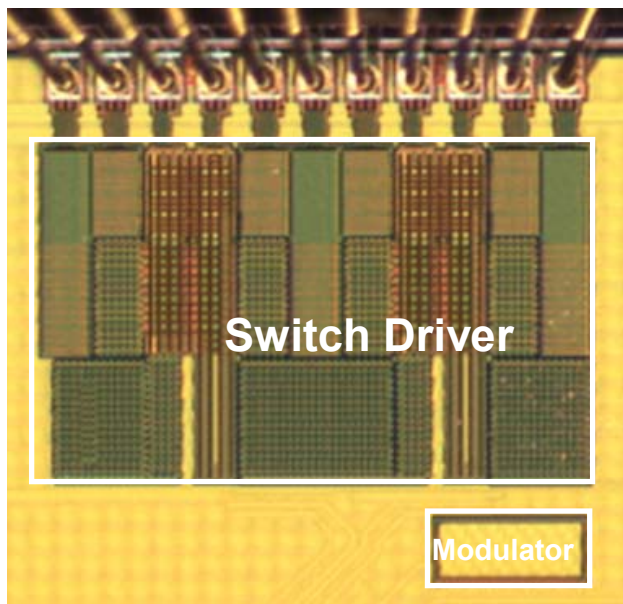


Fig. 7: Die micrograph.

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