

Clocking Circuits for a 16Gb/s Memory Interface

Ting Wu, Xudong Shi, Kambiz Kaviani, Haechang Lee, Jung-Hoon Chun,
TJ Chin, Jie Shen, Rich Perego, and Ken Chang
Rambus Inc. 4440 El Camino Real, Los Altos, CA 94022, USA

Abstract - 8GHz clocking circuits for a 16Gb/s/pin asymmetric memory interface [1] are described. A combination of an LC-PLL and a ring-PLL achieves improved jitter performance for multiple phase outputs with a wide frequency range. A direct phase mixer and a digitally controlled duty-cycle corrector (DCC) are time-multiplexed between transmitter (TX) and receiver (RX), thereby reducing area and power. The prototype chip implemented in a 65nm CMOS technology has measured 734fs RJ (rms) at the TX output when operating at 16Gb/s.

I. Introduction

Driven by today's advances in personal computing, game consoles, mobile phones, and HDTV, the demand for high bandwidth memory interfaces has been steadily growing. As the performance demands of memory interfaces increase, clock generation and distribution techniques are among the most important design considerations [2]. To meet the market requirements, clocking circuits must achieve both low jitter and low power at an increasingly higher data rate.

In this paper, we present a high-performance clocking architecture featuring dual-loop PLLs on the controller side of an asymmetric memory interface [1]. An LC oscillator based PLL produces a low jitter high frequency clock as the reference clock of a ring oscillator based PLL. The ring-PLL then generates quadrature phase outputs, which drive phase mixers for clock phase adjustments. As a consequence, the overall architecture achieves improved jitter performance for multiple phase outputs with a wide frequency range.

To simplify the interface circuitry of the associated DRAM devices, the controller interface must ensure a $\sim 50\%$ duty-cycle with 360-degree phase adjustment at both TX and RX circuits. The phase adjustment and duty-cycle adjustment are achieved by using a direct phase mixer and a duty-cycle corrector (DCC), respectively. In this work, one phase mixer and one DCC are time-multiplexed between TX and RX on a bi-directional I/O. This reduces the area overhead significantly. However, to support minimal overhead memory read/write bus turnaround, a conventional analog DCC loop [3] is not adequate. In this work, a new digitally controlled DCC is employed to meet the requirement. As a result, both the phase mixer and the DCC are digitally controlled. Each uses a MUX to select the corresponding control code for TX and RX operations. The digital phase and DCC codes are determined during initial and periodic timing and duty-cycle calibrations, respectively.

This paper is organized as follows. In Section II, the architectural choices are considered and our clocking scheme is described. Section III presents the circuit techniques for area and power reduction. This is followed by measurement results in Section IV. Finally, Section V concludes this paper.

II. Clocking Architecture

There are several conflicting requirements for our clock generator: low jitter, a wide frequency range, and 360 degrees phase adjustment. Although ring oscillators have great flexibility to generate multiple phase outputs that are necessary for phase adjustment, their poor phase noise performance would not meet the timing budget for 16Gb/s operation. On the contrary, LC-tank oscillators have superior noise performance compared to ring oscillators. Unfortunately, they only produce two phases with a much narrower frequency range.

In order to provide a wide frequency range, an LC-VCO requires a large varactor or a bank of switched capacitors, resulting in reduced tank quality factor and increased AM-to-FM noise conversion. Quadrature phases can be achieved by either using a quadrature LC oscillator or dividing a 2x faster LC-VCO with a divide-by-2 divider. However, both approaches make the design of LC-VCO and PLL more challenging. A quadrature LC-VCO typically impairs phase noise. A 2x faster LC-VCO requires a 16GHz divider. It is also difficult to acquire accurate models for both active and passive devices operating at 16GHz frequency.

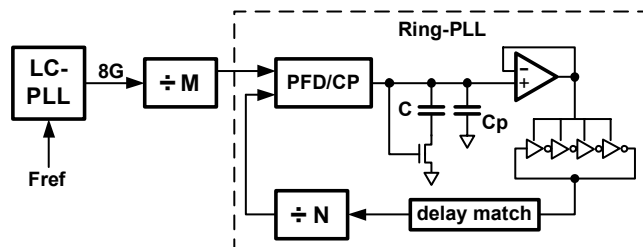


Fig. 1: Clocking architecture consists of an LC-PLL and a ring-PLL.

To regain the benefits of the LC-VCO PLL, we developed our dual-PLLs architecture. As shown in Fig. 1, an LC-PLL and a ring-PLL are cascaded. From the external reference clock, the LC-PLL generates a fixed output frequency, 8GHz, with a fixed divider ratio. This 8GHz output is fed to a divide-by-M divider which provides the reference clock for the ring-PLL. The ring-PLL has another programmable divider, divide-by-N, in the feedback loop to generate an $8\text{GHz} \times (N/M)$ frequency under lock condition. The overall output frequency range is limited by the tuning range of the ring VCO rather than that of the LC-VCO. In our work, M is set to be either 4 or 5, and another integer number N is programmable from 1 to 6. With this configuration, the clock generator is able to provide a frequency range from 1.6GHz up to 9.6GHz that is only limited by the ring oscillator.

Fig. 1 also shows the supply regulated ring-PLL, where the ring-VCO consists of four differential inverter stages. A larger ring bandwidth is allowed for the ring-PLL due to its

increased reference frequency. Consequently, the noise from the ring VCO is greatly attenuated. To optimize the noise performance of the whole clock architecture, the bandwidths of both LC-PLL and ring-PLL are carefully chosen. In this work, the LC and the ring PLLs have a loop bandwidth of approximately 3MHz and 80MHz, respectively. The supply regulator for the ring VCO has an approximately 1GHz bandwidth; hence, it has a negligible impact on the PLL dynamic. A replica compensated regulator [4] is adopted to achieve both high power supply rejection and low power consumption.

One drawback of our clocking architecture is the increased die area due to the additional ring-PLL. Although the increased ring-PLL bandwidth leads to a smaller loop filter capacitor, we still need to alleviate the area constraints. In previous designs, a second Charge Pump (CP) driving an opamp [3] was used to obtain an active loop filter resistor and an adaptive PLL bandwidth at the expense of area and power overhead. In this work, a MOS transistor operating in the linear region is employed as the loop filter resistor (Fig. 1). It can be shown that, when both the MOS transistor and the CP current are controlled by PLL control voltage, the PLL bandwidth is tolerant to process, voltage, and temperature (PVT) variations. Therefore, the ring-PLL area and power are reduced without compromising the PLL performance.

Only one LC-PLL is used for a whole data-byte, while each two data-bit bi-directional I/O circuits share one ring-PLL [1]. Other clocking circuits, including phase mixers, DCCs, and clock buffers, are placed between the two I/O circuits to shorten the high-speed clock wires. Reducing the power and area overhead of these circuits that are close to the I/O circuits are important. In the next Section, we describe our circuit techniques for power and area reduction.

III. Circuit Design

A. Time-multiplexing technique

Time-multiplexing is an efficient way to improve area efficiency by sharing common components among different functional blocks. On a bi-directional I/O link, the TX and RX operate at different times. Therefore, we can employ the time-multiplexing technique for each pair of TX/RX. In Fig. 2, the quadrature outputs from the ring VCO are fed to a phase mixer, whose differential outputs drive a duty-cycle corrector (DCC). The phase mixer and the DCC are time-multiplexed between the output clocks *tclk* and *rclk* for TX and RX, respectively. Each uses a MUX to select the corresponding control codes for TX and RX operations. Two separate clock buffers are used due to the different loading requirements for the TX and RX. With this architecture, the number of phase mixers and DCCs are halved, leading to a significant amount of area reduction. Further power reduction can be achieved by disabling the clock buffers that are not in operation.

Fig. 2 also shows our duty-cycle error correction loop consisting of the DCC and the clock buffers in the forward path and an m-to-1 MUX, a duty-cycle error detector, and a FSM in the feedback path. The duty-cycle error detector is essentially an analog integrator followed by a comparator. The integrator is a fully-differential charge pump with a common-

mode feedback circuit [3]. To reduce the additional duty-cycle distortion due to the detector, its input-referred offset should be minimized, leading to the use of large transistor size and an area penalty. Since the duty-cycle detection and calibration only happen periodically, the duty-cycle error detector is time-multiplexed among multiple clock signals. A novel duty-cycle error free MUX is used to select one clock signal during each individual duty-cycle calibration phase.

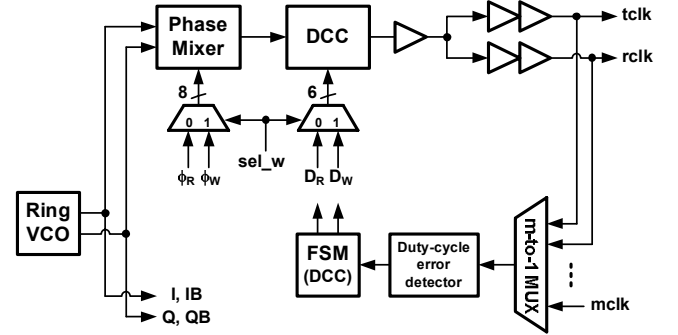


Fig. 2: Time-multiplexed phase mixers and DCCs between TX and RX, and time-multiplexed duty-cycle error detector among multiple clocks.

B. Direct phase mixer

The phase mixer is used to adjust the output clock phase with respect to the input over 360 degrees. Traditional phase mixer [3] consists of a MUX that selects two phases from the quadrature phases and a phase interpolator that interpolates between the chosen phases. However, this type of the phase mixer suffers from charge-injection and clock feed-through from the input devices, resulting in degraded phase linearity.

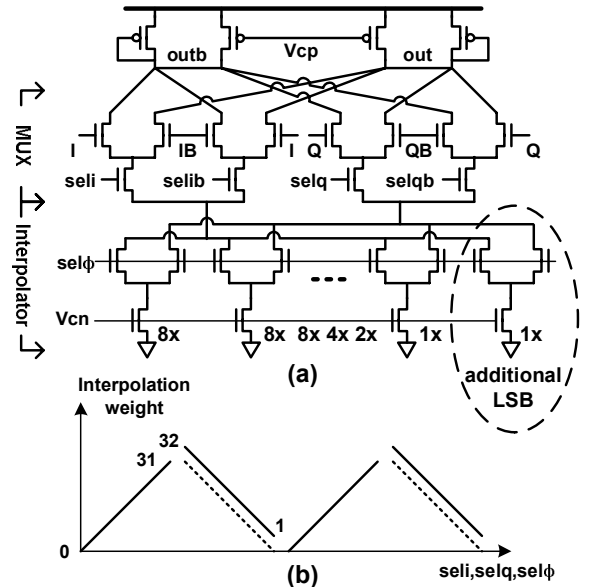


Fig. 3: (a) Simplified schematic of direct phase mixer. (b) Conceptual phase transfer of the phase mixer in (a) in comparison with the traditional results (shown in the dashed lines).

To address this issue, a direct phase mixer depicted in Fig. 3(a) is employed in this work. The MUX and the phase interpolator are cascaded rather than being cascaded, similar to [5]. By doing so, each output node is connected to four

transistors that are driven by the quadrature phases. Therefore, the overall injected charge at the output remains the same and is no longer dependent on the chosen phases, resulting in improved phase linearity. Additionally, the cascoded circuits reduce total power consumption. Since the cascoded switches operate in the deep-linear region, the resulting supply voltage headroom reduction is very small.

To avoid having the same interpolation weights across each quadrant boundary, in Fig. 3(a), we added one LSB current cell. The control bit for this additional LSB is only varied at each phase boundary. Fig. 3(b) shows the resulting phase transfer curve (shown in the solid lines) in comparison with the traditional one (shown in the dashed lines). The interpolation weights vary from 0:31 LSBs to 32:1 LSBs rather than from 0:31 LSBs to 31:0 LSBs. As a result, two consecutive phase outputs at the phase boundaries are made different by one LSB. In this work, one LSB is defined as $0.5UI/32$, or 976fs at 16Gb/s.

In order to guarantee phase linearity across frequency range, both the phase mixer and its input buffers are biased based on the ring-PLL control voltage.

C. Digitally controlled Duty-Cycle Corrector (DCC)

The digitally controlled DCC is shown in Fig. 4. A small swing differential input signal from the phase mixer goes through an AC-coupled capacitor and drives an inverter with a feedback resistor [6]. The feedback resistor DC biases the inverter input to its switching point. Therefore, the input signal is amplified to a full CMOS output after 3 inverter stages. In addition, any duty-cycle error of the input signal will be corrected by the first inverter stage via the feedback resistor [7]. Consequently, this circuitry combines both functions of low-to-high swing amplification and duty-cycle error correction, resulting in a significant area reduction.

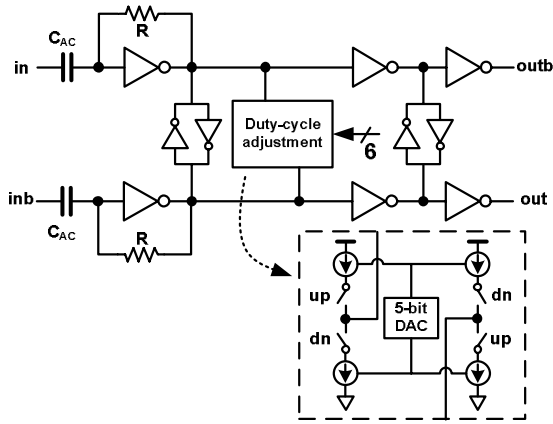


Fig. 4: Digitally controlled duty-cycle corrector (DCC).

Given an input with $\pm 10\%$ duty-cycle error, simulation results show that the resulting duty-cycle error at the output is reduced to $\pm 3\%$ over PVT variations. This unfortunately still falls short of our target of $\pm 1\%$ duty-cycle error for 8GHz clocks. To mitigate this problem, a digitally controlled duty-cycle adjustment circuitry is added at the output of the first inverter stage. The adjustment circuitry consists of two charge-pump circuits with one bit polarity control and a 5-bit

current-steering DAC. Depending on the polarity, the adjustment circuitry sources or sinks current at the first-stage output nodes, thereby applying a differential offset to the signal. As a result, the duty-cycle of the output is varied. The duty-cycle adjustment range is approximately $\pm 4\%$ with an LSB of 0.125%.

D. Duty-cycle error correction

The digital codes for the duty-cycle adjustment circuitry are determined by the duty-cycle error correction loop (Fig. 2). During one DCC calibration cycle, the duty-cycle error of a chosen clock signal is detected by the duty-cycle error detector which consists of an integrator and a comparator. The integrator accumulates the duty-cycle error over a number of clock phases. According to the integrator output, the comparator determines the polarity of the present duty-cycle error and feeds it to a Finite State Machine (FSM), which correspondingly increments or decrements the control value for the duty-cycle adjustment circuitry. This finishes one duty-cycle calibration cycle. In the next cycle, these updated control values are loaded to the adjustment circuitry, which varies the output duty-cycle toward its desired 50% value.

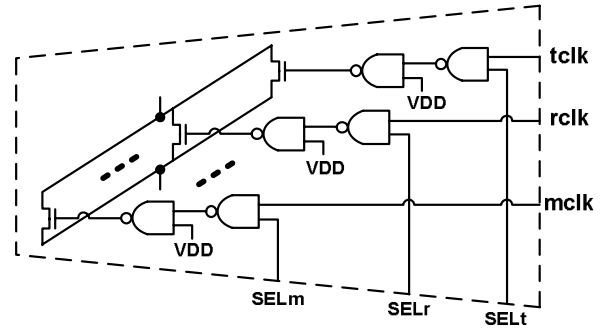


Fig. 5: Simplified schematic of the m-to-1 MUX used in the time-multiplexed duty-cycle error correction loop (Fig. 2).

To relax the area constraint, the duty-cycle detector is time-multiplexed by multiple clock signals with an m-to-1 MUX. In this work, m is 5 with two pairs of tclk/rclk and one feedback clock as the MUX input. Care should be taken to minimize both extra duty-cycle error (introduced by the MUX and the detection circuit) and coupling between the input clocks. To mitigate this extra distortion, we proposed a duty-cycle error free MUX as depicted in Fig. 5. It consists of multiple pairs of NAND gates for multiple input signals. In each pair, two identical NAND gates are cascaded. The first stage NAND gate is driven by a clock signal and the corresponding select signal, while the second stage driven by the first stage output and VDD. Through the two cascaded identical stages, any introduced systematic duty-cycle error from the first stage is cancelled at the second stage output. Therefore, the additional duty-cycle error due to the MUX is minimized. The outputs from the MUX drive the gate nodes of NMOS transistors connected in parallel in a CML buffer stage. Since there is only one active signal at the first stage output for all pairs of NAND gates, the coupling from other clock signals to the selected clock path which occurs at the CML buffer output is also minimized.

IV. Measurement Results

The prototype chip was fabricated in TSMC 65nm G+ CMOS technology with flip-chip package assembly. Fig. 6 shows the die photo of one data-byte and two data bits. The LC-PLL and ring-PLL occupy 0.048mm² (220μm×220μm) and 0.014mm² (280μm×50μm) die area, respectively. An approximately 0.01mm² area reduction was achieved by using the time-multiplexed components in the design.

Fig. 7 shows the measured TX output jitter histogram when a clock pattern running at 16Gb/s. The measured RJ (rms) and TJ (BER=10⁻¹²) at TX output are 734fs and 13.0ps, respectively. The power (from simulations) of the LC-PLL and one ring-PLL are 36mW and 21mW from a 1.1V supply voltage, respectively.

By changing the TX phase codes manually, the output phases are obtained and used to generate the INL of the phase transfer curve. As shown in Fig. 8, the direct phase mixer achieves a measured INL better than 4ps.

Fig. 9 shows the measured duty-cycle at the TX output when the DCC control code is varied manually. Without duty-cycle error calibration, the output duty-cycle is 51% (correspondingly at code 32). With the help of the calibration, the duty-cycle error is reduced to 0.2%. Across chips and measuring conditions, the calibrated duty-cycle measures from 48.5% to 51%.

Table 1 summarizes the performance of the clocking circuits in our prototype chip.

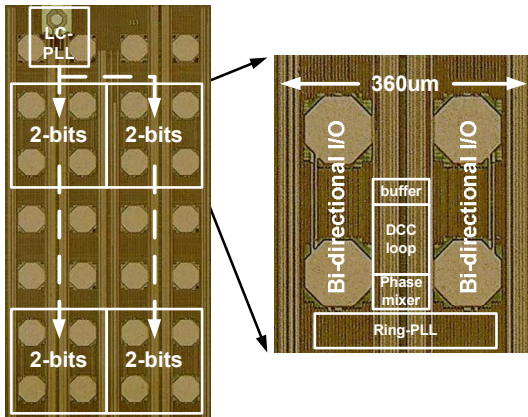


Fig. 6: Die photograph showing one data byte and two data bits.

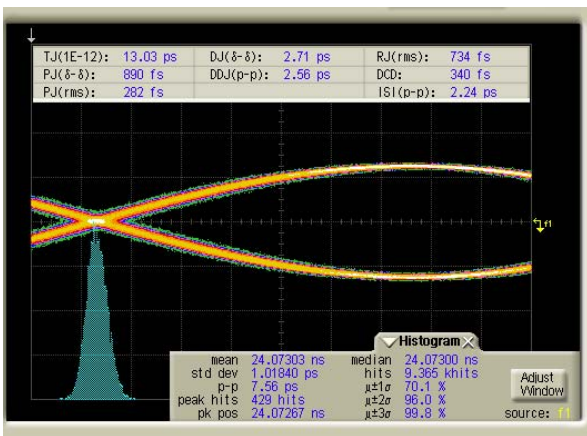


Fig. 7: Measured TX output jitter histogram when operating at 16Gb/s.

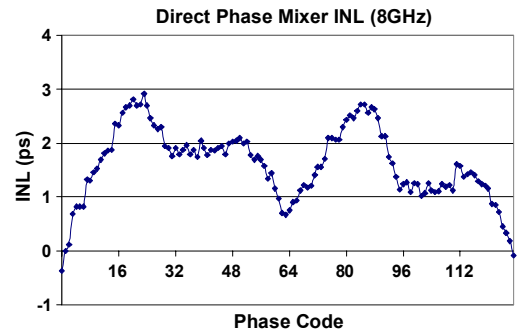


Fig. 8: Measured INL of the direct phase mixer phase transfer curve.

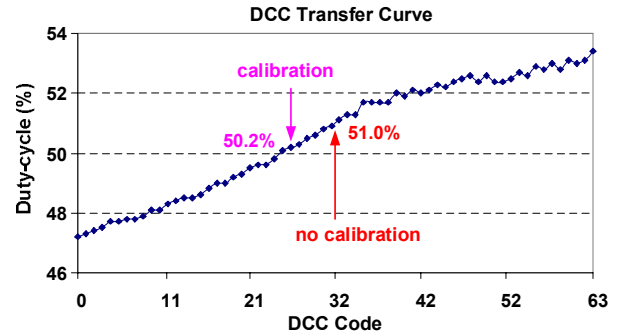


Fig. 9: Measured output duty-cycle vs. control code of the DCC. Duty-cycle calibration improved the duty-cycle error from 1% to 0.2%.

Table 1: Performance summary

Technology	TSMC 65nm G+
Supply voltage of clocking circuits	1.1V
Locking range of LC-PLL / Ring-PLL	8GHz ±5% / 1.6-9.6GHz
Power of LC-PLL / Ring-PLL	36mW / 21mW
TX RJ (rms) / TJ (BER=10 ⁻¹²)	734fs / 13.0ps
Phase linearity	INL < 4ps
Duty-cycle across chips	48.5% - 51%

V. Conclusions

We have presented 8GHz clocking circuits for a 16Gb/s/pin asymmetric link memory interface. The ring-PLL noise performance is improved by using an LC-PLL as a reference clock generator. The area constraints have been greatly alleviated by using time-multiplexed building blocks. Operating at 16Gb/s, the prototype chip has measured 0.73ps RJ (rms) jitter performance.

Acknowledgments

The authors gratefully thank Wendem Beyene and Chris Madden for testing assistance.

References

- [1] K. Chang, *et al.*, "A 16Gb/s/link, 64GB/s bidirectional asymmetric memory interface cell," to be appeared in *IEEE Symp. VLSI Circuits*, Jun. 2008.
- [2] D. Pham, *et al.*, "The design methodology and implementation of a first-generation CELL processor: a multi-core SOC," *IEEE Custom Integrated Circuits Conf.*, pp. 41-45, Sep. 2005.
- [3] K. Chang, *et al.*, "A 0.4-4Gb/s CMOS Quad transceiver cell using on-chip regulated dual-loop PLLs," *IEEE Symp. VLSI Circuits*, pp.88-91, Jun. 2002.
- [4] E. Alon, *et al.*, "Replica compensated linear regulators for supply regulated phase-locked loops," *IEEE JSSC*, vol. 41, pp. 413-424, Feb. 2006.
- [5] M. Meghelli, *et al.*, "A 10Gb/s 5-tap-DFE/4-tap-FFE transceiver in 90nm CMOS," *ISSCC Dig. Tech. Papers*, pp.213-214, Feb. 2006.
- [6] J. Savoj and B. Razavi, "A CMOS interface circuit for detection of 1.2Gb/s RZ data," *ISSCC Dig. Tech. Papers*, pp.278-279, Feb. 1999.
- [7] C. Menolfi, *et al.*, "A 16Gb/s source-series terminated transmitter in 65nm CMOS SOI," *ISSCC Dig. Tech. Papers*, pp.446-447, Feb. 2007.