

Session 22 - Millimeter-Wave ICs

Wednesday Afternoon, September 16
Oak Ballroom

Chair: Ramesh Harjani, University of Minnesota
Co-Chair: Alireza Shirvani, Marvell

Circuit techniques, building blocks and transceivers for mm-wave to terahertz wireless applications. Applications covered in this session include high-speed data communications, imaging, and RFID.

1:30 Introduction

1:35 **Paths to Terahertz CMOS Integrated Circuits (INVITED)**, Dongha Shim, Chuying Mao, Ruonan Han, Swaminathan Sankaran*, Eunyong Seok*, Changhua Cao**, Wojciech Knap[^] and Kenneth O, University of Florida, Gainesville, FL, *Texas Instruments Inc., Dallas, TX, **ST-Ericsson, [^]GES CNSR-U, Montpellier, France

A 140-GHz fundamental mode VCO in 90-nm CMOS and a 410-GHz push-push VCO in 45-nm CMOS, and a 125-GHz Schottky diode frequency doubler, a 50-GHz phase locked loop with a frequency doubled output at 100 GHz, a 180-GHz Schottky diode detector and a 700-GHz plasma wave detector in 130-nm CMOS have been demonstrated. Based on these, paths to terahertz CMOS circuits are suggested.

2:25 **A 60 GHz CMOS Combined mm-wave VCO/Divider with 10-GHz Tuning Range**, Burak Çatli and Mona Mostafa Hella, Rensselaer Polytechnic Institute, Troy, NY

This paper proposes the use of N-push operation for combining the functions of the VCO and dividers in the mm-wave frequency range. If employed in a PLL, the combined VCO/divider (C-VCO/D) would potentially provide wider tuning range than traditional mm-wave PLLs employing injection locked frequency dividers, thus exploiting the full range available in the 60GHz ISM band (57GHz-64GHz). The C-VCO/D is fabricated in 130nm IBM CMOS technology and achieves a tuning range from 55GHz-65GHz using a VDD=1.5V, I_{core}=20mA, and I_{buffer}=15mA. The C-VCO/D has a phase noise of 97.1 dBc/Hz at 1MHz Offset.

2:50 **A Sliding IF Receiver For mm-wave WLANs In 65nm CMOS**, Stefano Bozzola, Davide Guermandi*, Federico Vecchi, Matteo Repossi*, Massimo Pozzoni*, Andrea Mazzanti** and Francesco Svelto, Università degli Studi di Pavia, Pavia, Italy, *STMICROELECTRONICS, PAVIA, ITALY, **UNIVERSITÀ DI MODENA E REGGIO EMILIA, MODENA, ITALY

This paper presents an integrated receiver with on-chip LO for HDMI atmm-waves. Measured prototypes show a remarkable -115dBc/Hz phase noise at 10MHz from 64GHz while frequency tuning range is 12.5%. Other performances are:28dB gain, 9dB NF, 5GHz RF bandwidth, -26dBm 1-dB C.P., >60dB IRR with 80mW consumption.

3:15 PM BREAK

3:30 **A 24-GHz CMOS Sub-harmonic Mixer based Zero-IF Receiver with an Improved Active Balun**, Rahul Kodkani and Lawrence Larson, University of California at San Diego, La Jolla, CA

The design and implementation of a 24 GHz sub-harmonic mixer-based quadrature direct-conversion receiver is presented. The receiver includes an improved active balun and a LO octet phase generator with on-chip quadrature VCO. Fabricated in a 0.13 μm CMOS process, the RF and IF sections consume 48 mA and the LO section consumes 40 mA, using a 1.6V supply. The measured conversion gain of the receiver was 12.5 dB and Noise Figure of 7.4 dB.

3:55 **A mm-Wave Power Harvesting RFID Tag in 90nm CMOS**, Stefano Pellerano, Javier Alvarado Jr.* and Yorgos Palaskas, Intel Corporation, Hillsboro, OR, *Raytheon Company, El Segundo, CA

A mm-wave power-harvesting RFID tag is implemented in 90nm CMOS. Operation at mm-wave reduces antenna size and could allow antenna integration on-chip. This, together with power harvesting that can be used in lieu of a battery, can result in a CMOS-only tag with no off-chip components whatsoever. The tag harvests energy from the incoming mm-wave CW signal by the reader and then uses a 60GHz free-running oscillator to transmit back pulse-width modulated bursts. With 2dBm mm-wave input power, the tag transmits 5kb/s. The tag size is 1.3x0.95mm² including pads.

Session 23 - ESD Design Challenges

Wednesday Afternoon, September 16
Fir Ballroom

Chair: Manoj Sachdev, University of Waterloo
Co-Chair: Hong-Ha Vuong, LSI

With the scaling of technology the design of ESD protection circuits is becoming a challenge due to thinner gate oxide, shorter channel length, and shallower junctions.

1:30 Introduction

1:35 **ESD Design Challenges and Strategies in Deeply-Scaled Integrated Circuits (INVITED)**, *Shuqing Cao, Tze Wee Chen, Stephen G. Beebe* and Robert W. Dutton, Stanford University, Stanford, CA, *GlobalFoundries Inc., Sunnyvale, CA*

Challenges of design-window shrinkage in deeply-scaled silicon technologies are addressed by improving design, characterization, and modeling of I/O and ESD devices, and by developing ESD-performance co-design methodologies. Advanced ESD metrology methods are reviewed and their applications in reliability modeling are investigated. Package and wafer level CDM correlation issues are examined.

2:25 **Circuit Solutions on ESD Protection Design for Mixed-Voltage I/O Buffers in Nanoscale CMOS (INVITED)**, *Ming-Dou Ker and Chang-Tzu Wang, National Chiao-Tung University, Hsinchu, Taiwan*

This invited paper presents the ESD circuit solutions to protect the mixed-voltage I/O buffers in nanoscale CMOS processes against ESD stresses. The ESD protection scheme and the specific ESD clamp circuits with low standby leakage current have been successfully verified in nanoscale CMOS processes. Effective on-chip ESD protection scheme should be early started in the beginning phase of chip design in order to achieve good enough ESD robustness for IC products.

3:15 PM BREAK

3:30 **ESD Protection Circuit for 8.5Gbps I/Os in 90nm CMOS Technology**, *Hossein Sarbishaei and Manoj Sachdev, University of Waterloo, Waterloo, Canada*

In this paper we designed an ESD protected CML driver for 8.5Gbps data rate. ESD protection for this circuit is provided with DSCR. A detailed analysis is done on the impact of ESD protection on performance of the driver. It is shown that DSCR offers up to 2.7kV HBM protection with very small impact on performance of the driver

Session 24 - Memory Trends

Wednesday Afternoon, September 16
Pine Ballroom

Chair: Vikas Chandra, ARM
Co-Chair: Tom Andre, EverSpin Technologies

A wide variety of memory topics addressing design trends at advanced technology nodes are presented. Variation tolerant and low power approaches are discussed as well as their application to SRAM, DRAM, non-volatile memories and DDR5 interfaces.

1:30 **Introduction**

1:35 **A 40-nm Low-Power SRAM with Multi-Stage Replica-Bitline Technique for Reducing Timing Variation**, *Shigenobu Komatsu, Masanao Yamaoka, Masao Morimoto*, Noriaki Maeda*, Yasuhisa Shimazaki* and Kenichi Osada, Hitachi Ltd., Tokyo, Japan, *Renesas Technology Corp., Tokyo, Japan*

A multi-stage replica bitline technique for reducing access time by suppressing enable timing variation of a sense amplifier was developed. Applied to a 288-kbit SRAM of the 40-nm process node, this technique achieves 6.1% access time reduction by reducing the sense-amplifier timing variation by 43%.

2:00 **Low-Overhead, Digital Offset Compensated, SRAM Sense Amplifiers**, *Mudit Bhargava, Mark McCartney, Alexander Hoefler* and Ken Mai, Carnegie Mellon University, *Freescale Semiconductor*

Device variability in modern processes has become a major concern in SRAM design. In SRAMs that use low-swing bitlines, device variability can lead to high sense amplifier offsets, which limits the design scalability. A promising method for decreasing the offset is post-silicon tuning using low-overhead, digital offset compensation in the sense amplifiers. Measured results from a 4mm² testchip in 45nm bulk CMOS show that we can reduce sense amplifier offset sigma by over 5x.

2:25 **Asymmetric Sizing in a 45nm 5T SRAM to Improve Read Stability over 6T**, *Satyanand Nalam and Benton Calhoun, University of Virginia, Charlottesville, VA*

This paper describes a 5-transistor (5T) SRAM bitcell that uses a novel asymmetric sizing approach to achieve increased read stability. Measurements of a 32 kb 5T SRAM in a 45nm bulk CMOS technology validate the design, showing read functionality below 0.5V. The 5T bitcell has lower write margin than the 6T, but measurements of the 45nm 5T array confirm that a write assist method restores comparable writability with a 6T down to 0.7 V.

2:50 **An Ultra Low Power Non-Volatile Memory in Standard CMOS Process For Passive RFID Tags**, *Peng Feng, Yunlong Li and Nanjian Wu, Chinese Academy of Sciences, Beijing, China*

An ultra low power, 192bit, non-volatile memory is designed in a 0.18μm standard CMOS process for passive RFID tags. The memory includes a high efficiency charge pump and a register array, and can operate under a wide supply voltage and clock frequency range. The measured results indicate that, for the supply voltage of 1.2 volts, the current consumption is 1.8μA (3.6μA) at the read (write) rate of 1.3Mb/s (0.8Kb/s).

3:15 PM BREAK

3:30 **Small-Area High-Accuracy ODT/ODC by Calibration of Global On-Chip for 512M GDDR5 Application**, *Jabeom Koo, Gil-su Kim,*

The proposed on-die termination (ODT) calibration method is implemented by using a 0.18 μm CMOS technology. The proposed ODT can detect the impedance variations of each ODT/OCD independently with the help of the proposed local PVT variation sensor and can decrease the impedance mismatch error lower than 1% by calibration of global on-chip variation with small area overhead. The measured eye diagram area at 2Gbps is widened by 26% when the ODT is on. The random data rate used for testing the eye diagram is 2Gbps. The global impedance mismatch error is within 1% under the supply voltage variation from 1.7V to 1.9V. The ODT and its calibration circuit occupy 0.003mm² and 0.015mm², respectively. The power consumption of the calibration circuit is 10mW at 2Gbps.