Technical Sessions
Wednesday, September 22 - Afternoon

Session 23 – Power Optimization and Multi-Processing for SoCs

Wednesday Afternoon, September 22
Fir Ballroom

Chair: Aurangzeb Khan, EverSpin Technologies
Co-Chair: Rick Paul

In this session we present a variety of SoCs implementing multi-processor and power efficient designs, as well as power and security aware techniques.

1:30 **Introduction**

1:35
23-1 **A 0.077 to 0.168 nJ/bit/iteration Scalable 3GPP LTE Turbo Decoder with an Adaptive Sub-Block Parallel Scheme and an Embedded DVFS Engine,** *Chih-Chi Cheng, Yi-Min Tsai*, Liang-Gee Chen*, Anantha P. Chandrakasan, Massachusetts Institute of Technology, *National Taiwan University*

3GPP LTE requires a 100 Mbps of peak bandwidth, and the instantaneous throughput demand changes with different applications. Fixed sub-block parallel turbo decoding scheme introduces a bit-error rate (BER) performance drop when the block length is short. In this paper, an LTE turbo decoder implemented on a 0.66 mm^2 die in a 65 nm CMOS technology is presented. An adaptive sub-block parallel (ASP) decoding scheme that improves the BER performance by up to 2.7 dB while maintaining the same parallelism is developed. A DVFS engine combining with an early-termination scheme is also developed. It generates the supply voltage and the clock rate that lead to the lowest energy consumption given the output bandwidth requirement. The measured energy consumption is 0.077~0.168 nJ per bit per iteration and 0.39~0.85 nJ per bit.

2:00
23-2 **A Semi-Passive UHF RFID Tag with On-Chip Temperature Sensor,** *Wenyi Che, Dechao Meng, Xuegui Chang, Wei Chen, Lifang Wang, Yuqing Yang, Conghui Xu, Xi Tan, Na Yan, Hao Min, Fudan University*

A semi-passive UHF temperature sensor tag compatible with ISO 18000-6C protocol Revision-1 is presented in this paper. Novel power management techniques are proposed to prolong battery life, including two-stage wake-up detection, optimized rectifier design for wireless recharge, quasi CC-CV battery charging, and on-chip battery voltage surveillance. Both real-time temperature sensing and temperature log function are implemented with a bandgap based PTAT circuit. It has a -40~100 ℃ sensing range with ±1.6 ℃ accuracy. The tag is fabricated in 0.18 μm CMOS technology with EEPROM. Measured sensitivity and standby current are -23.7 dBm and 150 nA respectively.

2:25
23-3 **Intelligent NoC with Neuro-Fuzzy Bandwidth Regulation for a 51 IP Object Recognition Processor,** *Seungjin Lee, Jinwook Oh, Minsu Kim, Junyoung Park, Joonsoo Kwon, Joo-Young Kim, Hoi-Jun Yoo, KAIST*

Balancing the execution times of concurrent tasks in a multi-core processor is critical to achieving good performance scaling with increasing core count. However, this is difficult when the tasks' execution times are not known in advance. In this work, we propose an intelligent Network-on-Chip that performs bandwidth regulation using weighted round robin packet arbitration to balance the execution times of four Feature Extraction Clusters whose workloads vary depending on the input content. A neuro-fuzzy inference block, named the Intelligent Inference Engine, predicts the workload of each FEC, and assigns a priority weight to each

FEC channel. As a result, a 34% reduction in synchronization overhead due to unbalanced execution time was achieved, and the overall execution time was reduced by 11.5%.

2:50 23-4 **Reconfigurable Mobile Stream Processor for Ray Tracing,** *Hong-Yun Kim, Young-Jun Kim, Lee-Sup Kim, Korea Advanced Institute of Science and Technology*

This paper presents a reconfigurable mobile stream processor for ray tracing. The processor is implemented with 16mm^2 area in 0.13µm CMOS technology. The processor adopts a single instruction, multiple thread (SIMT) architecture in order to exploit instruction-level and thread-level parallelism. The SIMT architecture consists of twelve stream processors (SPs). A low hardware utilization caused by a branch divergence in SIMT architecture is addressed by reconfiguring the SPs between scalar SIMT and vector SIMT with negligible hardware overhead. A slim special function unit (SFU) with a table loader reduces the SFU area and look-up table access counts. Reusing previous result for a ray generator reduces its operations by up to 71.9%. The proposed processor achieves a peak performance of 6.3M rays per second while consuming 156mW.

3:15 BREAK

3:30 23-5 **A Dynamic Timing Control Technique Utilizing Time Borrowing and Clock Stretching,** *Kwanyeob Chae, Saibal Mukhopadhyay, Chang-Ho Lee, Joy Laskar*, *Georgia Institute of Technology*

This paper presents an effective method for preventing timing failures of a system by utilizing time borrowing and clock stretching, thereby eliminating a safety margin. A design with the proposed method can effectively reduce power consumption or increase the operating frequency, which extends the dynamic operating margin of pipelined systems.

3:55 23-6 **On Security of Cryptosystem-on-Chip (CoC) in Nano-metric Technology,** *Amir Khatib Zadeh, Catherine Gebotys, University of Waterloo*

Evolution of the security threat posed by power consumption is assessed and a quantitative analysis is validated by real attack on two test chips (180nm and 65nm). The effectiveness of a novel use of high threshold transistor assignment for security of crypto core is proposed in 65nm test chip. The presented approach provides a significant resistance against information leakage for nano-scaled crypto ICs.

Session 24 – MM-Wave and Beyond

Wednesday Afternoon, September 22
Pine Ballroom

Chair: Howard Luong, Hong Kong University of Science and Technology
Co-Chair: Cicero Vaucher, NXP Semiconductors

This session consists of circuits and design techniques for mm-wave applications and beyond, including RF front-end, amplifiers, and VCOS and dividers.

1:30 **Introduction**

1:35 24-1 **A 60-GHz 1.65mW 25.9% Locking Range Multi-Order LC Oscillator Based Injection Locked Frequency Divider in 65nm CMOS,** *Keita Takatsu, Hirotaka Tamura*, Takuji Yamamoto*, Yoshiyasu Doi*, Koichi Kanda*, Takayuki Shibasaki*, Tadahiro Kuroda, Keio University, *Fujitsu Laboratories, Ltd.*

A 60-GHz injection-locked frequency divider (ILFD) fabricated in 65nm CMOS and operating at 1.2V consumes 1.65mW, and has a measured locking range of 25.9% with 0dBm input power without a frequency-adjustment mechanism. The core ILFD area is 0.0157mm^2. The large locking range is attributed to the use of the multi-order LC oscillator topology. To the best of our knowledge, this ILFD achieves the highest FOM (locking range per unit power) in mm-Wave frequency dividers.

2:00
24-2
A V-Band Divide-by-Three Differential Direct Injection-Locked Frequency Divider in 65-nm CMOS, *Hsieh-Hung Hsieh, Fu-Lung Hsueh, Chewn-Pu Jou, Fred Kuo, Sean Chen, Tzu-Jin Yeh, Kevin Kai-Wen Tan, Po-Yi Wu, Yu-Ling Lin, Ming-Hsien Tsai, Taiwan Semiconductor Manufacturing Company, Ltd.*

In this paper, a novel circuit topology of CMOS divide-by-three injection-locked frequency divider is demonstrated. By using a differential direct injection pair with a LC-tank oscillator, the proposed circuit can perform the division ratio of three while the wide locking range is obtained. Based on the presented circuit architecture, a V-band frequency divider is implemented in 65-nm CMOS for demonstration. Operated at a supply voltage of 1.0 V, the divider core consumes a dc power of 5.2 mW. At an incident power of 0 dBm, the fabricated circuit exhibits an input locking range from 58.6 to 67.2 GHz. The measured output power and locked phase noise at a 1-MHz offset are -10 dBm and -127 dBc/Hz, respectively. To the authors' best knowledge, this work is the first CMOS V-band divide-by-three injection-locked frequency divider owning a locking range over 10% without any tuning mechanism reported to date.

2:25
24-3
V-Band Varactor-less Interpolative-Phase-Tuning Oscillators with Multiphase Outputs, *Sujiang Rong, Howard C. Luong, The Hong Kong University of Science and Technology*

A novel interpolative-phase-tuning technique is proposed in this work to implement varactor-less multi-phase LC oscillators with wide tuning range and low phase noise at millimeter-wave frequencies. Two phase-tuning CCO prototypes, one with 8-phase 50GHz outputs and another with 4-phase 60GHz outputs, implemented in a 0.13-micro-meter CMOS process and operated at 0.8-V supply, measure phase noise of -127.8dBc/Hz and -120.6dBc/Hz at 10MHz offset, FOMs of 186.4dB and 180.6dB, and FOMTs of 183dB and 179.7dB, respectively, which are much better compared to other state-of-the-art millimeter-wave oscillators using capacitive tuning.

2:50
24-4
Digital Phase Tightening for Millimeter-Wave Imaging, *Khoa Nguyen, Anthony Accardi, Helen Kim*, Gregory Wornell, Charles Sodini, Massachusetts Institute of Technology, *Massacusetts Instiute of Technology Lincoln Laboratory*

A new technique called digital phase tightening reduces phase noise from receiver front-end circuits to allow precise phase estimation for digital beamforming in millimeter-wave (MMW) imaging applications. This is achieved by leveraging the large ratio between the MMW carrier frequency and the relatively low frame rates in imaging applications. By mixing down to an intermediate frequency (IF) and then averaging over many samples to estimate the phase, we reduce phase noise and attain phase error of the MMW beamformer in the femtosecond range. A test chip demonstrating the phase tightening concept was designed and fabricated using 0.13µm CMOS, and we show that an RMS error of 3.5fs is feasible with this technique.

3:15 BREAK

3:30
24-5
A 77-GHz to 90-GHz Bidirectional Amplifier for Half-Duplex Front-Ends, *Joohwa Kim, Mehmet Parlak, James Buckwalter, University of California, San Diego*

A W-band, bidirectional constructive wave amplifier is proposed that eliminates the need for a T/R switch. The amplifier allows amplification of either a forward or backward traveling wave. The measured amplifier has a peak gain of 16 dB and bandwidth of 14.5 GHz at 90 GHz and the center frequency can be electronically controlled between 77 and 90 GHz. The circuit is fabricated in a 0.12 µm SiGe BiCMOS process, occupies an area of 0.47 mm^2, and consumes approximately 32 mA from a 2 V supply. To the author's knowledge, this is the first W-band, bidirectional amplifier in a silicon/silicon-germanium process.

3:55
24-6
280-GHz Schottky Diode Detector in 130-nm Digital CMOS, *Ruonan Han, Yaming Zhang*, Dominique Coquillat**, Julie Hoy^, Hadley Videlier**, Wojciech Knap**, Elliott Brown^, Kenneth O, University of Florida, *University of Texas at Dallas, **University of Montpellier II, ^University of California, Santa Barbara*

Abstract-A 2×2 array of Schottky-barrier diode detectors with an on-chip patch antenna and a preamplifier is fabricated in a 130-nm logic CMOS process. Each detector cell can detect the 25-kHz modulated 280-GHz radiation signal with a measured responsivity and noise equivalent power (NEP) of 21kV/W and 360pW/sqrt(Hz), respectively. At 4-MHz modulation frequency, NEP should be ~40pW/sqrt(Hz). At supply voltage of 1.2V, the detector consumes 1.6mW. By utilizing the detector, a millimeter-wave image is constructed, demonstrating its potential application in millimeter-wave and THz imaging.