

## Session 18 - Analog Techniques

Wednesday Morning, September 16  
Oak Ballroom

Chair: Sang-Soo Lee, Hynix Semiconductor America  
Co-Chair: Julian Tham, Arda Technologies

This session presents two invited papers on noise and signal integrity. A chopper amplifier, a voltage reference and a MOSFET-C filter are also covered.

9:00 **Introduction**

9:05 **Noise in Short Channel MOSFETs (INVITED)**, *John McNeill, Worcester Polytechnic Institute, Worcester, MA*  
18-1

For short channel MOSFETs, observed noise can be much higher than predicted from thermal noise analysis of long channel MOSFETs. The increase can be viewed as resulting from the current noise approaching a shot noise limit as carrier transit time becomes so small that thermal equilibration does not have time to occur.

9:55 **Auto Correction Feedback for Ripple Suppression in a Chopper Amplifier**, *Yoshinori Kusuda, Analog Devices, Wilmington, MA*  
18-2

It proposes a local feedback, named Auto Correction Feedback (ACFB), used in a chopper amplifier to suppress its offset related ripple. It nulls out amplifier's offset in DC domain which would otherwise become modulated ripple at the chopper amplifier's output, instead of filtering the ripple by a postfilter.

10:20 **A 0.5V 2.2pW 2-Transistor Voltage Reference**, *Mingoo Seok, Gyouho Kim, Dennis Sylvester and David Blaauw, University of Michigan, Ann Arbor, MI*  
18-3

A voltage reference using a depletion-mode device was designed in a 0.13 $\mu$ m CMOS process for achieving ultra-low power consumption and sub-1V operation without sacrificing temperature and supply voltage insensitivity. Measurements show a temperature coefficient of 3.6ppm/ $^{\circ}$ C, line sensitivity of 0.033%/V, power supply rejection ratio of -67dB, and power consumption of 2.2pW. It requires only two devices and functions down at V<sub>dd</sub>=0.5V with an area of 1350 $\mu$ m<sup>2</sup>. A variant for higher V<sub>out</sub> is also demonstrated.

10:45 AM **BREAK**

11:05 **Moving Signals On and Off Chip (INVITED)**, *Elyse Rosenbaum, Hyeon-Min Bae, Karan Bhatia\* and Adam Faust, University of Illinois at Urbana-Champaign, Urbana, IL, \*Finisar Corp., Champaign, IL*  
18-4

Today, signals being transmitted on and off chip have frequency spectra extending to 10 GHz and beyond. The parasitic impedance associated with the package and ESD protection circuit can distort a signal and must be carefully managed. An overview of methods for parasitic impedance mitigation and co-design is provided.

11:55 **A Widely-Tunable and Ultra-Low-Power MOSFET-C Filter Operating in Subthreshold**, *Armin Tajalli and Yusuf Leblebici, Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland*  
18-5

A wide-tuning range MOSFET-C low-pass filter is presented. The wide-tuning range in this filter has been achieved without using any switchable component. The filter cutoff frequency is tunable over 20Hz to 184kHz with a constant power consumption per cutoff frequency. Realized in 0.18 $\mu$ m CMOS technology, the filter occupies 0.09mm<sup>2</sup>.

## Session 19 - Test Methods and ICs for High-Speed Serdes

Wednesday Morning, September 16  
Fir Ballroom

Chair: Mike Li, Altera  
Co-Chair: Gordon Roberts, McGill University

This session addresses testing challenges associated with high speed I/O including adaptive equalization, loopback, and PLL bandwidth and peaking measurement.

9:00 **Introduction**

9:05 **Test Strategies for Adaptive Equalizers (INVITED)**, *Kwang-Ting (Tim) Cheng and Hsiu-Ming (Sherman) Chang, University of California, Santa Barbara, CA*  
19-1

This paper provides an overview of the test strategies for both continuous-time and digitally-assisted adaptive equalizers. Conventionally, an equalizer is characterized by the explicit measurement of the eye diagram at its output, which requires a lengthy testing time and is too costly for production testing. Design for testability and special test stimuli have been developed to facilitate circuit performance characterization and go/no-go production testing. In addition, for digitally-assisted

adaptive equalizers, digital signatures extracted from the tap coefficients in the digital adaptation unit can be used for performance prediction and fault detection.

9:55  
19-2 **Loopback Architecture for Wafer-Level At-Speed Testing of Embedded HyperTransport™ Processor Links**, *Alvin Loke, Bruce Doyle, Michael Oshima\*, Wade Williams\*\*, Robert Lewis\*\*, Charles Wang\*, Audie Hanpachern\*, Karen Tucker, Prashanth Gurunath\*, Gladney Asada\*, Chad Lackey, Tin Tin Wee and Emerson Fang\*, Advanced Micro Devices, Inc., Fort Collins, CO, \*Sunnyvale, CA, \*\*Austin, TX*

We present transceiver serial loopback that enables cost-effective wafer-level at-speed testing of HyperTransport™ I/O for processor die-to-die communication. Besides facilitating known-good-die testing, this feature provides observability of multi-chip module die-to-die links that are completely embedded without external pin visibility. We demonstrate production screening of 45-nm SOI-CMOS wafers at 6.4 Gb/s.

10:20 19-3 **An On-Chip All-Digital Measurement Circuit to Characterize Phase-Locked Loop Response in 45-nm SOI**, *Dennis Fischette, Richard DeSantis and John Lee, Advanced Micro Devices, Inc., Sunnyvale, CA*

An all-digital measurement circuit, built in 45-nm SOI-CMOS, enables on-chip characterization of phase-locked loop (PLL) response to a self-induced phase step. This technique allows estimation of PLL closed-loop bandwidth and jitter peaking. The circuit can be used to plot step-response vs. time, measure static phase error, and observe phase-lock status.

10:45 AM **BREAK**

## Session 20 - Circuit Simulation and Design Methodology

Wednesday Morning, September 16  
Pine Ballroom

Chair: Larry Nagel, Omega Enterprises Consulting  
Co-Chair: Colin McAndrew, Freescale

This session's papers address evolutionary advances in circuit design, methodology, analysis, and simulation tools, and a breakthrough improvement in circuit simulation speed.

9:00 **Introduction**

9:05  
20-1 **Leveraging Designer's Intent: A Path Toward Simpler Analog CAD Tools (INVITED)**, *Jaeha Kim, Metha Jeeradi, Byongchan Lim and Mark Horowitz, Stanford University, Stanford, CA*

Leveraging the Boolean intent of digital circuits has enabled a wide set of CAD tools that helped increase the productivity of digital designers. Increasing analog designers' productivity requires a similar encapsulation of designer's intent for analog circuits. We argue that linear system models serve this role for almost all analog circuits, while the variables of these models may be in some transformed domains, rather than being the direct voltage/current waveforms of the circuits. We show how using these models enable new ways to design, optimize, and validate mixed-signal circuits. Even systems that reach steady states only in a stochastic sense can be analyzed as linear systems. Then a remaining issue is to ensure that the non-linear circuit reaches the intended "linear" operating point during start-up, which can be addressed by global convergence analysis.

9:55  
20-2 **System Power Distribution Network Theory and Performance with Various Noise Current Stimuli Including Impacts on Chip Level Timing (INVITED)**, *Larry Smith, Shishuang Sun, Peter Boyle and Bozidar Krsnik, Altera Corp.*

Power Quality has become a determining factor in product performance and reliability. The reactive portions of the power distribution network (PDN) have a greater effect on power quality than DC IR drop. Resonance in the parallel inductance and capacitance network creates an impedance peak in the frequency domain and undesirable voltage noise in the time domain. The on-chip voltage noise is usually much higher than PCB PDN noise. A method of determining and simulating circuit parameters and comparing results to a target impedance is presented. A test vehicle has been built and measured to provide laboratory measured results for PDN voltage noise. Switching current patterns are defined which generate typical and pathological voltage waveforms. PRBS patterns are used as a characterization technique to provide reasonable worstcase resonance stimulation. The voltage noise is responsible for measured timing and jitter degradation in logic circuits.

10:45 AM **BREAK**

11:05  
20-3 **GPU-Accelerated Time-Domain Circuit Simulation**, *Rick Poore, Agilent Technologies*

Time-domain circuit simulation is dominated by transistor model evaluation. A modern graphics processing unit (GPU) is a parallel, high performance computer suitable for non-graphics tasks. Simulation is sped up by 3-6x by moving transistor evaluation to a GPU. Implications for writing transistor models for good GPU performance are discussed.

11:30  
20-4 **Adjoint Sensitivity Analysis of Nonlinear Distortion in RF Circuits**, *Dani Tannir and Roni Khazaka, McGill University, Quebec, Canada*

Recently, an efficient moments based method for computing the third order intercept point of RF circuits was proposed. The moments based approach did not however provide sensitivity information. In this paper we propose a new method based on moments of the adjoint network. This new approach provides both the third order intercept point as well as its sensitivity in a

very computationally efficient manner. As is generally the case in adjoint based methods, the sensitivity is provided with respect to all circuit parameters simultaneously.

11:55 **Discrete-Time, Cyclostationary Phase-Locked Loop Model for Jitter Analysis**, *Socrates Vamvakos, Vladimir Stojanovic\* and Borivoje Nikolic\*\**, Richardson, TX, \*Massachusetts Institute of Technology, Cambridge, MA, \*\*University of California, Berkeley, CA

20-5  
The paper presents a discrete-time, linear, cyclostationary PLL model for jitter analysis, which accounts for the cyclostationarity of noise injected into the PLL loop and predicts the effects of aliasing on jitter. Expressions are derived for the output jitter spectrum, which agree with event-driven simulations of a 3rd-order PLL.

## Session 21 - SoC Architectures for Signal Processing

Wednesday Morning, September 16  
Fir Ballroom

Chair: Henry Chang, Designer's Guide Consulting  
Co-Chair: Steve Wilton, University of British Columbia

These papers explore different architectures, fabrics, and interconnect structures for signal processing and computing. These structures range from general purpose, domain specific, to application specific. These papers consider power, throughput, and flexibility trade-offs.

11:00 **Introduction**

11:05 **A Heterogeneous Digital Signal Processor Implementation for Dynamically Reconfigurable Computing**, *Davide Rossi, Fabio Campi, Antonello Deledda, Simone Spolzino and Stefano Pucillo, University of Bologna, Italy*

21-1  
This paper describes a SoC implementation of a heterogeneous multi-core digital signal processor, including an embedded field-programmable gate array (eFPGA), a mid-grain reconfigurable datapath (DREAM), and a coarse-grain reconfigurable array (PACT-XPP) integrated on independent clock islands. An ARM processor manages communication, configuration and synchronization. The device joins the flexibility of the heterogeneous configurable engines with the dynamic frequency scaling techniques, enabling performance/power tuning. The SoC was implemented in 90nm CMOS technology and is 110mm<sup>2</sup>.

11:30 **A 64-PE Folded-Torus Intra-chip Communication Fabric for Guaranteed Throughput in Network-on-Chip Based Applications**, *Phi-Hung Pham, Phuong Mau and Chulwoo Kim, Korea University, Seoul, Korea*

21-2  
A 64-PE folded-torus intra-chip communication fabric is proposed to provide guaranteed throughput in terms of dead- and live-lock free and in order data delivery. The intra-chip network consuming 9.4% chip area and 18% of total chip power can provide max 44.6Gb/s bisection bandwidth with an Ebit of 0.14pJ/bit/hop.

11:55 **A 54GOPS 51.8mW Analog-Digital Mixed Mode Neural Perception Engine for Fast Object Detection**, *Minsu Kim, Joo-Young Kim, Seunghin Lee, Jinwook Oh and Hoi-Jun Yoo, Korea Advanced Institute of Science and Technology, Daejeon, Korea*

21-3  
A mixed mode Neural Perception Engine (NPE) is proposed as the pre-processing accelerator of multi-object recognition processor to reduce the computational complexity and increase its efficiency. It consists of Motion Estimator (ME), Visual Attention Engine (VAE) and Object Detection Engine (ODE). The fabricated chip achieves 54 GOPS 51.8mW NPE. By implementing a fast and robust neuro-fuzzy algorithm in analog-digital mixed circuits, the area and power of the ODE is reduced by 59% and 44%, respectively, compared to those of all digital implementation. The NPE can increase the frame rate by 2.09x and reduce power consumption by 38% of the multi-object recognition processor.

12:20 **A 1.4 MHz 0.21 mW MPEG-2/4 AAC Single Chip Decoder**, *Tsung-Han Tsai, Chun-Nan Liu, Hsueh-Yi Lin, Hsing-Chuang Liu and Chia-Ying Wu, National Central University, Taiwan*

21-4  
A low power and full ASIC MPEG-2/4 AAC single chip decoder is presented. Through algorithm, architecture, RTL and circuit level lower power techniques, the proposed AAC decoder is operated at 1.4 MHz for the 44.1 KHz sampling frequency and consumes only 0.21 mW using TSMC 0.13 μm library.