

Wednesday Morning Program

Session 18 – mm Wave Circuits and Systems

Wednesday Morning, September 21
Donner Pass Ballroom

Chair: Ehsan Afshari, Cornell University
Co-Chair: John Rogers, Carleton University

There is growing interest in mm-wave frequency range for communication, sensing, and imaging. The papers in this session present advances in CMOS implementation of such systems.

9:00 AM **Introduction**

9:05 AM **Circuit Technologies for mm-Wave Wireless Systems on Silicon (INVITED)**, *J. Long, Y. Zhao, Y. Jin, W. Wu, M. Spirito, Delft University of Technology*
18-1

Silicon SoCs capable of millimeter-wave (mm-wave) frequency operation now offer a combination of performance, functionality, integration scale and cost unrivaled by other IC technologies. The components, design techniques and circuits that are propelling deep submicron silicon technologies in mm-wave system front-ends are surveyed in this paper. Examples relevant to Gbit/s rate wireless communication are highlighted, with emphasis on innovations drawn from the recent literature.

9:55 AM **A 76-81GHz Transmitter with 10dBm Output Power at 125°C for Automotive Radar in 65nm Bulk CMOS**, *K. To, V. Trivedi, Freescale Semiconductor Inc.*
18-2

A high power and wide tuning range CMOS-only transmitter, composed of a VCO and a power amplifier, operating from -40C to 125C for automotive radar is presented. The transmitter has 10dBm output power at 125C and >10GHz tuning range to cover PVT variations, with power consumption of 420mW. The 77GHz phase noise is -87dBc/Hz at 1MHz offset.

10:20 AM **A 2.9-dB Noise Figure, Q-Band Millimeter-Wave CMOS SOI LNA**, *M. Parlak, J.F. Buckwalter, University of California, San Diego*
18-3

This paper discusses a two-stage low noise amplifier(LNA) implemented in a 45nm CMOS SOI process that operates between 43 and 53 GHz. The LNA stages are based on a cascode amplifier with simultaneous noise and input power matching. The LNA exhibits a minimum noise figure (NF) of 2.9 dB at 47 GHz and measured gain of 18.5 dB at 49 GHz. The output P1dB compression power is 3 dBm and saturation output power is 7 dBm to reach a peak efficiency of 22%. The measured OIP3 is 14 dBm. The LNA occupies an area of 0.35mm² with pads and consumes 19 mA from 1.2 V supply. The results present the lowest noise figure for a silicon-based millimeter-wave LNA.

10:45 AM **BREAK**

11:05 AM **A High Gain 107 GHz Amplifier in 130 nm CMOS**, *O. Momeni, E. Afshari, Cornell University*
18-4

A systematic method to design high gain amplifiers at frequencies close to the f_{max} of the transistors is introduced. Next, in a 130 nm CMOS process, we design and implement a 107 GHz amplifier with a gain of 12.5 dB, PAE of 4.4%, and saturated output power of >2.3 dBm.

11:30 AM **Double-Balanced 130-180 GHz Passive and Balanced 145-165 GHz Active Mixers in 45 nm**

18-5 **CMOS**, O. Inac, A. Fung*, G.M. Rebeiz, Univeristy of California, San Diego, *NASA Jet Propulsion Laboratory

This paper presents wideband passive and active mixers in the 100-200 GHz range. The mixers are built using a 45nm CMOS SOI process with an ft of 220 GHz when referenced to the top metal layer. The passive double-balanced mixer results in a conversion loss of 12-13 dB from 130-180 GHz (including balun, transmission line and GSG pad losses) and achieves optimal performance with 3 dBm of LO power (referenced to the GSG LO pads). The active mixer achieves a conversion loss of 4.5 dB with a 3-dB bandwidth of 145-165 GHz, and consumes only 10 mW of DC power from a 1.5 V supply. The application areas are in wideband Gbps communications, imaging arrays with large IF bandwidths, and mm-wave spectrometers. To our knowledge, this work represents the first demonstration of high performance CMOS mixers in the 130-180 GHz frequency range.

11:55 AM **60GHz Low-Loss Compact Phase Shifters Using A Transformer-Based Hybrid in 65nm CMOS**, M. Tabesh, A. Arbabian, A. Niknejad, University of California, Berkeley
18-6

Two compact, low-loss, passive reflective type 60GHz phase shifters are presented in standard 65nm CMOS using lumped-element baluns to implement the hybrid. The first architecture achieves 180 degrees phase shift with an average loss of 6.6dB and area of 0.031mm². The second phase shifter demonstrates the best reported average loss of 4.5dB with an area of 0.048mm² while having 150 degrees of phase shift. These are the smallest reported 60GHz phase shifters in silicon.

Session 19 – Nyquist A/D

Wednesday Morning, September 21
Siskiyou Ballroom

Chair: Erick Naviasky, Cadence
Co-Chair: George LaRue, Washington State University

This year we have 4 Nyquist A/D's starting with a nW SAF for biomedical applications. Then we have a comparator based 2 step A/D and finish with 2 time-interleaved High-speed converters.

9:00 AM **Introduction**

9:05 AM **A 0.5V 1KS/s 2.5nW 8.52-ENOB 6.8fJ/Conversion-Step SAR ADC for Biomedical Applications**, Tsung-Che Lu, Lan-Da Van, Chi-Sheng Lin*, Chun-Ming Huang*, National Chia Tung University, *National Chip Implementation Center
19-1

A SAR ADC with leakage reduction bootstrapped switch (LRBS) and low-power approach for biomedical applications is presented. LRBS is employed to alleviate the leakage caused by the low-power approach for increasing SNDR. The 0.18 μ m CMOS prototype achieves 6.8fJ/conversion-step and 2.5nW under a 0.5V supply at 1KS/s with a Nyquist input.

9:30 AM **A 0.7V 810 μ W 10b 30MS/s Comparator-Based Two-Step Pipelined ADC**, Ho-Young Lee, David Gubbins*, Bumha Lee**, Un-Ku Moon, Oregon State University, *Linear Technology, **National Semiconductor
19-2

This paper presents a 10b 30MS/s comparator-based two-step pipelined ADC that uses a comparator instead of an opamp to reach low-voltage and low-power operation with a rail-to-rail input. The prototype ADC, fabricated in a 0.13 μ m CMOS process, consumes 810 μ W at 0.7V supply and achieves 121fJ FOM at 10MHz input frequency.

9:55 AM **A 450 MS/s 10-bit Time-Interleaved Zero-Crossing Based ADC**, Jack Chu, Hae-Seung Lee,

19-3 *Massachusetts Institute of Technology*

A 450-MS/s 10-bit time-interleaved zero-crossing based pipelined ADC is described. The prototype ADC, fabricated in a 90-nm CMOS process, occupies 1.3 mm². A reference pre-charging technique is applied to reduce the voltage ripples on the reference voltages. Gain, offset, and timing calibration is applied to achieve an 8.7 ENOB with a 211 MHz input signal and dissipates 34 mW from a 1.2V supply for a FOM of 182 fJ/step.

10:20 AM **A 40-mW 7-bit 2.2-GS/s Time-Interleaved Subranging ADC for Low-Power Gigabit**
19-4 **Wireless Communications in 65-nm CMOS**, *I-Ning Ku, Zhiwei Xu, Yen-Cheng Kuan, Yen-Hsiang Wang, Mau-Chung Frank Chang, University of California, Los Angeles*

A compact, low-power time-interleaved ADC is presented. Novel time-splitting subranging architecture is invented to significantly boost the speed of individual ADC channels. In addition, a low-power and fast-settling distributed resistor array for reference voltages is proposed to mitigate mismatches within channels.

10:45 AM **BREAK**

Session 20 – Enhanced Simulation Techniques

Wednesday Morning, September 21
Cascade Ballroom

Chair: Larry Nagel, Omega Enterprises Consulting
Co-Chair: Frank Liu, IBM Austin Research Lab

This session presents the latest advancements in fast timing simulation algorithms, statistical modeling, parasitic extractors, as well as simulation techniques for special power-gating structures.

9:00 AM **Introduction**

9:05 AM **High-Dimensional Statistical Modeling and Analysis of Custom Integrated Circuits**
20-1 **(INVITED)**, *Trent McConaghy, Solido Design Automation Inc.*

Custom circuit designers have long favored manual equation-based approaches in early design stages, because it gives excellent insight and control over the design. However, this flow is threatened: as modern process nodes advance, process variation affects circuit performance more strongly, hurting the accuracy of existing equations. Because designers are typically not statistical modeling experts, it is difficult to adapt the equations to incorporate statistical variations. This paper presents a fast, deterministic technique to help designers revise equations to account for statistical variation. Specifically, the technique extracts compact equations of performance as a function of process variables, even for cases when there are thousands of possible variables and the equations are highly nonlinear. In fact, it provides a whole set of equations that trade off simplicity versus accuracy compared to SPICE. The technique is validated on a broad range of custom integrated circuit modeling problems.

9:55 AM **Fast and Accurate Event-Driven Simulation of Mixed-Signal Systems with Data**
20-2 **Supplementation**, *Myeong-Jae Park, Hanseok Kim, Minbok Lee, Jaeha Kim, Seoul National University*

This paper presents a methodology for simulating behaviors and performances of complex mixed-signal systems with an event-driven HDL simulator. Prototype models for a PLL and a high-speed I/O system demonstrate 50-times and 80-times faster simulation speeds, respectively, with the same or better accuracy compared with the conventional Verilog models.

10:20 AM **Enhanced Sensitivity Computation for BEM Based Capacitance Extraction Using the Schur Complement Technique**, *Y. Bi, S. de Graaf, N.P. van der Meijs, Delft University of Technology*

We present a useful extension for an existing algorithm of capacitance sensitivity computation w.r.t. multiple geometric variations. The extension achieves an even better accuracy at a modest increase of computational cost compared to the existing algorithm. With such an extension, the enhanced algorithm can provide different solutions for different requirements of accuracy and efficiency. This algorithm provides a flexible tool for BEM-based extractors subject to process variations.

10:45 AM **BREAK**

11:05 AM **Power Gating Implementation for Noise Mitigation with Body-Tied Triple-Well Structure**, *Y. Takai, M. Hashimoto, T. Onoye, Osaka University*

This paper investigates power-gating implementations that mitigate power supply noise. We focus on the body connection of power-gated circuits, and examine the amount of power supply noise induced by power-on rush current and the contribution of a power-gated circuit as a decoupling capacitance during the sleep mode. To figure out the best implementation, we designed and fabricated a test chip in 65nm process. Experimental results with measurement and simulation reveal that the power-gated circuit with body-tied structure in triple-well is the best implementation from the following three points; power supply noise due to rush current, the contribution of decoupling capacitance during the sleep mode and the leakage reduction thanks to power gating.

11:30 AM **Exploration Of On-Chip Switched-Capacitor DC-DC Converter For Multicore Processors Using A Distributed Power Delivery Network**, *P. Zhou, D. Jiao, C. H. Kim, S. S. Sapatnekar, University of Minnesota*

We explore the design of on-chip switched-capacitor DC-DC converters for chip-multiprocessors using an accurate power grid simulator. Results show that distributed design of switched-capacitor converters can achieve largely improved IR noise and supply voltage compared to lumped design. We also demonstrate the usage of switched-capacitor converters for multi-domain power supply.

Session 21 – Power Management

Wednesday Morning, September 21
Sierra Ballroom

Chair: Jerry Zheng, Iwatt
Co-Chair: William McIntyre

Effective power management requires innovative techniques to optimize system cost and efficiency. This session includes advancements in power management for emerging applications and nanometer CMOS.

9:00 AM **Introduction**

9:05 AM **A 90nm Data Flow Processor Demonstrating Fine Grained DVS for Energy Efficient Operation from 0.25V to 1.2V**, *Y. Shakhsheer, S. Khanna, K. Craig, S. Arrabi, J. Lach, and B. H. Calhoun, University of Virginia*

We present a 90nm data flow processor that executes DSP algorithms using fine grained DVS at the component level with rapid VDD switching and VDD dithering for near-ideal quadratic dynamic energy scaling from 0.25V-1.2V. Measurements show energy savings up to 50% and

46% compared to single-VDD and multi-VDD alternatives.

9:30 AM
21-2 **An Integrated Four-Phase Buck Converter Delivering 1A/mm² with 700ps Controller Delay and Network-on-Chip Load in 45-nm SOI**, *N. Sturcken, M. Petracca, S. Warren, L. P. Carloni, A. V. Peterchev*, K. L. Shepard, Columbia University, *Duke University*

We present a four-phase integrated buck converter in 45nm SOI technology. The controller uses unlatched pulse-width modulation (PWM) with nonlinear gain to provide both stable small-signal dynamics and fast response (~700ps) to large input and output transients. This fast control approach reduces the required output capacitance by 5X in comparison to a controller with latched PWM at similar operating point. The converter switches at 80MHz and delivers 1A/mm² at 83% efficiency and 0.66 conversion ratio.

9:55 AM
21-3 **A Wide-Range DC/DC Converter with 2nd Order Digital Compensation and Direct Battery Connection in 40nm CMOS**, *Justin Shi, Ying-Chih Hsu, Eric Soenen, Alan Roth, Justin Gaither, TSMC*

This paper presents a digital DC-DC converter with 2nd order compensation and direct battery connect capability in 40nm CMOS. A combination of circuit and process technology is used to achieve an input range up to 5.5V with peak efficiencies of 95%. It also outlines an approach to optimize a control loop based on a sigma-delta ADC and higher order digital filter, which is demonstrated on a prototype achieving step response times under load below 38μs/V.

10:20 AM
21-4 **An 80% Peak Efficiency, 0.84mW Sleep Power Consumption, Fully-Integrated DC-DC Converter with Buck/LDO Mode Control**, *X. Gong, J. Ni*, Z. Hong, B. Liu*, Fudan University, *Analog Devices*

A fully-integrated step-down DC-DC converter with LDO mode to reduce the sleep power consumption and improve efficiency at light loads is presented. It reaches 80% at 90mA load, and efficiency at 10mA load increases by 22.6%. Furthermore, the sleep power consumption is reduced from 10mW without hybrid mode to 0.84mW.

10:45 AM **BREAK**

11:05 AM
21-5 **Perturbation On-time (POT) Control and Inhibit Time Control (ITC) in Suppression of THD of Power Factor Correction (PFC) Design**, *Jen-Chieh Tsai, Chi-Lin Chen, Yi-Ting Chen, Chia-Lung Ni, Chun-Yen Chen, Ke-Horng Chen, Chih-Jen Chen*, Heng-Lin Pan*, National Chiao Tung University, *Industrial Technology Research Institute*

The paper presented the perturbation on-time (POT) control technique to suppress the total harmonic distortion (THD) to improve the performance of the power factor correction (PFC) in the AC-DC converter. Simultaneously, it can improve the efficiency through the proposed inhibit time control (ITC) mechanism at low AC input voltage. The test circuit fabricated in TSMC 800V UHV process can show the highly-integrated PFC controller. Experimental results demonstrate low THD of 8%, which results in high PF of 99%. Besides, high efficiency of 95% can be ensured at the output power of 90W.

11:30 AM
21-6 **A Reconfigurable 2x / 2.5x / 3x / 4x SC DC-DC Regulator for Enhancing Area and Power Efficiencies in Transcutaneous Power Transmission**, *X. Zhang, H. Lee, University of Texas at Dallas*

A reconfigurable 2x / 2.5x / 3x / 4x switched-capacitor DC-DC regulator for transcutaneous power transmission is presented in this paper. The proposed power stage enables the regulator to maintain high power efficiencies under different input voltages caused by coupling variations. A fixed on-time regulation scheme is developed to minimize the switching power loss and to achieve small output ripple voltages of the regulator. Implemented in a standard

0.35-um n-well CMOS process, the proposed regulator delivers a maximum output current of 10 mA and achieves the peak power efficiency of 82%. When the input voltage varies by 1.6 V, the power efficiency of the proposed regulator can be improved by 40% compared to that of the fixed-ratio 4x counterpart. The output ripple reaches 0.5% of the output voltage.

11:55 AM
21-7

A Near Zero Cross-Regulation Single-Inductor Bipolar-Output (SIBO) Converter with an Active-Energy-Correlation Control for Driving Cholesteric-LCD, *Yu-Huei Lee, Ming-Yan Fan, Wei-Chung Chen, Ke-Horng Chen, Sheng-Fa Liu*, Pao-Hsien Chiu*, Sandy Chen*, Chun-Yu Shen*, Ming-Ta Hsieh*, Huai-An Li*, National Chiao Tung University, *Chunghwa Picture Tubes, Ltd.*

A zero cross-regulation (zero-CR) single-inductor bipolar-output (SIBO) converter with an adaptive-energy correlation (AEC) control is proposed as a compact power management solution for driving cholesteric-LCD (Ch-LCD). The SIBO converter can provide a pair of positive and negative output voltages with only one external inductor for achieving the polarity reversion operation in Ch-LCD to obtain high-quality displays. The proposed AEC control decides energy distribution for bipolar outputs without any cross regulation through the embedded prediction function. The chip fabricated by 0.25 μm CMOS process demonstrates zero cross-regulation at bipolar outputs with 90 % peak power conversion efficiency.