

Technical Sessions
Wednesday, September 22 - Morning

Session 19 – Nyquist ADCs

Wednesday Morning, September 22
Oak Ballroom

Chair: David Nairn, University of Waterloo
Co-Chair: Takahiro Miki, Renesas Electronics Corp.

The need for speed and minimum power continues to drive advances in ADCs. These papers each adopt a different approach to the speed/power tradeoff.

9:00 **Introduction**

9:05 **An 8-bit 1.5GS/s Flash ADC Using Post-Manufacturing Statistical Selection**, *Jonathan Proesel, Gokce Keskin, Jean-Olivier Plouchart*, Lawrence Pileggi, Carnegie Mellon University, *IBM TJ Watson Research Center*

An 8-bit, 1.5GS/s flash ADC is presented. Comparators are digitally calibrated using statistical selection. INL of 1.32 LSB and DNL of 1.23 LSB are achieved. Average comparator noise of 5mVrms (1.3 LSB) limits SNDR to 37dB at low frequencies. Total power is 35mW, 20mW in the S&H and 15mW in the ADC core. The figure of merit is 0.42pJ/conv, the best reported for 1+GS/s, 7+-bit ADCs.

9:30 **Single-Channel, 1.25-GS/s, 6-bit, Loop-Unrolled Asynchronous SAR-ADC in 40nm-CMOS**, *Tao Jiang, Wing Liu*, Freeman Y Zhong*, Charlie Zhong*, Patrick Y Chiang, Oregon State University, *LSI Corporation*

A single channel, loop-unrolled, asynchronous successive approximation (SAR) ADC fabricated in 40nm CMOS is presented. Compared with a conventional SAR structure that exhibits significant delay in the digital feedback logic, the proposed 6b SAR-ADC employs a different comparator for each bit of conversion, with an asynchronous ripple clock generated after each quantization. With the sample rate limited only by the six delays of the C-DAC settling and comparator quantizations, the 40nm-CMOS SAR-ADC achieves a peak SNDR of 32.9dB and 30.5dB at 1GS/s and 1.25GS/s, respectively, consuming 5.28mW and 6.08mW in a core area less than 170um x 85um.

9:55 **A 550μW 10b 40MS/s SAR ADC with Multistep Addition-only Digital Error Correction**, *Sang-Hyun Cho, Chang-Kyo Lee, Jong-Kee Kwon*, Seung-Tak Ryu, KAIST, *ETRI*

A speed-enhanced 10b asynchronous SAR ADC with multistep addition-only digital error correction (ADEC) is presented in this paper. Three virtually divided sub-DACs have a 0.5 LSB over-range between stages owing to additional decision phases incorporating DAC switch control. These redundancies make it possible to guarantee 10b linearity with a 37% speed enhancement under a 4b-accurate DAC settling condition at MSB decision. A prototype ADC was implemented in CMOS 0.13μm technology. The chip consumes 550μW and achieves a 50.6dB SNDR at 40MS/s under a 1.2V supply. The figure-of-merit (FOM) is 42fJ/conv-step.

10:20 **A 10b 120MS/s 45nm CMOS ADC Using A Re-Configurable Three-Stage Switched Op-Amp**, *Young-Ju Kim, Kyung-Hoon Lee, Seung-Hak Ji, Yi-Gi Kwon, Seung-Hoon Lee, Kyoung-Jun Moon*, Michael Choi*, Ho-Jin Park*, Byeong-Ha Park*, Sogang University, *Samsung Electronics*

10:45 BREAK

11:05 SHA-Less Pipelined ADC Converting 10th Nyquist Band with In-Situ Clock-Skew Calibration, *Pingli Huang, Szukang Hsien**, *Victor Lu, Peiyuan Wan***, *Seung-Chul Lee, Wenbo Liu, Bo-Wei Chen^, Yung-Pin Lee^, Wen-Tsao Chen^, Tzu-Yi Yang^, Gin-Kou Ma^, Yun Chiu, UIUC*, **Texas Instruments*, ***Beijing University of Technology*, *^Industrial Technology Research Institute*

Conversion from dc to the 10th Nyquist band is enabled in a SHA-less, 10-b, 100-MS/s pipelined ADC by digitally calibrating the clock skew in the 3.5-b front-end stage. The architectural redundancy of a pipelined ADC is exploited to extract skew information from the first-stage residue output with two out-of-range comparators and some simple digital logic; a gradient-descent algorithm is used to adaptively adjust the timing of the front-end sub-ADC to synchronize with that of the S/H. The 90-nm proto-type consumes 12.2 mW and digitizes inputs up to 480 MHz (limited by testing equipment) without skew errors in experiments, whereas the same ADC fails at 130 MHz when the calibration is disabled. The measured SFDR is 71 dB at 20 MHz and 55 dB at 480 MHz.

Session 20 – Modeling of Layout-Dependent Effects and RF Devices

Wednesday Morning, September 22
Fir Ballroom

Chair: Hidetoshi Onodera, Kyoto University
Co-Chair: Brian Chen

This session presents a review of state-of-the-art modeling techniques for integrated RF passive devices, RF LDMOS, and layout-dependent effects in VLSI designs.

9:00 Introduction

9:05 Layout-Dependent Proximity Effects in Deep Nanoscale CMOS (INVITED), *John Faricelli, Advanced Micro Devices*

As CMOS scaling extends into the nanoscale regime, designers need to be aware that device behavior depends not only on traditional geometric parameters such as channel length and width, but also on layout implementation details of the device and its surrounding neighborhood. The advent of stress engineering, in which intentional mechanical stress is applied to improve device performance, also adds new geometric dependencies. This paper reviews the major process technology features that cause layout-dependent proximity effects and how to account for these effects in circuit and layout design.

9:55 Modeling of Integrated RF Passive Devices (INVITED), *Sharad Kapur, David Long, Integrand Software, Inc.*

We use an electromagnetic (EM) simulator for modeling integrated RF components. EM simulators such as EMX are fast and accurate enough to provide good models of such components. It is feasible to simulate thousands of possible designs and build scalable component models. Scalable models allow fast choices of optimal components.

10:45 BREAK

11:05 On the Modeling of LDMOS RF Power Transistors (INVITED), *John Wood, Peter Aaen, Freescale Semiconductor Inv.*

In this review we present a technology-independent approach to the construction of a circuit model for high-power radio-frequency (RF) LDMOS FETs. This model is fully nonlinear, with a self-consistent dynamic electrothermal component. We compare and contrast this approach with other MOSFET modeling approaches used for digital and RF CMOS applications.

Session 21 – RF Power Amplifiers

Wednesday Morning, September 22
Pine Ballroom

Chair: Alireza Shirvani, Ralink Technologies
Co-Chair: Rick Booth, Panasonic PWRL

This session discusses integrated RF power amplifiers in CMOS technology and the challenges of achieving high output power, high efficiency, and high frequency operation.

9:00 **Introduction**

9:05 **Will CMOS Amplifiers Ever Kick-GaAs? (INVITED)**, *Peter Zampardi, Skyworks Solutions, Inc.*
21-1

In this paper, we present a discussion and comparison of CMOS and GaAs HBT technologies for handset power amplifiers. Our perspective is unique to other comparisons in that we actually have products in both technologies. To understand the application space where each of these technologies makes sense, we discuss current and near-term PA requirements as well as technology and technology support issues. Finally, we aim to dispel some the common misperceptions surrounding these technologies.

9:30 **A Stacked 6.5-GHz 29.6-dBm Power Amplifier in Standard 65-nm CMOS**, *Maryam Fathi, David K. Su, Bruce A. Wooley, Stanford University*
21-2

A stacked amplifier architecture has been used to achieve high RF output power levels in sub-100nm CMOS. The stacking makes it possible to both operate the power amplifier (PA) from a large supply voltage and implement RF power combining. A 6.5-GHz PA has been integrated in a 65-nm standard CMOS technology. The amplifier achieves 29.6-dBm output power with an efficiency of 20.3% at 6.5 GHz when driven from a 4.6-V supply voltage.

9:55 **A 2.4GHz Mixed-Signal Polar Power Amplifier with Low-Power Integrated Filtering in 65nm CMOS**, *Debopriyo Chowdhury, Lu Ye, Elad Alon, Ali Niknejad, University of California, Berkeley*
21-3

A 65nm digitally-modulated polar transmitter incorporates a fully-integrated 2.4GHz efficient switching Inverse Class D power amplifier. Low power digital filtering on the amplitude path helps remove spectral images for coexistence. The transmitter integrates the complete LO distribution network and digital drivers. Operating from a 1-V supply, the PA has 21.8dBm peak output power with 44% efficiency. Simple static predistortion helps the transmitter meet EVM and mask requirements of 802.11g 54Mbps WLAN standard with 18% average efficiency.

10:20 **An Integrated 33.5dBm Linear 2.4GHz Power Amplifier in 65nm CMOS for WLAN Applications**, *Ali Afsahi, Lawrence E. Larson, University of California, San Diego*
21-4

An integrated linear 2.4GHz CMOS power amplifier is presented. With a 3.3V supply, the PA produces a saturated output power of 33.5dBm with peak drain and power-added efficiencies of 44.2% and 37.6%, respectively and has 40dB small-signal gain. By utilizing gm-linearization and digital pre-distortion, an EVM of -25dB is achieved at 26.4dBm with 22% PAE while

transmitting 54Mbps OFDM. The chip is fabricated in standard 65nm CMOS and packaged in a 40-pin QFN package. The PA occupies 2.2mm² active area.

10:45 BREAK

11:05 **Millimeter-Wave 14dBm CMOS Power Amplifier with Input-Output Distributed**
21-5 **Transformers**, *Andrea Pallotta, Wissam Eyssa*, Luca Larcher**, Riccardo Brama**, STMicroelectronics S.r.l., *Institute for Advanced Study of Pavia, **University of Modena and Reggio Emilia*

We present a novel fully differential input/output distributed transformer topology used for the design of millimeter-wave power amplifiers. Input/output distributed transformers are used to feed the input signal to four differential couples and to combine their output power. This topology improves the stability and the efficiency of the power amplifier, minimizing the chip area. The PA prototype realized in a standard 65nm CMOS technology, supplied with 1.2V, achieves a 1dB single-ended output power compression point of 14dBm at 56GHz with a PAE of 8.3%, occupying only 0.2mm².

11:30 **A 77 GHz Power Amplifier Using Transformer-Based Power Combiner in 90 nm CMOS**,
21-6 *Tao-Yao Chang, Chao-Shiun Wang, Chorn-Kuang Wang, National Taiwan University*

A 77 GHz PA with 50 Ω input and output matching has been realized in a general purpose 90 nm CMOS technology. In order to improve the output power and reduce the signal loss, a transformer and a short stub topology are employed respectively. The PA achieves a saturated output power (P_{out,sat}) of +13.2 dBm and 1dB compressed output power (P_{out,1dB}) of +11.2 dBm with a peak power-added efficiency (PAE) of 10.4% while operated with a 1.2 V supply.

Session 22 – Tutorial Silicon Debug in Advanced Technologies

Wednesday Morning, September 22
Cedar Ballroom

This session (3 hours) will discuss debug methods in leading edge technologies for SOCs, FPGAs, and Microprocessors. The discussion will cover first silicon bring-up, pre and post-silicon practices for enhancing silicon debug, speed path debug, and power problem debug.

9:00 **Introduction**
Mike Li, Altera

9:05 **Using Electrical Test Data for Technology/Design Bring-up**, *Anne Gattiker, IBM Austin*
22-1 *Research Lab*

Given the many facets of complexity in today's manufacturing processes and the fact that time-to-market pressures make it necessary to begin design before technology is mature, it is a given that there will be mismatch between design models and manufactured hardware. As a result it is necessary during bring-up to consider not just model-hardware mismatches, but to prioritize attention on those mismatches that affect the product power and performance. This talk discusses approaches to understanding model-hardware correlation, including use of both embedded test structures and product test data, to identify and prioritize problems and speed bring-up.

9:40 **Pre and Post-silicon Practices for Enhancing Silicon Debug and Failure Analysis on**
22-2 **Deep-Submicron Complex Chips**, *Eric C. Chang, Bergen Hung, Altera*

As process technology continues to scale and chip design complexity increases, silicon debug

and failure analysis becomes more challenging which directly impacts development and mask costs, in addition to time to market costs. This presentation describes pre and post-silicon practices that are valuable for enhancing silicon debug and failure analysis. Various DFX (Design-For Verification, Debug, Yield, Manufacturability) and debug techniques, including use of FPGA programmability, is discussed.

10:15 **BREAK**

10:30 **Speed Debug Challenges for High Performance SOC/Processor, T.M. Mak, Intel**
22-3

Many SoC applications today require a high level of performance (e.g. smartphones, small office/home office (SOHO) network/servers, network attached storage (NAS)/servers) with operating frequencies going beyond 1 GHz. On-die and overall process variation will create new speed paths that may not be predictable with timing models. This tutorial will introduce some speed path debug techniques that have long been employed by high performance processor designs. Additional debug challenges as a result of 3D TSV integration will also be discussed

11:05 **Low Power Design Debug, Jackie Snyder, Marvell and Raymond Lee, EAG**
22-4

Design for low power brings a set of unique debug challenges. First silicon may show disappointing low power state results, which may be process or design related. These designs may have multiple voltage domains and internal supply domains that are switched off or back-biased which can create a number of baffling problems if not treated properly. This talk is a collaborative effort from design and failure analysis labs. We will go over a number of low power design bug types and methodologies for finding the problem devices. We will also discuss device fixturing best practices and DFT modes to allow thermal and emissions FA analysis.

11:40 **Bring Your Questions - Ask the Experts - Group discussion**