

Poster Session

Tuesday Evening, September 15
Cascade/Sierra Ballroom
5:00 pm – 7:00 pm

- T-1 **A 3 – 14V Rail-to-Rail Constant g_m Opamp in Conventional 0.18 μ m CMOS Process**, *E. Lee, Alfred Mann Foundation*
- A 3 – 14V rail-to-rail constant g_m opamp was fabricated in a conventional 0.18 μ m CMOS process using 3.3V I/O devices. Different high-voltage opamp sub-circuits were proposed. For a 14V supply, variations on the input stage g_m were <10.2%. The opamp has a ft of 1.3MHz for a current consumption of 40.7 μ A.
- T-2 **An Integrated CMOS Receiver Chip for NMR-Applications**, *J. Anders, P. SanGiorgio, G. Boero, Ecole Polytechnique Federal de Lausanne (EPFL)*
- We present the first CMOS-only receiver chip for NMR-applications at 300 MHz. The system consists of an on-chip reception coil, a tuning-capacitor, a down conversion-mixer and a low-frequency gain-stage as well as biasing and offset-compensation circuitry. It has an input referred voltage noise density of 0.7 nV/sqrt(Hz) and a gain of 75 dB. The power consumption is 18 mA from a single 3.3 V supply. The chip is realized in 0.35 μ m technology and occupies an area of 1200 x 850 μ m².
- T-3 **A 1.2-V 2.7-mW 160MHz Continuous-Time Delta-Sigma Modulator with Input-Feedforward Structure**, *J. Zhang, L. Yao, Y. Lian, National University of Singapore, Singapore*
- A power and area efficient continuous-time input-feedforward delta-sigma modulator (DSM) structure is proposed. The coefficients are optimized to increase the input range and reduce the power. The feedforward paths and the summer are embedded into the quantizer, hence the circuit is simplified, and the power consumption and area are reduced. The prototype chip, fabricated in a 0.13- μ m CMOS technology, achieves a 68-dB DR (Dynamic Range) and 66.1-dB SNDR (signal-to-noise-and-distortion ratio) over a 1.25-MHz signal bandwidth with a 160-MHz clock. The power consumption of the modulator is 2.7 mW under a 1.2-V supply, and the chip core area is 0.082mm².
- T-4 **Dual-Loop Direct VCO Modulation for Spread Spectrum Clock Generation**, *Christopher D. LeBlanc, Benjamin T. Voegeli, Tian Xia*, IBM, *University of Vermont*
- This paper presents a new spread spectrum clock generator (SSCG) circuit for EMI reduction. The proposed design adopts a standard integer-N phased locked loop (PLL) with two dual-voltage-controlled oscillators (VCOs). A frequency modulation loop is implemented with a digital frequency limit detector to direct the spectrum-spreading profile. An integrator is applied to generate the triangular modulation signal. Comparing with some recent designs [1,2,3,4] in the literature, the spread spectrum clock generator in this paper is simple and area efficient.
- T-5 **Phase Noise in a Synchronized Concurrent Dual-Frequency Oscillator**, *A. Goel, H. Hashemi, University of Southern California*
- The phase noise in synchronized concurrent dual-frequency oscillators is analyzed. The phase noise of an injection locked concurrent dual-frequency oscillator for either of the frequencies follows the phase noise of external injection near that frequency for offsets within the locking bandwidth of the injection. In the system of two coupled concurrent dual-frequency oscillators with bilateral coupling, the phase noise at either frequency is 3dB smaller than that at the free running case for offsets smaller than the locking bandwidth. Measurement results show a good match with the theory.
- T-6 **A Unified Parallel Radix-4 Turbo Decoder for Mobile WiMAX and 3GPP-LTE**, *Ji-Hoon Kim, In-Cheol Park*, Samsung Electronics Co., Ltd., *KAIST, Republic of Korea*
- This paper describes the energy-efficient implementation of a high performance turbo decoder, which is designed to support both Mobile WiMAX and 3GPP-LTE. We propose a new hardware architecture that can share hardware resources for the two standards. It consists of eight retimed radix-4 SISO decoders to achieve high throughput and a dual-mode hardware interleaver. A prototype chip exhibits a decoding rate of more than 100Mb/s with eight iterations while achieving an energy efficiency of 0.31nJ/bit/iter.
- T-7 **Tera-Scale Performance Machine Learning SoC with Dual Stream Processor Architecture for Multimedia Content Analysis**, *T.-W. Chen, C.-S. Tang, S.-F. Tsai, C.-H. Tsai, S.-Y. Chien, L.-G. Chen, National Taiwan University*
- A new SoC architecture for multimedia content analysis is implemented in 90nm CMOS technology. It focuses on the co-acceleration of computer vision and machine learning algorithms, and two stream processors with massively parallel processing elements are integrated to achieve tera-scale performance. In the dual processor architecture, the data are transferred between processors and the high bandwidth dual memory through the local media bus, which reduces the power consumption in the AHB data access.
- T-8 **A Fully Integrated CMOS UHF RFID Reader Transceiver for Handheld Applications**, *J. Wang, C. Zhang, B. Chi, Z. Wang, Z.H. Wang, Tsinghua University of China*
- This paper presents a fully integrated single-chip UHF radio frequency identification (RFID) reader transceiver for short distance handheld applications. The transceiver integrates an OOK modulator and a power amplifier in transmitter chain, an

IQ direct-down converter, two operational amplifiers, and two comparators in the receiver chain. A PLL frequency synthesizer is also integrated on the same chip to provide the local oscillating signals for the transceiver. The measured output P1dB power of the transmitter is 16.4dBm and the measured receiver sensitivity is -60dBm. The on-chip integer-N synthesizer achieves a frequency resolution of 200kHz with a phase noise of -92.78 dBc/Hz at 100kHz frequency offset and -124.4 dBc/Hz at 1MHz frequency offset. The reader consumes a total power of 231.2mW when the output power is 16.4dBm. The proposed reader can communicate with commercial tags in a distance of more than 50cm without any off-chip power amplifier. The chip has a die area of 4.5mm*1.3mm including pads.

- T-9 **A 1.5GS/s 4096-Point Digital Spectrum Analyzer for Space-Borne Applications**, *Brian Richards, Nicola Nicolici*, Henry Chen, Kevin Chao, Robert Abiad**, Dan Werthimer, and Borivoje Nikolic, University of California, Berkeley, *McMaster University, **Space Sciences Laboratory*

A high-performance digital spectrometer backend ASIC has been designed for use with an off-the-shelf ADC frontend. The design is based on an architecture described in Simulink that has been field-tested on FPGA platforms for radio astronomy applications. The architecture maximizes the utilization of operators to nearly 100%. A test structure has been added to the design to support the detection of soft errors, since several space-borne applications may expose the circuit to high-energy particles. An in-house automated design flow was used to map the same Simulink description to a 90nm CMOS ASIC, preserving cycle-accurate and bit-accurate behavior. The chip operates with clock rates up to 390MHz, delivering a throughput of up to 1.56GS/s with 710 mW of power.

- T-10 **REad/Access-Preferred (REAP) SRAM – Architecture-Aware Bit Cell Design for Improved Yield and Lower V_{MIN}** , *A. Goel, P. Nda, J.P. Kulkarni, K. Roy, Purdue University*

We present an architecture-aware SRAM design that decouples the conflicting requirements between read stability and writeability. Read and hold failures are reduced by preferentially sizing the cell to have better read stability at the expense of write failures (at iso-area). The increased write failures are handled by stretching the write cycle. Measurement results on a 90nm 2kb test chip show 80mV higher weak-write test voltage, 61%, 25% and 500X reduction in hold, read and write failures, respectively, without any increase in access failures. This results in improved yield relative to an iso-area nominal 6T cell, with only 3% loss in performance (based on architecture level simulation) on average.

- T-11 **A 1-V 60- μ W 16-Channel Interface Chip for Implantable Neural Recording**, *W. Liew, X. Zou, L. Yao, Y. Lian, National University of Singapore*

A 1-V 60- μ W 16-channel interface chip dedicated for implantable neural signal recording is presented. To comply with the implantation safety issue, the overall system is optimized for low power dissipation. A power efficient front-end OTA topology and a novel dual-capacitive-array SAR ADC are adopted to achieve better power efficiency. A prototype fabricated in 0.35- μ m CMOS technology achieves NEF of 2.16 and THD of 0.53% at full output swing while providing 16-kSample/s per channel output.

- T-12 **CMOS-Based Flexible Multi-Site Retinal Stimulator Toward Retinal Prosthesis Technology**, *T. Tokuda, Y. Takeuchi, T. Noda, K. Sasagawa, and J. Ohta, Nara Institute of Science and Technology*

We developed a CMOS LSI stimulator chip for retinal prosthesis technology with features of (1) multi-site stimulation using an on-chip stimulator, (2) light-controlled (image-based) stimulation. The retinal stimulator was configured as an array of small-sized intelligent CMOS stimulators called a "unit chip." We can set different conditions for each unit chip connected to a single set of 5-channel bus wiring and perform multi-site, constant-current biphasic retinal stimulation. We implemented simple binary light-sensing circuitry on the unit chip to realize image-based patterned stimulation on the retina. We verified that all the implemented functionalities correctly work and characterized the performance of the circuitry. A demonstration for image-based patterned current injection using radially aligned unit chips was also performed.

- T-13 **Chemical Microsystem Based on Integration of Microresonant Sensor and CMOS ASIC**, *K. S. Demirci, S. Truax, L. A. Beardslee, O. Brand, Georgia Institute of Technology*

A silicon-based microsystem consisting of a mass-sensitive resonant sensor and a CMOS ASIC containing feedback circuitry is demonstrated for portable sensing applications. The feedback circuitry sustains oscillation of the resonant sensor at its mechanical resonance frequency ranging between 200 and 800 kHz. The microsystem has been used for detection of volatile organic compounds in the gas-phase, and a limit of detection of 13 ppm for toluene is obtained with a frequency stability of 16 mHz.

- T-14 **Fixed- and Variable-Length Ring Oscillators for Variability Characterization in 45nm CMOS**, *Ji-Hoon Park, Liang-Teck Pang*, Kenneth Duong**, Borivoje Nikolic, University of California Berkeley, *IBM T.J. Watson Research Center, **Sun Microsystems*

Fixed- and variable-length ring oscillators (RO's) are designed for characterization of circuit-topology induced variations and spatial correlations. A 930 μ m \times 775 μ m test array is implemented in a low-power 45nm CMOS process. Measurements from the fixed-length RO's quantify an increase in variability with transistor stack height in logic gates and added variability associated to the top transistor in the stack. In addition, Variable-length RO's (VRO's) are designed to measure spatial correlation with a single-gate resolution.

- T-15 **An Energy-Recycling (ER) Technique for Field Color Sequential LCD Backlight Driving**, *Ming-Hsin Huang, Yueh-Chang Tsai, Chun-Yu Hsieh, and Ke-Horng Chen, National Chiao Tung University, Hsinchu, Taiwan*

An energy-recycling (ER) technique has been proposed to implement high power conversion efficiency and low cost solution of field color sequential (FCS) LEDs backlight driving. One recycling capacitor CR and one power-transistor MR are added to synchronous boost converter to compose the ER function. When the output voltage of FCS-LEDs backlight driver switches

from 40V to 26V for driving RGB LEDs during related time interval, ER technique stops to boost input voltage and switches to recycle energy from output terminal to the recycling capacitor CR. Thus, the output voltage can be rapidly switched between two different voltage levels with minimum power losses. The proposed ER technique has been fabricated by TSMC 40V BCD process. The experimental results demonstrate fast and efficient output voltage tracking performance is achieved by the proposed ER technique.

- T-16 **A Monolithic Buck Converter Using Differentially Enhanced Duty Ripple Control**, J. Fan, X. Li*, J. Park, A. Huang, North Carolina State University, *Texas Instruments Corporation

This paper reports a monolithic DC-DC buck converter using the differentially enhanced duty ripple control (DE-DRC). Without any compensation circuit, this converter is stable over a wide input and output range with constant switching frequency. The large duty ripple voltage with a big noise margin gives the DE-DRC buck converter good noise immunity. The positive and negative differential difference amplifier gains can adjust the high and low frequency portion of the loop transfer function to achieve fast load transient response and pure resistive output impedance, which is used to achieve the adaptive voltage position (AVP) function. We demonstrated a 1.85MHz single phase converter with wide conversion range of 10%-86.6%. This circuit was implemented in 0.5 μ m BCD process of TI.

- T-17 **Nonvolatile SRAM (NV-SRAM) Using Functional MOSFET Merged with Resistive Switching Devices**, S. Yamamoto**, Y. Shuto**, S. Sugahara**, *Dept. Information Processing, Tokyo Institute of Technology, **CREST, JST, ***ISEL, Tokyo Institute of Technology

The paper presents functional MOSFET (F-MOSFET) architecture using nonpolar-type resistive switching devices (RSDs) for nonvolatile SRAM (NV-SRAM) application. The architecture can be achieved by connecting a RSD to the source terminal of an ordinary MOSFET. The current drive capability of the F-MOSFET can be modified by the resistance state of the connected RSD, which is a very useful function for recently emerging nonvolatile logic and reconfigurable logic applications. NV-SRAM can be easily configured with a standard SRAM cell and F-MOSFETs. Using our developed SPICE macromodel for nonpolar-type RSDs, the circuit operation of the proposed NV-SRAM cell was computationally simulated.

- T-18 **A Simplified Method for Phase Noise Calculation**, Massoud Tohidian, Ali Fotowat Ahmady*, Mahmoud Kamarei, University of Tehran, *Sharif University of Technology, Tehran, Iran

A new phase noise calculation method is proposed in which noise sources are modeled with single tone sources. It uses a nonlinear frequency-domain analysis to calculate total gain from noise sources to the output phase noise. This single tone (ST) simulation directly calculates noise frequency contributions and is much faster than Hajimiri's impulse sensitivity function (ISF) method. A quadrature VCO has been implemented in TSMC 0.18- μ m CMOS and the predicted phase noise matches measurement.

- T-19 **Design of 2xVDD-Tolerant I/O Buffer with 1xVDD CMOS Devices**, Ming-Dou Ker, Yan-Liang Lin*, Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan, *Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.

A new 2xVDD-tolerant I/O buffer realized with only 1xVDD devices has been proposed and successfully verified in silicon. With the dynamic source output technique and the gate-controlled circuit, the proposed I/O buffer can transmit and receive the signals of 2xVDD without suffering gate-oxide reliability issue to meet the mixed-voltage interface applications in microelectronic systems.

- T-20 **A 3-Level PWM ADSL2+ CO Line Driver**, S. Gierkink, K. Lakshmikummar, V. Mukundagiri, D. Lim, A. Murali, F. Larsen, Conexant Systems Inc.

A PWM ADSL2+ line driver with 2.2MHz signal bandwidth is realized in a 3 metal, 2 poly 0.35 μ m CMOS process. A low 8.832MHz switching frequency is used with filtering in the feedback path to suppress aliasing. Signal processing and triangular wave generation are combined in the forward integrators. The driver delivers 100mW to a 100 Ω line with an MTPR less than -52 dB. Active area is 3mm².

- T-21 **A 65nm CMOS, Ring-Oscillator Based, High Accuracy Digital Phase Lock Loop for USB2.0**, Anant S Kamath, Biman Chattopadhyay, Gopalkrishna Nayak, Texas Instruments Inc.

A high accuracy, ring-oscillator based Digital PLL is presented here. Sigma-Delta dithering is used for improved frequency accuracy. To reduce noise due to Sigma Delta dithering and to allow for passive filtering of this noise, the Sigma Delta section of the DCO is limited to a small range. This range, however, is not sufficient to account for frequency drifts due to temperature: a novel temperature compensation scheme is used for this purpose. The DPLL is built in 65nm technology, and provides a 480MHz output, with a phase noise of -103.5dBc/Hz at 1 MHz offset, and a frequency accuracy of +/-100ppm. It supports various input frequencies and does not require an external component.

- T-22 **A Phase Detector for 12.5Gbps Clock and Data Recovery with Optimal Detection**, J. Jang, T. Choi, B. Jung, Purdue University

We propose a phase detector using a matched filter that maximizes the performance for a given input noise condition. The phase detector is designed for a 12.5Gbps CDR circuit. The performance of the proposed phase detector is compared with a typical one through simulation. A DLL-based clock recovery circuit is also implemented with the proposed phase detector and measured showing noise rejection characteristic.

- T-23 **Design-Space Exploration of Backplane Receivers with High-Speed ADCs and Digital Equalization**, H. Chung, G.-Y. Wei, Harvard University

This paper presents a backplane receiver model consisting of a simple, accurate, experimentally-verified, and parameterized high-speed flash ADC and a configurable digital equalizer for design-space exploration. Simulations demonstrate tradeoffs between ADC and equalizer bit resolution while maintaining constant receiver performance.

T-24 **A CMOS 3.3-8.4 GHz Wide Tuning Range, Low Phase Noise LC VCO**, *Bodhisatwa Sadhu, Jaehyup Kim, Ramesh Harjani, University of Minnesota*

A novel inductor switching technique is used to implement a wide-band LC VCO in 130nm CMOS. It achieves a tuning range of 87.2% with phase noise between -122 and -117.2 dBc/Hz at 1MHz offset. The resulting PFTN-FOM lies between 6.6 and 10.2 dB which is the best reported to date.

T-25 **Near-Field Communication using Phase-Locking and Pulse Signaling for Millimeter-Scale Systems**, *Yu-Shiang Lin*, Dennis Sylvester, David Blaauw, University of Michigan, *Now with IBM TJ Watson Research Center*

An inductive coupling based proximity communication system is proposed for data readout of remote powered sensor systems with ultra small form factor in $\sim\text{mm}^3$ range for implantable applications. The passive transponder is powered with a $1\times 1\text{mm}$ on-chip inductor, which also enables readout signaling using pulse signaling. The required resonance frequency for pulse signaling is obtained using a transponder PLL that locks to the incoming frequency transmitted by the reader system. The system is demonstrated with $0.13\mu\text{m}$ CMOS technology.