

Tuesday Poster Session

Tuesday Evening, September 20
Cascade/Sierra Ballroom

5:00 pm – 7:00 pm

T-1 **A Low-Power and Low-Noise 21~29 GHz Ultra-Wideband Receiver Front-End in 0.18 μm CMOS Technology**, *S.L. Huang, Y.S. Lin, J.H. Lee, National Chi Nan University*

This paper presents the design and analysis of a 21~29 GHz CMOS receiver front-end in a standard 0.18 μm CMOS process for ultra-wideband (UWB) automotive radar systems. The circuit comprises a low-noise amplifier (LNA), a double-balanced Gilbert-cell mixer, and two Marchand baluns. Over the 21~29 GHz automotive radar band, the receiver front-end exhibited excellent NF of 4.6 ± 0.5 dB and conversion gain of 23.7 ± 1.4 dB. The dc power dissipation was only 39.2 mW.

T-2 **A 2GHz Digital PLL, with Temperature Lock Range of -40°C to 125°C, in 45nm CMOS**, *B. Chattopadhyay, A. S. Kamath, S. Evani, K. Subburaj, Texas Instruments Inc.*

A 45nm, 0.09mm², 0.5-50MHz input, 2GHz output, ring-oscillator Digital PLL, achieves -90dBc/Hz at 1MHz offset, and a temperature lock range of -40C to 125C. Outputs of any two adjacent current elements of the current-mode DAC in the DCO can be progressively brought out for separate Sigma-Delta (SD) operation. This enables the DPLL to track temperature over a large range, even as the SD step size and range are kept small to minimize jitter.

T-3 **Indirect Phase Noise Sensing for Self-Healing Voltage Controlled Oscillators,**

The push for higher performance analog/RF circuits in scaled CMOS necessitates self-healing via post-manufacturing tuning. A major challenge with self-healing is the efficient design of on-chip sensors. We propose indirect sensing that exploits the correlations between the performance of interest and those that can be measured using easy-to-integrate sensors.

T-4 **An At-speed Self-testable Technique for the High Speed Domino Adder**, *Yu-Shun Wang, Min-Han Hsieh, Chia-Ming Liu, Chi-Wei Liu, James C.-M. Li, and Charlie Chung-Ping Chen, Graduate Institute of Electronics Engineering, National Taiwan University*

An at-speed self-testable technique is proposed for the high speed domino adder. We apply pseudo-exhaustive testing so that all testable faults in the 64-bit adder are detected by just 23K patterns. The adder latency is accurately measured by the programmable-skew clock generated from delay-locked loop (DLL). The proposed technique is validated on a 6.4GHz 64-bit domino adder with 181ps latency in 90nm CMOS technology. This on-chip technique is very useful for at-speed testing and speed binning of high performance CPU.

T-5 **A 95dB SNDR Audio $\Delta\Sigma$ Modulator in 65nm CMOS**, *L.Liu, D.Li, Y.Ye, L.Chen, Z.Wang, Tsinghua University*

A DT single loop 3rd order 5-bit $\Delta\Sigma$ modulator is implemented in 65nm CMOS. The modulator achieves 95dB SNDR with 24 kHz bandwidth and consumes only 371 μW from 1V supply. SNDR keeps at 90.2dB with 133 μW under 0.6V. The core area is 0.41mm².

T-6 **A Fully Integrated CMOS Nanoscale Biosensor Microarray**, *Lei Zhang, Xiangqing He, Yan Wang, Zhiping Yu, Institute of Microelectronics, Tsinghua University*

This paper presents a fully integrated CMOS microarray for biosensor applications. A 64-pixel working electrode array with optimized reference and counter electrode structure is proposed to improve symmetry, and the feature sizes of electrodes have been scaled down to 600nm. The circuit utilizes the decoding scheme of memories to simplify the pixel design while shares potentiostat opamp and current amplifiers, which allows the miniaturization of electrodes and enables large-scale integration of the microarray. The demo is fabricated in 0.18 μm CMOS technology, and experimental results successfully demonstrated the biosensing detections on the

nanoscale microarray. The circuit provides a current gain of 19.9dB, 3dB bandwidth of 15kHz, dynamic range of 141dB, sensing sensitivity of 37.6pA, and a driving capability of 0.46mA, respectively.

- T-7 **A Passive UHF Tag for RFID-based Train Axle Temperature Measurement System**, *Jianqin Qian, Chun Zhang, Liji Wu, Xijin Zhao, Dingguo Wei, Zhihao Jiang, Yuhui He, Institute of Microelectronics, Tsinghua University*
- A fully integrated passive UHF RFID tag with embedded temperature sensor, compatible with the ISO/IEC 18000 type 6C protocol, is developed in a standard 0.18 μ m CMOS process, which is designed to measure the axle temperature of a running train. The consumption of RF/analog front-end circuits is 1.556 μ A@1.0V, and power dissipation of digital part is 5 μ A@1.0V. The CMOS temperature sensor exhibits a conversion time under 2 ms, less than 7 μ W power dissipation, resolution of 0.31 $^{\circ}$ C/LSB and error of +2.3/-1.1 $^{\circ}$ C with a 1.8 V power supply for range from -35 $^{\circ}$ C to 105 $^{\circ}$ C. Measured sensitivity of tag is -5dBm at room temperature.
- T-8 **A 48-mW, 12-bit, 150MS/s Pipelined ADC with Digital Calibration in 65nm CMOS**, *B. Peng, G.-Z. Huang, H. Li, P.-Y. Wan, P.-F. Lin, Beijing University of Technology, University of Science and Technology of China*
- Digital calibrated pipelined ADC with peak SNDR=67dB, peak SFDR=81dB at 150MS/s sampling rate in 65nm CMOS process.
- T-9 **Statistical VTH Shift Variation Self-Convergence Scheme Using Near Threshold VWL Injection for Local Electron Injected Asymmetric Pass Gate Transistor SRAM**, *K. Miyaji, Y. Shinozuka, S. Miyano*, K. Takeuchi, University of Tokyo, *STARC*
- Statistical VTH shift variation in asymmetric pass gate transistor by local electron injection is studied. VD effect is self-compensated by ID effect. Near threshold VWL self-convergence injection is proposed to achieve self-convergence in VTH shift variation by enhancing ID effect. The fabricated SRAM macro shows excellent operation margin.
- T-10 **A Fully-integrated Optical Duobinary Transceiver in a 130nm SOI CMOS Technology**, *J. Buckwalter, J. Kim, X. Zheng*, G. Li*, K. Raj*, A. Krishnamoorthy*, UCSD, *Oracle Laboratories*
- A 5-Gb/s, fully-integrated optical duobinary transceiver is demonstrated in a 130-nm silicon-on-insulator CMOS technology. Duobinary modulation is proposed to mitigate opto-electronic bandwidth limitations for photonic ring modulators. The circuit demonstrates an NRZ data eye of 500 uW amplitude and consumes 115 mW for analog and digital portions of the transmitter.
- T-11 **Electrically-Driven Retargeting for Nanoscale Layouts**, *S. Banerjee*, K. B. Agarwal**, S. R. Nassif**, *IBM Research East Fishkill NY, **IBM Research Austin*
- Scaling into the nanometer regime with limited lithographic capabilities leads to printability issues during manufacturing, which are due to lithographically poor target layout shapes. In this paper, we propose to perform electrically-aware modifications of the physical design to improve layout printability with minimum design perturbation. Results on sample 32nm layouts demonstrate that we can obtain required control over delay variability and lithographic yield using this method.
- T-12 **A Partial Tree Vector Quantizer Dynamic Element Matching Technique for Audio Δ - Σ Converters**, *E. Hardy, H. Ihs, C. Dufaza, S. Meillère*, R. Bouchakour*, Primachip SAS, *IM2NP*
- Multi-bit Delta-Sigma modulators are widely used in performing accurate, low-power, and low cost ADCs but their internal feedback DAC exhibits non-linearity. Unwanted tones and noise are generated in the band of interest. We propose in this paper a new vector-based Dynamic Element Matching scheme to avoid this effect.
- T-13 **5 Gbps BPSK CMOS Transmitter with On-Chip Antenna Using Gaussian Monocycle Pulses**, *S. Kubota, N. Sasaki, M. Hafiz, A. Toya, T. Kikkawa, Hiroshima University*
- A CMOS transmitter with on-chip dipole antenna using 65 nm CMOS technology was developed. The transmitter generated BPSK GMP whose center frequency was 10 GHz. GMP signals were

transmitted and received by the on-chip dipole antennas. 5 Gb/s BPSK differential GMP was generated by PRBS of 27 with 1.51 pJ/bit.

T-14 **Amorphous Silicon Current Steering Digital to Analog Converter**, *A. Dey, D R. Allee, Flexible Display Center at Arizona State University*

A 6-bit current steering D/A converter (DAC) is built using only n-channel amorphous silicon (a-Si:H) thin film transistors (TFT) and capacitors. The circuit is built on silicon using a low temperature process, compatible with flexible plastic substrates. The measurements show reasonably good characteristics, achieving a DNL of less than ± 1.2 LSB and INL of less than ± 1.8 LSB.

T-15 **A 65nm CMOS Self-Terminated Open-Drain IDAC Line Driver Suitable for Fast Ethernet Applications**, *Joseph Aziz, Ark-Chew Wong*, Andrew Chen**, Derek Tam, Broadcom Corp., *Semtech Corp., **Lincoln Labs.*

A self-terminated line driver suitable for fast Ethernet operates in class AB mode and combines digital signal processing with low-power analog circuits. It dissipates 108mW, 48% less than an existing state-of-the-art design. It occupies 0.22mm² in a 65nm standard CMOS technology and operates from a 2.5V supply.

T-16 **A High-PSR LDO using Feedforward Supply-Noise Cancellation Technique**, *B. Yang, B. Drost, Sachin Rao, P. K. Hanumolu, Oregon State University*

A feed-forward noise cancellation (FFNC) technique to improve the power supply noise rejection (PSR) of a low dropout regulator (LDO) is presented. The proposed FFNC operates in conjunction with a conventional LDO and extends the noise rejection bandwidth by nearly an order of magnitude. Fabricated in 0.18 μ m CMOS, at 10mA load current, the prototype achieves a PSR of -50dB and -25dB at 1MHz and 10MHz supply noise frequencies, respectively. Compared to a conventional LDO, this represents an improvement of at least 30dB at 1MHz and 15dB at 10MHz. The prototype uses only 20pF load capacitance and occupies an active area of 0.04 mm².

T-17 **A Time-domain Latch Interpolation Technique for Low Power Flash ADCs**, *Jong-In Kim, Wan Kim, Barosaim Sung, Seung-Tak Ryu, KAIST*

A Time-domain latch interpolation technique is presented for low power flash analog-to-digital converter (ADC). The proposed technique reduces the number of first stage latches by half, and reduces power consumption and hardware complexity. A prototype 6bit 1GS/s flash ADC was designed for concept proof in a 90nm CMOS process.

T-18 **Low-Power Block-Level Instantaneous Comparison 7T SRAM for Dual Modular Redundancy**, *Shunsuke Okumura*, Yohei Nakata*, Koji Yanagida*, Yuki Kagiyama*, Shusuke Yoshimoto*, Hiroshi Kawaguchi*, Masahiko Yoshimoto**, **Kobe University, **JST, CREST*

This paper proposes a 7T SRAM that realizes a block-level instantaneous comparison feature. The data size that can be instantaneously compared is scalable. The proposed SRAM can compare 8-kb data in 130.0ns, and reduces power consumption in data comparison by 92.3%, compared to that of a parallel CRC circuit.

T-19 **A 40 nm 144 mW VLSI Processor for Realtime 60 kWord Continuous Speech Recognition**, *Multiple authors same affiliations : G.He, T.Sugahara, T.Fujinaga, Y.Miyamoto, H.Noguchi, S.Izumi, H.Kawaguchi, M.Yoshimoto, Kobe University*

We developed a low-power VLSI chip for 60-kWord real-time continuous speech recognition. We proposed several schemes to reduce the memory bandwidth and the operating clock frequency. We fabricated a VLSI test chip in 40 nm CMOS technology and measured the performance. Results show that the chip described in this paper can perform 60-kWord continuous real-time speech recognition at 126.5 MHz with power consumption of 144 mW and with little accuracy degradation.

T-20 **A Non-Coherent Versatile DPSK Receiver for High Channel-Density Neural Prosthesis**, *Le*

A non-coherent versatile DPSK receiver for high channel-density neural prosthesis is presented. Detailed analyses on the non-idealities in realistic DPSK demodulation require a more adaptable DPSK receiver to ensure robust data recovery. New features such as tunable threshold voltage, area-efficient switched-capacitor array and flexible digital control are incorporated into the design. At a coil separation of 16mm, the receiver achieves a bit error rate of $2e-7$ at a data rate of 2Mbps with a power consumption of 5.4mW.

T-21

Performance, Metastability and Soft-Error Robustness Tradeoffs for Flip-Flops in 40nm CMOS, D. Rennie, D. Li, M. Sachdev, B. Bhuva*, S. Jagannathan*, S-J. Wen**, R. Wong**, University of Waterloo, *Vanderbilt University, **Cisco Systems Inc.

In this paper the design tradeoffs for flip-flops between performance, soft-error robustness and metastability are analyzed. SPICE simulations are used to characterize flip-flop performance and metastability. 40nm flip-flops are fabricated and in radiation testing Quatro flip-flops showed improved SER and metastability compared with both a reference flip-flop and DICE flip-flop.

T-22

A 5-GS/s 4-Bit Flash ADC with Triode-Load Bias Voltage Trimming Offset Calibration in 65-nm CMOS, Junjie Yao, Guangzhou Runxin Information Tech. Co. Ltd., China, and Jin Liu, The University of Texas at Dallas, TX

A 5-GS/s 4-bit ADC is implemented in 65-nm CMOS. Offset calibration is achieved by digitally adjusting the bias voltages of the triode loads in the preamplifier without introducing additional capacitive loading in the analog path and degrading the high-speed performance. The ADC consumes 34.3 mW from a 1.2-V supply at 5 GS/s, and occupies 0.0828mm^2 active area. The ADC achieves 3.93 ENOB with a 2.5-GHz ERBW and a 0.45-pJ/convstep FOM at 5 GS/s.