

## Tuesday Poster Session

Tuesday Evening, September 21  
Cascade/Sierra Ballroom  
5:00 pm – 7:00 pm

- T-1 **A CMOS Programmable Gain Amplifier with a Novel DC-offset Cancellation Technique**, *Xiaojie Chu, Min Lin, Zheng Gong, Yin Shi, Fa Foster Dai\**, Suzhou-CAS Semiconductors Integrated Technology Research Center, \*Auburn University

A programmable gain amplifier with a novel DC offset cancellation technique for IEEE 802.11b/g wireless LAN direct-conversion receiver is presented. An operational amplifier utilizing an improved Miller compensation approach is adopted in this PGA design. A gain tuning range of 0dB to 56dB with 2dB per tuning step is achieved. The DCOC loop is based on a voltage-current negative feedback that includes a switchable bandwidth algorithm to speed up the settling time of DC offset cancellation. The proposed approach requires no external components and demonstrates excellent DC offset cancellation capability in measurement. Fabricated in a 0.13  $\mu\text{m}$  CMOS technology, this PGA dissipates 9.7mW from a 1.2 V supply voltage and occupies an area of 0.17 mm<sup>2</sup>.

- T-2 **A Micropower Delta-Sigma Modulator based on a Self-Biased Super Inverter for Neural Recording Systems**, *Le Wang, Luke Theogarajan, University of California, Santa Barbara*

This paper presents a micropower 2nd order switched-capacitor delta-sigma modulator based on a novel self-biased fully differential super inverter for neural recording systems. The prototype modulator is implemented in a 0.13  $\mu\text{m}$  CMOS process and achieves 68dB DR over the 8 KHz neural signal bandwidth, while consuming only 4.8  $\mu\text{W}$  from 1.2 V supply.

- T-3 **A 1.16mW 69dB SNR (1.2MHz BW) Continuous Time  $\Sigma\Delta$  ADC with Immunity to Clock Jitter**, *Ganesh Balachandran, Venkatesh Srinivasan, Vijay Rentala, Srinath Ramaswamy, Texas Instruments Inc.*

A low-power jitter tolerant 2nd order active-passive continuous-time sigma-delta ADC in 65nm CMOS is presented. The use of just one active Gm-C integrator and a feed-forward path from the ADC's input to the Gm's output helps reduce power consumption. A FIR filter in the outermost feedback path reduces clock jitter impact. For a -2dBFS input, the ADC clocked at 300MHz achieves a 69dB SNR (10KHz – 1.2MHz BW) while consuming 1.16mW from a 1.4V supply.

- T-4 **A 10 bit Piecewise Linear Cascade Interpolation DAC with Loop Gain Ratio Control**, *Sungwoo Lee, Kiduk Kim, Kyusung Park, Changbyung Park, Byunghun Lee, Jinyong Jeon, Seungchul Jung, Jin Huh, Junhyeok Yang, Hyunsik Kim, Gyu-Hyeong Cho, KAIST*

This paper proposes a 10 bit linear interpolation digital-to-analog converter (DAC) with area efficiency and a high resolution for an AMLCD drive. Because this proposed structure implements a 1 bit interpolation circuit with a control block for a loop gain ratio, it shows a wide voltage range of interpolation as well as superior linearity. The proposed circuit is fabricated with Samsung 90nm CMOS 1.5V / 5V technology. The power dissipation is 7 $\mu\text{W}$ /channel, and the chip area of the 10 bit piecewise linear DAC is only 91% of the area of a conventional 8 bit resistor DAC. The INL and DNL properties are +0.8LSB/-0.2LSB and +0.23LSB/-0.23LSB, respectively. The maximum interchannel DVO is 10mV without the application of any offset cancellation techniques.

- T-5 **A 9.15mW 0.22mm<sup>2</sup> 10b 204MS/s Pipelined SAR ADC in 65nm CMOS**, *Young-Deuk Jeon, Young-Kyun Cho, Jae-Won Nam, Kwi-Dong Kim, Woo-Yol Lee\*, Kuk-Tae Hong\*, Jong-Kee*

*Kwon, ETRI, \*LG Electronics*

This paper describes a 10b 204MS/s analog-to-digital converter (ADC) employing a pipelined successive approximation register (SAR) architecture for low power consumption and small area. To improve the operation frequency, the pipelined SAR ADC consists of two channels with a proposed asynchronous timing technique. This technique increases the amplification time of a residue opamp. To reduce power and area, the opamp is shared between two channels. A reference buffer with a deglitch circuit reduces the glitch and settling time of reference voltages. The prototype ADC fabricated in a 65nm CMOS process shows a SNDR of 55.2dB and a SFDR of 63.5dB with a 2.4MHz input at 204MS/s. The ADC occupies 0.22mm<sup>2</sup> and dissipates 9.15mW at a 1.0V supply. The FoM of the ADC is 95.4fJ/conversion-step.

- T-6 **A 9 $\mu$ W 88dB DR Fully-Clocked Switched-Opamp  $\Delta\Sigma$  Modulator with Novel Power and Area Efficient Resonator**, *Jian Xu, Xiaobo Wu, Hanqing Wang, Bill Liu\*, Menglian Zhao, Zhejiang University, China, \*Analog Devices*

A 9 $\mu$ W 88dB DR switched-opamp (SO)  $\Delta\Sigma$  modulator is implemented in a low cost 0.35 $\mu$ m CMOS process. To evaluate the effects of finite voltage gain and 1/f noise clearly, two high efficient methods are introduced. And a new fully switched-off SO with a 50% power saving and double Figure-of-Merit (FOM) over the traditional type is proposed to reduce the total power. Besides, to improve the performance, a novel resonator idea applicable to SO technique is adopted to realize a coefficient of 1/100 with 75% power and 70% area reduction over the conventional design. The FOM of the designed modulator is highest among the collected recent low power modulators.

- T-7 **A Low-Supply PLL with Enhanced Cascode Compensation and a Low-Supply-Sensitivity CCO**, *Xiong Liu, Alan Willson, UCLA*

Multiple techniques are proposed to realize a self-contained low-supply PLL macro that can share a digital supply thereby saving one supply regulator on the board. Enhanced Cascode Compensation features fast and slow loops to regulate the supply noise without the need of a replica. A novel topology for a current controlled oscillator (CCO) improves the supply noise rejection by more than 10 dB. A built-in 0.6V bandgap avoids the need for another 1.8V supply. Implemented in a 0.18- $\mu$ m CMOS process, the whole PLL consumes less than 4 mW for 800-MHz operation. The measured random jitter is less than 2 ps. These features make it ideal for SoC integration.

- T-8 **Realization of 0.7-V Analog Circuits by Adaptive-Vt Operation of FinFET**, *Shin-ichi O'uchi, Kazuhiko Endo, Yongxun Liu, Takashi Matsukawa, Yuki Ishikawa, Junichi Tsukada, Toshihiro Sekigawa, Hanpe Koike, T. Nakagawa, Kunihiro Sakamoto, Meishoku Masahara, National Institute of AIST*

An adaptive-threshold-voltage differential pair and a low-voltage source follower using independent-double-gate- (IDG-) FinFETs are proposed for a low-voltage operational amplifier (op amp). These circuits were implemented by our FinFET technology that enables co-integration of connected-DG- (CDG-) and IDG-FinFETs. The proposed components enable a two-stage op amp to accept the input below the nominal threshold voltage. More than 40-dB gain and 1-MHz GBW in the 500-mV-wide CM input range under 0.7-V supply voltage was estimated by SPICE simulation. Our preliminary silicon implementation demonstrated 0.7-V operation of the proposed source follower.

- T-9 **A Low-power Area-efficient Switching Scheme for Charge-sharing DACs in SAR ADCs**, *Fred Chen, Anantha Chandrakasan, Vladimir Stojanovic, Massachusetts Institute of Technology*

Analysis and experimental results for a new switching scheme and topology for charge-sharing DACs used in SAR ADCs is presented. The SAR algorithm is exploited to develop a switching

scheme that reduces the number of required unit capacitors by nearly 10x over conventional charge sharing DACs without the aid of any additional reference voltages. An 8-bit SAR ADC is implemented in a 90nm CMOS process and consumes 700nW at 0.7V and 100kS/s while occupying 0.0135mm<sup>2</sup>.

- T-10 **A 50-300-MHz Low power and High Linear Active RF Tracking Filter for Digital TV Tuner ICs**, *Yang Sun, Chang-jin Jeong, In-young Lee, Jeong-seon Lee, Sang-gug Lee, Korea Advanced Institute of Science and Technology*

A low power and highly linear CMOS active tracking bandpass filter is presented to overcome a local oscillator harmonic mixing problem for Digital TV tuner ICs. A transconductor linearization technique based on a method of dynamic source degenerated differential pair is adopted to improve the linearity performance. The newly proposed low power high quality factor (Q) biquad and the linearized transconductor with negative resistance load (NRL) enables a low power and high Q RF tracking filter design. The total chip area is 0.25 mm X 0.9 mm. The fabricated tracking filter based on the 0.13 um CMOS process shows 48~300 MHz tracking range with 10~50 MHz bandwidth, more than 38 dB 3rd order harmonic rejection, 6 dB unwanted signal rejection@N+6 channel offset, and a maximum IIP3 of 6 dBm at 5 dB gain while drawing 6.4 mA from a 1.2 V supply.

- T-11 **A 2.6Gb/s 1.56mm<sup>2</sup> Near-Optimal MIMO Detector in 0.18μm CMOS**, *Tae-Hwan Kim, In-Cheol Park, KAIST*

This paper presents an ASIC implementation of a multi-Gb/s MIMO detector targeting 4x4 16-QAM systems. A modified Dijkstra's algorithm and a pre-calculation technique are proposed to improve the throughput up to 2.6Gb/s, and the Euclidean norm computation is approximated to reduce the chip area. The entire detector occupies 1.56mm<sup>2</sup> in 0.18μm CMOS. In achieving a BER of 10<sup>-3</sup>, the performance is only 0.1dB away from that of the optimal detection in terms of SNR.

- T-12 **Design and Analysis of 3D-MAPS: A Many-Core 3D Processor with Stacked Memory**, *Michael B.Healy, Krit Athikulwongse, Rohan Goel, Mohammed M. Hossain, Dae Hyun Kim, Young-Joon Lee, Dean L. Lewis, Tzu-Wei Lin, Chang Liu, Moongon Jung, Brian Ouellette, Mohit Pathak, Hemant Sane, Guan hao Shen, Dong Hyuk Woo, Xin Zhao, Gabriel H. Loh, Hsien-Hsin S. Lee, Sung Kyu Lim, Georgia Institute of Technology*

We describe the design and analysis of 3D-MAPS, a 64-core 3D-stacked memory-on-processor running at 277 MHz with 63 GB/s memory bandwidth, sent for fabrication using Tezzaron's 3D stacking technology. We also describe the design flow used to implement it using industrial 2D tools and custom add-ons to handle 3D specifics.

- T-13 **A Customized Design of DRAM Controller for On-Chip 3D DRAM Stacking**, *Tao Zhang, Kui Wang\*, Yi Feng\*\*, Xiaodi Song\*, Lian Duan, Yuan Xie, Xu Cheng\*\*, Youn-Long Lin\*\*\*, The Pennsylvania State University, \*Peking University Unity Microsystems Technology Co. Ltd, \*\*Peking University, \*\*\*National Tsing Hua University*

This paper introduces the implementation of 3D on-chip memory controller which is integrated in a 3D SoC architecture to demonstrate the feasibility of 3D memory stacking. It also presents a parallel access policy to improve the bandwidth. In addition, the 3D memory stacking is illustrated in the end of paper. The whole chip has been fabricated in Chartered 130nm process with Tezzaron's 3D bonding technology.

- T-14 **A Sub-Threshold FPGA with Low-Swing Dual-V<sup>DD</sup> Interconnect in 90nm CMOS**, *Joseph Ryan, Benton Calhoun, University of Virginia*

This paper presents a sub-threshold field programmable gGate array (FPGA) that uses a low-

swing dual-VDD global interconnect fabric to reduce energy and improve delay. A 90nm chip implements the FPGA with 1134 LUTs, which is 2.7X smaller, 14X faster, and 4.7X less energy than a sub-threshold FPGA using conventional interconnect and 22X less energy than an equivalent FPGA at full VDD.

- T-16 **A 34.7-mW Quad-Core MIQP Solver Processor for Robot Control**, Hiroki Noguchi, Junichi Tani, Yusuke Shimai, Masanori Nishino, Shintaro Izumi, Hiroshi Kawaguchi, Masahiko Yoshimoto, Kobe University

We propose a quad-core mixed integer quadric programming (MIQP) solver processor. The MIQP solver is applicable to hybrid control systems including real-time control robotics. Using multi-core architecture, fixed-point calculations, and branch-and-bound method with high-dispersion performance while processing a 50-variable problem, our design achieves 34.7-mW operation at a frequency of 52 MHz in measurement results, although a core 2 duo PC requires 3.16 GHz to solve it as rapidly.

- T-17 **Data-Dependant Sense-Amplifier Flip-Flop for Low Power Applications**, Farshad Moradi, Charles Augustine, Ashish Goel, Georgeos Karakonstantis, Tuan Vu Cao\*, Dag Wisland\*, Hamid Mahmoodi\*\*, Kaushik Roy, Purdue University, \*University of Oslo, \*\*San Francisco State University,

In this paper, we present a new sense amplifier based flip-flop that exploits input data activity, to achieve reduced power consumption. The internal nodes of the proposed flip-flop are charged/discharged only when the input data changes state. Simulations show that the power consumption of proposed flip-flop is reduced by 20% to 70% compared to standard sense-amplifier flip-flop. An FIR-filter based on the proposed flip-flop, implemented in 45nm ST process, shows more than 42% improvement in power consumption (with 5% delay penalty) compared standard sense-amplifier flip-flops

- T-18 **A 2.5-8Gb/s Transceiver with 5-Tap DFE and Second Order CDR Against 28-inch channel and 5000ppm SSC in 40nm CMOS Technology**, Wei-Chih Chen, Chien-Chun Tsai, Chih-Hsien Chang, Yung-Chow Peng, Fu-Lung Hsueh, Tsung-Hsin Yu, Jinn-Yeh Chien, Wen-Hung Huang, Chi-Chang Lu, Mu-Shan Lin, Chin-Ming Fu, Shu-Chun Yang, Chung-Wing Wong, Wan-Te Chen, Chin-Hua Wen, Li-Yueh Wang, Chiang Pu, TSMC

This paper presents a 2.5-8Gb/s transceiver for PCI Express Gen3.0/2.0/1.0 applications. To overcome channel loss of high bit rate application, a linear equalizer (LEQ) and decision feedback equalizer (DFE) are used to eliminate ISI effect, compensate channel loss, and improve BER performance for 28-inch FR4 channel. The 3-tap feed-forward equalizer (FFE) is used to improve signal quality in transmitter. The resolution of de-emphasis and pre-shoot is up to 1/63 and 1/15. It also performs 0.8UIpp eye opening for 8Gb/s operation. A second order clock and data recovery (CDR) employs digital finite state machine to track phase difference and frequency between clock and data. The CDR can cover 0 to -5000ppm frequency offset of SSC modulation and achieve jitter tolerance of up to 0.2UIpp at 8Gb/s with a BER=10<sup>-10</sup> when all specified jitter sources is included. The integrated transceiver operates from 2.5Gb/s to 8Gb/s and consumes 235mA at 8Gb/s current with 0.95V supply voltage. The test-chip is implemented by flip chip layout and fabricated in TSMC 40nm 0.9V/1.8V CMOS technology. The area of transceiver is 725um x 615um.

- T-19 **A Crosstalk-and-ISI Equalizing Receiver in 2-Drop Single-Ended SSTL Memory Channel**, Jun-Hyun Bae, Young-Soo Sohn\*, Seung-Jun Bae\*, Kwang-Il Park\*, Joo-Sun Choi\*, Young-Hyun Jun\*, Jae-Yoon Sim, Hong-Jun Park, POSTECH, \*Samsung Electronics

An equalizer circuit which minimizes both crosstalk and ISI is applied to a receiver with a strongly-coupled two-parallel two-drop single-ended microstrip SSTL memory channel. The crosstalk equalizer adds a crosstalk-canceling pulse to a victim receiver signal to make the

signal crosstalk-free during the transition interval of an incoming signal. A DFE is used for ISI compensation. The equalization of both crosstalk and ISI increases the data rate for BER < 1E-12 from 2.5Gbps to 3.6Gbps (+44%) with a 0.18µm CMOS process.

T-20 **A 100MHz-to-1GHz Open-Loop ADDLL with Fast Lock-Time for Mobile Applications**, *Mi-Jo Kim, Lee-Sup Kim, KAIST*

This paper presents a fast-lock wide-range all-digital delay locked loops (ADDLL) for mobile applications. The proposed open-loop architecture based on time-to-digital converter (TDC) has a lock time of 3~10 clock cycles. The multi-path delay line is implemented to achieve high resolution in TDC. The frequency range selector is adopted for a wide-range operation. The ADDLL is implemented in a 0.18µm CMOS process and operates from 100MHz to 1GHz.

T-21 **A 16 Gb/s Four-Wire CDMA-Based High Speed I/O Link with Transmitter Timing Adjustment**, *Tzu-Chien Hsueh, Sudhakar Pamarti, University of California, Los Angeles*

A simplified code division multiple access (CDMA) technique has been used to cancel crosstalk in a four-wire signaling high-speed I/O system. To further improve the crosstalk suppression and power efficiency, transmitter (TX) timing adjustment in conjunction with the CDMA-based I/O system is proposed. The integrated transceiver achieves an aggregate 16 Gb/s (5.33 Gb/s/link) data rate and 6 mW/Gb/s/wire power efficiency over four 6" FR4 PCB traces with BER < 1e-12 in a 90 nm standard CMOS technology.

T-22 **Interpolated VCO Design for a Low Bandwidth, Low-Jitter, Self-Biased PLL in 45 nm CMOS**, *David Duarte, Suching Hsu\*, Keng Wong\*\*, Mingwei Huang, Greg Taylor, Intel Corp \*Qualcomm Corp., \*\*Anax Corp.*

A novel self-biased PLL design incorporating a low-gain interpolated inverter-based ring oscillator VCO achieves lower bandwidth and jitter without sacrificing PSRR or area. Charge pump programmability provides an effective mechanism for bandwidth adjustments. Data collected on a high-k, metal gate 45 nm process confirms the suitability of the proposed scheme.

T-23 **Process Variation Tolerant All-Digital Multiphase DLL for DDR3 Interface**, *Heechai Kang, Kyungho Ryu, DongHwan Lee\*, Won Lee\*, SuHo Kim\*, JongRyun Choi\*, Seong-Ook Jung, Yonsei University, \*Samsung Electronics*

An all-digital multiphase DLL is presented that is robust to delay mismatch due to process variation. Each of four 90° phase shift blocks accurately align each phase to 90° delay using its own ring oscillator and locking delay code. Harmonic locking is protected by a ring oscillator and a counter. An area efficient binary to thermometer converter is proposed to diminish the area overhead due to four delay line controllers. An edge combiner is used for duty cycle correction and clock 2x multiplications. The measured large locking delay code difference between four 90° phase shift delay lines in the proposed DLL implemented in 45nm CMOS process, which corresponds to ±31ps at 800MHz, proves that the DLL corrects significant phase error caused by delay mismatch. Phase shift accuracy errors at 90° and 270° phases are 0.43° and 1.01°, respectively, and output frequency is 1.6GHz with 50% duty cycle at 800MHz. Power consumption is 3.3mW at 800MHz.

T-24 **Varactor-Based Signal Restoration for Near-Speed-of-Light Surfing Global Interconnect**, *Suwen Yang, Robert Drost, Mark Greenstreet\*, Shahriar Mirabbasi\*, Frank O'Mahony\*\*, Oracle Corporation, \*University of British Columbia, \*\* Intel Corporation*

We present a varactor-based "near-speed-of-light" interconnect design. The varactors compensate for delay variations enabling a simple, source-synchronous solution for clock-and-data recovery. Furthermore, the varactors provide pulse shaping that reduces ISI. We

implemented these interconnects in the TSMC 90 nm CMOS process and present test results for 16 mm long lines.