

Session 13 - RF Transceivers and Building Blocks

Tuesday Afternoon, September 15
Oak Ballroom

Chair: John Rogers, Carleton University
Co-Chair: Aristotele Hadjichristo, Qualcomm

This session discusses advances in RF transceiver architectures and building blocks. New techniques that will allow radios to handle multiple standards that span multiple bands are presented.

2:00 Introduction

2:05 **A 5.5mA 2.4-GHz Two-Point Modulation Zigbee Transmitter with Modulation Gain Calibration**, Rui Yu, Theng-Tee Yeo,
13-1 Kwang-Hung Tan, Shouxian Mou, Yike Cui, Haifeng Wang, Hwa-Seng Yap, Eugene Ting and Masaaki Itoh, WIPRO Techno Center, Singapore

A 2.4-GHz two-point modulation IEEE 802.15.4 (Zigbee) compliant transmitter is presented. This sigma-delta fractional-N PLL based transmitter is optimized for both low-power and low-cost purposes. A novel closed-loop calibration scheme is proposed to minimize the gain mismatch between two modulation points, which is the main source of error in two-point modulation. Fabricated in a 0.15- μm CMOS process, the proposed transmitter achieves EVM less than 8% for 2-M chips/s MSK modulated signal and consumes 5.5mA under a 1.55-V regulated power supply. The core area is $0.8 \times 1.1 \text{mm}^2$.

2:30 **A SAW-less CMOS CDMA Receiver With Active Tx Filtering**, Himanshu Khatri, Prasad S. Gudem* and Lawrence E.
13-2 Larson, University of California, San Diego, La Jolla, CA, *Qualcomm Inc., San Diego, CA

A CDMA-2000 receiver that eliminates the interstage SAW filter is presented. An active technique is proposed for filtering the transmitter leakage after down conversion. This technique improves the triple-beat (TB) and IIP₂ performances by 6.5 dB each, at the expense of a small increase in DC current and noise.

2:55 **A High Dynamic Range ASK Demodulator for Passive UHF RFID with Automatic Over-Voltage Protection and**
13-3 **Detection Threshold Adjustment**, Ganesh Balachandran and Raymond Barnett, Texas Instruments, Inc., Dallas, TX

This paper presents a passive UHF RFID ASK demodulator that operates over a +24dBm to -14dBm RF input power range. The demodulator automatically adjusts between high sensitivity mode for weak RF signals and over-voltage protection mode for high RF power. The input over-voltage protection circuit is designed to protect the IC from high input power while not impacting the sensitivity at weak input power. The demodulator is comprised of a RF rectifier, a variable gain attenuator with automatic threshold adjustment and a nano-power data slicer. The demodulator handles demodulating signals with a minimum to maximum envelope ratio of 0.8 over the entire input power range, and the data slicer consumes only 160nA from a 0.9 to 1.25V rectified supply. The RFID chip is fabricated in a 0.13 μm analog-CMOS technology and the entire chip occupies an area of 0.55mm^2 .

3:20 **A 1 Watt 1-5 GHz Class B Push-Pull Si/SiGe HBT Power Amplifier**, Tyson Wooten and Lawrence Larson, University of
13-4 *California at San Diego, La Jolla, CA*

A 1-5 GHz, Class B push-pull power amplifier is reported. The amplifier utilized low loss, broadband baluns, coupled spiral inductor transformers, and a differential π -doubler. Output powers of greater than 30 dBm and efficiencies greater than 30% from 1 GHz to 4 GHz have been achieved.

3:45 PM BREAK

4:00 **Challenges in the Design of Cognitive Radios (INVITED)**, Behzad Razavi, University of California, Los Angeles, CA
13-5

Cognitive radios are expected to perform spectrum sensing and communication in the frequency range of tens of megahertz to about 10 GHz. As such, they pose tough architecture and circuit design problems. This paper deals with issues such as broadband, low-noise amplification, multi-decade carrier frequency synthesis, and spectrum sensing. The paper also describes the effect of nonlinearity and local oscillator harmonics, demonstrating that cognitive radios entail more difficult challenges than do software-defined radios. Multi-decade synthesis techniques and RF-assisted sensing methods are also presented.

4:50 **A 29 dBm CMOS Class-E Power Amplifier with 63% PAE Using Negative Capacitance**, Yonghoon Song, Sungho Lee,
13-6 *Jaeyun Lee and Sangwook Nam, Seoul National University, Seoul, Korea*

This paper proposes class-E power amplifier including negative capacitance to optimize shunt drain capacitance. The negative capacitance improves efficiency, compensates for surplus shunt drain capacitance resulting from parasitic capacitance, and is implemented without an external circuit. A cascode single-ended class-E RF power amplifier including driver stage is fabricated using a 0.13- μm standard CMOS technology delivering 29 dBm with 66% drain efficiency and 63% power-added efficiency at 1.8 GHz.

5:15 **CMOS RF Transmitter with Integrated Power Amplifier Utilizing Digital Equalization**, Dae Hyun Kwon, Hao Li, Yuchun

A digitally equalized 3.5-GHz CMOS RF transmitter (TX) with integrated 23-dBm power amplifier (PA) in 0.13- μ m CMOS is presented. I/Q mismatch and memoryless nonlinearities of the whole transmit path, including the severe amplitude and phase distortions of the on-chip Class-B PA, are compensated by a digital, two-dimensional look-up table (2-D LUT) adapted by an LMS algorithm. The equalization results in an efficient TX with minimum analog and RF complexity. When a 20-MHz, 64-QAM OFDM signal with 9.6-dB peak-to-average power ratio(PAPR) was transmitted, the measured average drain efficiency of the PA was 12.5% with a -29.6-dB EVM after equalization. An 8.7-dB EVM improvement was achieved with a regular baseband sample rate of 80 MS/s in a typical 802.11a transmitter. A peak drain efficiency of 55% and a 25-dBm saturated output power were also measured for the same PA in a stand-alone package.

Session 14 - Micro-Robotics and Energy Harvesting

Tuesday Afternoon, September 15
Fir Ballroom

Chairman: Gu-Yeon Wu, Harvard University

2:00 **Introduction**

2:05 **Power And Actuation Challenges For Flying Robotic Insects**, Robert Wood, Harvard SEAS, Cambridge, MA
14-1

2:40 **Hardware Specialization And Acceleration For Ultra Low Power Computing In Microrobotic Bees**, David Brooks, Harvard SEAS, Cambridge, MA
14-2

3:15 **Integrated Power Management – The Case for Switched Capacitor Conversion**, Seth Sanders, University of California, Berkeley, Berkeley, CA
14-3

3:50 PM BREAK

Session 15 - Modeling of Passive Elements and Reliability

Tuesday Afternoon, September 15
Pine Ballroom

Chair: Gennady Gildenblat, Arizona State University
Co-Chair: Hidetoshi Onodera, Kyoto University

The first three papers present advances in modeling and measurements of RF inductors and contact resistance as well as interconnect capacitance extraction. Reliability and circuit aging prediction is the subject of the last two papers.

2:00 **Introduction**

2:05 **RF CMOS is More than CMOS: Modeling of RF Passive Components (INVITED)**, Zhiping Yu, Colin McAndrew*, Tsinghua University, China, *Freescale Semiconductor, Tempe, Az
15-1

This paper details recent progress in modeling of inductors, transformers, and resistors. One- and two-segment inductor models are analyzed, including techniques for modeling distributed effects and coupling through a lossy substrate. Details of accurate physical modeling of polysilicon resistors, including nonlinearities, parasitics, and self-heating, are provided.

2:55 **Measurement and Analysis of Contact Plug Resistance Variability (INVITED)**, Karthik Balakrishnan and Duane Boning, Massachusetts Institute of Technology, Cambridge, MA
15-2

The importance of contacts increases with technology scaling due to higher resistance and variability. techniques for measurement, analysis, and modeling of variation in contacts are presented. A test-chip enables contact plug resistance measurement in 35,000 DUTs. Statistical analysis shows significant layout effects on mean resistance; spatial analysis shows systematic components as well as random, normally distributed variation. Spatial separation-distance correlation is negligible. Future compact models are needed to incorporate such variability information.

3:45 PM BREAK

4:00 **Sensitivity Computation Using Domain-Decomposition for Boundary Element Method Based Capacitance Extractors**, Yu Bi, Kees-Jan van der Kolk and Nick van der Meijs, Delft University of Technology, Delft, The Netherlands
15-3

We present an algorithm that enables an extension of BEM based 3-D capacitance extractors to generate both the nominal capacitances and their sensitivities w.r.t. all geometric parameters with only one extraction. The algorithm is based on the domain-decomposition technique and has been implemented in a layout-to-circuit extractor. It is shown by experiments that the additional cost for the sensitivity computation is less than 20% of the time consumption for standard capacitance extraction.

4:25 **Circuit Aging Prediction for Low-Power Operation**, Rui Zheng, Jyothi Velamala, Vijay Reddy*, Varsha Balakrishnan,

15-4 *Evelyn Mintarno***, *Subhasish Mitra***, *Srikanth Krishnan** and *Yu Cao*, *Arizona State University, Tempe, AZ*, **Texas Instruments, Dallas, TX*, ***Stanford University, Stanford, CA*

Low-power circuit operations pose a unique challenge to aging prediction. Traditional models ignore the impact of the sleep period and thus, overestimate the degradation rate. This work examines critical model assumptions that are responsible for the NBTI effect. It then proposes a new aging model that effectively analyzes the degradation. The new model well predicts the aging behavior of 45nm and 65nm data with different operation patterns, especially sleep mode operation and dynamic voltage scaling.

4:50 **Impact of Transistor Level Degradation on Product Reliability (INVITED)**, *Tanya Nigam*, *GLOBAL FOUNDRIES*,
15-5 *Sunnyvale, CA*

Product level lifetime margins, determined by HCI and BTI, are shrinking with scaling. Accurate device-level HCI degradation models, together with known BTI models, are needed to predict frequency degradation of a ring oscillator. Both NBTI and HCI exhibit relief during AC operation and the respective contribution to RO frequency degradation is a function of applied bias.

Session 16 - 3D ICs and 3D Systems

Tuesday Afternoon, September 15
Cedar Ballroom

Chair: Ann Marie Rincon, SMSC
Co-Chair: Alvin Loke, Advanced Micro Devices

After 40 years of planar ICs the age of 3D is finally dawning. In this session three invited papers describe the newest trends, and three contributed papers demonstrate the power and performance advantages of real silicon

2:00 **Introduction**

2:05 **Trend from ICs to 3D ICs to 3D Systems (INVITED)**, *Rao Tummala*, *Venky Sundaram*, *Ritwik Chatterjee*, *P. Markodeya*
16-1 *Raj*, *Nitesh Kumbhat*, *Vijay Sukumaran*, *Vikay Sridharan*, *Abhishek Choudury*, *Qiao Chen* and *Tapobrata Bandyopadhyay*,
Georgia Institute of Technology, Atlanta, GA

Moore's Law drove the IC industry to a billion transistor chip but major barriers are foreseen beyond 32nm. One alternative may be stacked 3D ICs, a small system part, but miniaturization may require entire system miniaturization. 3D miniaturization described herein includes Si or wafer level interposers with Through-Package-Vias (TPV), nano-scale passives, thermal materials and interfaces and fine pitch system interconnections.

2:55 **The Prospect of 3D-IC (INVITED)**, *Simon Wong* and *Abbas El Gamal*, *Stanford University, Stanford, CA*
16-2

This paper illustrates the performance advantages of 3D integrated circuits with two specific examples, namely 3D-FPGA and 3D-SRAM. Through strategic modification of the architectures to take advantage of 3D, significant improvement in speed and reduction in power consumption can be achieved.

3:20 **47% Power Reduction and 91% Area Reduction in Inductive-Coupling Programmable Bus for NAND Flash Memory**
16-3 **Stacking**, *Mitsuko Saito*, *Yasufumi Sugimori*, *Yoshinori Kohama*, *Yoichi Yoshida*, *Noriyuki Miura*, *Hiroki Ishikuro* and
Tadahiro Kuroda, *Keio University, Japan*

An inductive-coupling programmable bus is developed for NAND-flash-memory stacking. 3-coil channel arrangement scheme enables random access for memory read/write. Transmission power is reduced by 47% compared to [1]. A coil-layout style, XY coil, allows coils covered by logic interconnections, reducing area by 91%. Relayed-data transmission at 1.6Gb/s, BER<10⁻¹² is achieved.

3:45 PM **BREAK**

4:00 **60GHz CMOS/PCB Co-Design and Phased Array Technology (INVITED)**, *Joy Laskar*, *Stephane Pinel*, *Saikat Sarkar*,
16-4 *Padmanavan Sen*, *Bevin Perumana*, *Matthew Leung*, *Debasis Dawn*, *David Yeh*, *Francesco Barale*, *Kevin Chuang*, *Gopal Iyer*,
Jong-Hoon Lee and *Patrick Melet*, *Georgia Institute of Technology, Atlanta, GA*

In this paper, we present a highly integrated 60 GHz CMOS/PCB single-chip digital phased array solution, embedded in QFN package. This represents a unique opportunity to develop low power 60GHz multi-gigabit radio at a similar cost structure as a Bluetooth® radio, addressing the needs of a multitude of bandwidth hungry wireless multimedia applications such as high definition streaming and massive side-loading. The convergence of 60GHz CMOS digital radio, phased array technology, low power multi-gigabit mixed-signal processing low cost filter, phased array antenna embedded in standard package is discussed. In addition, uncompressed HDMI video streaming is demonstrated for the first time, using a standard battery (AAA) operated compact 60GHz CMOS/PCBQFN based module. These solutions offer the lowest energy per bit transmitted wirelessly at multi-gigabit rate, reported till date, to meet the very stringent low-power specifications for battery operated consumer electronic portable devices.

4:50 **The Highly Integrated Mobile WiMAX Module Using Embedded PCB & SIP Technology**, *Jeong-Hoon Cho*, *Hwan-Hee*
16-5 *Lee** and *Jeong-Sik Moon*, *LG Innotek, Ansan-si, Korea*, **Daeduck Electronics, Ansan-si, Korea*

The highly integrated mobile WiMAX module is presented by employing embedded PCB and system in package technology. It is one chip solution that is composed of WiMAX Chipset, memory, EEPROM, TCXO, PMIC and RF Front End. Furthermore, RF components such as LPF, BPF and Balun are embedded in the multilayered organic substrate. The total size of module targeted is 15mm x 15mm x 1.34mm. The measured results of the mobile WiMAX module show the Rx sensitivity of typical -98dBm and error vector modulation of -28dB in the Tx band with 3.3 V supply. The proposed module is compatible with IEEE802.16e standard. In this paper, the high performance RCT (Radio Conformance Test) results of WiMAX module can be achieved by using embedded BPF, LPF with low insertion loss of the 2.07dB and 0.65dB, respectively.

5:15 **System on Chip with 1.12mW-32Gb/s AC-Coupled 3D Memory Interface**, *Roberto Canegallo, Luca Perugini, Alberto*
16-6 *Pasini*, Massimiliano Innocenti, Mauro Scandiuazzo, Roberto Guerrieri* and PierLuigi Rolandi, STMicroelectronics, Agrate,*
*Italy, *University of Bologna, Bologna, Italy*

An AC-coupled 3D memory interface for chip-to-chip communication is implemented in 90nm CMOS technology. It transfers 128 bit words between stacked SRAMs in an ARM-based System on Chip (SoC) platform at 250MHz. This interface requires 0.05mm² of occupation area and achieves a 32Gbit/sec of throughput and an average energy consumption of 35uW/Gbit/sec.

Session 17 – Panel Discussion: Design of High Performance Radios in Bulk-CMOS, SOI, SiGe or GaAs? 4:00 pm – 5:30 pm
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Tuesday Afternoon, September 15
Fir Ballroom

Panel Organizers: Aurangzeb Khan, Everspin Technologies
Alireza Shirvani, Marvell Semiconductor

Panel Moderator: Horacio Mendez, Executive Director, SOI Consortium

Panelists:

Dr. Shayan Farahvash
Senior Engineer, Manager, RF Micro Devices

Jim McMahon
Senior Staff Design Engineer, RF, Cadence

David Haramé
Director of Derivative
and Value Added
Technology Development, IBM

Dr. Jacob Rael
Senior Manager, Broadcom

Thomas Zirkle, MicroPower Global

Semiconductor suppliers need to develop multi-mode and multi-band radio products that meet stringent power dissipation, space and weight constraints as well as FCC and many other regulations, to take advantage of the rapidly growing market for "mobile/portable/pocketable" devices.

While most of today's chips for multi-mode radios can be designed in bulk CMOS, some demand the use of SiGe, GaAs or other materials. As higher frequency applications push the power dissipation and band-width limitations of bulk CMOS, SOI has emerged as a cost-effective alternative to bulk CMOS for an increasing number of RF applications.

The panelists - from semiconductor vendors and an EDA company - will outline these challenges and discuss benefits and trade-offs of the chosen process technologies and circuit design techniques.

Poster Session

Tuesday Evening, September 15
Cascade/Sierra Ballroom
5:00 pm – 7:00 pm

T-1 **A 3 – 14V Rail-to-Rail Constant g_m Opamp in Conventional 0.18 μ m CMOS Process**, *E. Lee, Alfred Mann Foundation*

A 3 – 14V rail-to-rail constant g_m opamp was fabricated in a conventional 0.18 μ m CMOS process using 3.3V I/O devices. Different high-voltage opamp sub-circuits were proposed. For a 14V supply, variations on the input stage g_m were <10.2%. The opamp has a ft of 1.3MHz for a current consumption of 40.7 μ A.

T-2 **An Integrated CMOS Receiver Chip for NMR-Applications**, *J. Anders, P. SanGiorgio, G. Boero, Ecole Polytechnique Federal de Lausanne (EPFL)*

We present the first CMOS-only receiver chip for NMR-applications at 300 MHz. The system consists of an on-chip reception coil, a tuning-capacitor, a down conversion-mixer and a low-frequency gain-stage as well as biasing and offset-compensation circuitry. It has an input referred voltage noise density of 0.7 nV/sqrt(Hz) and a gain of 75 dB. The power consumption is 18 mA from a single 3.3 V supply. The chip is realized in 0.35 μ m technology and occupies an area of 1200 x 850 μ m².

- T-3 **A 1.2-V 2.7-mW 160MHz Continuous-Time Delta-Sigma Modulator with Input-Feedforward Structure**, *J. Zhang, L. Yao, Y. Lian, National University of Singapore, Singapore*
- A power and area efficient continuous-time input-feedforward delta-sigma modulator (DSM) structure is proposed. The coefficients are optimized to increase the input range and reduce the power. The feedforward paths and the summer are embedded into the quantizer, hence the circuit is simplified, and the power consumption and area are reduced. The prototype chip, fabricated in a 0.13- μm CMOS technology, achieves a 68-dB DR (Dynamic Range) and 66.1-dB SNDR (signal-to-noise-and-distortion ratio) over a 1.25-MHz signal bandwidth with a 160-MHz clock. The power consumption of the modulator is 2.7 mW under a 1.2-V supply, and the chip core area is 0.082mm².
- T-4 **Dual-Loop Direct VCO Modulation for Spread Spectrum Clock Generation**, *Christopher D. LeBlanc, Benjamin T. Voegeli, Tian Xia*, IBM, *University of Vermont*
- This paper presents a new spread spectrum clock generator (SSCG) circuit for EMI reduction. The proposed design adopts a standard integer-N phased locked loop (PLL) with two dual-voltage-controlled oscillators (VCOs). A frequency modulation loop is implemented with a digital frequency limit detector to direct the spectrum-spreading profile. An integrator is applied to generate the triangular modulation signal. Comparing with some recent designs [1,2,3,4] in the literature, the spread spectrum clock generator in this paper is simple and area efficient.
- T-5 **Phase Noise in a Synchronized Concurrent Dual-Frequency Oscillator**, *A. Goel, H. Hashemi, University of Southern California*
- The phase noise in synchronized concurrent dual-frequency oscillators is analyzed. The phase noise of an injection locked concurrent dual-frequency oscillator for either of the frequencies follows the phase noise of external injection near that frequency for offsets within the locking bandwidth of the injection. In the system of two coupled concurrent dual-frequency oscillators with bilateral coupling, the phase noise at either frequency is 3dB smaller than that at the free running case for offsets smaller than the locking bandwidth. Measurement results show a good match with the theory.
- T-6 **A Unified Parallel Radix-4 Turbo Decoder for Mobile WiMAX and 3GPP-LTE**, *Ji-Hoon Kim, In-Cheol Park*, Samsung Electronics Co., Ltd., *KAIST, Republic of Korea*
- This paper describes the energy-efficient implementation of a high performance turbo decoder, which is designed to support both Mobile WiMAX and 3GPP-LTE. We propose a new hardware architecture that can share hardware resources for the two standards. It consists of eight retimed radix-4 SISO decoders to achieve high throughput and a dual-mode hardware interleaver. A prototype chip exhibits a decoding rate of more than 100Mb/s with eight iterations while achieving an energy efficiency of 0.31nJ/bit/iter.
- T-7 **Tera-Scale Performance Machine Learning SoC with Dual Stream Processor Architecture for Multimedia Content Analysis**, *T.-W. Chen, C.-S. Tang, S.-F. Tsai, C.-H. Tsai, S.-Y. Chien, L.-G. Chen, National Taiwan University*
- A new SoC architecture for multimedia content analysis is implemented in 90nm CMOS technology. It focuses on the co-acceleration of computer vision and machine learning algorithms, and two stream processors with massively parallel processing elements are integrated to achieve tera-scale performance. In the dual processor architecture, the data are transferred between processors and the high bandwidth dual memory through the local media bus, which reduces the power consumption in the AHB data access.
- T-8 **A Fully Integrated CMOS UHF RFID Reader Transceiver for Handheld Applications**, *J. Wang, C. Zhang, B. Chi, Z. Wang, Z.H. Wang, Tsinghua University of China*
- This paper presents a fully integrated single-chip UHF radio frequency identification (RFID) reader transceiver for short distance handheld applications. The transceiver integrates an OOK modulator and a power amplifier in transmitter chain, an IQ direct-down converter, two operational amplifiers, and two comparators in the receiver chain. A PLL frequency synthesizer is also integrated on the same chip to provide the local oscillating signals for the transceiver. The measured output P1dB power of the transmitter is 16.4dBm and the measured receiver sensitivity is -60dBm. The on-chip integer-N synthesizer achieves a frequency resolution of 200kHz with a phase noise of -92.78 dBc/Hz at 100kHz frequency offset and -124.4 dBc/Hz at 1MHz frequency offset. The reader consumes a total power of 231.2mW when the output power is 16.4dBm. The proposed reader can communicate with commercial tags in a distance of more than 50cm without any off-chip power amplifier. The chip has a die area of 4.5mm*1.3mm including pads.
- T-9 **A 1.5GS/s 4096-Point Digital Spectrum Analyzer for Space-Borne Applications**, *Brian Richards, Nicola Nicolici*, Henry Chen, Kevin Chao, Robert Abiad**, Dan Werthimer, and Borivoje Nikolic, University of California, Berkeley, *McMaster University, **Space Sciences Laboratory*
- A high-performance digital spectrometer backend ASIC has been designed for use with an off-the-shelf ADC frontend. The design is based on an architecture described in Simulink that has been field-tested on FPGA platforms for radio astronomy applications. The architecture maximizes the utilization of operators to nearly 100%. A test structure has been added to the design to support the detection of soft errors, since several space-borne applications may expose the circuit to high-energy particles. An in-house automated design flow was used to map the same Simulink description to a 90nm CMOS ASIC, preserving cycle-accurate and bit-accurate behavior. The chip operates with clock rates up to 390MHz, delivering a throughput of up to 1.56GS/s with 710 mW of power.
- T-10 **REAd/Access-Preferred (REAP) SRAM – Architecture-Aware Bit Cell Design for Improved Yield and Lower V_{MIN}**, *A. Goel, P. Ndai, J.P. Kulkarni, K. Roy, Purdue University*

We present an architecture-aware SRAM design that decouples the conflicting requirements between read stability and writeability. Read and hold failures are reduced by preferentially sizing the cell to have better read stability at the expense of write failures (at iso-area). The increased write failures are handled by stretching the write cycle. Measurement results on a 90nm 2kb test chip show 80mV higher weak-write test voltage, 61%, 25% and 500X reduction in hold, read and write failures, respectively, without any increase in access failures. This results in improved yield relative to an iso-area nominal 6T cell, with only 3% loss in performance (based on architecture level simulation) on average.

T-11 **A 1-V 60- μ W 16-Channel Interface Chip for Implantable Neural Recording**, *W. Liew, X. Zou, L. Yao, Y. Lian, National University of Singapore*

A 1-V 60- μ W 16-channel interface chip dedicated for implantable neural signal recording is presented. To comply with the implantation safety issue, the overall system is optimized for low power dissipation. A power efficient front-end OTA topology and a novel dual-capacitive-array SAR ADC are adopted to achieve better power efficiency. A prototype fabricated in 0.35- μ m CMOS technology achieves NEF of 2.16 and THD of 0.53% at full output swing while providing 16-kSample/s per channel output.

T-12 **CMOS-Based Flexible Multi-Site Retinal Stimulator Toward Retinal Prosthesis Technology**, *T. Tokuda, Y. Takeuchi, T. Noda, K. Sasagawa, and J. Ohta, Nara Institute of Science and Technology*

We developed a CMOS LSI stimulator chip for retinal prosthesis technology with features of (1) multi-site stimulation using an on-chip stimulator, (2) light-controlled (image-based) stimulation. The retinal stimulator was configured as an array of small-sized intelligent CMOS stimulators called a "unit chip." We can set different conditions for each unit chip connected to a single set of 5-channel bus wiring and perform multi-site, constant-current biphasic retinal stimulation. We implemented simple binary light-sensing circuitry on the unit chip to realize image-based patterned stimulation on the retina. We verified that all the implemented functionalities correctly work and characterized the performance of the circuitry. A demonstration for image-based patterned current injection using radially aligned unit chips was also performed.

T-13 **Chemical Microsystem Based on Integration of Microresonant Sensor and CMOS ASIC**, *K. S. Demirci, S. Truax, L. A. Beardslee, O. Brand, Georgia Institute of Technology*

A silicon-based microsystem consisting of a mass-sensitive resonant sensor and a CMOS ASIC containing feedback circuitry is demonstrated for portable sensing applications. The feedback circuitry sustains oscillation of the resonant sensor at its mechanical resonance frequency ranging between 200 and 800 kHz. The microsystem has been used for detection of volatile organic compounds in the gas-phase, and a limit of detection of 13 ppm for toluene is obtained with a frequency stability of 16 mHz.

T-14 **Fixed- and Variable-Length Ring Oscillators for Variability Characterization in 45nm CMOS**, *Ji-Hoon Park, Liang-Teck Pang*, Kenneth Duong**, Borivoje Nikolic, University of California Berkeley, *IBM T.J. Watson Research Center, **Sun Microsystems*

Fixed- and variable-length ring oscillators (RO's) are designed for characterization of circuit-topology induced variations and spatial correlations. A $930\mu\text{m} \times 775\mu\text{m}$ test array is implemented in a low-power 45nm CMOS process. Measurements from the fixed-length RO's quantify an increase in variability with transistor stack height in logic gates and added variability associated to the top transistor in the stack. In addition, Variable-length RO's (VRO's) are designed to measure spatial correlation with a single-gate resolution.

T-15 **An Energy-Recycling (ER) Technique for Field Color Sequential LCD Backlight Driving**, *Ming-Hsin Huang, Yueh-Chang Tsai, Chun-Yu Hsieh, and Ke-Horng Chen, National Chiao Tung University, Hsinchu, Taiwan*

An energy-recycling (ER) technique has been proposed to implement high power conversion efficiency and low cost solution of field color sequential (FCS) LEDs backlight driving. One recycling capacitor CR and one power-transistor MR are added to synchronous boost converter to compose the ER function. When the output voltage of FCS-LEDs backlight driver switches from 40V to 26V for driving RGB LEDs during related time interval, ER technique stops to boost input voltage and switches to recycle energy from output terminal to the recycling capacitor CR. Thus, the output voltage can be rapidly switched between two different voltage levels with minimum power losses. The proposed ER technique has been fabricated by TSMC 40V BCD process. The experimental results demonstrate fast and efficient output voltage tracking performance is achieved by the proposed ER technique.

T-16 **A Monolithic Buck Converter Using Differentially Enhanced Duty Ripple Control**, *J. Fan, X. Li*, J. Park, A. Huang, North Carolina State University, *Texas Instruments Corporation*

This paper reports a monolithic DC-DC buck converter using the differentially enhanced duty ripple control (DE-DRC). Without any compensation circuit, this converter is stable over a wide input and output range with constant switching frequency. The large duty ripple voltage with a big noise margin gives the DE-DRC buck converter good noise immunity. The positive and negative differential difference amplifier gains can adjust the high and low frequency portion of the loop transfer function to achieve fast load transient response and pure resistive output impedance, which is used to achieve the adaptive voltage position (AVP) function. We demonstrated a 1.85MHz single phase converter with wide conversion range of 10%-86.6%. This circuit was implemented in 0.5 μ m BCD process of TI.

T-17 **Nonvolatile SRAM (NV-SRAM) Using Functional MOSFET Merged with Resistive Switching Devices**, *S. Yamamoto**, Y. Shuto**, S. Sugahara**, *Dept. Information Processing, Tokyo Institute of Technology, **CREST, JST, ***ISEL, Tokyo Institute of Technology*

The paper presents functional MOSFET (F-MOSFET) architecture using nonpolar-type resistive switching devices (RSDs) for nonvolatile SRAM (NV-SRAM) application. The architecture can be achieved by connecting a RSD to the source terminal of

an ordinary MOSFET. The current drive capability of the F-MOSFET can be modified by the resistance state of the connected RSD, which is a very useful function for recently emerging nonvolatile logic and reconfigurable logic applications. NV-SRAM can be easily configured with a standard SRAM cell and F-MOSFETs. Using our developed SPICE macromodel for nonpolar-type RSDs, the circuit operation of the proposed NV-SRAM cell was computationally simulated.

T-18 **A Simplified Method for Phase Noise Calculation**, *Massoud Tohidian, Ali Fotowat Ahmady*, Mahmoud Kamarei, University of Tehran, *Sharif University of Technology, Tehran, Iran*

A new phase noise calculation method is proposed in which noise sources are modeled with single tone sources. It uses a nonlinear frequency-domain analysis to calculate total gain from noise sources to the output phase noise. This single tone (ST) simulation directly calculates noise frequency contributions and is much faster than Hajimiri's impulse sensitivity function (ISF) method. A quadrature VCO has been implemented in TSMC 0.18- μm CMOS and the predicted phase noise matches measurement.

T-19 **Design of 2xVDD-Tolerant I/O Buffer with 1xVDD CMOS Devices**, *Ming-Dou Ker, Yan-Liang Lin*, Department of Electronic Engineering, I-Shou University, Kaohsiung, Taiwan, *Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan.*

A new 2xVDD-tolerant I/O buffer realized with only 1xVDD devices has been proposed and successfully verified in silicon. With the dynamic source output technique and the gate-controlled circuit, the proposed I/O buffer can transmit and receive the signals of 2xVDD without suffering gate-oxide reliability issue to meet the mixed-voltage interface applications in microelectronic systems.

T-20 **A 3-Level PWM ADSL2+ CO Line Driver**, *S. Gierkink, K. Lakshmikummar, V. Mukundagiri, D. Lim, A. Muralt, F. Larsen, Conexant Systems Inc.*

A PWM ADSL2+ line driver with 2.2MHz signal bandwidth is realized in a 3 metal, 2 poly 0.35 μm CMOS process. A low 8.832MHz switching frequency is used with filtering in the feedback path to suppress aliasing. Signal processing and triangular wave generation are combined in the forward integrators. The driver delivers 100mW to a 100 Ω line with an MTPR less than -52 dB. Active area is 3mm².

T-21 **A 65nm CMOS, Ring-Oscillator Based, High Accuracy Digital Phase Lock Loop for USB2.0**, *Anant S Kamath, Biman Chattopadhyay, Gopalkrishna Nayak, Texas Instruments Inc.*

A high accuracy, ring-oscillator based Digital PLL is presented here. Sigma-Delta dithering is used for improved frequency accuracy. To reduce noise due to Sigma Delta dithering and to allow for passive filtering of this noise, the Sigma Delta section of the DCO is limited to a small range. This range, however, is not sufficient to account for frequency drifts due to temperature: a novel temperature compensation scheme is used for this purpose. The DPPLL is built in 65nm technology, and provides a 480MHz output, with a phase noise of -103.5dBc/Hz at 1 MHz offset, and a frequency accuracy of +/-100ppm. It supports various input frequencies and does not require an external component.

T-22 **A Phase Detector for 12.5Gbps Clock and Data Recovery with Optimal Detection**, *J. Jang, T. Choi, B. Jung, Purdue University*

We propose a phase detector using a matched filter that maximizes the performance for a given input noise condition. The phase detector is designed for a 12.5Gbps CDR circuit. The performance of the proposed phase detector is compared with a typical one through simulation. A DLL-based clock recovery circuit is also implemented with the proposed phase detector and measured showing noise rejection characteristic.

T-23 **Design-Space Exploration of Backplane Receivers with High-Speed ADCs and Digital Equalization**, *H. Chung, G.-Y. Wei, Harvard University*

This paper presents a backplane receiver model consisting of a simple, accurate, experimentally-verified, and parameterized high-speed flash ADC and a configurable digital equalizer for design-space exploration. Simulations demonstrate tradeoffs between ADC and equalizer bit resolution while maintaining constant receiver performance.

T-24 **A CMOS 3.3-8.4 GHz Wide Tuning Range, Low Phase Noise LC VCO**, *Bodhisatwa Sadhu, Jaehyup Kim, Ramesh Harjani, University of Minnesota*

A novel inductor switching technique is used to implement a wide-band LC VCO in 130nm CMOS. It achieves a tuning range of 87.2% with phase noise between -122 and -117.2 dBc/Hz at 1MHz offset. The resulting PFTN-FOM lies between 6.6 and 10.2 dB which is the best reported to date.

T-25 **Near-Field Communication using Phase-Locking and Pulse Signaling for Millimeter-Scale Systems**, *Yu-Shiang Lin*, Dennis Sylvester, David Blaauw, University of Michigan, *Now with IBM TJ Watson Research Center*

An inductive coupling based proximity communication system is proposed for data readout of remote powered sensor systems with ultra small form factor in $\sim\text{mm}^3$ range for implantable applications. The passive transponder is powered with a 1 \times 1mm on-chip inductor, which also enables readout signaling using pulse signaling. The required resonance frequency for pulse signaling is obtained using a transponder PLL that locks to the incoming frequency transmitted by the reader system. The system is demonstrated with 0.13 μm CMOS technology.