Tuesday Afternoon Program

Session 14 – VCOs, Quadrature VCOs, PLLs and All Digital PLLs

Tuesday Afternoon, September 20
Oak Ballroom

Chair: Rick Booth, Panasonic PWRL
Co-Chair: Earl McCune, Consultant

Signal generation is one of the fundamental building blocks in a wireless system. This session covers advances in VCO implementation, phase locked loops, and the emerging topics of all digital PLLs.

2:00 PM **Introduction**

2:05 PM 14-1 **A Dither-less All Digital PLL for Cellular Transmitters (INVITED),** *L. Vercesi, L. Fanori*, F. De Bernardinis, A. Liscidini*, R. Castello*, Marvell Italia Srl.,* University of Pavia*

Frequency synthesizer for cellular transmitters demands low phase-noise both in-band and out-of-band.. The paper describes the first dither-less ADPLL capable to satisfy both these requirements. These results are achieved exploiting a highly linear 2-dimension Vernier TDC and a very fine frequency resolution DCO. Both building blocks heavily rely on digital calibration techniques to precisely and efficiently implement two-point modulation and spur cancellation in the presence of many implementation impairments

2:55 PM 14-2 **A 0.5-V, 440-µW Frequency Synthesizer For Implantable Medical Devices,** *Wu-Hsin Chen, Wing-Fai Loke, Gabriel J. Thompson, Byunghoo Jung, Purdue University*

This paper presents an ultra-low-power, low-voltage frequency synthesizer designed for medical implantable devices. Several design techniques are adopted to address the issues in ultra-low voltage design. Implemented in a 130-nm CMOS technology, the 0.5-V medical band frequency synthesizer consumes 440uW with a phase noise of -91.5dBc/Hz at 1-MHz frequency offset.

3:20 PM 14-3 **A 4-GHz All Digital Fractional-N PLL with Low-Power TDC and Big Phase-Error Compensation,** *J-Y Lee, M.Park, M.Mhin, S-D Kim, M-Y Park, H-K Yu, Electronics and Telecommunications Research Institute*

This paper presents an all-digital fractional-N PLL with a low-power TDC operating at the retimed reference clock. Two retimed reference clocks are employed to reduce the power of the proposed TDC estimating the fractional phase error between the reference clock and CKV clock. The application of the retimed reference clocks to TDC does not only reduce dynamic power in TDC delay inverter chain, but also simplify □r estimation including a new Tv calculation algorithm. Also, a phase-error compensation block is proposed for compensating for the big phase-error change due to the timing skew of all high-speed counter output bits. And a loop settling scanner is invented to shift DCO operation mode and additionally enhance PLL channel switching time for frequency hopping application. The proposed all-digital PLL represents -36dBc integrated phase noise (1kHz - 20MHz), 778fs rms jitter, 9.6mW power consumption. The channel switching time of the ADPLL is measured as 630ns.

3:45 PM **BREAK**

4:00 PM 14-4 **A Quadrature LO Generator Using Bidirectionally-Coupled Oscillators for 60-GHz Applications,** *M. Hekmat, D. K. Su, B. A. Wooley, Stanford University*

A multiphase reference signal generation technique employing bidirectional coupling solves the frequency ambiguity and off-resonance operation issues in conventional coupled oscillators.

Quadrature signals generated at twice the frequency of the loop drive a 40-GHz single-sideband transmitter that achieves a sideband suppression of 45dB in 90nm CMOS.

4:25 PM 14-5 **A 0.6V Quadrature VCO With Optimized Capacitive Coupling for Phase Noise Reduction,** *Feng Zhao, Fa Foster Dai, Auburn University*

This paper presents a 0.6V quadrature voltage-controlled oscillator (QVCO) with a novel capacitive coupling technique, which is employed not only for quadrature signal coupling, but also for noise reduction. As a result, the proposed QVCO can even achieve 3 to 5dB lower phase noise than a single-phase VCO of the same kind. Optimized capacitive coupling combined with inductive enhance-swing technique enables low-power consumption and low phase noise simultaneously. The QVCO achieves a measured phase noise of -132.3dBc/Hz @ 3MHz offset with a center frequency of 5.6GHz and consumes 4.2mW from a 0.6V supply. This performance corresponds to a Figure-of-Merit (FoM) of 191.5dB. The QVCO RFIC is implemented in a 0.13 μm CMOS technology with core area of 0.6x0.8mm2.

4:50 PM 14-6 **A Combined VCO and Divide-by-Two for Low-Voltage Low-Power 1.6 GHz Quadrature Signal Generation,** *Shen Wang, Dong Sam Ha, Beomsup Kim* and Vipul Chawla*, Virginia Tech, *Qualcomm*

We present a transformer-based VCO stacked with a divide-by-two for low-power quadrature signal generation. The VCO adopts Amstrong VCO configuration to alleviate small headroom and noise coupling encountered. Start-up condition and phase noise performance are analyzed. The LO fabricated in 65 nm CMOS dissipates only 2.6mW under 1V supply.

Session 15 – Phase-Locked Loop and Analog Techniques

Tuesday Afternoon, September 20
Fir Ballroom

Chair: Wei-Zen Chen, NCTU
Co-Chair: Kenneth Szajda, LSI Corporation

This session presents noise suppression techniques for PLL, a nested feedback frequency synthesizer, a high performance VCO using FBAR, and high dynamic range analog techniques.

2:00 PM **Introduction**

2:05 PM 15-1 **A 2.2GHz PLL using a Phase-Frequency Detector with an Auxiliary Sub-Sampling Phase Detector for In-Band Noise Suppression,** *Chun-wei Hsu, Karthik Tripurari, Shih-An Yu, Peter R. Kinget, Columbia University*

Tri-state digital phase-frequency detectors (PFDs) are widely used for the large capture and locking range that they enable, but suffer from relatively large in-band phase noise. Subsampling phase detectors have recently been demonstrated to offer very low in-band noise but with only a very small capture range. We show how a PFD and a sub-sampling phase detector can be combined to maintain the phase-frequency detection capabilities while simultaneously obtaining in-band noise suppression. A 2.2GHz PLL is demonstrated in a 65nm CMOS process with an on-chip loop filter area of 0.04mm^2. The measured in-band phase noise improves from -110dBc/Hz to -122dBc/Hz when the auxiliary sub-sampling phase detector is active.

2:30 PM 15-2 **A Fractional-N Frequency Synthesizer using High-OSR Delta-Sigma Modulator and Nested-PLL,** *Pyoungwon Park, Dongmin Park, SeongHwan Cho, KAIST*

A nested-PLL(NPLL) architecture for low-noise wide-bandwidth fractional-N frequency synthesizer is presented. In order to reduce the quantization noise of the fractional-N PLL, delta-

sigma modulator(DSM) is clocked at nine times of the reference frequency. A band pass filter, implemented in form of a PLL, is added to reduce the noise folding. Prototype implemented in 0.13um CMOS process achieves 26dB quantization noise suppression while consuming 9.6mW and occupying 0.46mm2

2:55 PM 15-3 **A Sub-100µW 2GHz Differential Colpitts CMOS/FBAR VCO,** *Jianlei Shi, Brian P. Otis,University of Washington*

We present a 2GHz FBAR-based differential Colpitts CMOS VCO with gm-boosting. The oscillator works with wide Vdd range(0.51V-1.5V). Under 0.6V nominal supply, the VCO consumes 126 uW and achieves -149 dBc/Hz phase noise at 1MHz offset,showing a FOM of -224dB. The minimum power consumption is 67uW with 0.51V Vdd.

3:20 PM 15-4 **A 60mW 1.15mA/channel Class-G Stereo Headphone Driver with 111dB DR and 120dB PSRR,** *Sherif Galal, Hui Zheng, Khaled Abdelfattah, Vinay Chandrasekhar, Iuri Mehr, Alex Jianzhong Chen, John Platenak, Nir Matalon, Todd L. Brooks, Broadcom Corp.*

A 60mW 111dB DR Class-G Stereo Headphone Driver is described. The driver utilizes higher-order loop filter to achieve PSRR of 120dB at the GSM TDMA rate of 217Hz. A driver architecture that combines Class-G and a split Class-AB/B amplifier reduces the quiescent current to 1.15mA/channel. A dual-voltage charge-pump with a single flying capacitor enables Class-G operation by adjusting the supply rails as a function of the input signal. The driver supports battery range of 2.65V-4.5V and occupies an area of 2.3mm2 in 0.18µm CMOS technology.

3:45 PM **BREAK**

4:00 PM 15-5 **A Multi-GHz Area-Efficient Comparator with Dynamic Offset Cancellation,** *L. Kong, Y. Lu, E. Alon, University of California, Berkeley*

This paper proposes a dynamic impedance modulation technique to significantly improve the speed of comparators utilizing dynamic-offset-cancellation (DOC). Measurements show that proposed technique achieve 6X lower input-referred offset and 9X better power-supply-noise-rejection than a StrongArm comparator with only 20% speed penalty at identical core area (98um2) while dissipating 455uW.

4:25 PM 15-6 ***Zero-Pole* Modulation and Demodulation for Noise Reduction in Charge Amplifiers,** *N. Jaffari, K. Vleugels, B. Wooley, Stanford University*

A novel method of noise reduction, referred to as zero-pole modulation and demodulation, is proposed for charge amplifiers in photo-detection and sensor systems. The experimental charge amplifier achieves a noise reduction of 40% compared to a basic charge amplifier. The input-referred noise of the experimental charge amplifier is 100 ENC.

Session 16 – Embedded Memory Trends

Tuesday Afternoon, September 20
Pine Ballroom

Chair: Koji Nii, Renesas Electronics Corporation
Co-Chair: Chris Kim, University of Minnesota

Embedded memory topics ranging from low voltage SRAMs and emerging non-volatile memories to unclonable ID generation and fast ROMs in advanced technology nodes are presented.

2:00 PM **Introduction**

2:05 PM 16-1 **Device-Conscious Circuit Designs for 0.5-V High-Speed Memory-Rich Nanoscale CMOS LSIs (INVITED),** *A.Kotabe, K.Itoh, R.Takemura, R.Tsuchiya, M.Horiguchi*, Hitachi, Ltd., *Renesas Electronics Corporation*

Repair techniques and nanoscale FD-SOI MOSTs, sub-0.5-V logic circuits, a 0.5-V 1-Gb SRAM/DRAM, and compensations especially for process variations are discussed. Based on the discussion, it is concluded that a 0.5-V memory-rich CMOS LSI is possible while reducing the power to one-tenth that of a conventional 1-V CMOS LSI.

2:55 PM 16-2 **Dynamic Stability in Minimum Operating Voltage *Vmin* for Single-port and Dual-port SRAMs,** *Y. Tsukamoto, T. Kida, T. Yamaki, Y. Ishii, K. Nii, K. Tanaka, S. Tanaka, Y. Kihara, Renesas Electronics Corporation*

We discuss dynamic stability for single-port SRAM by examining Vmin difference between longer and shorter WL pulse width. Regarding dual-port SRAM, the Vmin degradation induced by WL pulse skew between ports in asynchronous operation is studied. The validity of our simulation results are verified by measured data for SRAM modules in 28nm generation.

3:20 PM 16-3 **Characterization of SRAM Sense Amplifier Input Offset for Yield Prediction in 28nm CMOS,** *Mohamed H. Abu-Rahma, Ying Chen, Wing Sy, Wee Ling Ong, Leon Yeow Ting, Sei Seung Yoon, Michael Han, Esin Terzioglu, Qualcomm Incorporated*

A process control monitor for SRAM sense amplifier (SA) offset is implemented in 28nm LP CMOS technology. The all-digital design of the monitor makes it adequate for low voltage testing, high speed data collection, and ease of migration to newer technologies. Detailed measurement results are provided for SA types at different conditions. Statistical yield estimation using the measured sense amplifier offset shows good correlation with measured yield for a 512Kb SRAM.

3:45 PM **BREAK**

4:00 PM 16-4 **Design Challenges for Prototypical and Emerging Memory Concepts Relying on Resistance Switching (INVITED),** *Ch. Muller, D. Deleruyelle, O. Ginez, J-M. Portal, M. Bocquet, IM2NP, Aix-Marseille University*

Integration of functional materials in memory architectures leads to emerging concepts with disruptive performances as compared to conventional charge storage technologies. Beside floating gate solutions such as EEPROM and Flash, these alternative devices involve voltage or current-controlled switching mechanisms between two distinct resistance states. The origin of the resistance change straightforwardly depends upon the nature and fundamental physical properties of func-tional materials integrated in the memory cell. After a general overview of non volatile memories, this paper is focused on prototypical and emerging memory cells and on their ability to withstand a downscaling of their critical dimensions. In addi-tion, despite different maturity levels, a peculiar attention is turned toward common guidelines helpful for designing em-bedded or distributed resistive switching memory circuits.

4:50 PM 16-5 **A 28 nm 50% Power Reduced 2T mask ROM with 0.72 ns Read Access Time Using Column Source Bias,** *Y. Umemoto, K. Nii, J. Ishikawa, K. Okamoto, K. Mori, K. Yanagisawa, Renesas Electronics Corporation*

We propose a new 2T mask ROM with dynamic column source bias control technique, which allows for high-speed operation, low-power consumption and reduction in cross-talk noise. The fabricated 128-kb ROM macro using 28-nm HK+MG technology realizes 0.72ns access time at 0.85V and a half power consumption of conventional ROM macro.

5:15 PM **Improved Circuits for Microchip Identification using SRAM Mismatch,** *Srivatsan Chellappa,*

16-6 *Aritra Dey , Lawrence T. Clark , Arizona State University*

In this paper we present a new, more robust hardware technique for generating secret keys and unique serial numbers using SRAM cells' inherent mismatch due to process variations in the constituent transistors. It is experimentally demonstrated and analyzed on a 90 nm test chip.

Session 17 (Panel Discussion)
Can Heterogeneous MCM Solutions Kill 3D-ICs in Their Infancy?

Tuesday Afternoon, September 20
Cedar Room

2:00pm – 4:00 pm

3D integration improves circuit density and offers a solution to continue on the performance-growth path of Moore's law. 3D-ICs based on vertical integration with TSVs are a promising alternative but not the only one. Heterogeneous integration techniques of multiple ICs such as SiP, silicon-carrier and 3D packaging are becoming mature. Will these alternatives eliminate TSV-based 3D-ICs before their implementation challenges are solved? A panel of experts and industry leaders discusses the promises and hurdles associated with different multi-dimensional integration techniques.

Chair:
Dr. Alberto Valdes-Garcia, Research Staff Member, IBM T. J. Watson Research Center

Moderator:
Prof. Rao Tummala, *Director, Microsystems Packaging Research Center, Georgia Institute of Technology*

Panelists:
Dr. Pol Marchal, *Program Manager for 3D Design Technology, IMEC*
Dr. John Osenbach, *Fellow, Materials and Interconnect Technology World Wide Manufacturing, LSI Company*
Mr. Robert Patti, *CTO and VP of Design Engineering, Tezzaron Semiconductor*
Dr. Rajendra D. Pendse, *VP, Advanced Products and Technology Marketing, STATSChipPAC*
Dr. Christian Val, *Founder & CEO, 3D Plus*
Dr. Subramanian Iyer, *Fellow, IBM Systems & Technology Group*

Poster Session

Tuesday Evening, September 20
Cascade/Sierra Ballroom
5:00 pm – 7:00 pm

T-1 **A Low-Power and Low-Noise 21~29 GHz Ultra-Wideband Receiver Front-End in 0.18 µm CMOS Technology,** *S.L. Huang, Y.S. Lin, J.H. Lee, National Chi Nan University*

This paper presents the design and analysis of a 21~29 GHz CMOS receiver front-end in a standard 0.18 um CMOS process for ultra-wideband (UWB) automotive radar systems. The circuit comprises a low-noise amplifier (LNA), a double-balanced Gilbert-cell mixer, and two Marchand baluns. Over the 21~29 GHz automotive radar band, the receiver front-end exhibited excellent NF of 4.6±0.5 dB and conversion gain of 23.7±1.4 dB. The dc power dissipation was only 39.2 mW.

T-2 **A 2GHz Digital PLL, with Temperature Lock Range of -40°C to 125°C, in 45nm CMOS,** *B. Chattopadhyay, A. S. Kamath, S. Evani, K. Subburaj, Texas Instrument.*

A 45nm, 0.09mm2, 0.5-50MHz input, 2GHz output, ring-oscillator Digital PLL, achieves -90dBC/Hz at 1MHz offset, and a temperature lock range of -40C to 125C. Outputs of any two adjacent current elements of the current-mode DAC in the DCO can be progressively brought out for separate Sigma-Delta (SD) operation. This enables the DPLL to track temperature over a large range, even as the SD step size and range are kept small to minimize jitter.

T-3 **Indirect Phase Noise Sensing for Self-Healing Voltage Controlled Oscillators,** S. Yaldiz, *V. Calayir, X. Li, L. Pileggi, A. Natarajan*, M. Ferriss*, J. Tierno*, Carnegie Mellon University, *IBM TJ Watson Research Center*

The push for higher performance analog/RF circuits in scaled CMOS necessitates self-healing via post-manufacturing tuning. A major challenge with self-healing is the efficient design of on-chip sensors. We propose indirect sensing that exploits the correlations between the performance of interest and those that can be measured using easy-to-integrate sensors.

T-4 **An At-speed Self-testable Technique for the High Speed Domino Adder,** *Yu-Shun Wang, Min-Han Hsieh, Chia-Ming Liu, Chi-Wei Liu, James C.-M. Li, and Charlie Chung-Ping Chen, National Taiwan University*

An at-speed self-testable technique is proposed for the high speed domino adder. We apply pseudo-exhaustive testing so that all testable faults in the 64-bit adder are detected by just 23K patterns. The adder latency is accurately measured by the programmable-skew clock generated from delay-locked loop (DLL). The proposed technique is validated on a 6.4GHz 64- bit domino adder with 181ps latency in 90nm CMOS technology. This on-chip technique is very useful for at-speed testing and speed binning of high performance CPU.

T-5 **A 95dB SNDR Audio ΔΣ Modulator in 65nm CMOS,** *L. Liu, D. Li,Y. Ye, L. Chen, Z. Wang, Tsinghua University*

A DT single loop 3rd order 5-bit ΔΣ modulator is implemented in 65nm CMOS. The modulator achieves 95dB SNDR with 24 kHz bandwidth and consumes only 371μW from 1V supply. SNDR keeps at 90.2dB with 133μW under 0.6V. The core area is 0.41mm2.

T-6 **A Fully Integrated CMOS Nanoscale Biosensor Microarray,** *Lei Zhang, Xiangqing He, Yan Wang, Zhiping Yu, Tsinghua University*

This paper presents a fully integrated CMOS microarray for biosensor applications. A 64-pixel working electrode array with optimized reference and counter electrode structure is proposed to improve symmetry, and the feature sizes of electrodes have been scaled down to 600nm. The circuit utilizes the decoding scheme of memories to simplify the pixel design while shares potentiostat opamp and current amplifers, which allows the miniaturization of electrodes and enables large-scale integration of the microarray. The demo is fabricated in 0.18μm CMOS technology, and experimental results successfully demonstrated the biosensing detections on the nanoscale microarray. The circuit provides a current gain of 19.9dB, 3dB bandwidth of 15kHz, dynamic range of 141dB, sensing sensitivity of 37.6pA, and a driving capability of 0.46mA, respectively.

T-7 **A Passive UHF Tag for RFID-based Train Axle Temperature Measurement System,** *Jianqin Qian, Chun Zhang, Liji Wu, Xijin Zhao, Dingguo Wei, Zhihao Jiang, Yuhui He, Tsinghua University*

A fully integrated passive UHF RFID tag with embedded temperature sensor, compatible with the ISO/IEC 18000 type 6C protocol, is developed in a standard 0.18μm CMOS process, which is designed to measure the axle temperature of a running train. The consumption of RF/analog front-end circuits is 1.556μA@1.0V, and power dissipation of digital part is 5μA@1.0V. The CMOS temperature sensor exhibits a conversion time under 2 ms, less than 7 μW power dissipation, resolution of 0.31□/LSB and error of +2.3/-1.1 □ with a 1.8 V power supply for range from -35 □

to 105 □. Measured sensitivity of tag is -5dBm at room temperature.

T-8 **A 48-mW, 12-bit, 150MS/s Pipelined ADC with Digital Calibration in 65nm CMOS,** *B. Peng, G.-Z. Huang, H. Li*, P.-Y. Wan, P.-F. Lin*, Beijing University of Technology, *University of Science and Technology of China*

Digital calibrated pipelined ADC with peak SNDR=67dB,peak SFDR=81dB at 150MS/s sampling rate in 65nm CMOS process.

T-9 **Statistical V_{TH} Shift Variation Self-Convergence Scheme Using Near Threshold V_{WL} Injection for Local Electron Injected Asymmetric Pass Gate Transistor SRAM,** *K. Miyaji, Y. Shinozuka, S. Miyano*, K. Takeuchi, University of Tokyo, *STARC*

Statistical VTH shift variation in asymmetric pass gate transistor by local electron injection is studied. VD effect is self-compensated by ID effect. Near threshold VWL self-convergence injection is proposed to achieve self-convergence in VTH shift variation by enhancing ID effect. The fabricated SRAM macro shows excellent operation margin.

T-10 **A Fully-integrated Optical Duobinary Transceiver in a 130nm SOI CMOS Technology,** *J. Buckwalter, J. Kim, X. Zheng*, G. Li*, K. Raj*, A. Krishnamoorthy*, University of California, San Diego, *Oracle Laboratories*

A 5-Gb/s, fully-integrated optical duobinary transceiver is demonstrated in a 130-nm silicon-on-insulator CMOS technology. Duobinary modulation is proposed to mitigate opto-electronic bandwidth limitations for photonic ring modulators. The circuit demonstrates an NRZ data eye of 500 uW amplitude and consumes 115 mW for analog and digital portions of the transmitter.

T-11 **Electrically-Driven Retargeting for Nanoscale Layouts,** *S. Banerjee, K. B. Agarwal*, S. R. Nassif*, IBM Research East Fishkill NY, *IBM Research Austin*

Scaling into the nanometer regime with limited lithographic capabilities leads to printability issues during manufacturing, which are due to lithographically poor target layout shapes. In this paper, we propose to perform electrically-aware modifications of the physical design to improve layout printability with minimum design perturbation. Results on sample 32nm layouts demonstrate that we can obtain required control over delay variability and lithographic yield using this method.

T-12 **A Partial Tree Vector Quantizer Dynamic Element Matching Technique for Audio Δ-Σ Converters,** *E. Hardy, H. Ihs, C. Dufaza, S. Meillère*, R. Bouchakour*, Primachip SAS, *IM2NP*

Multi-bit Delta-Sigma modulators are widely used in performing accurate, low-power, and low cost ADCs but their internal feedback DAC exhibits non-linearity. Unwanted tones and noise are generated in the band of interest. We propose in this paper a new vector-based Dynamic Element Matching scheme to avoid this effect.

T-13 **5 Gbps BPSK CMOS Transmitter with On-Chip Antenna Using Gaussian Monocycle Pulses,** *S. Kubota, N. Sasaki, M. Hafiz, A. Toya, T. Kikkawa, Hiroshima University*

A CMOS transmitter with on-chip dipole antenna using 65 nm CMOS technology was developed. The transmitter generated BPSK GMP whose center frequency was 10 GHz. GMP signals were transmitted and received by the on-chip dipole antennas. 5 Gb/s BPSK differential GMP was generated by PRBS of 27 with 1.51 pJ/bit.

T-14 **Amorphous Silicon Current Steering Digital to Analog Converter,** *A. Dey, D R. Allee, Flexible Display Center at Arizona State University*

A 6-bit current steering D/A converter (DAC) is built using only n-channel amorphous silicon (a-

Si:H) thin film transistors (TFT) and capacitors. The circuit is built on silicon using a low temperature process, compatible with flexible plastic substrates. The measurements show reasonably good characteristics, achieving a DNL of less than ±1.2 LSB and INL of less than ±1.8 LSB.

T-15 **A 65nm CMOS Self-Terminated Open-Drain IDAC Line Driver Suitable for Fast Ethernet Applications,** *Joseph Aziz, Ark-Chew Wong*, Andrew Chen**, Derek Tam, Broadcom Corp., *Semtech Corp., **Lincoln Labs.*

A self-terminated line driver suitable for fast Ethernet operates in class AB mode and combines digital signal processing with low-power analog circuits. It dissipates 108mW, 48% less than an existing state-of-the-art design. It occupies 0.22mm2 in a 65nm standard CMOS technology and operates from a 2.5V supply.

T-16 **A High-PSR LDO using Feedforward Supply-Noise Cancellation Technique,** *B. Yang, B. Drost, Sachin Rao, P. K. Hanumolu, Oregon State University*

A feed-forward noise cancellation (FFNC) technique to improve the power supply noise rejection (PSR) of a low dropout regulator (LDO) is presented. The proposed FFNC operates in conjunction with a conventional LDO and extends the noise rejection bandwidth by nearly an order of magnitude. Fabricated in 0.18um CMOS, at 10mA load current, the prototype achieves a PSR of -50dB and -25dB at 1MHz and 10MHz supply noise frequencies, respectively. Compared to a conventional LDO, this represents an improvement of at least 30dB at 1MHz and 15dB at 10MHz. The prototype uses only 20pF load capacitance and occupies an active area of 0.04 mm^2.

T-17 **A Time-domain Latch Interpolation Technique for Low Power Flash ADCs,** *Jong-In Kim, Wan Kim, Barosaim Sung, Seung-Tak Ryu, KAIST*

A Time-domain latch interpolation technique is presented for low power flash analog-to-digital converter (ADC). The proposed technique reduces the number of first stage latches by half, and reduces power consumption and hardware complexity. A prototype 6bit 1GS/s flash ADC was designed for concept proof in a 90nm CMOS process.

T-18 **Low-Power Block-Level Instantaneous Comparison 7T SRAM for Dual Modular Redundancy,** *Shunsuke Okumura*, Yohei Nakata*, Koji Yanagida*, Yuki Kagiyama*, Shusuke Yoshimoto*, Hiroshi Kawaguchi*, Masahiko Yoshimoto*,**, *Kobe University, **JST, CREST*

This paper proposes a 7T SRAM that realizes a block-level instantaneous comparison feature. The data size that can be instantaneously compared is scalable. The proposed SRAM can compare 8-kb data in 130.0ns, and reduces power consumption in data comparison by 92.3%, compared to that of a parallel CRC circuit.

T-19 **A 40 nm 144 mW VLSI Processor for Realtime 60 kWord Continuous Speech Recognition,** *G. He, T. Sugahara, T. Fujinaga, Y. Miyamoto, H. Noguchi, S. Izumi, H. Kawaguchi, M. Yoshimoto, Kobe University*

We developed a low-power VLSI chip for 60-kWord real-time continuous speech recognition. We proposed several schemes to reduce the memory bandwidth and the operating clock frequency.We fabricated a VLSI test chip in 40 nm CMOS technology and measured the performance. Results show that the chip described in this paper can perform 60-kWord continuous real-time speech recognition at 126.5 MHz with power consumption of 144 mW and with little accuracy degradationn.

T-20 **A Non-Coherent Versatile DPSK Receiver for High Channel-Density Neural Prosthesis,** *Le*

Zheng, Kuanfu Chen, Wentai Liu, University of California, Santa Cruz

A non-coherent versatile DPSK receiver for high channel-density neural prosthesis is presented. Detailed analyses on the non-idealities in realistic DPSK demodulation require a more adaptable DPSK receiver to ensure robust data recovery. New features such as tunable threshold voltage, area-efficient switched-capacitor array and flexible digital control are incorporated into the design. At a coil separation of 16mm, the receiver achieves a bit error rate of 2e-7 at a data rate of 2Mbps with a power consumption of 5.4mW.

T-21 **Performance, Metastability and Soft-Error Robustness Tradeoffs for Flip-Flops in 40nm CMOS,** *D. Rennie, D. Li, M. Sachdev, B. Bhuva*, S. Jagannathan*, S-J. Wen**, R. Wong**, University of Waterloo, *Vanderbilt University, **Cisco Systems Inc.*

In this paper the design tradeoffs for flip-flops between performance, soft-error robustness and metastability are analyzed. SPICE simulations are used to characterize flip-flop performance and metastability. 40nm flip-flops are fabricated and in radiation testing Quatro flip-flops showed improved SER and metastability compared with both a reference flip-flop and DICE flip-flop.

T-22 **A 5-GS/s 4-Bit Flash ADC with Triode-Load Bias Voltage Trimming Offset Calibration in 65-nm CMOS,** Junjie Yao, Guangzhou Runxin Information Tech. Co. Ltd., China, and Jin Liu, The University of Texas at Dallas, TX

A 5-GS/s 4-bit ADC is implemented in 65-nm MCOS. Offset calibration is achieved by digitally adjusting the bias voltages of the triode loads in the preamplifier without introducing additional capacitive loading in the analog path and degrading the high-speed performance. The ADC consumes 34.3 mW from a 1.2-V supply at 5 GS/s, and occupies 0.0828mm^2 active area. The ADC achieves 3.93 ENOB with a 2.5-GHz ERBW and a 0.45-pJ/convstep FOM at 5 GS/s.