

Session 14 – VCOs, Quadrature VCOs, PLLs and All Digital PLLs

Tuesday Afternoon, September 20
Oak Ballroom

Chair: Rick Booth, Panasonic PWRL
Co-Chair: Earl McCune, Consultant

Signal generation is one of the fundamental building blocks in a wireless system. This session covers advances in VCO implementation, phase locked loops, and the emerging topics of all digital PLLs.

2:00 PM **Introduction**

2:05 PM **A Dither-less All Digital PLL for Cellular Transmitters (INVITED)**, *L. Vercesi, L. Fanori*,
14-1 F. De Bernardinis, A. Liscidini*, R. Castello*, Marvell Italia Srl.,* University of Pavia*

Frequency synthesizer for cellular transmitters demands low phase-noise both in-band and out-of-band.. The paper describes the first dither-less ADPLL capable to satisfy both these requirements. These results are achieved exploiting a highly linear 2-dimension Vernier TDC and a very fine frequency resolution DCO. Both building blocks heavily rely on digital calibration techniques to precisely and efficiently implement two-point modulation and spur cancellation in the presence of many implementation impairments

2:55 PM **A 0.5-V, 440- μ W Frequency Synthesizer For Implantable Medical Devices**, *Wu-Hsin
14-2 Chen, Wing-Fai Loke, Gabriel J. Thompson, Byunghoo Jung, Purdue University*

This paper presents an ultra-low-power, low-voltage frequency synthesizer designed for medical implantable devices. Several design techniques are adopted to address the issues in ultra-low voltage design. Implemented in a 130-nm CMOS technology, the 0.5-V medical band frequency synthesizer consumes 440uW with a phase noise of -91.5dBc/Hz at 1-MHz frequency offset.

3:20 PM **A 4-GHz All Digital Fractional-N PLL with Low-Power TDC and Big Phase-Error
14-3 Compensation**, *J-Y Lee, M.Park, M.Mhin, S-D Kim, M-Y Park, H-K Yu, Electronics and
Telecommunications Research Institute*

This paper presents an all-digital fractional-N PLL with a low-power TDC operating at the retimed reference clock. Two retimed reference clocks are employed to reduce the power of the proposed TDC estimating the fractional phase error between the reference clock and CKV clock. The application of the retimed reference clocks to TDC does not only reduce dynamic power in TDC delay inverter chain, but also simplify ϕ r estimation including a new T_v calculation algorithm. Also, a phase-error compensation block is proposed for compensating for the big phase-error change due to the timing skew of all high-speed counter output bits. And a loop settling scanner is invented to shift DCO operation mode and additionally enhance PLL channel switching time for frequency hopping application. The proposed all-digital PLL represents - 36dBc integrated phase noise (1kHz - 20MHz), 778fs rms jitter, 9.6mW power consumption. The channel switching time of the ADPLL is measured as 630ns.

3:45 PM **BREAK**

4:00 PM **A Quadrature LO Generator Using Bidirectionally-Coupled Oscillators for 60-GHz Applications**, *M. Hekmat, D. K. Su, B. A. Wooley, Stanford University*
14-4

A multiphase reference signal generation technique employing bidirectional coupling solves the frequency ambiguity and off-resonance operation issues in conventional coupled oscillators. Quadrature signals generated at twice the frequency of the loop drive a 40-GHz single-sideband transmitter that achieves a sideband suppression of 45dB in 90nm CMOS.

4:25 PM **A 0.6V Quadrature VCO With Optimized Capacitive Coupling for Phase Noise Reduction**, *Feng Zhao, Fa Foster Dai, Auburn University*
14-5

This paper presents a 0.6V quadrature voltage-controlled oscillator (QVCO) with a novel capacitive coupling technique, which is employed not only for quadrature signal coupling, but also for noise reduction. As a result, the proposed QVCO can even achieve 3 to 5dB lower phase noise than a single-phase VCO of the same kind. Optimized capacitive coupling combined with inductive enhance-swing technique enables low-power consumption and low phase noise simultaneously. The QVCO achieves a measured phase noise of -132.3dBc/Hz @ 3MHz offset with a center frequency of 5.6GHz and consumes 4.2mW from a 0.6V supply. This performance corresponds to a Figure-of-Merit (FoM) of 191.5dB. The QVCO RFIC is implemented in a 0.13 μm CMOS technology with core area of 0.6x0.8mm².

4:50 PM **A Combined VCO and Divide-by-Two for Low-Voltage Low-Power 1.6 GHz Quadrature Signal Generation**, *Shen Wang, Dong Sam Ha, Beomsup Kim* and Vipul Chawla*, Virginia Tech, *Qualcomm*
14-6

We present a transformer-based VCO stacked with a divide-by-two for low-power quadrature signal generation. The VCO adopts Armstrong VCO configuration to alleviate small headroom and noise coupling encountered. Start-up condition and phase noise performance are analyzed. The LO fabricated in 65 nm CMOS dissipates only 2.6mW under 1V supply.

Session 15 – Phase-Locked Loop and Analog Techniques

Tuesday Afternoon, September 20
Fir Ballroom

Chair: Wei-Zen Chen, NCTU
Co-Chair: Kenneth Szajda, LSI Corporation

This session presents noise suppression techniques for PLL, a nested feedback frequency synthesizer, a high performance VCO using FBAR, and high dynamic range analog techniques.

2:00 PM **Introduction**

2:05 PM **A 2.2GHz PLL using a Phase-Frequency Detector with an Auxiliary Sub-Sampling Phase Detector for In-Band Noise Suppression**, *Chun-wei Hsu, Karthik Tripurari, Shih-An Yu, Peter R. Kinget, Columbia University*
15-1

Tri-state digital phase-frequency detectors (PFDs) are widely used for the large capture and locking range that they enable, but suffer from relatively large in-band phase noise. Subsampling phase detectors have recently been demonstrated to offer very low in-band noise but with only a very small capture range. We show how a PFD and a sub-sampling phase detector can be combined to maintain the phase-frequency detection capabilities while simultaneously obtaining in-band noise suppression. A 2.2GHz PLL is demonstrated in a 65nm CMOS process with an on-chip loop filter area of 0.04mm². The measured in-band phase noise improves from -110dBc/Hz to -122dBc/Hz when the auxiliary sub-sampling phase detector is active.

2:30 PM
15-2

A Fractional-N Frequency Synthesizer using High-OSR Delta-Sigma Modulator and Nested-PLL, *Pyoungwon Park, Dongmin Park, SeongHwan Cho, KAIST*

A nested-PLL(NPLL) architecture for low-noise wide-bandwidth fractional-N frequency synthesizer is presented. In order to reduce the quantization noise of the fractional-N PLL, delta-sigma modulator(DSM) is clocked at nine times of the reference frequency. A band pass filter, implemented in form of a PLL, is added to reduce the noise folding. Prototype implemented in 0.13um CMOS process achieves 26dB quantization noise suppression while consuming 9.6mW and occupying 0.46mm²

2:55 PM
15-3

A Sub-100μW 2GHz Differential Colpitts CMOS/FBAR VCO, *Jianlei Shi, Brian P. Otis, University of Washington*

We present a 2GHz FBAR-based differential Colpitts CMOS VCO with gm-boosting. The oscillator works with wide Vdd range(0.51V-1.5V). Under 0.6V nominal supply, the VCO consumes 126 uW and achieves -149 dBc/Hz phase noise at 1MHz offset, showing a FOM of -224dB. The minimum power consumption is 67uW with 0.51V Vdd.

3:20 PM
15-4

A 60mW 1.15mA/channel Class-G Stereo Headphone Driver with 111dB DR and 120dB PSRR, *Sherif Galal, Hui Zheng, Khaled Abdelfattah, Vinay Chandrasekhar, Iuri Mehr, Alex Jianzhong Chen, John Platenak, Nir Matalon, Todd L. Brooks, Broadcom Corp.*

A 60mW 111dB DR Class-G Stereo Headphone Driver is described. The driver utilizes higher-order loop filter to achieve PSRR of 120dB at the GSM TDMA rate of 217Hz. A driver architecture that combines Class-G and a split Class-AB/B amplifier reduces the quiescent current to 1.15mA/channel. A dual-voltage charge-pump with a single flying capacitor enables Class-G operation by adjusting the supply rails as a function of the input signal. The driver supports battery range of 2.65V-4.5V and occupies an area of 2.3mm² in 0.18μm CMOS technology.

3:45 PM

BREAK

4:00 PM
15-5

A Multi-GHz Area-Efficient Comparator with Dynamic Offset Cancellation, *L. Kong, Y. Lu, E. Alon, University of California, Berkeley*

This paper proposes a dynamic impedance modulation technique to significantly improve the speed of comparators utilizing dynamic-offset-cancellation (DOC). Measurements show that proposed technique achieve 6X lower input-referred offset and 9X better power-supply-noise-rejection than a StrongArm comparator with only 20% speed penalty at identical core area (98um²) while dissipating 455uW.

4:25 PM **Zero-Pole Modulation and Demodulation for Noise Reduction in Charge Amplifiers**, *N. Jaffari, K. Vleugels, B. Wooley, Stanford University*
15-6

A novel method of noise reduction, referred to as zero-pole modulation and demodulation, is proposed for charge amplifiers in photo-detection and sensor systems. The experimental charge amplifier achieves a noise reduction of 40% compared to a basic charge amplifier. The input-referred noise of the experimental charge amplifier is 100 ENC.

Session 16 – Embedded Memory Trends

Tuesday Afternoon, September 20
Pine Ballroom

Chair: Koji Nii, Renesas Electronics Corporation
Co-Chair: Chris Kim, University of Minnesota

Embedded memory topics ranging from low voltage SRAMs and emerging non-volatile memories to unclonable ID generation and fast ROMs in advanced technology nodes are presented.

2:00 PM **Introduction**

2:05 PM **Device-Conscious Circuit Designs for 0.5-V High-Speed Memory-Rich Nanoscale CMOS LSIs (INVITED)**, *A.Kotabe, K.Itoh, R.Takemura, R.Tsuchiya, M.Horiguchi*, Hitachi, Ltd., *Renesas Electronics Corporation*
16-1

Repair techniques and nanoscale FD-SOI MOSTs, sub-0.5-V logic circuits, a 0.5-V 1-Gb SRAM/DRAM, and compensations especially for process variations are discussed. Based on the discussion, it is concluded that a 0.5-V memory-rich CMOS LSI is possible while reducing the power to one-tenth that of a conventional 1-V CMOS LSI.

2:55 PM **Dynamic Stability in Minimum Operating Voltage V_{min} for Single-port and Dual-port SRAMs**, *Y. Tsukamoto, T. Kida, T. Yamaki, Y. Ishii, K. Nii, K. Tanaka, S. Tanaka, Y. Kihara, Renesas Electronics Corporation*
16-2

We discuss dynamic stability for single-port SRAM by examining V_{min} difference between longer and shorter WL pulse width. Regarding dual-port SRAM, the V_{min} degradation induced by WL pulse skew between ports in asynchronous operation is studied. The validity of our simulation results are verified by measured data for SRAM modules in 28nm generation.

3:20 PM **Characterization of SRAM Sense Amplifier Input Offset for Yield Prediction in 28nm CMOS**, *Mohamed H. Abu-Rahma, Ying Chen, Wing Sy, Wee Ling Ong, Leon Yeow Ting, Sei Seung Yoon, Michael Han, Esin Terzioglu, Qualcomm Incorporated*
16-3

A process control monitor for SRAM sense amplifier (SA) offset is implemented in 28nm LP CMOS technology. The all-digital design of the monitor makes it adequate for low voltage testing, high speed data collection, and ease of migration to newer technologies. Detailed measurement results are provided for SA types at different conditions. Statistical yield estimation using the measured sense amplifier offset shows good correlation with measured

yield for a 512Kb SRAM.

3:45 PM

BREAK

4:00 PM
16-4

Design Challenges for Prototypical and Emerging Memory Concepts Relying on Resistance Switching (INVITED), *Ch. Muller, D. Deleruyelle, O. Ginez, J-M. Portal, M. Bocquet, IM2NP, Aix-Marseille University*

Integration of functional materials in memory architectures leads to emerging concepts with disruptive performances as compared to conventional charge storage technologies. Beside floating gate solutions such as EEPROM and Flash, these alternative devices involve voltage or current-controlled switching mechanisms between two distinct resistance states. The origin of the resistance change straightforwardly depends upon the nature and fundamental physical properties of functional materials integrated in the memory cell. After a general overview of non volatile memories, this paper is focused on prototypical and emerging memory cells and on their ability to withstand a downscaling of their critical dimensions. In addition, despite different maturity levels, a peculiar attention is turned toward common guidelines helpful for designing embedded or distributed resistive switching memory circuits.

4:50 PM
16-5

A 28 nm 50% Power Reduced 2T mask ROM with 0.72 ns Read Access Time Using Column Source Bias, *Y. Umemoto, K. Nii, J. Ishikawa, K. Okamoto, K. Mori, K. Yanagisawa, Renesas Electronics Corporation*

We propose a new 2T mask ROM with dynamic column source bias control technique, which allows for high-speed operation, low-power consumption and reduction in cross-talk noise. The fabricated 128-kb ROM macro using 28-nm HK+MG technology realizes 0.72ns access time at 0.85V and a half power consumption of conventional ROM macro.

5:15 PM
16-6

Improved Circuits for Microchip Identification using SRAM Mismatch, *Srivatsan Chellappa, Aritra Dey, Lawrence T. Clark, Arizona State University*

In this paper we present a new, more robust hardware technique for generating secret keys and unique serial numbers using SRAM cells' inherent mismatch due to process variations in the constituent transistors. It is experimentally demonstrated and analyzed on a 90 nm test chip.

<p>Session 17 (Panel Discussion) Can Heterogeneous MCM Solutions Kill 3D-ICs in Their Infancy?</p>

Tuesday Afternoon, September 20
Cedar Room

2:00pm – 4:00 pm

3D integration improves circuit density and offers a solution to continue on the performance-growth path of Moore's law. 3D-ICs based on vertical integration with TSVs are a promising alternative but not the only

one. Heterogeneous integration techniques of multiple ICs such as SiP, silicon-carrier and 3D packaging are becoming mature. Will these alternatives eliminate TSV-based 3D-ICs before their implementation challenges are solved? A panel of experts and industry leaders discusses the promises and hurdles associated with different multi-dimensional integration techniques.

Chair:

Dr. Alberto Valdes-Garcia, Research Staff Member, IBM T. J. Watson Research Center

Moderator:

Prof. Rao Tummala, *Director, Microsystems Packaging Research Center, Georgia Institute of Technology*

Panelists:

Dr. Pol Marchal, *Program Manager for 3D Design Technology, IMEC*

Dr. John Osenbach, *Fellow, Materials and Interconnect Technology World Wide Manufacturing, LSI Company*

Mr. Robert Patti, *CTO and VP of Design Engineering, Tezzaron Semiconductor*

Dr. Rajendra D. Pendse, *VP, Advanced Products and Technology Marketing, STATSChipPAC*

Dr. Christian Val, *Founder & CEO, 3D Plus*

Dr. Subramanian Iyer, *Fellow, IBM Systems & Technology Group*