

**Technical Sessions
Tuesday, September 21 – Afternoon**

Luncheon Keynote

Tuesday, 12:20 pm, September 21

Sierra Ballroom

Tickets for the luncheon are for sale at the Conference Registration Desk

From Pistons and Gears to Electronics and Software: The Coming Transportation Technology Disruption, *Ian Wright, Wrightspeed*



Electric vehicles have been around for more than a century. Heavy, ugly, slow, expensive, with short range and short life, they have been limited to golf carts and forklifts. From grocery getters to Formula One cars, pistons and gears have been the hot technology. That's about to change. Advances in battery technology, control and power electronics make electric drive the hot technology now. From parcel delivery vans to ultra-high performance cars, electric drive offers higher performance at a 10 times efficiency improvement, and

for the first time, shifts transportation away from a total dependence on oil. In this Keynote, Ian Wright explains how this is possible, why it is inevitable, and how much fun it will be for engineers. The implications for vehicle electronics systems architecture are profound.

Ian Wright has over 20 years of experience as an entrepreneur and an operating executive. Since co-founding Tesla Motors in 2003, Ian has focused on electric drive system technology for vehicles. He founded Wrightspeed in 2005, building the world's fastest street-legal electric car as an early demonstrator. It's still unbeaten in 2010. Wrightspeed builds Range-Extended Electric Vehicle drive systems for high fuel consumption vehicles. Prior to Tesla, Ian was a co-founder or senior executive in several networking technology startups, including Altamar Networks (optical switching and ultra-long-haul transmission), QPSX (802.6 MAN), and Scitec (T1 TDMs.) He has also worked for some larger companies: DEC, NET (ATM switches) and Cisco (the terabit router project, for which he holds two patents.) Ian has broad interests in engineering from microelectronics through racecars and aeronautics. He has been a successful amateur racing driver, and is now an active pilot and owner of an experimental airplane. These interests extend to the social, economic, and policy implications of technology; in 2008 he was invited to consult with the NZ Government on the feasibility and implications of electrification of the vehicle fleet. A native New Zealander, Ian has lived and worked in Auckland, Sydney, and Perth before moving to Silicon Valley in 1993.

Session 14 – Novel Simulation and Modeling Techniques

Tuesday Afternoon, September 21

Oak Ballroom

Chair: Larry Nagel, Omega Enterprises Consulting

Co-Chair: Hong-Ha Vuong, LSI Corporation

This session presents three novel, specialized simulation techniques for analog circuit design. In addition, there are two papers that present novel transmission line models.

2:00 **Introduction**

2:05 **Loop Finder Analysis for Analog Circuits**, *G. Peter Fang, Rod Burt, Ning Dong, Texas*
14-1 *Instruments*

The loop finder (LF) analysis is a newly developed method for automatic loop identification and full chip stability analysis. It allows designers to find local potentially problematic return loops in their analog circuits. Node impedance transfer functions in pole-residue format are utilized to generate second-order continuous-time system that approximate the loops. This method was implemented in our in-house Spice-like simulator and has been very helpful identifying instability problems.

2:30 **Noise Analysis of Non-Linear Dynamic Integrated Circuits**, *Amir Zjajo, Qin Tang, Michel*
14-2 *Berkelaar, Nick van der Meijs, Delft University of Technology*

A time-domain methodology for noise analysis of non-linear dynamic integrated circuits with arbitrary excitations is presented. A non-stationary stochastic noise process is described as an Ito system of stochastic differential equations and a numerical solution for such a set of equations is found. Statistical simulation of specific circuits fabricated in 65 nm CMOS process shows that the proposed numerical methods offer accurate and efficient solution of stochastic differentials for noise analysis of integrated circuits.

2:55 **Setup Time, Hold Time and Clock-to-Q Delay Computation under Dynamic Supply Noise**,
14-3 *Takaaki Okumura, Masanori Hashimoto**, *Semiconductor Technology Academic Research Center, *Osaka University*

This paper discusses how to cope with dynamic power supply noise in FF timing estimation. We first review the dependence of setup and hold time on supply voltage, and point out that setup time is more sensitive to supply voltage than hold time and hold time at nominal voltage is reasonably pessimistic. We thus propose a procedure to estimate setup time and clock-to-Q delay taking into account given voltage drop waveforms using an equivalent DC voltage approach. Experimental results show that the proposed procedure estimates setup time and clock-to-Q delay fluctuations well with 5% and 3% errors on average.

3:20 **Modelling and Measurement on minimum-width Transmission-lines from 10-67 GHz in 65**
14-4 **nm CMOS**, *Paul van Zeijl, Henry van der Zanden, Bob Theunissen, Henk Termeer, Philips Research*

Transmission-line models for high-frequency wideband applications should preferably directly relate to the physical dimensions and effects. Various simulation modes (both linear and non-linear in the frequency- and time-domain) point towards the use of a straightforward model using frequency dependent resistances, inductances, and capacitances. However, not all simulators accept frequency dependent elements. This paper presents the design, characterisation and modelling results of 35, 50 and 70 ohm minimum-width transmission lines and 90 degree corners in the TSMC 65 nm process for high frequency (10-67 GHz) applications using frequency-independent elements.

3:45 **A Novel Equivalent Circuit For On Chip Transmission Lines Modeling**, *Dajie Zeng,*
14-5 *Hongrui Wang*, Dongxu Yang*, Li Zhang*, Yan Wang*, Zhiping Yu*, Yaohui Zhang, Institute of SINANO, Tsinghua University*

Microstrip transmission line (MS), coplanar waveguide transmission line (CPW), grounded coplanar waveguide transmission line (GCPW), slow-wave transmission line with slotted grounded shields (GSCPW), and slow-wave transmission line with slotted floating shields (FSCPW) are widely used in silicon technology. Because the quasi-TEM assumption is still valid in these structures, an equivalent circuit is proposed to model all these structures. In this work, we notice that for some types of transmission lines, say GCPW and GSCPW, the per unit

length capacitance increases with frequency. An LC series subcircuit is proposed to model this phenomenon. For CPW, GCPW, GSCPW and FSCPW, the model has very good accuracy and fits the measurement results very well up to the highest measurement frequency (40GHz). For MS, the results from the 3D EM simulation software are adopted and the model shows a great agreement with the simulation results up to the highest simulation frequency (100GHz).

4:10 **BREAK**

Session 15 – 3D Design Considerations

Tuesday Afternoon, September 21
Fir Ballroom

Chair: Rakesh Patel, GlobalFoundries
Co-Chair: John Biggs, ARM LTD.

Stacking die introduces stress levels and thermal distribution challenges that are significantly higher than in 2D. This session introduces TSV related design-verification challenges and solutions, as well as mitigating low power techniques.

2:00 **Introduction**

2:05 **Verifying Electrical/Thermal/Thermo-mechanical Behavior of a 3D Stack – Challenges and Solutions (INVITED)**, *Geert Van der Plas, Steven Thijs, Dimitri Linten, Guruprasad Katti, Paresh Limaye, Abdelkarim Mercha, Michele Stucchi, Herman Oprins, Bart Vandeveld, Nikolas Minas, Miro Cupac, Morin Dehan, Marc Nelis, Rahul Agarwal, Wim Dehaene, Youssef Travaly, Eric Beyne, Paul Marchal, IMEC*

We describe the design challenges for a low-cost 130nm 3D CMOS technology with 5µm diameter at 10µm pitch Cu-TSV. We investigate electrical, thermal and thermo-mechanical issues encountered in 3D. The electrical yield and ESD of TSVs is reviewed and designers are advised how to ensure yield and reliability. For thermal and thermo-mechanical we'll indicate based on experimental characterization, the importance of extending the chip package co-design flow with thermo-mechanical simulations of the chip stack. We propose a new design flow which leverages information captured by smart samples.

2:55 **Simulation Methodology and Flow Integration for 3D IC Stress Management**, *Mark Nakamoto, Riko Radojcic, Wei Zhao, Vinay K. Dasarapu*, Aditya P. Karmarkar*, Xiaopeng Xu*, Qualcomm Inc., *Synopsys Inc.*

This paper describes a method/flow to model stress in 3D packed chip stacks. A new methodology to bridge package and silicon domain simulations is demonstrated using a new data file to facilitate stress information exchange. The flow integration uses equivalent stress conditions to replace sensitive process information and parameterized modules to minimize user interventions for 3D IC stress simulations.

3:20 **Ultra-Low Power Circuit Techniques for a New Class of Sub-mm³ Sensor Nodes (INVITED)**, *Yoonmyung Lee, Gregory Chen, Scott Hanson, Dennis Sylvester, David Blaauw, University of Michigan*

Bell's Law predicts continual reductions in the size of computing systems. We investigate the status of the next paradigm shift that will usher in ubiquitous computing – sub-mm³ sensor nodes. However, this form factor remains beyond the capabilities of modern integrated circuit design techniques due to battery size. This paper describes new ultra-low power circuit techniques applied to digital processors, memory, power management, and a special focus on

standby mode operation, that will bring mm3 sensor nodes to reality.

4:10 **BREAK**

Session 16 – Optical Communication IC's and PLL's

Tuesday Afternoon, September 21
Pine Ballroom

Chair: Gu-Yeon Wei, Harvard University
Co-Chair: Wei-Zen Chen

This section presents high performance transceivers and drivers for multi-gigabits optical communications and advanced PLL techniques for wireline systems.

2:00 **Introduction**

2:05 **A 25 Gb/s × 4-channel 74 mW/ch Transimpedance Amplifier in 65 nm CMOS**, *Takashi*
16-1 *Takemoto, Fumio Yuki, Hiroki Yamashita, Shinji Tsuji, Tatsuya Saito, Shinji Nishimura, Hitachi, Ltd.*

25 Gb/s × 4-channel transimpedance amplifier has been realized in 65-nm CMOS technology. It achieves transimpedance gain of 69.8 dB Ω , bandwidth of 22.8 GHz, and gains flatness of ± 2 dB after equalizing the effect of transmission loss, incorporating gain-stage amplifier with flat frequency response, and 50 Ω output driver with an analogue equalizer. Our TIA dissipates only 74 mW/ch and demonstrates the transimpedance bandwidth products per DC power of 952.1 GHz Ω /mW and crosstalk of under -17dB.

2:30 **Progress and Trends in Multi-Gbps Optical Receivers with CMOS Integrated**
16-2 **Photodetectors (INVITED)**, *Anthony Chan Carusone, Hemesh Yasotharan, Tony Kao, University of Toronto*

There has been significant recent progress towards the realization of multi-Gbps optical receivers fully integrated into standard CMOS processes. Although CMOS photodetectors exhibit performance inferior to discrete photodetectors, they offer the potential for a low-cost highly-integrated solution that suits growing and emerging applications in short-reach optical communication. Past work has focused on using the pn-junctions and depletion regions available in standard CMOS process flows to eliminate, minimize, or cancel the slowly diffusing photocarriers that usually limit the bandwidth of CMOS photodetectors. However, if considered simply as a form of ISI, the slowly diffusing carriers can be dealt with using the same signal processing tools in wide use for other wireline communication applications, including decision feedback equalization. A combination of spatially-modulated light detection, analog equalization, and modest decision feedback equalization appears to offer a path towards data rates in excess of 10-Gbps using integrated photodetectors. Nanoscale CMOS is particularly well suited to the implementation of such signal processing functions. Measured results of photodetectors implemented in a standard 65-nm CMOS process are presented.

3:20 **A 40-Gb/s Optical Transceiver Front-end in 45nm SOI CMOS Technology**, *Joohwa Kim,*
16-3 *James Buckwalter, University of California-San Diego*

A low-power, 40-Gb/s optical transceiver front-end is demonstrated in a 45 nm silicon on insulator (SOI) CMOS technology. A modulator driver uses floating body devices to realize voltage swing of 2 VPP with a small-signal gain of 7.6 dB over 33 GHz. The optical receiver consists of a transimpedance amplifier (TIA) and post-amplifier with 55-dB $\cdot\Omega$ of transimpedance over 30 GHz. The group delay variation is ± 3.9 ps over the 3-dB bandwidth and the average

input-referred noise density is 20.47 pA/√Hz. The TIA consumes 9 mW from a 1 V supply for a transimpedance figure of merit of 1874.5 Ω/pJ. To the author's knowledge, this represents the lowest power consumption for a transmitter and receiver operating at 40-Gb/s in a CMOS process.

3:45
16-4 **A 25Gb/s Laser Diode Driver with Mutually Coupled Peaking Inductors for Optical Interconnects**, *Norio Chujo, Tsuneo Kawamata, Kenichi Ohhata*, Toshinobu Ohno*, Hitachi Ltd., *Kagoshima University*

This paper describes a LD driver for optical interconnects. A main driver with mutually coupled peaking inductors and pre-driver with CMOS dual-loop active-feedback makes possible 25Gb/s operation with low power consumption (142mW, 5.7mW/Gb/s) and small area occupation (95x115μm²).

4:10 **BREAK**

4:25
16-5 **A 16Gbps Laser-Diode Driver with Interwoven Peaking Inductors in 0.18-μm CMOS**, *Takeshi Kuboki, Yusuke Ohtomo*, Akira Tsuchiya, Keiji Kishine**, Hidetoshi Onodera, Kyoto University, *NTT Corporation, **University of Shiga Prefecture*

A laser-diode (LD) driver with interwoven mutually-coupled peaking inductors for high-speed optical networks is presented. Six and four inductors are interwoven into two sets of inductors for area-effective implementation as well as performance enhancement. The proposed circuit is fabricated in CMOS 0.18-μm process. The circuit area is 0.34mm² and the maximum operating speed is 16Gbps. Compared to a conventional LD driver in 0.18-μm CMOS, the proposed circuit achieves 1.6 times faster operation, 26% smaller area with 60% reduction in power consumption under the condition for the same amount of data transmission and the LD driving current.

4:50
16-6 **An Energy-Efficient Ring-Oscillator Digital PLL**, *John Crossley, Eric Naviasky*, Elad Alon, University of California, Berkeley, *Cadence*

A linear but fully digital phase control path and a bang-bang frequency control path enable an energy-efficient digital ring-oscillator PLL architecture. A 65nm CMOS prototype occupies 150μm x 170μm of area and generates a 3GHz clock from a 300MHz reference with 1.13ps rms period jitter while consuming 2mW from a single 1V power supply.

5:15
16-7 **An Offset Phase-Locked Loop Spread Spectrum Clock Generator for SATA III**, *Chin-Yu Lin, Chun-Yu Chiang, Tai-Cheng Lee, National Taiwan University*

A spread spectrum clock generator (SSCG) based on an offset phase-locked loop (OPLL) for the Serial AT Attachment 3 (SATA-III) is presented in this paper. The SSCG can be applied to many systems due to its characteristic of spreading the energy of frequency harmonics and reducing the radiated power per unit bandwidth. In the proposed architecture, a low-frequency spread spectrum signal is synthesized by a direct digital frequency synthesizer (DDFS) and mixed with a high frequency signal to produce a higher modulated reference source. The OPLL is employed to lock its output with the modulated reference to generate the desired spread spectrum clock. This SSCG is fabricated in a 0.13-μm RF CMOS technology and its area is 0.7 x 0.45 mm². It reduces main tone power by 16dB while drawing 21.16 mW from a 1.2 V supply.

Session 17 – On Die Test and Debug Enabler at 65nm and Beyond

Tuesday Afternoon, September 21
Cedar Ballroom

Chair: Manoj Sachdev, University of Waterloo
Co-Chair: Gordon Roberts, McGill University

The first two papers discuss how embedded circuits can be used to identify/debug 45 nm silicon. The third paper demonstrates how an antenna matrix can be used to develop the SOC EMI profile.

2:00 **Introduction**

2:05 **Dynamic Variation Monitor for Measuring the Impact of Voltage Droops on**
17-1 **Microprocessor Clock Frequency**, *Keith Bowman, Carlos Tokunaga, James Tschanz, Arijit Raychowdhury, Muhammad Khellah, Bibiche Geuskens, Shih-Lien Lu, Paolo Aseron, Tanay Karnik, Vivek De, Intel Corporation*

A 45nm microprocessor integrates a dynamic variation monitor (DVM) to measure dynamic path-level frequency changes. Measurements reveal the sensitivity of the microprocessor maximum clock frequency (Fmax) to high-frequency voltage droops and demonstrate the DVM capability of tracking Fmax changes to within 1% for a wide range of voltage droop profiles.

2:30 **Dynamic NBTI Management Using a 45nm Multi-Degradation Sensor**, *Prashant Singh, Eric*
17-2 *Karl*, Dennis Sylvester, David Blaauw, University of Michigan, Ann Arbor, *Intel*

We propose a low power unified oxide and NBTI degradation sensor designed in 45nm process node. The cell power consumption is 105 lower than a previously proposed sensor. The unified nature enables efficient reliability monitoring with reduced sensor deployment effort and area overhead. Using the sensor Dynamic NBTI Management (DNM) has been implemented for the first time. DNM trades the excess 'reliability-margin' present in the design, due to better than worst case operating conditions, with performance. For the typical case shown in this paper, DNM allows for an average boost of 90mV in accelerated supply voltage while bringing down the excess NBTI margin of 22.5mV to 8mV where the total NBTI budget was of 66mV.

2:55 **EMI Camera LSI (EMcam) with 12 x 4 On-Chip Loop Antenna Matrix in 65-nm CMOS to**
17-3 **Measure EMI Noise Distribution with 60- μ m Spatial Precision**, *Naoki Masunaga, Koichi Ishida, Makoto Takamiya, Takayasu Sakurai, University of Tokyo*

An EMI Camera LSI (EMcam) with a 12 x 4 on-chip 250 μ m x 50 μ m loop antenna matrix in 65nm CMOS is developed. EMcam achieves both the 2D electric scanning and 60 μ m-level spatial precision for the first time. The down-conversion architecture increases the bandwidth of EMcam and enables the measurement of EMI spectrum. Shared IF block scheme is proposed to alleviate the increasing power and area penalty inherent to the matrix measurement. 'Mixer and antenna selector (MAS)' reduces the switches and prevents the EMI attenuation due to the switches. EMI measurement with the smallest 32 μ m x 12 μ m antenna to date is also demonstrated.

Session 18 -Panel Discussion Will "Digital RF" Replace RFIC Designers in Ten Years?

Tuesday Afternoon, September 21
Cedar Ballroom

4:25pm – 5:30pm

Over the years, RF IC designers have taken pride in their craft as being the “black magic”, requiring highly skillful and creative minds to craft the circuits operating at high frequencies. Such art, however, has reached a level of maturity and publications reflect efforts to utilize high frequency sampling and signal processing techniques to replace the traditional analog frontends, and make these circuits more amenable to technology scaling and the possibly of automatic synthesis and placement. A panel of experts discusses the possibility of such techniques becoming mainstream, and replacing the “black magic” trade of RFIC designers in ten years.

Moderator:

Prof. Behzad Razavi, *Professor, UCLA*

Panelists:

Dr. Hooman Darabi, *Sr. Engineering Director, Broadcom Corp.*

Mr. Srenik Mehta, *Engineering Director, Atheros Communications*

Prof. Ali Niknejad, *Professor, UC Berkeley*

Prof. Jacques Rudell, *Professor, University of Washington*

Dr. Khurram Waheed, *Senior Systems Engineer, Freescale Semiconductor*