

Session 9 - Nyquist Rate ADC's

Tuesday Morning, September 15
Oak Ballroom

Chair: Eric Naviasky, Cadence
Co-Chair: Ronald Kapusta, Analog Devices

4 designs extending pipeline speeds to 160MSPS at 12-bits and power down to <10mW at 10-bits, 50MHz. The session continues with a SAR calibration technique and two 6-bit converters pushing 1+ GSPS.

9:00 **Introduction**

9:05 **A 10b 50MS/s Opamp-Sharing Pipeline A/D With Current-Reuse OTAs**, *Kailash Chandrashekar and Bertan Bakkaloglu, Arizona State University, Tempe, AZ*

A 10b opamp-sharing pipeline A/D using current-reuse OTAs is presented. The current-reuse OTA, with two NMOS differential inputs, facilitates opamp-sharing between consecutive stages and constant transistor biasing to minimize power consumption. The A/D is fabricated in 0.18 μ m CMOS process and achieves SNDR>57.5dB with 9.2mW analog power consumption at 50MS/s.

9:30 **A 12-b 56MS/s Pipelined ADC in 65nm CMOS**, *Adrian Leuciuc, William Evans, Honghao Ji, Eric Naviasky and Xinhua He, Cadence Design Systems, Columbia, MD*

This paper describes a 1.2V, 12-b pipelined ADC implemented in a 65nm CMOS process. The circuit design techniques used to obtain high gain operational amplifiers in a deep-submicron process are described. A novel top-level simulation methodology is used to quantify the transient errors in each subrange stage, allowing their optimal design. The circuit employs various techniques for power reduction: class A-B op-amps, improved reference design, and frequency-to-current biasing.

9:55 **A 9.43-ENOB 160MS/s 1.2V 65nm CMOS ADC Based on Multi-Stage Amplifiers**, *Young-Ju Kim, Hee-Cheol Choi, Kyung-Hoon Lee, Gil-Cho Ahn, Seung-Hoon Lee, Ju-Hwa Kim*, Kyoung-Jun Moon*, Michael Choi*, Kyoung-Ho Moon*, Ho-Jin Park* and Byeong-Ha Park*, Sogang University, Seoul, Korea, *Samsung Electronics Co., Gyeonggi-Do, Korea*

A 12-bit 160MS/s pipeline ADC is presented. The proposed multipath frequency-compensation technique enables the conventional RNMC-based three-stage amplifier to achieve a stable operation. The measured differential and integral nonlinearities are less than 0.69LSB and 1.00LSB respectively. The ADC shows a FoM of 0.75pJ/conv-step at 160MS/s and 1.2V.

10:20 **A Continuous-Time Input Pipeline ADC with Inherent Anti-Alias Filtering**, *David Gubbins*, Sunwoo Kwon, Bumha Lee**, Pavan Kumar Hanumolu and Un-Ku Moon, *Linear Technology, Colorado Springs, CO, Oregon State University, Corvallis, OR, **National Semiconductor, Santa Clara, CA*

The first continuous-time input pipeline Nyquist rate ADC architecture with inherent anti-alias filtering is introduced. Such an approach overcomes many of the challenges associated with a pure switched-capacitor architecture. Inherent anti-alias filtering is implemented in the first stage MDAC using first order Sinc filtering and a simple RC filter, allowing the possibility of eliminating costly anti-alias filters. The effect of switched capacitor sampling distortion is reduced. This architecture also eases the jitter requirements of the ADC clock when compared to switched capacitor pipeline ADCs. 9.85 ENOB is achieved with 21.4mW analog power from a 1.8V supply at 26MSPS in a 0.18 μ m CMOS process.

10:45 AM **BREAK**

11:05 **Split Capacitor DAC Mismatch Calibration in Successive Approximation ADC**, *Yanfei Chen, Xiaolei Zhu, Hirota Tamura*, Masaya Kibune*, Yasumoto Tomita*, Takayuki Hamada*, Masato Yoshioka*, Kiyoshi Ishikawa*, Takeshi Takayama*, Junji Ogawa*, Sanroku Tsukamoto* and Tadahiro Kuroda, Keio University, Yokohama, Japan, *Fujitsu Laboratories Ltd., Kawasaki, Japan*

A split capacitor DAC calibration method is proposed that a bridge capacitor larger than conventional design allows a tunable capacitor to compensate for mismatch. To guarantee proper calibration, a comparator with digital timing control offset cancellation is proposed. An 8-bit successive approximation ADC with 4b+4b split capacitor DAC calibration has been implemented in 65nm CMOS, achieving 0.3LSB DNL and INL with 180fF input capacitance.

11:30 **A 6b 3GS/s Flash ADC with Background Calibration**, *Masashi Kijima, Kenji Ito, Kuniyoshi Kamei and Sanroku Tsukamoto*, Fujitsu VLSI Ltd., Kasugai, Japan, *Fujitsu Laboratories Ltd., Kawasaki, Japan*

A 6b 3GS/s flash ADC is implemented in a 90nm CMOS process. The proposed ADC is based on an interpolating flash architecture without a T/H. To overcome the offset mismatch among comparators, an interleaved offset calibration system is applied. The ADC achieves the ENOB of 5.8bit at 3GS/s and the ERBW of 500MHz, while consuming 90mW from a 1.2V supply. The ADC occupies a 0.28mm² area.

11:55 **A 1-GS/s 6-bit 6.7-mW ADC in 65-nm CMOS**, *Jing Yang, Thura Lin Naing and Bob Brodersen, University of California, Berkeley, CA*

An asynchronous 6bit 1GS/s ADC is achieved by time inter-leaving two ADCs based on binary successive approximation algorithm (SA) using a capacitive ladder. The semi-close loop asynchronous technique eliminates the high internal clocks and significantly speeds up the SA algorithm. One bit redundancy is implemented to compensate the process variation of parasitic and the MOM capacitance. Fabricated in 65nm CMOS with an active area of 0.11mm², it achieves a peak SNDR of 31.5dB at 1 GS/s sampling rate and has a power consumption of 6.7mW for the analog and digital processing.

Session 10 - Power Management

Tuesday Morning, September 15
Fir Ballroom

Chair: Raj Amirtharajah, University of California, Davis
Co-Chair: Cory Arnold, Maxim Integrated Products

Effective power management requires innovative circuits to optimize system cost and efficiency. This session includes advancements in integrated magnetics, switching regulators, and charge pumps.

9:00 AM **Introduction**

9:05 **Integrating Magnetics for On-Chip Power: Challenges and Opportunities (INVITED)**, *Charles R. Sullivan, Thayer School of Engineering at Dartmouth, Hanover, NH*

Integration of efficient power converters requires a technology for efficient, high-power on-chip inductors. The state of the art is reviewed, and possible future developments are discussed for both air-core and magnetic-core inductors. Performance limits and scaling are analyzed. General design possibilities are outlined and different approaches are compared. Magnetic materials are reviewed, and nano-granular composite materials are highlighted as an attractive option.

9:55 **A Wide-Load-Range Single-Inductor-Dual-Output Boost Regulator with Minimized Cross-Regulation by Constant-Charge-Auto-Hopping (CCAH) Control**, *Xiaocheng Jing, Philip Mok and Ming Chak Lee, The Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong*

A novel single-inductor-dual-output (SIDO) boost regulator with constant-charge-auto-hopping (CCAH) control to minimize the cross interference between channels is presented. In order to have a predictable system switching noise spectrum, the switching frequency of the converter is automatically hopped between 1.25MHz and 1.25MHz/N where N = 2 to 5 according to the loads and during transient. Load transient measurements show that the cross-regulation is less than 0.1mV/mA with a 200mA change of load current.

10:20 **A Single-Inductor Dual-Output Switching Converter with Low Ripples and Improved Cross Regulation**, *Weiwei Xu, Ye Li, Xiaohan Gong, Zhiliang Hong and Dirk Killat*, Fudan University, Shanghai, China, *Brandenburg University of Technology, Cottbus, Germany*

This paper proposes a novel fly capacitor method for single-inductor dual-output (SIDO) switching converters to reduce the output ripples and spikes. An adaptive common-mode control is presented to suppress the cross regulation problem. The converter can automatically switch between pulse-width modulation (PWM) and pulse-frequency modulation (PFM) control to improve the efficiency. The SIDO converter is specified for one channel 1.2 V/400 mA and the other 1.8 V/200 mA with input voltage ranging from 2.7 V to 5 V. The chip has been fabricated on a 0.25µm CMOS mixed signal process. The conversion efficiency is 82% at a total output power of 840 mW while the output ripples are about 20 mV and spikes less than 40 mV.

10:45 AM **BREAK**

11:05 **An Area- and Power-efficient Monolithic Buck Converter with Fast Transient Response**, *Ying Wu, Sam Tsui and Philip Mok, Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong*

A voltage-mode Buck converter with a novel Pseudo-Type III compensation is presented. It maintains the fast load transient response, as confirmed by the measured loop gain, and 7µs settling time for 500mA load current step. It also transforms the Type III compensator into a summation of an area- and power-efficient error amplifier plus a low-power band-pass filter. Consequently, the area and power consumption of proposed compensator is reduced by 80% and 85%.

11:30 **An Efficiency-Enhanced Auto-Reconfigurable 2x/3x SC Charge Pump for Transcutaneous Power Transmission**, *Xiwen Zhang and Hoi Lee, The University of Texas at Dallas, Richardson, TX*

An auto-reconfigurable 2x/3x switched-capacitor charge pump (SC-CP) for transcutaneous power transmission is presented in this paper. The proposed SC-CP can automatically configure its own voltage conversion ratio by adaptive control circuitry for maintaining high efficiencies of the DC/DC regulator under coupling variations. An adaptive deadtime control is developed to improve the efficiency of the proposed SC-CP by minimizing the shoot-through current. Implemented in a standard 0.35-µm n-well CMOS process, the proposed SC-CP achieves peak power efficiencies of 95% (2x) and 92% (3x). The efficiency of the DC/DC regulator with the proposed SC-CP is improved by >25%, compared to that using the conventional 3x SC-CP, when the input voltage varies from 1.6V to 2.4V.

11:55 **A Novel On-Chip Voltage Generator for Low Voltage DRAMs and PRAMs**, *Tatsuya Matano, Koji Sato, Kiyoshi Nakai and Isamu Asano, Elpida Memory, Inc., Kanagawa, Japan*

A novel on-chip voltage generator suitable for 1V range DRAMs and PRAMs has been developed using a cross charge

pump circuit with a shift charge method, an incidental pumping scheme, and a dual regulator scheme. These effectiveness has been confirmed by the experimental 128Mb PRAM device using 0.072 μ m CMOS process.

Session 11 - Digital Wireline and PLL Techniques

Tuesday Morning, September 15
Pine Ballroom

Chair: Gu-Yeon Wei, Harvard University
Co-Chair: Afshin Momtaz, Broadcom

Digital techniques offer several advantages for PLLs and wireline designs. This session presents designs, models, and analysis of digital-centric solutions.

9:00 **Introduction**

9:05 **Fast Lock Scheme for Phase-Locked Loops**, Amir Bashir, Jing Li, Kiran Ivatury, Naveed Khan, Nirav Gala, Noam Familia*
11-1 and Zulfiqar Mohammed, Intel Corporation, Folsom, CA, *Intel Corporation, Jerusalem, Israel

A fast lock scheme for PLLs is presented, which can enable significant power savings in SOC designs. Multiple Self-Bias PLLs were designed to operate at VCO frequencies from 1.6GHz to 5GHz, and fabricated using 65nm CMOS process. Silicon measurements indicate up to 75% reduction in worst-case PLL lock times.

9:30 **ADC-Based Serial I/O Receivers (INVITED)**, Chih-Kong Yang and E-Hung Chen, University of California, Los Angeles, CA
11-2

Fully digital receiver front ends have garnered interest for serial I/Oreceivers. While the speed and resolution are achievable in CMOS technologies, the challenge is to achieve low power dissipation so that the I/O links can be integrated in large ASICs. This paper describes different design techniques and shows that power can be reduced by constraining the specifications and by making architectural trade-offs.

10:20 **A 2.4-GHz Low-Power All-Digital Phase-Locked Loop**, Liangge Xu, Saska Lindfors, Kari Stadius and Jussi Ryyänen,
11-3 Helsinki University of Technology, TKK, Finland

This paper presents a 2.4-GHz all-digital phase locked loop (ADPLL) frequency synthesizer for wireless applications. The ADPLL is built around a digitally controlled LC oscillator, and it covers the target frequency range with fine frequency resolution. In the feedback path, a high-speed topology is employed for the variable phase accumulator to count full cycles of the RF output. A simple technique based on a short delay line in the reference signal path effectively lowers power consumption of the time-to-digital converter (TDC) and reduces in-band spurs of the output spectrum. Fabricated in a 65-nm CMOS, the ADPLL has an active area of 0.24 mm². Measured output frequency range is from 2.29 to 2.92 GHz. The worst case phase noise at 1-MHz offset over the whole frequency range is -120 dBc/Hz when the PLL consumes 12 mW from a 1.2-V supply, and -112 dBc when power is lowered to 8 mW. The inband spurs are below -61 dBc, and far-off spurs below -57 dBc.

10:45 AM BREAK

11:05 **A Nonlinear Phase Detector for Digital Phase Locked Loops**, Ping-Hsuan Hsieh, Jay Maxey* and Chih-Kong Ken Yang,
11-4 University of California, Los Angeles, CA, *Texas Instruments, Dallas, TX

This paper examines several transfer curves of the phase detector in a digital phase-locked loop and illustrates the benefits of applying non-linearity to the phase transfer characteristics. Taking advantage of the programmability of the digital implementation, the proposed technique shows a better trade-off between the acquisition speed and the steady-state dithering jitter performance.

11:30 **Nonlinear Behavior Study in Digital Bang-Bang PLL**, Albert Vareljian, Mohsen Moussavi, William Bereza, Walter
11-5 Fergusson, Charles Berndt and Rakesh H. Patel, Altera Corp., San Jose, CA

A simple high-performance nonlinear digital PLL is fabricated in 90 nm CMOS with operating range of 0.5 to 3.25 GHz and 1.24 ps jitter. New insights into the PLL behavior are discussed. The classical "20Log" in-band phase noise tracking does not hold for the type of nonlinear digital loops.

11:55 **Analysis of Digital Bang-Bang Clock and Data Recovery for Multi-Gigabit/s Serial Transceivers**, Yehui Sun and Hui
11-6 Wang, Integrated Device Technology, Shanghai, China

A Harmonic Balance method for analyzing digital bang-bang clock and data recovery (CDR) is proposed in this paper. The jitter tolerance performance of the CDR is predicted by a function with variables that can be easily correlated to design parameters. A 6.25Gb/s serial transceiver was fabricated in 90nm CMOS technology. Measurements show that the jitter tolerance performance can be accurately predicted by the proposed method.

Session 12 - Process Integration and Manufacturing Issues

Tuesday Morning, September 15
Cedar Ballroom

Chair: Philippe Jansen, IMEC
Co-Chair: David Sunderland, Boeing Space and Intelligence Systems

Ultra-high frequency applications, functional system integration, and regulatory material constraints drive new approaches for integration of heterogeneous technologies and packaging. This session discusses high-speed BiCMOS, lead-free package reliability, and process integration for high-voltage CMOS and 3D images.

9:00 **Introduction**

9:05 12-1 **Pushing the Speed Limits of SiGe:C HBTs up to 0.5 Terahertz (INVITED)**, *Stefaan Decoutere, Stefaan Van Huylenbroeck, Bernd Heinemann*, Alexander Fox*, Pascal Chevalier**, Alain Chantre**, Thomas Meister^, Klaus Aufinger^ and Michael Schröter#, IMEC, Leuven, Belgium, *IHP, Frankfurt, Germany, **STMicroelectronics, Crolles, France, ^Infineon Technologies, Munich, Germany, #TUD, Dresden, Germany*

The European project DOTFIVE is a 3-year project targeting a 0.5 THz SiGe Heterojunction Bipolar Transistor for the future development of communication, imaging and radar applications. The project explores further evolutionary scaling of self-aligned selective epitaxial base HBTs, and advanced process modules and disruptive novel device architectures.

9:55 12-2 **The Challenge of Lead-Free Electronics for Aerospace Electronic Systems (INVITED)**, *Lloyd Condra, Stephan Meschter*, Dave Pinsky** and Anthony Rafanelli**, Boeing, Seattle, WA *BAE Systems, Johnson City, NY,**Raytheon Integrated Defense Systems, Portsmouth, RI,*

Most commercial electronics manufacturers are delivering lead-free electronic components, assemblies, and equipment to aerospace users, with significant impact on the design, production, and support of aerospace electronic systems. Unique aerospace requirements force the aerospace industry to develop unique responses to the challenges posed by lead-free electronics.

10:45 AM BREAK

11:05 12-3 **High Voltage Devices in Advanced CMOS Technologies (INVITED)**, *Raúl Andrés Bianchi, Christine Raynaud, Floria Blanchet, Frederic Monsieur and Olivier Noblanc, STMicroelectronics, Crolles Cedex, France*

CMOS technologies for mobile systems require integrated high voltage devices, on bulk and thin SOI substrates, for analog baseband and RF power applications. Main challenges for their integration in advanced CMOS are explained. Gate oxide thickness influence on the relevant figures of merit and considerations on performance-reliability tradeoff are provided

11:55 12-4 **Angle Sensitive Pixels in CMOS for Lensless 3D Imaging**, *Albert Wang, Patrick Gill and Alyosha Molnar, Cornell University, Ithaca, NY*

We present a pixel-scale CMOS sensor built in an unmodified 130nm CMOS process, for near-field, lensless imaging. This angle-sensitive pixel uses local diffraction gratings to discriminate the incident angle of incoming light. Arrays of these pixels can reconstruct the 3-dimensional structure of light sources.