Tuesday Morning Program

Session 10 – RF Building Blocks

Tuesday Morning, September 20
Oak Ballroom

Chair: Alberto Valdes-Garcia, IBM TJ Watson Research Center
Co-Chair: Andrea Mazzanti, Universita di Pavia

How to deal with non-linearity? This session presents recent advances in linearization techniques for PAs, a wide-band T/R switch, and exploiting non-linearity for frequency multiplication.

9:00 AM **Introduction**

9:05 AM
10-1 **A Fully Integrated Highly Linear Efficient Power Amplifier in 0.25μm BiCMOS Technology for Wireless Applications,** *H. Hedayati, M. Mobarak, G. Varin*, P. Meunier*, P. Gamand*, E. Sánchez-Sinencio, K. Entesari, Texas A&M University, *NXP Semiconductors*

A highly linear, efficient power amplifier in 0.25μm BiCMOS technology is presented. The linearity is improved by adding an auxiliary amplifier to the main bipolar junction transistor (BJT). The efficiency enhancement is achieved using a switchable biasing and output matching network. The experimental results show a gain of 13 dB and an output PdB of 21 dBm with a 32% PAE. The IM3 and IM5 terms are -41 dBc and -44 dBc at 21 dBm average output power.

9:30 AM
10-2 **A 1.9/2.4GHz Dual Band CMOS Power Amplifier with Integrated AM-PM Distortion Canceller,** *K. Onizuka, H. Isihara, M. Hosoya, S. Saigusa, O. Watanabe, S. Otaka, Toshiba Corporation*

A transformer-based dual band watt-level linear CMOS power amplifier is demonstrated for upcoming SDRs. Proposed AM-PM canceller improves ACLR of WCDMA uplink signal by 2.6dB at 28.0dBm output power. The test chip demonstrates peak output powers of 28.3dBm at 1.95GHz and 23.7dBm at 2.4GHz satisfying WCDMA and IEEE802.11g spectrum masks.

9:55 AM
10-3 **Managing Linearity in Radio Front-Ends (INVITED),** *Ranjit Gharpurey, University of Texas at Austin*

Front-end linearity plays a crucial role in determining the overall performance of a radio receiver. Non-linearity can impact performance in several ways, including degradation in sensitivity, reduction in gain and the appearance of spurious energy within the frequency band of interest from out-of-band sources. In this paper, an overview of techniques for enhancing front-end linearity is presented. Circuit and device-level techniques, as well as architectures for linearization are described.

10:45 AM **BREAK**

11:05 AM
10-4 **A Transformer-Based Broadband I/O Matching-Balun-T/R Switch Front-end Combo Scheme in Standard CMOS,** *Yanjie Wang, Hua Wang, Chris Hull, Shmuel Ravid, Intel Corporation*

A transformer-based broadband front-end combo scheme (I/O matching, balun, and T/R switch) is proposed with high isolation and linearity performance. An implementation example is prototyped in a standard 90nm CMOS process covering a 1dB-bandwidth of 2GHz from 5GHz to 7GHz based on the total insertion loss. In transmitting (TX) mode, the complete front-end combo achieves 2.77dB insertion loss, +45.65dBm IIP3, and -42dB antenna-receiver isolation.

In receiving (RX) mode, the front-end combo demonstrates an insertion loss of 2.62dB and +44.18dBm IIP3 with -42dB transmitter-antenna isolation. The front-end combo occupies a core area of 0.5mm2 including on-chip balun, which is conducive to broadband transceiver SOC integration.

11:30 AM 10-5 **A Low Conversion Loss Passive Frequency Doubler,** *Muhammad Adnan, Ehsan Afshari, Cornell University*

We propose a passive frequency multiplication technique that can achieve low conversion loss even for small input powers. Using this, a 20GHz doubler is designed in a 65nm CMOS process. The doubler is tested from 14GHz-25GHz and achieves conversion loss of 3.5dB with input power of 2.7dBm at 20GHz.

Session 11 – Over-Sampling Converters

Tuesday Morning, September 20
Fir Ballroom

Chair: Ron Kapusta, Analog Devices
Co-Chair: Pavan Hanumolu, Oregon State University

Over-sampling data converters using both discrete- and continuous-time look filters are presented. These converters cover signal bandwidths from 20 KHz up to 28 MHz and achieve excellent figure of merit.

9:00 AM **Introduction**

9:05 AM 11-1 **An 18µW 79dB-DR 20KHz-BW MASH ΔΣ Modulator Utilizing Self-Biased Amplifiers for Biomedical Applications,** *Le Wang, Luke Theogarajan, *University of California Santa Barbara*

This paper presents a micro power, area-efficient 4th-order MASH delta-sigma modulator based on a novel self-biased amplifiers for neural sensing applications. A high-gain self-biased CMOS amplifier is proposed to achieve low power operation. Floating correlated double sampling technique is devised to enhance the amplifer’s gain-linearity and hence the modulator’s SFDR and SNDR performance. Fabricated in a 0.13 µm CMOS process, the prototype achieves 71 dB peak SNDR and 79 dB peak DR over 20 KHz neural signal bandwidth, while occupying only 0.06 mm2 silicon area. By optimizing the power budgets for different amplifiers, the MASH modulator consumes only 18 µW from 1.5 V supply. The proposed circuit techniques can be applied to other operational transconductance amplifier-based circuits for low power, high speed, and area-efficient design.

9:30 AM 11-2 **A 75dB SNDR, 10MHz Conversion Bandwidth Stage-Shared 2-2 MASH ΔΣ Modulator Dissipating 9mW,** *Ramin Zanbaghi, Saurabh Saxena, Gabor C. Temes, and Terri S. Fiez, Oregon State University*

This paper presents a new stage-sharing technique in a discrete-time 2-2 MASH ΔΣ ADC to reduce the modulator power consumption. The proposed technique shares all active blocks of the modulator second stage with its first stage. The 2-2 MASH modulator utilizes second-order Chain of Integrators with Weighted Feed-forward Summation (CIFF) and Cascade of Integrators with Distributed Feedback Branches (CIFB) architectures for the first and second stages, respectively. Using the proposed technique, the second integrator and the adder op-amps of the modulator first stage are shared with the first and second integrator op-amps of the second stage. Measurement results show that the modulator designed in a 0.13um CMOS technology achieves 75-dB SNDR over a 5MHz signal bandwidth with a clock frequency of 130MHz, while dissipating less than 9mW analog power.

9:55 AM 11-3 **A 1-1-1-1 MASH Delta-Sigma Modulator Using Dynamic Comparator-Based OTAs,** *K. Yamamoto, A. Chan Carusone, University of Toronto*

A 1-1-1-1 MASH delta-sigma modulator with dynamic comparator-based OTAs is presented. The proposed OTA asynchronously alternates between input comparison and current pulse injection. The 65-nm LP CMOS prototype achieves a FoM of 276 fJ/conv-step with 70.4 dB SNDR over a 2.5-MHz bandwidth while dissipating 3.73 mW from a 1.2-V supply.

10:20 AM 11-4 **A Double-Sampled Low-Distortion Cascade ΔΣ Modulator with an Adder/Integrator for WLAN Application,** *S. Lee, J. Chae*, M. Aniya**, S. Takeuchi**, K. Hamashita**, P. K. Hanumolu, and G. C. Temes, Oregon State University, *Maxlinear, **Asahi Kasei Microdevices Corporation*

A cascade switched-capacitor ΔΣ analog-to-digital converter, suitable for WLANs, is presented. It uses a double sampling scheme with single set of DAC capacitors, and an improved low-distortion architecture with an embedded-adder integrator. The proposed architecture eliminates one active stage, and reduces the output swings in the loop-filter and hence the non-linearity. It was fabricated with a 0.18um CMOS process. The prototype chip achieves 75.5 dB DR, 74 dB SNR, 73.8 dB SNDR, -88.1 dB THD, and 90.2 dB SFDR over a 10 MHz signal band with an FoM of 0.27 pJ/conv-step.

10:45 AM **BREAK**

11:05 AM 11-5 **A 77dB SNDR, 4MHz MASH ΔΣ Modulator with a Second-Stage Multi-rate VCO-Based Quantizer,** *Samira Zali Asl, Saurabh Saxena, Pavan Kumar Hanumolu, Kartikeya Mayaram, Terri S. Fiez, Oregon State University*

A VCO-based MASH delta-sigma ADC consisting of a first-order switched-capacitor integrator with a 4-bit quantizer operating at 100MHz is followed by a second-stage VCO-based ADC operating at 1.2GHz. In a 130nm CMOS process, the prototype has a measured SNDR of 77dB with 4MHz signal bandwidth. The resulting FoM is 298fJ/conv.

11:30 AM 11-6 **A 16MHz BW 75dB DR CT ΔΣ ADC Compensated for More than One Cycle Excess Loop Delay,** *Vikas Singh, Nagendra Krishnapura, Shanthi Pavan, Baradwaj Vigraham, Nimit Nigania, Debasish Behera, Indian Institute of Technology*

An 800MS/s CT Delta Sigma ADC with 16MHz/32MHz bandwidths consumes 47.6mW from 1.8V and occupies 1mm2 in a 0.18 μm CMOS process. The DR/SNR/SNDR for the two bandwidths are 75/67/65 dB and 64/57/57 dB respectively. Excess loop delay (ELD) of more than one cycle is compensated using a fast path outside the flash ADC. This and a low latency flash ADC and delay free DAC calibration result in the highest reported sampling rate in this process.

11:55 AM 11-7 **A 3.6GS/s, 15mW, 50dB SNDR, 28MHz Bandwidth RF ΣΔ ADC with a FoM of 1pJ/bit in 130nm CMOS,** *A. Ashry, H. Aboushady, LIP6 Laboratory*

A 4th order RF LC Sigma-Delta ADC clocked at 3.6GHz and centered at 900MHz is presented. The simplicity of the ADC architecture results in a significant performance enhancement and power consumption reduction. The ADC, suitable for Software Defined Radio applications, is implemented in a standard 130nm CMOS technology. It achieves a 52dB SFDR and a 50dB SNDR in a 28MHz BW and consumes only 15mW from a 1.2V supply. The Figure of Merit of the ADC is 1.0pJ/bit, which is to date the best reported FoM for an RF ADC. An efficient algorithm for the tuning and calibration of the Sigma-Delta LC-based loop filter is also presented in this paper.

Session 12 – Single Chip Architectures for Sensing and Signal Processing

Tuesday Morning, September 20
Pine Ballroom

Chair: Manoj Sachdev, University of Waterloo
Co-Chair: Ohsang Kwon, Samsung

Architectures for single-chip ICs utilizing neural networks and 2D signal processing for computational and energy challenges. Smart temperature sensing techniques for on-chip power efficiency and reliability.

9:00 AM **Introduction**

9:05 AM
12-1 **A 45nm CMOS Neuromorphic Chip with a Scalable Architecture for Learning in Networks of Spiking Neurons,** *Jae-sun Seo, Bernard Brezzo, Yong Liu, Benjamin D. Parker, Steven K. Esser*, Robert K. Montoye, Bipin Rajendran, José A. Tierno, Leland Chang, Dharmendra S. Modha*, and Daniel J. Friedman, IBM T. J. Watson Research Center, *IBM Research - Almaden*

We present a scalable integrated circuit platform for networks of spiking neurons. Through tight integration of memory (synapses) and computation (neurons), a 45nm reconfigurable chip comprising 256 neurons and 64K binary synapses with on-chip learning is demonstrated. Near-threshold, event-driven operation at 0.53V maximizes power efficiency for real-time pattern classification tasks.

9:30 AM
12-2 **A Digital Neurosynaptic Core Using Embedded Crossbar Memory with 45pJ per Spike in 45nm,** *Paul Merolla, John Arthur, Filipp Akopyan, Nabil Imam*, Rajit Manohar*, Dharmendra Modha, IBM Research - Almaden, *Cornell University*

We fabricated a key building block of a modular neuromorphic architecture, a neurosynaptic core, with 256 digital integrate-and-fire neurons and a 1024 by 256 bit SRAM crossbar memory for synapses using IBM's 45-nm SOI process. Our fully digital implementation is able to leverage favorable CMOS scaling trends, while ensuring one-to-one correspondence between hardware and software. The core is fully configurable in terms of neuron parameters, axon types, and synapse states and is thus amenable to a wide range of applications.

9:55 AM
12-3 **Smart Integrated Temperature Sensor - Mixed-Signal Circuits and Systems in 32-nm and Beyond (INVITED),** *Y. William Li, H. Lakdawala, Intel Corporation*

Integrating smart temperature sensors into digital platforms facilitates information to be processed and transmitted, and open up new applications. Furthermore, temperature sensors are crucial components in computing platforms to manage power-efficiency trade-offs reliably under a thermal budget. This paper presents a holistic perspective about smart temperature sensor design from system- to device-level including manufacturing concerns. Through smart sensor design evolutions, we identify some scaling paths and circuit techniques to surmount analog/mixed-signal design challenges in 32-nm and beyond. We close with opportunities to design smarter temperature sensors.

10:45 AM **BREAK**

11:05 AM
12-4 **ReSSP: A 5.877 TOPS/W Reconfigurable Smart-Camera Stream Processor,** *Wei-Kai Chan, Yu-Hsiang Tseng, Pei-Kuei Tsung, Tzu-Der Chuang, Yi-Min Tsai, Wei-Yin Chen, Liang-Gee Chen, Shao-Yi Chien, National Taiwan University*

A 5.877 TOPS/W Reconfigurable Smart-camera Stream Processor is implemented in 90nm

CMOS technology. A re-configurable hardware architecture with heterogeneous stream processing and subword-level parallelism is implemented to accelerate the vision processing for smart-camera applications. The area efficiency reaches 111.329 GOPS/mm2. The power efficiency and area efficiency are 4.5x to 33.0x and 3.8x to 74.2x better than the state-of-the-art works, respectively.

11:30 AM 12-5 **3.6-GHz 0.2-mW/ch/GHz 65-nm Cross-Correlator for Synthetic Aperture Radiometry,** *E. Ryman, A. Emrich, S. Andersson, J. Riesbeck, L. Svensson*, P. Larsson-Edefors*, Omnisys Instruments AB, *Chalmers University of Technology*

A high-speed low-power cross-correlator ASIC has been implemented in a 65-nm CMOS process for the purpose of synthetic aperture radiometry from geostationary orbiting earth observation satellites. Experimental evaluation demonstrates that the chip has a top performance of 3.6 GHz at which it dissipates 790 mW.

Session 13 (Forum 2) – Evolution of Clocks

Tuesday Morning, September 20
Cedar Room

Chair: Steven L. Garverick, Case Western Reserve University

9:05 am 13-1 **Understanding the Antikythera Mechanism,** *Tom Malzbender, HP Labs*

In 1900, a party of sponge divers chanced on the wreck of a Roman merchant vessel between Crete and mainland Greece. It was found to contain numerous ancient Greek treasures, among them a mysterious lump of clay that split open to reveal ‘mathematical gears’ as it dried out. Constructed in roughly 150 B.C.E., this object is now known as the Antikythera Mechanism, one of the most enlightening artifacts in terms of revealing the advanced nature of ancient Greek science and technology. In 2005 we travelled to the National Archeological Museum in Athens to apply our Reflectance Imaging methods to the mechanism in the hopes of revealing ancient writing on the device. We were successful, and along with the results of Microfocus CT imaging, we are able to decipher 3000 characters compared with the original 800 known. This lead to an understanding that the device was a mechanical, astronomical computer capable of predicting solar and lunar eclipses along with other celestial events. This talk will overview both the imaging methods as well as what they reveal about the Antikythera Mechanism.

9:55 am 13 -2 **Timing Inaccuracy of Clocks,** *Ali Hajimiri, California Institute of Technology*

Since the beginning of time, timing accuracy has been strived for by clock designers. Although everyone has an intuitive sense of what clock accuracy and stability means, there is often an implicit comparison to some sort of assumed reference. In this talk, we will discuss the general notion of oscillator instability and evaluate the oscillator short term instability using a time-variant model which explains the evolution of the physical noise into phase noise in an oscillator. We will examine some of the design implications of such the noise evolution in the oscillator design via some practical examples.

10:40 13 -3 **Frequency Reference Challenges - A Systemic View**, *Harmeet Bhugra, Integrated Device Technology, Inc.*

The performance of conventional quartz oscillators is being tested to the limit. We will introduce basics behind quartz and then go over known technical challenges including activity dips, aging, vibration sensitivity etc. that are encountered using quartz oscillators. We will cover new technologies on the horizon specifically MEMS based technologies that continue to solve issues faced by crystal oscillators.

11:30 **Micromechanical Oscillators**, *Mourad El-Gamal, McGill University*
13 -4