

**Technical Sessions**  
**Tuesday, September 21 - Morning**

**Session 10 – Oversampled Data Converters**

Tuesday Morning, September 21  
Oak Ballroom

Chair: Don Thelen, ON Semiconductor  
Co-Chair: Alessandro Piovaccari, Silicon Laboratories

Delta sigma ADCs continue to improve and are being used in more applications each year. This session includes many novel examples.

9:00           **Introduction**

9:05           **A 32-Channel Front-End for Wireless HID using Inverse-STF Pre-Filtering Technique,**  
10-1           *Sherif Galal, Jurgen van Engelen\*, Jared Welz, Henrik Jensen, Khaled Abdelfattah, Felix Cheung, Sasi Kumar Arunachalam, Xicheng Jiang, Todd Brooks, Broadcom Corp., \*Mobius Semiconductor*

A 32-channel front-end circuit for wireless human interface devices (HID) is described. The front-end incorporates a Sigma-Delta ADC combined with an inverse-STF pre-filtering technique to achieve 10.8 ENOB at a conversion rate of 7.5us per channel. Chopping and digital calibration are employed to achieve an offset voltage < 850uV and gain error < 0.17%. The HID front-end measures single-ended rail-to-rail inputs with 1.62V to 3.63V supply range, occupies 0.28mm<sup>2</sup> in 65nm CMOS and consumes 1.8mW from 1.2V supply.

9:30           **82 dB SNDR 20-Channel Incremental ADC with Optimal Decimation Filter and Digital**  
10-2           **Correction, Wenhuan Yu, Mehmet Aslan\*, Gabor Temes, Oregon State University, \*National Semiconductor Corporation**

A third-order multi-channel incremental ADC with a 5-level quantizer is presented. An optimal decimation filter is used which minimizes the weighted sum of the thermal and quantization output noises. Digital correction is used to suppress mismatches in the multi-bit DAC.

9:55           **A +5dBFS Third-Order Extended Dynamic Range Single-Loop  $\Delta\Sigma$  Modulator, Nima**  
10-3           **Maghari, Skyler Weaver, Un-Ku Moon, Oregon State University**

A new single-loop delta-sigma modulator with extended dynamic range is proposed. It employs an auxiliary multi-bit quantizer which processes the quantization error of the main quantizer. This addition guarantees improved stability over a wider input signal range. The cancelation of the quantization noise of the main quantizer is done via in-loop digital summation and is immune to opamp DC gain. As a proof of concept, a 3rd order modulator is designed in a 0.18 $\mu$ m CMOS process. This implementation incorporates a 3-level main quantizer, a 9-level auxiliary quantizer and 30dB open-loop opamp gain. Measurement results show that at 1.2V power supply and reference, the input signal can go over +5dBFS without any stability issues, achieving 75dB SNDR and 77.2dB dynamic range at OSR of 16. The clock frequency is 40MHz and the power dissipation is 4.9mW.

10:20           **A 63 dB 16 mW 20 MHz BW Double-Sampled  $\Delta\Sigma$  Analog-to-Digital Converter with an**  
10-4           **Embedded-Adder Quantizer, Jeongseok Chae, Sanghyeon Lee, M. Aniya\*, S. Takeuchi\*, K. Hamashita\*, Pavan Hanumolu, Gabor Temes, Oregon State University, \*Asahi Kasei Microdevices**

A wideband  $\Delta\Sigma$  ADC using a novel double-sampling scheme with a single set of capacitors and a dynamic embedded-adder quantizer is presented. The proposed quantizer eliminates static currents in the adder of a low-distortion architecture. Fabricated in 0.18  $\mu\text{m}$  CMOS process, the prototype chip operates with a 320 MHz sampling frequency and achieves 63 dB SNDR in a 20 MHz signal band while consuming 16 mW power.

**10:45 BREAK**

11:05 **A 69.8 dB SNDR 3<sup>rd</sup>-order Continuous Time Delta-Sigma Modulator with an Ultimate Low Power Tuning System for a Worldwide Digital TV-Receiver**, Kazuo Matsukawa, Yosuke Mitani, Masao Takayama, Koji Obata, Yusuke Tokunaga, Shiro Sakiyama, Shiro Doshio, Panasonic Corporation  
10-5

This paper presents a 3rd-order continuous time delta-sigma modulator for a worldwide digital TV-receiver whose SNDR is 69.8 dB. An ultimate low power tuning system using RC-relaxation oscillator is developed in order to achieve high yield against PVT variations. A 3rd-order modulator with modified single opamp resonator contributes to cost reduction by realizing very compact circuit. The mechanism to occur 2nd-order harmonic distortion at current feedback DAC was analyzed and a reduction scheme of the distortion enabled the modulator to achieved FOM of 0.18 pJ/conv-step.

11:30 **A Robust STF 6mW CT  $\Delta\Sigma$  Modulator with 76dB Dynamic Range and 5MHz Bandwidth**, Mohammad Ranjbar, Omid Oliaei, Robert Jackson, University of Massachusetts Amherst  
10-6

A third-order continuous-time delta-sigma modulator achieving 76dB dynamic range over 5MHz signal bandwidth is presented. The modulator has a monotonic lowpass signal transfer function and achieves over 70dB anti-aliasing. The prototype chip implemented in a 130nm CMOS process consumes 6mw power from a single 1.2V supply and occupies 0.56 mm<sup>2</sup> active area.

11:55 **A 5-MHz 11-bit Delay-Based Self-Oscillating  $\Sigma\Delta$  Modulator in 0.025mm<sup>2</sup>**, Bart De Vuyst, Pieter Rombouts, Ghent University  
10-7

In this paper a self-oscillating sigma-delta modulator is presented. The self-oscillation is induced here by introducing a controlled delay in the feedback loop of the modulator. A second order CMOS prototype was constructed in a 0.18  $\mu\text{m}$  technology. The modulator achieves a dynamic range (DR) of 66 dB for a signal bandwidth of 5 MHz. The power consumption is 6 mW and the chip area of is 0.025 mm<sup>2</sup>.

## Session 11 – Power Management

Tuesday Morning, September 21  
Fir Ballroom

Chair: Cory Arnold, Maxim Integrated Products  
Co-Chair: Hoi Lee

Effective power management requires innovative circuits to optimize system cost and efficiency. This session includes advancements in switching regulators, linear regulators, and smart power drivers.

9:00 **Introduction**

9:05 **Ramp Signal Generation in Voltage Mode CCM Random Switching Frequency Buck Converter for Conductive EMI Reduction**, Edward N. Y. Ho, Philip K. T. Mok, Hong Kong University of Science and Technology  
11-1

An output voltage ripple aware design of different voltage ramp signal of voltage mode CCM random frequency buck converter for conductive EMI reduction has been presented in this paper. Simulation and experimental results with a standard CMOS-0.35 $\mu$ m process verifies the proposed design and analysis. From experimental result, a carefully designed ramp can reduce output voltage ripple by more than 8 times with no influence on the inductor current spectrum spread and without any increment of inductance and capacitance comparing to conventional design.

9:30  
11-2 **A 5-MHz 91% Peak-Power-Efficiency Buck Regulator With Auto-Selectable Peak- and Valley-Current Control**, Mengmeng Du, Hoi Lee, University of Texas at Dallas

This paper presents a multi-MHz buck regulator for portable applications using an auto-selectable peak- and valley-current control (ASPVCC) scheme. The proposed ASPVCC scheme and the dynamically-biased shunt feedback in the current sensors relax the settling-time requirement of the current sensing and improve the sensing speed. The proposed converter can thus operate at high switching frequencies with a wide range of duty ratios for reducing the required inductance. Implemented in a 0.35- $\mu$ m CMOS process, the proposed buck converter can operate at 5-MHz with a duty-ratio range of 0.6, use a small-value off-chip inductor of 1  $\mu$ H, and achieve 91% peak power efficiency.

9:55  
11-3 **Fully Integrated On-Chip DC-DC Converter with a 450x Output Range**, Sudhir Kudva, Ramesh Harjani, University of Minnesota

This paper presents a technique to efficiently supply power over a wide power range using a fully integrated on-chip converter for dynamic voltage scaling (DVS) based applications. All components, including filter elements, are integrated onchip. To achieve high efficiency the converter adaptively switches between different modes of operation by detecting the output current. The design, implemented in the IBM 130nm CMOS technology achieves a peak efficiency of 74.5% and can operate over a 450X power range (0.6mW to 266mW). This represents the best reported power range for a high-efficiency fully integrated on-chip power converter.

10:20  
11-4 **A 140mA 90nm CMOS Low Drop-out Regulator with -56dB Power Supply Rejection at 10MHz**, Ahmed Amer, Edgar Sánchez-Sinencio, Texas A&M University

A high power supply rejection (PSR) low drop-out (LDO) voltage regulator employing a supply ripple cancellation adaptive technique is presented. The LDO is implemented in 90nm CMOS process and occupies an active area of 0.015mm<sup>2</sup>. Measured PSR is better than -50dB up to 10MHz across the load current range of 140mA with a drop-out voltage of 0.15V and a current efficiency of 99.9%. Load regulation of 6mV for a 140mA current step is measured.

10:45 **BREAK**

11:05  
11-5 **0.5-V Input Digital LDO with 98.7% Current Efficiency and 2.7- $\mu$ A Quiescent Current in 65nm CMOS**, Yasuyuki Okuma, Koichi Ishida\*, Yoshikatsu Ryu, Xin Zhang\*, Po-Hung Chen\*, Kazunori Watanabe, Makoto Takamiya\*, Takayasu Sakurai\*, Semiconductor Technology Academic Research Center, \*The University of Tokyo

A digital LDO is proposed to provide the low noise and tunable power supply voltage to the 0.5-V near-threshold logic circuits. Because the conventional LDO feedback-controlled by the operational amplifier fail to operate at 0.5V, the digital LDO eliminates all analog circuits and is controlled by digital circuits, which enables the 0.5-V operation. The developed digital LDO in 65nm CMOS achieved the 0.5-V input voltage and 0.45-V output voltage with 98.7% current efficiency and 2.7- $\mu$ A quiescent current at 200- $\mu$ A load current. Both the input voltage and the quiescent current are the lowest values in the published LDO's, which indicates the good energy efficiency of the digital LDO at 0.5-V operation.

11:30 **Smart Universal Control IC for High Loaded Factor Resonant Converters**, *Yujia Yang, Fabio E. Bisogno, Sadachai Nittayarumphong, Matthias Radecker, Marc Fahlenkamp\*, Wolf-Joachim Fischer\*\*, Fraunhofer IZM, \*Infineon Technologies AG, \*\*TU Dresden*

This paper presents an adaptive universal control IC with error protection functions for high loaded factor ( $Q > 5$ ) resonant converters. It has a wide frequency tuning range from 25 to 500 kHz. Duty cycle (Dc) tracking and synchronization (SY) are included to ensure zero voltage switching (ZVS). Automatic burst mode (BM) recognition is implemented by external resistive adjustment. The IC has been fabricated with Infineon 0.6  $\mu\text{m}$  B6CA BiCMOS technology.

## Session 12 – Low Phase Noise VCOS and ADPLL Building Blocks

Tuesday Morning, September 21  
Pine Ballroom

Chair: Julian Tham, Arda Technologies  
Co-Chair: Foster Dai, Auburn University

This session focuses on design techniques for GHz range low phase noise voltage-controlled oscillators and building blocks for all digital phase-locked loops.

9:00 **Introduction**

9:05 **A 4-Port-Inductor-Based VCO Coupling Method for Phase Noise Reduction**, *Zhiming Deng, Ali Niknejad, University of California, Berkeley*

A 4-port-inductor-based VCO coupling technique is introduced to improve VCO phase noise performance. Complete design steps including resonant network design and circuit topology selection are discussed and prototype designs have been demonstrated to verify the analysis. The proposed 12.8 GHz CCVCO design achieves phase noise of -116 dBc/Hz at 1 MHz offset, a tuning range of 31.4%, FOM and FOMT of 184 and 194 respectively.

9:30 **A 10 GHz Low Phase Noise VCO Employing Current Reuse and Capacitive Power Combining**, *Diptendu Ghosh, Stewart Taylor\*, Yulin Tan\*, Ranjit Gharpurey, University of Texas at Austin, \*Intel Corporation*

A VCO employing capacitive power combining to reduce phase noise is presented. A current reuse technique is utilized to improve the phase noise per unit power metric over conventional LC oscillators. The VCO achieves a phase noise of -148.7 dBc/Hz at 20 MHz offset and a tuning range of 9.15-10.6 GHz while dissipating 30 mW from a 1.3 V supply. Implemented in a 45 nm CMOS technology, it achieves an FOM of 188 dBc/Hz while occupying an area of 0.67  $\text{mm}^2$ .

9:55 **A 475 mV, 4.9 GHz Enhanced Swing Differential Colpitts VCO in 130 nm CMOS with an FoM of 196.2 dBc/Hz**, *Farhad Farhabakhshian, Thomas Brown\*, Kartikeya Mayaram\*, Terri Fiez\*, Maxim Integrated Products, \*Oregon State University*

An enhanced swing differential Colpitts VCO operates as low as 400 mV and enables oscillations to go beyond both the supply voltage and ground. Operating at 475 mV, the 4.9 GHz VCO consumes 2.7 mW. The 130 nm CMOS VCO's measured phase noise is -136.2 dBc/Hz at a 3 MHz offset frequency. The resulting FoM of 196.2 dBc/Hz makes it the highest performing integrated LC oscillator published to date.

10:20 **1.5-GHz CMOS Voltage-Controlled Oscillator Based On Thickness-Field-Excited**  
12-4 **Piezoelectric AlN Contour-Mode MEMS Resonators**, *Chengjie Zuo, Jan Van der Spiegel, Gianluca Piazza, University of Pennsylvania*

This paper reports on the first demonstration of a 1.5 GHz CMOS VCO based on TFE piezoelectric AlN contour-mode MEMS resonators. The measured phase noise is  $-85$  dBc/Hz at 10 kHz offset frequency and  $-151$  dBc/Hz at 1 MHz offset. This is the highest frequency MEMS oscillator ever reported using a laterally vibrating mechanical resonator. A tunable-supply oscillator design is proposed to enable this novel GHz VCO without using any low-Q tunable component.

**10:45 BREAK**

11:05 **A 1.56GHz Wide-Tuning All Digital FBAR-Based PLL in 0.13 $\mu$ m CMOS**, *Julie Hu, Richard*  
12-5 *Ruby\*, Brian Otis, University of Washington, \*Avago Technologies*

This paper presents the design rationale and measured results of a low power, low jitter, PVT-stable FBAR-based RF synthesizer implemented in 0.13 $\mu$ m CMOS. A digitally controlled FBAR oscillator, tuned with a switched-capacitor array, provides 5800ppm of frequency tuning, sufficient to cover a wide range of manufacturing and temperature variations of an FBAR. An all-digital phase-locked loop (ADPLL) is used to stabilize the FBAR DCO. In the ADPLL architecture, we introduce a twostage time-to-digital converter (TDC) to detect phase differences between reference and divider clocks. The solution offers a fine TDC resolution without large and power-hungry TDC circuitry typically used to address in-band phase noise requirements. With the tuning range, the power consumption of 2.8 mW, and an integrated RMS jitter of 0.38ps from 10kHz to 20MHz, the FBAR ADPLL provides a PVT-stable, high quality RF frequency reference for a range of low power, high data rate applications.

11:30 **Spurious Free Time-to-Digital Conversion in an ADPLL using Short Dithering**  
12-6 **Sequences**, *Khurram Waheed, Mahbuba Sheba, Robert Bogdan Staszewski\*, Fikret Dulger, Socrates Vamvakos, Texas Instruments Inc., \*Technische Universiteit Delft*

This paper proposes an enhancement of the digital phase detection mechanism in an all-digital phase locked loop (ADPLL) operable at multi-GHz by randomization of the reference frequency phase by carefully chosen dither sequences. This renders the digital phase detector in the ADPLL free from any phase domain spurious tones as a consequence of ill-conditioned sampling of variable oscillator phase in the time-to-digital converter (TDC). TDC has a typical time quantization in the range of 5 to 30 ps using modern deep sub-micron technologies. This finite dead-band can result in spurious tones, whenever an "integer" relationship arises between the oscillator phase and the TDC sampling process. This anomaly can be resolved using carefully selected spectrum-friendly dithering mechanisms. This work proposes injection of a short sequence dither signal into the reference signal to overcome the quantization introduced limit-cycles. This results in a robust phase tracking and spurious free operation of the ADPLL.

11:55 **A 3-Dimensional Vernier Ring Time-to-Digital Converter in 0.13 $\mu$ m CMOS**, *Jianjun Yu, Fa*  
12-7 *Foster Dai, Auburn University*

A 3-dimensional Vernier ring time-to-digital converter (TDC) is presented for the first time that greatly improves the measurement time and power consumption and achieves large detectable range and fine resolution simultaneously. The TDC prototype chip achieves 16.5-ps resolution and an 8-bit detectable range with 0.16 mm<sup>2</sup> die area in a 0.13 $\mu$ m CMOS technology. The power consumption for the entire TDC is only 4.5mW with 1.5V power supply at 15MSps sample rate.

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## Session 13 - Forum 2 Biomedical and Bio-inspired Systems

Tuesday Morning, September 21  
Cedar Ballroom

Chair: Ed Lee, Alfred Mann Foundation

9:00 am     **Architecting Therapeutic Interface Circuits and Algorithms for the Nervous System**, *Tim Denison, Medtronic*  
13-1

This talk discusses prototyping sensor, algorithm and actuation technology for interfacing to the nervous system, with a particular focus on creating research tools for exploring treatments for chronic disease. While advances in technology might potentially help improve devices treating neurological conditions, designing a complete system is a complex engineering problem drawing on such diverse fields as applied physics, circuit design, algorithms/classifiers and biology. Fundamental to the design problem is a consideration of the physiology and anatomy of the neural circuits, which helps guide the designer on choosing the most appropriate interface strategy for a given application. Since many of the core operating principles of the nervous system are still being discovered, flexibility and addressing technology validation must also be considered. To put these concepts in context, we will provide an overview of recent work in academics and industry prototyping bi-directional brain-machine interfaces and closed loop systems for preclinical research. These systems seek to provide adaptive neuromodulation of a neural circuit based on detected biomarkers in the nervous system. The applications will highlight how advancements in merging silicon and biological systems might help someday advance the treatment of a variety of neurological disorders.

10:00 am   **Opportunities for RF integrated circuits in bio-molecular diagnostics**, *Ali Hajimiri, California Institute of Technology*  
13-2

Silicon integrated circuits have seen a tremendous growth in the last half century. Today, we are at a point where we can integrate an unlimited (practically) number of transistors on a chip with remarkably high yields. We have also spent the last two decades understanding the fundamentals of high-performance RF and mm-wave system integration in silicon, which has led to the tremendous growth in portable RF systems. There is tremendous opportunity in combining these techniques in biological and bio-medical applications and combining them with new developments from the field of molecular machines to create truly novel and practical molecular detection and sensing systems. We will discuss some examples in the field of molecular diagnostics and discuss how silicon integration can enable truly handheld molecular diagnostics devices, where the low cost does not have to come at the price of low performance.

11:00       **Integrated Circuits for Bio-inspired and Biomedical Systems**, *Rahul Sarpeshkar, Massachusetts Institute of Technology*  
13-3

Nature is a great analog and digital circuit designer. She has innovated circuits in the biochemical, biomechanical, and bioelectronic domains that operate very robustly with highly imprecise parts and with incredibly low levels of power. I will discuss how analog and bio-inspired circuits and architectures have led to and are leading to novel architectures in sensing and computing, e.g., in ear-inspired radios, architectures for improving operation in noise, neuron-inspired signal-to-symbol conversion, and hybrid analog-digital architectures that are inspired by computations within cells. Such techniques can lead to highly energy-efficient parallel architectures that operate rapidly and precisely and solve computationally intensive tasks. I will provide examples from systems built in my lab for bionic ear processors for the deaf, brain-machine interfaces for the blind and paralyzed, body sensor networks for cardiac

monitoring, and in circuits for systems and synthetic biology.