

Poster Session

Monday Evening, September 14
Cascade/Sierra Ballroom
5:00 pm – 7:00 pm

- M-1 **Trimless Second Order Curvature Compensated Bandgap Reference using Diffusion Resistor**, *Ajay Kumar, Texas Instruments*
- A trim-less second order curvature compensated bandgap reference current using diffusion resistor is presented. An order of magnitude higher sheet-resistance (x50) and tighter process control of diffusion resistor than the poly has enabled this work to achieve the same current in one-third area. The process spread of diffusion resistor and V_{PNP} transistor tracks each other, thereby resulting in higher accuracy without using any trim techniques. The proposed circuit is fabricated in a 0.5 μ m CMOS process. The measured reference current has a variation of 46ppm/oC over a temperature range of -55oC to 125oC.
- M-2 **A 10mW 9.7ENOB 80MSPS Pipeline ADC in 65nm CMOS Process without any Special Mask Requirement and with Single 1.3V Supply**, *Abhijit Kumar Das, Hemant Bhasin, Sundara Siva Rao Giduturi, Texas Instruments, India*
- This paper describes a power and area efficient pipeline ADC design. This ADC was designed in 65nm process without any special mask requirement and can work with supply voltage of 1.3V consuming 10mW providing 9.7 ENOB at 80MSPS while occupying less than 0.2 square millimeters.
- M-3 **A 1.5mW 16b ADC with Improved Segmentation and Centroiding Algorithms and Litho-Friendly Physical Design (LFD) Used in Space Telescope Imaging Applications**, *L. Lewyn, M. Loose* SnowBush-Gennum, *Teledyne Imaging Sensors*
- This paper describes the 16b ADC ASIC replacing the survey camera image processor in the 2009 Hubble rescue mission. The ADC uses a combination of improved MSB-LSB segmentation, 3 centroiding algorithms and litho-friendly physical design (LFD) to achieve <0.4b DNL and <2.3b INL without requiring initial or background calibration.
- M-4 **An 11mW 100MHz 16X-OSR 64dB-SNDR Hybrid CT/DT $\Delta\Sigma$ ADC with Relaxed DEM Timing**, *S. Kwon*, P. Hanumolu, S. Kim**, S. Lee**, S. You**, H. Park**, J. Kim**, and U. Moon, Oregon State University, *Now with Dongbu HiTek, **Samsung Electronics*
- A multi-bit 3rd-order hybrid Delta-Sigma ADC is presented. The ADC obviates the need for a dynamic element matching technique (DEM) in the critical feedback path. Eliminating the DEM allows to minimize feedback latency, thus helping to increase clock frequency. The first two continuous-time integrators decrease power consumption and the last discrete-time integrator mitigates the excess loop delay and the quantizer sampling timing problem. Moreover, switched-R-MOSFET-C technique offers benefit of absorbing the finite opamp delay as well as frequency scalability. The proposed ADC is also capable of converting up to +2 dBFS without pole optimization technique. A prototype IC implemented in a 65 nm digital CMOS achieves 68 dB DR, 65 dB SNR, 64 dB SNDR, and 84 dB SFDR while consuming 11 mW and clocking at 100 MHz.
- M-5 **A 14.6th-order 3.456GHz Transmit Baseband filter in 110nm CMOS for Millimeter-Wave Communication Systems**, *M. Tokumar, H. Ikoma, Y. Yamada, K. Okamoto, A. Yamamoto, Y. Shirakawa, Panasonic Corporation*
- This paper presents a 1.728Gbps transmit baseband filter for transmitters of millimeter-wave communication systems. In order to avoid the inter symbol interference, wide band and high order filter is demanded. The proposed filter consists of a 3.456GHz digital filter and an 8-bit 3.456Gbps digital to analog converter (DAC) with a clock divider, which occupies 0.265mm² in 110nm CMOS. The filter consumes 142mW and achieves the transmit spectrum very close to the mask regulated by IEEE802.15.3c.
- M-6 **64-bit Prefix Adders: Power-Efficient Topologies and Design Solutions**, *Ching Zhou, Bruce M. Fleischer, Michael Gschwind, Ruchir Puri, IBM T.J. Watson Research Center*
- 64-bit adders of various prefix algorithms are designed using a novel data flow synthesis methodology. The power-performance tradeoffs are analyzed for a portfolio of popular adder topologies and design styles. The intrinsically sparser designs in hierarchical prefix scheme are demonstrated to be preferable choices for both high-performance and low-power adder applications.
- M-7 **Energy-Performance Tunable Logic**, *Bita Nezamfar, Mark Horowitz, Stanford University*
- An externally static, internally dynamic topology creates a new logic family that enables the user to tune effective transistor thresholds post-fabrication by adjusting a few power supplies. These gates can therefore be programmed for higher speed or for lower power based on the system requirements. An application of this logic to programmable interconnect circuits is shown in this paper. In a 90-nm test chip, the circuit achieves the same performance as conventional static circuits at 65% energy and has a 2X wider energy-performance tuning range. This property enables building in-field energy-performance tunable FPGAs.
- M-8 **A 6-bit Arbitrary Digital Noise Emulator in 65nm CMOS Technology**, *Tetsuro Matsuno*, Daisuke Fujimoto*, Daisuke Kosaka**, Naoyuki Hamanishi***, Ken Tanabe***, Masazumi Shiochi***, Makoto Nagata* **, *Kobe University, **A-R-Tec Corporation, ***Toshiba Corporation*
- An arbitrary noise generator (ANG) is based on time-series charging of divided parasitic capacitance (TSDPC) and emulates

power supply noise generation in a CMOS digital circuit. A prototype ANG incorporates an array of 32×32 6-bit TSDPC cells along with a 128-word vector memory and occupies $2 \times 2 \text{ mm}^2$ in a 65 nm 1.2 V CMOS technology. Digital noise emulation of functional logic cores such as register arrays and processing elements is demonstrated with chip-level waveform monitoring at power supply, ground, as well as substrate nodes.

- M-9 **A 0.92mm² 23.4mW Fully-Compliant CTC Decoder for WiMAX 802.16e Application**, Shao-Wei Yen, Ming-Chih Hu, Chih-Lung Chen, Hsie-Chia Chang, Shyh-Jye Jou, Chen-Yi Lee, National Chiao Tung University
An area-efficient and fully-compliant decoder for convolutional turbo code (CTC) of WiMAX 802.16e is presented. The proposed decoder can support all 17 modes specified in IEEE 802.16e system. By scaling the extrinsic information, the Max-Log MAP algorithm is used to reduce the hardware complexity with the minimized performance loss. A two-phase extrinsic memory and reversed sliding window technique are demonstrated for less memory requirement and decoding latency. Moreover, a division-free reconfigurable interleaver architecture is proposed to use simple addition and subtraction instead of division. Fabricated with the 90nm cmos process, the proposed CTC decoder chip which occupies core area of 0.92mm² can achieve 30Mb/s with 23.4mW power consumption.
- M-10 **Embedded High-Speed BCH Decoder for New-Generation NOR Flash Memories**, Xueqiang Wang, Dong Wu, Chaohong Hu*, Liyang Pan, Runde Zhou, Tsinghua University, *Intel Technology Development Co. Ltd
A high-speed double-error-correcting (DEC) BCH decoder for new-generation NOR flash memory is presented to improve reliability. To speed up the decoding process, a multiplication-free linear transform is developed to eliminate iterations and divisions in Galois fields. Furthermore, the reverse data-flow analysis (RDFA) and smoothest descent approach are proposed to reduce latency in the parallel Chien search. Based on peripheral 180nm CMOS process, the whole BCH decoder is designed and the latency is significantly reduced to less than 5ns.
- M-11 **A 56M Ω CMOS TIA for MEMS Applications**, J. Salvia, P. Lajevardi, M. Hekmat, B. Murmann, Stanford University
We present a high-gain, low-noise differential transimpedance amplifier designed to interface with electrostatic micromechanical resonators. The capacitive feedback topology achieves a 56M Ω gain, 1.8MHz bandwidth, phase response near 0 degrees, and 65 fA/rootHz input-referred noise. It was fabricated in 0.18 μ m CMOS technology and dissipates 436 μ W from a 1.8V supply.
- M-12 **A 366kS/s 400uW 0.0013mm² Frequency-to-Digital Converter Based CMOS Temperature Sensor Utilizing Multiphase Clock**, Kisoo Kim, Hokyu Lee, Sangdon Jung, Chulwoo Kim, Korea University, Seoul, Korea
The proposed temperature sensor is based on CMOS ring oscillators and a frequency-to-digital converter capable of simple and efficient temperature conversion to digital value. The proposed temperature sensor consumes 400 μ W at a conversion rate of 366kS/s and performs the fastest temperature-to-digital conversion among those introduced in previous work. The whole block occupies 0.0066 mm² (0.0013 mm² for temperature sensor). Four multiphase clocks were utilized to enhance the resolution of the sensor 8 times better. After one point calibration, the chip-to-chip measurement spread was +2.748 $^{\circ}$ C ~ -2.899 $^{\circ}$ C over the temperature range of -40 $^{\circ}$ C to 110 $^{\circ}$ C.
- M-13 **Design-for-Manufacturing Features in Nanometer Logic Processes – A Reverse Engineering Perspective**, Dick James, Chipworks Inc.
Recently we have seen the introduction of production disciplines known collectively as Design for Manufacturability (DFM), which are techniques used to co-optimize design, layout, and processing to reduce variability and improve manufacturing parameters. This paper illustrates some different layout features used for DFM in some recent 65-, and 45-nm products.
- M-14 **Quadratic Differential and Integration Technique in V² Control Buck Converter with Small ESR Capacitor**, Shih-Jung Wang, Yu-Huei Lee, Yung-Chih Lai, Ke-Hong Chen, National Chiao Tung University, Hsinchu, Taiwan
This paper proposes a quadratic differential and integration (QDI) technique for the design of buck converters with small equivalent series resistance (ESR) of the output capacitor. The QDI circuit not only further removes the dependence of ESR in the V² control but also achieves a fast transient response with small load transient voltage variation. The experimental results show the output voltage can have voltage ripple about 30 mV and recovery time of 20 μ s in case of 300 mA load current variation.
- M-15 **Adaptive Performance Compensation with In-Situ Timing Error Prediction for Subthreshold Circuits**, H. Fuketa, M. Hashimoto, Y. Mitsuyama, T. Onoye, Osaka University
This paper presents an adaptive technique for compensating manufacturing and environmental variability in subthreshold circuits using "canary Flip-Flop" that can predict timing errors. A 32-bit Kogge-Stone adder whose performance was controlled by body-biasing was fabricated in a 65 nm CMOS process. Measurement results show that the adaptive control can compensate PVT variations and improve energy-efficiency of subthreshold circuits significantly compared to worst-case design and operation with guardbanding.
- M-16 **A Full Chip Integrated Power and Substrate Noise Analysis Framework for Mixed-Signal SoC Design**, D. Kosaka*,****, Y. Bando*, G. Yokomizo**, K. Tsuboi**, Y. S. Li***, S. Lin***, M. Nagata*,****, *Kobe University, **STARC, ***Apache Design Solutions, Inc., ****A-R-Tec Corp.
A fully integrated framework of full-chip power and substrate noise analysis is discussed, featuring description of transistor-level custom circuits as dynamic noise sources, a high capacity solver for chip-level substrate coupling, and noise back annotation flow to transistors of sensitive circuits. Recursive evaluation of power current and operation timing under the presence of dynamic IR drop greatly improves the accuracy of analysis. A 90-nm CMOS chip was examined both by on-chip noise measurements and full-chip noise analysis.

- M-17 **An Accurate and Fast Behavioral Model for PLL Frequency Synthesizer Phase Noise/Spurs Prediction**, Xiaozhou Yan, Xiaofei Kuang, Nanjian Wu, Chinese Academy of Sciences
- This paper presents a behavior model for PLL Frequency Synthesizer. All the noise sources are modeled with noise voltages or currents in time-domain. An accurate VCO noise model is introduced, including both thermal noise and $1/f$ noise. The behavioral model can be co-simulated with transistor level circuits with fast speed and provides more accurate phase noise and spurs prediction. Comparison shows that simulation results match very well with measurement results.
- M-18 **Pathfinding for 22nm CMOS Designs using Predictive Technology Models**, Xia Li, Wei Zhao, Yu Cao*, Zhi Zhu, Jooyoung Song, David Bang, Chi-Chao Wang*, Seung H. Kang, Joseph Wang, Matt Nowak, Nick Yu, Qualcomm Incorporated, *Arizona State University
- Traditional IC scaling is difficult at the 22nm node. Dealing with these challenges increase product development cycle time. For continued CMOS scaling, it requires having Predictive Technology Models to start design explorations in new process nodes as early as possible. In this paper we propose a strategy that enables simultaneous investigation of advanced process and design concepts. We capture the heuristic device behavior during the scaling, make tradeoffs of circuit design for next technology node.
- M-19 **An SRAM Reliability Test Macro for Fully-Automated Statistical Measurements of V_{min} Degradation**, Tae-Hyoung Kim, Wei Zhang, Chris H. Kim, University of Minnesota
- An SRAM reliability test macro is designed in a 1.2V, 65nm CMOS process for statistical measurements of V_{min} degradation. An automated test program efficiently collects statistical V_{min} data and reduces test time. The proposed test structure enables V_{min} degradation measurements for different SRAM failure modes such as the SNM-limited case and the access-time-limited case. The impact of voltage stress on the time to cell data flip was measured.
- M-20 **A 60 GHz CMOS Balanced Downconversion Mixer with a Layout Efficient 90° Hybrid Coupler**, R. E. Amaya, Cornelius J. Verver, Communications Research Centre, Ottawa, Canada.
- This paper presents the design and implementation of a downconversion mixer implemented in a standard 130nm commercial CMOS process and aimed at applications in the 60 GHz ISM band. A balanced mixer configuration was implemented by using a layout efficient 90° hybrid coupler which serves as a diplexer to inject the LO signal while also providing two outputs with 3dB of attenuation and 90° phase shift. The mixer achieves a conversion gain of +0.3 dB and OIP3 of +2.3 dBm. The mixer also consumes 200 μ A of DC current and 8mA of peak current while driven from a single 2V supply. The layout area including test pads is 1.4mm x 1.0mm.
- M-21 **A 0.46ps RJrms 5GHz Wideband LC PLL for Multi-Protocol 10Gb/s SerDes**, C. Rao, A. Wang, S. Desai, Prism Circuits Inc.
- A 2.3 to 5GHz LC PLL is implemented in 65nm CMOS for 0.6 to 10Gb/s SerDes. The LC VCO has 67% coarse tuning range, 9.6% worst-case hold range. RJrms at TX output with a clock pattern is 460fs at 5GHz, 548fs at 3.125GHz. Total power dissipated is 29mW at 5GHz.
- M-22 **A 10MHz to 315MHz Cascaded Hybrid PLL with Piecewise Linear Calibrated TDC**, Minyoung Song, Young-Ho Kwak, Sunghoon Ahn, Wooseok Kim*, ByeongHa Park* and Chulwoo Kim, Korea University, *Samsung Electronics
- An ADPLL with a piecewise linear calibrated hierarchical TDC is proposed to achieve a wide range of operation and a CPPLL is cascaded to filter out $1/f$ noise. A phase selectable divider is also proposed to divide the clock frequency while keeping the relative phase difference of output same as that of input. The cascaded hybrid PLL fabricated in 65nm CMOS process burns 17mW and occupies 0.4mm². The measured jitters are 1.1nspp and 223.6psrms, respectively with a multiplication factor of 1,024.
- M-23 **A 430MHz-2.15GHz Fractional-N Frequency Synthesizer for DVB and ABS-S Applications**, P. Yu, Z. Gong, M. Gu, Y. Shi, F. Dai*, Suzhou-CAS Semiconductors Integrated Technology Research Center, *Auburn University
- The frequency synthesizer covers a very wide frequency range of 430MHz-2.15GHz while integrates only one on-chip inductor. The AFC helps to correct VCO sub-band selection when PVT varies. The LDO helps to suppress in-band and out-of-band noise generated by 3rd-order $\Sigma\Delta$ modulator. The fast setting time and low phase noise make the PLL suitable of numerous multi-band, multi-standard applications such as DVB and ABS-S
- M-24 **SiGe Digital Frequency Dividers with Reduced Residual Phase Noise**, S. Horst, S. Phillips, H.M. Lavasani, F. Ayazi, J.D. Cressler, Georgia Institute of Technology
- A new design methodology for achieving very low residual phase noise in SiGe HBT digital frequency dividers is presented. A modified CML D latch design is proposed that enables the latch to draw more current, thereby reducing the residual phase noise. The latch modification yields a 10 dB phase noise improvement over a standard D latch topology, with measurements at 10 GHz resulting in a phase noise floor of -160 dBc/Hz. The circuit dissipates 350 mW of DC power, but a standard phase noise figure-of-merit that accounts for phase noise, DC power dissipation, and operating frequency, reveals that this new design is among the best in its class.
- M-25 **A 54-862 MHz CMOS Direct Conversion Transceiver for IEEE 802.22 Cognitive Radio Applications**, Jongsik Kim, Seung Jun Lee, Seungsoo Kim, Jong Ok Ha, Junki Min*, Yun Seong Eo, Hyunchoi Shin, Kwangwoon University, *Samsung Electro-Mechanics Co.
- A CMOS single-chip transceiver IC is developed for IEEE 802.22 cognitive radio applications. Over the 54 to 862 MHz ultra

wideband, the in-band harmonic distortions of the transmitter and the unwanted harmonic mixing of the receiver are effectively suppressed by exploiting the dual-path direct-conversion architecture. A seamless coverage of the full band is achieved by employing a fractional-N PLL with a single LC VCO and a multi-modulus LO generator. Implemented in 0.18 μm CMOS, the receiver achieves 110 dB gain dynamic range, < 8.5 dB noise figure, and > -11 dBm IIP3 at the LNA bypass mode. The transmitter delivers -3 dBm output power with OP1dB and OIP3 greater than +6.4 dBm and +15.9 dBm, respectively. On-chip calibration circuits suppress the image and carrier leakage components below -41 dBc across the total band.

M-26

A 1.8V, Sub-mW, Over 100% Locking Range, Divide-by-3 and 7 Complementary-Injection-Locked 4 GHz Frequency Divider, Y.-C. Lo, H.-P. Chen, J. Silva-Martinez, S. Hoyos, Texas A&M University

A low-power wideband divide-by-odd-ratio ring-oscillator-based complementary-injection-locked frequency divider that widens its locking range over 100% is proposed. The differential architecture's frequency locking range spans from 1.4-to-4.4 GHz with an input incident power of -4dBm. The power consumption of the 0.18 μm CMOS topology is 0.9mW while locked at 4.7GHz.