

Monday Posters

Monday Evening, September 19
Cascade/Sierra Ballroom
5:00 pm – 7:00 pm

- M-1 **A Discrete-Time Charge-Domain Filter with Bandwidth Calibration for LTE Application**, *Ming-Feng Huang, Industrial Technology Research Institute*

A discrete-time charge-domain filter (CDF) with bandwidth calibration was proposed for LTE application. The CDF, based on feedback gain and delay, could suppress sinc distortion to achieve a like brick-wall filtering. The measurement showed that CDF performed a >59dB adjacent-channel rejection, >85dB stop-band attenuation, and 5-to-26 MHz reconfigurable bandwidth.

- M-2 **A True Single SoC for UHF Mobile RFID Reader**, *J. Kim, S. Yun, W. Oh, M. Kil, S. Cho, PHYCHIPS Inc.*

A true single SoC for UHF Mobile RFID Reader has been implemented in a 0.18 μ m embedded flash CMOS technology. The SoC includes 900MHz RF transceiver, PA, MODEM, MCU, memory and peripherals with fully compliant ISO/IEC 18000-6C and EPC Global Class1 Gen2 reader protocol.

- M-3 **An 80% Peak Efficiency, 410mW, Single Supply Rail Powered Class-I Linear Audio Amplifier**, *Z. Peng, S. Yang, Y. Feng, Z. Hong, B. Liu*, Fudan University, *Analog Devices*

A high efficiency high linearity Class-I audio amplifier is presented. Efficiency is improved by adopting a self-generated adaptive supply. The employed gain compression technique uses only one positive supply to maintain good linearity, and achieve above 20% better efficiency over a conventional Class-AB design.

- M-4 **Band-gap Circuit Design Challenges in High-performance 32-nm Technology**, *J. Buller, J. Fletcher, S. Meyers, M. Robinson*, F. Tamayo, A. Prakash, D. Cabler, Advanced Micro Devices, *Vidatronic*

32-nm complementary metal oxide semiconductor (CMOS) silicon-on-insulator (SOI) with metal gate high-k (MGHK) offers high performance and low power for microprocessors. However, these advanced technologies come with challenges for analog design. Many of the stressor performance elements can adversely impact analog circuit behavior. For example, band-gap circuits, used ubiquitously in voltage references, are one such challenging component. We investigated both design and process methods that resulted in robust band-gap voltage and temperature response characteristics without impacting performance elements for microprocessor frequency.

- M-5 **Low Power and Error Resilient PN Code Acquisition Filter via Statistical Error Compensation**, *E. Kim, D. Baker, S. Narayanan, D. Jones, N. Shanbhag, University of Illinois at Urbana Champaign*

We present a 256-tap PN code acquisition filter in an 180nm CMOS process employing statistical system-level error compensation. Under voltage overscaling (VOS), near constant detection probability P_{det} above 90% with 5.8x reduction in energy is achieved at a supply voltage 27% below the point of first failure (PoFF) with an error rate p_e of 0.868. This is an improvement of 5.8x in energy-efficiency over conventional error free designs and 3.79x in energy-efficiency and 2170x in error tolerance over existing error tolerant designs.

- M-6 **0.4V SRAM with Bit Line Swing Suppression Charge Share Hierarchical Bit Line Scheme**, S. Moriwaki, A. Kawasumi, T. Suzuki, T. Sakurai*, S. Miyano, Semiconductor Technology Academic Reserch Center, *The University of Tokyo

128kbit SRAM with charge share hierarchical bit line scheme has been fabricated in 65nm foundry technology. By transferring the data between local bit lines and global bit lines with charge sharing, the variation of bit line swing which causes wasted power consumption in low voltage operation has been suppressed. 3.3 μ W/MHz of power consumption at 0.4V is achieved.

- M-7 **An Output Structure for a Bi-Modal 6.4-Gbps GDDR5 and 2.4-Gbps DDR3 Compatible Memory Interface**, Navin K. Mishra, Manish Jain, Phuong Le*, Sanku Mukherjee*, Arul Sendhil, Amir Amirkhany*, Rambus Chip Technologies, *Rambus Inc.

A bi-modal x32 memory interface supports 6.4-Gbps GDDR5 signaling as well as 2.4-Gbps DDR3 signaling with a 1.5V IO supply. The interface incorporates a novel driver and pre-driver structure that supports one-tap equalization and presents very small capacitive loading to the pins. The entire interface, including both data and request channels achieves 11.6mW/Gbps and 27.7mW/Gbps energy efficiencies in GDDR5 and DDR3 modes respectively, and communicates successfully with 1.6-Gbps DDR3 and 6.0-Gbps GDDR5 DRAMs.

- M-8 **A CMOS Image Sensor with on-chip Motion Detection and Object Localization**, B. Zhao, X. Zhang, S. Chen, Nanyang Technological Univeristy

This paper presents a CMOS image sensor with on-chip moving objects detection and localization. The sensor generates motion events by frame differencing. An on-chip localization unit processes the events on the fly and localizes moving objects in the scene. The sensor can switched to ROI mode and shoot a zoomed picture of the object. It has been fabricated using UMC 0.18 μ m CMOS process, power consumption was measured to only 0.4 mW at 100 FPS.

- M-9 **Ultra Low-FOM High-Precision $\Delta\Sigma$ Modulators with Fully-Clocked SO and Zero Static Power Quantizers**, Jian Xu, Xiaobo Wu, Menglian Zhao, Rui Fan, Hanqing Wang, Xiaofen Ma, Bill Liu*, Zhejiang University, *Analog Devices

Two high-precision MBSO-based Delta-Sigma modulators with ultra low FOM (< 45 fJ/conv.-step) are implemented in 0.18 μ m CMOS. To save 50% power, both modulators adopt novel fully-clocked SOs with new bias circuits. Modulator-I for bio-medical applications uses high density MOSCAPs and innovative area-efficient static power-less quantizer to achieve 85dB peak-SNDR over 10kHz BW and only 13 μ W at 1.0V supply. Modulator-II for audio applications employs another novel static power-less quantizer and duty cycle shift DWA to achieve 92dB peak-SNDR over 25kHz BW and only 58 μ W at 0.9V supply.

- M-10 **A New CMOS Image Sensor Readout Structure for 3D Integrated Imagers**, Shang-Fu Yeh, Jin-Yi Lin, Chih-Cheng Hsieh, Ka-Yi Yeh* and Chung-Chi Jim Li*, National Tsing Hua, Taiwan *Industrial Technology Research Institute

This paper presents a new CMOS image sensor (CIS) structure and ADC design for three-dimensional (3D) integrated imagers. The proposed CIS structure achieves a high spatial resolution without degrading the frame rate. A prototype chip shows that the array is expandable by modular sub-array design and is expected to achieve 100fps at multi-mega imaging for high-speed HDTV camera applications.

- M-11 **All-Digital 3-50 GHz Ultra-Wideband Pulse Generator for Short-Range Wireless Interconnect in 40nm CMOS**, C. Hu, P. Chiang*, Marvell Technology, *Oregon State University

A reconfigurable, 3-50GHz all-digital impulse generator for short-distance wireless communications is designed in 40nm-CMOS. Digital back-gate biasing is used for raised-cosine envelope pulse-shaping to achieve better spectral-mask efficiency. Pulse duration, duty-cycle, and

operating frequency are digitally programmable, in order to satisfy multi-band standards compatibility. An asymmetric inverter design within the Mono-Pulse-Generator (MPG) eliminates undesired glitches for the complementary clock edge. Occupying 350umx260um die area, the proposed impulse transmitter achieves a maximum data-rate of 3Gbps and an energy-efficiency of 0.5pJ/pulse for a 25GHz carrier frequency.

- M-12 **A 4GS/s, 8.45 ENOB and 5.7fJ/Conversion, Digital Assisted, Sampling System in 45nm CMOS SOI**, *M.A.T. Sanduleanu, S. Reynolds, J.O. Plouchart, IBM T.J. Watson Research Center*

A 4GS/s sampling system achieved 8.45-ENOB linearity with 5.7fJ/conversion energy efficiency. The measured IIP3 and IIP2 are 17.7dBm and 40dBm respectively. The ENOB of the sampler shows no degradation up to Nyquist frequency. Realized in a 45nm SOI CMOS the active area of the sampler is only 0.2 x 0.2mm².

- M-13 **Energy-Efficient Transceiver Circuits for Short-Range On-chip Interconnects**, *J. Postman, P. Chiang, Oregon State University*

Transceiver blocks for low-swing signaling across short on-chip wires are proposed. First, a charge-sharing transmitter enables adjustable swing signaling from a single supply voltage. Compact sense-amplifier offset correction is introduced that enables improved sensitivity without increasing energy/conversion. Finally, digital hysteresis tuning is used to implement compact decision feedback equalization. Optimized for low-energy applications and operating from V_{dd} = 0.2-1.0V, measurements show energy efficiencies of 4.0-136fJ/bit/mm across 1mm and 4mm wires in 65nm-CMOS.

- M-14 **A Novel Audio Playback Chip Using Digitally Driven Speaker Architecture with 80%@-10dBFS Power Efficiency, 5.5W@3.3V Supply and 100dB SNR**, *Michitaka Yoshino, Mitsuhiro Iwaide, Daigo Kuniyoshi, Hajime Ohtani, Akira Yasuda, Jun-ichi Okamura*, Hosei University, *Trigence Semiconductor*

A novel audio playback chip using digitally driven speaker architecture based on a delta-sigma modulator and newly proposed high-order mismatch shaper with novel dither circuit is presented. It can realize 5.5W output power into 4Ω speakers with only 3.3V power supply. The power efficiency from -10dBFS to 0dBFS is higher than 80%. The efficiency at low power output can realize long battery life. This chip can realize battery powered high-fidelity and high-power audio system.

- M-15 **32-nm SOI Programmable, High-bandwidth 8.0-GHz Digital PLL**, *Sanjeev K Maheshwari, Emerson Fang, Sanjeev Aggarwal, AMD, Inc.*

A digital phase-locked loop to filter clock jitter in source-synchronous serial link applications is presented. The PLL achieves bandwidth programmability from 20 to 300 MHz while allowing for a maximum input frequency of 4 GHz. An improved resolution bang-bang phase detector and a double-regulated, supply-insensitive VCO mitigate extreme noise environments.

- M-16 **A 38.6nV/Hz^{0.5} -59.6dB THD Dual-Band Micro-Electrode Array Signal Acquisition IC**, *Jing Guo, Jiageng Huang, Jie Yuan, Jessica Ka-Yan Law, Chi-Kong Yeung*, Mansun Chan, Hong Kong University of Science and Technology, *Chinese University of Hong Kong*

This paper reports the novel design of a dual-band monolithic MEA signal acquisition IC in a 0.35um CMOS process. It achieves low noise (0.9uVrms for LFP signal, 3.9uVrms for SP signal) and good linearity (-59.4dB THD for 20mVpp signal). Other performance also compares favorably against major bio-potential acquisition benchmark designs.

- M-17 **Analysis and Modeling of On-Chip Power Combiners and their losses in LINC Transmitters**, *A. Koukab, O.T. Amir, Swiss Federal Institute of Technology in Lausanne*

This paper presents a compact model for LINC (linear amplification with non linear components) transmitters and their power combiners. The study focuses on the detrimental effect of the transmission line nonidealities. A mathematical description of the system that considers these nonidealities is proposed. The developed analytical expressions can be used to optimize, analyze and build pre-distortion algorithms for this family of transmitters. The efficiency and linearity are reexamined in light of the new analytical expressions of the model.

- M-18 **Programmable Phase/Frequency Generator for System Debug and Diagnosis Using The IEEE 1149.1 Test Bus**, *T.-Y. Tsai, G. Roberts, McGill University*

A method of analog signal generation is presented that is suitable for digital test methodologies such as the IEEE 1149.1 test standard; it can be used to produce phase and frequency signals for system test debug and diagnosis. A 0.13 μ m chip at 4 GHz illustrates the signaling capabilities of this generator.

- M-19 **Overlapped Inductors and Its Application on a Shared RF Front-end in a MultiStandard IC**, *L. Feng, R. Sadhwani, Y. Peperovits, C. D. Hull, J. C. Jensen, Intel Corporation*

A technique to build overlapped inductors at the same location while keeping good isolation between them is presented. The key idea is to use magnetic and electric cancellation to reduce coupling. A shared LNA for WiFi and Bluetooth (BT) applications using the overlapped inductor is proposed. It enables independent gain control up to the first RF stage in a receiver so that the system integration complexity is reduced.

- M-20 **A 1.0V 45nm Nonvolatile Magnetic Latch Design and Its Robustness Analysis**, *Peiyuan Wang, Xiang Chen, Yiran Chen, Hai (Helen) Li*, Seung Kang**, Xiaochun Zhu**, Wenqing Wu**, University of Pittsburgh, *Polytechnic Institute of New York University, **Qualcomm Inc.*

A new nonvolatile latch design is proposed based on the magnetic tunneling junction (MTJ) devices. In the standby mode, the latched data can be retained in the MTJs without consuming any power. Two types of operation errors, namely, persistent and non-persistent errors, are quantitatively analyzed by including the process variations and thermal fluctuations during the read and write operations. A design at 45nm technology node is used as the example to discuss the design tradeoffs.

- M-21 **A 1V 13mW Frequency-Translating $\Delta\Sigma$ ADC with 55dB SNDR for a 4MHz Band at 225MHz**, *P. M. Chopp, A. A. Hamoui, McGill University*

A frequency-translating delta-sigma ADC is fabricated in 1V 65nm CMOS. It uses single-path mixing inside its feedback loop to down-convert a 4MHz band from 225MHz (IF1) to 25MHz (IF2), achieving 55dB SNDR. Low power (13mW) is realized by sampling below IF1, and by noise-shaping at IF2.

- M-22 **CMOS Field-Modulated Color Sensor**, *D. Ho, G. Gulak, R. Genov, University of Toronto*

A digital photosensor for multi-color imaging is presented. By modulating the electric field applied to the photo sensing region, the sensor reports light intensity at discrete wavelengths. It utilizes standard CMOS technology, integrating a spectrally-sensitive photodiode and a current-to-frequency analog-to-digital converter on the same die.
