

Monday Poster Session

Monday Evening, September 20

Cascade/Sierra Ballroom

5:00 pm – 7:00 pm

- M-1 **Amorphous Silicon 7 Bit Digital-to-Analog Converter on PEN**, *Aritra Dey, Hongjiang Song*, Tofayel Ahmed*, Sameer Venugopal, David Allee, Flexible Display Center at Arizona State University, *Intel Corp, Arizona*

A 7-bit switched capacitor D/A converter (DAC) is built using only n-channel amorphous silicon hydride (a-Si:H) thin film transistors (TFTs) and capacitors. The circuit is fabricated on both polyethylene naphthalate (PEN) and glass using a low temperature process, compatible with flexible plastic substrates. Switched capacitor architectures are chosen as they are less prone to TFT aging because of electrical stress, and also to active device mismatches. The measurements from the fabricated DAC show excellent linearity characteristics, achieving a DNL of less than ± 0.6 LSB and INL of less than ± 1 LSB without additional calibration, at a conversion rate of 500 Hz.

- M-2 **Design of Low-noise CMOS MEMS Accelerometer with Techniques for Thermal Stability and Stable DC Biasing**, *S. S. Tan, C. Y. Liu, L. K. Yeh, Y. H. Chiu, Michael S.-C. Lu, Klaus Y. J. Hsu, National Tsing Hua University*

An integrated high-sensitivity CMOS MEMS capacitive accelerometer with thermal stability has been designed and demonstrated in this work. Issue of obtaining stable DC bias at input terminals is particularly addressed. Sensitivity of 595 mV/g is achieved in the accelerometer and the overall noise floor is $50 \mu\text{g}/\sqrt{\text{Hz}}$, which corresponds to an effective capacitance noise floor of $0.024 \text{ aF}/\sqrt{\text{Hz}}$. The zero-g thermal variation is as low as $1.68 \text{ mg}/^\circ\text{C}$.

- M-3 **A Signal-agnostic Compressed Sensing Acquisition System for Wireless and Implantable Sensors**, *Fred Chen, Anantha Chandrakasan, Vladimir Stojanovic, Massachusetts Institute of Technology*

We present the design and implementation of a new sensor system based on the theory of compressed sensing that addresses the energy and telemetry bandwidth constraints of wireless sensors. A hardware efficient realization demonstrates continuous data acquisition and compression of up to 40x on an EEG signal, while relaxing the noise constraints of the analog frontend by nearly 10x. The hardware is implemented in a 90nm CMOS process and consumes $1.9 \mu\text{W}$ at 0.6V and 20kS/s.

- M-4 **Analysis and Demonstration of MEM-Relay Power Gating**, *Hossein Fariborzi, Matthew Spencer*, Vaibhav Karkare**, Jaeseok Jeon*, Rhessa Nathanael*, Chengcheng Wang**, Fred Chen, Hei Kam*, Vincent Pott*, Tsu-Jae King Liu*, Elad Alon*, Vladimir Stojanović, Dejan Marković**, Massachusetts Institute of Technology, *University of California, Berkeley, **University of California, Los Angeles*

This paper shows that due to their negligibly low leakage, chips utilizing MEM relay power gates can potentially achieve lower energy than those utilizing CMOS power gates. A simple analysis provides design guidelines and savings estimates for relay designs. Finally, a relay chip successfully power-gating a CMOS chip is demonstrated.

- M-5 **An Energy-Efficient SoC for Closed-Loop Medical Monitoring and Intervention**, *Xiaoyu Zhang, Hanjun Jiang, Fule Li, Songyuan Cheng, Chun Zhang, Zhihua Wang, Tsinghua*

University

This paper presents an energy-efficient SoC dedicated for portable medical monitoring and intervention systems capable of closed-loop control. The SoC contains a 0.9V/165 μ W MCU and a dual-band RF block including a 403MHz transceiver for data link and a 915MHz receiver for wake-up link. The data link transceiver is composed of a 200kbps FSK transmitter and a 64kbps OOK receiver, consuming 5.58mW and 3.13mW, respectively. The 915MHz receiver based on wireless energy harvesting gives the SoC the unique power-silent work-on-demand capability, avoiding wasting energy during the idle-listening period. The power consumption of the integrated MCU is reduced by means of acceleration instructions and modules. The implemented work-on-demand MAC protocol with instant response satisfies the requirements of typical medical applications. The SoC is fabricated in 0.18 μ m CMOS technology, and occupies a die area of 5.9mm².

- M-6 **A Novel Readout IC with High Noise Immunity for Charge-Based Touch Screen Panels**, Jun-HyeokYang, Seung-Chul Jung, Young-Jin Woo, Jin-Yong Jeon, Sung-Woo Lee, Chang-byung Park, Hyun-Sik Kim, Seung-Tak Ryu, Gyu-Hyeong Cho, KAIST

The critical issues in charge-based touch screen panels for large size display are noise and speed. To solve these, this paper introduces a 'Delta-integration' scheme. It effectively solves local noise and speed issues. In addition, it can replace a high-resolution ADC with a comparator and counter.

- M-7 **Ground Rule Slack Aware Tolerance-Driven Optical Proximity Correction for Local Metal Interconnects**, Shayak Banerjee, Kanak Agarwal*, Michael Orshansky, University of Texas - Austin, *IBM Research

The current method of communicating process capabilities to the designer is in the form of ground rules. However, due to constraints on the complexity and number of rules, there may exist shapes that are design-rule clean but difficult to manufacture. This problem is exacerbated in local routes drawn on 1x metal (M1) which allows highly bi-directional shapes at tight spacing. On the other hand, local M1 routes have low parasitic resistance and capacitance as compared to device impedances. Hence there exists an opportunity to perturb these shapes to improve their manufacturability without significant performance impact. We propose to guide this perturbation by the amount of leeway available between the designed values and the ground rules – which we refer to as ground rule slack. In this paper, we utilize ground rule slack to generate tolerance bands for layout features. We further develop a tolerance-driven optical proximity correction (TD-OPC) algorithm which utilizes such tolerance bands to find a lithographically optimal mask solution for manufacturing. Our experiments on sample layouts shows that the use of this methodology helps reduce lithographic hotspots by 59% in comparison to process window optical proximity correction.

- M-8 **HVM Performance Validation and DFM Techniques used in a 32nm CMOS Thermal Sensor System**, David Duarte, Paola Zepeda, Suching Hsu, Atul Maheshwari, Greg Taylor, Intel Corp.

This paper describes the design of a thermal sensor and its accompanying supply voltage regulator, both implemented in a Hi-K, metal-gate, 32nm technology. The designs incorporated built-in run-time variability reduction schemes and silicon data verified the expected performance. The DFT circuits needed to validate circuit performance in HVM are described.

- M-9 **Single Event Transient Mitigation in Cache Memory using Transient Error Checking Circuits**, Xiao Yinyao, Lawrence Clark, Dan Patterson, Keith Holbert, Arizona State University

Protecting a high performance radiation hardened by design cache from single-event transient induced peripheral circuit errors is presented. A 16 kB cache and test engine, fabricated on an

IBM 90 nm bulk CMOS process, irradiated with heavy ions, is used to provide experimental validation of the design.

- M-10 **Elimination of Half Select Disturb in 8T-SRAM by Local Injected Electron Asymmetric Pass Gate Transistor**, Kentaro Honda, Kousuke Miyaji, Shuhei Tanakamaru, Shinji Miyano*, Ken Takeuchi, University of Tokyo, *Semiconductor Technology Academic Research Center

An 8T-SRAM cell with asymmetric PG transistor by local electron injection is proposed. Both side injection scheme and SR one side injection scheme are also proposed and analyzed for 6T-SRAM and 8T-SRAM cell. The SR one side injection scheme combined with the 8T-SRAM shows the best characteristics and suppresses half select disturb by 141% without write margin and read speed degradation.

- M-11 **Opportunities for PMOS Read and Write Ports in Low Voltage Dual-Port 8T Bit Cell Arrays**, Bibiche Geuskens, Muhammad Khellah, Jaydeep Kulkarni, Tanay Karnik, Vivek De, Intel Labs

Strained silicon has enhanced PMOS transistor current much more than NMOS. As such, IDSATN/IDSATP equal to 1 is nearing reality. This work studies the effect of this presumably continuing trend on dual-port 8T bit cell performance. Preference for using NMOS or PMOS in write and read ports is shown to depend on current ratio, VMIN circuit assist and array access type.

- M-12 **Radio-Frequency Signal Tracking (RFST) Technique for Improving Efficiency in RF Amplifier Supplying Systems**, Yu-Huei Lee, Wei-Chan Wu, Pin-Chin Huang, Shih-Wei Wang, Ke-Horng Chen, National Chiao Tung University

A current mode buck-boost (BB) converter with the RFST technique is proposed to improve the efficiency of radio frequency (RF) power amplifiers (PAs). The fast up/down tracking is implemented to meet the requirement of the RF amplifier supplying systems. Besides, the current mode control with the self-tuning pulse skipping (SPS) mechanism can extend the effective duty cycle to achieve voltage regulation and get high efficiency when the input voltage is close to the output. Through the RFST tracking technique, the tracking speed from 3 V to 2 V and vice versa are 15 μ s and 20 μ s, respectively. Besides, the recycling energy improves the efficiency to be higher than 85 % under a high switching frequency of 5 MHz.

- M-13 **A 1.2A 2MHz Tri-Mode Buck-Boost LED Driver With Feed-Forward Duty Cycle Correction**, Sarvesh Bang, Damian Swank, Arun Rao, William McIntyre, Qadeer Khan*, Pavan Hanumolu*, National Semiconductor Corporation, *Oregon State University

A flash LED Buck-Boost driver employs a dual duty cycle control and feed-forward duty cycle correction to achieve high efficiency over the entire Li-On battery voltage range of 3.0 to 5.2V. Fabricated in a 0.5 μ m CMOS process, the converter uses an external 1 μ H inductor and a 10 μ F capacitor and operates at 2MHz switching frequency. The measured peak efficiency is 83% and 87% at 1.2A and 0.6A LED currents, respectively. This achieved efficiency represents an improvement of more than 10% over conventional approaches.

- M-14 **0.18-V Input Charge Pump with Forward Body Biasing in Startup Circuit using 65nm CMOS**, Po-Hung Chen, Koichi Ishida, Xin Zhang, Yasuaki Okuma*, Yoshikatsu Ryu*, Makoto Takamiya, Takayasu Sakurai, The University of Tokyo, *Semiconductor Technology Academic Research Center

To kick up the boost converter in low operation voltage, a charge pump circuit with forward body biasing is proposed. Because of applying the appropriate forward bias to each MOSFET, the pumping efficiency can be improved more than conventional charge pump without applying forward bias. The experiment results show that the proposed charge pump can improve the

output current more than 150% with 1.5% area overhead. The boost converter connected with the proposed charge pump can kick up the 0.18-V input to 0.74-V output while the conventional one only provides 4.7mV output. With the higher pumping ability and the lower kick-up voltage, the proposed charge pump circuit is more suitable for energy harvesting applications which only provide low voltages.

- M-15 **A Novel Wideband 1- π Model with Accurate Substrate Modeling for On-Chip Spiral Inductors**, *Huanhuan Zou, Jun Liu, Jincai Wen, Huang Wang, Lingling Sun, Zhiping Yu, Hangzhou Dianzi University*

This paper presents a novel wideband 1- π equivalent circuit model for on-chip spiral inductors is presented. A substrate network, consisting of R/L/C, is proposed to model the broadband loss mechanisms in the silicon substrate. The skin and distributed effects for windings have been taken into account. A series of inductors with different geometries are fabricated in standard 0.18- μ m 1P6M RF CMOS process to verify the model. Excellent agreements have been obtained between the modeled and measured data up to 40 GHz, which verify that the proposed 1- π model naturally has better wideband prediction capability than published 1- π or T-models, and simpler topology than 2- π models for on-chip spiral inductors.

- M-16 **Reliability Analysis of Analog Circuits Using Quadratic Lifetime Worst-Case Distance Prediction**, *Xin Pan, Helmut Graeb, Technische Universitaet Muenchen*

This paper proposes an efficient method to predict the lifetime yield of analog circuits considering the joint effects of manufacturing process variations and parameter lifetime degradations. The method uses the idea of worst-case distance, which is an indicator of circuit robustness concerning process variations. The worst-case distance in circuit lifetime is predicted based on a new, quadratic prediction model in time domain. The lifetime yield of the circuit is obtained based on this quadratic model. We prove for the first time that the lifetime yield value is directly applicable to the calculation of reliability function and lifetime distribution of analog circuits, while previous modeling techniques either are only applicable for digital circuits, or require long simulation time. The experimental results show that the proposed method has an average error smaller than 5%, with a speed up of six times in comparison to an iterative optimization based lifetime yield analysis method.

- M-17 **A 70 GHz 10.2 mW Self-Demodulator for OOK Modulation in 65-nm CMOS Technology**, *Xia Li, Peter Baltus, Paul van Zeijl*, Dusan Milosevic, Arthur van Roermund, Eindhoven University of Technology, *Philips Research Eindhoven*

A 70.86 to 79.29 GHz low-power self-demodulator for on-off-keying (OOK) modulation is realized in TSMC 65-nm CMOS technology. By using a frequency-sweeping injection-locked oscillator (IJLO), the OOK modulated 70 GHz signal is demodulated by itself in a passive mixer and an 8.43 GHz bandwidth is achieved at 10.2 mW power consumption from a 1-V supply. The conversion gain is 10 dB and constant over the entire bandwidth. The core area of the chip is 0.072 mm².

- M-18 **A 10 GHz Frequency-Drift Temperature Compensated LC VCO with Fast-Settling Low-Noise Voltage Regulator in 0.13 μ m CMOS**, *Hiroshi Akima, Aleksander Dec, Timothy Merkin, Ken Suyama, Epoch Microelectronics, Inc.*

An LC voltage controlled oscillator (VCO) with frequency-drift temperature compensation circuit in 0.13 μ m CMOS process is presented. The compensation circuit consists of MOS inversion varactor and utilizes negative temperature coefficient of VBE characteristic of BJT. With the compensation circuit, 82 % of improvement in VCO frequency-drift due to temperature is demonstrated in measurement. The VCO is supplied from a fast-settling low-noise voltage regulator.

M-19 **A 43.5mW 77GHz Receiver Front-End in 65nm CMOS suitable for FM-CW Automotive Radar**, Roc Berenguer, Gui Liu, Abe Akhiyat, Keya Kamtikar, Yang Xu, Illinois Institute of Technology

A low power 77GHz receiver front-end, suitable for a FM-CW Automotive Radar has been implemented using a 65nm RFCMOS process. It has been designed using direct conversion architecture. The fabricated front-end exhibits a maximum voltage gain of 15dB over the baseband and presents a LNA NF of 7dB which makes it suitable for next generation of collision avoidance systems. The achieved power consumption of the receiver front-end is 43.5mW from a 1.5V supply.

M-20 **A 27mW 2.2dB NF GPS Receiver using a Capacitive Cross-coupled Structure in 65nm CMOS**, Hyunwon Moon, Seung-Chan Heo, Hwayeal Yu, Jinhyuck Yu, Ji-Soo Chang, Seung-Il Choi, Sangyoub Lee, Woo-Seung Choo, Byeong-Ha Park, Samsung Electronics

A fully integrated low-IF GPS receiver with minimum external components is implemented in a 65nm CMOS process. It has an integrated LNA and an active complex bandpass filter with a switchable signal bandwidth of 2MHz or 6 MHz to achieve the SNR improvement. To reduce power consumption, the current reusing method and current mode interface technique using a capacitive cross-coupled common-gate structure are applied. The measured noise figure of whole receiver including an external inter-stage SAW filter is 2.2dB. Its current consumption is 15mA at 1.8V supply.

M-21 **A Low Power High Reliability Dual-Path Noise-Cancelling LNA for WSN Applications**, Ming-Yeh Hsu, Chao-Shiun Wang, Chorng-Kuang Wang, National Taiwan University

This paper presents a dual-path noise-cancelling (DPNC) LNA, which is designed for low power wireless sensor network (WSN) applications and operates at 2.4GHz band. The proposed DPNC LNA can effectively cancel internal circuit noise while consuming less power by gm-boosted technique. The measured voltage gain and NF are 22dB and 3.7dB, respectively. IIP3 is +8dBm and consumes 1.2mW with a 1.0V single supply. Fabricating in the 0.18 μ m standard CMOS process, the LNA occupies an active area of 0.3mm².

M-22 **W-Band Pulsed Radar Receiver in Low Cost CMOS**, Ning Zhang, Kenneth O, University of Florida

A CMOS heterodyne receiver integrating a phase-locked loop that includes a bulk of transmitter functions for W-band pulsed radar is realized using low leakage transistors of a low cost 65-nm bulk CMOS process with 5 thin and 1 thick metal layers used to manufacture cell phone RFIC's. The peak conversion gain of receiver is 7 dB and the minimum NF is 10.8 dB between 78 and 88 GHz in measurement. The entire receiver front-end consumes ~190 mW.