

Session 5 - Frequency Synthesizers

Monday Afternoon, September 14
Oak Ballroom

Chair: Cicero Vaucher, NXP
Co-Chair: Rick Booth, Panasonic

This session presents modern frequency synthesis techniques in integrated circuits. This includes all digital PLLs, improved frequency to digital converters, fractional-n synthesizers, and injection locked frequency dividers.

1:30 **Introduction**

1:35 **Insights into Wideband Fractional All-Digital PLLs for RF Applications (INVITED)**, *Enrico Temporiti, Colin Weltin-Wu*, Daniele Baldi, Riccardo Tonietto** and Francesco Svelto*, STMicroelectronics, Pavia, Italy, *Università di Pavia, Pavia, Italy, **STMicroelectronics, Grenoble, France*

Technology scaling and large-scale integration make the operating environment increasingly hostile for traditional analog design. In the area of frequency synthesis, All-Digital PLLs (ADPLLs) provide an attractive alternative to conventional PLLs. However, wideband fractional ADPLLs come with a different set of problems, principally in-band spurious tones. Techniques to suppress spurious tones would eliminate a major obstacle for ADPLLs' widespread proliferation into wireless RF applications. In this paper we first describe the evolution from the analog PLL to the divider-less ADPLL, of major interest for RF to date, then develop a model to predict location and level of spurs. Validation is performed through experiments on an ADPLL fabricated in 65nm digital CMOS.

2:25 **Time to Digital Converter Based on a 2-dimensions Vernier Architecture**, *Antonio Liscidini, Luca Vercesi and Rinaldo Castello, University of Pavia, Pavia, Italy*

A novel 2-dimension Vernier Time to digital converter (TDC) is presented. The proposed architecture reduces drastically the number of delay stage required by linear TDCs minimizing the power consumption and the area of the design. A 7bits TDC prototype realized in 65nm CMOS technology is presented. The chip has a resolution of 4.8ps with a power consumption of 1.7mW at a conversion rate of 50Msps.

2:50 **A Fractional-N PLL Modulator with Flexible Direct Digital Phase Modulation**, *Mark Ferriss, Davin Lin and Michael Flynn, University of Michigan, Ann Arbor, MI*

A 2.6GHz fractional-N synthesizer with a flexible digital modulation scheme is presented. The PLL output is modulated by adding a digital signal directly to the output of the phase detector. A pre-emphasis filter is used to allow switching rates faster than the loop bandwidth. The transmitter supports GMSK, OQPSK, BSK or any constant envelop modulation scheme. Measurements are presented at 300kBit/sec. The 0.7mm² prototype in 0.13µm CMOS consumes 20mW from a 1.5V supply.

3:15 PM **BREAK**

3:30 **A Sub-0.75°_{RMS}-Phase-Error Differentially-Tuned Fractional-N Synthesizer with On-Chip LDO Regulator and Analog-Enhanced AFC Technique**, *Lei Lu, Lingbu Meng, Liang Zou, Hao Min and Zhangwen Tang, Fudan University, Shanghai, China*

This paper presents a low-phase-error wideband fractional-N frequency synthesizer. Differential tuning is described and a level shift circuit is proposed to obtain symmetrical tuning range. On-chip LDO regulator is designed to improve the power supply rejection for VCO. A voltage monitor is used to enhance the digital AFC technique to overcome the temperature variation. The synthesizer was implemented in a 0.18-µm CMOS process with a 16-mA supply current and a 1.47-mm² die area. The measured in-band phase noise is less than -97 dBc/Hz at a 10-kHz frequency offset and the integrated phase error is less than 0.75°_{RMS}. The measured reference spur is less than -71dBc and the locking time is smaller than 20 µs.

3:55 **A Sub-2.5ns Frequency-Hopped Quadrature Frequency Synthesizer in 0.13-µm Technology**, *Narasimha Lanka, Satwik Patnaik and Ramesh Harjani, University of Minnesota, Minneapolis, MN*

This paper presents a fast-hopping frequency synthesizer architecture with quadrature outputs, based on sub-harmonic injection locking, that is compliant with Wireless-USB/WiMedia specifications. The overall architecture is a CMOS-only implementation and has been fabricated in 0.13-µm SiGe BiCMOS process. Measurement results indicate lock-times of less than 2.5 ns, a locked phase noise of -114 dBc/Hz at 1 MHz offset and a quadrature accuracy of better than 0.5 degrees. The frequency synthesizer (excluding output buffers) occupies an area of 0.27 sq.mm. and consumes 14.5 mW of power. The best and worst case spur suppression achieved are 47 and 31 dB, respectively. This is the lowest power fast-hopping quadrature frequency synthesizer that has been reported to date.

4:20 **A 5.2mW Ku-Band CMOS Injection-Locked Frequency Doubler with Differential Input / Output**, *Enrico Monaco, Mattia Borgarino, Francesco Svelto* and Andrea Mazzanti, Università degli Studi di Modena e Reggio E, Modena, Italy, *Università degli Studi di Pavia, Pavia, Italy*

A novel circuit topology, consisting of an LC oscillator injection locked by a push-push transistors pair, is proposed to realize a low power frequency multiplier by two. Prototypes, in 0.13µm CMOS, show 30% locking range around 13GHz with 3dBm input power. Corepower dissipation is 5.2mW only.

Session 6 - MEMS, Biomedical, and Sensors

Monday Afternoon, September 14
Fir Ballroom

Chair: Hasnain Lakdawala, Intel Corporation
Co-Chair: Kenneth Szajda, LSI Logic

This session showcases the state of the art advances in the field of circuit techniques and system integration for biomedical applications, MEMS, sensors and imagers.

1:30 **Introduction**

1:35 **MEMS for Integrated Timing and Spectral Processing (INVITED)**, Farrokh Ayazi, Georgia Institute of Technology, Atlanta, GA
6-1

This paper presents a review of micro-electromechanical devices for frequency references and RF spectral processing. The application of high-Q pure silicon and AlN-on-silicon bulk acoustic wave resonators in low phase-noise reference oscillators is discussed and compensation challenges are described. Low-loss piezo-acoustic filters and high-Q tunable and switchable silver passives are presented for applications in multi-mode front-end modules and spectral processors.

2:00 **Fully-Monolithic, 600°C Differential Amplifiers in 6H-SiC JFET IC Technology**, Amita Patil, Xiao-an Fu, Mehran Mehregany and Steven Garverick, Case Western University, Cleveland, OH
6-2

A family of fully-integrated differential amplifiers were designed and fabricated in 6H-SiC, n-channel JFET integrated-circuit technology. A single-stage amplifier with resistor loads has gain-bandwidth of ~2.8 MHz, and differential-mode gain that varies by less than 1 dB from 25-600C. A two-stage amplifier with current-source loads and common-mode feedback in 1st-stage, and resistor loads in 2nd-stage has gain-bandwidth of 1.4 MHz, and differential-mode gain of 69 dB at 576C, with just 3.6 dB gain-variation from 25-576C.

2:25 **A 32x32 50ps Resolution 10 bit Time to Digital Converter Array in 130nm CMOS for Time Correlated Imaging.**, Justin Richardson, Richard Walker, Lindsay Grant*, David Stoppa**, Fausto Borghetti**, Edoardo Charbon^, Marek Gersbach^ and Robert Henderson, The University of Edinburgh, Edinburgh, UK, *STMicroelectronics, Edingburgh, UK, **Fondazione Bruno Kessler, Trento, Italy, ^EPFL, Lausanne, Switzerland
6-3

We report the design and characterisation of a 32x32 time to digital (TDC) converter plus single photon avalanche diode (SPAD) pixel array implemented in a 130nm imaging process. Based on a gated ring oscillator approach, the 10 bit, 50µm pitch TDC array exhibits a minimum time resolution of 50ps, with accuracy of ±0.5 LSB DNL and 2.4 LSB INL. Process, voltage and temperature compensation (PVT) is achieved by locking the array to a stable external clock. The resulting time correlated pixel array is a viable candidate for single photon counting (TCSPC) applications such as fluorescent lifetime imaging microscopy (FLIM), nuclear or 3D imaging and permits scaling to larger array formats.

2:50 **RF-CMOS-MEMS Based Frequency-Reconfigurable Amplifiers (INVITED)**, Tamal Mukherjee and Gary Fedder, Carnegie Mellon University, Pittsburgh, PA
6-4

Chips from a foundry RF process are post-processed to release MEMS passivedevices and enable single-chip reconfigurable circuits. A MEMS variable capacitor, capable of 7:1 tuning ratio, reconfigures a narrow-band low-noise amplifier and a power amplifier over a 1 GHz frequency range. A suspended MEMS inductor, with > 50% improvement in Q, lowers amplifier power consumption.

3:15 PM BREAK

3:30 **Ultra-Low-Power Electronics for Non-Invasive Medical Monitoring (INVITED)**, Lorenzo Turicchia, Soumyajit Mandal, Maziar Tavakoli*, Leon Fay**, Vinith Misra^, Jose Bohorquez, William Sanchez and Rahul Sarpeshkar, Massachusetts Institute of Technology, Cambridge, MA, *Linear Technology Corporation, North Chelmsford, MA, **SRI International, Menlo Park, CA, ^Stanford University, Stanford, CA
6-5

Electronics for non-invasive medical monitoring promise low-cost, maintenance-free, and lightweight devices. We present results from six novelchips for reducing power consumption while retaining precision: We describe an electrocardiograph, a pulse oximeter, a phono cardiograph, a model of the heart,an RF-antenna-powered CMOS rectifier, and a battery-free platform for medical monitoring.

4:20 **High-Voltage Tolerant Stimulation Monitoring Circuit in Conventional CMOS Process**, Edward Lee, Alfred Mann Foundation, Santa Clarita, CA
6-6

A 6V 8-input stimulation monitoring circuit with high-voltage analog switches and rail-to-rail constant g_m opamp was implemented in a conventional 0.18µm CMOS process. The on-resistance for the switches was < 3.15kΩ and the variations on the opamp input g_m values were <2.9% with a current consumption of 20µA at 6V.

4:45 **Circuits Techniques and Microsystems Assembly for Intracortical Multichannel ENG Recording (INVITED)**, Benoit Gosselin and Mohamad Sawan, École Polytechnique de Montreal, Montreal, Canada
6-7

We present dedicated circuit techniques and strategies to design and assemble dense multi-channel microsystems intended for ENG recording. Efficient neural interfacing circuits are proposed and high-fidelity data reduction strategies are demonstrated. Also, an on-chip power management scheme based on automatic biopotential detection is suggested. The presented strategy is expected to improve power consumption in multi-channel ENG sensors by an order of magnitude. Low-power design techniques, ultra-low-power

neural signal processing circuits, and dedicated implementation strategies to achieve high integration density in multi-channel microsystems are also covered.

Session 7 - Gigabit Transceivers and Building Blocks

Monday Afternoon, September 14
Pine Ballroom

Chair: Jin Liu, University of Texas at Dallas
Co-Chair: Jim Buckwalter, University of California, San Diego

This session presents an emerging set of high-speed standards, low-power equalization circuits, new modulation and signaling schemes for serial links, and opto-electronic circuits in silicon.

1:30 **Introduction**

1:35 **Emerging Standards at ~10 Gbps for Wireline Communications and Associated Integrated Circuit Design and Validation (INVITED), Mike Li and Sergey Shumarayev, Altera Corporation, San Jose, CA**
7-1

We first review the signaling and jitter requirements for emerging high-speed wireline communication standards at ~10 Gbps, including CEI 11G, XLAUI/CAUI, XFI, and SFP+. We then present an FPGA transceiver architecture and subsystem/circuit blocks for clocking and timing generation, transmitter buffer, and receiver CDR and DFE, all designed and manufactured with 40-nm process node. Lastly, we present the signal/jitter transmitter output and receiver-tolerance measurement results at 10.3125 Gbps, with an ultra-low random jitter at ~550 fs.

2:25 **A 18mW 10Gbps Continuous-Time FIR Equalizer for Wired Line Data Communications in 0.12 μ m CMOS, Hao Liu, Jin Liu, Robert Payne*, Cy Cantrell and Mark Morgan*, University of Texas at Dallas, Dallas, TX, *Texas Instruments Incorporated, Dallas, TX**
7-2

This paper presents a 10Gbps continuous-time FIR receiver equalizer design with a $\frac{1}{4}$ symbol-period differential self-biased active inductor delay line in 0.12 μ m CMOS for wired line data communications. The proposed delay line, together with a proposed active inductor Cherry-Hooper transimpedance load at the FIR filter summing node, increases the equalizer speed, while reducing the equalizer power consumption to only 18mW. The prototype occupies 0.03mm² die area and measurement results show that the equalizer can compensate for 15dB channel loss at 5GHz for 10Gbps data transmission.

2:50 **A 1-mW 12-Gb/s Continuous-Time Adaptive Passive Equalizer in 90-nm CMOS, Dong Hun Shin, Ji Eun Jang, Frank O'Mahony* and C. Patrick Yue, University of California, Santa Barbara, CA, *Intel Corporation, Hillsboro, OR**
7-3

This paper presents a frequency-domain adaptive passive equalizer for high-speed receivers. A local control loop, without feedback from the final receiver output, is used to automatically adjust the gain compensation for different channel characteristics. As a result, the equalizer does not rely on the recovered clock signal. Implemented in a 90-nm digital CMOS process, the equalizer can provide up to 13 dB of gain compensation with 6 dB of tuning range while consuming 1 mW from a 1-V supply. The equalizer is able to open the data eye of a 12-Gb/s PRBS signal after a 72-inch RG-50 coaxial cable and an 8-inch FR-4 trace, whose attenuations at 6 GHz are 10.8 and 13 dB, respectively.

3:15 PM BREAK

3:30 **A 3x3.8Gb/s Four-Wire High Speed I/O Link Based On CDMA-Like Crosstalk Cancellation, Tzu-Chien Hsueh, Pin-En Su and Sudhakar Pamarti, University of California, Los Angeles, CA**
7-4

A signaling technique realizing three differential links over four wires is proposed. The technique uses Code Division Multiple Access (CDMA) principles to cancel the crosstalk between the links. A 3x3.8 Gb/s, 10-12 BER prototype IC built in 90nm CMOS is described and measurement results are presented.

3:55 **A 5Gbps 0.13 μ m CMOS Pilot-Based Clock and Data Recovery Scheme for High-Speed Links, Mahmoud Reza Ahmadi, Amir Amirkhany* and Ramesh Harjani, University of Minnesota, Minneapolis, MN, *Rambus Inc., Los Altos, CA**
7-5

A 5Gbps differential link fabricated in a 0.13 μ m IBM CMOS using a pilot-based clock and data recovery where a low-amplitude bit rate clock is added to the transmit signal. The designed CDR area is 0.171mm² and consumes 17.6mW. The recovered clock rms jitter is 1.6ps for a 5% transmitter overhead.

4:20 **A 10-Gbps CMOS Single Chip Optical Receiver with 2-D Meshed Spatially-Modulated Light Detector, Shih-Hao Huang and Wei-Zen Chen, National Chiao-Tung University, Hsinchu, Taiwan**
7-6

This paper presents a 10-Gbps optical receiver with monolithically integrated CMOS photo detector. A transimpedance amplifier with nested feedback and shunt-peaking is proposed for broad-band and high-gain operations. Incorporating a 2-D meshed spatially-modulated light detector, the optical receiver is capable of delivering 25-kohm transimpedance gain when driving 50-ohm output loads. The operating speed is improved by 3X over the prior art with the same technology. Implemented in a generic 180-nm CMOS technology, the chip size is 0.95 mm by 0.8 mm. This receiver core drains 118 mW from 1.8 V supply.

Session 8 - CMOS Scaling and Beyond

Monday Afternoon, September 14
Cedar Ballroom

Chair: Takamaro Kikkawa, Hiroshima University
Co-Chair: Jordan Lai, TSMC

This session of invited papers covers progress of CMOS scaling and key process technologies including lithography, copper interconnects, SOI CMOS transistors, and high mobility channel CMOS technologies

1:30 **Introduction**

1:35 **Progress and Outlook of Lithography for Semiconductor IC (INVITED)**, *Burn Lin and R.G. Liu, TSMC, Hsinchu, Taiwan*
8-1

Progress of lithography from the lensless type to lens-based systems using different kinds of photon and electron beams is reported here. The stages of lithography development with their physical principles are linked to the corresponding impacts to IC designers to help them understand the reasons they are more and more restricted. From this vantage point, we look at the prospects of the lithography systems that will handle patterning for 32-nm half pitch and beyond in feasibility and cost.

2:25 **Copper Interconnect Technology for the 32 nm Node and Beyond (INVITED)**, *Jeff Gambino, Fen Chen and John He, IBM Microelectronics, Essex Junction, VT*
8-2

Copper interconnects have gained wide acceptance in the microelectronics industry due to improved resistivity and reliability compared to Al interconnects. However, there are many challenges with implementation of Cu interconnects at the 32 nm node and beyond, including increased resistivity, integration with porous low-k materials, and reliability. In addition, for RF and mixed signal technology, integration of passive devices is required. In this paper, each of these topics is addressed.

3:15 PM BREAK

3:30 **Advanced SOI CMOS Transistor Technologies for High-Performance Microprocessor Applications (INVITED)**,
8-3 *Manfred Horstmann, Andy Wei, Jan hoentschel, Thomas Feudel, Thilo Scheiper, Rolf Stephan, Martin Gerhardt, Stephan Krügel and Michael Raab, GLOBALFOUNDRIES, Dresden, Germany*

In this paper we present an overview of partial depleted Silicon on Insulator (PD SOI) CMOS transistor technologies for high performance applications. To achieve a "high performance per watt" figure of merit, transistor technology elements like PD SOI, strained Si, aggressive junction scaling or asymmetric devices need hand-in-hand development with multiple core- and power efficient designs. These techniques have been developed, applied and optimized for 45nm SOI volume manufacturing at GLOBALFOUNDRIES in Dresden. To enable further transistor scaling to 32nm design rules, High K Metal Gate (HKMG) technology is key. Different HKMG integrations as well as future strained Si technologies like strained silicon directly bonded on SOI and embedded Si:C are discussed.

4:20 **High Mobility Channel CMOS Technologies for Realizing High Performance LSI's (INVITED)**, *Shinichi Takagi, The University of Tokyo, Tokyo, Japan*
8-4

Channel engineering including the high mobility channel has been recognized as mandatory for high performance CMOS. We report our approaches to further improvement of MOSFETs by using strained-Si, Ge, and III-V semiconductor channels on the Si CMOS platform with an emphasis on the combination of ultra-thin body and multi-gate structures.

Poster Session

Monday Evening, September 14
Cascade/Sierra Ballroom
5:00 pm – 7:00 pm

M-1 **Trimless Second Order Curvature Compensated Bandgap Reference using Diffusion Resistor**, *Ajay Kumar, Texas Instruments*

A trim-less second order curvature compensated bandgap reference current using diffusion resistor is presented. An order of magnitude higher sheet-resistance (x50) and tighter process control of diffusion resistor than the poly has enabled this work to achieve the same current in one-third area. The process spread of diffusion resistor and V_{PNP} transistor tracks each other, thereby resulting in higher accuracy without using any trim techniques. The proposed circuit is fabricated in a 0.5 μ m CMOS process. The measured reference current has a variation of 46ppm/oC over a temperature range of -55oC to 125oC.

M-2 **A 10mW 9.7ENOB 80MSPS Pipeline ADC in 65nm CMOS Process without any Special Mask Requirement and with Single 1.3V Supply**, *Abhijit Kumar Das, Hemant Bhasin, Sundara Siva Rao Giduturi, Texas Instruments, India*

This paper describes a power and area efficient pipeline ADC design. This ADC was designed in 65nm process without any special mask requirement and can work with supply voltage of 1.3V consuming 10mW providing 9.7 ENOB at 80MSPS while occupying less than 0.2 square millimeters.

- M-3 **A 1.5mW 16b ADC with Improved Segmentation and Centroiding Algorithms and Litho-Friendly Physical Design (LFD) Used in Space Telescope Imaging Applications**, L. Lewyn, M. Loose*
*SnowBush-Gennum, *Teledyne Imaging Sensors*
- This paper describes the 16b ADC ASIC replacing the survey camera image processor in the 2009 Hubble rescue mission. The ADC uses a combination of improved MSB-LSB segmentation, 3 centroiding algorithms and litho-friendly physical design (LFD) to achieve <0.4b DNL and <2.3b INL without requiring initial or background calibration.
- M-4 **An 11mW 100MHz 16X-OSR 64dB-SNDR Hybrid CT/DT $\Delta\Sigma$ ADC with Relaxed DEM Timing**, S. Kwon*, P. Hanumolu, S. Kim**, S. Lee**, S. You**, H. Park**, J. Kim**, and U. Moon, *Oregon State University, *Now with Dongbu HiTek, **Samsung Electronics*
- A multi-bit 3rd-order hybrid Delta-Sigma ADC is presented. The ADC obviates the need for a dynamic element matching technique (DEM) in the critical feedback path. Eliminating the DEM allows to minimize feedback latency, thus helping to increase clock frequency. The first two continuous-time integrators decrease power consumption and the last discrete-time integrator mitigates the excess loop delay and the quantizer sampling timing problem. Moreover, switched-R-MOSFET-C technique offers benefit of absorbing the finite opamp delay as well as frequency scalability. The proposed ADC is also capable of converting up to +2 dBFS without pole optimization technique. A prototype IC implemented in a 65 nm digital CMOS achieves 68 dB DR, 65 dB SNR, 64 dB SNDR, and 84 dB SFDR while consuming 11 mW and clocking at 100 MHz.
- M-5 **A 14.6th-order 3.456GHz Transmit Baseband filter in 110nm CMOS for Millimeter-Wave Communication Systems**, M. Tokumaru, H. Ikoma, Y. Yamada, K. Okamoto, A. Yamamoto, Y. Shirakawa, *Panasonic Corporation*
- This paper presents a 1.728Gbps transmit baseband filter for transmitters of millimeter-wave communication systems. In order to avoid the inter symbol interference, wide band and high order filter is demanded. The proposed filter consists of a 3.456GHz digital filter and an 8-bit 3.456Gbps digital to analog converter (DAC) with a clock divider, which occupies 0.265mm² in 110nm CMOS. The filter consumes 142mW and achieves the transmit spectrum very close to the mask regulated by IEEE802.15.3c.
- M-6 **64-bit Prefix Adders: Power-Efficient Topologies and Design Solutions**, Ching Zhou, Bruce M. Fleischer, Michael Gschwind, Ruchir Puri, IBM T.J. Watson Research Center
- 64-bit adders of various prefix algorithms are designed using a novel data flow synthesis methodology. The power-performance tradeoffs are analyzed for a portfolio of popular adder topologies and design styles. The intrinsically sparser designs in hierarchical prefix scheme are demonstrated to be preferable choices for both high-performance and low-power adder applications.
- M-7 **Energy-Performance Tunable Logic**, Bitu Nezamfar, Mark Horowitz, *Stanford University*
- An externally static, internally dynamic topology creates a new logic family that enables the user to tune effective transistor thresholds post-fabrication by adjusting a few power supplies. These gates can therefore be programmed for higher speed or for lower power based on the system requirements. An application of this logic to programmable interconnect circuits is shown in this paper. In a 90-nm test chip, the circuit achieves the same performance as conventional static circuits at 65% energy and has a 2X wider energy-performance tuning range. This property enables building in-field energy-performance tunable FPGAs.
- M-8 **A 6-bit Arbitrary Digital Noise Emulator in 65nm CMOS Technology**, Tetsuro Matsuno*, Daisuke Fujimoto*, Daisuke Kosaka**, Naoyuki Hamanishi***, Ken Tanabe***, Masazumi Shiochi***, Makoto Nagata* **, *Kobe University, **A-R-Tec Corporation, ***Toshiba Corporation
- An arbitrary noise generator (ANG) is based on time-series charging of divided parasitic capacitance (TSDPC) and emulates power supply noise generation in a CMOS digital circuit. A prototype ANG incorporates an array of 32 × 32 6-bit TSDPC cells along with a 128-word vector memory and occupies 2 × 2 mm² in a 65 nm 1.2 V CMOS technology. Digital noise emulation of functional logic cores such as register arrays and processing elements is demonstrated with chip-level waveform monitoring at power supply, ground, as well as substrate nodes.
- M-9 **A 0.92mm² 23.4mW Fully-Compliant CTC Decoder for WiMAX 802.16e Application**, Shao-Wei Yen, Ming-Chih Hu, Chih-Lung Chen, Hsie-Chia Chang, Shyh-Jye Jou, Chen-Yi Lee, *National Chiao Tung University*
- An area-efficient and fully-compliant decoder for convolutional turbo code (CTC) of WiMAX 802.16e is presented. The proposed decoder can support all 17 modes specified in IEEE 802.16e system. By scaling the extrinsic information, the Max-Log MAP algorithm is used to reduce the hardware complexity with the minimized performance loss. A two-phase extrinsic memory and reversed sliding window technique are demonstrated for less memory requirement and decoding latency. Moreover, a division-free reconfigurable interleaver architecture is proposed to use simple addition and subtraction instead of division. Fabricated with the 90nm cmos process, the proposed CTC decoder chip which occupies core area of 0.92mm² can achieve 30Mb/s with 23.4mW power consumption.
- M-10 **Embedded High-Speed BCH Decoder for New-Generation NOR Flash Memories**, Xueqiang Wang, Dong Wu, Chaohong Hu*, Liyang Pan, Runde Zhou, *Tsinghua University, *Intel Technology Development Co. Ltd*
- A high-speed double-error-correcting (DEC) BCH decoder for new-generation NOR flash memory is presented to improve reliability. To speed up the decoding process, a multiplication-free linear transform is developed to eliminate iterations and divisions in Galois fields. Furthermore, the reverse data-flow analysis (RDFA) and smoothest descent approach are proposed to reduce latency in the parallel Chien search. Based on peripheral 180nm CMOS process, the whole BCH decoder is designed and the latency is significantly reduced to less than 5ns.

- M-11 **A 56M Ω CMOS TIA for MEMS Applications**, *J. Salvia, P. Lajevardi, M. Hekmat, B. Murmann, Stanford University*
- We present a high-gain, low-noise differential transimpedance amplifier designed to interface with electrostatic micromechanical resonators. The capacitive feedback topology achieves a 56M Ω gain, 1.8MHz bandwidth, phase response near 0 degrees, and 65 fA/rootHz input-referred noise. It was fabricated in 0.18 μ m CMOS technology and dissipates 436 μ W from a 1.8V supply.
- M-12 **A 366kS/s 400uW 0.0013mm² Frequency-to-Digital Converter Based CMOS Temperature Sensor Utilizing Multiphase Clock**, *Kisoo Kim, Hokyoo Lee, Sangdon Jung, Chulwoo Kim, Korea University, Seoul, Korea*
- The proposed temperature sensor is based on CMOS ring oscillators and a frequency-to-digital converter capable of simple and efficient temperature conversion to digital value. The proposed temperature sensor consumes 400 μ W at a conversion rate of 366kS/s and performs the fastest temperature-to-digital conversion among those introduced in previous work. The whole block occupies 0.0066 mm² (0.0013 mm² for temperature sensor). Four multiphase clocks were utilized to enhance the resolution of the sensor 8 times better. After one point calibration, the chip-to-chip measurement spread was +2.748 $^{\circ}$ C ~ -2.899 $^{\circ}$ C over the temperature range of -40 $^{\circ}$ C to 110 $^{\circ}$ C.
- M-13 **Design-for-Manufacturing Features in Nanometer Logic Processes – A Reverse Engineering Perspective**, *Dick James, Chipworks Inc.*
- Recently we have seen the introduction of production disciplines known collectively as Design for Manufacturability (DFM), which are techniques used to co-optimize design, layout, and processing to reduce variability and improve manufacturing parameters. This paper illustrates some different layout features used for DFM in some recent 65-, and 45-nm products.
- M-14 **Quadratic Differential and Integration Technique in V² Control Buck Converter with Small ESR Capacitor**, *Shih-Jung Wang, Yu-Huei Lee, Yung-Chih Lai, Ke-Hong Chen, National Chiao Tung University, Hsinchu, Taiwan*
- This paper proposes a quadratic differential and integration (QDI) technique for the design of buck converters with small equivalent series resistance (ESR) of the output capacitor. The QDI circuit not only further removes the dependence of ESR in the V² control but also achieves a fast transient response with small load transient voltage variation. The experimental results show the output voltage can have voltage ripple about 30 mV and recovery time of 20 μ s in case of 300 mA load current variation.
- M-15 **Adaptive Performance Compensation with In-Situ Timing Error Prediction for Subthreshold Circuits**, *H. Fuketa, M. Hashimoto, Y. Mitsuyama, T. Onoye, Osaka University*
- This paper presents an adaptive technique for compensating manufacturing and environmental variability in subthreshold circuits using "canary Flip-Flop" that can predict timing errors. A 32-bit Kogge-Stone adder whose performance was controlled by body-biasing was fabricated in a 65 nm CMOS process. Measurement results show that the adaptive control can compensate PVT variations and improve energy-efficiency of subthreshold circuits significantly compared to worst-case design and operation with guardbanding.
- M-16 **A Full Chip Integrated Power and Substrate Noise Analysis Framework for Mixed-Signal SoC Design**, *D. Kosaka*,****, Y. Bando*, G. Yokomizo**, K. Tsuboi**, Y. S. Li***, S. Lin***, M. Nagata*, ****, *Kobe University, **STARC, ***Apache Design Solutions, Inc., ****A-R-Tec Corp.*
- A fully integrated framework of full-chip power and substrate noise analysis is discussed, featuring description of transistor-level custom circuits as dynamic noise sources, a high capacity solver for chip-level substrate coupling, and noise back annotation flow to transistors of sensitive circuits. Recursive evaluation of power current and operation timing under the presence of dynamic IR drop greatly improves the accuracy of analysis. A 90-nm CMOS chip was examined both by on-chip noise measurements and full-chip noise analysis.
- M-17 **An Accurate and Fast Behavioral Model for PLL Frequency Synthesizer Phase Noise/Spurs Prediction**, *Xiaozhou Yan, Xiaofei Kuang, Nanjian Wu, Chinese Academy of Sciences*
- This paper presents a behavior model for PLL Frequency Synthesizer. All the noise sources are modeled with noise voltages or currents in time-domain. An accurate VCO noise model is introduced, including both thermal noise and 1/f noise. The behavioral model can be co-simulated with transistor level circuits with fast speed and provides more accurate phase noise and spurs prediction. Comparison shows that simulation results match very well with measurement results.
- M-18 **Pathfinding for 22nm CMOS Designs using Predictive Technology Models**, *Xia Li, Wei Zhao, Yu Cao*, Zhi Zhu, Jooyoung Song, David Bang, Chi-Chao Wang*, Seung H. Kang, Joseph Wang, Matt Nowak, Nick Yu, Qualcomm Incorporated, *Arizona State University*
- Traditional IC scaling is difficult at the 22nm node. Dealing with these challenges increase product development cycle time. For continued CMOS scaling, it requires having Predictive Technology Models to start design explorations in new process nodes as early as possible. In this paper we propose a strategy that enables simultaneous investigation of advanced process and design concepts. We capture the heuristic device behavior during the scaling, make tradeoffs of circuit design for next technology node.
- M-19 **An SRAM Reliability Test Macro for Fully-Automated Statistical Measurements of V_{min} Degradation**, *Tae-Hyoung Kim, Wei Zhang, Chris H. Kim, University of Minnesota*
- An SRAM reliability test macro is designed in a 1.2V, 65nm CMOS process for statistical measurements of V_{min} degradation. An automated test program efficiently collects statistical V_{min} data and reduces test time. The proposed test

structure enables Vmin degradation measurements for different SRAM failure modes such as the SNM-limited case and the access-time-limited case. The impact of voltage stress on the time to cell data flip was measured.

- M-20 **A 60 GHz CMOS Balanced Downconversion Mixer with a Layout Efficient 90° Hybrid Coupler**, *R. E. Amaya, Cornelius J. Verver, Communications Research Centre, Ottawa, Canada.*

This paper presents the design and implementation of a downconversion mixer implemented in a standard 130nm commercial CMOS process and aimed at applications in the 60 GHz ISM band. A balanced mixer configuration was implemented by using a layout efficient 90° hybrid coupler which serves as a diplexer to inject the LO signal while also providing two outputs with 3dB of attenuation and 90° phase shift. The mixer achieves a conversion gain of +0.3 dB and OIP3 of +2.3 dBm. The mixer also consumes 200µA of DC current and 8mA of peak current while driven from a single 2V supply. The layout area including test pads is 1.4mm x 1.0mm.

- M-21 **A 0.46ps RJrms 5GHz Wideband LC PLL for Multi-Protocol 10Gb/s SerDes**, *C. Rao, A. Wang, S. Desai, Prism Circuits Inc.*

A 2.3 to 5GHz LC PLL is implemented in 65nm CMOS for 0.6 to 10Gb/s SerDes. The LC VCO has 67% coarse tuning range, 9.6% worst-case hold range. RJrms at TX output with a clock pattern is 460fs at 5GHz, 548fs at 3.125GHz. Total power dissipated is 29mW at 5GHz.

- M-22 **A 10MHz to 315MHz Cascaded Hybrid PLL with Piecewise Linear Calibrated TDC**, *Minyoung Song, Young-Ho Kwak, Sunghoon Ahn, Wooseok Kim*, ByeongHa Park* and Chulwoo Kim, Korea University, *Samsung Electronics*

An ADPLL with a piecewise linear calibrated hierarchical TDC is proposed to achieve a wide range of operation and a CPPLL is cascaded to filter out 1/f noise. A phase selectable divider is also proposed to divide the clock frequency while keeping the relative phase difference of output same as that of input. The cascaded hybrid PLL fabricated in 65nm CMOS process burns 17mW and occupies 0.4mm². The measured jitters are 1.1nspp and 223.6psrms, respectively with a multiplication factor of 1,024.

- M-23 **A 430MHz-2.15GHz Fractional-N Frequency Synthesizer for DVB and ABS-S Applications**, *P. Yu, Z. Gong, M. Gu, Y. Shi, F. Dai*, Suzhou-CAS Semiconductors Integrated Technology Research Center, *Auburn University*

The frequency synthesizer covers a very wide frequency range of 430MHz-2.15GHz while integrates only one on-chip inductor. The AFC helps to correct VCO sub-band selection when PVT varies. The LDO helps to suppress in-band and out-of-band noise generated by 3rd-order ΣΔ modulator. The fast setting time and low phase noise make the PLL suitable of numerous multi-band, multi-standard applications such as DVB and ABS-S

- M-24 **SiGe Digital Frequency Dividers with Reduced Residual Phase Noise**, *S. Horst, S. Phillips, H.M. Lavasani, F. Ayazi, J.D. Cressler, Georgia Institute of Technology*

A new design methodology for achieving very low residual phase noise in SiGe HBT digital frequency dividers is presented. A modified CML D latch design is proposed that enables the latch to draw more current, thereby reducing the residual phase noise. The latch modification yields a 10 dB phase noise improvement over a standard D latch topology, with measurements at 10 GHz resulting in a phase noise floor of -160 dBc/Hz. The circuit dissipates 350 mW of DC power, but a standard phase noise figure-of-merit that accounts for phase noise, DC power dissipation, and operating frequency, reveals that this new design is among the best in its class.

- M-25 **A 54-862 MHz CMOS Direct Conversion Transceiver for IEEE 802.22 Cognitive Radio Applications**, *Jongsik Kim, Seung Jun Lee, Seungsoo Kim, Jong Ok Ha, Junki Min*, Yun Seong Eo, Hyunchol Shin, Kwangwoon University, *Samsung Electro-Mechanics Co.*

A CMOS single-chip transceiver IC is developed for IEEE 802.22 cognitive radio applications. Over the 54 to 862 MHz ultra wideband, the in-band harmonic distortions of the transmitter and the unwanted harmonic mixing of the receiver are effectively suppressed by exploiting the dual-path direct-conversion architecture. A seamless coverage of the full band is achieved by employing a fractional-N PLL with a single LC VCO and a multi-modulus LO generator. Implemented in 0.18 µm CMOS, the receiver achieves 110 dB gain dynamic range, < 8.5 dB noise figure, and > -11 dBm IIP3 at the LNA bypass mode. The transmitter delivers -3 dBm output power with OP1dB and OIP3 greater than +6.4 dBm and +15.9 dBm, respectively. On-chip calibration circuits suppress the image and carrier leakage components below -41 dBc across the total band.

- M-26 **A 1.8V, Sub-mW, Over 100% Locking Range, Divide-by-3 and 7 Complementary-Injection-Locked 4 GHz Frequency Divider**, *Y.-C. Lo, H.-P. Chen, J. Silva-Martinez, S. Hoyos, Texas A&M University*

A low-power wideband divide-by-odd-ratio ring-oscillator-based complementary-injection-locked frequency divider that widens its locking range over 100% is proposed. The differential architecture's frequency locking range spans from 1.4-to-4.4 GHz with an input incident power of -4dBm. The power consumption of the 0.18µm CMOS topology is 0.9mW while locked at 4.7GHz.