Monday Afternoon Program

Session 6 – 3D and Photonic Interconnect

Monday Afternoon, September 19
Oak Ballroom

Chair: Arif Rahman, Altera
Co-Chair: Mike Li, Altera

This session covers the design, implementation, modeling and test of advanced interconnect technologies including 3D integrated circuits and photonics.

1:30 PM **Introduction**

1:35 PM
6-1 **Three Dimensional Integration – Considerations for Memory Applications (INVITED),** *S.S. Iyer, T. Kirihata, and J.E. Barth, IBM Systems and Technology Group*

This paper reviews the technology and design considerations for the implementation of 3 Dimensional integration of memory in a high performance logic environment.

2:25 PM
6-2 **DRAM-on-logic Stack — Calibrated Thermal and Mechanical Models Integrated into PathFinding Flow (INVITED),** *D. Milojevic, H. Oprins, J. Ryckaert, P. Marchal, G. Van der Plas, IMEC*

In this paper, we present thermal and mechanical characterization of a DRAM-on-logic stack. Our experimental data indicates that a holistic optimization of design and technology is needed to achieve working 3D stacks. Particularly, the stack organization and TSV/μbump layout must be fine-tuned together with the 3D technology for managing mechanical and thermal challenges. In order to support system designers, we propose hereto a dedicated thermal and mechanical model, integrated into the design flow. We also indicate the data required from foundries and OSATs to achieve good fidelity with measurement results.

3:15 PM **BREAK**

3:30 PM
6-3 **Test Challenges for 3D Integration (INVITED),** *W.R. Bottoms, 3MTS, Inc.*

4:20 PM
6-4 **CDM-ESD Induced Damage in Components using Stacked-Die Packaging,** *N. Olson, N. Jack, V. Shukla, E. Rosenbaum, University of Illinois at Urbana-Champaign*

CDM-ESD robustness of stacked-die packages is investigated and compared with single-die packages. The peak discharge current is not increased significantly by die stacking. The inter-die signal interfaces are shown to be well protected against CDM by placing just a small ESD protection clamp at the receiver, if certain package integration guidelines are followed.

4:45 PM
6-5 **Silicon Photonics for On-Chip Interconnections (INVITED),** *A. Mickelson, University of Colorado at Boulder*

The state of the art of silicon photonics for on-chip interconnections is reviewed from both historical and technological perspectives. Attention is placed on motivating why silicon photonics is the replacement for copper interconnection that offers the best possibility for future improvement in performance and reduction in power consumption. The broadcast interconnection effort being carried in the author's research group is discussed in light of the requirements of many-core interconnections.

Session 7 – High Speed Wireline and Optical Transceivers

Monday Afternoon, September 19
Fir Ballroom

Chair: Elad Alon, University of California, Berkeley
Co-Chair: Ed Van Tuijl, Axiom-IC Twente

With the increasing demand for high-speed wireline and optical transceivers, this session highlights advanced techniques to improve the power and performance of these designs.

1:30 PM **Introduction**

1:35 PM
7-1
A 19 mW/Lane SerDes Transceiver for SFI-5.1 Application, *Siavash Fallahi, Delong Cui, Deyi Pi, Rose Zhu, Greg Unruh, Marcel Lugthart, Afshin Momtaz, Broadcom Corporation*

A low-power, small-area transceiver PHY that supports SFI-5.1 is fabricated in standard 40 nm CMOS, supporting rates up to 50 Gb/s. The combined active core area of the receiver and transmitter occupies only 0.08 mm2 per lane. The RX can handle 0.65 UI plus 0.49 UI additional sinusoidal input jitter.

2:00 PM
7-2
A Monolithic 3.125 Gbps Fiber Optic Receiver Front-end for POF Applications in 65 nm CMOS, *Yunzhi Dong, Ken Martin, University of Toronto*

This paper describes the design of an analog receiver front-end targeting multi-gigabit data communications over large-core plastic optical fibers. A receiver front-end with an integrated photo detector has been implemented in a standard TSMC 65 nm low-power bulk-silicon CMOS process. A novel hybrid current buffer based transimpedance amplifier has been proposed to drive the 14 pF photo capacitance presented by the large-area photo detector to multi-gigahertz range. A digitally controlled slow-slope equalizer has also been integrated in the receiver front-end to compensate the high-frequency losses due to the integrated photo detector. The receiver front-end consumes 50 mW dc power from a 1.2 V supply (excluding output buffer) and achieves an NRZ data rate up to 3.125 Gbps.

2:25 PM
7-3
Addressing Link-Level Design Tradeoffs for Integrated Photonic Interconnects, *M. Georgas, J. Leu, B. Moss, C. Sun, V. Stojanovic, Massachusetts Institute of Technology*

Integrated photonic interconnects have emerged recently as a potential solution for relieving on-chip and chip-to-chip bandwidth bottlenecks for next-generation many-core processors. To help bridge the gap between device and circuit/system designers, and aid in understanding of inherent photonic link tradeoffs, we present a set of link component models for performing interconnect design-space exploration connected to the underlying device and circuit technology. To compensate for process and thermal-induced ring resonator mismatches, we take advantage of device and circuit characteristics to propose an efficient ring tuning solution. Finally, we perform optimization of a wavelength-division-multiplexed link, demonstrating the link-level interactions between components in achieving the optimal degree of parallelism and energy-efficiency.

3:15 PM **BREAK**

3:30 PM
7-4
A 7.4 Gb/s Forwarded Clock Receiver Based on First-Harmonic Injection-Locked Oscillator Using AC Coupled Clock Multiplication Unit in 0.13µm CMOS, *Young-Ju Kim, Sang-Hye Chung,Lee-Sup Kim, KAIST*

This paper presents a forwarded clock receiver based on an injection-locked oscillator (ILO) with a simple clock multiplication unit to reduce the clock jitter and power consumption. The clock multiplication unit employs AC coupling and superposition technique to generate first-harmonic pulses. The first-harmonic injection reduces the rms and peak to peak jitter of the ILO output clock by about 0.65ps (29%) and 46.06ps (65%), respectively. The measured power efficiency of the receiver is 1.69mW/Gbps at 7.4Gb/s data rate in a 1.2V 0.13μm CMOS process.

3:55 PM
7-5

Low-Power 8Gb/s Near-Threshold Serial Link Receivers Using Super-Harmonic Injection Locking in 65nm CMOS, *Kangmin Hu, Tao Jiang, Sam Palermo*, Patrick Yin Chiang, Oregon State University, *Texas A&M University*

A testchip of 8Gb/s forwarded clock serial link receivers is presented. The receiver exploits a novel low-power super-harmonic injection-locked ring oscillator for symmetric multi-phase local clock generation and dekewing. Further power reduction is achieved by designing most the receiver circuits in the near-threshold region of 0.6V supply, with the exception of only the global clock buffer, test buffers and synthesized digital circuits at nominal 1V supply. At architectural level, 1:10 direct demultiplexing rate is chosen as a demonstration of achieving low supply operation by high-parallelism design. Fabricated in 65nm CMOS technology, two receiver prototypes are integrated in this testchip, one without and the other with front S/Hs. Including the amortized power of global clock distribution, they consume 1.3mW and 2mW respectively at 8Gb/s input data rate, which achieve the power efficiency of 0.163mW/Gb/s and 0.25mW/Gb/s. Measurement results show both receivers get BER < 10e-12 across a 20-cm FR4 PCB channel.

4:20 PM
7-6

A 16-Gb/s Backplane Transceiver with 12-Tap Current Integrating DFE and Dynamic Adaptation of Voltage Offset and Timing Drifts in 45-nm SOI CMOS Technology, *G. R. Gangasani, C. Hsu, J. F. Bulzacchelli*, S. Rylov*, T. Beukema*, D. Freitas, W. Kelly, M. Shannon, J. Qi, H. H. Xu, J. Natonio, T. Rasmus, J. Guo, M. Wielgos, J. Garlett, M. A. Sorna, M. Meghelli, IBM Systems and Technology Group, *IBM T. J. Watson Research Center*

This paper presents a 16-Gb/s 45-nm SOI CMOS transceiver for multi-standard backplane applications. The receiver uses a 12-tap DFE with circuit refinements for supporting higher data rates. Both the receiver and the transmitter use dynamic adaptation to combat parameter drift due to changing supply and temperature. A 3-tap FFE is included in the source-series-terminated driver. The combination of DFE and FFE permits error-free NRZ signaling at 16-Gb/s over channels exceeding 30dB loss. The 8-port core with two PLLs is fully characterized for 16GFC and consumes 385mW/link.

4:45 PM
7-7

Power-Efficient I/O Design Considerations for High-Bandwidth Applications (INVITED), *J. Eble, S. Best, B. Leibowitz, L. Luo, R. Palmer, J. Wilson, J. Zerbe, A. Amirkhany, N. Nguyen, Rambus Inc.*

Power-efficiency results from several generations of I/O interfaces with specific goals are presented as well as the tradeoffs made within and across those designs. Foundational work in active-power reduction at a single rate for a symmetric system, the subsequent application of that work to a burst-mode asymmetric interface, and recent research on low-overhead bursting are discussed. Dynamic voltage frequency scaling and efficiency increases enabled by system level interconnect improvements are also considered as important techniques.

Session 8 – Sensors and Biosystems

Monday Afternoon, September 19
Pine Ballroom

Chair: Farrokh Ayazi, Georgia Institute of Technology
Co-Chair: Ada Poon, Stanford University

This session presents works that push the limits and review the state of the art of general sensors, biosensors and circuits for biomedical applications.

1:30 PM **Introduction**

1:35 PM 8-1 **Thermal Diffusivity Sensing: A New Temperature Sensing Paradigm (INVITED),** *C.P.L. van Vroonhoven and K.A.A. Makinwa, Delft University of Technology*

This paper describes temperature sensors based on the well-defined thermal diffusivity of IC-grade silicon, which have low untrimmed inaccuracy (±0.2°C 3σ) and operate over a wide temperature range. Their near-linear digital output is insensitive to process spread and packaging stress, and their performance strongly benefits from process scaling.

2:00 PM 8-2 **A Self-Clocked ASIC Interface for MEMS Gyroscope with 1m˚/s/√Hz Noise Floor,** *A. Elsayed, A. Elshennawy, A. Elmallah, A. Shaban, B. George, M. Elmala, A. Ismail, A. Wassal, M. Sakr, A. Mokhtar, M. Hafez, A. Hamed, M. Saeed, M. Samir, M. Hammad, M. Elkhouly, A. Kamal, M. Rabieah*, A. Elghufaili*, S. Shaibani*, I. Hakami*, T. Alana, Si-Ware Systems, *King Abdulaziz City for Science and Technology*

An interface for MEMS gyroscope is implemented in 0.18μm HVCMOS and achieves noise floor of 1m deg/sec/sqrt(Hz) over 200Hz BW. Electromechanical sigma-delta force-feedback and self-clocking scheme based on gyro resonance are implemented. The interface includes on-chip reference generation, decimation, and temperature compensation.

2:25 PM 8-3 **A 20μW Contact Impedance Sensor for Wireless Body-Area-Network Transceiver,** *Kiseok Song, Joonsung Bae, Long Yan, Hoi-Jun Yoo, KAIST*

A low power contact impedance sensor (CIS) is presented for an energy efficient wireless body-area-network (WBAN) transceiver using a human body as a transmission medium. The proposed CIS adopts the capacitive sensing technique based on the LC resonance for detecting the parasitic capacitance between the electrodes and the human body to automatically turn on or off the transceiver. The 3'b resistive sensor, combined with a reconfigurable output driver in the transmitter, is proposed to compensate the channel quality degradation due to the contact impedance variation. It can reduce both the linearity and sensitivity requirements of the receiver front-end by 7 dB. It leads to significantly reduce the power of the LNA more than 70 % (from 2.0 mW to 0.6 mW). The proposed CIS of 1.0 mm X 1.4 mm is fabricated in 0.18 um CMOS technology, and dissipates only 20 uW from 1.0 V.

2:50 PM 8-4 **256-site Active Neural Probe and 64-channel Responsive Cortical Stimulator,** *R. Shulyzki, K. Abdelhalim, A. Bagheri, C. M. Florez, P. L. Carlen, R. Genov, University of Toronto*

The 0.35um CMOS active probe and stimulator enables responsive neural stimulation of the brain cortex. It monitors extracellular neural activity on 256 sites in the brain and generates 64 event-triggered current-mode neural stimuli. Each 0.035mm2 fully differential neural recording channel includes a 8-bit single slope ADC. Each 0.02mm2 neural stimulation channel reuses an OTA for both current sampling and current sourcing. The 13.5mW prototype is flip-chip bonded with a 64- shank Utah electrode array and validated in spatial recording of epileptic neural activity in the mouse hippocampus.

3:15 PM **BREAK**

3:30 PM 8-5 **Power Management Subsystem with Bi-directional DC to DC Converter for μ-Power Biomedical Applications,** *Raymond E. Barnett, Ganesh K. Balachandran* ,Texas Instruments, *Robert Bosch Research & Technology Center*

This paper presents a power management subsystem embedded in a biomedical wireless sensor SoC. A bi-directional capacitor only DC/DC converter, optimized for loads to 60uW, allows high efficiency operation using 1 to 3V batteries. The circuit is fabricated in a 0.35um BCD technology and occupies an area of 1.125 mm2.

3:55 PM
8-6
A Capacitor-Based AC-DC Step-Up Converter for Biomedical Implants, *Edward Lee, Alfred Mann Foundation*

An AC-DC step-up converter architecture for generating multiple compliance voltages (CVs) in an inductive powered biomedical implant is proposed. Switches and active rectifiers are used inside the converter for charging capacitors from the AC input and delivering currents to the loads. Regulated CVs with high power efficiency are obtained by controlling the on/off times of the switches using feedback loops. For a 1MHz, 2.3V peak AC input, a power efficiency of 92.9% for a combined load power of 12.3mW on 4 CVs (□3V and □3.6V) was achieved in a 0.18µm CMOS process.

4:20 PM
8-7
Fully Integrated Power-Efficient AC-to-DC Converter Design in Inductively-Powered Biomedical Applications (INVITED), *Hyung-Min Lee, Maysam Ghovanloo, Georgia Institute of Technology*

Limitations for achieving high power conversion efficiency (PCE) in integrated AC-to-DC converters have been reviewed for applications such as implantable microelectronic devices. We have presented a fully integrated active voltage doubler with offset-controlled high-speed comparators, which can convert 1.72V peak AC input at 13.56MHz to 2.4V DC across a 1kΩ load, with 78% PCE.

4:45 PM
8-8
Noise and Bandwidth Performance of Single-Molecule Biosensors (INVITED), *J. Rosenstein, S. Sorgenfrei, K. L. Shepard, Columbia University*

Single-molecule biosensors can reveal dynamics unavailable to ensemble measurements. Common fluorescence techniques are highly specific but fundamentally limited by the number of photons that can be collected. Here, we discuss the performance of new direct electronic sensors and their potential for sensing single-molecule processes on shorter timescales.

Session 9 (Forum 1) – Energy Management: From Datacenter to Handhelds

Monday Afternoon, September 19
Cedar Ballroom

Chair: Hasnain Lakdawala, Intel Labs

This forum explores energy consumption issues in computing, that have become an area of great concern. Power consumption in the datacenters that drive the cloud computing revolution is an increasing proportion of our energy consumption, and must be addressed in our energy future. On the client side, the need for pervasive portable computing and consequent need for battery life drives energy efficiency.

1:35 pm
9-1
Energy Efficient Computing In Large Scale Systems, *Tajana Rosing, University of California, San Diego*

An overview of the approaches we have developed to significantly lower the energy consumption in computing systems will be presented in this talk. We have derived optimal power management strategies for stationary workloads. Run-time adaptation can be done via an online learning algorithm that selects among a set of policies. We have generalized the algorithm to include thermal management since we found that minimizing the power consumption does not necessarily reduce the overall energy costs. To reduce the performance costs typically associated with state of the art thermal management techniques, we developed a new set of proactive management policies.

2:25 pm
9 -2

Energy Efficient Designs with Wide Dynamic Range, *Vivek De, Intel Corporation*

We must span a wide range of power/performance across diverse computing engines and workloads with the fewest distinct designs while providing maximum energy efficiency through aggressive voltage scalability. The designs must achieve near-threshold-voltage (NTV) operation while supporting a wide voltage-frequency operating range with minimal die area impact, while overcoming challenges posed by process scaling. The talk will present some solutions and research results from proof of concept prototypes.

3:15 pm
9-3

Advances and Challenges of Computing with FPGAs, John Wawrzynek, University of California, Berkeley

The primary challenges in reconfigurable computing relate to ease of use. The usual approach to mapping an application for execution on an FPGA has been equivalent to laborious RTL design. The research presented in this talk will highlight our experimentation with techniques for improving the ease of use of reconfigurable devices on a variety of fronts and for a wide range of computing tasks. This research has been driven by a few major application areas, including tasks in computer system simulation and a set of compute intensive tasks drawn from signal processing in radio astronomy and data-processing in systems biology.

4:45 pm
9-4

High-Efficient Dc-Dc Converter Design, Philip K T Mok, Hong Kong University of Science and Technology

DC-DC converters are a critical component of a system level power management solution to allow efficient energy conversion demanded by computing in scaled processes. In this talk I will talk about fast transient DC-DC converters that enable dynamic voltage frequency scaling (DVFS) in low power microprocessors. Challenges in the design of high efficiency DC-DC converters will also be discussed.

Poster Session

Monday Evening, September 19
Cascade/Sierra Ballroom
5:00 pm – 7:00 pm

M-1 **A Discrete-Time Charge-Domain Filter with Bandwidth Calibration for LTE Application,** *Ming-Feng Huang, Industrial Technology Research Institute*

A discrete-time charge-domain filter (CDF) with bandwidth calibration was proposed for LTE application. The CDF, based on feedback gain and delay, could suppress sinc distortion to achieve a like brick-wall filtering. The measurement showed that CDF performed a >59dB adjacent-channel rejection, >85dB stop-band attenuation, and 5-to-26 MHz reconfigurable bandwidth.

M-2 **A True Single SoC for UHF Mobile RFID Reader,** *J. Kim, S. Yun, W. Oh, M. Kil, S. Cho, PHYCHIPS Inc.*

A true single SoC for UHF Mobile RFID Reader has been implemented in a 0.18μm embedded flash CMOS technology. The SoC includes 900MHz RF transceiver, PA,MODEM, MCU, memory and peripherals with fully compliant ISO/IEC 18000-6C and EPC Global Class1 Gen2 reader protocol.

M-3 **An 80% Peak Efficiency, 410mW, Single Supply Rail Powered Class-I Linear Audio Amplifier,** *Z. Peng, S. Yang, Y. Feng, Z. Hong, B. Liu*, Fudan University, *Analog Devices*

A high efficiency high linearity Class-I audio amplifier is presented. Efficiency is improved by adopting a self-generated adaptive supply. The employed gain compression technique uses only one positive supply to maintain good linearity, and achieve above 20% better efficiency over a conventional Class-AB design.

M-4 **Band-gap Circuit Design Challenges in High-performance 32-nm Technology,** *J. Buller, J. Fletcher, S. Meyers, M. Robinson*, F. Tamayo, A. Prakash, D. Cabler, Advanced Micro Devices, *Vidatronic*

32-nm complementary metal oxide semiconductor (CMOS) silicon-on-insulator (SOI) with metal gate high-k (MGHK) offers high performance and low power for microprocessors. However, these advanced technologies come with challenges for analog design. Many of the stressor performance elements can adversely impact analog circuit behavior. For example, band-gap circuits, used ubiquitously in voltage references, are one such challenging component. We investigated both design and process methods that resulted in robust band-gap voltage and temperature response characteristics without impacting performance elements for microprocessor frequency.

M-5 **Low Power and Error Resilient PN Code Acquisition Filter via Statistical Error Compensation,** *E. Kim, D. Baker, S. Narayanan, D. Jones, N. Shanbhag, University of Illinois at Urbana Champaign*

We present a 256-tap PN code acquisition filter in an 180nm CMOS process employing statistical system-level error compensation. Under voltage overscaling (VOS), near constant detection probability Pdet above 90% with 5.8x reduction in energy is achieved at a supply voltage 27% below the point of first failure (PoFF) with an error rate pe of 0.868. This is an improvement of 5.8x in energy-efficiency over conventional error free designs and 3.79x in energy-efficiency and 2170x in error tolerance over existing error tolerant designs.

M-6 **0.4V SRAM with Bit Line Swing Suppression Charge Share Hierarchical Bit Line Scheme,** *S. Moriwaki, A. Kawasumi, T. Suzuki, T. Sakurai*, S. Miyano,Semiconductor Technology Academic Reserch Center, *The University of Tokyo*

128kbit SRAM with charge share hierarchical bit line scheme has been fabricated in 65nm foundry technology. By transferring the data between local bit lines and global bit lines with charge sharing, the variation of bit line swing which causes wasted power consumption in low voltage operation has been suppressed. 3.3μw/MHz of power consumption at 0.4V is achieved.

M-7 **An Output Structure for a Bi-Modal 6.4-Gbps GDDR5 and 2.4-Gbps DDR3 Compatible Memory Interface,** *Navin K. Mishra, Manish Jain, Phuong Le*, Sanku Mukherjee*, Arul Sendhil, Amir Amirkhany*, Rambus Chip Technologies, *Rambus Inc.*

A bi-modal x32 memory interface supports 6.4-Gbps GDDR5 signaling as well as 2.4-Gbps DDR3 signaling with a 1.5V IO supply. The interface incorporates a novel driver and pre-driver structure that supports one-tap equalization and presents very small capacitive loading to the pins. The entire interface, including both data and request channels achieves 11.6mW/Gbps and 27.7mW/Gbps energy efficiencies in GDDR5 and DDR3 modes respectively, and communicates successfully with 1.6-Gbps DDR3 and 6.0-Gbps GDDR5 DRAMs.

M-8 **A CMOS Image Sensor with on-chip Motion Detection and Object Localization,** *B. Zhao, X.*

Zhang, S. Chen, Nanyang Technological Univeristy

This paper presents a CMOS image sensor with on-chip moving objects detection and localization. The sensor generates motion events by frame differencing. An on-chip localization unit processes the events on the fly and localizes moving objects in the scene. The sensor can switched to ROI mode and shoot a zoomed picture of the object. It has been fabricated using UMC 0.18 um CMOS process, power consumption was measured to only 0.4 mW at 100 FPS.

M-9 **Ultra Low-FOM High-Precision ΔΣ Modulators with Fully-Clocked SO and Zero Static Power Quantizers,** *Jian Xu, Xiaobo Wu, Menglian Zhao, Rui Fan, Hanqing Wang, Xiaofen Ma, Bill Liu*, Zhejiang University, *Analog Devices*

Two high-precision MBSO-based Delta-Sigma modulators with ultra low FOM (< 45fJ/conv.-step) are implemented in 0.18μm CMOS. To save 50% power, both modulators adopt novel fully-clocked SOs with new bias circuits. Modulator-I for bio-medical applications uses high density MOSCAPs and innovative area-efficient static power-less quantizer to achieve 85dB peak-SNDR over 10kHz BW and only 13μW at 1.0V supply. Modulator-II for audio applications employs another novel static power-less quantizer and duty cycle shift DWA to achieve 92dB peak-SNDR over 25kHz BW and only 58μW at 0.9V supply.

M-10 **A New CMOS Image Sensor Readout Structure for 3D Integrated Imagers,** *Shang-Fu Yeh, Jin-Yi Lin, Chih-Cheng Hsieh, Ka-Yi Yeh* and Chung-Chi Jim Li*, National Tsing Hua, Taiwan *Industrial Technology Research Institute*

This paper presents a new CMOS image sensor (CIS) structure and ADC design for three-dimensional (3D) integrated imagers. The proposed CIS structure achieves a high spatial resolution without degrading the frame rate. A prototype chip shows that the array is expandable by modular sub-array design and is expected to achieve 100fps at multi-mega imaging for high-speed HDTV camera applications.

M-11 **All-Digital 3-50 GHz Ultra-Wideband Pulse Generator for Short-Range Wireless Interconnect in 40nm CMOS,** *C. Hu, P. Chiang*, Marvell Technology, *Oregon State University*

A reconfigurable, 3-50GHz all-digital impulse generator for short-distance wireless communications is designed in 40nm-CMOS. Digital back-gate biasing is used for raised-cosine envelope pulse-shaping to achieve better spectral-mask efficiency. Pulse duration, duty-cycle, and operating frequency are digitally programmable, in order to satisfy multi-band standards compatibility. An asymmetric inverter design within the Mono-Pulse-Generator (MPG) eliminates undesired glitches for the complementary clock edge. Occupying 350umx260um die area, the proposed impulse transmitter achieves a maximum data-rate of 3Gbps and an energy-efficiency of 0.5pJ/pulse for a 25GHz carrier frequency.

M-12 **A 4GS/s, 8.45 ENOB and 5.7fJ/Conversion, Digital Assisted, Sampling System in 45nm CMOS SOI,** *M.A.T. Sanduleanu, S. Reynolds, J.O. Plouchart, IBM T.J. Watson Research Center*

A 4GS/s sampling system achieved 8.45-ENOB linearity with 5.7fJ/conversion energy efficiency. The measured IIP3 and IIP2 are 17.7dBm and 40dBm respectively. The ENOB of the sampler shows no degradation up to Nyquist frequency. Realized in a 45nm SOI CMOS the active area of the sampler is only 0.2 x 0.2mm^2.

M-13 **Energy-Efficient Transceiver Circuits for Short-Range On-chip Interconnects,** *J. Postman, P. Chiang, Oregon State University*

Transceiver blocks for low-swing signaling across short on-chip wires are proposed. First, a charge-sharing transmitter enables adjustable swing signaling from a single supply voltage. Compact sense-amplifier offset correction is introduced that enables improved sensitivity without increasing energy/conversion. Finally, digital hysteresis tuning is used to implement compact decision feedback equalization. Optimized for low-energy applications and operating from Vdd = 0.2-1.0V, measurements show energy efficiencies of 4.0-136fJ/bit/mm across 1mm and 4mm wires in 65nm-CMOS.

M-14 **A Novel Audio Playback Chip Using Digitally Driven Speaker Architecture with 80%@-10dBFS Power Efficiency, 5.5W@3.3V Supply and 100dB SNR,** *Michitaka Yoshino, Mitsuhiro Iwaide, Daigo Kuniyoshi, Hajime Ohtani, Akira Yasuda, Jun-ichi Okamura*, Hosei University, *Trigence Semiconductor*

A novel audio playback chip using digitally driven speaker architecture based on a delta-sigma modulator and newly proposed high-order mismatch shaper with novel dither circuit is presented. It can realize 5.5W output power into 4Ω speakers with only 3.3V power supply. The power efficiency from -10dBFS to 0dBFS is higher than 80%. The efficiency at low power output can realize long battery life. This chip can realize battery powered high-fidelity and high-power audio system.

M-15 **32-nm SOI Programmable, High-bandwidth 8.0-GHz Digital PLL,** *Sanjeev K Maheshwari, Emerson Fang, Sanjeev Aggarwal, AMD, Inc.*

A digital phase-locked loop to filter clock jitter in source-synchronous serial link applications is presented. The PLL achieves bandwidth programmability from 20 to 300 MHz while allowing for a maximum input frequency of 4 GHz. An improved resolution bang-bang phase detector and a double-regulated, supply-insensitive VCO mitigate extreme noise environments.

M-16 **A 38.6nV/Hz$^{0.5}$ -59.6dB THD Dual-Band Micro-Electrode Array Signal Acquisition IC,** *Jing Guo, Jiageng Huang, Jie Yuan, Jessica Ka-Yan Law, Chi-Kong Yeung*, Mansun Chan, Hong Kong University of Science and Technology, *Chinese University of Hong Kong*

This paper reports the novel design of a dual-band monolithic MEA signal acquisition IC in a 0.35um CMOS process. It achieves low noise (0.9uVrms for LFP signal, 3.9uVrms for SP signal) and good linearity (-59.4dB THD for 20mVpp signal). Other performance also compares favorably against major bio-potential acquisition benchmark designs.

M-17 **Analysis and Modeling of On-Chip Power Combiners and their losses in LINC Transmitters,** *A. Koukab, O.T. Amir, Swiss Federal Institute of Technology in Lausanne*

This paper presents a compact model for LINC (linear amplification with non linear components) transmitters an their power combiners. The study focuses on the detrimental effect of the transmission line nonidealities. A mathematical description of the system that considers these nonidealities is proposed. The developed analytical expressions can be used to optimize, analyze and build pre-distortion algorithms for this family of transmitters. The efficiency and linearity are reexamined in light of the new analytical expressions of the model.

M-18 **Programmable Phase/Frequency Generator for System Debug and Diagnosis Using The IEEE 1149.1 Test Bus,** *T.-Y. Tsai, G. Roberts, McGill University*

A method of analog signal generation is presented that is suitable for digital test methodologies such as the IEEE 1149.1 test standard; it can be used to produce phase and frequency signals for system test debug and diagnosis. A 0.13um chip at 4 GHz illustrates the signaling capabilities of this generator.

M-19 **Overlapped Inductors and Its Application on a Shared RF Front-end in a MultiStandard IC,** *L. Feng, R. Sadhwani, Y. Peperovits, C. D. Hull, J. C. Jensen, Intel Corporation*

A technique to build overlapped inductors at the same location while keeping good isolation between them is presented. The key idea is to use magnetic and electric cancellation to reduce coupling. A shared LNA for WiFi and Bluetooth (BT) applications using the overlapped inductor is proposed. It enables independent gain control up to the first RF stage in a receiver so that the system integration complexity is reduced.

M-20 **A 1.0V 45nm Nonvolatile Magnetic Latch Design and Its Robustness Analysis,** *Peiyuan Wang, Xiang Chen, Yiran Chen, Hai (Helen) Li*, Seung Kang**, Xiaochun Zhu**, Wenqing Wu**, University of Pittsburgh, *Polytechnic Institute of New York University, **Qualcomm Inc.*

A new nonvolatile latch design is proposed based on the magnetic tunneling junction (MTJ) devices. In the standby mode, the latched data can be retained in the MTJs without consuming any power. Two types of operation errors, namely, persistent and non-persistent errors, are quantitatively analyzed by including the process variations and thermal fluctuations during the read and write operations. A design at 45nm technology node is used as the example to discuss the design tradeoffs.

M-21 **A 1V 13mW Frequency-Translating ΔΣ ADC with 55dB SNDR for a 4MHz Band at 225MHz,** *P. M. Chopp, A. A. Hamoui, McGill University*

A frequency-translating delta-sigma ADC is fabricated in 1V 65nm CMOS. It uses single-path mixing inside its feedback loop to down-convert a 4MHz band from 225MHz (IF1) to 25MHz (IF2), achieving 55dB SNDR. Low power (13mW) is realized by sampling below IF1, and by noise-shaping at IF2.

M-22 **CMOS Field-Modulated Color Sensor,** *D. Ho, G. Gulak, R. Genov, University of Toronto*

A digital photosensor for multi-color imaging is presented. By modulating the electric field applied to the photo sensing region, the sensor reports light intensity at discrete wavelengths. It utilizes standard CMOS technology, integrating a spectrally-sensitive photodiode and a current-to-frequency analog-to-digital converter on the same die.