Technical Sessions
Monday, September 20 - Afternoon

Session 6 – Analog Technologies

Monday Afternoon, September 20
Oak Ballroom

Chair: Eric Naviasky, Cadence
Co-Chari: Ken Suyama, Epoch Microelectronics

This session is a potpourri of analog techniques spanning from asynchronous data acquisition and class D amplification to filters for RF applications, ring oscillators and PLL's and a novel TDC.

1:30 **Introduction**

1:35
06-1
Event-Driven Data Acquisition and Continuous-Time Digital Signal Processing (INVITED), *Yannis Tsividis, Columbia University*

This paper reviews research in event-driven data acquisition and associated digital signal processing. The approaches considered can potentially offer significant energy and bandwidth savings with certain important classes of signals, in which activity varies significantly with time. An extensive bibliography is provided.

2:25
06-2
A Self-Oscillating Class D Audio Amplifier with 0.0012% THD+N and 116.5 dB Dynamic Range, *Jingxue Lu, Ranjit Gharpurey, University of Texas at Austin*

A low distortion third-order self-oscillating class D audio amplifier is integrated in a 0.7-um CMOS process. It can deliver 1.4 W into an 8 ohm load with 5 V power supply. The presented amplifier eliminates the requirement for a high quality carrier. It achieves a dynamic range (DR) of 116.5 dB, and a peak THD+N of 0.0012% for a 1 kHz sinusoidal input. The efficiency is 84.5%. The area of the amplifier is 6 mm^2.

2:50
06-3
Dynamic Push-Pull Operational Amplifier for AMLCD Common Voltage Driver Using Minimum Current Limiting Circuit, *Seungchul Jung, Young-Jin Woo, Tae-Kyu Nam*, Jin-Yong Jeon, Gyu-Ha Cho**, Gyu-Hyeong Cho, KAIST, *Silicon Works, **JDA Technology*

This paper reports a Class AB output stage based on a complementary common source with a minimum current limiting circuit. The non-active transistor in the output stage remains slightly turned on to react immediately for the opposite operation. The quiescent current of the output stage is defined by the proposed minimum current limiting circuit. This operational amplifier is designed for an AMLCD common voltage driver and fabricated by MagnaChip 18V 0.35µm CMOS process. The operation range of the supply voltage is from 5V to 16V and the total quiescent current is independent of temperature variation from -40ºC to 120ºC. On a single 8V supply, the operational amplifier has 1.37mA quiescent current including the bias generation block. The offset voltage is measured from -3.2mV to 5.4mV for 80 samples. The maximum transient current capacity is measured 200mA. The bandwidth is 15MHz with 62º phase margin and the slew-rate is measured 29.9V/µs (rising) and 45.0V/µs (falling).

3:15 **BREAK**

3:30
06-4
A 5.8-mW, 20-MHz, 4th-Order Programmable Elliptic Filter Achieving Over -80-dB IM3, *Peiyuan Wan, Yun Chiu, Pingfen Lin*, University of Illinois at Urbana-Champaign, *Beijing*

University of Technology

Frequency compensation of an active-RC elliptic filter is enabled for the first time by employing a derivative-free architecture. In conjunction with a built-in automatic unity-gain bandwidth tracking scheme, the prototype 4th-order active-RC elliptic low-pass filter (LPF) measures a digitally programmable bandwidth of 14-23MHz, a two-tone IM3 at 6MHz consistently better than -80dB with a full-scale input of over 800mVpp, a 1-dB in-band ripple and 45-dB stop-band rejection, all across wide temperature and voltage ranges. The LPF dissipates 5.8mW from a 1.2-V supply and occupies 0.1mm^2 in 0.13-um CMOS.

3:55
06-5

A Low-Noise Analog Baseband in 65nm CMOS, *Hassan Elwan, Ahmet Tekin*, Kenneth Pedrotti*, Newport Media Inc., * University of California, Santa Cruz*

In this paper, a universal receiver baseband approach is introduced. The chain includes a post-mixer noise shaping blocker pre-filter, a programmable-gain post mixer amplifier (PMA) with blocker suppression, a differential ramp-based linear-in-dB variable gain amplifier and a Sallen-Key output buffer. The 1.2-V chain is implemented in a 65-nm CMOS process, occupying a die area of 0.45 mm^2. While the device can be tuned across a bandwidth of 700-KHz to 5.2-MHz with 20 KHz resolution, it is tested for two distinct mobile-TV applications; Integrated Services Digital Broadcasting-Terrestrial ISDB-T (3-Segment fc=700 KHz) and Digital Video Broadcasting-Terrestrial/Handheld (DVB-T/H fc=3.8 MHz).

4:20
06-6

A 1.6mW 1.6ps-rms-Jitter 2.5GHz Digital PLL with 0.7-to-3.5GHz Frequency Range in 90nm CMOS, *Wenjing Yin, Rajesh Inti, Pavan Kumar Hanumolu, Oregon State University*

A digital phase-locked loop (DPLL) employs a linear proportional path, a double integral path, bandwidth and tuning range tracking, and a novel delta-sigma digital to analog converter to achieve low jitter, wide operating range and low power. The prototype DPLL fabricated in a 90nm CMOS process operates from 0.7 to 3.5GHz. At 2.5GHz, the proposed DPLL consumes only 1.6mW power from a 1V supply and achieves 1.6ps and 11.6ps of long-term r.m.s and peak-to-peak jitter, respectively.

4:45
06-7

A 2.4ps Resolution 2.1mW Second-Order Noise-Shaped Time-to-Digital Converter with 3.2ns Range in 1MHz Bandwidth, *Brian Young, Sunwoo Kwon*, Amr Elshazly, Pavan Kumar Hanumolu, Oregon State University, *Dongbu HiTek*

A time-to-digital converter (TDC) employs a phase-reference second-order continuous-time delta-sigma modulator to achieve high resolution and low power. The modulator operates on the phase of the input signal and generates an equivalent noise-shaped one-bit output data stream. Fabricated in an LP 90nm CMOS process, the prototype TDC achieves better than 2.4ps resolution over a 3.2ns range in a 1MHz signal bandwidth while consuming 2.1mW from a 1.2V supply.

5:10
06-8

High-Speed CMOS Ring Oscillators with Low Supply Sensitivity, *Xiaoyan Gui, Michael Green, University of California, Irvine*

A novel circuit topology for CMOS CML ring oscillators that reduces the supply sensitivity is presented. It is shown that this technique causes only a slight reduction in the maximum frequency of the oscillator and maintains the same random jitter generation while greatly reducing the sinusoidal jitter caused by power supply variation. Measurement results from a prototype chip fabricated in 0.18μm CMOS process verify the effectiveness of the proposed technique.

Session 7 – Biomedical Sensors and Systems

Monday Afternoon, September 20
Fir Ballroom

Chair: Ken Szajda, LSI Corporation
Co-Chair: Steve Garverick, Case Western Reserve University

This session covers work that pushes the limit of biosensors and their interface electronics in terms of very low power, extended functionality and high performance.

1:30 **Introduction**

1:35 **Smart CMOS Substrates for Bioelectronic Interfaces: Overview and Trends (INVITED),**
07-1 *Marco Tartagni, University of Bologna*

The paper will overview the recent trends of smart CMOS substrates hosting arrays of biosensor interfaces. It will review figures of merit and will discuss the design trade-offs and the trends with respect to the scaling in both sensing and actuation.

2:25 **A Low-Power Multi-band ECoG/EEG Interface IC,** *Fan Zhang, Apurva Mishra, Andrew G.*
07-2 *Richardson, Stavros Zanos, Brian P. Otis, University of Washington*

We present a 6.4 microwatt core electrocorticography (ECoG)/electroencephalography (EEG) processing integrated circuit with a 0.4 microvolt rms noise floor intended for emerging brain-computer interface applications. This chip conditions the signal and simultaneously extracts energy in four fully-programmable frequency bands. Measured results from in-vivo ECoG recording from the primary motor cortex of an awake monkey are presented.

2:50 **A Programmable Pulse UWB Transmitter with 34% Energy Efficiency for Multichannel**
07-3 **Neuro-Recording Systems,** *Henrique Miranda, Teresa Meng, Stanford University*

This paper describes configurable, 3.6 to 7.5 GHz pulse UWB transmitter IC targeted for neurological implants with high data rate requirements. Each cycle of the RF pulse is digitally programmable in amplitude and duration, enabling a very flexible shaping of the transmitted PSD signal, without the use of an output filter. The transmitter achieves a maximum of 34% of energy efficiency when drawing 8.5 pJ/bit from the supply, with 13 uW of constant static power. This transmitter was implemented in 65nm CMOS and measures 1.0 mm x 0.7 mm. A 32-channel recording experiment using this chip is also reported.

3:15 BREAK

3:30 **An Inside Body Power and Bidirectional Data Transfer IC Module Pair,** *Edward Lee, Alfred*
07-4 *Mann Foundation*

An IC module pair connected with 3 wires was proposed for an implant that consisted of a master unit (MU) and a small, light-weight satellite unit (SU). Power was delivered from the MU to the SU using a 3-phase signal, and converted to DC in the SU by a passive MOS AC-DC converter. Data transfer between the two units was achieved by modulating the amplitudes and the positions of the rising and falling edges of the 3-phase signal. A bidirectional data rate in the range of MB/s and an overall power efficiency of 90.2% for a 3.2mW load were achieved in a 0.18µm CMOS process.

3:55 **192-Channel CMOS Neurochemical Microarray,** *Meisam Honarvar Nazari, Hamed Mazhab-*
07-5 *Jafari, Lian Leng, Axel Guenther, Roman Genov, University of Toronto*

A 16×12-channel neurochemical microarray is presented. Each channel acquires bidirectional currents down to pico-amperes proportional to the concentration of a neurochemical. By combining the current-to-frequency and the single-slope analog-to-digital converter (ADC) 110dB of dynamic range is achieved. The ADC in each channel generates a 16-bit output in less than a millisecond. The microarray with flat and 3D gold electrodes and an on-chip microfluidic network is experimentally validated in in-situ recording of neurotransmitter dopamine.

4:20
07-6

A Frequency-Shift-Based CMOS Magnetic Biosensor with Spatially Uniform Sensor Transducer Gain, *Hua Wang, Constantine Sideris, Ali Hajimiri, California Institute of Technology*

This paper presents a scalable and ultrasensitive magnetic biosensing scheme based on on-chip LC resonance frequency-shifting. The sensor transducer gain is demonstrated as being location-dependent on the sensing surface and proportional to the local polarization magnetic field strength |B|2 generated by the sensing inductor. To improve the gain uniformity, a bowl-shape stacked coil together with floating shimming metal is proposed for the inductor design. As an implementation example, a 16-cell sensor array is designed in a 45nm CMOS process. The spatially uniform sensor gain of the array is verified by testing micron-size magnetic particles randomly placed on the sensing surface. The Correlated-Double-Counting (CDC) noise cancellation scheme is also implemented in the presented design, which achieves a noise suppression of 10.6dB with no power overhead. Overall, the presented sensor demonstrates a dynamic range of at least 85.4dB.

Session 8 – Advanced Wireline Techniques

Monday Afternoon, September 20
Pine Ballroom

Chair: Ed Van Tuijl, Axiom-IC Twente
Co-Chair: Afshin Momtaz, Broadcom

This session presents multi-GHz wireline transceivers, emphasizing equalization, high performance, and low power techniques.

1:30 **Introduction**

1:35
08-1

Gain and Equalization Adaptation to Optimize the Vertical Eye Opening in a Wireline Receiver, *Dustin Dunwell, Anothony Chan Carusone, University of Toronto*

Control signals for an equalizer and variable gain amplifier are optimized by examining the PDF of received data, which is obtained from the DC output of an analog sampler. Measured results show that the adaptation scheme functions correctly over channels of varying lengths at speeds from 2 to 10 Gb/s.

2:00
08-2

Equalizer Design and Performance Trade-offs in ADC-based Serial Links (INVITED), *Jaeha Kim, Jihong Ren,Brian Leibowitz, Patrick Satarzadeh, Ali-Azam Abbasfar, Jared Zerbe, Rambus, Inc.*

This paper analyzes the performance benefit of using non-uniform quantization in ADC-based backplane receivers. The optimal way of placing the ADC quantization thresholds is not what minimizes the quantization error, especially with limited ADC resolution. The proposed reduced-slicer partial-response DFE receiver achieves the BER of 3~4-bit uniform ADCs with only 4 data slicers.

2:50
08-3

A Combined Anti-Aliasing Filter and 2-tap FFE in 65-nm CMOS for 2x Blind 2-10 Gb/s ADC-Based Receivers, *Tina Tahmoureszadeh, Siamak Sarvari, Ali Sheikholeslami, Hirotaka Tamura*, Yasumoto Tomita*, Masaya Kibune*, University of Toronto, *Fujitsu Laboratories Limited*

This paper presents a combined anti-aliasing filter and 2-tap feed-forward equalizer (AAF/FFE) as an analog front-end (AFE) for 2x blind ADC-based receivers. The front-end optimizes the channel/filter characteristics for data-rates of 2-10 Gb/s. The AAF bandwidth scales with the data-rate and the 2-tap FFE is designed without the need for noise-sensitive analog delay cells. The AAF/FFE is implemented in 65-nm CMOS, occupies 0.013 mm^2, and consumes 2.4 mW at 10 Gb/s.

3:15 BREAK

3:30
08-4

A 5Gb/s 2×2 MIMO Crosstalk Cancellation Scheme for High-Speed I/Os, *Taehyoun Oh, Ramesh Harjani, University of Minnesota*

We describe a multiple-input multiple-output crosstalk cancellation (MIMO-XTC) architecture, particularly applicable to single-ended I/O. The MIMO architecture efficiently cancels crosstalk and improves jitter and eye-opening at the same time. A continuous-time prototype design was fabricated using a 130nm CMOS process and occupies 0.03mm^2 of die area. The XTC equalizer performance has been verified for a variety of FR4 channel spacings and data rates. Measured eye diagrams show that the jitter_pp reduces by 67%UI and the vertical eye opening increases by 58.2% at 5Gb/s. The prototype MIMO-XTC circuit consumes 2.8 mW/Gbps/lane which is roughly two times lower than other XTC schemes.

3:55
08-5

A 6Gb/s Receiver With Discrete-Time Based Channel Filtering For Wireline FDM Communications, *Tsutomu Takeya, Kazuhisa Sunaga*, Koichi Yamaguchi*, Hideyuki Sugita*, Yoichi Yoshida, Masayuki Mizuno*, Tadahiro Kuroda, Keio University , *NEC Corporation*

We present a 6Gb/s wireline receiver having frequency division multiplexing (FDM) with four frequency sub-channels. Its discrete-time filter consumes less power than a conventional filter and provides channel filtering of FDM signals. Improved I/Q-based phase detection makes possible low-power symbol-rate clock recovery. The receiver achieves BER<10^-12 over a 25cm low-ε channel, while consuming 250mW from a 1.4V supply.

4:20
08-6

A Slew-Rate Controlled Transmitter to Compensate for the Crosstalk-Induced Jitter of Coupled Microstrip Lines, *Hae-Kang Jung, Soo-Min Lee, Jae-Yoon Sim, Hong-June Park, POSTECH*

A single-ended transmitter eliminates the crosstalk-induced jitter at the receiver by controlling the slew rates of the signal at the transmitter for the even and odd modes of two parallel coupled microstrip lines. The transmitter chip in a 0.18 μm CMOS process reduces the total RX jitter by about 38 ps (53%) for the data rates from 2.6 to 5 Gbps, and increases the horizontal eye-opening (BER < 1E-12) by about 21% at 5 Gbps.

4:45
08-7

Digital Link Pre-emphasis with Dynamic Driver Impedance Modulation, *Ranko Sredojevic, Vladimir Stojanovic, Massachusetts Institute of Technology*

Digital impedance-modulating equalizer overcomes the power overhead of equalization in voltage-mode drivers. Compact, fully-digital RAM-DAC implementation compensates duty-cycle distortion and driver nonlinearity. A 90nm CMOS testchip shows small signal degradation from dynamic modulation of transmitter impedance, achieving 100mV receiver eye with 2pJ/bit at 4Gb/s over wide variety of 20’’ backplanes.

Session 9 - Forum 1
3D Integration Infrastructure

Monday Afternoon, September 20
Cedar Ballroom

Chair: David Sunderland, Boeing Space & Intelligence Systems

Vertically stacked integrated circuits, enabled by Through-Silicon Via (TSV) technology, appear poised to provide significant improvements in density and performance. But is the design, assembly and test infrastructure ready to support this innovation in mainstream products? We explore this issue with four Invited talks.

1:35
9-1

3D Integration Infrastructure: Requirements to Support High Volume Production, *W. R. Bottoms, Third Millennium Test Solutions, Santa Clara, CA*

This presentation reviews the status of 3D technology integration and product development, and discusses a variety of potential "roadblocks" to the adoption of 3D for the mainstream. Meeting the challenges posed by these roadblocks will require new materials, new equipment, new process technologies and even new production flows. The known solutions and the potential solutions in development will be discussed.

2:25
9-2

3D IC – TSV & Micro-bump Modeling and Design Implementation Tools, *Vassilios Gerousis, Cadence, San Jose, CA*

This talk will explore 3D IC physical modeling, physical design methodology and physical design tools. It will first provide the basic modeling features of 3D IC to allow the specification and the integration of multiple chips in either a vertical stack or a silicon interposer. The second part of the talk will focus on design implementation and analysis of the 3D IC interconnect components and how those are integrated in a design flow.

3:30
9-3

3D Packaging Evolution from an OSAT Perspective, *Raj Pendse, STATSChipPAC, Fremont, CA*

This presentation illustrates parallel developments in the three areas of packaging technology, i.e. traditional die and package stacking on substrates, fan-in and fan-out wafer level packaging and 3D Si integration, and the role of the Out-Sourced Assembly and Test (OSAT) industry in supporting this evolution. Latest developments in the key elements of 3D Si integration such as wafer thinning, micro bumping, micro bonding and logical hand off points among Si and package foundries are presented.

4:20
9-4

Challenges and Emerging Solutions for Testing TSV-Based Three-Dimensional Stacked ICs, *Erik Jan Marinissen, IMEC, Leuven, Belgium*

This presentation focuses on the challenges of testing 3D-SICs, and describes for which challenges solutions are already available or emerging. It provides an overview of the manufacturing steps of TSV-based 3D-SICs, as far as relevant for testing. Subsequently, it discusses test flows for wafer probing and packaged-device tests, the challenges with respect to test contents and wafer-level probe access, and the on-chip design-for-test (DFT) infrastructure required for 3D-SICs.